# Galvanically Isolated on Chip Communication

# by Resonant Coupling

by

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# ABSTRACT

Galvanic isolation is used in various applications such as power management circuits and medical equipment. In applications where high voltage DC transients are involved, it is necessary to isolate the high voltage portion of the system from the low voltage side to maintain reliability and/or safety requirements. But, most applications require communication between the low voltage and high voltage circuits, thus presenting a challenge to pass information through an isolation barrier.

A concern in high-voltage gate drivers is when the middle point of the half-bridge falls below ground during a low-side switching occurrence. The negative voltage causes minority carrier injected to the substrate that travels into low voltage circuitry, such as the control circuit, and causes voltage shift or latch-up. Isolating the high side driver from the low voltage circuits can prevent the injected carriers from traveling to low side circuits. But, the control circuits must communicate to the high-side circuits, making it necessary to provide coupling to transmit the signal over the galvanically isolated barrier.

In this research, a novel galvanic isolation method using magnetic coupled on-chip resonators has been proposed. Utilizing adjacently placed magnetically coupled resonators provides 1) high voltage galvanic isolation using the gaps between resonators filled with oxide and 2) magnetic coupling for signal transfer over these gaps. An OOK method has been used as the digital modulation scheme, which is upconverted to RF frequencies to pass through the galvanic isolator. The presented design is completely integrated on a silicon technology and occupies a small on chip area. The design is low-cost, without requiring exotic packaging, and has a competitive communication

performance, with a propagation delay of 12ns and a minimum high-voltage isolation of 700V.

The design has been fabricated in a silicon 250 nm process and verified through both simulation and measurements. Results show good correlation between theoretical evaluation, simulation, and measurement.

To My Parents

Fariba and Mahmoud

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# CHAPTER 1

# INTRODUCTION

## 1.1 Statement of the Problem

Galvanic isolation is used in various applications such as power management circuits and medical equipment [1]. In applications where high voltage DC transients are involved, it is necessary to isolate the high voltage portion of the system from the low voltage side to maintain reliability and/or safety requirements. But, most applications require communication between the low voltage and high voltage circuits, thus presenting a challenge to pass information through an isolation barrier.

Half-bridge circuit drivers for power management circuits are one application for galvanic isolation. Figure 1-1 shows a half-bridge circuit with gate drive and control circuits, where the high side driver is galvaically isolated from the low voltage circuits. A concern in high voltage gate drivers that do not have galvanic isolation is that during a low side switching occurance, the half bridge's middle point has a floating voltage that will drop below ground due to parasitic or existense of an inductive load. This negative voltage causes minority carrier injection to the substrate of the high side gate driver. If this gate driver is not isolated from the rest of the low voltage circuits, these minority carriers can travel to low voltage circuits, creating latch-up and voltage shifts that degrade system reliability [2].

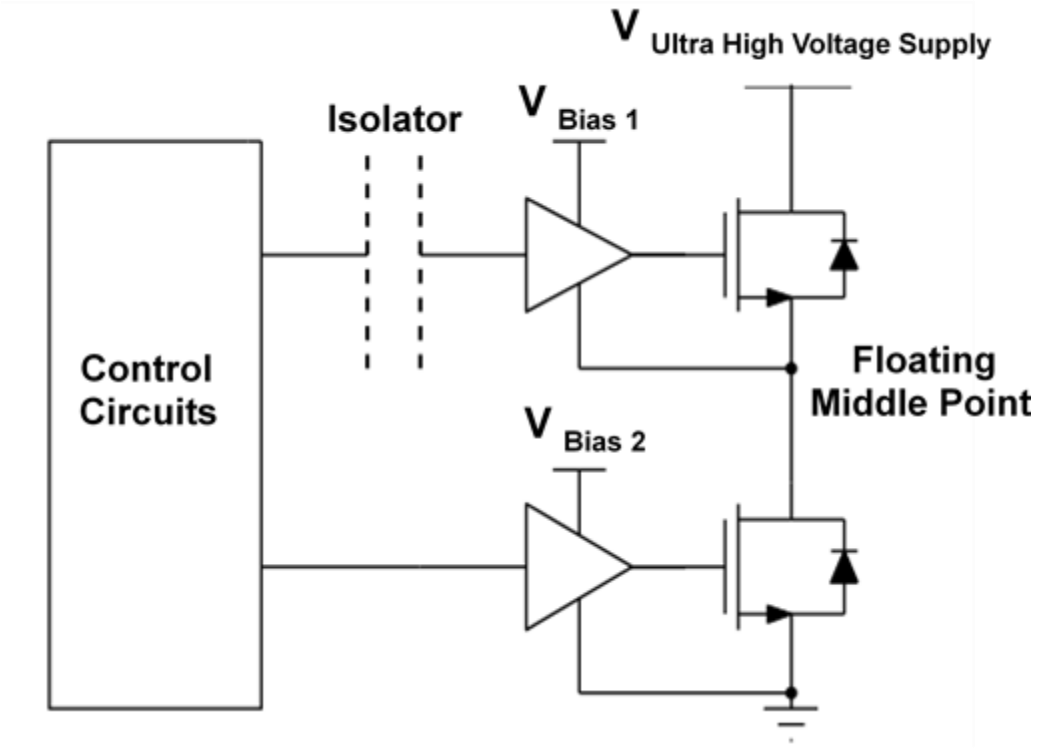



Figure 1-1 Galvanically Isolated Half Bridge Circuit

Separation and substrate isolation of the high side driver from the low voltage circuits can prevent the injected carriers from traveling to the low voltage circuits. However, the high side driver must be able to receive a command signal from the control circuits, making it necessary to have a coupling technique to transmit the control signal across the isolation barrier created between the high side driver and the low voltage circuits. The objective of this work was to create an integrated galvanic isolation barrier with resonant couplers to allow for command signals to control low side and high side gate drivers.

## 1.2 Significance and Motivations of the Study

Increasing demand for integrated galvanic isolation solutions is arising from the ever-increasing levels of integration in power electronic components. To-date, four of the most popular galvanic coupling methods are: opto-couplers, isolation transformers, on-chip capacitive coupling, and giant magneto resistance. Aside from a few works using multi-chip butterfly resonators and exotic (sapphire) material [3] [4] [5], magnetically coupled resonators have not been thoroughly investigated for galvanic isolation prior to this research.

This study has demonstrated an on-chip galvanic isolation technology capable of ultra-high voltage isolation for a high-side gate driver of a half-bridge circuit. The developed system communicates across the galvanically isolated barrier, from the low-side chip to the high-side chip. The solution is low cost, occupies a small area, and uses standard silicon processes with a maximum of four metal layers. The system shows competitive communication performance, including short propagation delay and high CMTI (Common Mode Transient Immunity).

The presented architecture uses on chip adjacent resonator loops consisting of an inductor, formed by a loop of metal, in series with a metal-insulator-metal (MIM) capacitor. These adjacent resonator loops are separated from each other using the chip's oxide as insulation material to provide the high voltage isolation. When connected to an oscillator on the low side chip and a receiver on the high side chip, this communication channel can deliver a signal from across the galvanically isolated chips. The design also uses an on chip transformer to reduce attenuation on the propagating RF signal.

## 1.3 Research Questions

This research addresses the following design implementation questions for on-chip galvanic coupling:

1- Is it feasible to use adjacently coupled resonators for communication on a standard CMOS technology without exotic materials or complex packaging technologies?
2- Can a system be designed with minimal voltage attenuation to ensure that it is compatible with a standard receiver‘s sensitivity?
3- Do the designed galvanic isolator and communication channel have predictable performance in simulation?
4- How well does the galvanic isolator perform over all process variations?

## 1.4 Organization of the Thesis

In Chapter 2 of the thesis, an overview of galvanic isolation applications is given, and the performance metrics for the implemented design are summarized. Chapter 3 introduces the theory of the presented design approach, and Chapter 4 details the presented system’s silicon implementation and simulation results. Chapter 5 describes the lumped element equivalent models developed to allow for transient simulations of the communication channel. Chapter 6 presents the measurement results, including a discussion on the accuracy of the EM simulations and lumped element models compared to measurement results. The final chapter contains the concluding remarks.

# CHAPTER 2

# BACKGROUND

## 2.1 Galvanic Isolation

The word galvanic means “of or relating to direct-current electricity” [6]. Galvanic isolation means to provide direct current (DC) isolation [7]. However, blocking the DC currents does not mean blocking the information flow across an isolation barrier. This is important because information is usually required to flow between two isolated parts in an electrical system [8]. For this reason, different methods have been developed to enable signaling from the primary side of the isolator to the secondary side. These are known as coupling methods. Figure 6-1 illustrates the galvanic coupling concept, demonstrating that galvanic couplers block DC current flow, while still allowing the information signals to pass.

In this chapter, motivations and applications of galvanic isolation and communication across a galvanic barrier are explained. Finally, the key performance parameters of an isolator and different coupling methods for galvanic isolation are introduced.

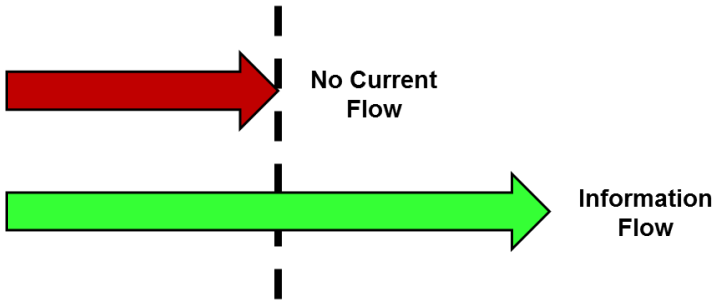



Figure 2-1 Galvanic Coupling Concept

## 2.2 Motivations for Galvanic Isolation

Galvanic isolation can be used in various applications that have high safety requirements, such as medical equipment, network equipment, and power monitoring. This study targets applications for half-bridge (switching converter) power management circuits. As explained in Chapter 1, below ground voltage is a problematic phenomenon when using ultra high voltages supplies. It has been proven that substrate minority carrier injection can cause voltage shift and latch up [2].

Figure 2-2 shows a conceptual schematic of an N- type region from a high side driver and an N-type region from the low voltage circuitries fabricated on a common P-type substrate. When the middle point falls below ground, the PN junction between substrate and the high voltage circuit's N-region will become forward biased, causing minority carriers (electrons) to flow through the substrate. At the same time, the N-region from the low voltage circuits is connected to a positive voltage, thus forming an NPN BJT where the low voltage region acts as a collector and the portion of the electrons that are not recombined in the substrate travel to the low voltage region. The n-regions on a positive potential, e.g. those of the controlling circuitry, collect minority carriers, which can disturb the circuits' functionalities [2]. In addition, the substrate electron injection can lead to a shift in substrate voltage potential, hence triggering a latch-up [2].

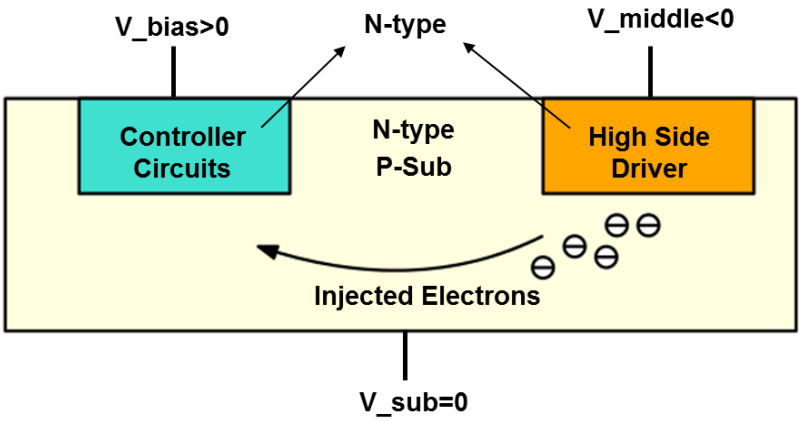



Figure 2-2 Substrate Minority Carrier Injection


Figure 2-3 Separated Chips

To prevent substrate minority carrier injection, the high side driver and controller circuitry can be separated, as shown in Figure 2-3. This will prevent the electrons from traveling to the low voltage circuits, but the controller circuits are not enable to command or communicate with the high voltage circuits. To solve the communication problem, a solution is developed to enable signaling from the low side chip to the high side chip. A galvanic isolator can be used to make die-to-die communication possible, while preventing high voltages from appearing on the low side circuitry.

## 2.3 Significant Parameter of Isolators

The key parameters for an isolator are: its voltage isolation rating, which points to the RMS value of the highest voltage that the product can reliably isolate, and propagation delay, which gives the time period required for an isolator input event to propagate to the isolator output. Common mode transient immunity (CMTI) is an important parameter in isolators used for half-bridge drivers because a rapidly changing voltage transient can cause bit errors once communicated across the barrier [9].

### 2.3.1 Opto-couplers

Opto-couplers consist of a light-emitting device (e.g. an LED) and a light sensor. Current flowing through the LED causes emitting light to strike the photo detector, and upon the reception of the light signal by the photo detector, the signaling is complete [10]. When the space between the photo detector and light emitter is filled with a transparent isolating material, it can be used as a galvanic isolator. Since opto-couplers use light for signaling, they may have considerable distance (e.g. 1 mm [10]) between their transmitters and receivers, allowing for a thicker isolation material and high isolation ratings. However, opto-couplers can be toned to operate at high current levels, which will increase power consumption and also reduce lifetime [9]. Furthermore, the opto-couplers suffer from low integration levels because 1) opto-couplers are fabricated with GaAs technologies that cannot be integrated with silicon-based active circuits, and 2) discrete opto-coupler chips are required for optical separation among multiple isolation channels [11].

### 2.3.2 Capacitive Coupling

Capacitive coupling uses capacitors as the isolation barrier. This capacitor blocks the DC signals and current and can perform communication by passing an RF signal. However, they have limitations on CMTI and size [12]. Signaling through capacitors is a single-ended communication and in presence of noise, the signal becomes corrupted. To overcome the noise problem, two capacitors can be used to create a differential signal [13] [14]. Moreover, the isolation capacitors must have high isolation reliability, requiring development of high voltage capacitors. In [1], a capacitive galvanic isolator has been reported that is 2 times better than the previous literature. However, it has been done using a silicon-on-sapphire technology.

### 2.3.3 Transformers

Transformers use magnetic coupling to transfer a signal from the primary coil to secondary coil. When the space between the coils filled with high reliability dielectric, they can provide high voltage galvanic isolation. Transformers are differential devices and have the benefit from a good CMTI. Additionally, they can be implemented on standard silicon CMOS. Various techniques for implementing galvanic isolators have been used. In [15] and [16], transformer isolators have been reported using standard CMOS with a polyamide isolator material. On-chip transformer isolators have been developed with 1) interlayer die-electric material in CMOS and 2) die attach fill (DAF) and passivation layers in CMOS [17]. The benefit of using interlayer dielectric is that it does not require special packaging and there isn't misalignment between the coils to cause degraded coil coupling. But, the interlayer dielectric insulation voltage rating is limited by the thickness of the process dielectric [11] .In [18], a novel method for

transformer coupling is demonstrated with 3D through-silicon via (TSV) technology to eliminate bondwires between face-to-face coupling chips.

### 2.3.4 Giant Magnetoresistance (GMR)

Giant magnetoresistance is a quantum mechanical magnetoresistance effect observed in thin films, which is observed as a significant change in electrical resistance depending on parallel or anti-parallel alignment of the thin film's Ferro-magnetic layers [19]. This characteristic makes GMRs a candidate for coupling across a galvanic isolation barrier. Upon generation of magnetic field through a planar coil winding, the GMR senses the magnetic field and sends a signal to the circuit's output [20]. GMR isolators may have small propagation delays, small size, and high voltage isolation ratings. But, implementation requires complex, high-cost GMR technology development and materials.

### 2.3.5 Resonators

In [3], [4], and [5], a galvanic isolator for a gate driver is implemented in a GaN on sapphire substrate with a butterfly coupler architecture. High voltage isolation and good data rate has been achieved, but the design requires an expensive sapphire isolation material.

# CHAPTER 3

# GALVANIC ISOLATION USING MAGNETIC COUPLED RESONATORS

## 3.1 Introduction

In Chapter 2, various coupling methods for communication across a galvanically isolated barrier have been summarized. This Chapter explains the fundamental concepts and system architecture for this work. The presented architecture enables RF signaling across an isolation barrier. This chapter explains how magnetically coupled resonators provide die to die communication between galvanically isolated dies, as well as the challenges for on chip implementation. Metrics for performance and verification of the presented design have also been explained.

## 3.2 Fundamental Overview

Figure 3-1 (a) shows a schematic of two mutually coupled inductor loops, separated from each other by a dielectric gap. The gap behaves like a capacitor and can withstand high break down voltages when filled with proper dielectric, providing galvanic isolation and therefore blocking DC currents between the two inductors.

Utilizing an oscillator connected to the primary loop generates an RF voltage and the flux linkage between the two loops induces an RF signal in the secondary loop that is detected by a receiver circuit. This makes the communication between two loops possible. However, it is crucial to have enough coupling between the loops due to the finite receiver sensitivity. Reduction of the distance between the loops can improve the coupling. However, a decrease in the distance means lower isolation voltage, as:

$$E_{Breakdown} = \frac{V_{Breakdown}}{t_{dielectric}}$$

Where $t_{dielectric}$ is the dielectric thickness and $E_{Breakdown}$ is the breakdown electric field, which varies based on the dielectric material. One method to enhance the performance, in terms of energy transfer, is to resonate the inductor loops. This idea is also being used in wireless power transfer (WPT) systems to improve the power transfer efficiency between transmitter and receiver coils that are distanced from each other. Figure 3-1 (b) shows the system discussed in Figure 3-1 (a) with capacitors added in parallel to the inductors in order to generate a resonance. Each loop has a resonant frequency $f_0 = 1/(2\pi\sqrt{LC})$ [21]. However, it can be shown that mutual coupling splits the resonant frequency of the two loops into two frequencies, one higher and one lower than $f_0$ [16]. The capacitor and inductor values can be tuned to achieve the maximum voltage around the targeted operation frequency.

With help of the resonance, a voltage builds up in the receiver loop that is higher than the non-resonance circuit of Figure 3-1 (a), where all the transferred energy would have been dissipated in the resistance of the inductor loop.

### 3.3 System Architecture

The resonant coupling concept in Section 3.2 has been implemented to provide galvanic isolation. The schematic in Figure 3-2 demonstrates the galvanic isolator using resonant coupling. The designed system consists of two chips. The “Low Side” chip is defined as the portion of the system that contains the low voltage circuitry, such as control circuits and low side gate driver of a switching load (e.g. half-bridge circuits).

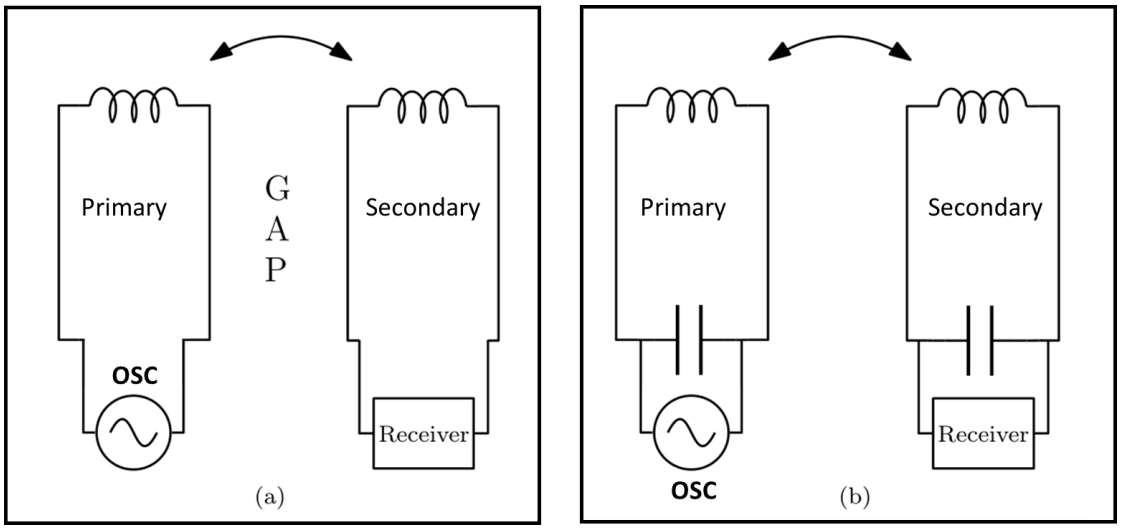



Figure 3-1(a) Non-resonant Coupled Inductors, and (b) Resonant Coupled Inductors

The Low Side chip is referenced to ground. The "High Side" chip is defined as the portion of the isolator connected to the high voltage circuits with a "floating ground" (half-bridge middle point) or reference point. The high side gate driver would be located on the High Side chip. Both chips include digital and analog circuits that help with modulating, transmitting, and receiving a signal across the isolation. The passive portion of the system starting from the input of Loop1 to the differential outputs of the transformer will be referred to as the communication channel.

As Figure 3-2 indicates, the oscillator generates an RF voltage in Loop 1, magnetic coupling induces an RF voltage in Loop 2, and then the signal is transferred from Loop 2 to an inductor connected to two bond pads. Bond wires transfer the signal from the low side chip to the high side chip. The RF signal is transferred from the bond pads to Loop 3 through magnetic coupling and then from Loop3 to an inductive loop that magnetically couples the signal to the primary of a center tapped step-up transformer. The output of the transformer delivers a differential signal to the receiver.

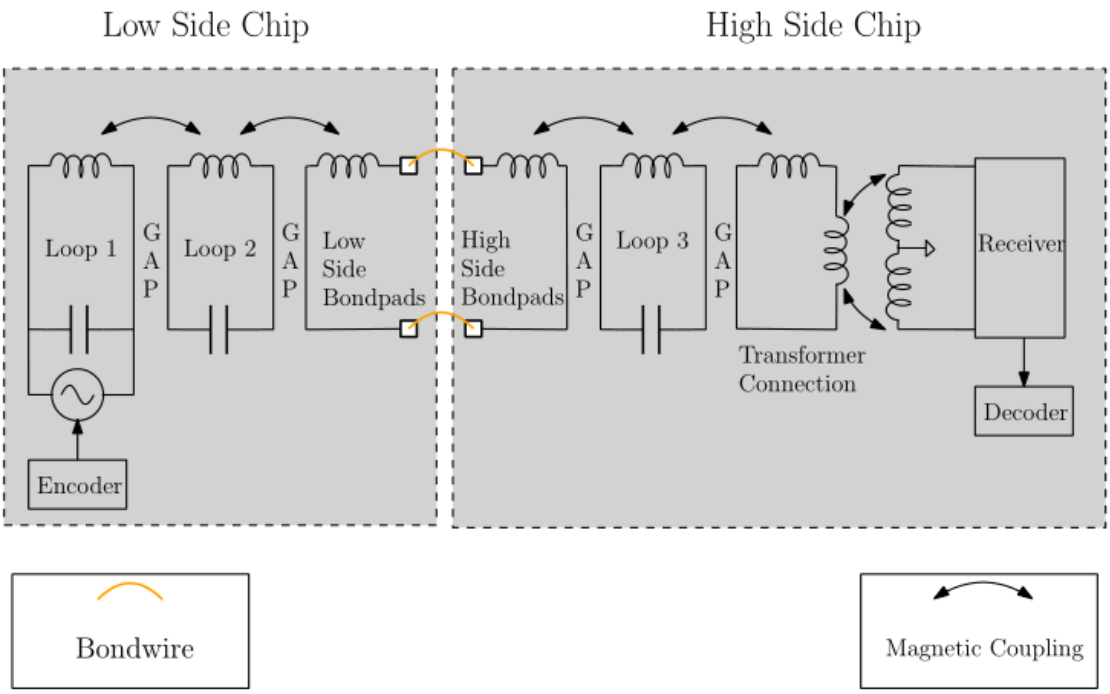



Figure 3-2 System Topology

It is also worth mentioning that resonator loops 2 and 3 function as repeaters. Adding each repeater increases the number of Gaps by one, enhancing the isolation capability and reliability. This means that instead of adding distance between the magnetically coupled elements, which attenuates the coupling, keeping the gap width to a minimum and increasing the number of gaps can improve isolation. This method has considerably less effect on the communication performance and voltage gain from the low side oscillator to the high side receiver's input.

It is also valuable to highlight the motivations for implementing the transformer. The RF signal generated at the oscillator is attenuated when transferred from one coupled section to another, and also has significant attenuation over the bondwires. This brings the RF signal to a level below the receiver's sensitivity, if a transformer is not implemented. The transformer steps up the voltage to solve this problem, while

increasing the number of gaps by one (the gap between primary and secondary) and making the output voltage differential in reference with the high side's floating 'ground'. Figure 1-1 illustrates that the center tap is connected to the floating ground. This floating ground comes from the middle point of the half bridge (high side gate driver's ground reference). The outputs of the transformer connect to a differential receiver, which rejects the common mode signals, thus improving the common mode transient immunity (CMTI).

When implemented on chip, the Gaps will be filled by oxide to form a capacitor. Silicon Oxide has a minimum breakdown voltage of approximately 600 V/um. During a DC transient on the middle point of the half-bridge circuit, the gaps will perform galvanic isolation between the power stage and the silicon-based circuitry.

Silicon Oxide gaps are used instead of metal-insulator-metal (MIM) capacitors because the dielectric thickness of MIM capacitors is generally thin in contrast with the gaps that may have microns of thickness. Therefore, the breakdown voltage of MIM capacitors is considerably lower than oxide gaps, and MIM capacitors are not a reliable option for ultra-high voltage isolation. Each of the gaps in the presented architecture (3 um) is capable of more than 1 kV, while not more than 15 V is generally allowed over MIM capacitors in silicon-based processes [22].

With successful communication of an RF signal from Low Side to High Side, an encoder on the input and output is introduced to encode a digital signal on the Low Side and decode it on the High Side to reproduce the same binary [digital] signal. Utilizing On-Off Keying (OOK) modulation scheme, the encoder can process a digital input code, by turning on the normally off oscillator for a time length of t1 on the rising edge and t2

for a falling edge, the decoder on the output can decode and reproduce the same digital signal with respect to the detected oscillation time lengths.

### 3.4 Technology

ONBCD25 has been used to implement the system on chip. ONBCD25 is 0.25μm silicon BCD (Bipolar-CMOS-DMOS) technology from ON semiconductor. It has four metal layers, including a 3μm thickness top metal layer, two 0.94μm metal layers, and a 0.64μm for the bottom metal layer. The process includes MIM capacitors and low-loss resistors. A detailed description of the process can be found in [22].

### 3.5 Performance Metrics

Key considerations for designing a galvanic isolator have been highlighted in Chapter 2. Table 3-1 shows the key design specifications for this work.

Table 3-1 Design Specification

| Specification Name | Value | Unit |
|---|---|---|
| Minimum Isolation | 700 | V |
| Maximum Propagation Delay | 15 | ns |
| Maximum Digital Input Frequency | 500 | kHz |
| Maximum Die Area | 1 | mm2 |
| Minimum Voltage Gain expected from Communication Channel | 0.1 | V/V |
| Design Frequency | 2.8 | GHz |

## 3.6 Design and Performance Verification Metrics

It is of paramount importance to review the steps that have been taken to convert the proposed concept in the beginning of this chapter to an implementable design and a successfully fabricated chip. The design and verification procedures are explained in this section.

### 3.6.1 EM Simulation and Visualization

Upon completion of the initial physical layout of the communication channel, importing it to a Full wave EM simulator makes it possible to predict the system's RF behavior. The EM software simulates the 2.5D passive structures using MOM (method of moments) [23], and generates S-parameter models (.snp files where n is number of the ports on the simulated structure) that can be imported to circuit and system simulators, such as Cadence, MATLAB, or ADS schematic.

An RF system simulator provides options to analyze and visualize various key parameters such as S, Y, and Z parameters, while equation based variables that are functions of these parameters can also be introduced to visualize parameters such as voltage gain, resonance frequency, capacitance, inductance, etc. It also gives the user options such as tuning, performance optimization, and bondwire modeling. Design parameters can be modified to achieve best expected performance using tuning and optimization tools in schematic and layout modifications. After meeting the communication channel's design requirements (especially the voltage gain requirement), the .snp files are imported to a circuit simulator tool to simulate the active portions of the design, including the receiver and oscillator.

### 3.6.2 Circuit and System Simulation

The circuit simulator (e.g. Cadence) has the models for the active devices of the system. Therefore, the entire isolator system is simulated in a SPICE-based software. Simulations verify the successful generation, transmission, and reception of the RF signal. Some design modifications take place during this phase. Upon achieving satisfactory results from the simulations, the layout of the design is completed by drawing the active circuits' layout and integrating them with the overall communication channel. At this point, the layout is re-simulated in the EM simulator to include all connecting metals between the transistor circuits and passive communication channel structures. A final tuning for the communication channel can be done in this phase and values for connections' inductance and resistance can be extracted and added to the circuit in the SPICE simulator. Multiple iterations between the SPICE-based circuit simulator, EM simulator, and RF system simulator are necessary to achieve the expected performance.

Multiple test structures have been fabricated on silicon, including the passives and actives, where the passive structures are compatible with on-chip RF probing. In addition, on-chip de-embedding structures have been fabricated to increase the measurement accuracy.

All of the passives have been measured on an RF probe-station using a Programmable Network Analyzer (PNA). A MATLAB code has been developed to de-embed the measurement results, using the de-embedding structures' measurement data. Comparison between the results from measurements and simulations show good correlation between the measured and expected performance.

### 3.6.3 Verifying the Isolation Capabilities

For full system simulation, a .snp file is imported to the circuit simulator. But, transient simulations based on the S-parameter models leads to conversion errors and inaccuracy, especially when performing high voltage transient simulations. To solve this problem, a lumped element model has been developed. Utilizing the lumped element model, transient simulations demonstrate the distribution of the high voltage transients over the silicon oxide gaps, thus making it possible to predict the communication channel's voltage rating of isolation.

### 3.6.4 Optimization for the Next Tapeout

Having a lumped element that is tailored for measurement results enables transient simulations in a SPICE-based simulator with higher level of accuracy, thus allowing the receiver circuit to be tweaked/redesigned according to measurement results from the first tape-out.

# CHAPTER 4

# ISOLATOR BUILDING BLOCKS

The fundamental concepts and system architecture described in Chapter 3 have been prototyped with an integrated die-to-die communication channel. This chapter explains the implemented design and presents simulation results that prove the design functionality and communication performance.

Fig 4-1 shows the layout of the implemented communication channel, with the high side and low side boundary shown as a dashed line. Bondwires connect the two silicon chips together. Each block of the system is explained in detail with respect to its design and implementation challenges.

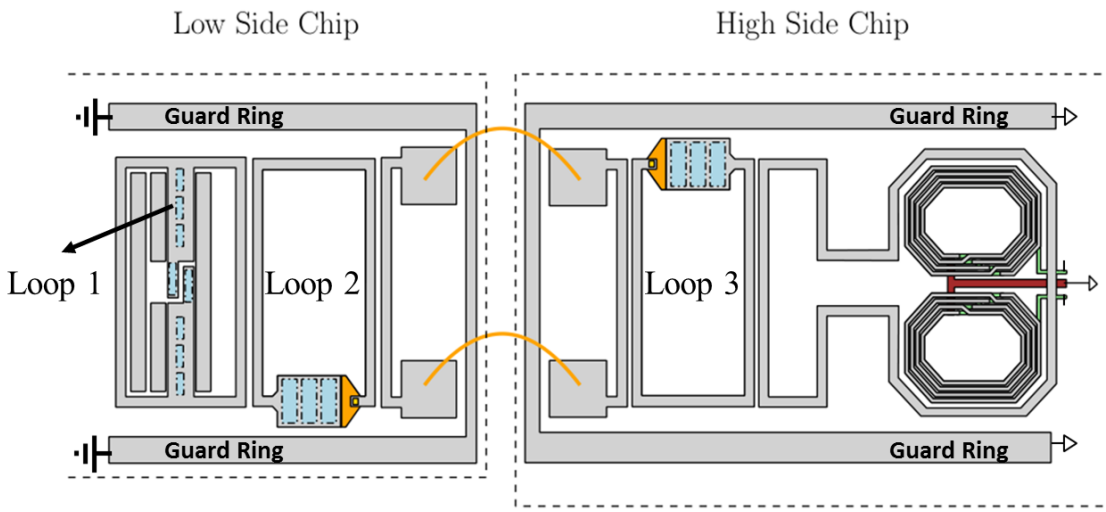



Figure 4-1 Implemented Communication Channel

## 4.1 Fundamental Resonator

Figure 4-2 shows both the layout of the LC resonator and its equivalent circuit model. This is the on-chip layout of the repeaters discussed in the previous chapter, labeled as Loop 1 and Loop 3. A resistor in series with the inductor has been added to account for the sheet resistance (finite quality factor) of the metal loop.

The resonator consists of a transmission line loop in the top metal layer, which generates the inductance, and a Metal-Insulator-Metal (MIM) capacitor in series with the loop. The MIM capacitor consists of two metal plates, where the top plate is the topmost layer metal, and the bottom plate is the metal layer one level below. The bottom plate of the capacitor is connected to the inductor loop through a via array.

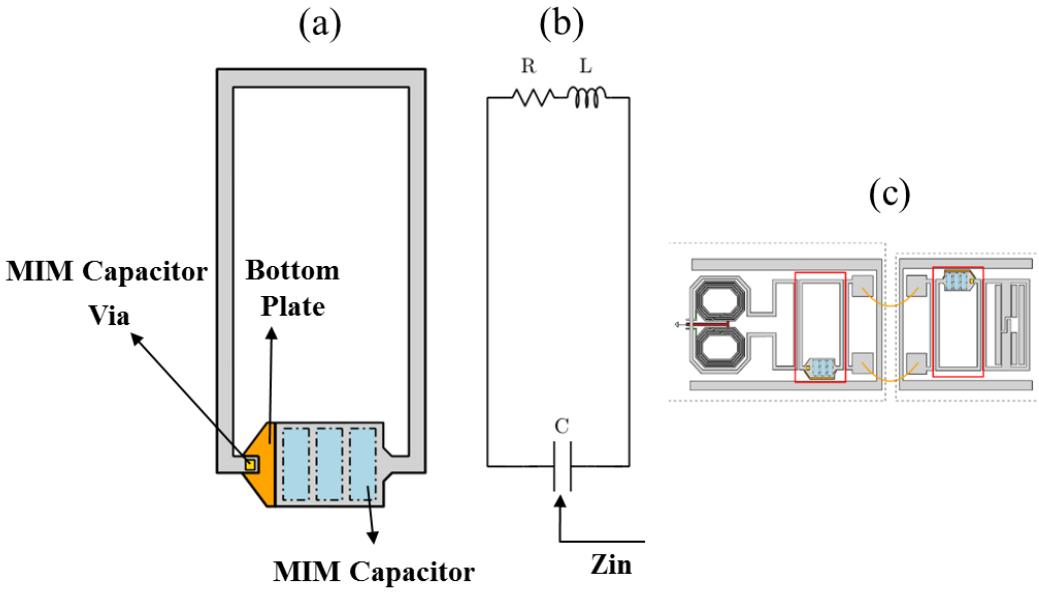



Figure 4-2 Fundamental Resonator (a) Layout, (b) Equivalent Model, and (c) Location in the System's Layout.

It is proven that the resonance frequency looking into the capacitor in parallel with the inductance loop can be found as [20]:

$$\omega_0 = \left(\frac{1}{LC} - \frac{R^2}{L^2}\right)^{\frac{1}{2}} \quad (4\text{-}1)$$

According to [20], for a Q>10, equation 4-1 can be estimated as $\omega_0 = 1/\sqrt{LC}$, where $Q = \frac{\omega_0 L}{R}$.

When at resonance, the input impedance will be a resistance (a real impedance) equal to $Z_{in\_resonance}$, where:

$$Z_{in\_resonanace} = R(Q^2 + 1) \quad (4\text{-}2)$$

In the case of an ideal LC resonator, the input impedance at resonance will be equal to infinity or an open circuit; however, in the non-ideal case, the resistance at resonance is approximately the DC resistance of the inductor multiplied by the squared of Q, which is usually a large number (for a Q of 10, R will be multiplied by a factor of 100). When the loop is used as an LC tank for creating a negative conductance oscillator, a high Q creates a low input conductance that is easier to compensate with an active circuit.

The layout structure shown in Figure 4-2 b has been simulated in an EM software, and the values of R, L and C have been optimized. The circuit model and EM software simulations enable optimization for R, L and C with reasonable accuracy. Figure 4-3 shows good correlation between the simulation results from both EM and equivalent model simulation. At the resonance frequency the real part converges to a value that can be calculated from equation 4-2 ($R_{RESONANCE}$) and the imaginary part becomes zero. The extracted values of R, L and C are displayed in Table 4-1.

Table 4-1 Fundamental Resonator Properties

| Parameter | Value | Unit |
|---|---|---|
| R | 1.345 | Ohm |
| L | 588.808 | pH |
| C | 5.602 | pF |
| $R_{Resonance}$ | 75.624 | Ohm |
| Q | 7.371 | - |
| $f_{Resonance}$ | 2.748 | GHz |

It is important to note that the layout of Loop 1 and Loop 3 are not identical, as the layout of Loop 3 includes metal connections to the oscillator. The differences between these loops are explained in the oscillator design section.

### 4.2 Oscillator

The circuit diagram for the active portion of the oscillator is shown in Fig 4-4. The oscillator uses a PMOS-NMOS cross-coupled pair in order to generate negative conductance, compensating the input conductance seen from the output LC tank. When using an NMOS cross coupled or PMOS cross coupled pair, the conductance looking into the output pair will be equal to $-\frac{g_{mn}}{2}$ or $-\frac{g_{mp}}{2}$, respectively [24] [25]. Using an NMOS-PMOS has the advantage of increasing the output conductance to a value of [25]:

$$G_{out} = -\frac{g_{mp}}{2} - \frac{g_{mn}}{2} \tag{4-3}$$

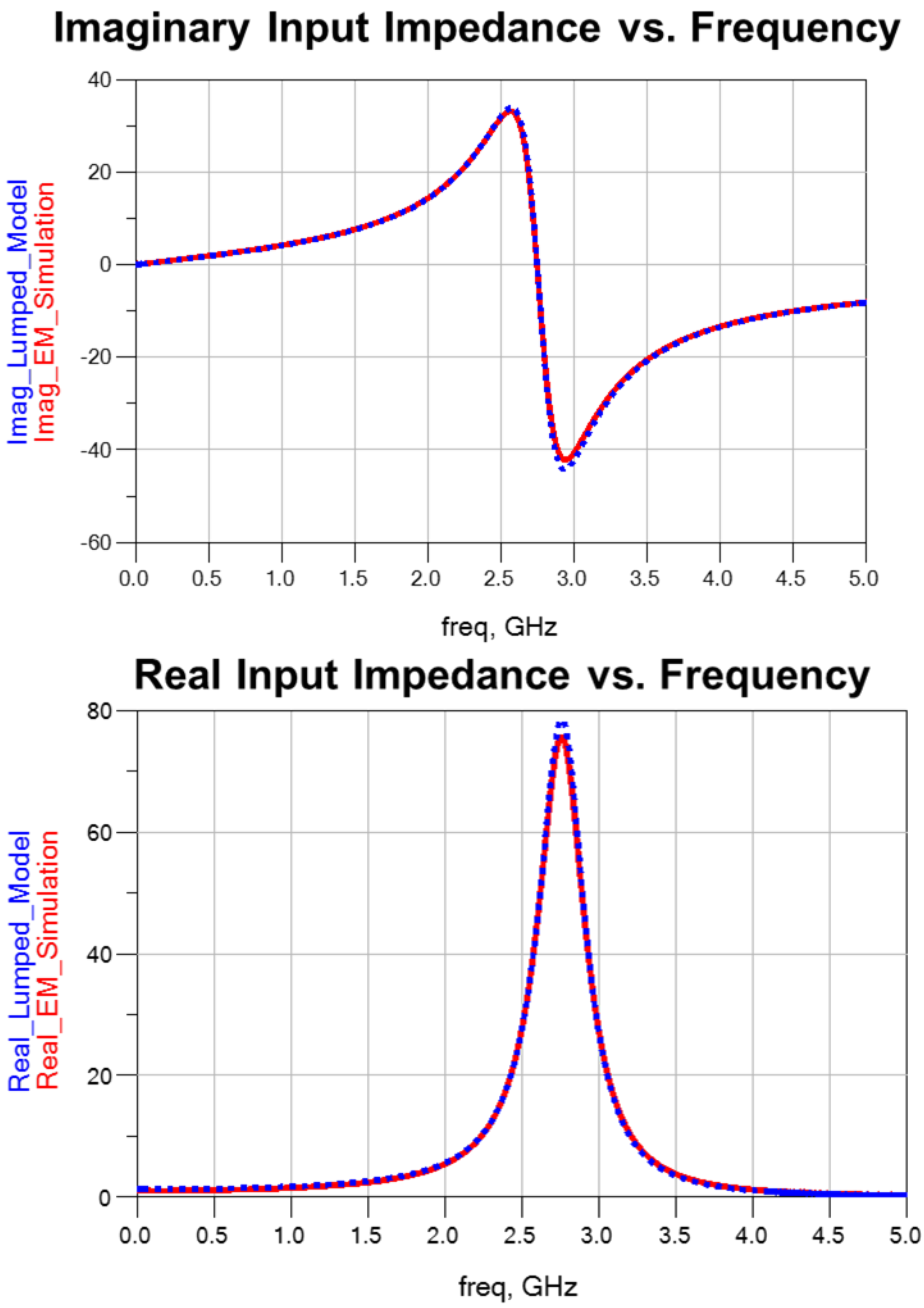



Figure 4-3 Simulation Results for Input Impedance of Fundamental Resonator. (top) Imaginary Impedance vs. Frequency, and (bottom) Real Impedance vs. Frequency.

which is the sum of the conductance of the NMOS pair (M3-M4) and PMOS (M1-M2) pair connected in parallel. A current bias switch (M5-M6) is implemented in the sources of the NMOS pairs to turn the oscillator on and off. The switches' control signal comes from the encoder circuit, which is a digital circuit that detects the rising and falling edges of the digital command signal and translates them into pulses with pulse widths of t_rise and t_fall, where t_rise is not equal to t_fall. This coded signal turns on the normally off oscillator for time lengths of the applied pulse width.

In order to minimize die area, significant effort was put into integrating the active part of the oscillator below its passive LC tank (resonator loop). Both the MIM capacitors and the four cross-couple transistors' parasitic capacitors are the other major source of capacitance within the LC tank. Figure 4-5 (a) shows the inductance loop for the oscillator. The outer loop size of Loop 1 is identical to Loop 2 and Loop 3 from Figure 4-2 (a), however two metal branches are added to connect the oscillator's output devices (M1 through M4) to this loop. The equivalent inductance seen from the output of the oscillator is equal to the inductance of the half loops in parallel, in addition to the inductances coming from the metals connecting the loop to the active circuit. A total capacitance of 15.94 pF is needed for the oscillator to operate at the optimum frequency (2.8 GHz). The output capacitance of the active core is determined to be 10.00 pF from SPICE simulations, so the remaining 5.94 pF is implemented as MIM capacitors between the positive and negative outputs of the oscillator. The blue boxes with dashed boundaries in Figure 4-5 (a) show the MIM capacitors located under the metal connections.

In addition to the metals that connect the oscillator's transistors to the LC tank, there are additional metal connections that are a part of the active core's layout (such as

metals connecting M4's source to M6's drain) and affect the system's performance. Figure 4-5 (b) shows the loop with the top metal layer connecting the active core to the LC tank including additional metals.

Figure 4-6 plots the EM simulations for the structure shown in Figure 4-5 (b). It can be seen that the real part of the input impedance looking into the oscillator's tank (disconnected from active core) peaks at its resonance frequency (2.845 GHz) to a value of 22.5 Ohms, and the imaginary part becomes zero.

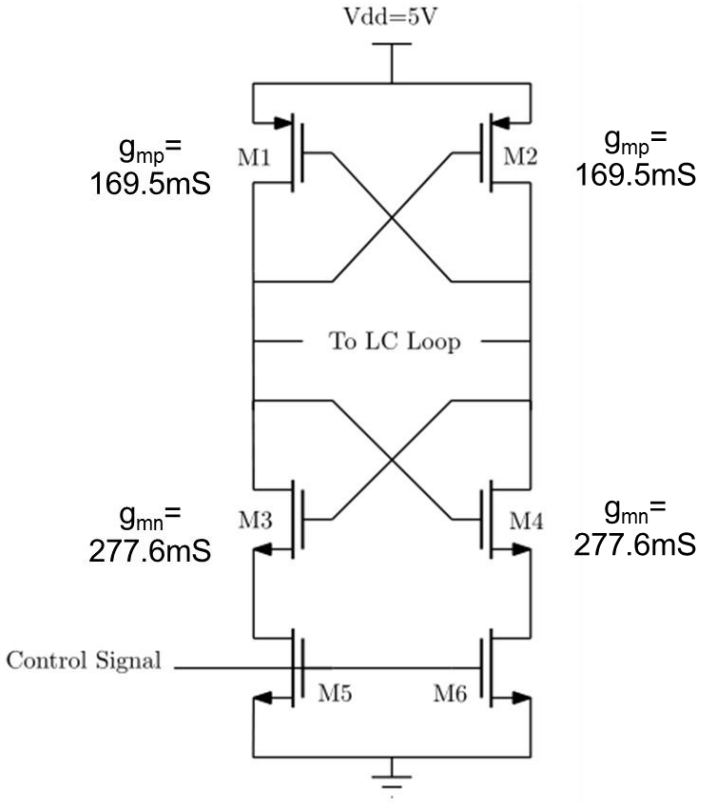



Figure 4-4 Oscillator Circuit Diagram

The impedance seen from the active circuit's output is not only the impedance of Loop 1, but since Loop 1 is magnetically coupled to Loop 2, Loop 2 also loads Loop 1

and slightly shifts the resonance frequency to lower frequencies. Therefore, the input impedance of the resonance tank resonates at a frequency slightly higher than 2.8 GHz, but it will be shifted to lower frequencies when operating within the overall system. The capacitor values have been chosen through optimization within the total system for achieving the maximum voltage gain for the communication channel.

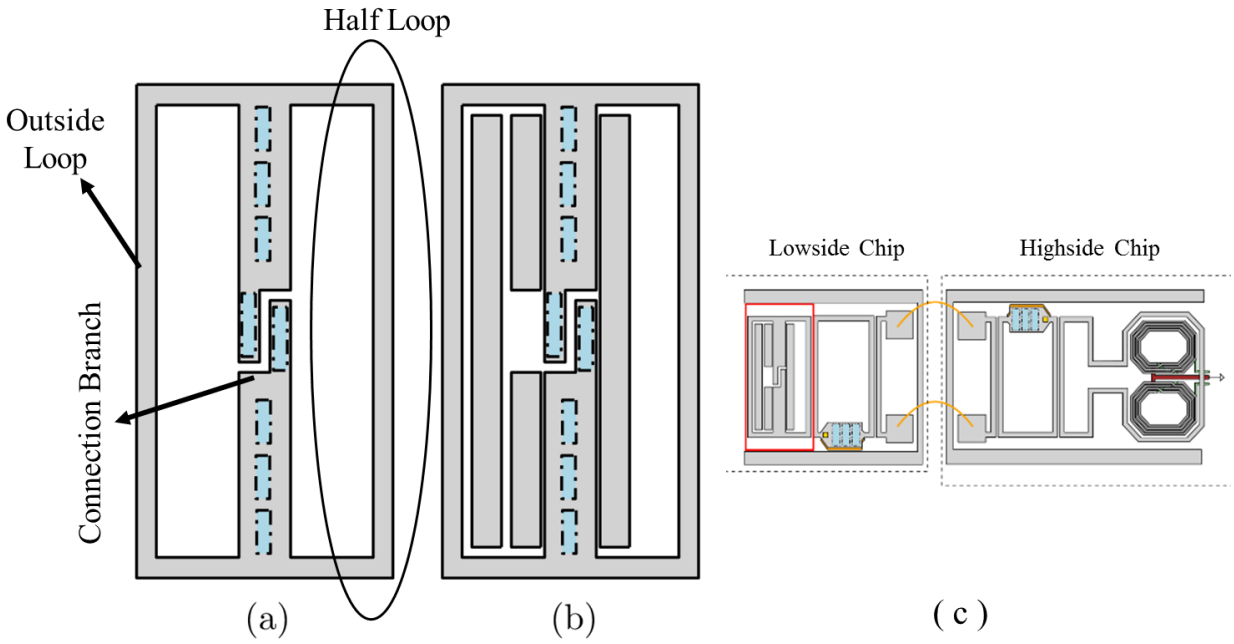



Figure 4-5 Oscillator's LC Loop (a) without and (b) with Connection Metals from the Active Core Layout, and (c) Location within the Overall System Layout.

Table 4-2 Oscillator Performance Parameters

| Parameter | Value |
|---|---|
| **$G_{out}$ @ 2.74 GHz** | -0.17 |
| **Min Expected $G_{out}$** | -0.1 |
| **$F_{Oscillation}$** | 2.74 GHz |
| **Output Capacitance** | 10 pF |

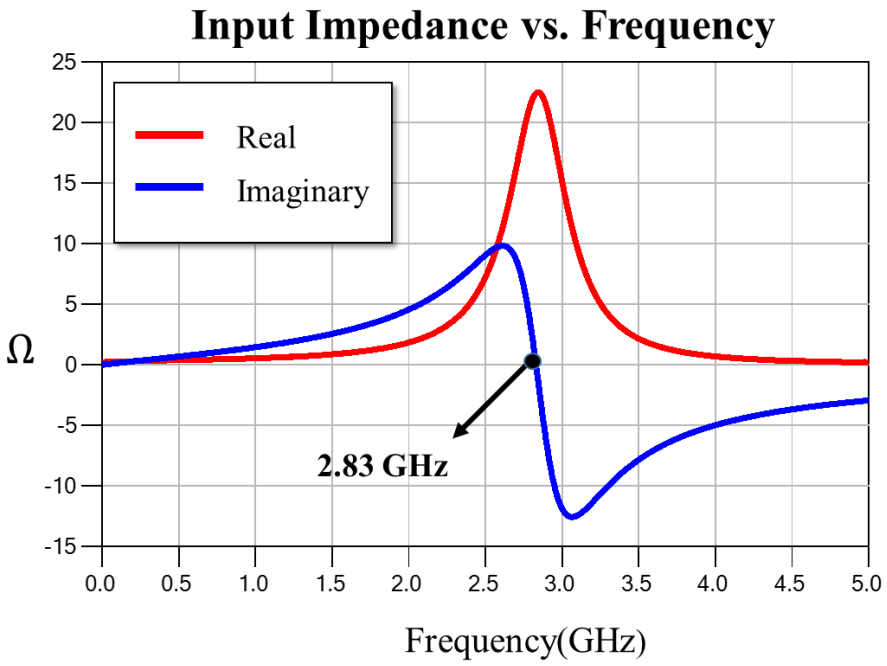


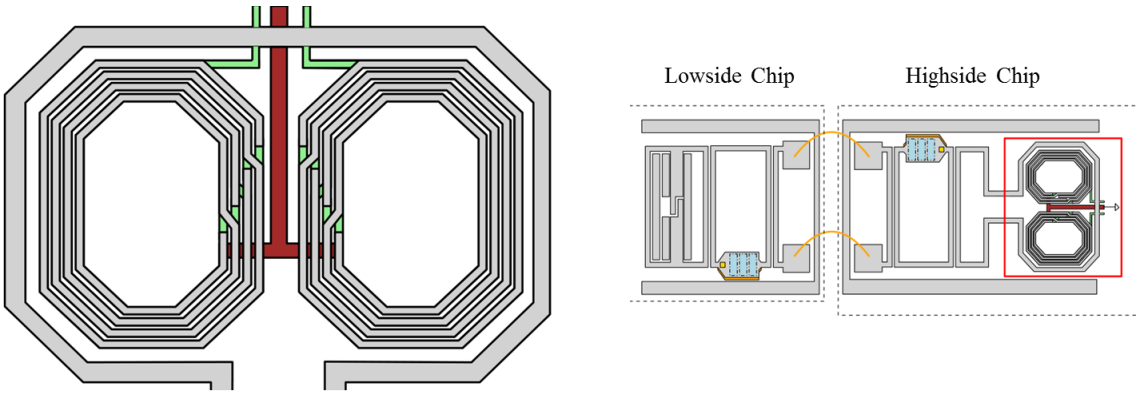

Figure 4-6 EM Simulation Results of Input Impedance of the LC Structure in Figure 4-5 (b) vs. Frequency.

## 4.3 Center-tapped Solenoid Differential Transformer

The step-up transformer is necessary for increasing the voltage gain of the RF signal and delivering a fully differential signal to the receiver on the High Side chip. In addition, the transformer needs to have a center tapped architecture with the center tap connected to the middle point of the half bridge power circuit, since the transformer's secondary winding is driving the transistors' gates on the high-side receiver.

One of the challenges with monolithic transformers is the die size area that they occupy. In this work, a solenoid structure similar to [26] has been utilized to achieve a high voltage ratio. The solenoid structure has the advantage of using windings in multiple metal layers to achieve double the turns ratio in the same area of single-layer windings. The solenoid structure takes advantage of the vertical space on the die to minimize the area on the x-y surface.

The transformer consists of a one-turn inductor as the primary side and a pair of inductors that are connected two each other as the secondary side, as illustrated in Figure 4-7. Figure 4-8 shows the transformer with the part of the top metal of the secondary winding removed, illustrating that the lower level layer is in series with the top layer winding. It can be seen that each of the secondary inductors consist of 8 turns, 4 on the top metal (grey), and 4 on the lower level metal (green), connected in series to each other using vias (with one turn on top and one turn on bottom). These 8 turns are connected in series, and two secondary halves are connected to each other in series on the symmetry line where the center tap (red) is connected. Figure 4-9 shows a bottom view of the transformer, with a more clear shot of the center tap and vias forming the solenoid.




(a) (b)

Figure 4-7 (a) Solenoid Transformer layout, and (b) Location within the Entire System

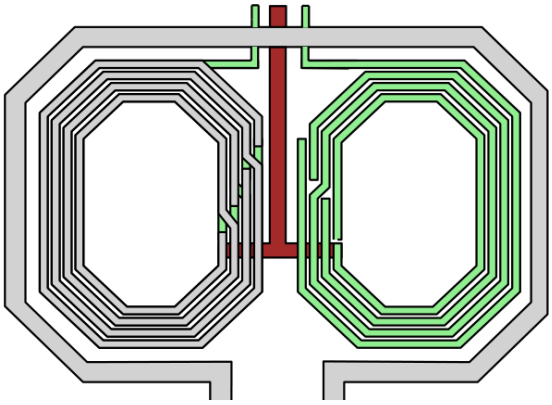


Figure 4-8 Solenoid Transformer Layout with Top Metal Removed from the Inductor on the Right

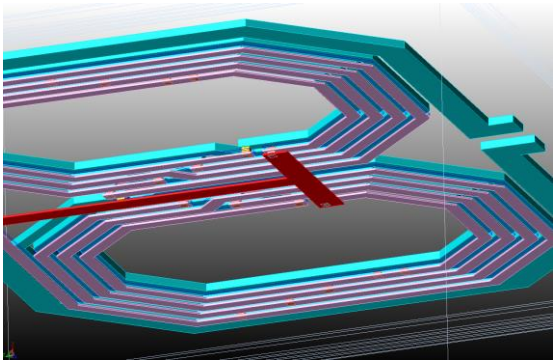


Figure 4-9 3D Bottom View of the Solenoid Transformer

The center tap of the transformer during EM simulation is grounded, and the secondary outputs are loaded by a capacitance representing the receiver's input impedance. The value of this capacitive load has been determined as 195 fF to achieve a maximum voltage gain in the system. This capacitive loading also causes Tesla resonance of the transformer, increasing the output to input voltage ratio of the transformer.

The voltage gain of port j (output) to port i (input) can be written as $G_{ji} = \frac{Z_{ji}}{Zii}$.

Figure 4-10 plots the EM simulated transformer voltage gain over frequency. A gain of 13.3V/V has been achieved, which is more than the transformer's turn ratio of 8.

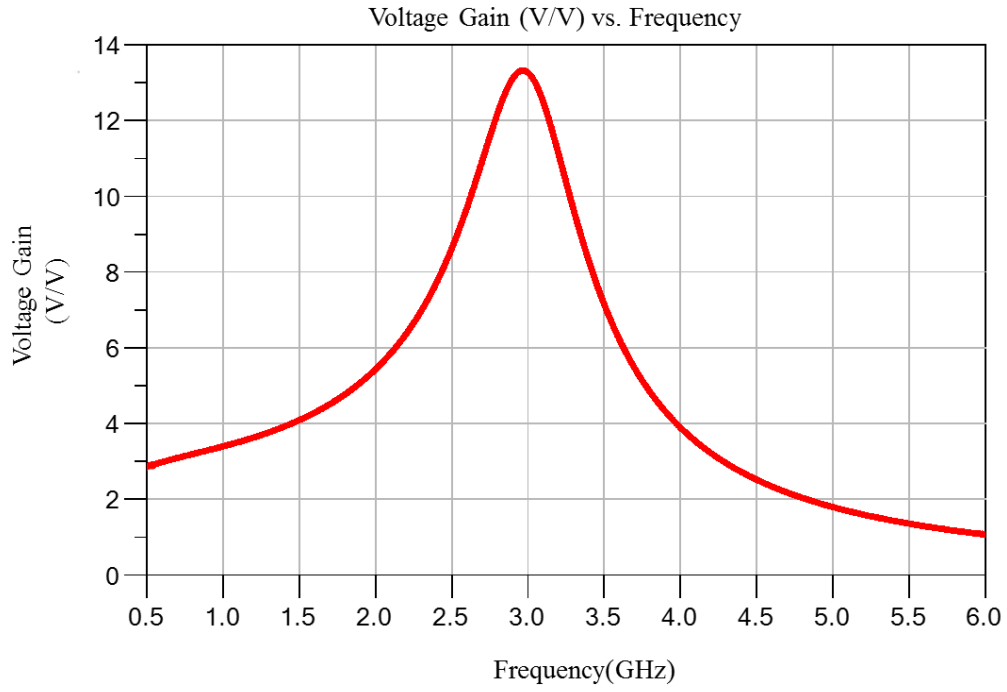



Figure 4-10 Transformer Voltage Ratio Over Frequency for a 195 fF Differential Load.

## 4.4 Bondwire

Modeling the bondwires has been done using design kit models already established by the RF system simulator. Using the physical parameters of the bondwires, such as their thickness, spacing between wires, and wire shape, fairly accurate bondwire models are implemented in the RF system simulator. Bondwires were not simulated in an EM simulator, due to their requirements for a 3D EM simulation and high simulation memory and time.

## 4.5 System Simulation Results

### 4.5.1 Communication Channel

The entire system consists of a cascade of the building blocks described in the previous sections. Figure 4-13 plots the EM simulation results for the communication channel with 195 fF capacitance as the load. Input impedance of the entire system, which is the input impedance looking into Loop 1, and output impedance, which is the impedance looking into the transformer's output.

The input impedance shows two peaks as predicted because of the loading effect coming from resonant coupling of Loop1 and Loop2, causing resonance frequency splitting. Also transformer output shows a resonance at the same frequency with the input. From the real part of input, it can be seen that around resonance frequency the minimum of input resistance is slightly more than 10 (Ω), thus the negative conductance oscillator connected to the system should be able to provide a minimum of -0.1 (S) conductance.

Also, the real part of input impedance indicates that the active core of the oscillator should be able to provide negative conductance to compensate 13.6 ohms of resistance

looking into the oscillator's LC tank. Figure 4-14 depicts the voltage gain of the communication channel from the oscillator's output to the transformer's output. A maximum voltage ratio of 0.22 V/V has been achieved by optimizing the capacitor values on the resonator loops, oscillator loop, and the receiver input capacitance (load capacitance).

Looking at Figure 4-12, it can be seen that the communication channel has been tuned to peak at 2.8 GHz, however according to Figure 4-11 the Oscillator is expected to oscillate at 2.70 GHz. The reason that the channel voltage gain peak has been chosen at 2.8 GHz can be seen looking into imaginary part of input in Figure 4-11 (top). The area encircled in green shows that the imaginary part is very close to zero in the range of 2.7-2.9 GHz. This means that if the design after tape out experiences a higher inductance, the resonance frequency is prone to shift 200-300 MHz. A shift in frequency because of the narrow band of the voltage gain of the channel can considerably affect the gain, and for this reason, the center of the flat region (green circle) at 2.8 GHz was chosen as the peak frequency to ensure the gain remains around 80 % of the maximum peak with frequency shift. It can be seen from Figure 4-12 that the voltage gain variation with a span of 300 MHz around the peak value is less than 20 %.

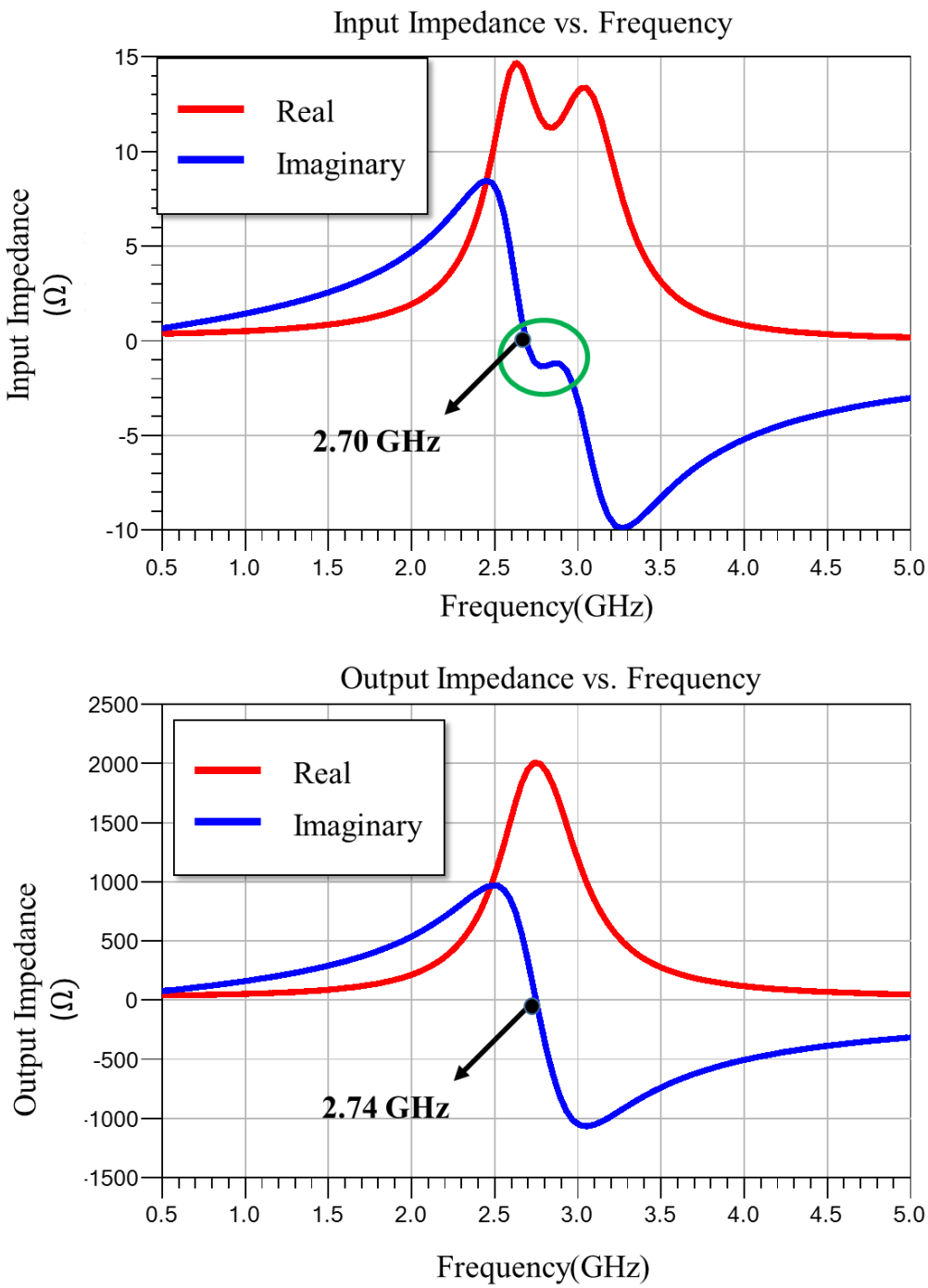



Figure 4-11 (top) Communication Channel Input Impedance Looking into Loop 1

(bottom) Output Impedance/Differential Transformer

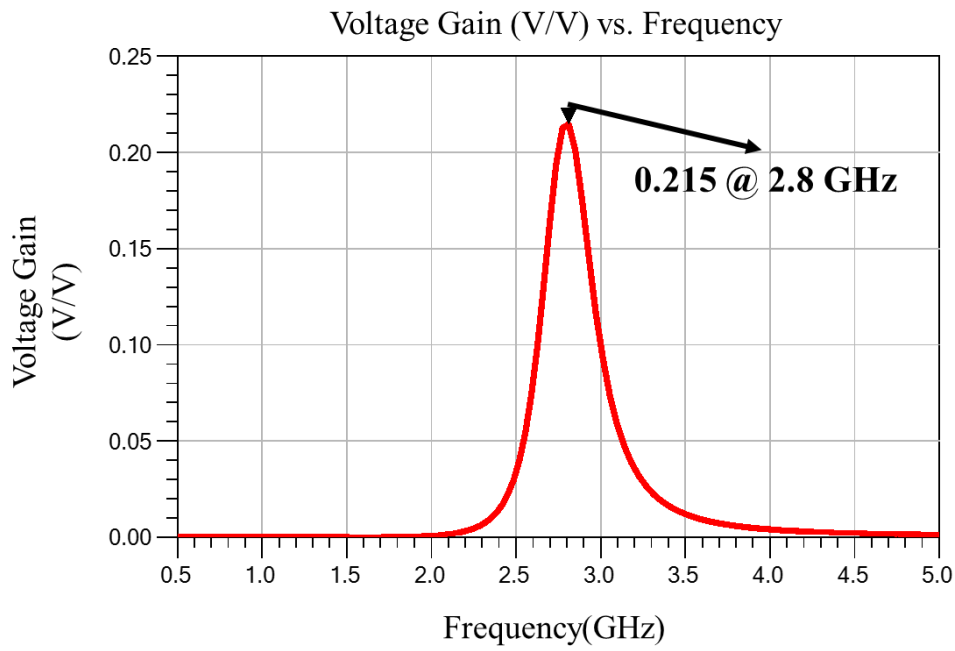



Figure 4-12 Entire System Voltage Gain from EM Simulations

### 4.5.2 Communication Performance for the Total System

The complete system's transient simulation (encoder-oscillator-receiver-decoder) is depicted in Figure 4-13, and demonstrates the successful operation of the total system. As the transient response indicates, a digital 0 V to 5 V input has been applied to the encoder, the encoder turns on the oscillator for a time length of 10 ns after detection of a rising edge and then for 5 ns after detection of the falling edge. When the oscillator turns on, a wavelet with an amplitude of 4V is generated and received as a wavelet with an amplitude of more than 0.8 V. The received wavelet has been successfully decoded, reproducing the input signal on the output with a propagation delay of less than 12 ns, which is 3ns better than the targeted 15 ns propagation delay. It should be mentioned that in this transient simulation, the communication channel has been implemented in SPICE

using an equivalent lumped element model to allow for transient convergence. The lumped element modeling is explained in detail in the next chapter.

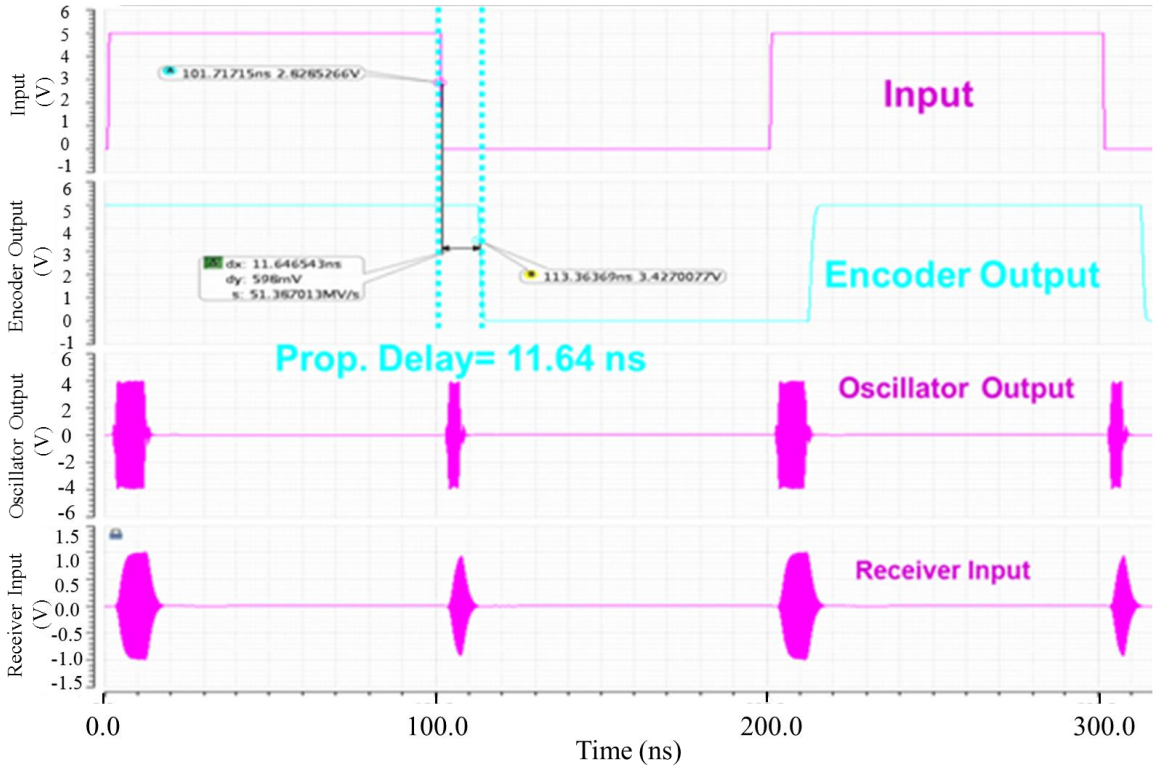



Figure 4-13 Full System Communication Performance

# CHAPTER 5

# Lumped Element Model

## 5.1 Motivations for Lumped Element Modeling

Transient simulations are a crucial part of the present study for two major reasons: 1) to verify the communication performance of the design, and 2) to verify the galvanic isolation capability of the system when applying a DC transient to the high side circuits' floating reference [ground].

When simulating the full system in a SPICE circuit simulator, such as Cadence, there are foundry-developed libraries for most standard elements, such as transistors, that are based on parametrized equations. However, for the communication channel, which is the heart of the isolator, an external model must be generated and imported to the SPICE simulator. One way to do this is to import an s-parameter file (e.g. Touchstone files with extension .snp) that is generated from electromagnetic (EM) simulation/measurements of various components in the communication channel. However, this solution can generate inaccuracies and convergence problems when simulating transient behavior and solving for DC operating points. Moreover, EM simulations that allow for fine resolution transient steps to help with convergence, generate a large number of data points and therefore consume copious amounts of memory and time for simulation. Furthermore, even after taking this step and modifying the numerical methods of the SPICE-based transient simulation for achieving convergence, the results may experience numerical errors. The problem becomes more challenging when simulating the transient DC pulses.

One solution that addresses convergence and allows for faster design and tuning for optimization is to use an equivalent lumped element model (LEM). The designed system operates at 2.8 GHz, and the wave length is more than 10cm. This means that the length of the implemented transmission lines are 100 times smaller than the wave length, with less than 1mm. Therefore, the LEM around the operation frequency can be realizable and valid.

## 5.2 Equivalent LEM Circuit Methodology

The generated LEMs in this work rely on two sources of data: EM Simulation results and measurement results. Depending on the parameters in the circuit that are being optimized, they may borrow their values from measurements or simulations.

To model the communication channel, three major blocks are modeled: low side chip, high side chip, and bondwires. After successful modeling of these blocks, they can be cascaded and compared with the performance of the full EM simulation of the communication channel.

The models have been generated and fitted to s-parameter based data. However, the component values used in the model have been chosen in a way to guarantee that the final model is realizable in most circuit simulators. For this reason, mutually coupled inductors have been used to model the magnetic coupling over the gaps and the transformer, rather than using transformer models from ADS libraries.

A valid LEM should not only match simulation and measurement data in terms of key performance parameters [voltage gain], but they should also represent a physical quantity in the system and have reasonable values. To attain this goal a series of steps have been taken, as outlined below.

The model uses inductors in series with resistors to model the inductor loop and transmission lines while substrate capacitance has also been included using a capacitor in series with a resistor. The isolation gaps have been modeled by using capacitors, and the magnetic couplings modeled using coupled inductors with a coupling coefficient parameter of "k". The steps for determining parameter values are as follows:

1. Model the bondwires based on an ADS model with lumped components.

2. Find the values of inductance and capacitances of metals (loops, bond pads…) from the EM simulations.

3. Tune the coupling coefficients, the inductance, resistance values of the pads and resonator loops to match resonant frequency, R, and L for both input and output. Compare the performance with EM simulations of the Low Side chip.

4. Repeat step 3 for the High Side chip and transformer, borrowing starting point values for bond pads and resonator loop from step 3.

5. Modify the transformer model based on the measurement results. Modify transformer coupling "k", and input and output impedances.

6. Replace the transformer model from 5th step in the high side model from the $4^{th}$ step. Modify the coupling coefficient between the transformer and the resonator loop, and the bondpads R and L to match the performance of the High Side system's measurements.

## 5.3 LEM for Bondwires

The lumped element for the bondwire has been developed based on the ADS bondwire model, as explained in the previous section. The ADS lumped element model is an equation-based model, therefore requiring translation to a LEM so that it can be imported to SPICE simulators.

Figure 5-1 represents the diagram of the circuit equivalent for two parallel bondwires. Each bondwire was modeled as an inductor in series with a resistor. The values of inductors and series resistance have been extracted from real and imaginary parts of the ADS model. Resistance R2 has been added to take into account the increasing slope [skin effect] for the resistance around 2.8 GHz. The mutual coupling (k) between the two bondwires is found by finding the inductance looking across ports 1 and 2, while ports 3 and 4 are shorted.

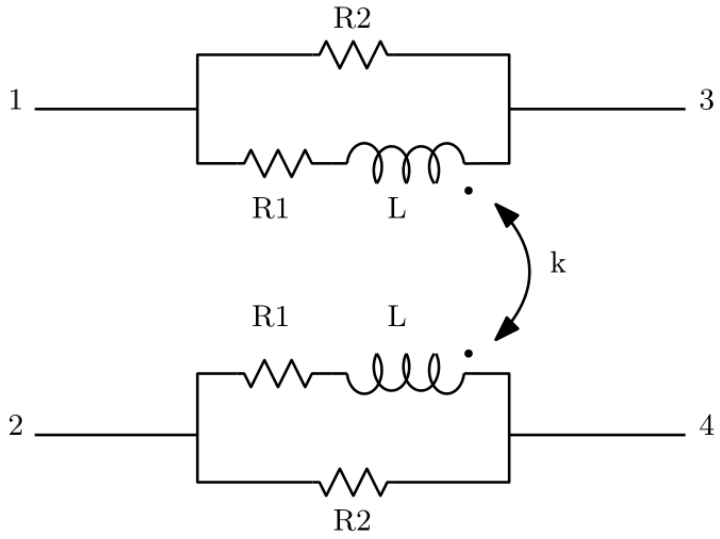



Figure 5-1 Bondwire's LEM Diagram

The extracted values for the components shown in Figure 5-1 are found in Table 5-1.

Table 5-1 Bondwire's LEM Parameters

| Parameter | Value | Unit |
|---|---|---|
| k | 0.16 | - |
| L | 0.70 | nH |
| $R_1$ | 280 | mOhm |
| $R_2$ | 1440 | Ohm |

The inductance is calculated using the following equation when looking across ports 1 and 2 and setting ports 3 and 4 as open in Figure 5-1:

$$L \cong \frac{\text{Image}(Z)}{2\pi\omega} \qquad (5\text{-}1)$$

Where M is the mutual inductance between two bondwires. It can be seen that according to Equation 5-2 since L is known, k is determined by tuning its value toward getting a fit. Figure 5-3 demonstrates the inductance looking into two bondwires in series. It can be seen that the total series inductance value is matched with less than 1% percent error from 500 MHz to 1 GHz.

The value of R2 is generally large and can be ignored. Figure 5-2 shows that the inductance value is in good agreement with the RF simulator [ADS] model with less than 1% error. The value and slope of the resistance is matched around 2.8 GHz.

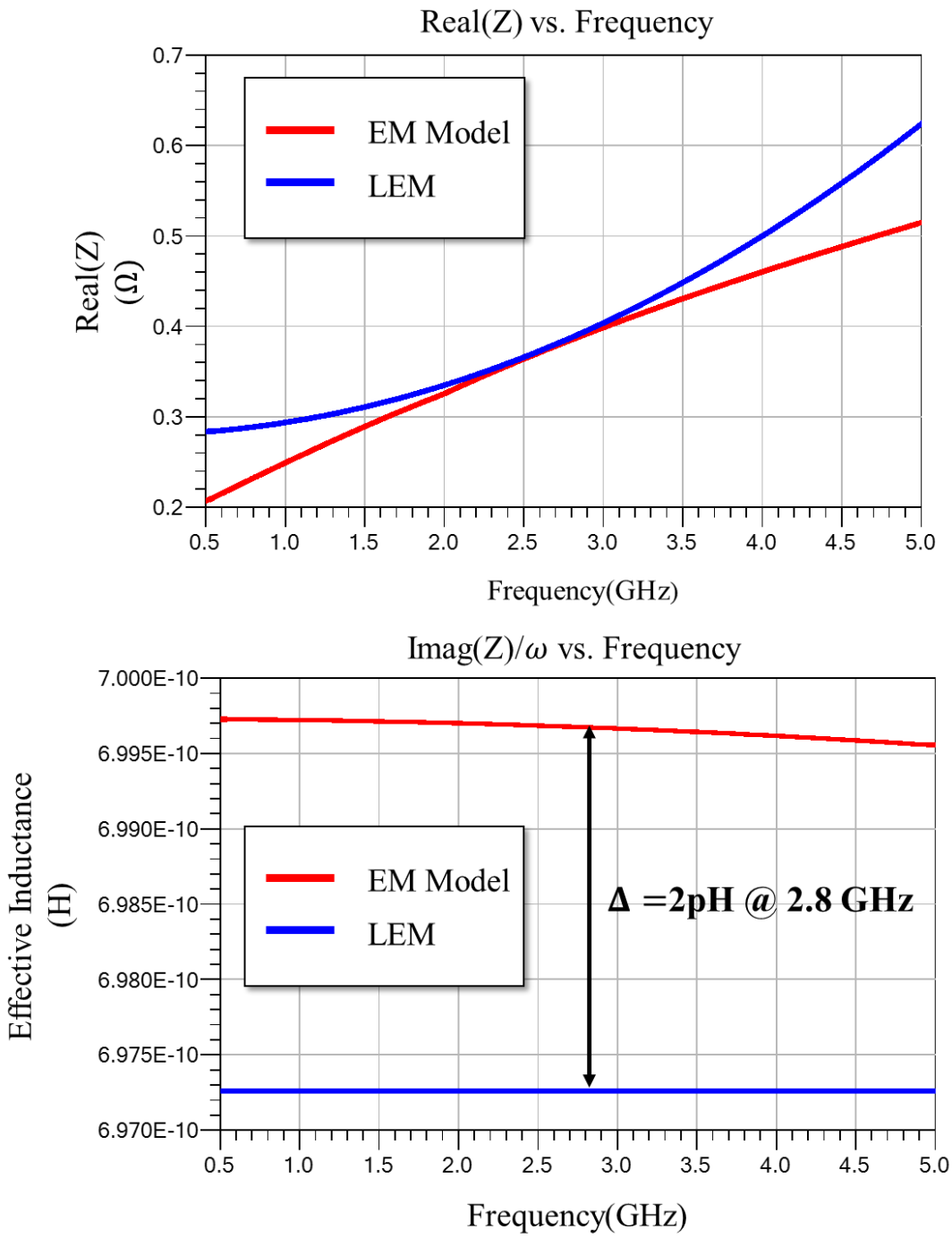



Figure 5-2 Inductance and Resistance Looking across Ports 1 and 3 while Ports 2 and 4 are Open.

The inductance looking into ports 1 and 2 while keeping ports 3 and 4 shorted is found with the equation below:

$$\frac{\text{Image}(Z)}{2\pi\omega} \cong L + L - M \qquad (5\text{-}2)$$

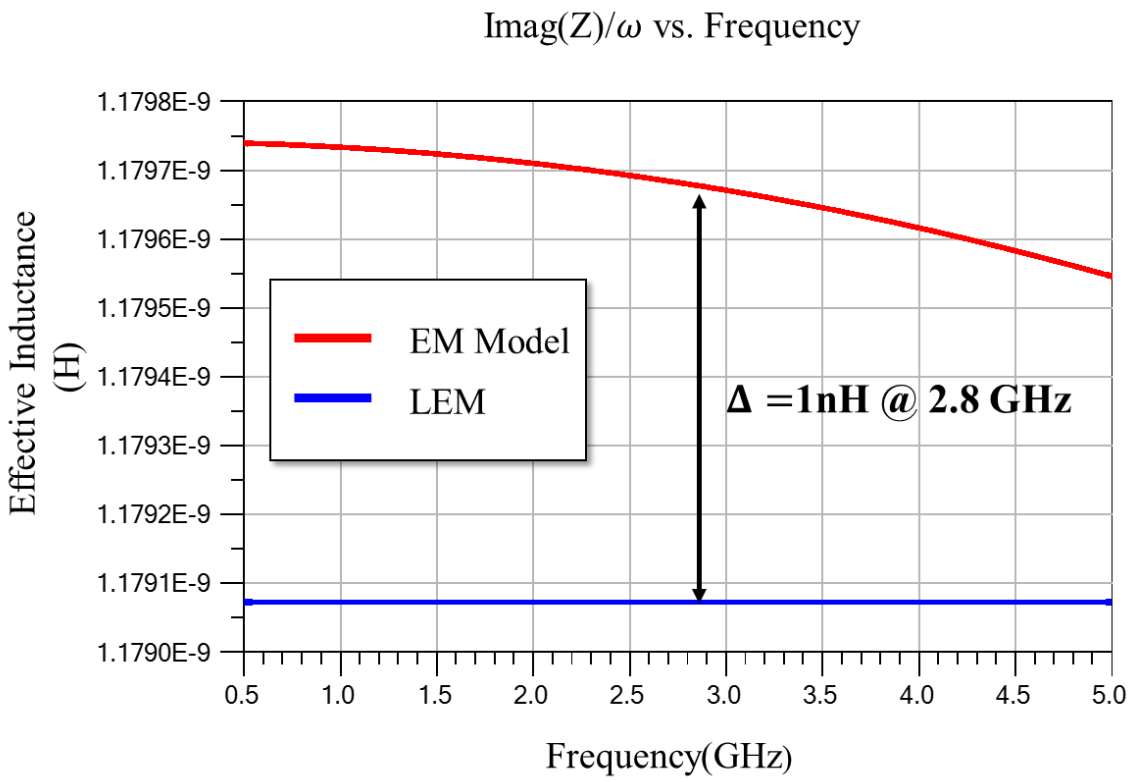



Figure 5-3 Inductance Looking Across Ports 1 and 2 while Ports 3 and 4 are Shorted

## 5.4 LEM for Low side Chip

The LEM for the low side is shown in Figure 5-4. The model for the low side consists of equivalent circuits for Loop 1, Loop 2, and the inductor between bond pads, where the loops are magnetically coupled to each other through mutual couplings with coupling coefficients of k1 and k2. The isolation gaps between the subsections are modeled using capacitors distributed between the adjacent metal arms of the loops ($C_{Gap}$

and $C'_{Gap}$). The substrate capacitance is also distributed to the center of each metal branch to ground ($R_{Sub1}$ and $R_{Sub2}$). Because of the identical shape between the half-loops of Loop1 and Loop 2, the component values of all half-loops are identical. The bondpads with bondwire inductance forms a half-loop, which also has the same component values. The MIM resonator capacitor in the repeater (Loop 2) is modeled as $C_{Loop2}$, and the total capacitance seen looking into Loop 1 is modeled as $C_{Loop1}$.

The majority of the model parameters were extracted from EM simulations, measurement structures for the entire Low Side chip were not available on the first fabrication cycle. Parameter values of Loop 2 were derived from the measurement data of the Fundamental Resonator.

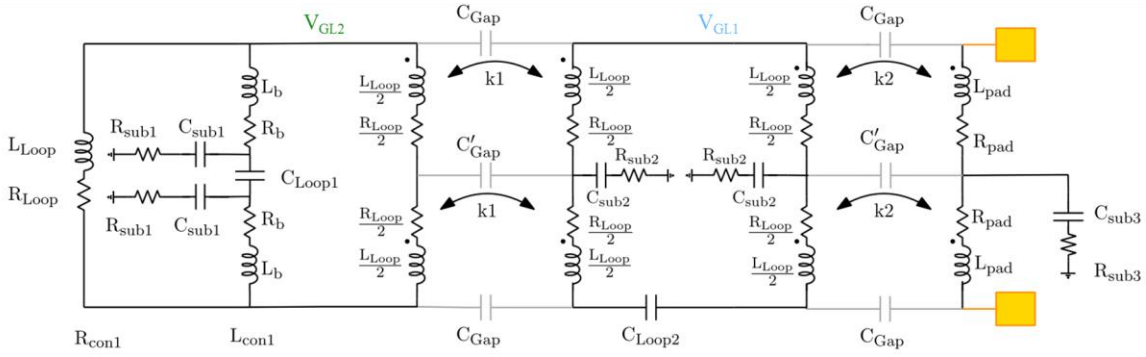



Figure 5-4 Low Side Chip's LEM diagram

Table 5-2 Low side LEM Parameters Value of Figure 5-4

| Parameter | Value | Unit | Parameter | Value | Unit |
|---|---|---|---|---|---|
| $R_{sub1}$ | 250 | Ω | $R_{sub2}$ | 300m | mΩ |
| $C_{sub1}$ | 88 | fF | $C_{sub2}$ | 75 | fF |
| $L_b$ | 20 | pH | $L_{pad}$ | 150 | pH |
| $R_b$ | 825 | mΩ | $R_{pad}$ | 235 | mΩ |
| $L_{Loop}$ | 305 | pH | $R_{sub3}$ | 150 | Ω |
| $R_{Loop}$ | 750 | mΩ | $C_{sub3}$ | 110 | fF |
| $C_{Gap}$ | 9 | fF | $C_{Loop2}$ | 10.00+5.94 | pF |
| $C'_{Gap}$ | 18 | fF | $C_{Loop1}$ | 5.47 | pF |
| k1 | 0.34 | - | k2 | 0.46 | - |

Table 5-3 Low Side Chip's LEM Parameters Extraction Method

| Extraction Method | Parameters |
|---|---|
| **Probing EM structures** | $C_{gap}$, $R_{sub}$, $C_{sub}$, Rpad, $L_{pad,}$ $L_b$, $R_b$ |
| **Curve fitting with EM simulation** | k1, k2 |
| **MIM Caps, known from design** | $C_{Loop1}$ |
| **Curve Fitting with Fundamental Resonator** | $C_{Loop2}$, $L_{Loop.}$ $R_{Loop}$ |

The extracted values of the LEM are shown in Table 5-2, and the extraction method for each parameter is explained in Table 5-3. Some of the values, such as k1 and k2, have been extracted by tuning the model with respect to simulated maximum voltage gain and frequency performance. The overlaid results of the lumped element model and EM simulations are shown in Figures 5-5 and 5-6.

The data reflects that input resistance and output resistance are in good agreement with EM simulations, matched at 2.8 GHz with less than 10% overall error. The peak frequencies for input resistance and effective inductance also match, which means that the resonance frequencies of the two chips match. In terms of voltage gain, it can be seen that the two curves are well fitted over 5 GHz of frequency range, and both results peak at 2.8 GHz with less than 5% difference. The compared results conclude that the system's target voltage gain was successfully achieved in the chips' first fabrication cycle.

## 5.5 LEM for High Side Chip

The circuit diagram for the High Side chip (Figure 5-7) includes similar bondwire and bondpad setup as well as repeater (loop) structures. The transformer connection has been modeled by using a half loop structure for the branch ($L_{Con1}$ and $R_{Con1}$) coupled to the repeater loop (Loop 3) and two inductors to model the metals connecting the half loop to the transformer ($L_{Con2}$ and $R_{Con2}$). The transformer's has been modeled using $L_{prim}$ and $R_{prim}$. The substrate capacitance of the primary has been modeled as $C_{Sub4}$ in series with $R_{Sub4}$ connected from middle of the primary to the ground. The primary is coupled to the secondary with a coupling coefficient of k3.

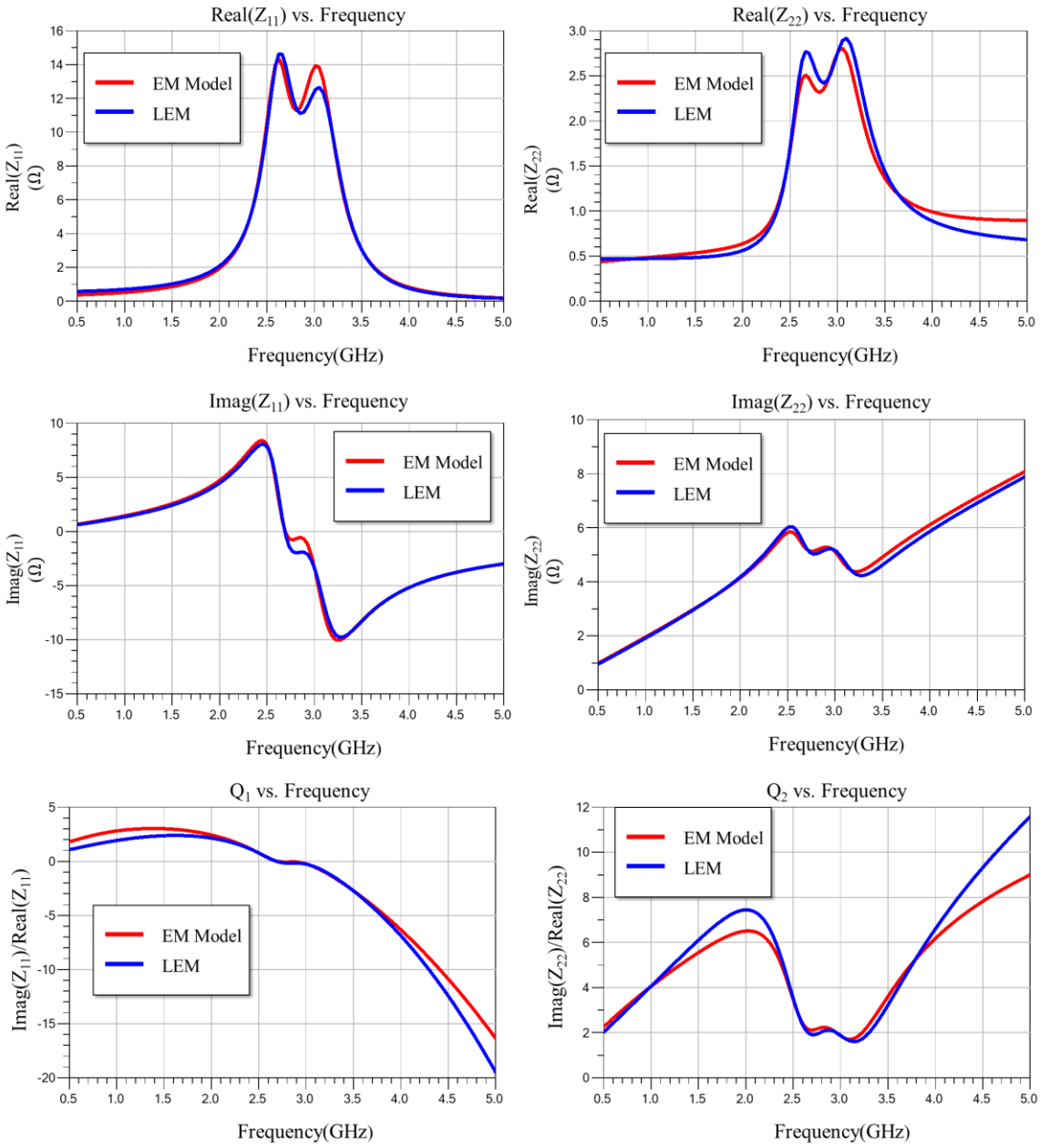



Figure 5-5 Low Side Chip LEM vs. EM Simulation Input/Output Performance Plots

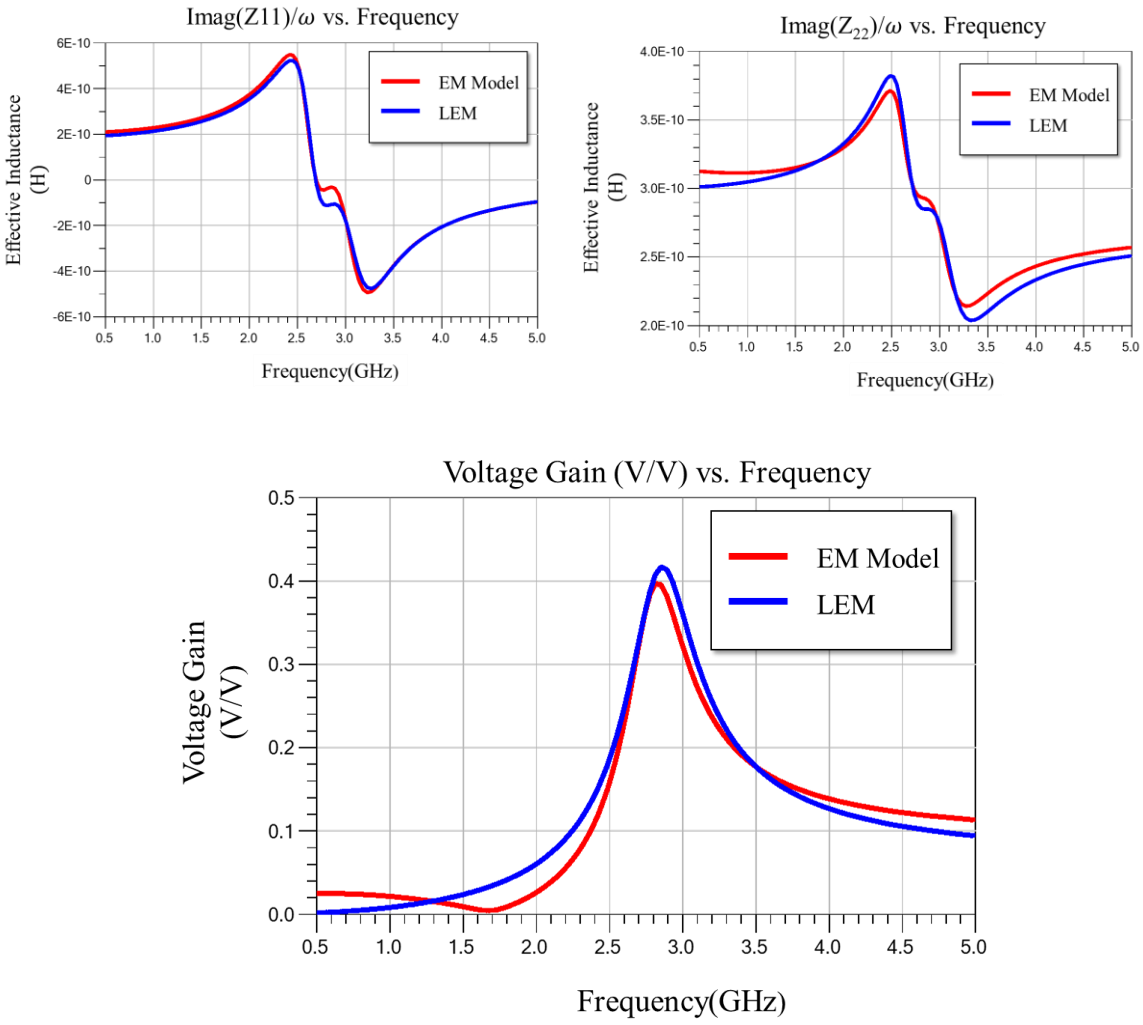



Figure 5-6 Low Side chip LEM vs. EM Simulation for Effective Inductance (top)

Voltage Gain (bottom)

The secondary has been modeled as a pair of inductors ($L_{sec}$ in series with $R_{sec}$) while there are two capacitors in parallel with these inductors to account for both substrate capacitance and averaged inter-winding capacitance of the secondary ($C_2$ in series with $R_2$). The gap between the secondary and primary has been modeled applying a pair of capacitors with values different from the gaps between other subsections ($C_{Gapt}$).

The LEM component values are summarized in Table 5-4 and Table 5-5, showing both the values and explanations on the sources of extraction.

Since the transformer and High Side chip were fabricated and measured, some of the values were extracted directly from measurements.

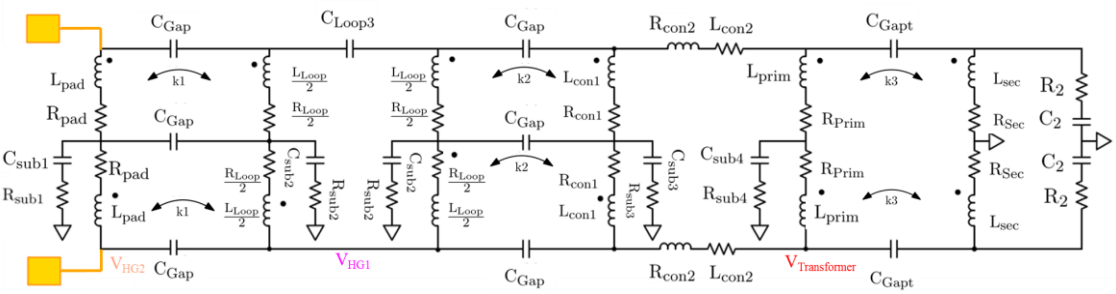



Figure 5-7 High Side Chip's Diagram

The comparison between the high side LEM and measurement results has been done for two conditions: 1) the high side chip is unloaded on the receiver side, and 2) the high side chip is loaded with a differential capacitive load of 195 fF. The performance plots for the unloaded network (Figures 5-8 and 5-9) show that all parameters are in good agreement. The input and output resonance frequency is well matched with the EM simulations, and the self-resonance of the transformer's secondary winding are in good agreement between both models. According to the effective output inductance and input resistance, it is apparent that the two models compare from low frequencies up to 3 GHz. The input port's inductance is well matched at 2.8 GHz and has less than 30% mismatch for all other frequencies. The input resistance is well matched up to 2.5 GHz. At the peak frequency, there is resistance mismatch of 50% between the two models. However, the Quality Factor compares closely, which means that the effect of the resistance in comparison with the inductance has a minor effect in the total input impedance.

Table 5-4 High Side Chip's LEM Parameter Value of Figure 5-7

| Parameter | Value | Unit | Parameter | Value | Unit |
|---|---|---|---|---|---|
| $R_{pad}$ | 232.25 | mΩ | $R_2$ | 2 | kΩ |
| $L_{pad}$ | 194.25 | pH | $C_{gap}$ | 9 | fF |
| $C_{Loop}$ | 5.47 | pF | $C'_{gap}$ | 18 | fF |
| $L_{Loop}$ | 155 | pH | $R_{sub1}$ | 150 | Ω |
| $R_{Loop}$ | 300 | mΩ | $C_{sub1}$ | 110 | fF |
| $C_{Gapt}$ | 75 | fF | $R_{sub2}$ | 300 | Ω |
| $L_{prim}$ | 310 | pH | $C_{sub2}$ | 75 | fF |
| $R_{prim}$ | 660 | mΩ | $R_{sub3}$ | 150 | Ω |
| $R_{con1}$ | 375 | mΩ | $C_{sub3}$ | 110 | fF |
| $R_{con2}$ | 305 | mΩ | $R_{sub4}$ | 120 | Ω |
| $L_{con1}$ | 150 | pH | $C_{sub4}$ | 110 | fF |
| $L_{con2}$ | 305 | pH | $k_1$ | 0.46 | - |
| $L_{sec}$ | 13.25 | nH | $k_2$ | 0.36 | - |
| $R_{sec}$ | 36 | Ω | $k_3$ | -0.45 | - |
| $C_2$ | 14 | fF | | | |

Table 5-5 High Side Chip's LEM Parameters

| Extraction Method | Parameter |
|---|---|
| **Curve Fitting with measurement** | k3,$L_{pad}$, $R_{pad}$, $R_{prim}$, $L_{prim}$, $R_{sec}$, $L_{sec}$, $R_2$,$C_2$, $L_{Loop3}$, $R_{Loop3}$, $C_{Loop3}$ |
| **Curve Fitting with EM simulation** | k1,k2 |
| **Direct Extraction from EM simulation** | $C_{Gap}$, $C_{Gapt}$, $R_{subi}$, $C_{subi}$, $L_{con}$, $R_{con}$, $L_{con2}$, $R_{con2}$ |

Compromises were made in matching the input resistance and voltage gain in order to correlate the results in resonant frequency. The model doesn't take into account the structures' skin effect. Looking at the voltage gain performance of Figure 5-9, both gains peak at 2.8 GHz with an error of 30%, and peak at the secondary resonance frequency with an error of approximately 50%. The amplitude of the second peak is not a subject of interest; however it can be fixed by choosing a more sophisticated model for the transformer that has more distributed elements.

Figures 5-10 and 5-11 plot the simulation results for the capacitively loaded High side chip. The input port doesn't show have much variation from the unloaded results. But, it can be seen from the input and output impedance plots that the resonance frequencies between LEM and EM models are matched. The effective input inductance shows a match at 2.8 GHz. The quality factor is also in agreement between 1GHz to 2.8GHz. According to the voltage gain plots, the voltage gain shows a perfect fit in all frequencies with less than 10 % mismatch at the peak frequency of 2.8GHz.

The model for the High Side chip is mostly based on the measurement data, so it is expected that the performance of the measurement-based model does not align perfectly with the EM simulation, as it did with the Low Side chip results.

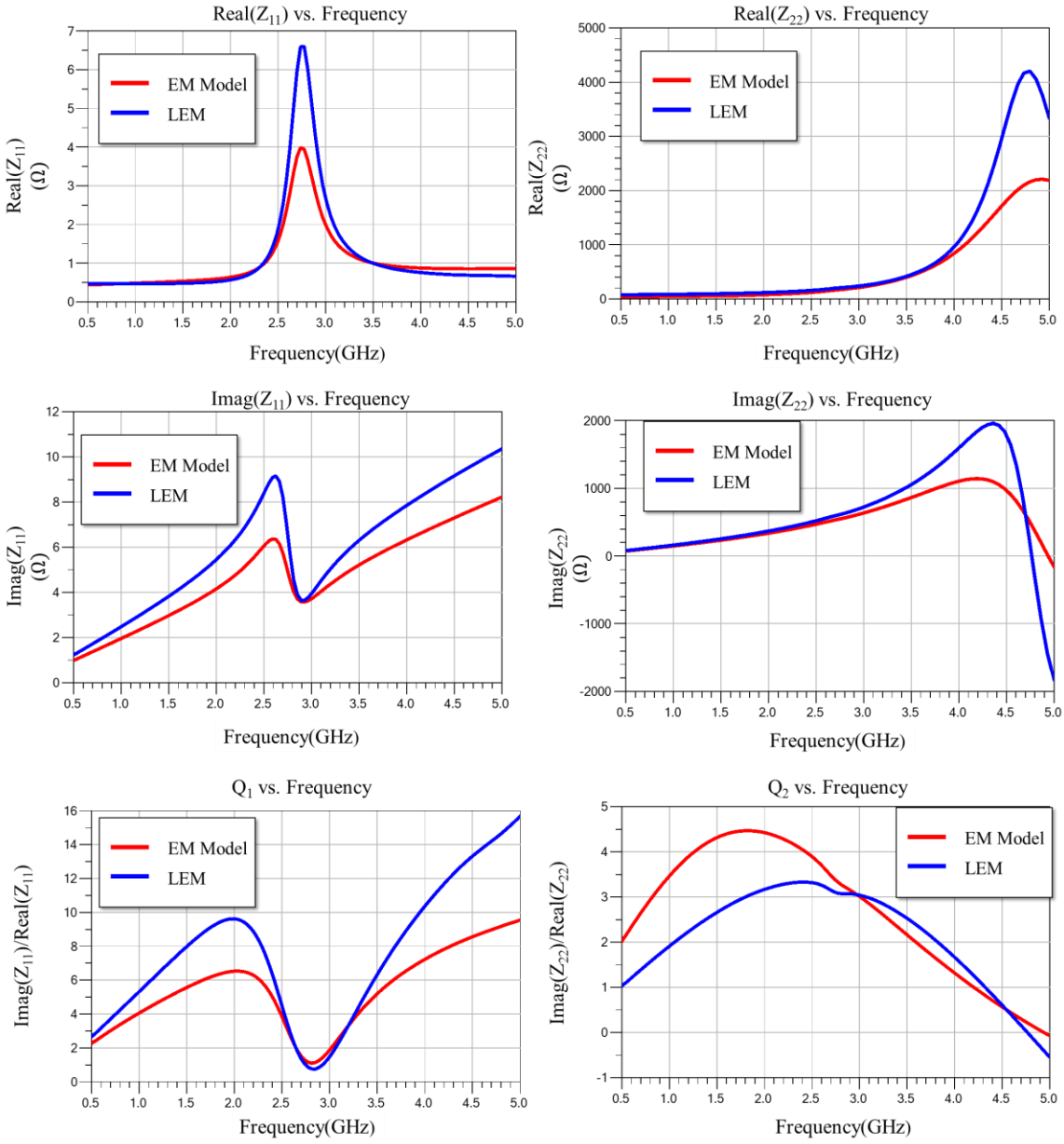



Figure 5-8 Unloaded High Side chip's LEM vs. EM Simulation Input/Output Performance Plots

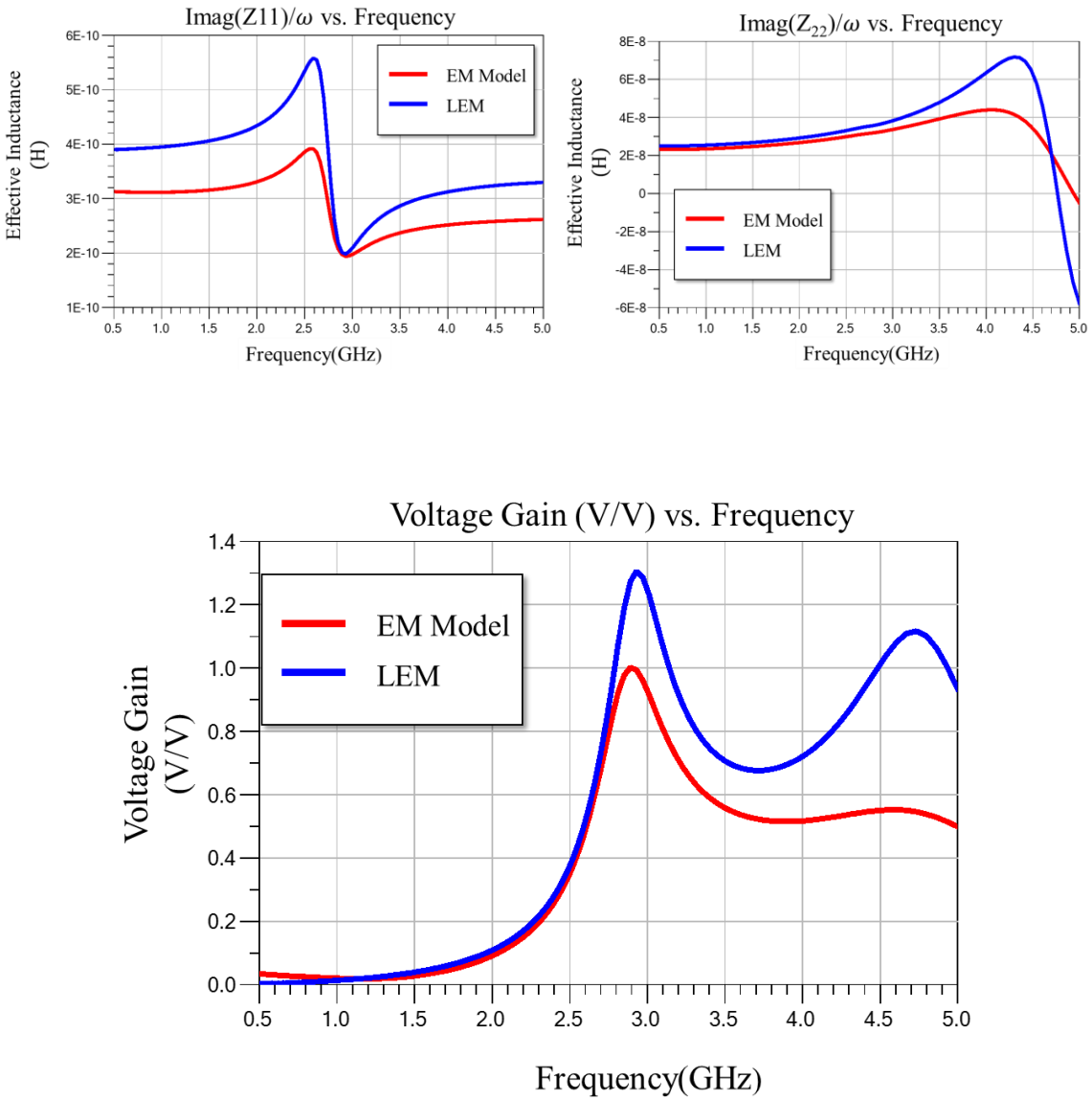



Figure 5-9 Unloaded High Side Chip's Overlaid Plots of Effective Inductance (top) and Voltage Gain (bottom) from LEM and EM Simulation

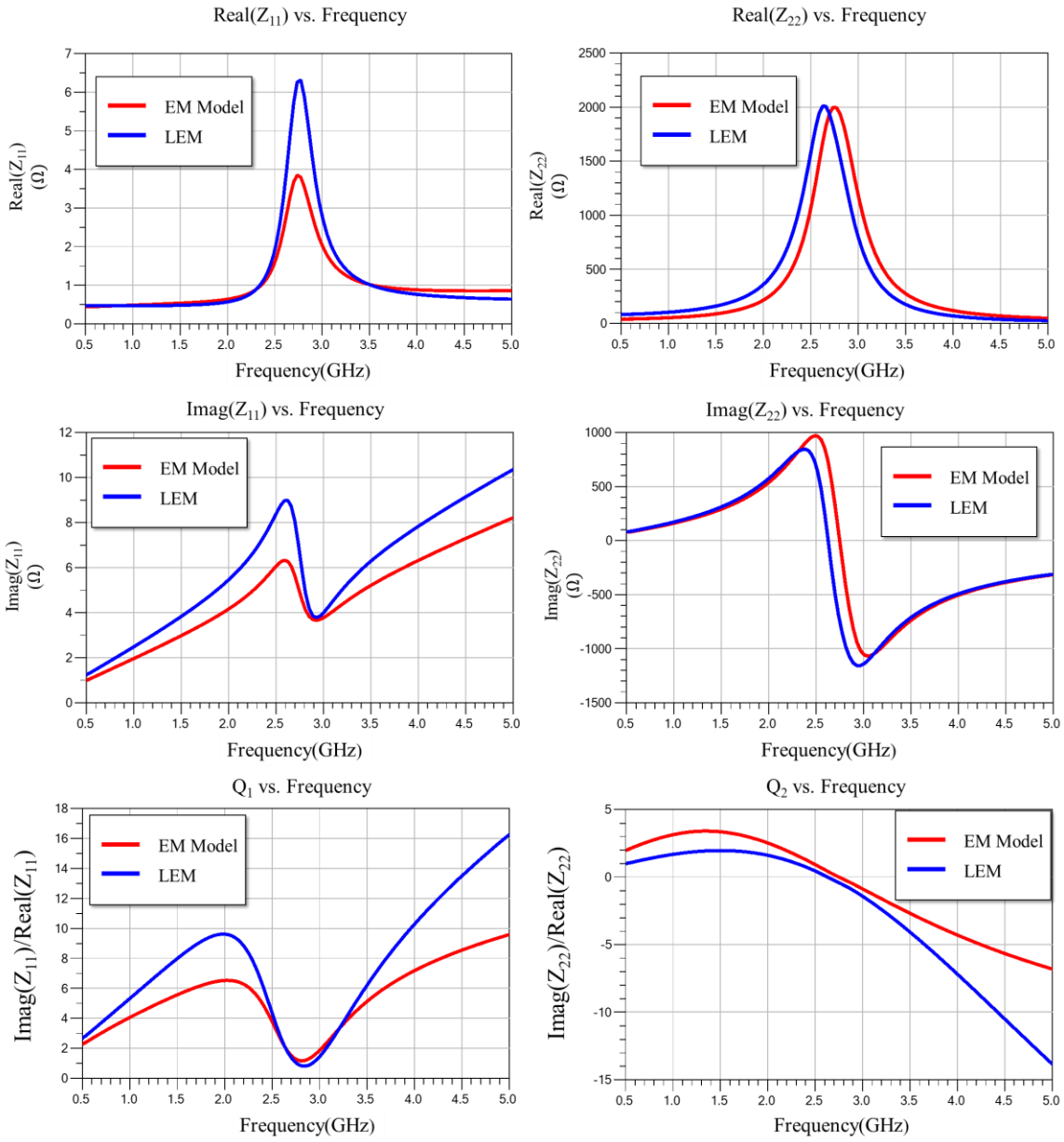



Figure 5-10 Loaded (195 fF) High Side Chip LEM vs. EM Simulation Input/Output Performance Plots.

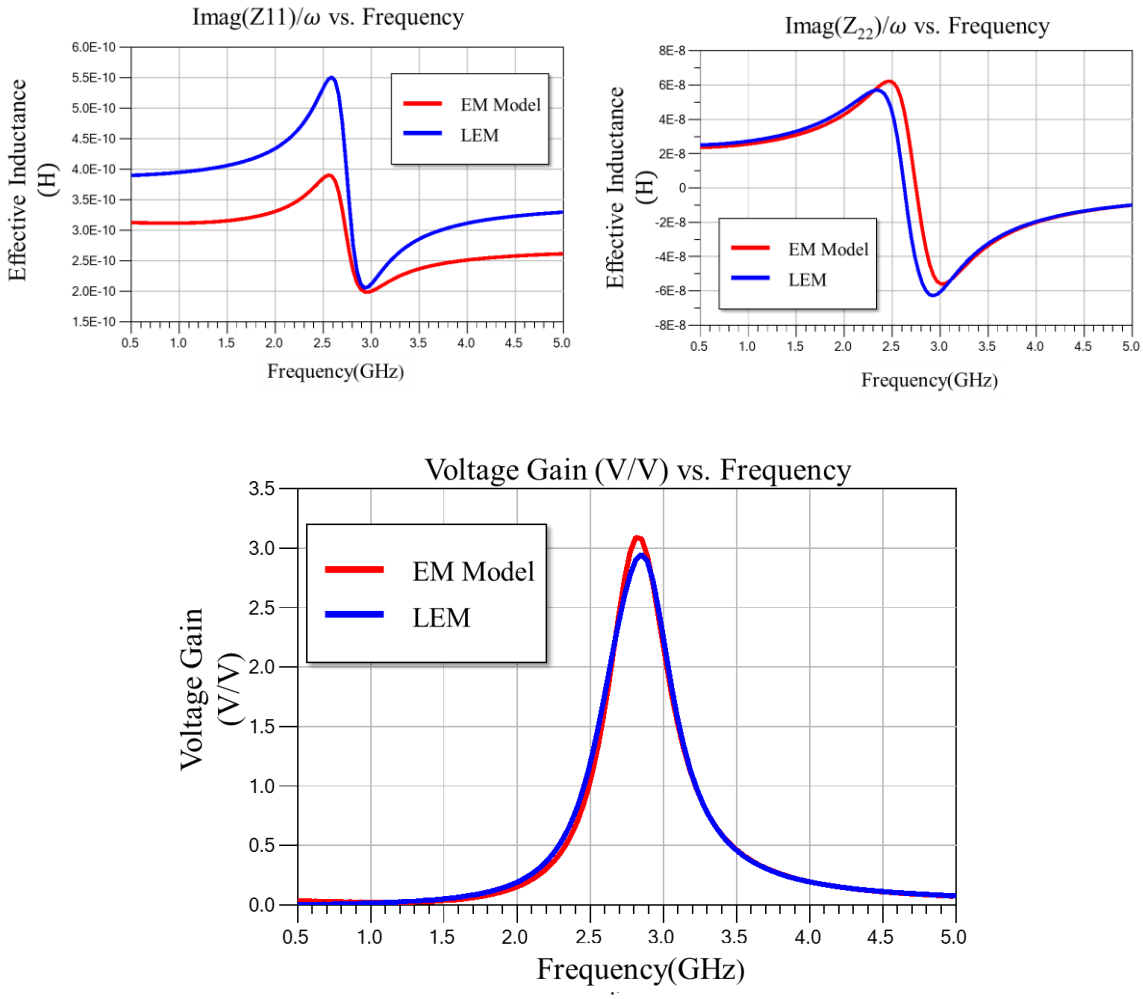



Figure 5-11 Loaded (195 fF) High Side Chip's Overlaid Plots of Effective Inductance (top) and Voltage Gain (bottom) from LEM and EM Simulation

## 5.6 Total System Performance

After verifying satisfactory performance from all circuit blocks, the models are cascaded together to predict overall system performance.

Comparing results from LEM and EM simulations indicates good agreement between results for frequencies spanning from 0.5 GHz to 5 GHz.

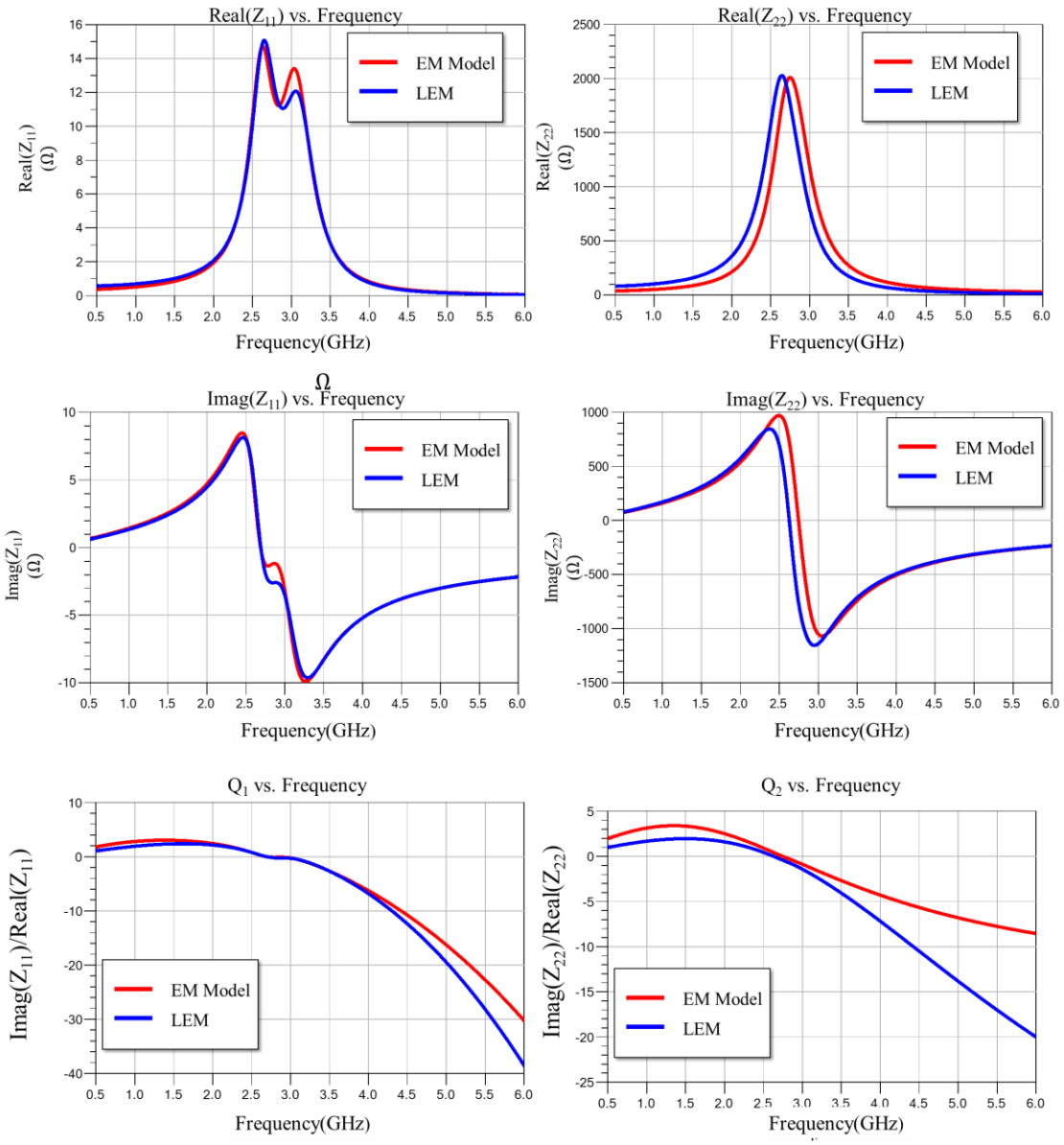



Figure 5-12 Input/Output Performance Plots for Entire System Predicted by EM Simulation and LEM

Comparison of the voltage gain results in Figure 5-13 shows identical frequencies trends, with the same peak frequencies and less than 20% variation between the two plots. This infers that the fabricated device has 20% better performance than what was

predicted from the EM simulation in terms of voltage gain, and the voltage gain peaks at the same frequency as the EM results predict.

The extracted results from s-parameter simulations are all in terms of differential performance. It is interesting to run the transient simulation in order to verify the single ended performance of the lumped element model. Figure 5-15 shows the single ended and differential simulations when a 2.8 GHz, 10 V p-p signal is applied to the communication channel. The result for both positive and negative outputs of the High Side chip are symmetric, differential, and 180 degrees out of phase.

Figure 5-16 shows the overlaid time-domain differential output signals from the S-parameter model and LEM. Recalculating the voltage gain using transient simulation results for the LEM gives a gain:

$$G_{LEM} = \frac{1.296}{5} = 0.26$$

The gain is less than 5% error from the results derived from S-Parameter measurements.

For the EM simulation based S-parameter model:

$$G_{MOM} = \frac{0.87}{5} = 0.174$$

This was expected to be 0.216 and has more than 20 % error.

Overall, more transient simulation accuracy and reliability was achieved when using LEM.

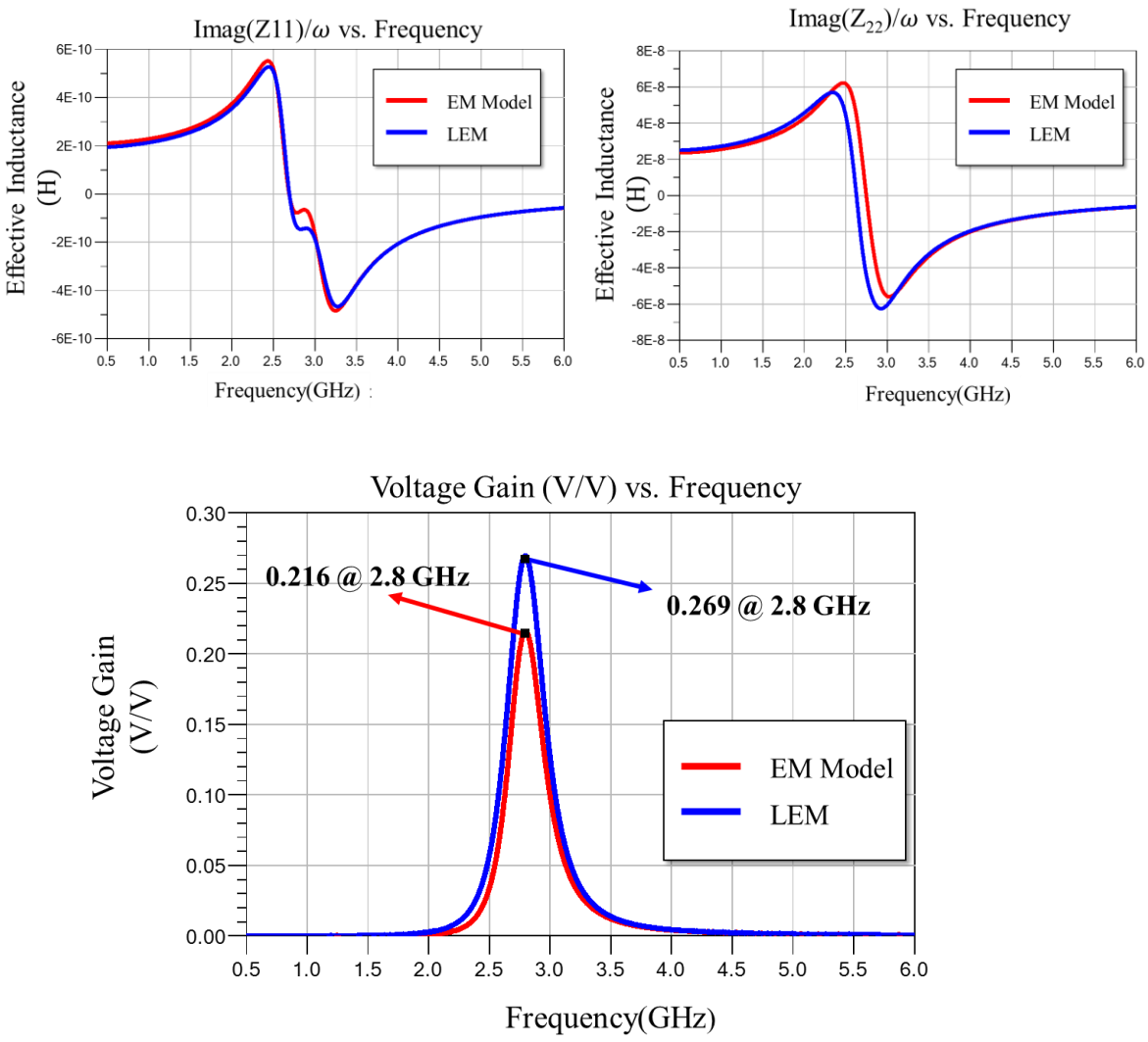



Figure 5-13 Entire System Overlaid Plots of Effective Inductance (top) and Voltage Gain (bottom) Predicted by EM Simulation and Measurement-Simulation based LEM

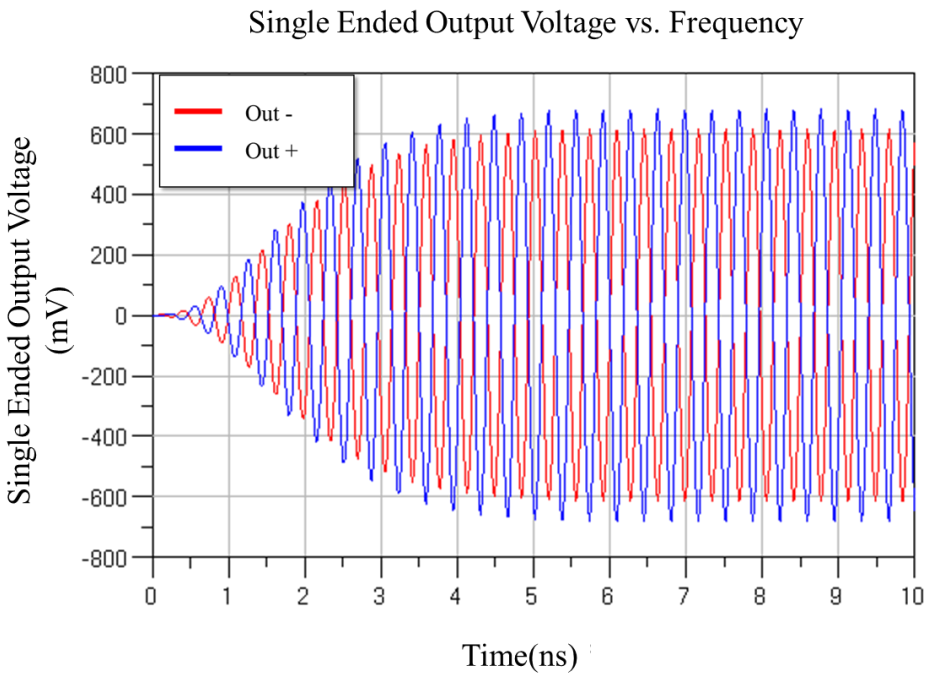



Figure 5-14 LEM Single Ended Measurement Results from LEM

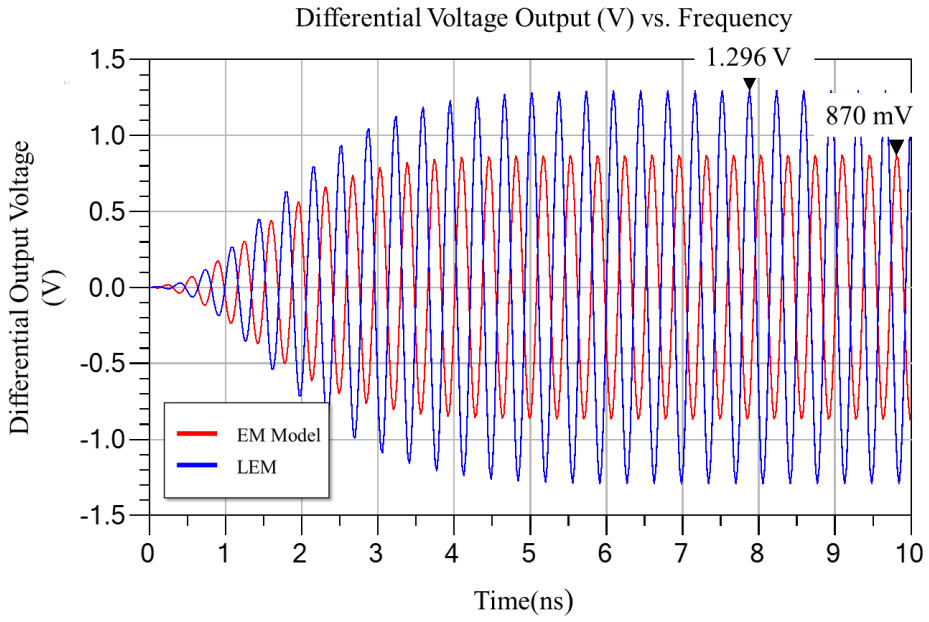



Figure 5-15 Comparison of Entire System Differential Output of S-parameters Model vs. LEM

## 5.7 HV Isolation Performance

A DC transient (350V with 50 V/us) has been applied to the High Side chip's ground (white triangle grounds in Figure 5-7) with reference to the Low Side chip's ground using the LEM model of the entire system. This model was made by cascading LEM models of Figures 5-3, 5-4 and 5-5. Figure 5-16 shows the system response to the applied pulse after each gap, with respect to the Low Side chip's ground. The locations of the probed points are marked in Figures 5-4 and Figure 5-7. It can be seen that the isolation gaps are able to successfully reduce the applied voltage to below 5 V after the last gap.

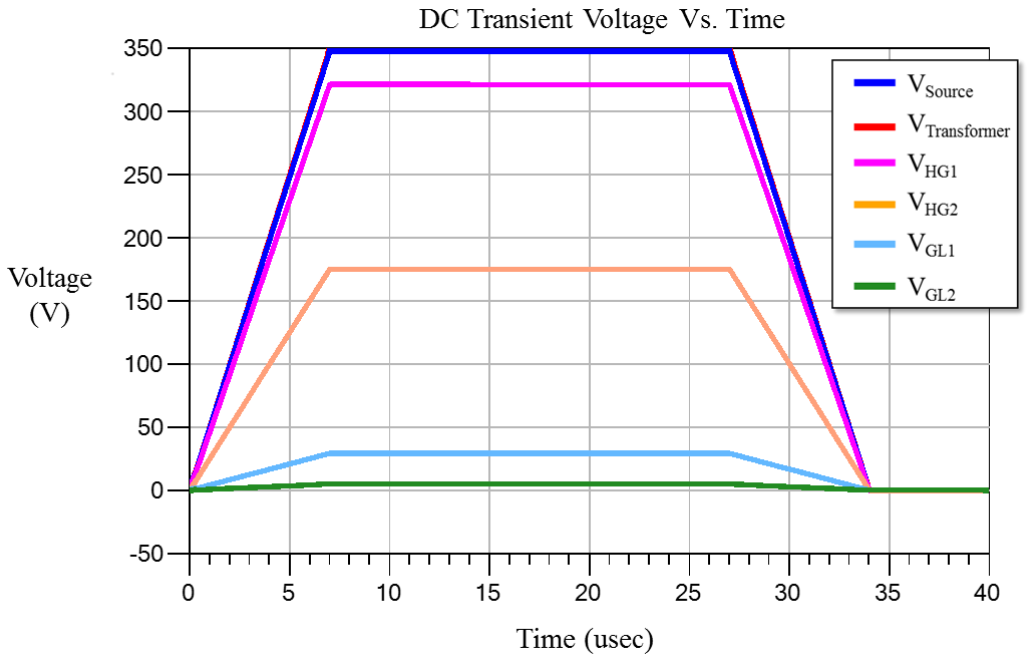



Figure 5-16 DC Transient Simulation on the High side Floating Ground

# CHAPTER 6

# RESULTS AND DISCUSSION

## 6.1 Overview

Previously in Chapter 3, the concept of chip to chip communication utilizing magnetically coupled resonators was demonstrated. In Chapter 4, the on-chip design realization and proof of performance through simulations was detailed. Chapter 5 introduced an equivalent lumped element model. This model used a combination of measurement results and EM simulations to extract unknown parameters and allow for transient simulations and ease of design optimization.

This chapter discusses the fabricated measurement structures, the procedure for measurement and de-embedding, and the measurements results.

The fabricated structures consist of: passive structures including fundamental resonator introduced in 4.1, the differential transformer introduced in 4.5.1, and the full High Side chip's passive circuitry. Moreover, the low side passive circuitry integrated with the active oscillator core as a free running oscillator was fabricated. It is expected that the passive structures will match with the simulation results in terms of resonance frequency and voltage gain. Since process variation, reliability and reproducibility is important in determining if the design concept is useful for future product, the measurement structures were fabricated on three different lots, and three data sets have been generated per structure.

## 6.2 Measurement Structures

### 6.2.1 Passive Structures

Figure 6-1 shows the layout and photos of the passive test structures with RF pads and grounding shield surrounding each structure. The RF pads are compatible with ground-signal-ground (GSG) 150μm probe pitch.

For the Fundamental Resonator structure, both signal pads are connected to the bottom plate of the MIM cap. The top plate of the MIM cap is connected to ground pads.

In the Transformer structure, one side of the primary is grounded and the other one is connected to the signal. On the secondary side, the signal line feeding the inductor on the left is floating, the center tap is connected to ground, and the coil on the right is connected to the signal pad.

For the High Side Chip structure, the signal line feeding the left inductor of the transformer is floating, the center tap of the transformer is connected to ground, and the coil on the right side of the transformer is connected to the top signal pad. The bottom of the High Side Chip structure would normally have a differential signal. But, for measuring the structure using single-eneded s-parameters and GSG probes, the right bondpad is connected to the input signal GSG and the left bondpad is connected to the ground pad.

### 6.2.2 Active Structures

A layout of the free-running oscillator and its die photo are shown in Figure 6-2. The oscillator circuit is placed under the LC tank. This circuit requires 5 V DC bias on the Vdd and enable pads to oscillate. Although this circuit is not the focus of the presented work, a single ended measurement was taken from one of the bondpads using a

DC probe connected to a spectrum analyzer. The measurement verifies the oscillation frequency.

## 6.3 Measurement Setup

Figure 6-4 shows a diagram of the RF measurement setup. The DUT is shown in green, placed over the chuck of an RF probe station. The RF probes (in gold) are placed over the DUT with RF cables connecting from GSG probes to the PNA (Programmable Network Analyzer). The PNA and Probe station used for measurements are shown in the pictures of Figures 6-4 and 6-5.

The test structures were simulated and mounted on a metal lead frame. To guarantee that the structures do not bounce or slide during probe touchdown, the metal lead frames were attached to a brass block.

The mounting structure can be seen in Figure 6-5 when it was been placed under an ACP GSG probe.

## 6.4 Calibration and De-embedding Approach

When performing RF measurements, the measured results by the PNA are not exactly the S-parameters of the DUT, since the RF connections, cables and probes have been included in the measurement. To ensure that measurements accurately reflect the stand-alone test structure's performance, an ISS-Cal Kit (Impedance Standard Substrate Calibration Kit) is used to de-embed probes and cables.

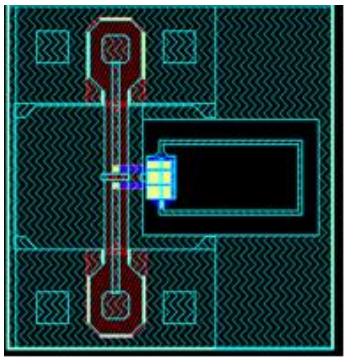
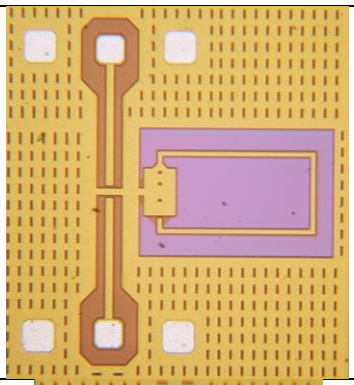
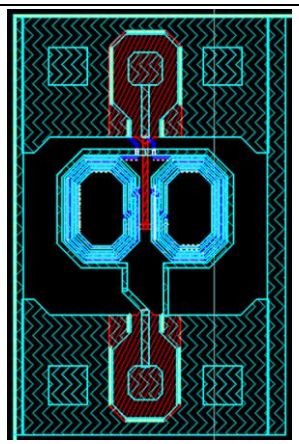
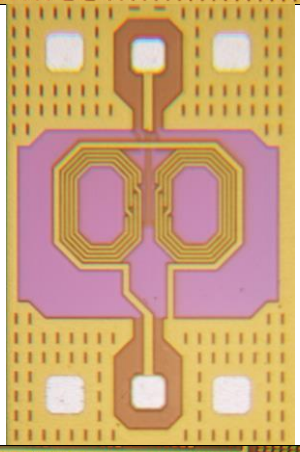
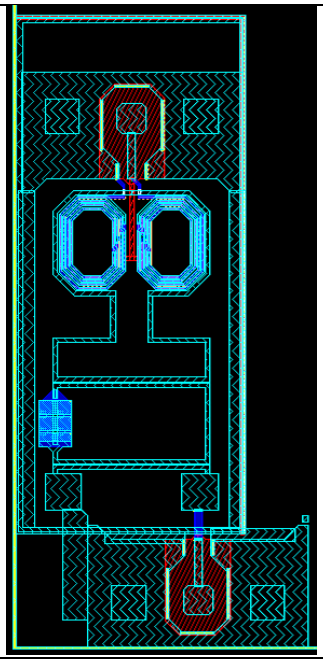
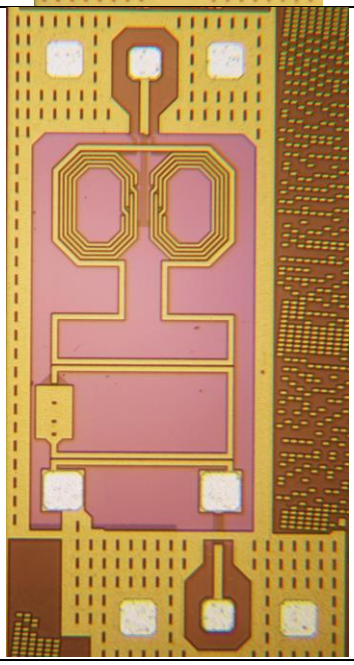
| Structure | Layout | Die Photo |
|---|---|---|
| Fundamental Resonator |  |  |
| Transformer |  |  |
| High Side Chip |  |  |

Figure 6-1 Passive Measurement Structures

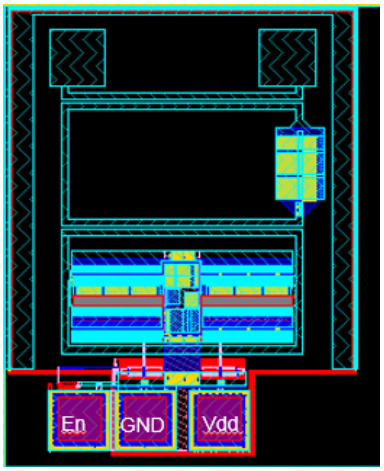
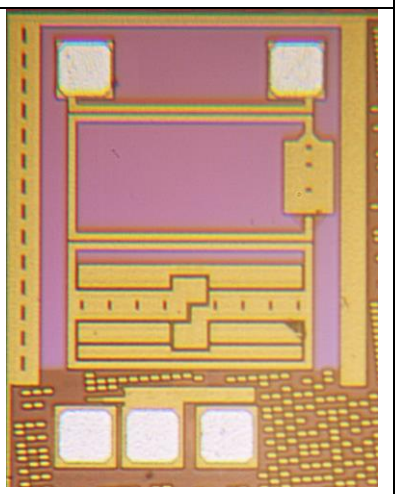
| Structure | Layout | Die Photo |
|---|---|---|
| Low side Chip |   |  |

Figure 6-2 Active Measurement Structure

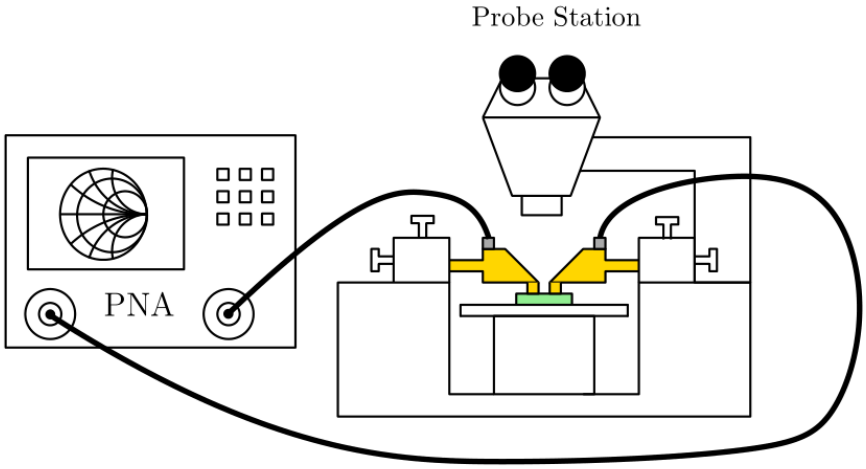
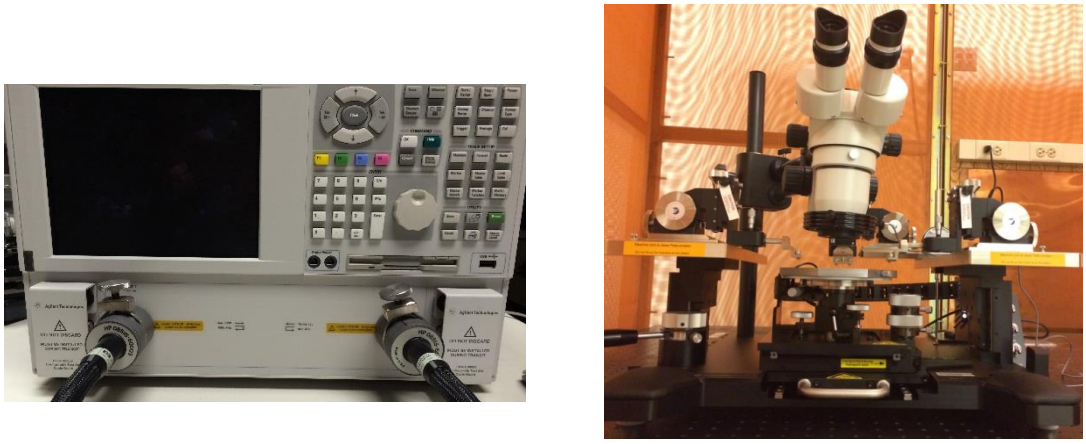



Figure 6-3 Schematic of RF Measurement Setup



(a) (b)

Figure 6-4 (a) Agilent PNA-E8361A (b) Cascade Microtech Probe station

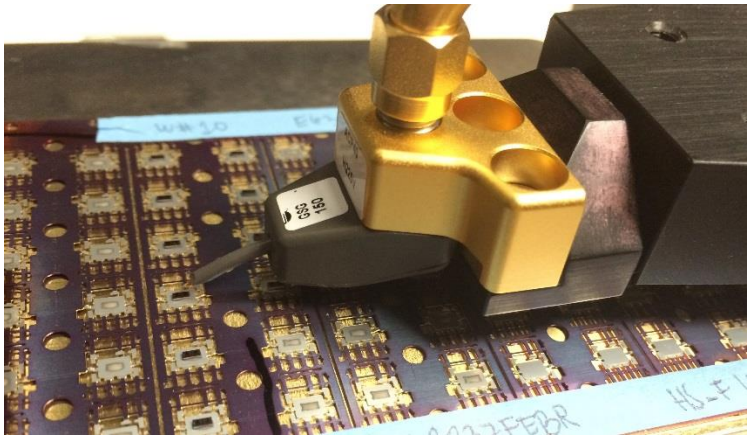


Figure 6-5 Dies placed in a metal frame under the GSG probe

The ISS-Cal consists of various de-embedding structures (e.g. shorts, opens, etc.) that calibrate the PNA measurements to the probe tips. However, going back to Figure 6-1, it is apparent that what is measured on chip is not only the device, but also includes the pads and on chip connections from signal and ground pads to the device. These measurement results are not comparable with the simulation results, since simulation results only include the devices. To de-embed the on chip pads and additional routing

parasitics to the test structure (device), it is necessary to include customized de-embedding structures on silicon.

In this study, short and opens are used to de-embed the pads. However, for the Fundamental Resonator, the structure was designed in a way to be accurately measured without needing de-embedding structures. A MATLAB code was developed to read the measured files (in Touchstone format), de-embed the structures using Pi and T models, and finally write the de-embedded structure as a Touchstone s2p file. The procedure for de-embedding each structure will be explained in details in the following section.

### 6.4.1 Open/Short De-embedding Utilizing Pi and T Model based on Y and Z

It has been proven that reciprocal two port networks can be represented as Pi and T models [27]. The Pi and T models based on Y and Z parameters are shown in Figure 6-6. The measured files are in terms of S-parameters and can be converted to either Z-parameter or Y-parameters [28].

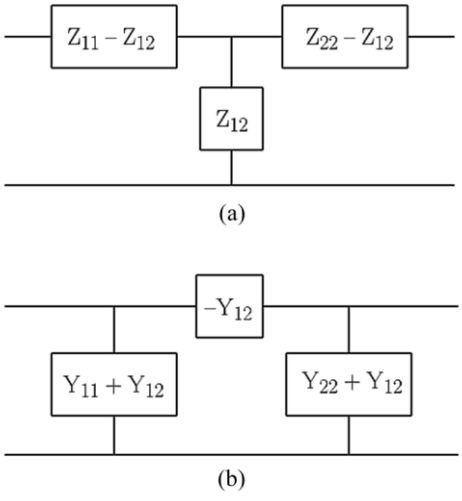



Figure 6-6 (a) T model (b) Pi model

One of the methods for de-embedding RF measurements is the Short/Open pattern method [29]. Figure 6-7 shows a device with parasitic elements around it. The Pi model parameters shown as green boxes can be found using the measurements from the open structure and equations in Figure 6-6 (b), while the T model shown in Figure 6-7 (blue boxes) can be extracted using a short measurement and equations in Figure 6-6(b). Note that the parasitic elements from the open measurement are still present in the short measurement. Therefore, for more accurate results, the open parasitic elements should be de-embedded from the short measurement results to get the T model parameters displayed in Figure 6-7.

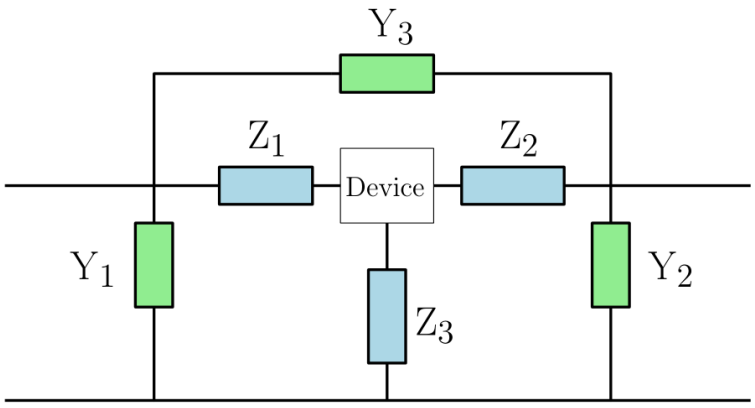



Figure 6-7 Pi and T Representation of Short/Open Parasitic Elements around the Device [25]

If a matrix of $Z_{Short}$ is defined as Z-Parameters extracted from the short, and a matrix of $Y_{Open}$ as Y parameters extracted from the open, the de-embedded result can be extracted using the following equation [30]:

$$Z_{De-embedded=}\left(Y_{Measured}-Y_{Open}\right)^{-1}-\left(Z_{short}^{-1}-Y_{open}\right)^{-1} \quad (6\text{-}1)$$

However, extracting $Z_{De\text{-}embedded}$ when $Y_{open}$ and $Z_{Short}$ are non-processed measured data from respective structures has a considerable drawback: the RF measurements are prone to measurement noise and when using equation (6-1), the noise extracted from the data is added to the measurements.

To reduce noise in this work, a data analysis has been initially done to determine the T and Pi parameters of Figure 6-7 in the form of physical parameters. Figure 6-8 (a) shows an equivalent of Figure 6-7, translated to a circuit diagram to represent the measurements in terms of physically meaningful parameters.

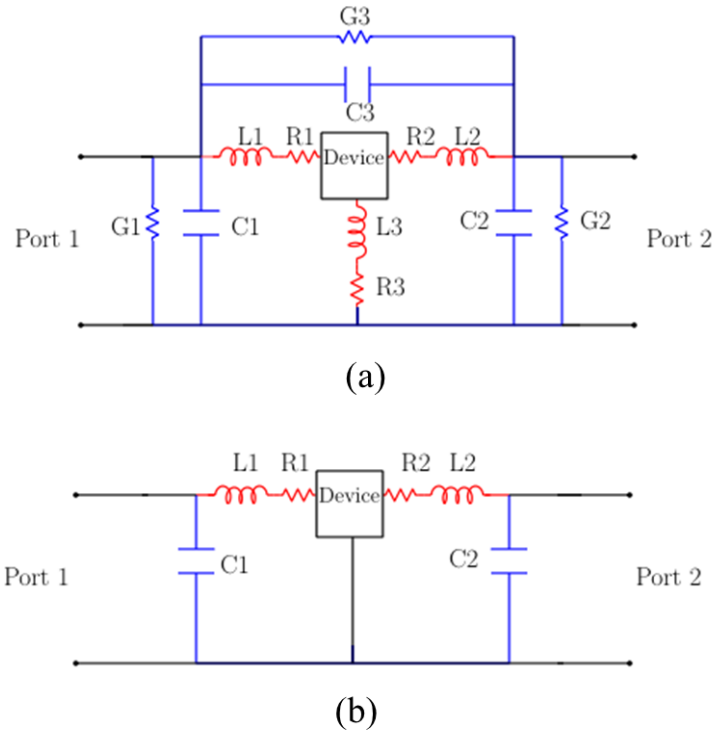



Figure 6-8 (a) Circuit Equivalent, and (b) Simplified Equivalent of Figure 6-7

The values of the parameters in Figure 6-8 are extracted using Table 6-1 equations.

Table 6-1 Pi and T Model for De-embedding

| Parameter | Equation | Parameter | Equation |
|---|---|---|---|
| **$C_1$** | $\mathrm{imag}(Y12 + Y11)/_{2\pi f}$ | **$G_1$** | $\mathrm{real}(Y12 + Y11)$ |
| **$C_2$** | $\mathrm{imag}(Y12 + Y22)/_{2\pi f}$ | **$G_2$** | $\mathrm{real}(Y12 + Y22)$ |
| **$C_3$** | $\mathrm{imag}(-Y12)/_{2\pi f}$ | **$G_3$** | $\mathrm{real}(-Y12)$ |
| **$L_1$** | $\mathrm{imag}(Z11 - Z12)/_{2\pi f}$ | **$R_1$** | $\mathrm{real}(Z11 - Z12)$ |
| **$L_2$** | $\mathrm{imag}(Z22 - Z12)/_{2\pi f}$ | **$R_2$** | $\mathrm{real}(Z22 - Z12)$ |
| **L3** | $\mathrm{imag}(Z12)/_{2\pi f}$ | **$R_3$** | $\mathrm{real}(Z12)$ |

Data analysis indicated that G parameters varied in a range of 0.1-100uS and were negligible. C3, L3 and R3 were also found to be 2-3 orders of magnitude smaller than those of other R, L and C values, and were therefore removed. The model in Figure 6-8 (a) was simplified to the model in Figure 6-8 (b). Data analysis indicated that the parameters in Table 6-1 were effected by measurement. Figure 6-9 shows the data from measurement of these parameters for the Transformer's de-embedding data. The plots contain spikes and oscillations that trend around an average value, with a mild slope. During the data analysis, the bad data sets (such as the Lot C curve for L2, which comes from measurement of a short structure) have been identified and eliminated. To make sure that de-embedding noise wasn't added to the measurements, the parameters in Table 6-1 were averaged over a valid range of frequencies and over measurement data from three lots (three measurements for each structure). The extracted averaged values are shown in Table 6-2 for all structures.

Using numbers from Table 6-2, updated $Y_{Open}$ and $Z_{Short}$ matrixes are defined and using Equation (6-1), the de-embedded data only contains won't contain noise from de-embedding data.

### 6.4.2 Fundamental Resonator De-embedding

As mentioned before, the top plate of the MIM capacitor is connected to the ground pads. The bottom plate of the capacitor is connected to the both signal pads. The extraction of Z12 from the measurement structure directly gives the input impedance of the resonator looking across its capacitor. No de-embedding structures are necessary, since the parasitic elements are excluded in Z12.

## 6.5 Measurement Results

With successful de-embedding of measurement results, a good comparison can be performed between measured data and predicted performance from simulation results. Comparisons are also made between various data sets from different lots. These comparisons deduce design performance success, simulation accuracy, measurement repeatability and reproducibility, and effects of the process variation on the system performance.

### 6.5.1 Measurement Characterization

As explained in 6.2, the full system was segmented into multiple sub-sections including the fundamental resonator (repeater), transformer, high side's receiver path and the low side integrated with the free running oscillator.

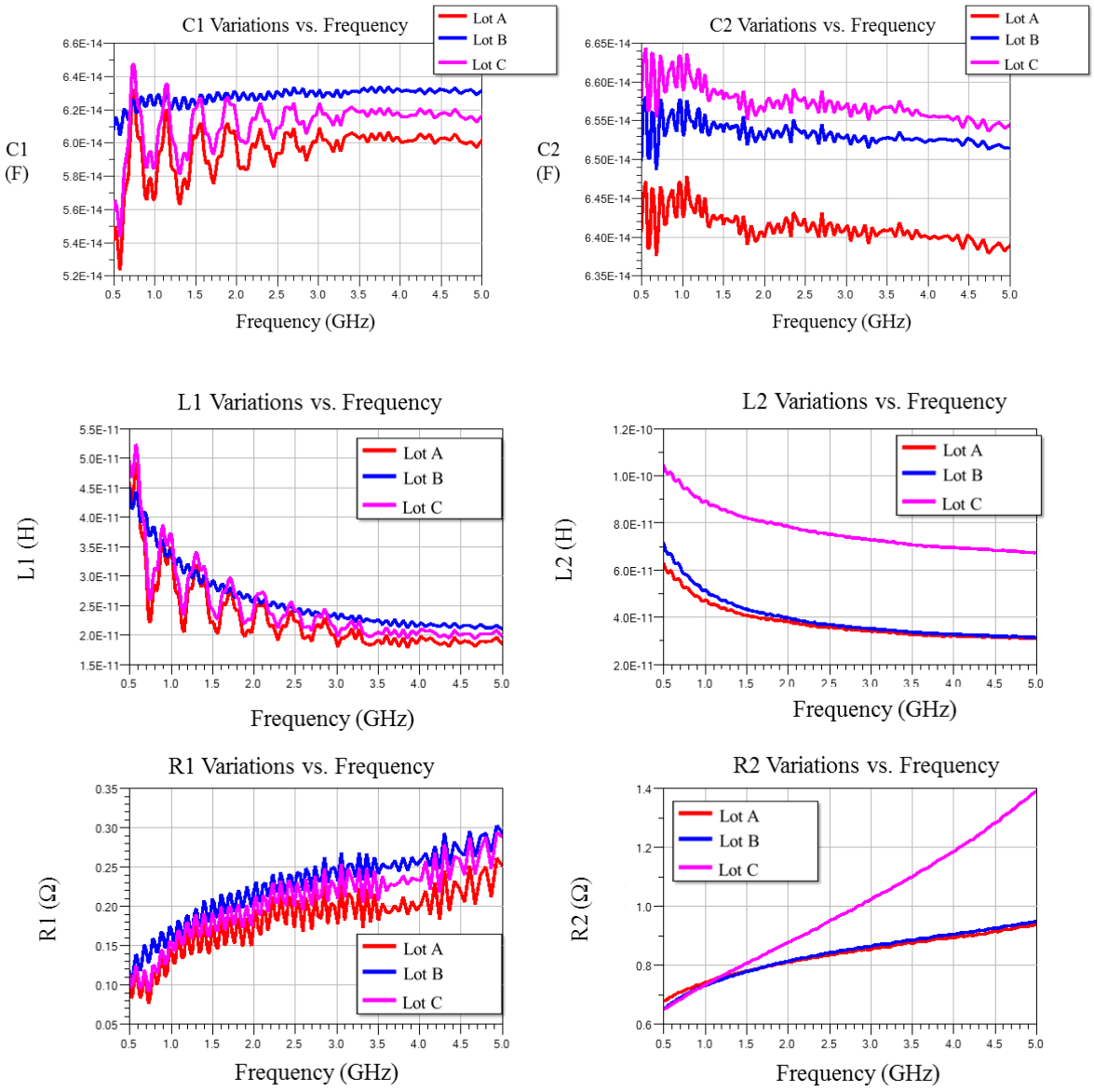



Figure 6-9 Transformer De-embedding Parameters

Table 6-2 Averaged De-embedding Parameters

| | Pi-model (Open) | | T-model (Short) | | | |
|---|---|---|---|---|---|---|
| **Structure** | **Cpi1 (fF)** | **Cpi2 (fF)** | **Lt1 (pH)** | **Lt2 (pH)** | **Rt1 (Ω)** | **Rt2 (Ω)** |
| Xformer | 61.8 ±1.4 | 64.7 ±0.6 | 21.6 ±1.6 | 34.7 ±0.5 | 0.22 ±0.02 | 0.86 ±0.01 |
| HS | 85.6 ±1.4 | 65.4 ±0.6 | 30.4 ±0.3 | 34.8 ±0.2 | 0.54 ±0.01 | 0.79 ±0.01 |

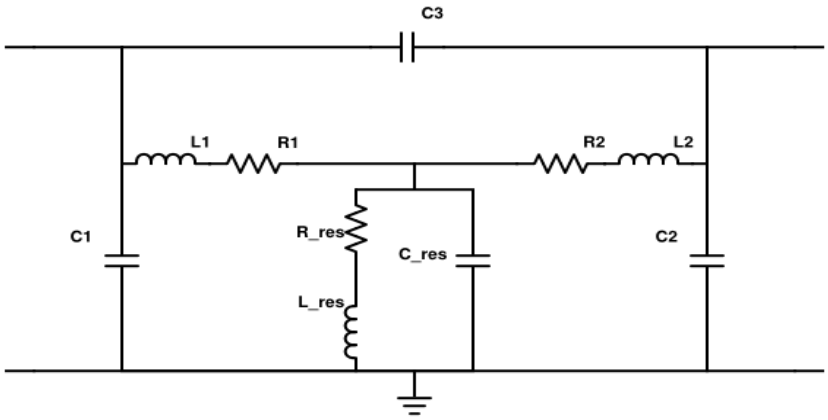



Figure 6-10 Circuit Diagram for the Fundamental Resonator

Answers to multiple questions are expected from measurements of each test structure, including those that have been asked in the research questions of Chapter 1.

### 6.5.2 Measurement Repeatability and Process Variations

A set of 3 measurements was taken from each passive structure, where each structure was taken from a separate lot. All of the test structures showed good agreement between the 3 samples, as illustrated by the measurements in Figure 6-11 (a) real and (b) imaginary parts. The measurements are overlaid for the three data sets of the fundamental resonator. This sample set shows similar performance with less than 3% error between lots.

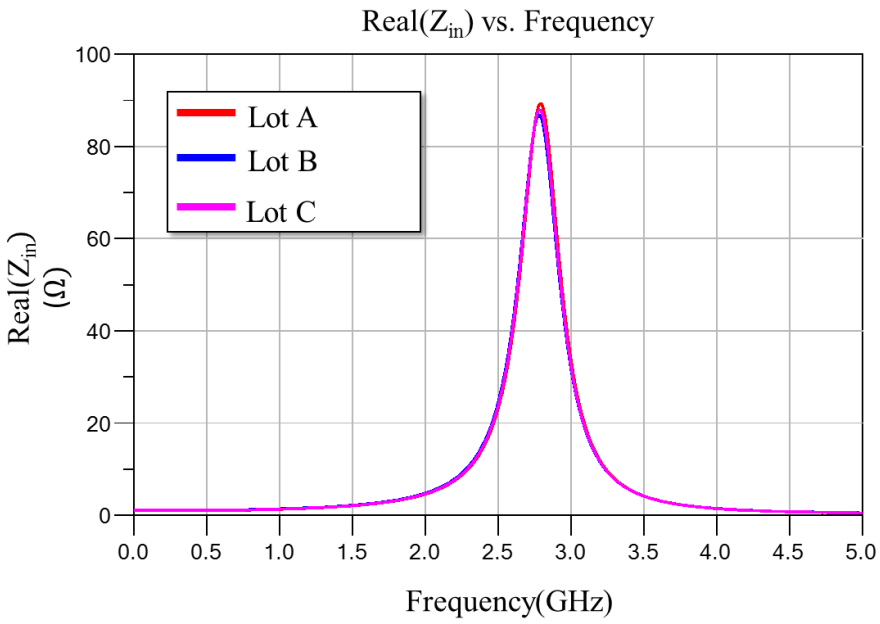
In order to avoid unnecessary complexity and to maintain clear graphs with high readability, the results of each test structure described in this section are presented using only one sample.

Table 6-3 Fundamental Resonator's Characterization Data Analysis

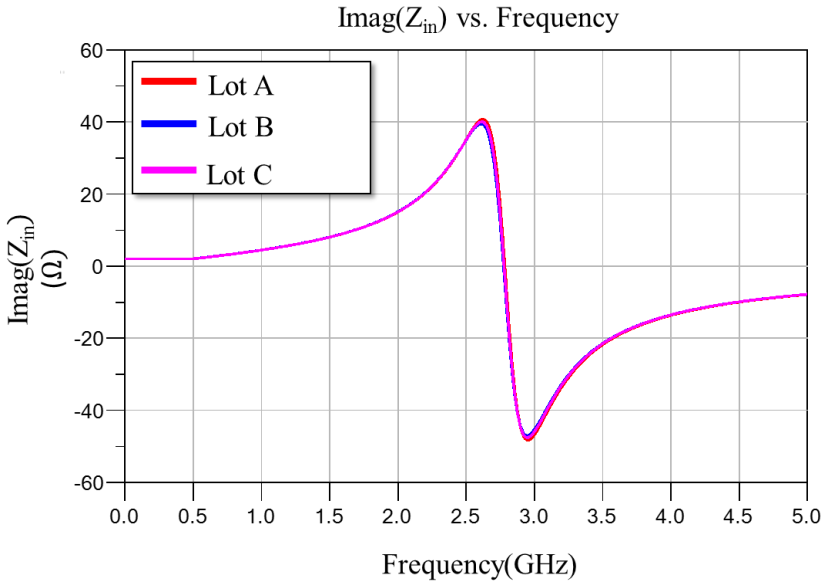
| Lot Label | R (Ohm) | L(pH) | C(pF) | f Individual Resonator (GHz) | f Resonator From HS (GHz) | % Δf |
|---|---|---|---|---|---|---|
| **A** | 1.30 | 590.7 | 5.47 | 2.783 | 2.775 | -0.29 |
| **B** | 1.22 | 594.5 | 5.47 | 2.773 | 2.750 | -0.83 |
| **C** | 1.22 | 592.7 | 5.47 | 2.777 | 2.750 | -0.97 |
| **Simulation** | 1.35 | 588.8 | 5.60 | 2.708 | 2.749 | -0.29 |

### 6.5.3 Fundamental Resonator

An overlaid plot of input impedance looking across the resonator capacitors has been shown in Figure 6-12 for both the real part and imaginary part. As Figure 6-12 illustrates, the results from measurement are in good agreement with results from EM simulation for both the real and imaginary impedances. The equivalent inductance of the measurement is slightly higher than that of simulations. Also, the resonance frequency is 80 MHz higher than simulated. The real part suggests a higher resistance at resonance from that of the measurements. In order to compare between results from three data sets and results from simulations using the equivalent circuit in 4.1, an identical approach has been taken to extract values for R, L and C. The error percentage of simulation results in comparison with measurements for R, L, C, and $f_{Resonance}$ stands within 3%. The resonance frequency of the repeater in the high side structures was also measured and compared with the simulation.




(a)




(b)

Figure 6-11 Fundamental Resonator $Z_{IN}$ for lots A, B and C (a) Real Part (b) Imaginary Part

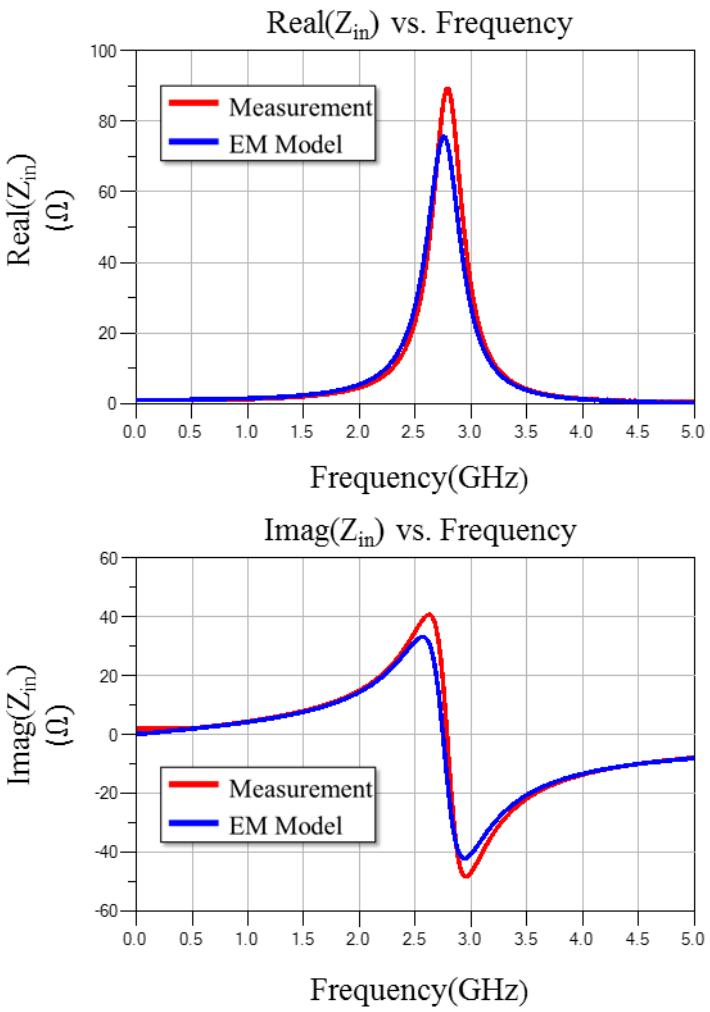



Figure 6-12 Measurement and EM Simulation Result Comparison For Real (top) and Imaginary (bottom) Part for Fundamental Resonator's Input Impedance

As Table 6-3 indicates the difference between two frequencies of the same lot is less than 1%, which meets both design reliability and validates the High Side Chip's resonator performance.

### 6.5.4 Transformer

A comparison between results from de-embedded measurement, EM simulation, and LEM of the transformer is shown in Figures 6-13 and 6-14 using overlaid plots. The comparison has been done on input and output resistance, effective inductance, and voltage gain. The plots show the aforementioned parameters for the primary side on the left column plots and for the secondary side on the right column plots. All plots show similar trend in terms of slope and shape. The plots are matched up to 3 GHz.

The LEM performance could be improved if a more distributed model is used for the transformer. But, the most important behavior is that near the operation frequency, which LEM fits well with the measurements.

For the primary plots on the left, all three curves are matched for up to 3 GHz with less than 15% deviation from the measurement and less than 10% deviation at 2.8 GHz. The models do not match well with the measurements for higher frequencies, especially when comparing LEM with the measurements. Effective inductance (L) for the primary side shows the LEM and EM simulation have less than 20% difference from measurements for up to 3 GHz and remain within 10% of the measurement result for 2-3 GHz.

For the secondary side on the right plots, the lumped element fits well with the measurement results, and the output resistance and L of the measurement are in good agreement with the LEM for up to 5 GHz. The secondary resonance frequency of the measurement is 4.93GHz, while the results from LEM and EM simulation show 4.77 GHz and 4.78 GHz, which is less than 5 % error between measurement and models.

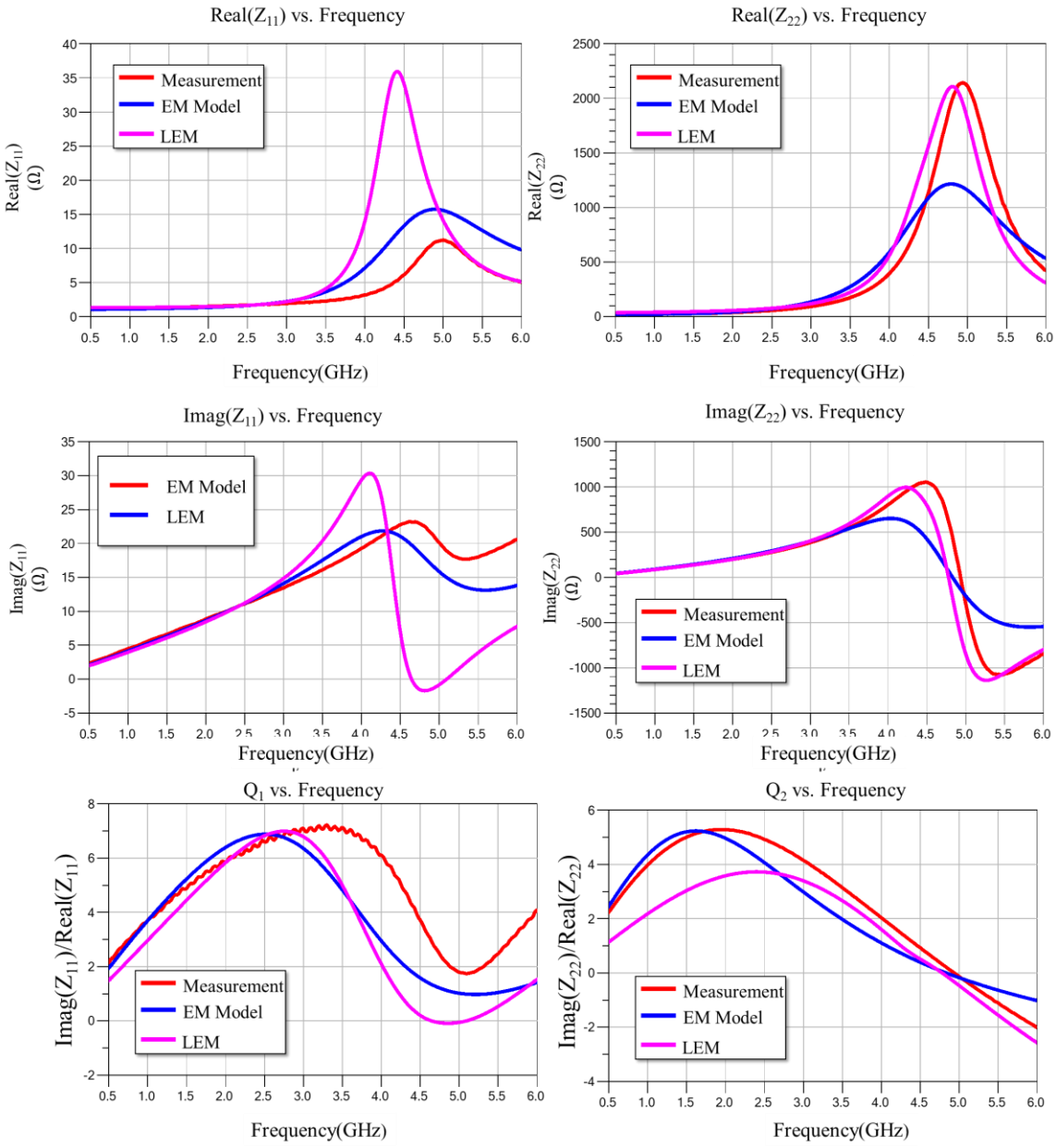



Figure 6-13 Unloaded (195 fF) Transformer Input/output Comparison between Measurement, EM simulations and LEM

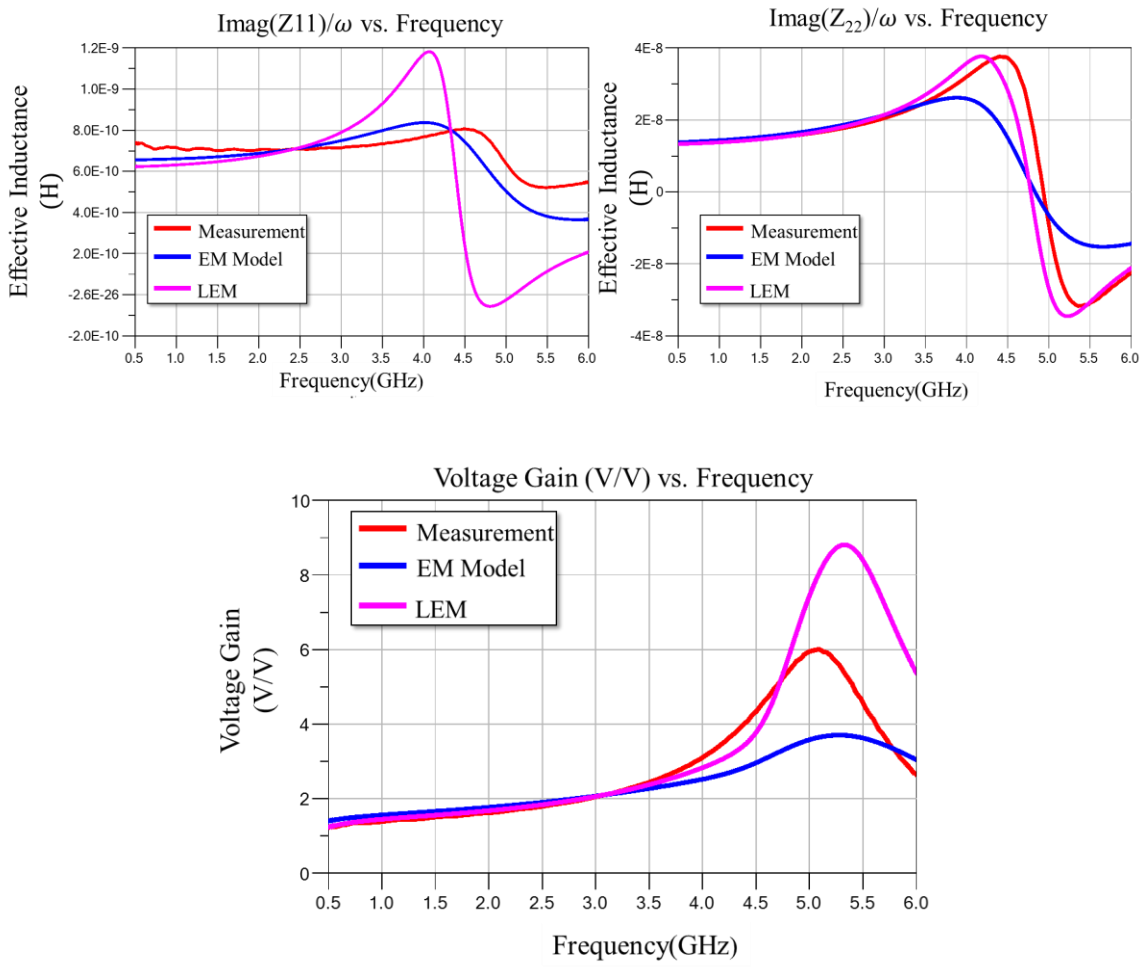



Figure 6-14 Unloaded Transformer Effective Inductance (top) and Voltage Gain (bottom) Comparison Between Measurement, EM Simulations and LEM

For the voltage gain, the results show that both measurements and models are in good agreement with each other from 500 MHz to 3GHz, and the deviation from measurement is less than 5% when comparing to EM simulation and less than 2% in comparison to LEM.

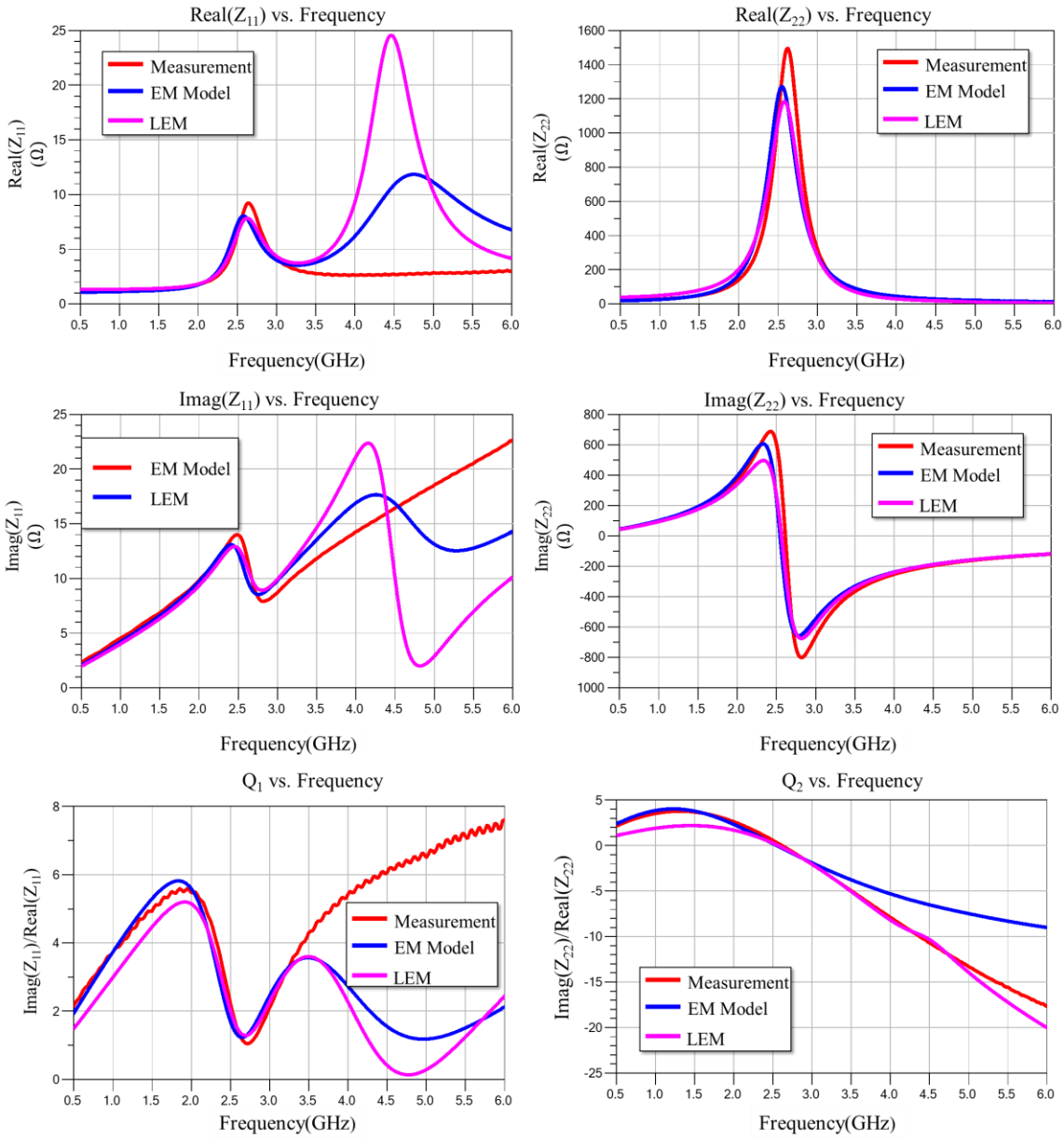



Figure 6-15 Loaded (195 fF) Transformer Input/Output Comparison between Measurement, EM Simulation and LEM

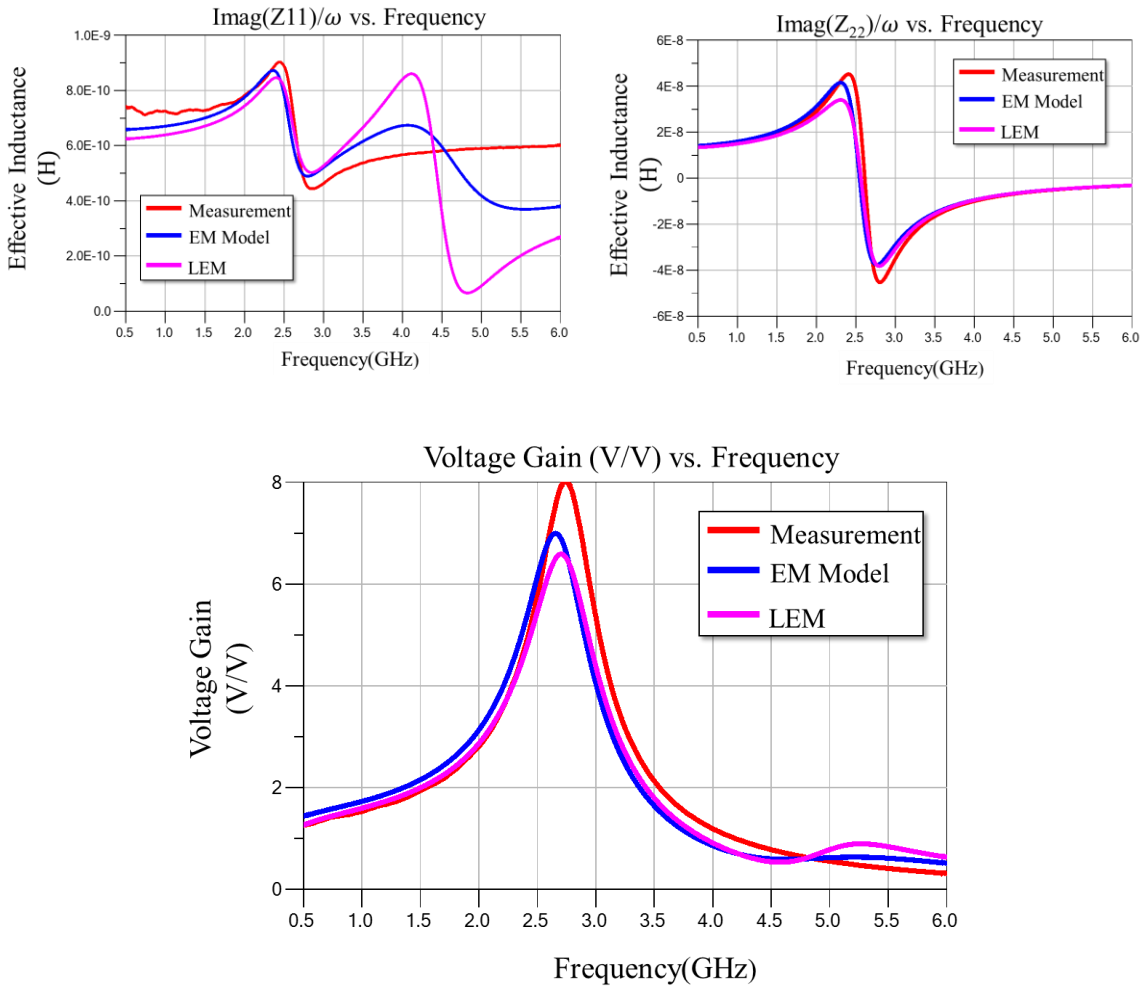



Figure 6-16 Loaded (195 fF) Transformer Effective Inductance (top) and Voltage Gain (bottom) Comparison between Measurement, EM Simulation and LEM

The same circuit parameters are also plotted when the transformer is loaded with the receiver's input capacitance. Figure 6-15 and Figure 6-16 show the plots for the transformer loaded with 195 fF capacitance. Similar to the unloaded condition, analyzing the data shows good agreement between the results for up to 3 GHz, and the voltage gain indicates that the transformer when loaded has a gain peak at 2.5 GHz. Both the EM

simulation results and LEM are within 100 MHz of the measured results, with less than 25% error in the peak value.

Therefore, the transformer is peaking very close to the operation frequency of 2.8 GHz, and the simulations are having reasonable accuracy in estimating the resonance frequency. In addition, the overall results of the transformer prove that the transformer is successfully stepping up the voltage and has a gain performance higher than predicted from the EM simulation.

### 6.5.5 High Side Chip

The measurement results for the High Side Chip are plotted in Figures 6-17 and 6-18, where port 1 is connected to the input of the Highside Chip and port 2 is connected to the output (transformer side).

From the input resistance looking into the bondpad side (of the de-embedded structure), one can see that there is resonance at a frequency of 2.75 GHz. This is the resonance frequency created by the repeater (resonator) coupled directly to the bond pad inductor. Similarly, from the resistive and imaginary parts of the receiver side's impedance, there is a resonance at 5.5 GHz. Comparing these plots with the plots from the previous section for the transformer, it is apparent that this resonance comes from the transformer's self-resonance. Moreover, the voltage gain shows a peak at 2.8 GHz.

Comparison of the results obtained from EM simulations with measurements demonstrate that the input resistance (bond pad side) matches well. However, the inductance value (L) has 25% error and is smaller in EM than in measurement. The results for the transformer side of the chip are similar to the previous section.

The LEM results correlate with the measurements for bond pad inductance, and there is an intersection with the measurement result at 2.8 GHz. The input resistance at resonance shows LEM values higher than measurements, and the voltage gain is at least 2 times higher in the LEM than the measurement. However, the EM simulation and LEM results for voltage gain are very close. This happens because extraction of the internal parameters, such as capacitance across gaps, was not possible directly from the fabricated test structures, and therefore, those parameters were extracted from the EM simulation. The LEM can be more closely fit to measurements by tuning the model parameters; however, the cost is unrealistic values or values inconsistent with the low side LEM.

When loading the high side chip with a 195 fF capacitance, the resonance frequency of the transformer is pushed to 2.8 GHz and has an increased voltage gain, as shown in Figures 6-19 and 6-20.. The input and output impedance curves match relatively well between loaded and unloaded conditions.

Looking at Figure 6-20, a total voltage gain of 1.06 is achievable from the measured structure, whereas the EM simulation predicts a gain of 1.24 and LEM predicts a gain of 1.63. The peak frequencies for measured, EM simulation, and LEM are 2.76, 2.79 and 2.86 GHz respectively, which has less than 5% error from measurements.

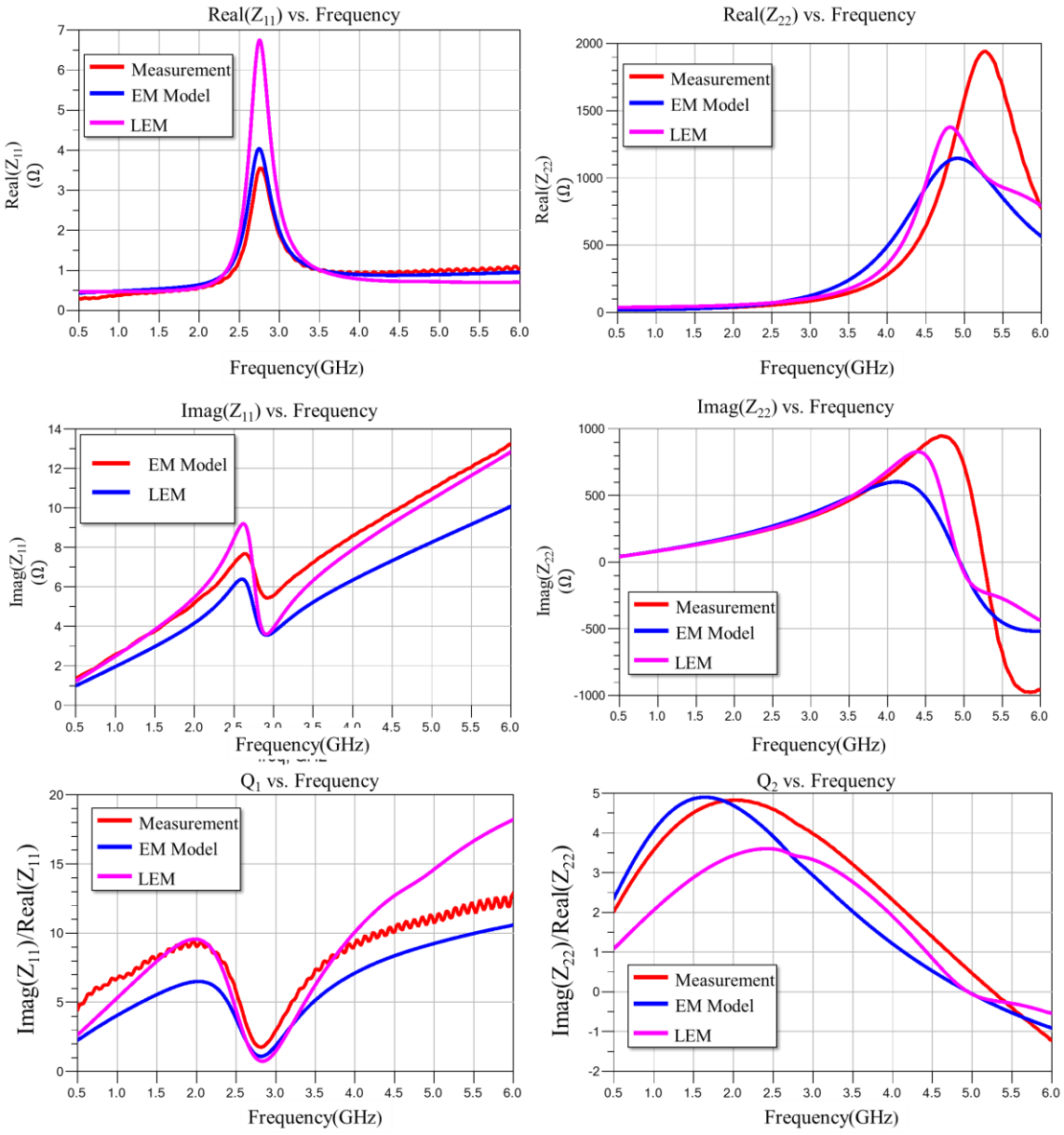



Figure 6-17 Unloaded High Side Chip's Overlaid Results of Input/Output Performance from Measurement, EM Simulation and LEM

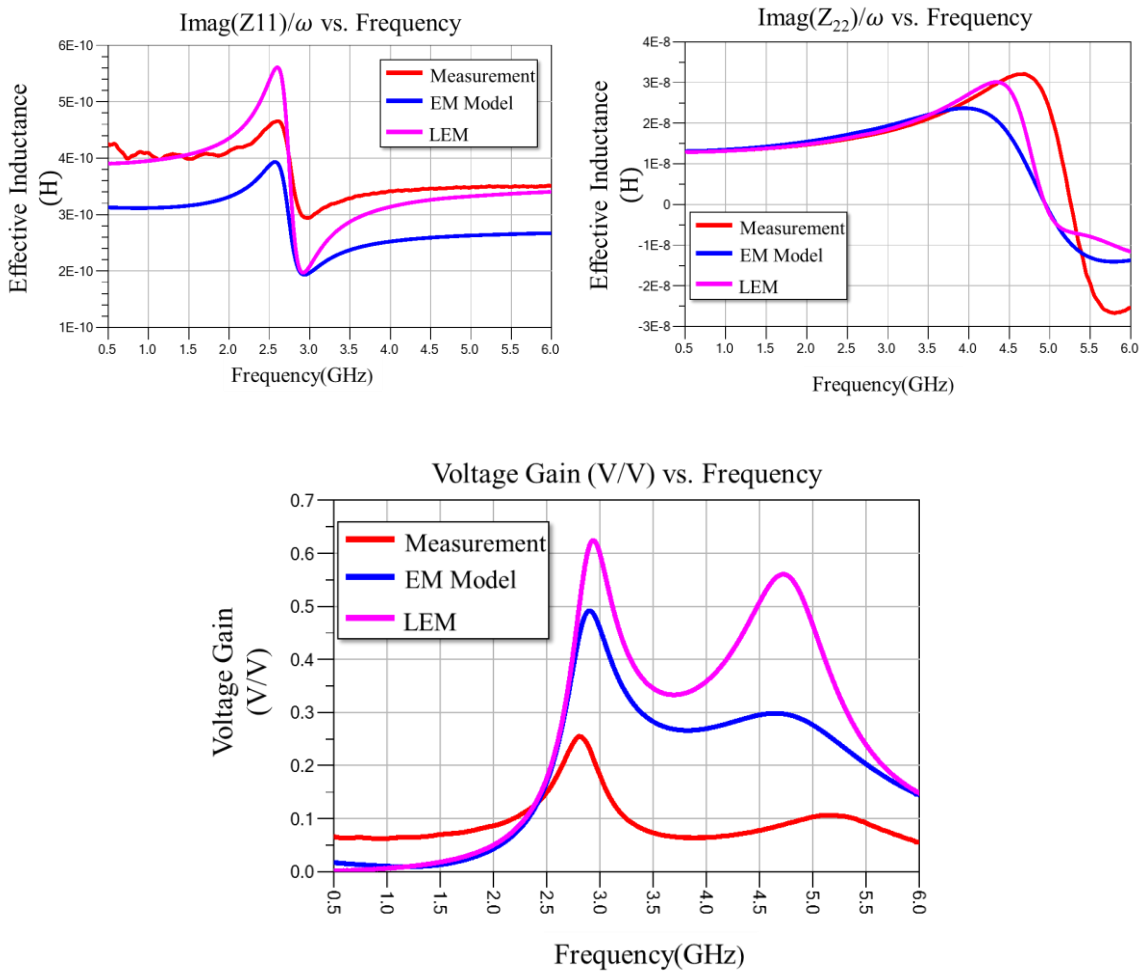



Figure 6-18 Unloaded High Side Chip's Overlaid Plots of Effective Inductance (top) and Voltage Gain (bottom) from Measurements, EM Simulation and LEM

The results for both unloaded voltage gain and loaded voltage gain has an important conclusion, that signaling through magnetic coupling is possible, and the proposed coupling can provide a voltage gain and general behavior close to simulated predictions.

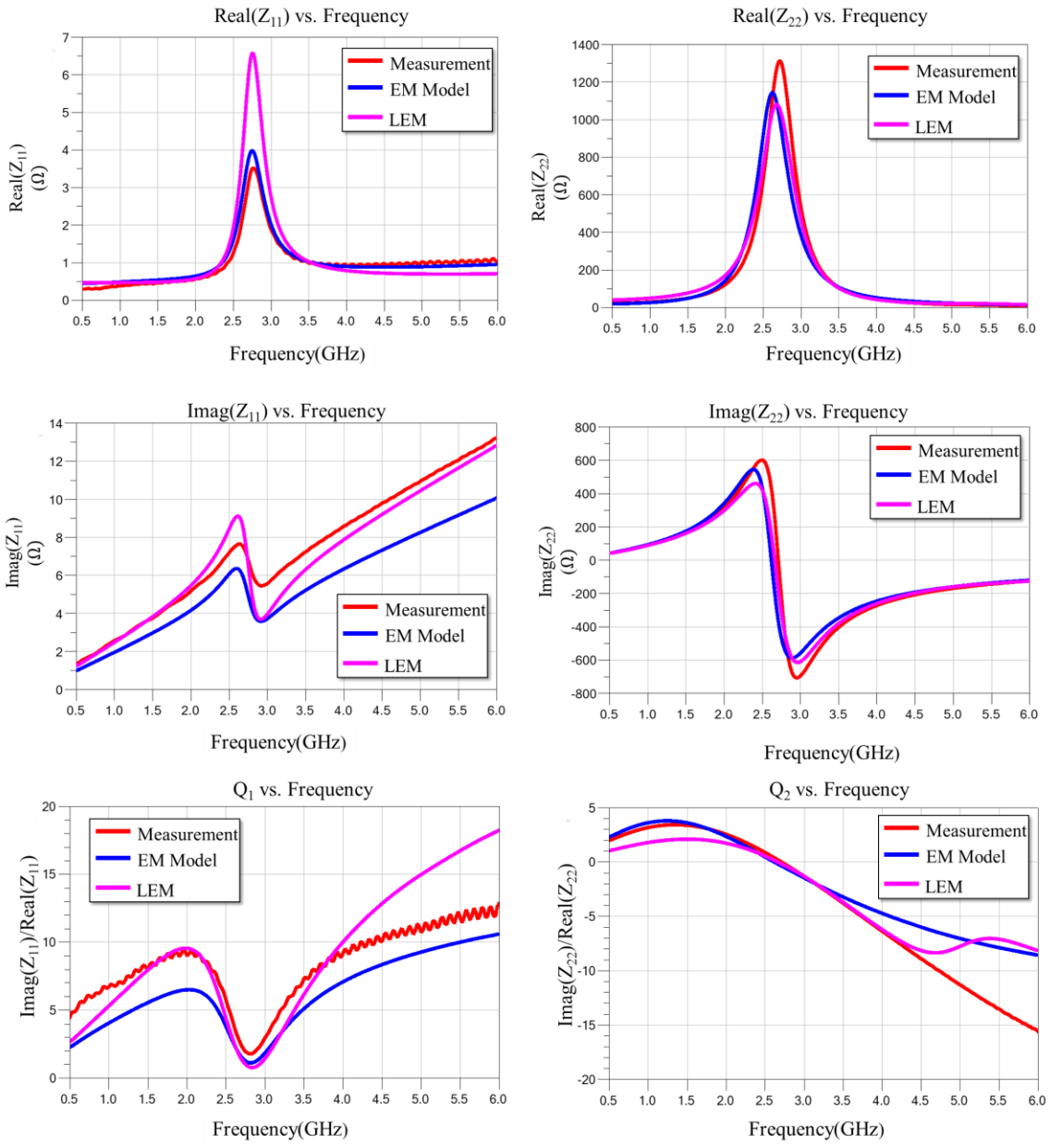



Figure 6-19 Loaded (195 fF) High Side Chip's Overlaid Results of Input/Output Performance from Measurement, EM Simulation and LEM

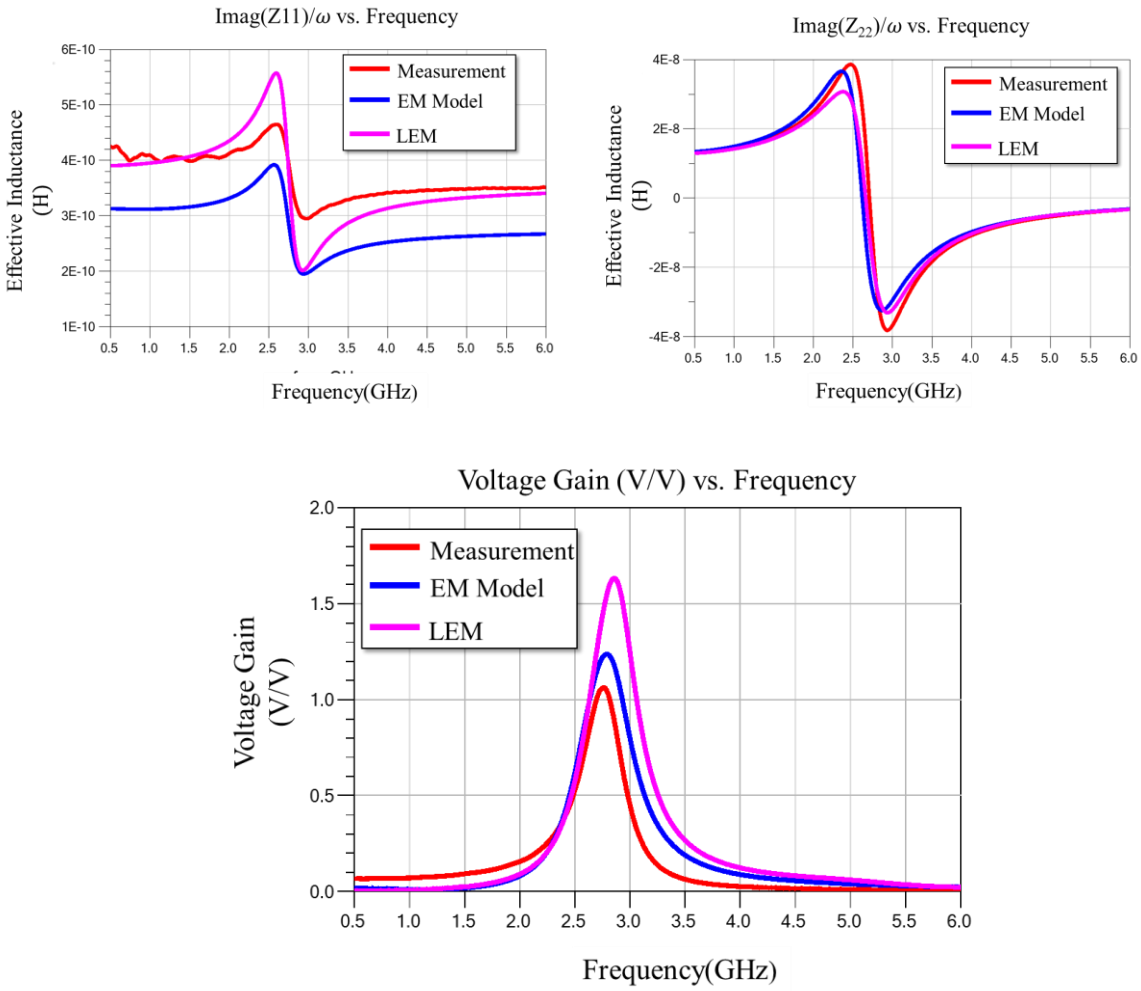



Figure 6-20 Loaded (195 fF) High Side Chip's Overlaid Plots of Effective Inductance (top) and Voltage Gain (bottom) from Measurements, EM Simulation and LEM

### 6.5.6 Low Side Chip

The low side structure has been measured using a spectrum analyzer connected to a DC probe, measuring the single ended output from one of the output bond pads of the low side chip. The enable and VDD pads were connected to 5V, and the GND pad is grounded.

As Figure 6-21 displays, the low side circuit oscillates at 2.817 GHz and drifts to 2.834 GHz. This is in good agreement with simulations in Chapter 4, where a 2.83 GHz oscillation frequency was predicted for the unloaded oscillator. The output voltage measurement results are not presented, since neither differential measurement nor RF probes have been used in this measurement procedure.

The oscillator consumed 350 mA DC current, which means 1.75 W power for the free running oscillator. From this, the maximum power consumption for the circuit is projected when assuming a 500 kHz digital input signal. For every digital pulse, the oscillator is turned on for 10 ns on a digital signal's rising edge and 5ns for the falling edge. This means a total of 15ns. Since the input signal is expected to have a maximum frequency of 500 kHz, the maximum power consumption is:

$$Pmax = 500k \times 15n \times 1.75 = 13.12\ mW \qquad (6\text{-}2)$$

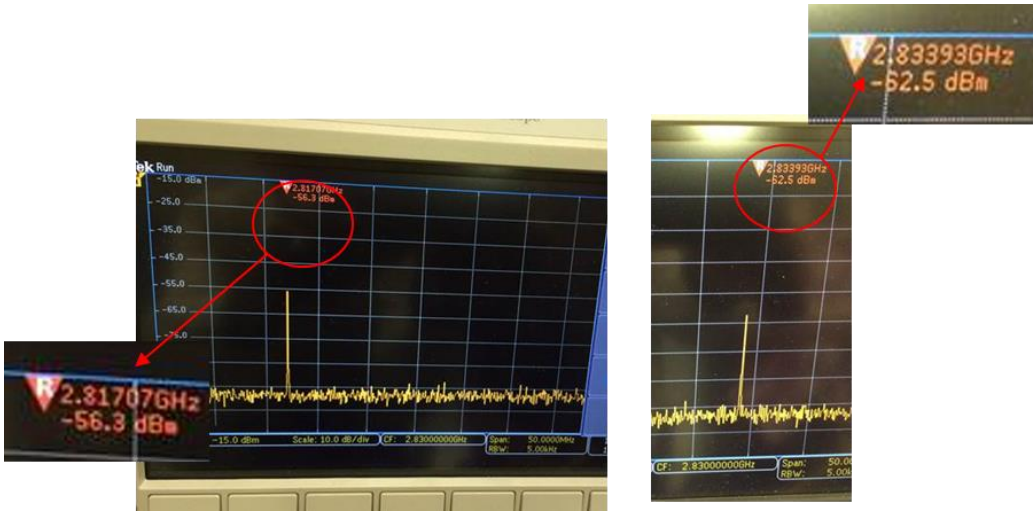



Figure 6-21 Snapshot of Spectrum Analyzer during Measurement of Low Side Chip's Oscillation Frequency (two oscillation frequencies indicate the frequency drift range)

# CHAPTER 7

# CONCLUSION

In summary, this work proposes a novel method for on-chip galvanic isolation utilizing magnetic coupled resonators. This design not only shows good performance in terms of high voltage isolation and communication across the isolation barrier, but the design integrates in silicon CMOS for low cost and small chip areas.

This work focuses on the design of a communication channel, which allows for signal communication and high voltage isolation. The functionality of the communication channel was verified using Full-wave EM simulators. The communication channel is able to provide a voltage gain required for meeting the requirements of a basic (low cost) receiver circuit's sensitivity. The communication channel has been simulated with an oscillator connected to its input (on Low Side Chip). The entire system simulation proved that the channel successfully generates and receives a signal with propagation delay shorter than the 15ns design specification. The communication channel was designed for OOK modulation, which has been chosen to minimize the system's power consumption. The oscillator circuit was successfully integrated below the communication channel to minimize the die area.

The High Side Chip, Transformer, and Fundamental Resonator were fabricated to verify design concept and performance. The measurement results show negligible process variation, and high design reproducibility and repeatability. The measurement results are in good correlation with EM simulations and the developed lumped element models (LEM). The LEM was developed to simulate transients and the condition when DC

transients appear on the floating ground of the high side circuitry. The close correlation between all results means that transferring a signal using magnetically coupled resonators has been done successfully, and the developed models can be used with confidence in future fabrication cycles to optimize system performance. Table 7-1 shows performance metrics derived from measurements and simulations. It is apparent that all sub-blocks are resonating at the same frequency, with closely matched parameter values.

Table 7-1 System Performance Conclusion

| Specification Name | Specification | Unit | Source* |
|---|---|---|---|
| Minimum HV Isolation | 700 | V | S |
| Maximum Propagation Delay | 12 | ns | S |
| Maximum Die Area | 0.8 | $mm^2$ | - |
| Voltage Gain From High side Chip | 1.06 | V/V | M |
| Fundamental Resonator Resonance Frequency | 2.78 | GHz | M |
| Oscillation Frequency** | 2.817-2.834 | GHz | M |
| Transformer Resonance Frequency | 2.74 | GHz | M |
| High Side Resonance Frequency | 2.76 | GHz | M |
| Biasing Voltage | 5 | V | M |
| Oscillator's Power Consumption @ 500kbps | 13.12 | mW | Projected from measurements |

* M: Measurement S: Simulation

** Oscillator was measured without being attached to the High Side Chip. When loaded by the high side, the resonance frequency is expected to shift to slightly lower frequency.

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