Radiation Detection and Imaging:

Neutrons and Electric Fields

by

Hugh E. Chung

A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science

Approved July 2015 by the
Graduate Supervisory Committee:

David R. Allee, Chair
Antonia Papandreou-Suppappola
Keith E. Holbert

ARIZONA STATE UNIVERSITY

August 2015

ABSTRACT

The work presented in this manuscript has the overarching theme of radiation. The two forms of radiation of interest are neutrons, i.e. nuclear, and electric fields. The ability to detect such forms of radiation have significant security implications that could also be extended to very practical industrial applications. The goal is therefore to detect, and even image, such radiation sources.

The method to do so revolved around the concept of building large-area sensor arrays. By covering a large area, we can increase the probability of detection and gather more data to build a more complete and clearer view of the environment. Large-area circuitry can be achieved cost-effectively by leveraging the thin-film transistor process of the display industry. With production of displays increasing with the explosion of mobile devices and continued growth in sales of flat panel monitors and television, the cost to build a unit continues to decrease.

Using a thin-film process also allows for flexible electronics, which could be taken advantage of in-house at the Flexible Electronics and Display Center. Flexible electronics implies new form factors and applications that would not otherwise be possible with their single crystal counterparts. To be able to effectively use thin-film technology, novel ways of overcoming the drawbacks of the thin-film process, namely the lower performance scale.

The two deliverable devices that underwent development are a preamplifier used in an active pixel sensor for neutron detection and a passive electric field imaging array. This thesis will cover the theory and process behind realizing these devices.

ACKNOWLEDGEMENTS

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ix

xiv

Chapter 1

INTRODUCTION

1.1 Problem Scenario

There has been an ever-increasing need of vigilance in the United States as the alert on terrorism continues to rise [1]. The use of explosive devices is unfortunately one all-too-common medium terrorists use to inflict harm on the masses while ensuing public panic. These bombs are often constructed with simple circuitry and have even contained radioactive materials in the form of radiological dispersal devices (RDD) [2], more commonly referred to as dirty bombs.

The Boston Marathon Bombing of 2012 is one such tragedy in which explosives were detonated, killing three and injuring 264 in the worst attack on U.S. soil since the attacks of September 11 [3]. During the aftermath, explosive ordnance disposal (EOD) personnel went about a frenzied search for more explosive devices that may have been left behind or planted at the scene [4].

With hundreds of backpacks left behind, the search was dangerous and inefficient. The research presented in this manuscript provides a solution that could alleviate the burden of such a task with the use of non-invasive detection systems. Namely, an electric field imager could provide a picture of active wires within a bag or container so that EOD personnel can safely determine whether a bomb is present. The use of a device such as a neutron detector can also determine whether a bomb poses a radioactive threat.

1.2 A Little Background

Materials can emit distinct radiation signatures and the ability to detect such radiation would allow for noninvasive measures to pinpoint the source. The term "radiation" in the

colloquial frequently evokes the subject of special nuclear materials (SNMs) as it poses a great concern for national security. However, other common forms of radiation include light, heat, sound, and electric fields. This thesis will focus on nuclear radiation in the form of neutron detection as well as electric field radiation in the form of very low frequency electric field imaging.

Finding such radiation sources are not only difficult to detect due to high environmental noise and sparsity of signal strength, but current methods encounter issues in cost, a shortage of supply in materials, size/portability, as well as general lack in performance and efficiency. This poses a need to find novel and efficient methods of radiation detection. There is a particular interest in implementing such systems on flexible substrates so both traditional and flexible processes were used to fabricate the devices.

Topics to be covered include an overview of the current state of the art and current challenges faced, the development and implementation of sensing arrays to detect neutrons and image electric fields, and the results of the experiments in both simulation and demonstration. While detecting neutrons and electric fields may have overlap in application, the mechanisms for the each are considered to be two independent problems. Therefore, it is worth noting that it is not the objective of this research to build an all-in-one device that both detects neutrons and images electric fields.

1.3   Organization of the Thesis

This thesis will be divided into two parts. The first part, covered by Chapters 2-5, will cover neutron detection while the second part, covered by Chapters 6-12, will cover electric-field imaging. These two parts will be preceded with the current Chapter, the introduction, providing a broad overview of background information as well as the research objectives.

Part I begins with Chapter 2 which discusses the proposed large area thin film transistor (TFT) active pixel sensor (APS) approach to neutron detection and a comparison to current

methods. Chapter 3 will discuss the evolution of the in-pixel pre-amplifier design over the generations and cover both the simulation and experimental results. Chapter 4 will cover the system level of the detector including integration efforts and array layout circuitry. Finally, concluding Part I, Chapter 5 will discuss future work to be done including full integration and array fabrication.

Part II begins with Chapter 6 which covers background of electric field sensing with a focus of D-dot sensors and why it was chosen for this research. Chapters 7 and 8 cover designs and results of a 1-dimensional and 2-dimensional D-dot array respectively and Chapter 9 and 10 cover solutions for the shortcomings of the 2-dimensional array by means of a 1-dimensional stepper and inverse problem algorithms such as computed tomography. Finally, Chapter 11 will conclude the thesis by discussing future work to be done in electric field imagining including a possible extension into magnetic field imaging.

The thesis will all be wrapped together in the final chapter which includes concluding thoughts on large area neutron detection and electric field imaging and the implications of both on the future, including further research and derivative topics.

1.4   Neutron Detection

A large emission of neutrons is a confident and fairly unique indicator of the presence of SNMs. Therefore, an improved performance in neutron detection would directly correlate to a greater ability to detect and defend against SNMs. This is useful in areas such as high security military bases and ports of entry [5], [6]. The methods to detect neutrons are indirect and rely on an interaction with a material to produce charged particles which are processed [7].

The uncharged nature of neutrons means they have minimal interactions with electron clouds, colloquially referred to as "empty space," because they do not ionize with atoms by means of coulombic interaction. Since the electron cloud constitutes the vast volume of an

atom, neutrons easily penetrate most matter, making it difficult to "catch" unlike gamma rays.

A neutron would essentially only undergo an interaction if it were to directly collide with the nucleus of an atom. While the material under test will depend on various parameters such as nucleus size and the energy of the neutron, as a frame of reference, the ratio of the combined volume of a proton and electron to the volume of a hydrogen atom as a whole is $1 : 9.9999999999314 \times 10^{13}$, making the probability of a neutron directly colliding with a proton exceptionally small.

In the instance that a neutron does interact with a nucleus, the neutron will either undergo scattering or absorption. If the neutron is scattered by the nucleus, a portion of the kinetic energy from the neutron will be transferred into the nucleus and can be either elastic or inelastic. In the case of absorption, there are multiple manners in which it can manifest including electromagnetic (release of gamma rays), neutral (release of more neutrons), fission (release of fission fragments), and charged absorption (release of charged particles) [8]. The approach of neutron detection in this thesis takes advantage of the charged absorption phenomenon for thermal (i.e. "slow") neutron detection which have energies below the cadmium cutoff of 0.5 eV [9]. Other methods of neutron detection and spectroscopy will not be covered as they do not immediately pertain to the research conducted.

There are a handful of isotope anomalies that have a high absorption cross section, seen in Table 1, such as ^{10}B and ^{6}Li that have a relatively high probability for slow incident neutron interaction. Such an interaction would radiate, i.e. release, a charged particle in the form of an alpha particle, which is then to be manipulated, amplified, and read. The thermal neutron cross section is directly correlated to the probability of an interaction and is measured in Barns which is defined as 10^{-28} m^2, approximately the cross sectional area of the nucleus of uranium.

Table 1: Notable materials for charged absorption neutron detection with their interactions and properties

Isotope	Thermal Neutron Cross Section (Barns)	Reaction	Q-Value (MeV)	Reaction Products/ Respective Energies
^{3}He	5333	$^3\text{He} + {}^1\text{n} \rightarrow {}^3\text{H} + {}^1\text{p}$	0.764	^{3}H: 0.191 MeV ^{1}p: 0.573 MeV
^{10}B	3835	$^{10}\text{B} + {}^1\text{n} \rightarrow {}^7\text{Li}^* + {}^4\alpha$ (94%) $^{10}\text{B} + {}^1\text{n} \rightarrow {}^7\text{Li} + {}^4\alpha$ (6%)	2.31 2.792	^{7}Li*: 0.84 MeV $^4\alpha$: 1.47 MeV ^{7}Li: 1.015 MeV $^4\alpha$: 1.777 MeV
^{6}Li	940	$^6\text{Li} + {}^1\text{n} \rightarrow {}^3\text{H} + {}^4\alpha$	4.78	^{3}H: 2.73 MeV $^4\alpha$: 2.05 MeV

Source: The information in this table was collected from [10]

1.4.1 Current Neutron Detection Technologies

There are two dominant forms of neutron detection today in the form of proportional counters and scintillator-based neutron detectors. A brief review of the theory behind the mechanisms of these two instruments will be discussed along with their advantages and disadvantages.

1.4.1.1 ^{3}He Proportional Counter

Proportional counters are some of the first and arguably still the most common and popular methods of neutron detection. It produces an output proportional to the energy of incident radiation. This is accomplished by means of a cylindrical inert gas-filled ionization chamber in which a small radius wire (e.g. 0.03 mm gold-plated tungsten [7]) running through the center of the chamber is given a very high voltage, creating an electric field to detect ionizing radiation. The proportional counter also contains a mixture of a quench gas to terminate pulse discharges.

The incident radiation ionizes with the gas in the detector, creating pairs of electrons and positively charged ions in the gas. This is known as primary ionization. The electrons

5

will gravitate towards the anode, the wire, and the heavier positive gas ions will migrate to the cathode, the wall, at a slower pace. The electrons will be read as hits and the positive ions will be neutralized with external circuitry.

If the voltage is too low, the ions slowly move to the electrodes due to a lack of an electric field (i.e. force per ion) and frequently recombine neutralizing the effect. While some of the electrons from primary ionization will reach the anode, many will be lost due to recombination and thus the signal strength will be less than proportionate to the amount of incident radiation. This is a region that is often not used when trying to detect neutrons as it does not provide much valuable information.

$$E(r) = \frac{V}{r \ln\left(\frac{b}{a}\right)} \tag{1.1}$$

$$F = m\frac{dv}{dt} = qE \tag{1.2}$$

The strength of the electric field is described by Equation 1.1 in which b is the radius of the wall of the counter, a is the radius of the anode, V is the voltage applied to the anode, and r is the position of the electron. The force and consequently the velocity on the electron due to the electric field can be explained by Equation 1.2 in which m and q are the mass and charge of an electron which are 9.11×10^{-31} kg and 1.602×10^{-19} C respectively, and E is this electric field.This is reflected in Region I in Figure 1 which is sometimes referred to as the recombination region.

With a higher voltage, there is enough of an electric field where recombination unlikely to occur and the number of electrons that read the anode is directly proportional to the number of primary ionizations. This voltage range reflected in Region II from Figure 1, or the ionization region. However, this signal strength is rather small and can be difficult to detect.

Gaseous Ionization Detector Regions
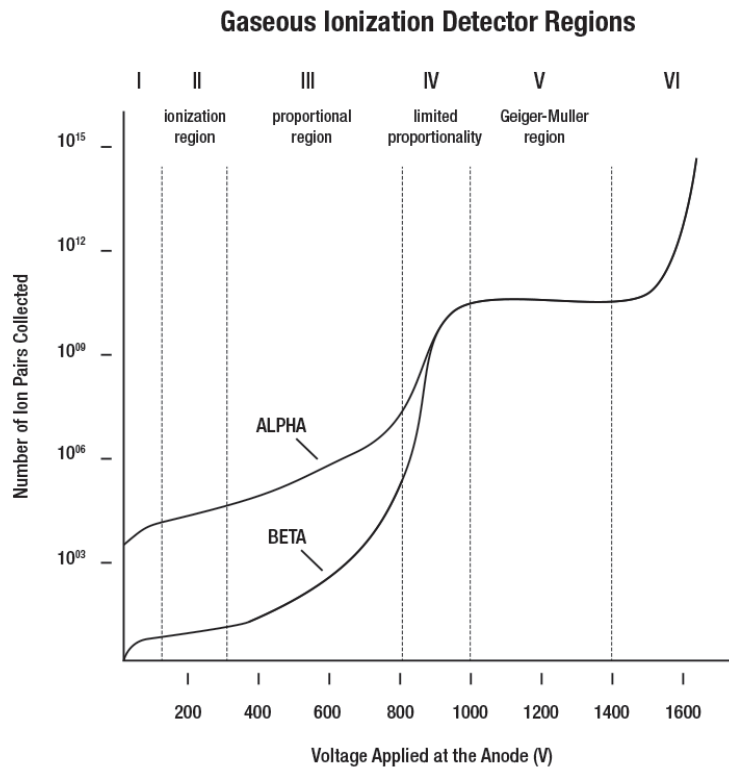
Figure 1: Practical detector regions and their respective voltage ranges.

Source: The graph was redrawn from data in [10].
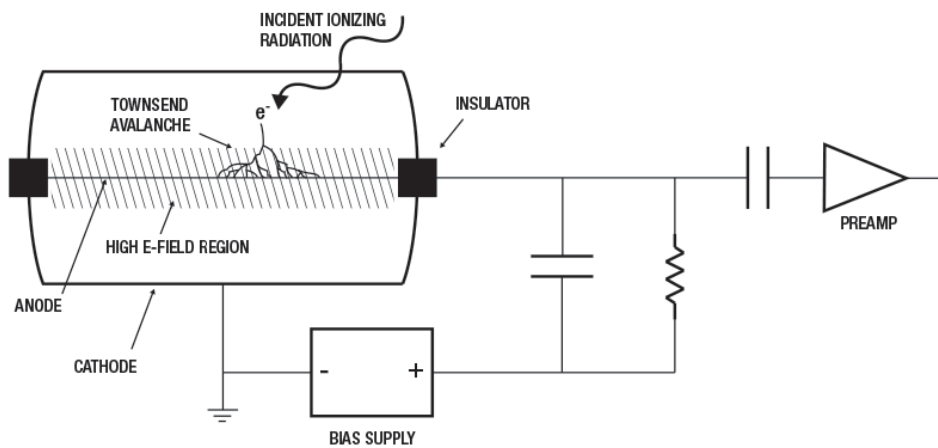
Figure 2: Proportional counter apparatus and depiction of operation.

A phenomenon occurs in Regions III-VI in which the electric field becomes sufficiently high that the electrons from primary ionizations gain enough kinetic energy that they form new electron-ion pairs which continue to multiply into what is known as the Townsend avalanche or gas amplification. This phenomenon is depicted in Figure 2.

Gas amplification begins in the voltage range of Region III seen in Figure 1. It occurs in a high electric field region near the anode which is consistent with small r values in Equation 1.1. In this region, the output is amplified but still directly proportional to the number of primary ionizations, hence the name proportional region.

Region IV is a voltage range in which the output signal is no longer directly proportional to the number of primary ionizations because the effect of gas amplification begins to overwhelm the anode as the electric field around the anode is too high. However, due to the loose correlation, this region is known as the limited proportional region. Region V, also known as the Geiger-Muller region, is an even more exaggerated range in which the number of secondary ionizations completely makes the number of primary ionizations insignificant, causing the user to lose all relevant information. Region VI represents the voltage levels that may damage the anode and should be avoided at all costs.

The gas used inside of the proportional counter is chosen for its thermal neutron cross section. From Table 1, it can be seen that ^{3}He has a very large thermal neutron cross section of 5333 barns, making it a very popular choice for its high intrinsic detection efficiency, i.e. the probability of detection if an incident strike of radiation passes through the detector [8]. Typical intrinsic efficiency rates are within 40%-60% but some have even recorded as high as 77% [5].

$$^3\text{He} + n \rightarrow {}^3\text{H} + {}^1\text{H} + 765 \text{ keV} \tag{1.3}$$

The reaction undergone in a ^{3}He tube is described in Equation 1.3. The 765 keV in the equation is the Q-value. The sign of this value reveals whether the reaction is exothermic or endothermic by being positive and negative respectively. In this reaction, the energy is

converted into kinetic energy and at such high energies, the reaction products are capable of removing electrons from other atoms creating electron hole pairs [8].

1.4.1.2   Scintillator-based Neutron Detection

Scintillators are another common method of neutron detection which emit photons, i.e. become fluorescent, when ionizing radiation passes through them. This floursecence is captured with a photomultiplier tube which amplifies the signal as demonstrated in Figure 3. Scintillators can be organic or inorganic and come in forms as crystals, liquid, or plastics. They also have a fast response and are not exorbitantly expensive, making them a popular solution to fast neutron detection, though they do suffer from poor gamma-ray radiation rejection which will be discussed later [7].

To go into further detail, when incident radiation causes the reaction products to deposit kinetic energy into the material, the electrons in the scintillator reach a excited states. As the electrons go through a deexcitation phase, they emit visible photons. The light then interacts with the photocathode in the photomultiplier tube which release electrons guided through an
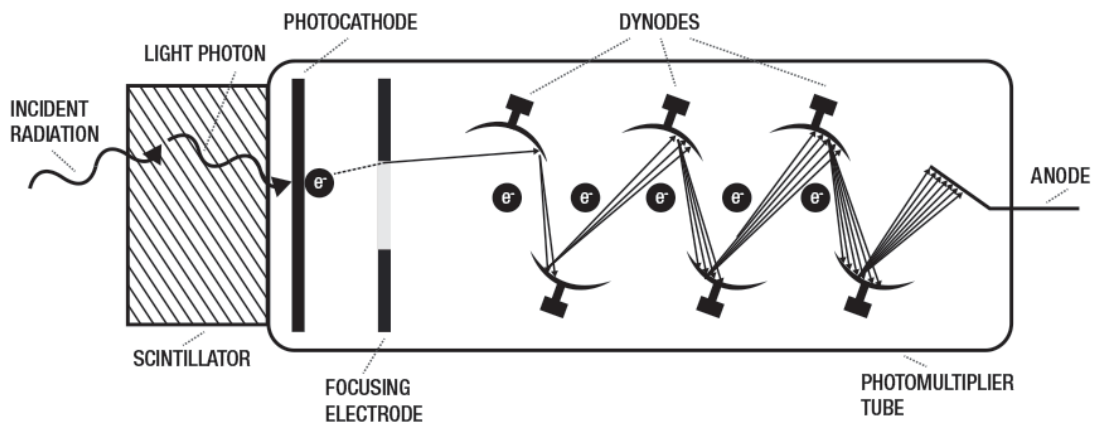
Figure 3: Demonstration of operation with a scintillator and photomultiplier used for neutron detection.

electric field by means of a focusing electrode to the first dynode. The dynodes are coated with materials such as BeO or MgO which emit secondary electrons with some reaching a multiplication factor of 10 [10]. This process is repeated through a chain of dynodes as seen in Figure 3 and can reach over 10^6 electrons at the anode for each electron that enters.

$$^{6}\text{Li} + n \rightarrow {}^{3}\text{H} + {}^{4}\text{He} + 4.78 \text{ MeV} \qquad (1.4)$$

One common scintillator material in neutron detection is ^{6}LiI which is typically enriched to 96% [11] and has a thermal neutron absorption cross section of 940 barns which can also be seen in Table 1 [10]. The key reaction taken place in the scintillator can be seen in Equation 1.4.

1.4.1.3 Advantages and Disadvantages of the State of the Art

Proportional counters are still the most accurate and efficient instruments for neutron detection. Not only can they provide a count of the number of neutron hits as the name might suggest, but by also having information about the energy of the particle, it can be applied for applications in spectroscopy. ^{3}He is particularly good at this as it not only converts neutrons but also acts as a proportional gas. Furthermore, proportional counters, when calibrated correctly, can have a very high gamma-ray rejection ratio which is important to prevent reading false positives of neutrons.

The primary disadvantage in ^{3}He proportional counters, is that ^{3}He is increasingly rare and thus very expensive. The natural abundance of ^{3}He is only about 0.000137%. The only practical method of obtaining ^{3}He is by extracting it from tritium as it decays with a half life of 12.3 years. Tritium was primarily obtained through the dismantlement of the nuclear stockpile during the post-Cold War era [8] and so since then, the production of ^{3}He has consequently reached a halt [6].

$$^{10}\text{B} + n \rightarrow {}^{7}\text{Li}^* + {}^{4}\text{He} - 2310 \text{ keV } (94\%) \tag{1.5}$$

$$^{7}\text{Li}^* \rightarrow {}^{7}\text{Li} + 480 \text{ keV} \tag{1.6}$$

$$^{10}\text{B} + n \rightarrow {}^{7}\text{Li} + {}^{4}\text{He} - 2792 \text{ keV } (6\%) \tag{1.7}$$
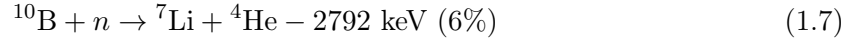
Substitutes for ^{3}He have been explored such as BF_3 filled proportional counters, i.e. ^{10}B, in which the reaction is described by occurs between ^{10}B and a neutron. Approximately 94% of the time, the reaction will leave ^{7}Li in an excited state which then decays as described by Equations 1.5 and 1.6. Approximately 4% of the time, the ^{7}Li is left in the ground state as described in Equation 1.7. While these Q-values and a thermal neutron cross section of 3835 barns are high enough to detect thermal neutrons, they are not as efficient as ^{3}He and thus need to be scaled up, making proportional counters even bulkier and less portable than they already were. Furthermore, ^{3}BF in gaseous form is rather toxic [6]. The toxicity is not the only danger proportional counters pose to the user as they require very high voltages to operate the instrument as well as constant maintenance.

Scintillators are an attractive alternative because they have a fast response time and are modestly inexpensive. However, the use of the photomultiplier tube, while amplifying the input signal a sizable amount, can bury the primary signal leading to poor energy resolution. When concerning neutron detection, the greatest drawback of scintillators are its poor efficiency at rejecting incident gamma-ray radiation.

1.4.2 Proposed Large Area Sensing Array

This research concerns an approach which utilizes a thin-film conversion layer in conjunction with a semiconductor-based charge detector for thermal neutron detection, Figure 4. A thin-layer of a high thermal neutron cross-section, e.g. ^{10}B or ^{6}Li, is applied on to a

reverse-biased PiN diode. An incident thermalized neutron that interacts with the conversion layer in a charged absorption reaction in which two charged particles traverse in opposite directions. One of the charged alpha particles can enter the reverse-biased diode to generate a string of electron-hole pairs between the two contacts, inducing a charge [12]. The induced charge, however, is often very small, e.g. 1 pC, and requires amplification for a readable signal which is accomplished with an in-pixel preamplifier.

Admittedly, with an intrinsic efficiency of about 5% [12], the efficiency of the thin-film conversion layer approach is considerably lower than other traditional methods. Different geometries have been explored to increase the intrinsic detection efficiency to 7.3% [13] as well as layering methods to increase the efficiency as high as 13.5% [12]. Even with improved efficiencies, the greatest benefit comes from the capability to cheaply produce large-area arrays by leveraging the manufacturing capabilities of the flat-panel display industry [14], [15]. By having a large area, the low intrinsic efficiency will be compensated by the high
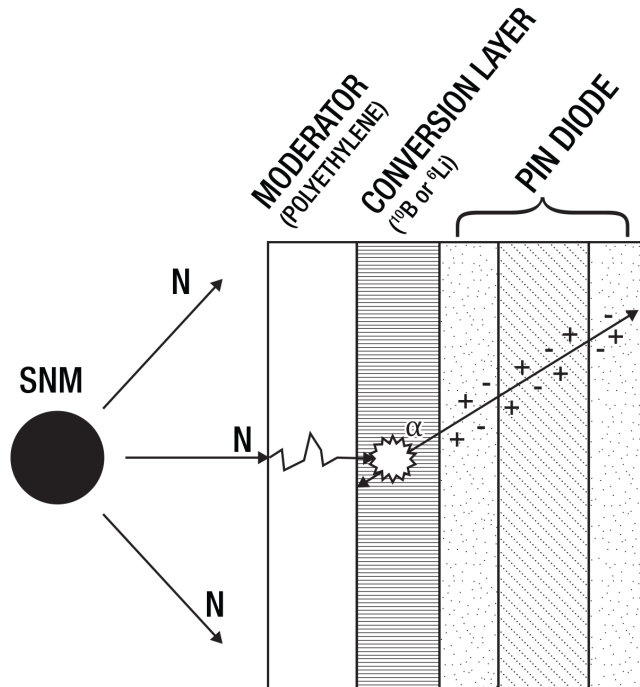
Figure 4: Thin-film conversion layer mechanism for neutron detection

collector efficiency, making probability of detection comparable to ^{3}He tubes. With the added benefits of having significantly lower maintenance costs, ease of use for safe operation, and portable form factor, such an approach has a promising outlook in further research.

1.5 Electric Field Imaging

The second part of the thesis concerns electric fields, another form of radiation. Electric field sensing has many advantages including its ability to penetrate non-conducting materials, its power efficient low information rate, low cost, compact size, and non-contact form factor [16], [17]. Most forms of electric field sensing rely on a transmit electrode at a given voltage and frequency to form an electric field with a receiver electrode [18]. Objects that have some level of conductivity, or permittivity different from the environment, would then perturb the electric field by adding to the capacitance between each of the electrodes. The change in current read at the receiver node can be unique to a variety of parameters including the dielectric constant, velocity, position, shape, size, etcetera of the target. Different parameter combinations could provide unique signatures for classification.

1.5.1 Current Electric Field Sensing Applications

Electric field sensing is prevalent in commercial and industrial applications such as in electric field proximity sensors which are used when detecting passengers in automobiles for proper airbag deployment, robotics, and home automation. Capacitive sensing is a similar derivative which also utilizes electric fields. Not only does proximity sensing with electric fields provide a cheap solution to novel and more intuitive user interfaces, but it also allows greater power savings as devices can rest in sleep mode until a human user presence is detected [19].

Weather analysis applications can also utilize electric field sensing. For example, atmospheric electric fields were observed to understand environmental conditions before

earthquakes, such as the infamous M6.8 earthquake in Taiwan 2002 [20], for preventative care. Thunderstorm prediction is another example in which the quasi-static electric fields generated above storm clouds are analyzed [21].

A large scale application of electric field sensing, and arguably the most mature, is with geophysical prospecting to find large deposits of oil and ore in the earth's crust [18], [22]. Prospectors place two driving electrodes into the ground at a very far distance to establish a voltage difference. Two closely placed sensing electrodes are read along the line of the two driving electrode to form a voltage gradient map based off of measurements of the earth's resistivity. Deviations from the uniform gradient is then an indicator of ore deposits. An alternative method applies a voltage on a probe which is lowered into an oil well in which the resulting current is measured.

Medical imaging techniques have been known to use electric fields such as electrical impedance technology (EIT) [18], [23] and non-contact EEG/ECG sensors [24]. In EIT, a ring of electrodes is wrapped around a body part in which a current is applied between pairs of electrodes to measure the resulting voltages. Using algorithms such as computed tomography, a cross-sectional image of the impedance map can be reconstructed. For EEG/ECGs, compact, non-contact electric field sensors integrated with amplification, bandpass, and analog-to-digital stages capacitively couple with the skin to produce clear EEG/ECG signals.

One fascinating phenomenon of electric field sensing can even be found in nature by species such as *Eigenmannia virescens* and *Mormyriformes*. These species are fish that use electric fields to sense their environment [18], [25] as a parallel to vision which proves to be critical in the dark and murky waters they reside in. The fish are capable of using their tail as a current source to induce a voltage which changes when an object of a dielectric constant different from water is introduced.

1.5.2 Electrostatic Theory

Maxwell's equations, seen in Equations 1.8- 1.12 below, cover the fundamentals of electricity of magnetism, giving a high-level mathematical understanding of relationships in a field. In the equations, $\mathbf{E}$ is the electric field, $\mathbf{B}$ is the magnetic field, $\mathbf{D}$ is is electric displacement, $\mathbf{H}$ is the magnetic field strength, ρ_f is the charge density, and $\mathbf{J}_f$ is the current density. In isotropic media, $\mathbf{D} = \epsilon\mathbf{E}$, $\mathbf{B} = \mu\mathbf{H}$, and $\mathbf{J}_f = \sigma\mathbf{E}$ where ϵ is the permittivity, μ is the permeability, and σ is the conductivity. These equations will frequently be referenced in the electrostatic derivations.

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{1.8}$$

$$\nabla \times \mathbf{H} = \mathbf{J}_f + \frac{\partial \mathbf{D}}{\partial t} \tag{1.9}$$

$$\nabla \cdot \mathbf{D} = \rho_f \tag{1.10}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{1.11}$$

$$\nabla \mathbf{J}_f = -\frac{\partial \rho_f}{\partial t} \tag{1.12}$$

Two new parameters in time-rate, α, and scaled time, $\tau = \alpha t$, are introduced. If the time dependent Maxwell's equations are rewritten with this scaled time parameter, the following equations are obtained.

$$\nabla \times \mathbf{E} = -\alpha\frac{\partial \mathbf{B}}{\partial \tau} \tag{1.13}$$

$$\nabla \times \mathbf{H} = \mathbf{J}_f + \alpha\frac{\partial \mathbf{D}}{\partial \tau} \tag{1.14}$$

$$\nabla \mathbf{J}_f = -\alpha\frac{\partial \rho_f}{\partial \tau} \tag{1.15}$$

This project concerns electric field sensing in or near the very low frequency (VLF) range and thus small α values are concerned. In the power series expansion of $\mathbf{E}$ in α, seen in Equation 1.16, the lower order terms sufficiently describe the low-frequency behavior [18]. With a low enough frequency, the zeroth and first terms are sufficient in which the solution is quasi-static [26].

$$\mathbf{E}(x, y, z, \tau, \alpha) = \alpha^i \sum_{i=0}^{\infty} \mathbf{E}_i(x, y, z, \tau) \tag{1.16}$$

$$\mathbf{E}_k(x, y, z, \tau) = \frac{1}{k!} \frac{\partial^k \mathbf{E}(x, y, z, \tau, \alpha)}{\partial \alpha^k} \tag{1.17}$$

Since the problem at hand is quasi-static, the zeroth and first order terms of Maxwell's equations will be derived. Substituting the expanded forms of $\mathbf{E}$ and $\mathbf{B}$ into Equation 1.8 yields Equation 1.18. This requires each term to equal 0 for all values of α. All fields couple only to lower order fields so any expansion can be evaluated once the initial zeroth order solution is determined. The remaining zeroth order electric field equations are derived similarly in Equations 1.19 - 1.22, the latter two regarding non-time dependent equations.

$$\nabla \times \mathbf{E}_0 + \sum_{i=0}^{\infty} \alpha^i (\nabla \times \mathbf{E}_i + \frac{\partial \mathbf{B}_{i-1}}{\partial \tau}) = \nabla \times \mathbf{E} = 0 \tag{1.18}$$

$$\nabla \times \mathbf{H}_0 = \mathbf{J}_{f0} \tag{1.19}$$

$$\nabla \cdot \mathbf{J}_{f0} = 0 \tag{1.20}$$

$$\nabla \cdot \epsilon \mathbf{E}_0 = \rho_{f0} \tag{1.21}$$

$$\nabla \cdot \mu \mathbf{H}_0 = 0 \tag{1.22}$$

The first order terms are realized in terms of t and $\alpha = 1$ since they correspond to realizable fields and can be seen in Equations 1.23 - 1.27. The first order term of $\mathbf{E}$ relates to the zeroth term of $\mathbf{B}$ and vice versa.

$$\nabla \times \mathbf{E}_1 = \mu \frac{\partial \mathbf{H}_0}{\partial t} \tag{1.23}$$

$$\nabla \times \mathbf{H}_1 = \epsilon \frac{\partial \mathbf{E}_0}{\partial t} + \mathbf{J}_{f1} \tag{1.24}$$

$$\nabla \cdot \mathbf{J}_{f1} = -\frac{\partial \rho_{f0}}{\partial t} \tag{1.25}$$

$$\nabla \cdot \epsilon \mathbf{E}_1 = \rho_{f1} \tag{1.26}$$

$$\nabla \cdot \mu \mathbf{H}_1 = 0 \tag{1.27}$$

It can be seen that because of Equation 1.24, a zeroth order electric field induces a first order magnetic field proportional to the time derivative of the electric field. Therefore, a zeroth order electric field implies a zeroth order charge and by Equation 1.25, the time derivative of said charge induces a first order current. The zeroth order electric field can be represented as a scalar potential and so the first order coupled is coupled to the time derivative of the zeroth order potential. This yields an explanation to the well known current to capacitance relationship seen in Equation 1.28. This relationship will be revisited shortly.

$$I = C \frac{dV}{dt} \tag{1.28}$$

A static zeroth order electric field satisfies Laplace's equation which is important because the first order fields are necessary to operate but do not provide new information from the zeroth order fields. In the circumstance of two conductors, i and j, the capacitance of one

17

due to the other is described by Equation 1.29 in which Q_i is the static charge on conductor i, S_i is the surface of i, and $\mathbf{n}$ is the normal of S_i.

$$\frac{Q_i}{V_j} = C_{ij} \tag{1.29}$$

$$Q_i = -\int_{S_i} \epsilon \mathbf{n} \cdot \nabla \phi_0 da = \sum_j C_{ij} V_j \tag{1.30}$$

$$I_i = \frac{dQ_i}{dt} = \frac{d}{dt} \sum_j C_{ij} V_j = \sum_j C_{ij} \frac{dV_j}{dt} \tag{1.31}$$

If more than two conductors are involved, by linearity, the total charge on i induced by other conductors is the sum of their individual induced capacitances, Equation 1.30. This also means that first order currents are related to zeroth order charge and thus current entering a receiver, I_i, is determined by the time derivative of i, Equation 1.31. Therefore, currents are first order phenomena but are only used to measure capacitance while the zeroth order property is geometry dependent [18].

1.5.3 Types of Electric Field Sensors

Before delving into electric field imaging, it is important to cover a basic understanding of electric field sensing as the performance of the imager will be directly correlated to the performance of each sensor. Since this research is primarily concerned with passive forms of electric field sensing, those methods will be covered in more depth.

Passive methods of electric field sensing include potential sensors, vector electric field sensors, and electric charge induction sensors which also known as D-dot sensors [27], [28]. These sensors respectively operate by measuring the voltage at specific points in space, the voltage difference between various points in space to form a 3-D field, and the time derivative

of the electric field. Passive methods of electric field sensing have been capable of detecting bullets [27], [29] and even classifying helicopters at extremely low frequencies [30].

1.5.4   Previous Work in Electric Field Imaging versus Proposed Electric Field Imager

In industrial applications, the aforementioned EIT method and geophysical prospecting are the most common form of imaging with electric fields. There is a body of research in academia in electric field imaging [18], [25], [31]–[33] that focus on active interrogation in which electric fields are a driving force in developing perception such as for machine vision. These methods of sensing use an active interrogation approach. Passive methods of electric field sensing include potential sensors, vector electric field sensors, and electric charge induction sensors which also known as D-dot sensors [27], [28].

Rather than using electric fields to image objects as a means of machine vision, this research introduces a passive design that directly images the electric fields themselves at very low frequency and consequently the sources of charge. This is accomplished through an array of D-dot sensors with corresponding lock-in circuitry on both a rigid printed circuit board (PCB) and flexbile polyethylene naphthalate substrate, the latter using an InGaZnO TFT process. These will be discussed in further detail in later chapters.

Such an imager has promising applications including discrete and noninvasive security inspection [34], safely imaging power lines through walls at construction sites, and mapping the electronic state of circuits for electromagnetic interference (EMI) which is a very common but expensive issue in industrial circuit design [35]. Having a flexible array will also introduce the possibility of new portable and versatile form factors [36].

1.6   FEDC TFT Process

The TFTs fabricated at FEDC use either Amorphous Silicon (a-Si) or Indium Gallium Zinc Oxide (InGaZnO) in an 8 mask, low temperature (180°C) process. They have an

inverted staggered tri-layer structure as seen in Figure 5 and can be processed on flexible substrates such as metal foil and polyethylene napthalate (PEN). These devices have been used to build flexible displays and a variety of other flexible electronics including bio-sensors and X-Rays. These devices were of interest in the pursuit to build flexible large-area arrays. While previous work used a-Si, all new designs are based off of the InGaZnO process. Further details of the TFT process and characteristics can be found in [37]–[39].
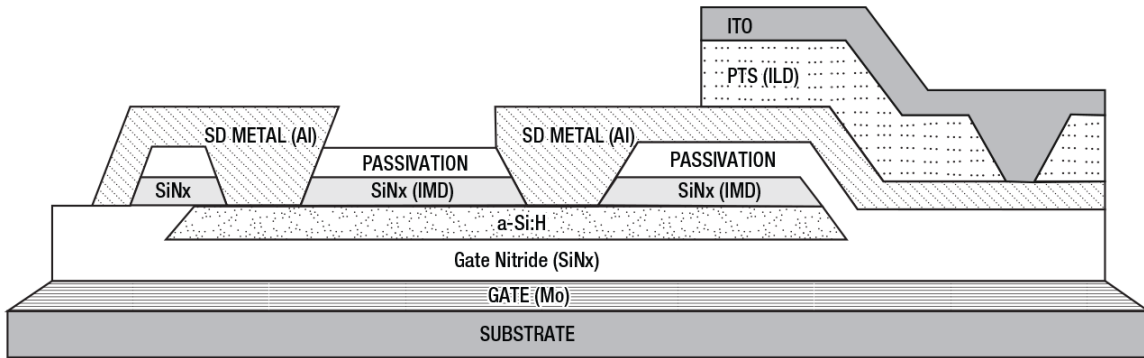
Figure 5: Basic cross-section view of the structure of the thin-film transistor process from FEDC.

Figure 6: Photographs of a wafer of flexible electronics (left) and a flexible display (right) built at FEDC.

PART I: NEUTRON DETECTION

Chapter 2

ACTIVE PIXEL SENSORS

This chapter discusses the motivation and provides an introductory design to TFT-based active pixel sensors (APSs). An APS is used to amplify charge to a readable level generated at a diode output induced by a radioactive reaction. This method will also be compared to more traditional CMOS amplification circuitry. First, a brief overview of the PiN diodes used will also be provided.

2.1   Detector Overview

The end-goal of this research is to develop large-area, thin-film neutron detectors. This is accomplished by applying a layer of a high thermal neutron cross-section material (e.g. ^{10}B) on top of a thin-film CdTe/CdS PiN diode. Upon incident radiation, the conversion layer will produce an alpha particle that will be detected through the reverse-biased PiN diode. To minimize noise, the small change in charge from the diode is fed directly into an in-pixel amplifier to produce readable outputs.

2.2   PiN Diode

A PiN diode, as opposed to a PN diode, has a wide undoped intrinsic region between the p-type and n-type doped regions. This is key as it provides a larger depletion region yielding a greater probability of an incident alpha particle to lose energy through scattering and ionize to create electron-hole pairs. In a reverse-biased configuration, the diode does not conduct aside for a small dark current, a.k.a leakage current. However, the reverse-biased
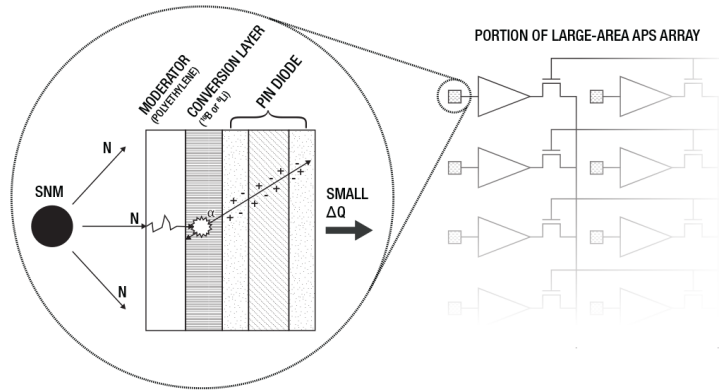
Figure 7: Photographs of a wafer of flexible electronics (left) and a flexible display (right) built at FEDC.

field sweeps electron-hole pair carriers out of the intrinsic region to their respective electrodes creating a detectable charge.

2.2.1 Si Diode

The OPF480, a commercial silicon PiN photodiode, was used as a reference diode in many of the experiments. With a high response rate (0.55 A/W) a low capacitance (1.5 pF) and low dark current level (0.1 nA), the diode exemplified many high performance qualities desired in the in-pixel diode. While we were not expected to reach these performance levels,

it was a good measure in ensuring that remaining circuitry was capable of detecting alpha particles.

$$\Delta Q = \frac{1.6 \times 10^{19} C \cdot 5.307 MeV}{3.6 eV} = 2.359 \times 10^{-13} C \tag{2.1}$$

$$\Delta V = \frac{\Delta Q}{C_{pix}} = \frac{2.539 \times 10^{-13} C}{1.5 pF} = 0.157 V \tag{2.2}$$

Many results using the OPF480 will be provided throughout this thesis. As a frame of reference, typical values for change in output are provided in Equations 2.1 and 2.2. In the calculations, it is assumed that the capacitance of the pixel is primarily from the capacitance of the diode at around 1.5 pF and that all of the energy from the incident alpha particle is 5.307 MeV, which is the maximum expected from a ^{210}Po source, is dissipated.

2.2.2 a-Si:H Diode

The Flexible Electronics and Display Center (FEDC) at Arizona State University (ASU) has already produced hydrogenated amorphous silicon (a-Si:H) diodes for flexible X-ray imaging using TFT technology [40]. It was only logical to explore the possibility that the diodes could detect high energy charged particles for a seemless integration process.

Unfortunately, after extensive measurements on numerous diode thicknesses, e.g. 1.2 μm, 2.4 μm, 4.8 μm, 7.2 μm, no alpha particles were detected. It was concluded that the charge collection efficiency was too low which was supported by previous research that suggested the charge collection efficiency would be less than 2% [41], [42]. Alternative solutions were thus sought.

2.2.3 CdTe/CdS Diodes

Our partnering institution, University of Texas, Dallas (UTDallas), have developed an alternative thin film diode using Cadmium Telluride (CdTe) [43] and Cadmium Sulfide (CdS) [44]. The charge collection efficiency of these devices have been reported to be upwards of 80%, a significant improvement from the performance of the a-Si:H diodes and have also detected alpha particles and neutrons when a ^{10}B converter was applied with conventional amplification techniques. The goal was to integrate custom TFT-based amplification designs with these diodes as a proof of concept. Examples of I-V characteristic curves as well as an image of a CdTe diode sample can be seen in Figure 8.

2.3 An Introduction to Preamplifiers

Typically, when dealing with an array of sensors, the method in which to read the sensor values borrows greatly from the principles of dynamic random access memory (DRAM). In such a structure, each sensing unit, signified as a pixel, has associated access circuitry,

(a) (b) (c)
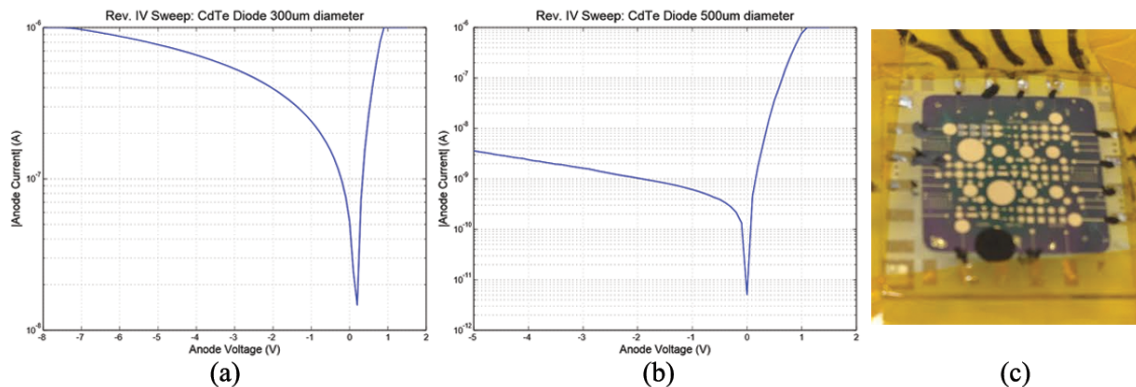
Figure 8: IV characteristic curves for 3 μm thick CdTe diodes for diameters of (a) 300 μm and (b) 500 μm. (c) A sample of CdTe diodes on a chip.

Source: The CdTe diode samples were provided by colleagues at UTDallas and remeasured at ASU.

often by means of a transistor connected the output of the sensing unit, a row line, and a column line. These signals are then amplified and read through external circuitry. Since the amplification is done externally outside of the pixel, these sensor heads are regarded as passive pixel sensors (PPS).

However, when dealing with very small amounts of charge such as the output produced by the diode, reliable readout is only possible with extremely low-noise and highly sensitive external circuitry. Even then, valuable information may be lost along the read lines and access transistors before the signal is even capable of reaching the external amplification stages. To overcome these shortcomings of the PPS, APS circuitry was developed so that the active in-pixel amplification stage could reduce noise while producing readable outputs for each sensing unit.

The APS designs incorporate TFTs which is important in allowing the PiN diodes to be compactly arrayed in a large sheet-like detector. Additionally, with the display industry optimizing the process to cheaply make large area arrays, using TFTs allows for the possibility to leverage said process. Finally, utilizing TFTs opens the possibility of fabricating flexible arrays for new form factors and applications. The greatest drawback is that only NMOS transistors are available. More detailed discussions of this limitation and how it is overcome are provided in the following sections.

2.4   CMOS Charge Sensitive Preamplifier

Typically, a charge sensitive premaplifier is used when detecting small currents through a diode. This accomplished with an operational amplifier of very high intrinsic gain, e.g. 1,000-100,000 V/V, with a negative feedback loop. Such high gains are possible with CMOS circuitry. The large gain provides a virtual ground at the input forcing nearly all of the charge to be stored on a small feedback capacitor, typically around 0.1-1 pF. A simplified preamplifier setup is seen in Figure 9.

In the simplified mechanism, expected output voltages are calculated for both a commercial
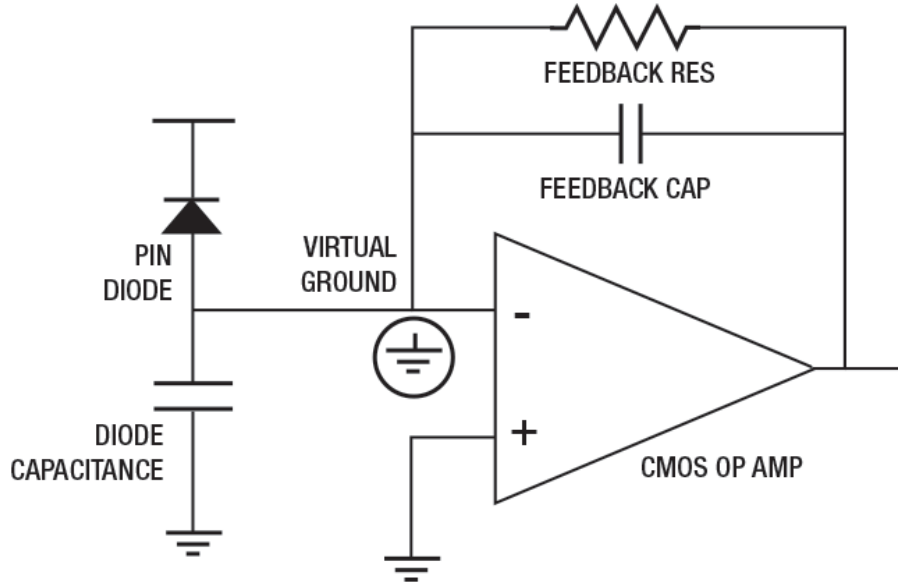
Figure 9: Simplified setup of CMOS preamplifier for charge detection including a model for the intrinsic diode capacitance.

OPF480 Si PiN photodiode and a CdTe diode fabricated at UTDallas, Equations 2.3 and 2.4. With the commercial diode, it is reasonable to expect around 10^6 electrons at the output and around a third of that for the CdTe diode due to its lower mean free path. With output voltages of around 1.6 V and 0.53 V, the output signal is large enough to be readily detected. Such values are fairly consistent with the performance of commercial charge sensitive amplifiers such as the ORTEC Model 142C preamplifier.

$$(\text{OPF480 Si Diode with ORTEC}) \quad \frac{10^6 1.6 \times 10^{-19} C}{0.1 pF} = 1.6V \tag{2.3}$$

$$(\text{CdTe Diode with ORTEC}) \quad \frac{\frac{1}{3} 10^6 1.6 \times 10^{-19} C}{0.1 pF} = 0.53V \tag{2.4}$$

The diode has a non-trivial amount of intrinsic capacitance that should be taken into consideration, especially at high frequency operation. While high frequency operation

is not a significant concern in our immediate application, a large diode capacitance can dramatically hurt the strength of the input signal since the voltage accross a capacitor is inversely proportional to the capacitance. By having a virtual ground, the voltage at the input is very close to zero. This causes almost no voltage drop across the intrinsic diode capacitance which forces all of the current to go through the feedback system. This is not as easily achieved in an NMOS only system and will be discussed further.
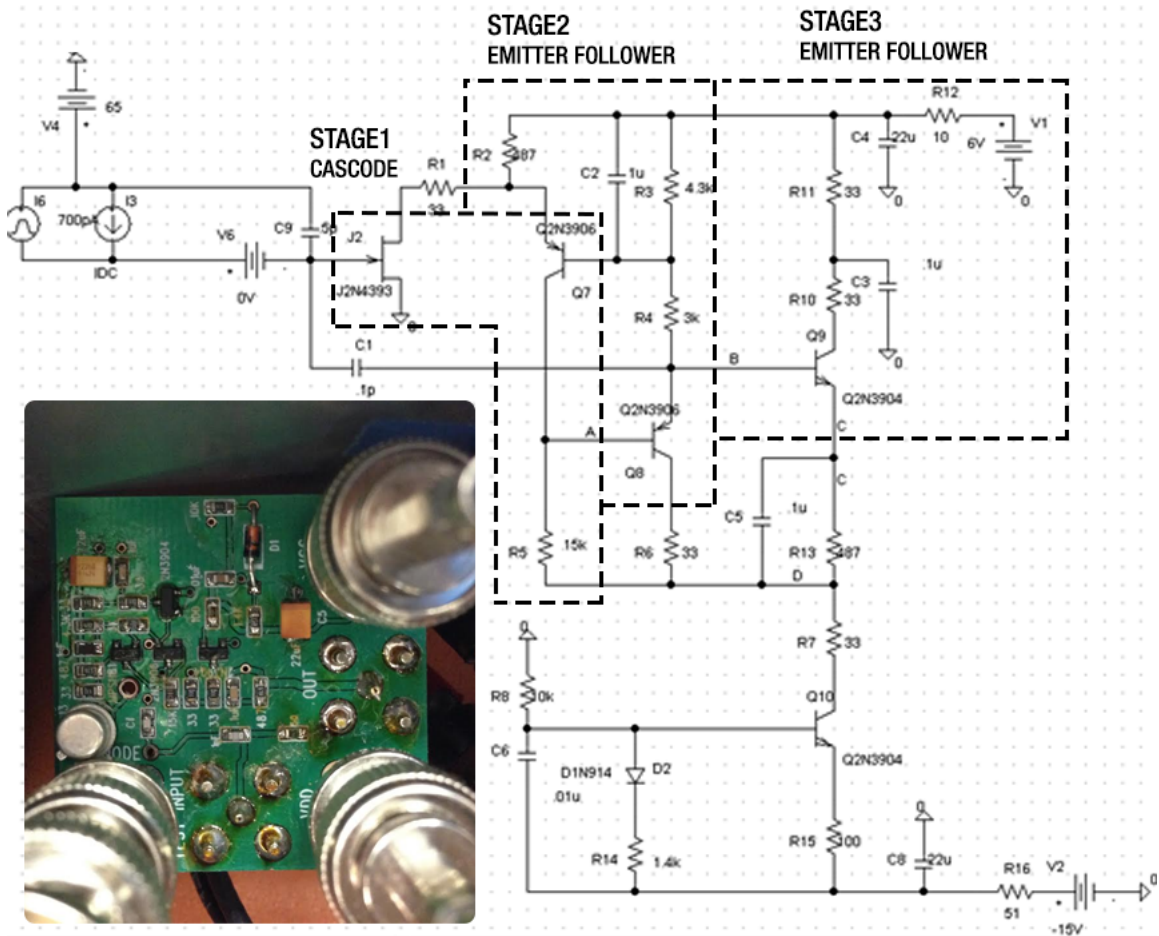
Figure 10: Schematic of charge sensitive CMOS preamplifier used in an alpha particle detector. An image of the final fabricated PCB is also provided (bottom-left). The amplifier was assembled using commercial off the shelf components.

Source: The amplifier design is based off of previous work done by Bertuccio [45], Ramirez [46], et al. The board was designed and assembled by my colleague, George R. Kunnen.

2.4.1 Reference CMOS Amplifier

Similar to how the OPF480 served as a best-case diode for a reference, a CMOS charge sensitive preamplifier served as a reference best-case preamplifier. The design was based off previous research which used it in an X-ray detector [45], [46].

A custom built design based of this work can be seen in Figure 10 in which the three main stages are highlighted by the dotted lines. The amplifier was assembled with commercial off the shelf components soldered onto the PCB. It was capable of producing outputs 1-1.2 V due to incident alpha particles from a ^{210}Po source. These results will be discussed in further detail in the following chapter.

2.5 NMOS-only TFT Preamplifiers

Ideally, a high gain CMOS operational amplifier would be available at each pixel to follow in suit with traditional preamplification methods. However, with our process not supporting PMOS transistors, novel methods were researched to overcome these obstacles.

2.5.1 Why no CMOS

CMOS TFTs have been a topic of interest at FEDC where they have even built the world's first CMOS TFT operational amplifier [47]. However, not only did it require an arduous process of fabricating the NMOS circuitry at FEDC, shipping the devices to UTDallas, fabricating the PMOS circuitry at UTDallas, shipping it back to FEDC for testing, it yielded modest gain and experienced severe lifetime issues, proving to be impractical for our application.

Higher performing CMOS TFTs have recently been developed with successful TFT-based CMOS inverters having been fabricated [48]. However, with the process in its infancy and the lack of large-scale industry support, unlike the support seen for NMOS-only TFT

circuitry by the flat panel display industry, such technology is not readily accessible. It is not unreasonable to believe that a stable process could be available if future commercial applications demand it such as wearable and transparent electronics.

2.5.2 Basic NMOS amplifier

The baseline PPS and APS architectures can be seen in Figure 11. In the PPS structure, an access transistor is all that is necessary at each pixel. The access transistor behaves as a switch that when "closed," allows the signal to travel through the column line. This provides a rather elegant and compact solution for high-resolution imaging. However, as aforementioned, the already small signal may be lost in noise and so highly sensitive, low-noise external amplification is necessary. The amplification circuitry themselves can also add additional unwanted noise and decrease the probability of detection.

The basic APS structure utilizes a source follower stage as was first presented by Karim et. al [49]. This design converts the small change in voltage detected by the diode and
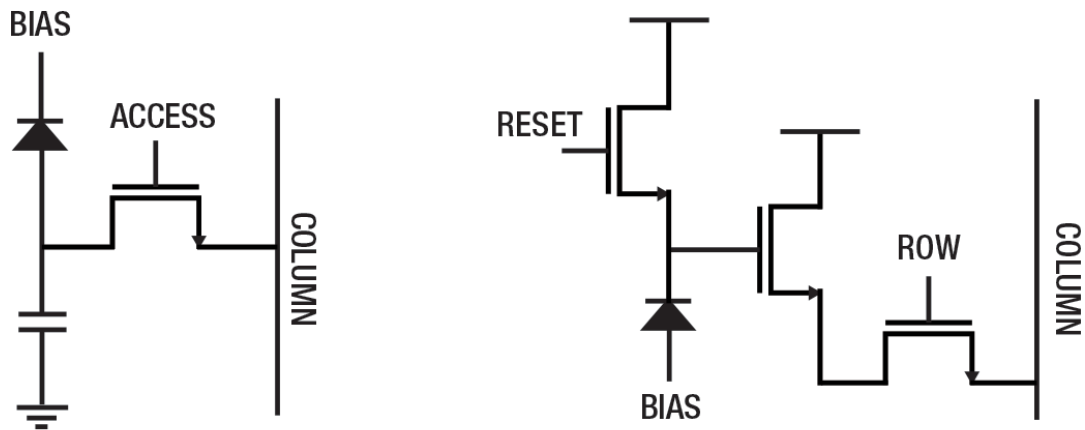
Figure 11: Schematic of PPS structure (left) and basic APS structure (right).

Source: The PPS architecture was presented by McGregor et al. [12] and the APS architecture was presented by Karim et al. [49].

30

converts it to a change in current at the output. A reset transistor is also present so that the input can return to its operating point after an ionizing event. This method provided high small-signal linearity and a great reduction in intrinsic noise. It was found, however, that this design did not provide enough gain for our application and the measures taken to improve the design will be discussed in the following chapter.

2.5.3 Obstacles of NMOS-only

Figure 12 provides a simplified view of how the diode signal can be configured with CMOS and NMOS common source configurations. From Equations 2.5 and 2.6, it is clear to see that obtaining gains high enough to produce a virtual ground in an operational amplifier would be difficult to achieve with only NMOS transistors. While NMOS-only operational amplifiers have been made [50] even with TFT technology [51], those designs were more concerned with digital-to-analog conversion, required a large number of transistors, and provided modest gain.
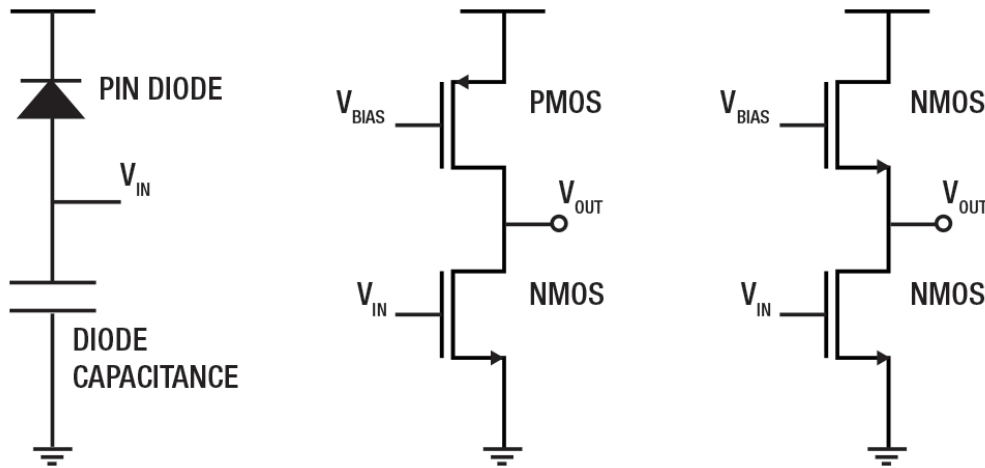
Figure 12: Schematic of the diode and its parasitic capacitance providing the input signal (left) which can be connected to an active load CMOS configuration (middle) or an NMOS configuration (right).

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{g_{mNMOS}}{g_{oNMOS} + g_{oPMOS}} \approx 20 - 100V/V \tag{2.5}$$

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{g_{mNMOS}}{g_{mNMOS}} \approx 2 - 4V/V \tag{2.6}$$

Another challenge encountered from having an NMOS TFT limitation was from the parasitic capacitance of the diode. Since there is no virtual ground, after an incident ionization event, the collected charge appears across the large diode capacitance resulting in a small signal as opposed to appearing across the small feedback capacitor resulting in a large signal. This is only exacerbated by the large input impedance.

Equations 2.7 and 2.8 provide estimated calculations of what would be expected at the input for the basic NMOS-only configuration seen in 12. Unlike the calculations made for the CMOS amplifier where the majority of the charge was collected on the feedback capacitor, the diode capacitance will dominate in this configuration.

$$\text{(OPF480 Si Diode with TFT Amp)} \quad \frac{10^6 1.6 \times 10^{-19}C}{1.5pF} = 106.7mV \tag{2.7}$$

$$\text{(CdTe Diode with TFT Amp)} \quad \frac{\frac{1}{3}10^6 1.6 \times 10^{-19}C}{18pF} = 2.9mV \tag{2.8}$$

Since voltage is inversely proportional to the capacitance, a large capacitance will reduce the input voltage. It can be seen that the signal strength is considerably lower compared to the CMOS amplifier and furthermore, if the parasitic capacitance is not carefully controlled, which can be expected from the CdTe diodes, then the signal, e.g. 1-3 mV, is too small for detection. Normally a minimum of a 10 mV input signal strength is a reasonable expected threshold for detection.

Chapter 3

EVOLUTION OF THE IN-PIXEL PREAMPLIFIER

This chapter will cover previous and current work done on improving APS preamplifier designs. Simulation and experimental results will be provided. Initially, the main obstacle was to overcome the low gain of NMOS-only TFTs to amplify the already small, noise-vulnerable diode output.

3.1 The Dual Stage Amplifier

The initial APS preamplifier design that started this research was designed by my colleagues, Edward H. Lee and George R. Kunnen, in which they presented a dual stage architecture [52], [53], Figure 13. The new design allowed one stage to minimize flicker noise while the other was optimized for high transconductance gain, resulting in a 55% reduction in input-referred noise and a transconductance gain to be around 3 A/V [52]. The design also utilized reset auto-zeroing to stabilize the circuit after an ionizing event.

When a high energy alpha particle interacted with the reverse-biased PiN diode, a small change in charge would be generated at the cathode. The change in charge is seen as a change in voltage at the first stage of the amplifier which is in a basic common source amplification configuration. This will correspond to a change in current at the column which can then be more reliably detected through simple external readout circuitry including a transimpedance amplifier to convert the current to a readable voltage output.

Two sets of amplifiers were fabricated using both FEDC's a-Si:H and InGaZnO TFT processes. To prove feasibility of utilizing this amplifier in a large-area application, a series of experiments were conducted to see if alpha strikes were detectable from a ^{210}Po source.
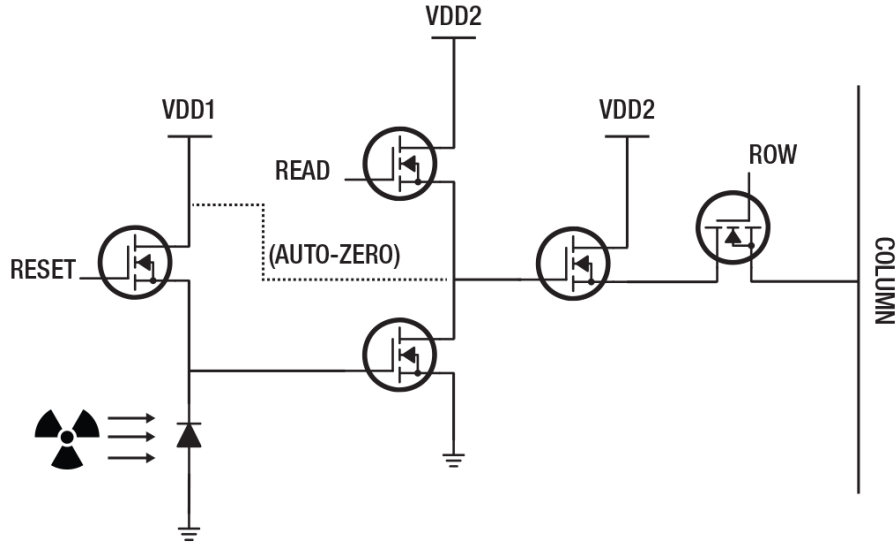
Figure 13: Schematic of the original dual stage APS preamplifier with auto-zero reset for alpha particle detection.

Source: This architecture was designed and first presented by Lee, Kunnen, et al. [52].

The various preamplifier and diode combinations tested can be found in Table 2 along with their results.

In the experimental setups, the environment was carefully controlled with extensive shielding by encasing all critical components in grounded metal boxes to reduce external noise. Furthermore, all of the voltage supplies were battery powered to reduce noise that could arise from DC voltage sources. An on-chip waveform generator (LM55 IC) was used to operate the reset transistor and a low-noise transimpedance amplifier (DLPCA-200) was used to convert the current output to a readable voltage on the oscilloscope.

Table 2 shows that alpha strikes were successfully detected using the OPF480 diode with both the CMOS charge sensitive preamplifier described in the previous chapter and the dual stage amplifier. Taking a closer look at the more pertinent latter result, a comparison can be made with theoretical and measured output strengths. With the estimated calculations made in Equations 2.1 and 2.2 of the previous chapter, and the reported transconductance gain of 3 μA/V, one could expect an output current of 471 nA, albeit in a best case scenario.

Table 2: Summary of alpha response experiments from a ^{210}Po source with the original dual stage APS amplifier design

Experimental Configuration	Observable Alpha Response
a-Si:H/InGaZnO APS with OPF480	YES
InGaZnO APS with a-Si:H diode	NO
Charge Sensitive Preamp with OPF480	YES
Charge Sensitive Preamp with a-Si:H diode	NO

Source: The information in this table was collected from [53].
Note: Both 1.2 μm and 2.4 μm a-Si:H diodes were used in all related experiments as well as a ^{210}Po alpha source.

When looking at the oscilloscope screen capture in Figure 14, the two observable alpha strikes can be seen by the dips in the output. After taking into account the gain from the transimpedance amplifier, these measurements correspond to a 20 nA change on the column line which is far below the estimated calculation.
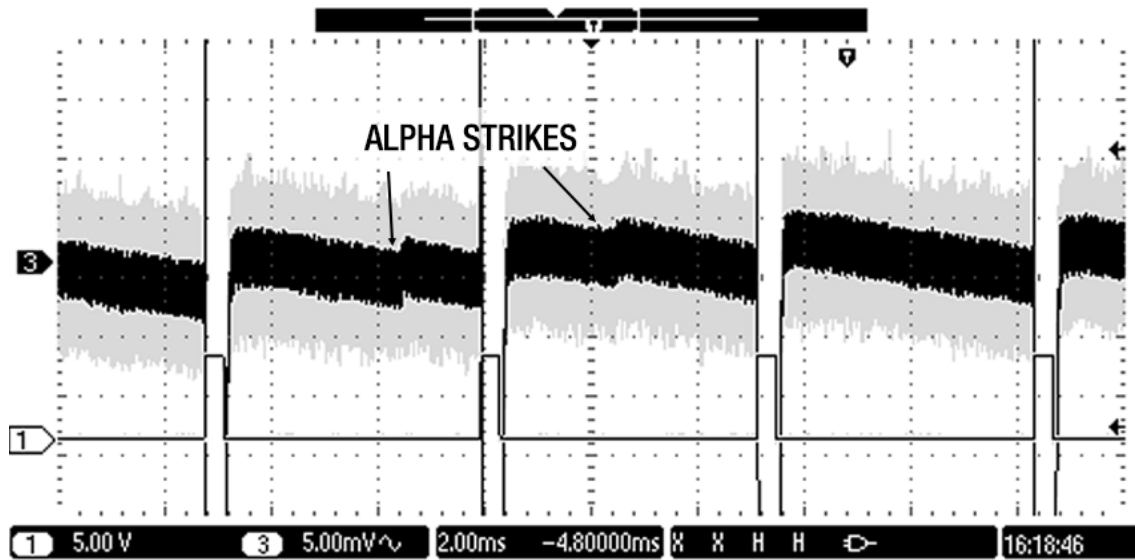
Figure 14: Oscilloscope screen capture of two alpha strikes observed with the a-Si:H dual stage APS preamplifier.

Source: This image was captured by Lee, Kunnen, et al. [52].

Despite the fact that the dissipation of energy from the alpha particle were best case scenarios, e.g. particles can lose energy as they are slowed down by air before striking the diode, the observed signals were far below expected values. The small output signal can be attributed to a variety of possibilities.

One possibility is from the aforementioned parasitic capacitance issue. It was seen how the parasitic capacitance at the input, whether it is from the diode or other source, can reduce the input signal and higher than anticipated capacitance at the input may have been present.

The capacitance from the diode can be reduced through a variety of measures, the most naive method being the decrease the surface area of the diode. However, if the diode area is too small, then the probability of catching an incident alpha particle reduces as well. Therefore, special design considerations were necessary to optimize this trade-off, particularly when building the custom CdTe/CdS diodes at UTDallas.

Most importantly, process variations can lead to shifts in threshold voltages in the transistors. This is more prevalent in this TFT a-Si:H and InGaZnO process which is not nearly as mature or stable as traditional single-crystal Si processes. These shifts can effect the biasing point of the common source stage and thus effect the transconductance gain.

3.2   Multi-Stage APS Preamplifiers

Despite having observable alpha responses with the dual stage amplifier, the output was only just detectable after extensive measures to minimize noise within the system. This made it clear that a higher gain amplifier was necessary for any practical real-world application.

3.2.1   First Generation

In order to increase gain, multiple common source stages (between two to five) were cascaded in an open-loop configuration. This design was done together with my colleague,

George R. Kunnen, and presented in [14]. With each stage producing roughly 1.5-3 V/V gain, the gain would theoretically grow geometrically with the gain level and number of stages. Therefore, despite each stage having relatively low gain, optimal conditions in a five-stage configuration could yield approximately 3^5 or 243 V/V of total gain at the output. Of course, other factors must be taken into consideration such as overwhelming gain that can pull the transistors out of saturation and area consumption preventing a very high number of stages. It should be noted that during this time, a-Si:H and InGaZnO processes were still used to fabricate the N-channel TFTs in our amplifiers, but there was a general shift to focus on InGaZnO for its higher mobility and greater electrical stability.

The full schematic for a three-stage preamplifier can be seen in Figure 15. A range from two to five stages were fabricated. With each stage being identical, it is easy to extrapolate what higher stage configurations would look like. Looking at the schematic, it can be seen that within each stage there are two sub-stages, the first is a self-biasing sub-stage and the
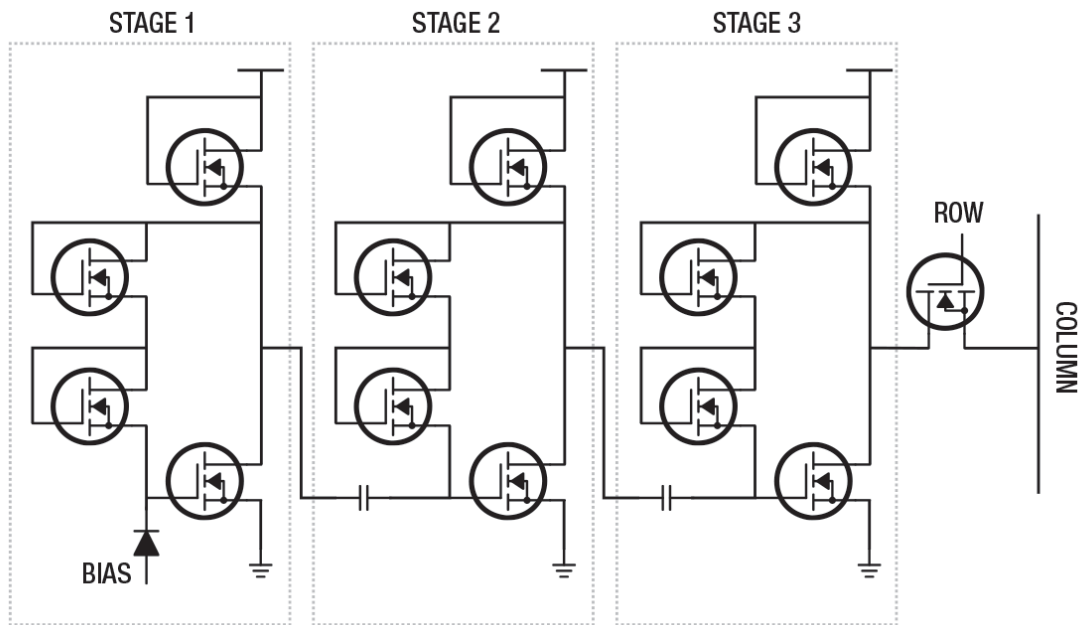
Figure 15: Schematic of a three-stage APS preamplifier from generation 1.

Source: This design was first presented in [14].

second is the amplification common source sub-stage. The self-biasing eliminates the need for an external waveform generator but rather the sensitive node will automatically reset to the high-gain DC operating point after an ionizing event.

This is accomplished by the two diode-connected transistors. Each stage is connected to one another via an AC coupling capacitor. The capacitor will essentially "block" DC from the previous stages allowing each stage to operate at the appropriate biasing point. However, the AC signal of interest will pass through the capacitor and reach the sensitive node of that stage to be amplified.

The four-stage amplifier yielded the greatest experimental results. Gains were reported at around 20 V/V which was measured by comparing the output of the amplifier with a known pulse. Figure 17 demonstrates an example characterization test with a four-stage amplifier. It also demonstrates how the amplifier was capable of resetting itself to the proper biasing point without the need of an external waveform generator. Furthermore, when connected to the commercial OPF480 diode and subjected to the ^{210}Po source, alpha strikes can clearly be detected, Figure 16.

When comparing the results of the multi-stage amplifier, Figure 16 with the dual stage a-Si:H amplifier, Figure 14, it is clear that there is a dramatic improvement in performance. Both setups used the same OPF480 diode and ^{210}Po source yet the multi-stage design yielded a much higher gain, with an intrinsic high-gain self biasing attribute, while not needing to undergo considerable efforts to shield the detector system, e.g. metal boxes were not necessary and standard voltage sources could be used as opposed to batteries.

The sample output is that of a four-stage amplifier but theoretically higher gain five-stage amplifiers were also available. The downside of having so many stages will be covered in further detail when discussing the latest generation of multi-stage amplifiers.
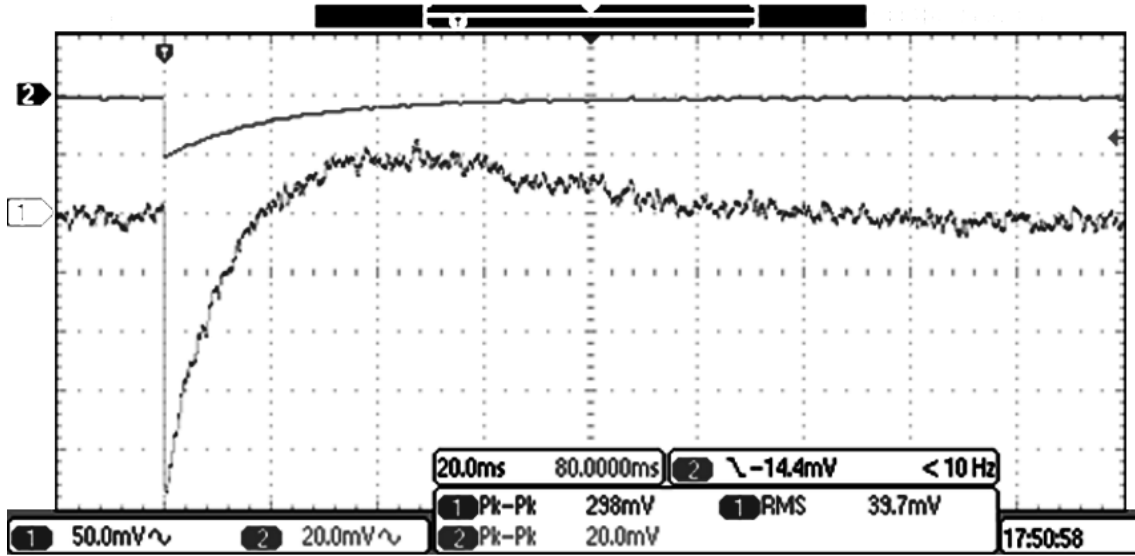
Figure 16: Test of 4-stage APS with known input signal (2) to characterize the gain at the output (1).
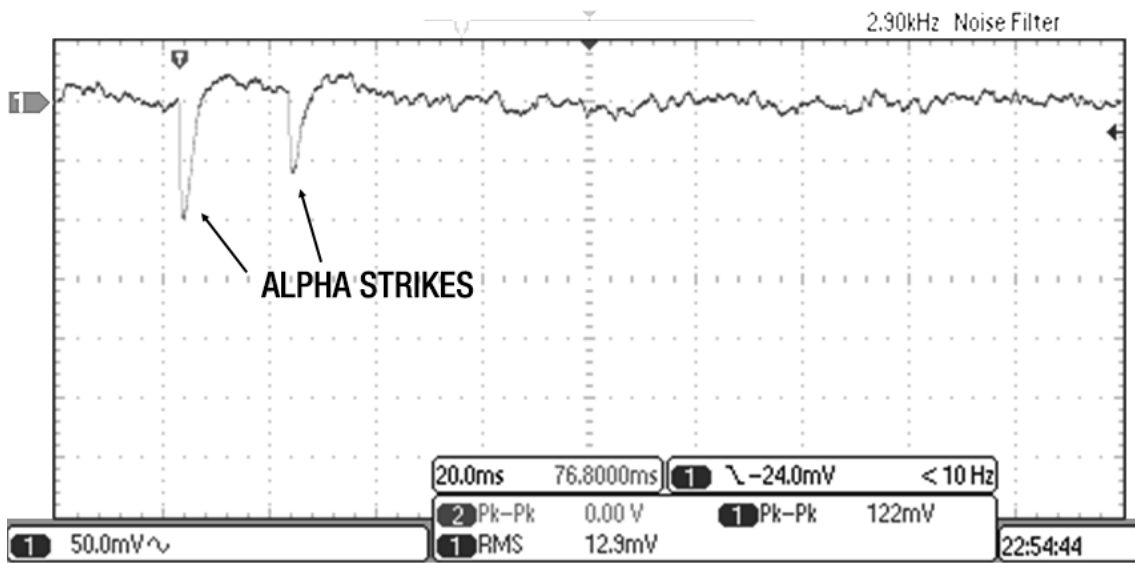
Figure 17: Two alpha responses seen at the output of a first generation four-stage APS with OPF480 diode and ^{210}Po source.

3.2.2 Second Generation: Independent Bias Control

Further design modifications were made on the multi-stage configuration to obtain even higher gain values, establishing the second generation[1]. The key feature was the addition of an independent bias control. With process variations, the threshold voltages can shift by nontrivial amounts.

Since the high-gain DC operating point heavily relies on the threshold voltages of the transistors, the optimal gain may not be achieved in certain devices. By implementing a biasing port to connect to an external voltage source, one could have better control to fine tune the operating point for optimal gain from device to device. The schematic for the second generation amplifier can be seen in Figure 18.

Ideally each stage would have its own biasing terminal, but this approach would not be scalable as it requires a large number of voltage supplies. Therefore, while the gains obtained may not necessarily reach the highest potential, they can see dramatic improvements.
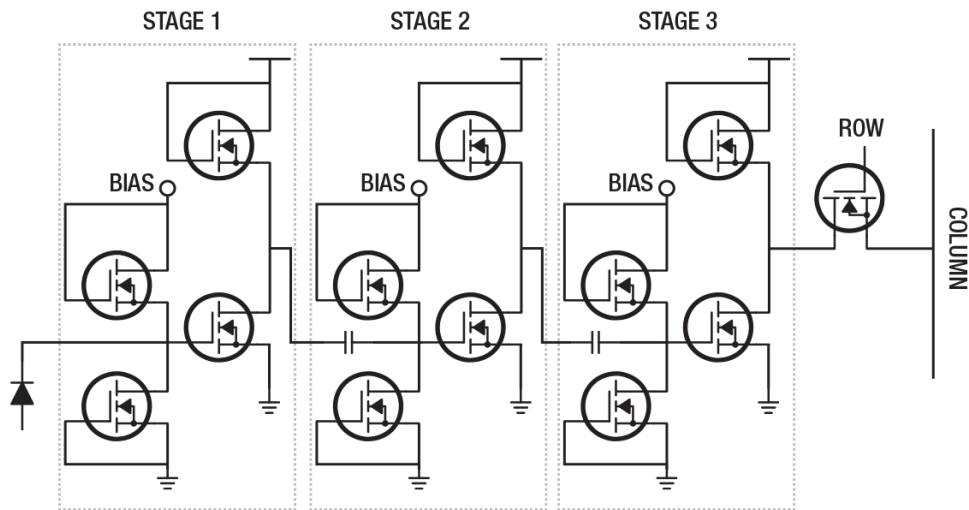
Figure 18: Schematic of a second generation three-stage APS preamplifier.

---

[1]This new design effort was done in collaboration with my colleague, George R. Kunnen.

Table 3: Table of the measured APS gains for different number of stages and various bias voltages.

Vbias	2-Stage	3-Stage	4-Stage	5-Stage
1.5 V	8 V/V	11 V/V	14 V/V	40 V/V
2.0 V	12 V/V	17 V/V	30 V/V	100 V/V
2.5 V	15 V/V	25 V/V	50 V/V	180 V/V
3.0 V	16 V/V	32 V/V	72 V/V	320 V/V
3.5 V	17 V/V	38 V/V	90 V/V	420 V/V
4.0 V	17 V/V	29 V/V	88 V/V	300 V/V
4.5 V	13 V/V	15 V/V	58 V/V	72 V/V
5.0 V	9 V/V	8 V/V	22 V/V	19 V/V

Note: The input signal was a 10 mV, 10 Hz square wave signal from 2.99 V to 3.00 V obtained from a function generator. V_{DD} was set at 20 V.

Preliminary gain measurements were made at different biasing points for the various number of stages. Lower stage amplifiers were particularly of interest to see if it would be possible to achieve the same gain but with fewer transistors and less space. These results can be seen in Table 3.

Similar to the gain characteristic test measurements made in the previous generation, a signal of known voltage step was fed into the amplifiers and compared to the voltage step at the output via an oscilloscope capture. It is important to note that while these measurements give a good approximate idea of achievable gains and optimal bias points, the process variations from APS to APS differ and so these optimal bias points are not necessarily universal.

3.2.2.1 Key Experimental Results of Second Generation APS

While the gain results from Table 3 were promising, it was important to prove that the amplifiers were more effective in making incident alpha strikes more detectable. A sample of

two-stage and four-stage outputs with observable alpha strikes are presented in Figures 19 and 20. These measurements were once again conducted with the OPF480 PiN diode and a ^{210}Po alpha source.

Even with the two-amplifier, the alpha strikes are very evident and produce an output equal to, if not greater, than a four-stage amplifier of the previous generation. The four-stage amplifier produced even greater output strength putting it well above the noise floor to be detected by even basic peak-detector circuitry. This boded very well to suggest the feasibility of this approach.

The most significant finding from this design, however, was that the gain was sufficient enough to detect alpha particles that entered a CdTe diode fabricated at UTDallas. The output signal capture can be seen in Figure 21 and 22. In Figure 21, while not as prominent as the outputs when using the commercial Si diode, the amplitude was reasonably large enough to be read by external readout circuitry. This was key in proving that all of the necessary components were capable of performing sufficiently to function in a fully integrated system. Results were only better when a new batch of samples were received from UTDallas yielding output signals of nearly 1.2 V, Figure 22.
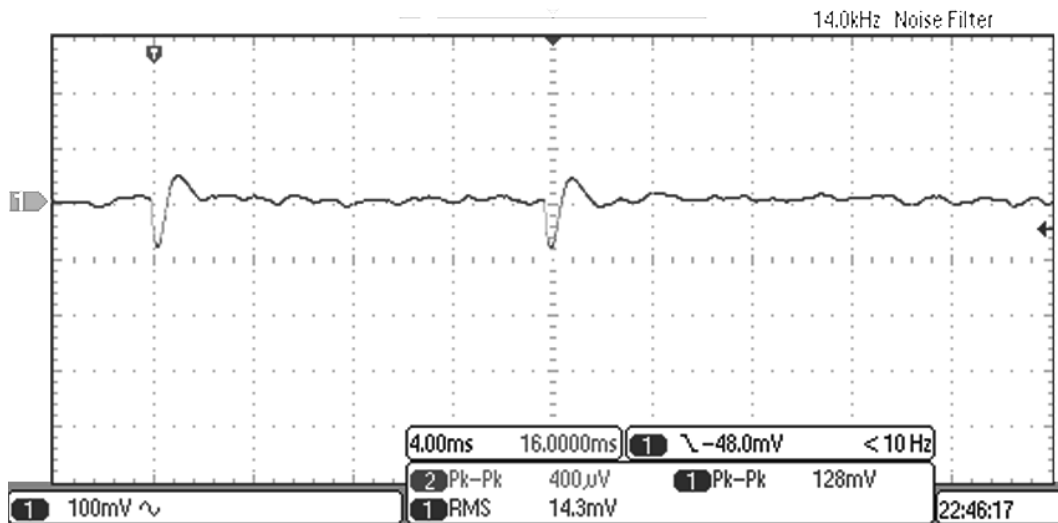
Figure 19: Two alpha responses seen at the output of a second generation two-stage APS with OPF480 diode and ^{210}Po source.
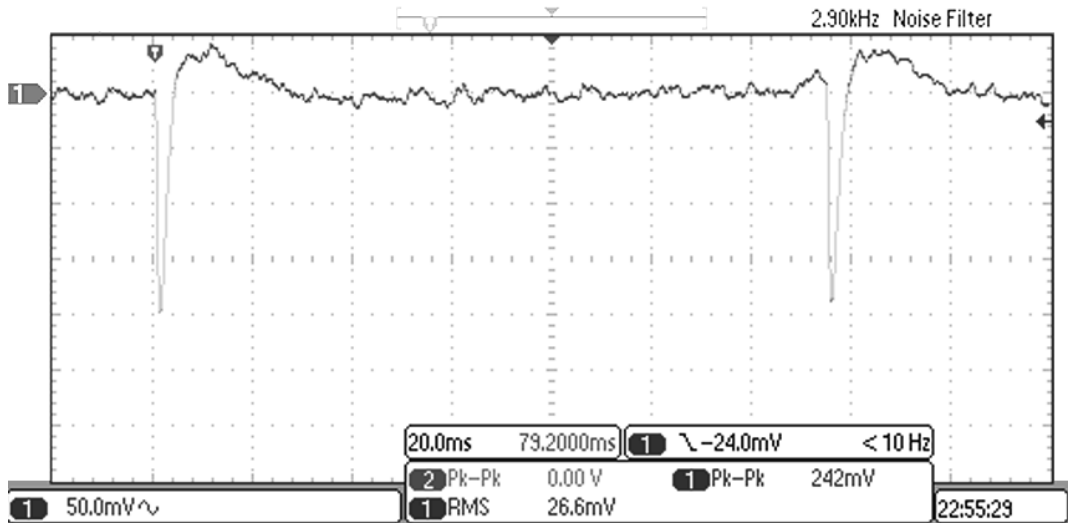
Figure 20: Two alpha responses seen at the output of a second generation four-stage APS with OPF480 diode and ^{210}Po source.
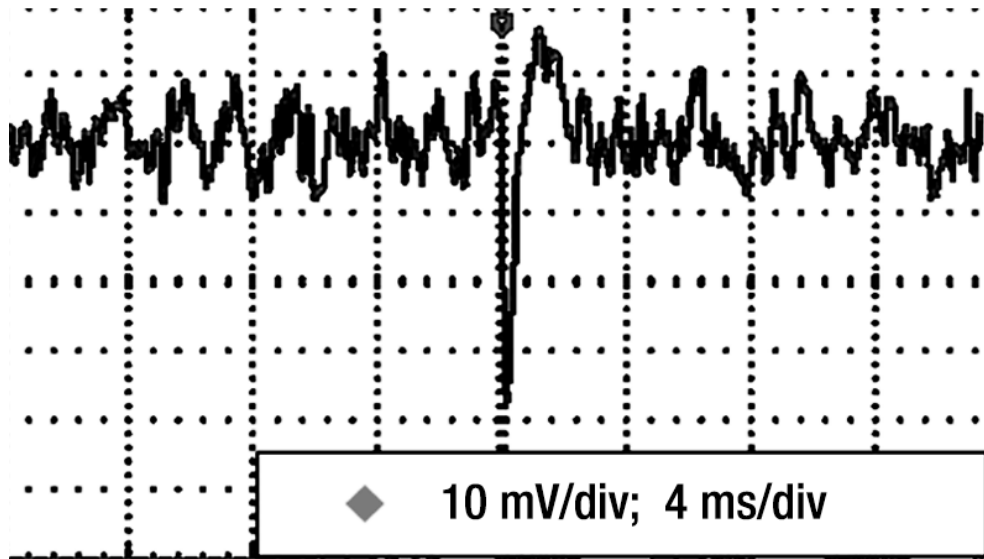
Figure 21: Observable alpha strike using a second generation four-stage APS preamplifier on InGaZnO in conjunction with a CdTe diode 500 μm in diameter fabricated at UTDallas.

43
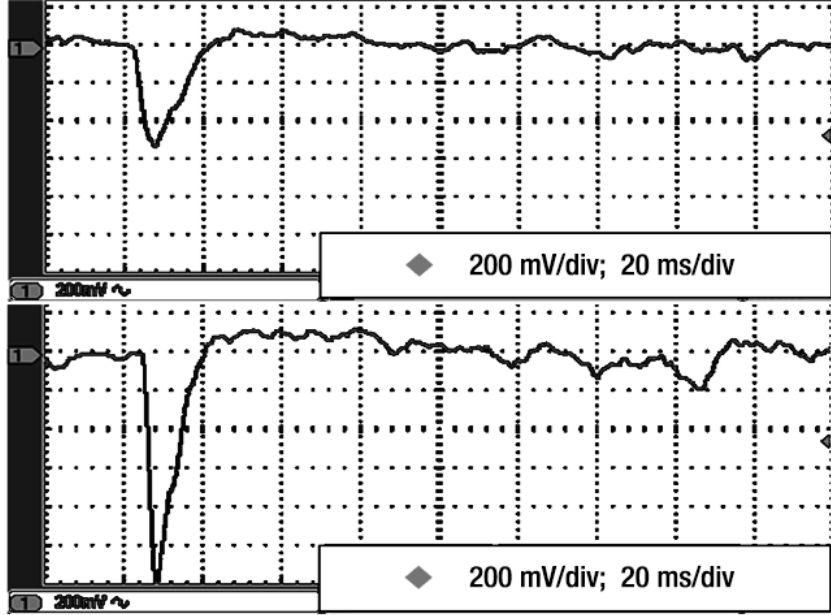
Figure 22: Observable alpha strike using a second generation four-stage APS preamplifier on InGaZnO in conjunction with a CdTe diode 300 μm in diameter fabricated at UTDallas.

3.2.2.2 Why Four is Greater than Five

To this point, the four-stage amplifier has been presented to exemplify optimal performance despite higher gains being seen in the characteristic tests in Table 3. While the five-stage had the potential to yield greater gain, it was not uncommon for the amplifier to become unstable due to higher order effects, Figure 23. Additionally, while the external bias port provided greater control, there were still process variations within the transistors of each APS.

Thus, the greater the number of transistors lead to a greater chance for the amplifier to shift out of the optimal operating points and experience undesirable transient effects. Furthermore, the operating points could shift so severely that gain would actually decrease by the final stage. Note that the alpha strikes in 23 is actually smaller than what had been achieved with some four-stage amplifiers. With the need for more amplifiers but available room with each mask set running low, it was decided to optimize the maximum number of

44
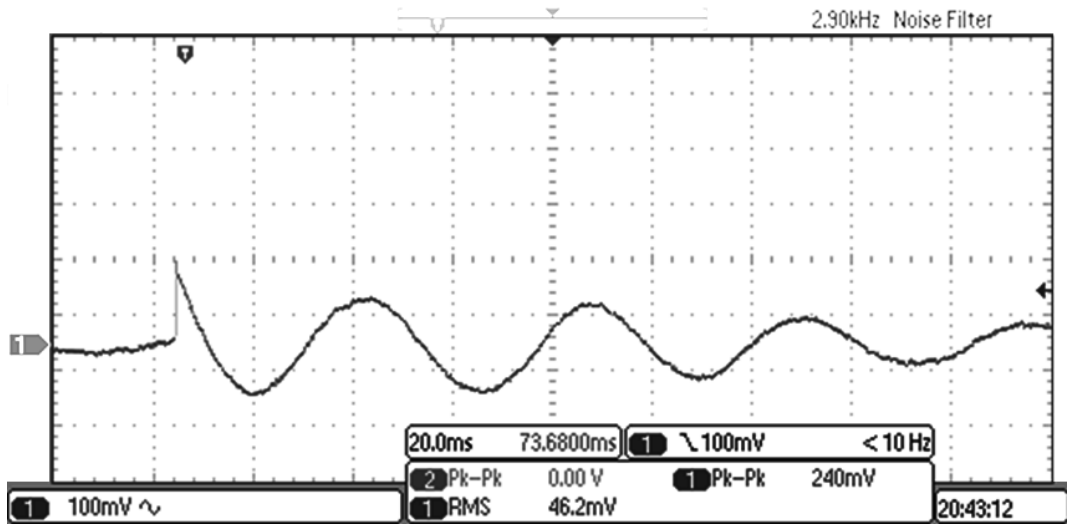
Figure 23: Observed alpha strike using a 5-stage APS with an OPF480 diode and ^{210}Po alpha source. Note the higher order transient effects seen in the tail.

working amplifiers by focusing on just the four-stage design, which did not experience these problems.

3.2.2.3 FDC50 Mask Run Results

Another mask was fabricated at FEDC for the second generation multi-stage amplifiers. Being the 50th pizza mask run at FEDC, amplifiers from this set will be referred to as the FDC50 mask set.

This time, only the four-stage design was fabricated due to the aforementioned reasons. Again, the InGaZnO TFTs were the circuits of interest. Measurements in a probe station with a known test pulse revealed that these amplifiers achieved gains of around 200 V/V, Figure 24, which was far above what had been seen thus far in a four-stage amplifier. It is believed that the improved gain performance is due to the constantly improving process control done by the engineering team at FEDC.

Knowing that our amplifiers were capable of detecting alpha strikes using the UTDallas
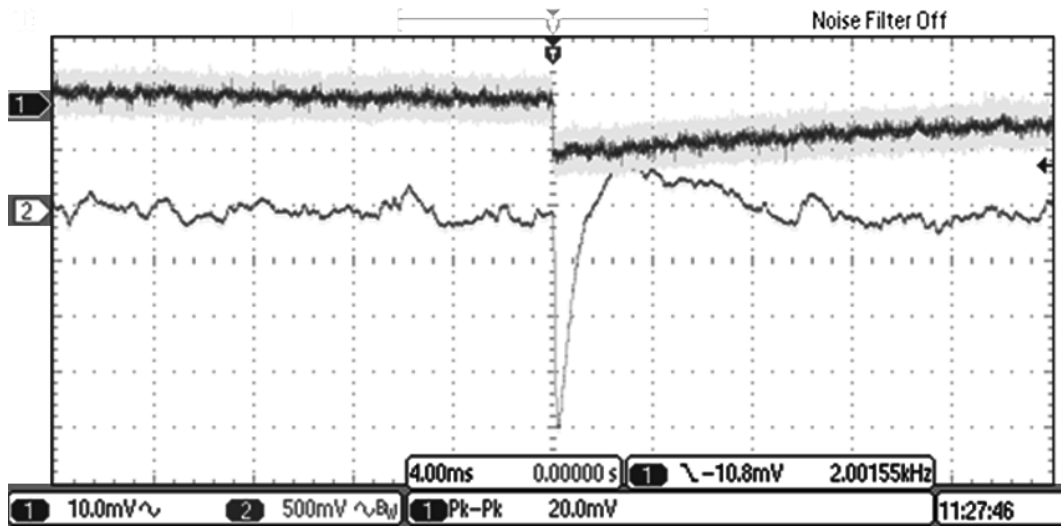
Figure 24: Gain characteristic test with a four-stage APS amplifier from the FDC50 mask set.

CdTe diodes, our next goal was to integrate the two into a single package as opposed to hardwiring the discrete components in a spread out fashion. The FDC50 amplifiers were a part of that integration effort which will be discussed in the following chapter.

Chapter 4

SYSTEMS LEVEL VIEW OF SEMICONDUCTOR DETECTOR

This chapter covers the steps taken to reach an integrated system. Various tasks needed to be accomplished including finding methods to integrate the InGaZnO amplifiers with CdTe diodes in a single package, developing a full integrated system on a single substrate using ZnO, design considerations for readout circuitry, and simulations to demonstrate the efficacy of a full large-area system.

4.1 An Integrated Package

Before developing a large-area array of sensors, it was important to prove that it was feasible to have a single working compact active pixel sensor. This task was approached with a two-pronged approach: 1) combine a TFT amplifier on InGaZnO developed at the FEDC at ASU with a CdTe/CdS diode developed at UTDallas in a 3-dimensional integration package and 2) develop and fabricate a TFT amplifier on the ZnO process run at UTDallas to fabricate both the diode and preamplifier on the same substrate.

4.1.1 InGaZnO APS with CdTe Diode

A key to the success of such an array requires an in-pixel amplifier with a high enough gain and signal to noise ratio to detect the small change in charge induced by the sensing unit, a task proven to be nontrivial with the limitation of an NMOS-only TFT process. It has been demonstrated through the evolution of our TFT amplifiers that such a task is feasible.

These adjustments have yielded improvements from 2 V/V gain to 90 V/V gain with output pulses improving from 2 mV to 1.2 V. With even further improvements made

to the InGaZnO process at FEDC, the current generation of amplifiers have yielded more consistent, high-performing circuits with gains of 200 V/V on even cursory measurements before parameter optimization, Figure 24.

With the current generation of amplifiers providing such high and reliable gains, it has been a motivation to find a method to integrate the APS preamplifiers made at FEDC with the CdTe diodes from UTDallas. Though not a truly fully integrated system, as they are not on the same substrate, the experimental results from the a-Si:H diodes suggested that such a system may not be immediately feasible on the FEDC process.

This brought about the inspiration for the 3-dimensional integration method, Figure 25, which places the preamplifier upside down so that the substrate of the device is open-face. The diode is then mounted directly on top of the preamplifier, though technically on the bottom-side of the preamplifier.

For testing purposes, the preamplifier was bonded to a PCB with a fan out pin layout for easy access to drive and read pads. The CdTe PiN diode pins, namely the anode and cathode, could then be connected to the same PCB via wire bond. The PCB could also be designed and used for other applications such as array connections and drivers, making the application scalable.
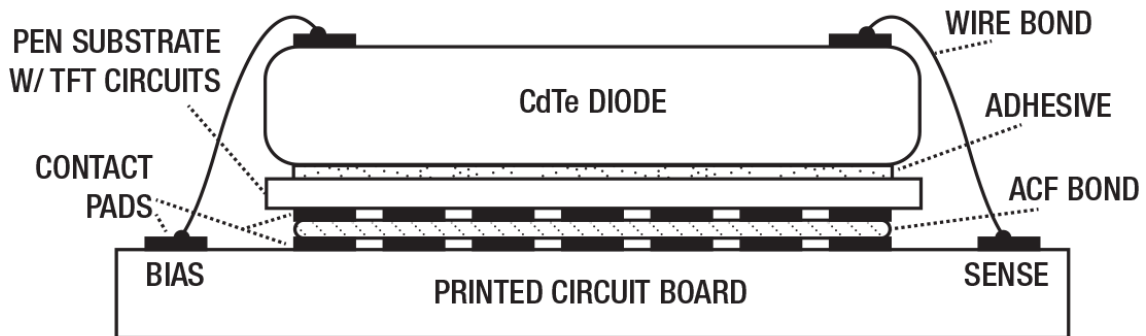
Figure 25: Cross-sectional view of the 3-dimensional integration concept of combining an FEDC APS preamplifier with a UTDallas CdTe PiN diode.

Figure 26: Top view (left) and bottom view (right) of an InGaZnO TFT preamplifier bonded to a pinout PCB.

Source: This package was assembled by John Stowell, a lab technician at FEDC.

Several obstacles were encountered and overcome when using this design. The first was degradation of the transistors in the preamplifier due to the high temperatures used in the ACF bonding process. The degradation would cause gain performance to drop by up to 40% or sometimes destroy key transistors rendering the circuit nonfunctional. To accommodate for this, a lower temperature process was developed[2] (net reduction of 70 degrees Celsius) which yielded marginally more consistent functional and high-gain circuits.

There were also issues of microcracks, Figure 27, forming on the amplifier pads due to the high force inflicted from the heat rod when bonding directly onto the PCB, causing open circuits in key connections. This was addressed by implementing an intermediary heatseal ribbon cable which was connected to the TFT amplifier on one end with a low pressure bonding method, and connected to the PCB on the other with as much pressure needed to bond the durable heatseal strip.

---

[2]The new bonding process was developed by John Stowell who also assembled all of the packages.
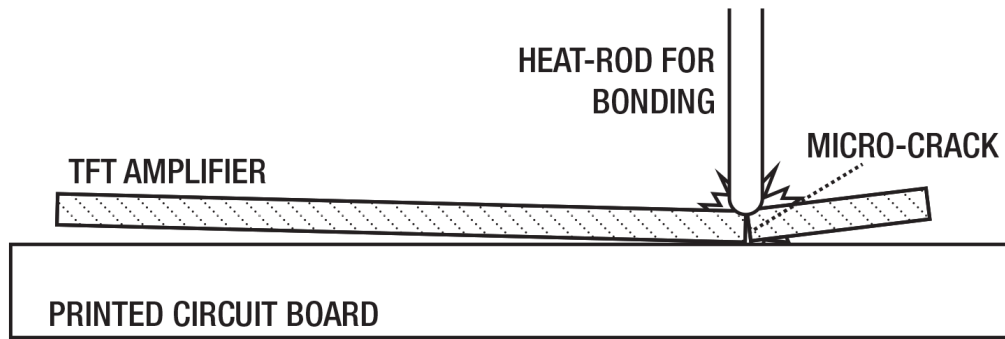
Figure 27: Demonstration of how microcracks were formed in TFT amplifiers during the bonding process.
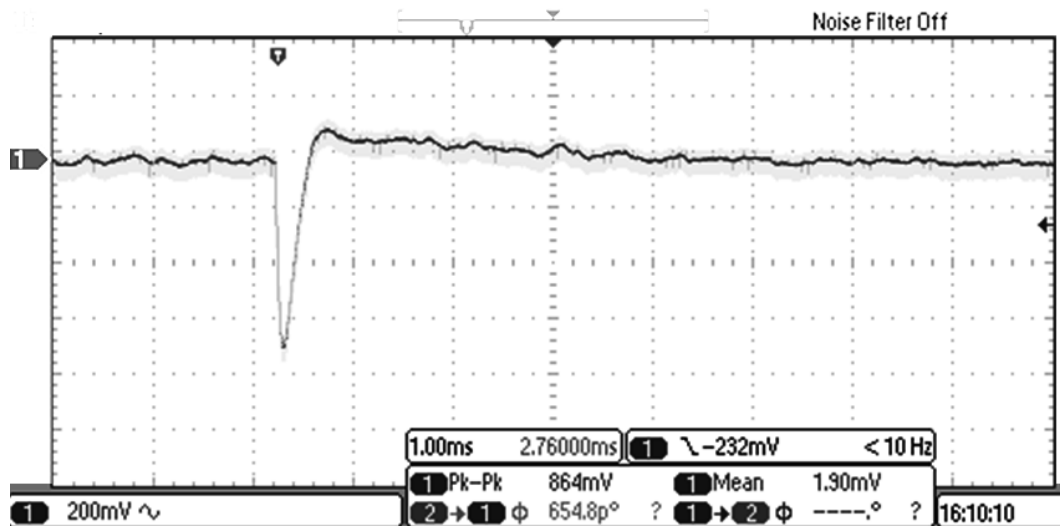
Figure 28: Observable alpha strikes with bonded four-stage InGaZnO preamplifier with an OPF480 PiN diode.

Note: This amplifier reported a gain of 200 V/V, powered at 20 V V_{DD}, and biased at 3.2 V.

The preamplifier was bonded in such an orientation so that the cable could be folded on itself so that the substrate of the circuit could still face up. The heatseal method also helped dissipate the temperature before reaching the TFTs in the amplifier. The combination of the low temperature method with the heatseal strip yielded minimal performance losses with our best amplifier yielding 200 V/V gain both before and after the bonding process.

The bonded amplifier was then first tested with the commercial Si OPF480 PiN diode

to test for alpha particles from the ^{210}Po source. While some fine tuning was necessary, it was capable of detecting alpha strikes, Figure 28. This is not all too surprising seeing how the bonding process did not affect the gain for this particular device and that four-stage amplifiers have been able to detect alpha particles when using the OPF480 diode.

The more pertinent task was to successfully combine a CdTe diode with said amplifier. While this was accomplished with previous batches of preamplifier and CdTe diode combinations, it proved to be more difficult with the current set. It is believed that the newly packaged CdTe diodes we were working with had too high of a capacitance[3].

Several methods were and are currently being explored to overcome the effect of the capacitance. The first approach is adjusting the CdTe diode parameters at UTDallas including decreasing the diameter while increasing the intrinsic length to reduce the capacitance. They are also looking at ways to replicate the diodes from previous runs which had significantly smaller parasitic capacitances.

The second approach was to experiment with alternative front-end circuitry modifications. One such modification was using a cascode stage. This method was inspired from the front-end design practices used to reduce the effect large parasitic capacitances found in photodiodes [54]. The logic behind the cascode stage, Figure 29, is to minimize the voltage swing across the parasitic capacitance. In the example of a BJT, emitter current is transferred to the collector while still keeping the emitter at a roughly constant voltage.

Since the proposed solution requires very few external components (one extra transistor), SPICE simulations were run to test the viability of integrating this design on the InGaZnO process for the next FEDC mask run. The schematic, Figure 30, was simplified so as just to see the effect of the cascode setup on the gain of one amplification stage with various parasitic capacitances.

---

[3]This run of CdTe diodes had a diode capacitance of 18-24 pF as opposed to 8-10 pF in previous runs. The effect of the diode capacitance can be read in further detail in Chapter 2.
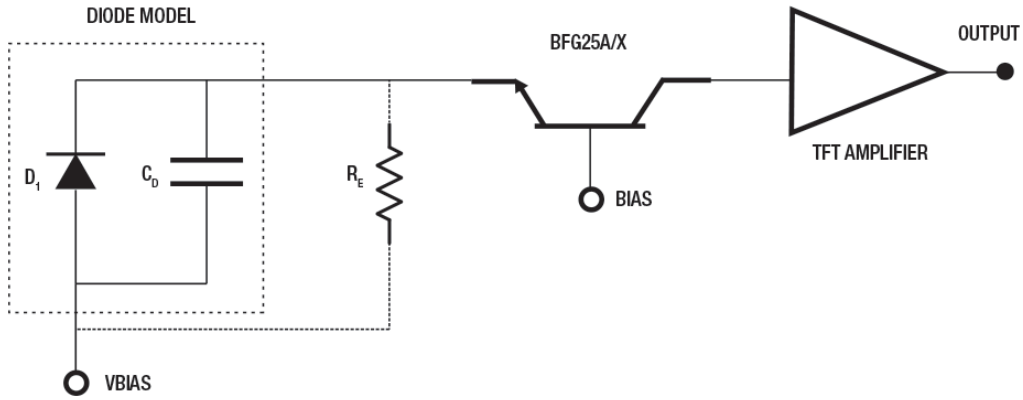
Figure 29: Schematic of cascode front-end setup with a preamplifier.

Source: This schematic is based off of the design presented by Hobbs [54].

Table 4: Table SPICE simulation results to see the effect of parasitic diode capacitances and cascode stages on a one stage APS gains.

C_{diode}	Cascode Stage	Input Swing	Output Swing	Gain
20p	no	8.2mV	35.9mV	4.38 V/V
1p	no	82mV	8000mV	97.56 V/V
20p	20V bias first	8.0mV	35.1mV	4.38 V/V
1p	20V bias first	60.2-118mV	259.2mV	2.2-4.3 V/V
20p	20V bias second	8.0mV	36.6mV	4.6 V/V
1p	20V bias second	58.3mV	26.7mV	4.6 V/V

Note: Simulations were run using LTSpice with a custom InGaZnO bsim3 library. "Bias second" implies that the bias stage was placed after the cascode stage as seen in Figure 30 and "Bias first" implies that the input was biased before entering the cascode.

Table 4 shows the results of the SPICE simulations and it appeared that the cascode stage did not have as great of an impact as anticipated. This is believed to be because the transconductance of the InGaZnO transistors are not as high as that of BJTs. Therefore, the effective resistance in the transistor to allow the current to flow would be too high. Still
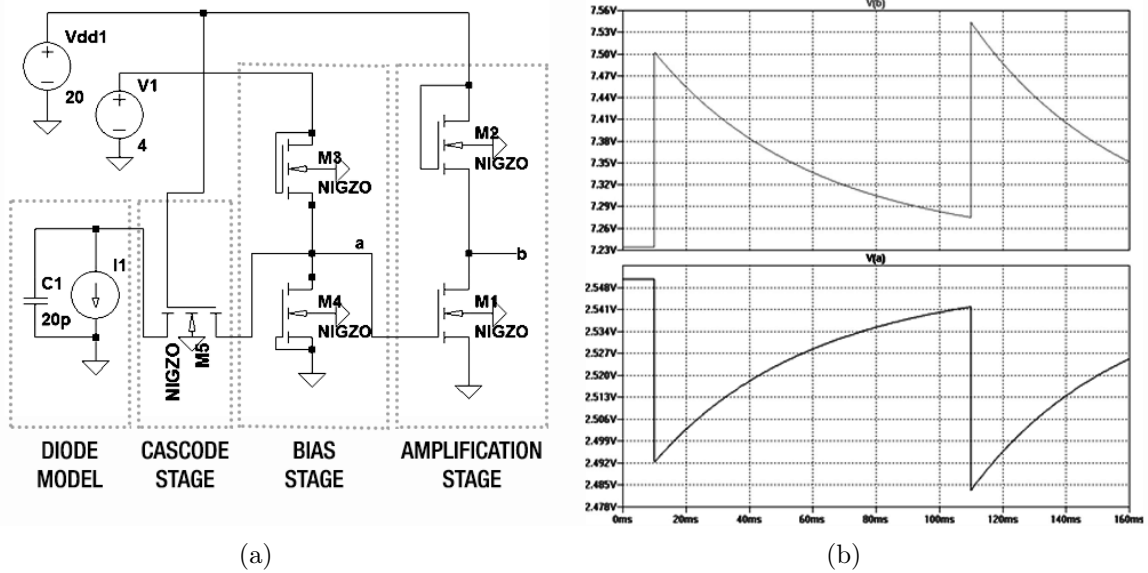
Figure 30: (a) Netlist of SPICE simulations to test the effect of the cascode stage and (b) a sample SPICE output after one stage (top) and corresponding input (bottom).

in an effort to utilize the current as opposed to the voltage, other methods are being sought after, e.g. a current mirror, which will be discussed in the following chapter.

4.1.2 Fully Integrated APS on ZnO

The second method in our two-pronged approach concerns developing and fabricating a reliable high performance preamplifier on a ZnO process for the ability to fabricate both the amplifier and the diode on the same substrate. These devices are relatively inexpensive and are fabricated at UTDallas.

In an attempt to debug issues at the device level and pinpoint the necessary modifications in the fabrication process, we designed an amplifier layout with access pads on all of the input and output nodes of the intermediary stages as well as individual bias controls at each stage for further optimization. To accommodate for the increase in pad counts (a total of 15 as opposed to 6), the layout was designed to be used with a Wentworth Laboratories probe card, Figure 31.
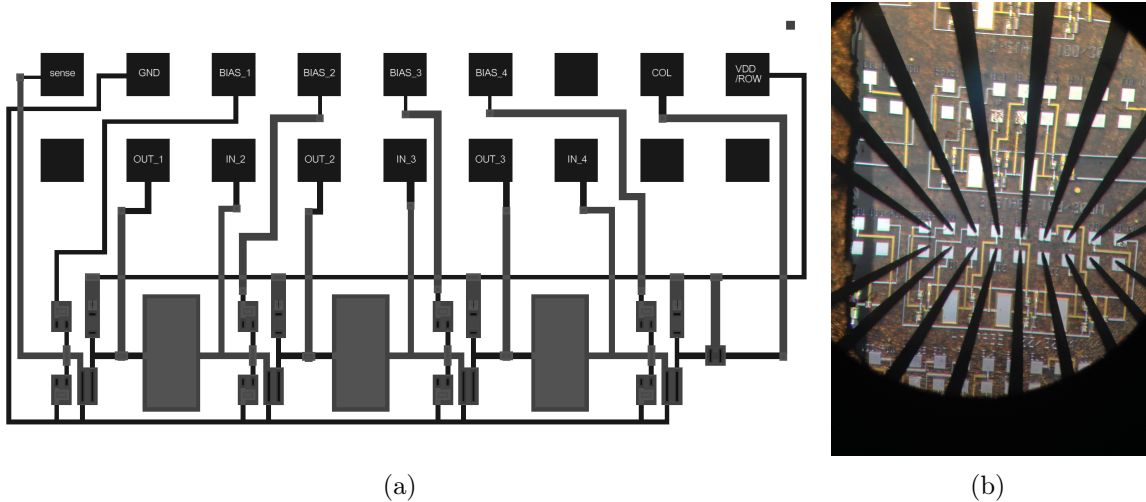
Figure 31: (a) Layout of a four-stage amplifier using ZnO with extra access pads and (b) a microscopic photograph of a four-stage APS on ZnO with a probe card.

With the ability to access intermediary stages, each stage is now capable of being tested in isolation as well as any combination of consecutive stages. Numerous samples[4] were first tested to determine gain characteristics. Similar to gain characteristic tests done for the InGaZnO amplifiers, a known test pulse was fed into the amplifier and measured at the various stages. Slight adjustments were made, e.g. lower power supply voltage, to accommodate for the different process.

Amongst all the permutations of testing setups, a meaningful output was only occasionally seen at the output of the first stage, Figure 31. The output at subsequent stages either displayed transients or no signal at all. This occurrence has been attributed to the leakage current, particularly in the large capacitors incorporated in each stage of the preamplifier, but could also be due to low TFT yield.

---

[4]ZnO amplifier samples were fabricated and provided by UTDallas
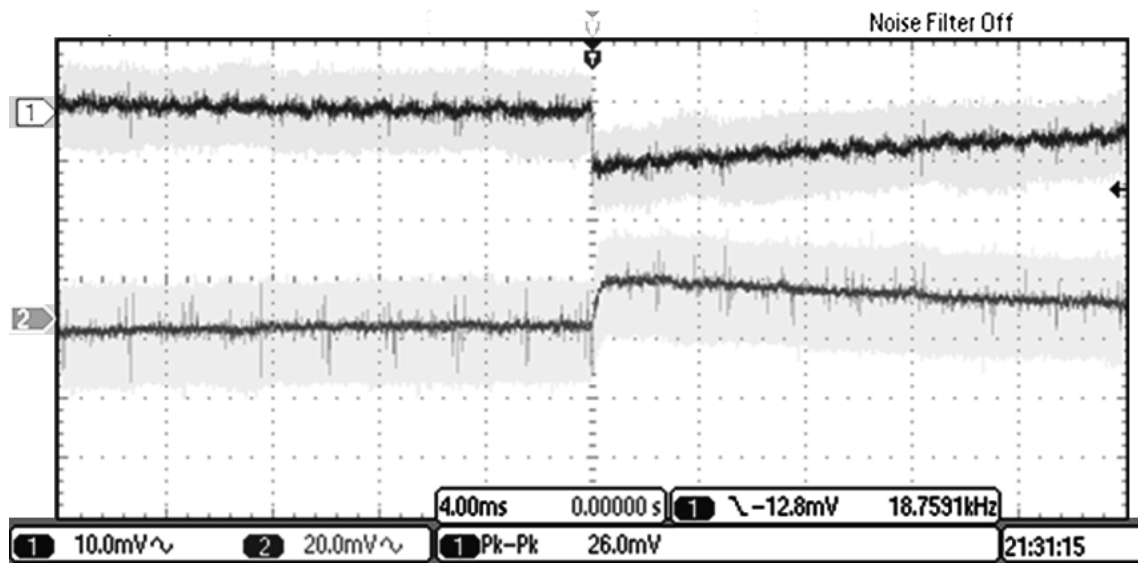
(a)
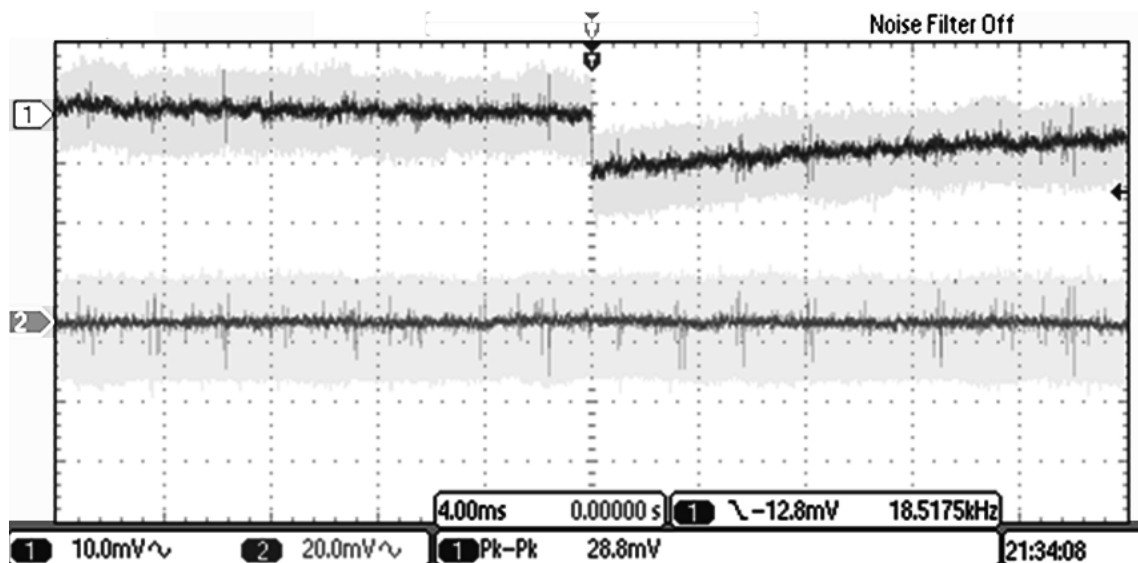
(b)

Figure 32: (a) Output of ZnO APS at the first stage. (b) Output of ZnO APS at the second stage.

Note: A lower V_{DD} voltage of 7.5 V was used to accommodate for the ZnO limitations. The test pulse was a generated 10 Hz square wave from 1.99-2.00 V and 2.99-3 V.
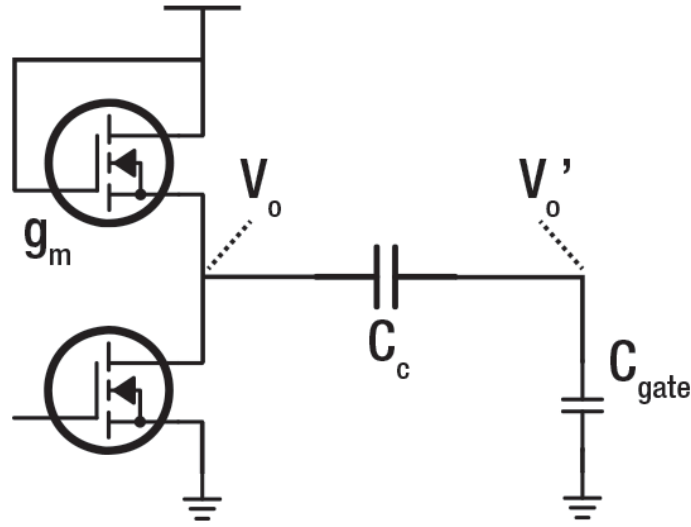
Figure 33: Schematic of the section pertaining to the output of an amplification stage, the parasitic gate capacitance to the input into the following stage, and the coupling capacitor connecting the two.

The larger the capacitor, the greater the probability that process variations can cause the capacitor to leak. Simply making smaller capacitors is not a viable option however. Observing Figure 33 and its corresponding calculations, Equations 4.1 and 4.2, the dominant pole and the voltage entering the subsequent stage is greatest when the coupling capacitance is large.

$$p_{\text{dominant}} = \frac{g_m}{\frac{C_c C_{gate}}{C_c + C_{gate}}} \tag{4.1}$$

$$\frac{V_o'}{V_o} = \frac{C_c}{C_c + C_{gate}} \tag{4.2}$$

Further research and development have yielded capacitors with lower levels of leakage which suggests a promising possibility of a fully functional amplifier. Our partners at UTDallas are currently working on unit process improvements to eliminate these issues.

One of the approaches we are testing is to replace the HfO_2 with Al_2O_3 for the capacitor dielectric.

It was also found that V_{DD} should be 3-4 times the value of V_{th} to achieve maximum gain. This prompted the investigation of Al_2O_3 also as an alternative gate dielectric because of its higher breakdown voltage, as compared to the low temperature HfO_2 gate dielectric. One of the concerns with switching to Al_2O_3 was the lower mobility for ZnO TFTs with an Al_2O_3 gate dielectric. Previously, the mobility for ZnO TFTs with Al_2O_3 as the gate dielectric was 2.5 cm^2/V-s.

UTDallas have reported an improved process to the point where their 15 nm thick Al_2O_3 gate dielectric TFTs have shown mobilities of 10 cm^2/V-s, which is comparable to results from their 15nm HfO_2 gate dielectric flow, as well as consistent V_{th} of 3 V. One-stage amplifiers manufactured with these TFTs have demonstrated gains of 2 V/V with breakdown voltages of the capacitors greater than 15 V. Capacitors with less than 10,000 μm^2 in area exhibit low leakage currents of less than 1 nA up to approximately 8.5 V.

It is believed that the leakage current for the big capacitors is due to extrinsic defects in the dielectric films. The change in dielectric material from HfO_2 to Al_2O_3 also improves device integration, because Al_2O_3 requires less aggressive etching compared to buffered oxide etch which would etch the glass substrate and cause roughness in subsequent layers.

4.2   Charge Storage Peak Detector Circuitry for Readout

In an active matrix array of pixels, it is required that readout occur before the pulse dissipates. Therefore, rows have to be polled quickly to scan through the entire array to ensure a pulse is caught. With an output pulse tail lasting approximately 100 ms, a minimum 10 Hz frame rate is necessary. The problem is further complicated by gain and offset variations from pixel to pixel due to process variations inherent in amorphous TFT fabrication. Some calibration of each pixel is necessary to know what pulse voltages would be expected from each pixel.
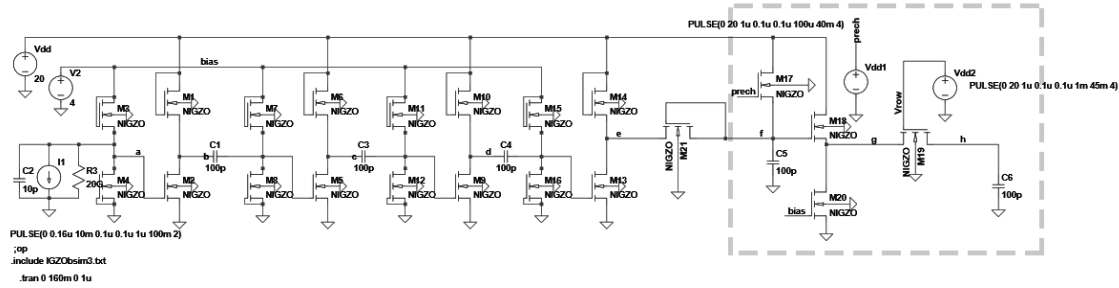
Figure 34: Schematic of a four-stage APS preamplifier with peak detector and readout circuitry (highlighted by the dotted box).

Note: A lower V_{DD} voltage of 7.5 V was used to accommodate for the ZnO limitations. The test pulse was a generated 10 Hz square wave from 1.99-2.00 V and 2.99-3 V.

This problem has been addressed with a new design that adds a peak detector circuit to the amplifier output, Figure 34. Peak detection and storage eases the reading of the array so it is no longer necessary to catch the pulse before it decays. Each pixel stores the minimum voltage at its output which is precharged after every read. A high voltage indicates that no strike on that pixel has occurred while a low voltage indicates at least one strike on that pixel has occurred since the last reset or precharge of the storage node. Since the number of events is low, it is unlikely to have more than one event on a given pixel in a single frame.

Transistors M1 to M16 are unchanged from the previous four-stage preamplifier design. The peak detector circuit begins with diode connected transistor (M21). This could also be replaced with an actual diode. This is followed by the precharge transistor (M17) and source follower / access transistor (M18 to M20). With this circuit, the peak of a pulse is captured and stored on the 100 pF capacitor (C5). When the row is asserted, the stored voltage is read on the column (node h).

Note that the diode (M21) can be fabricated at FEDC using their InGaZnO process. Alternatively, the diode can be implemented with the development of thin film a-Si PiN and avalanche PiN diodes, also at FEDC.

SPICE simulation verifies the operation of this new amplifier design, Figure 35. Traces
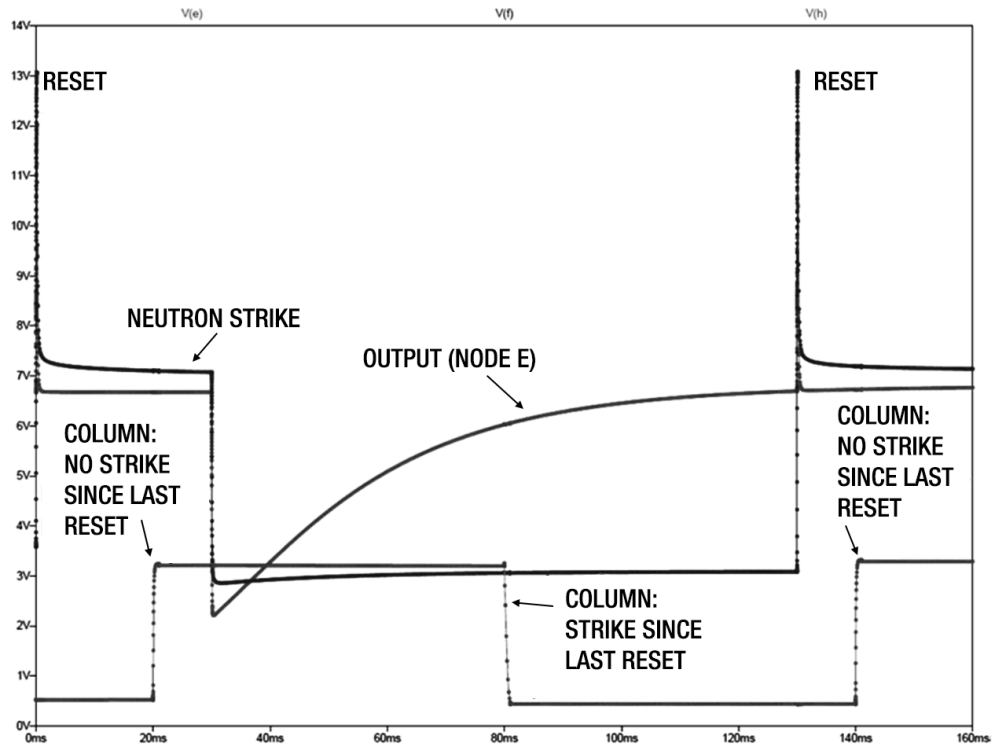
Figure 35: SPICE output of a four-stage APS preamplifier with peak detector and readout circuitry.

for amplifier output at node e (corresponding to a neutron/alpha strike on the pixel) and the voltage on the peak storage node f (reset at time equal to 0 s and 130 ms) can be observed. The voltage on the storage node is about 7 V if there has not been a strike and about 3 V after a strike, as can be seen in Figure 35. The storage node is read at 20 ms (before a strike), 80 ms (after a strike), and 140 ms after the following reset. The voltage read out is low at 80 ms (indicating a strike since the last reset) and high at 20 ms and 140 ms (indicating no strike since the last reset), verifying the proper operation.

It may still be necessary to calibrate the voltage levels corresponding to strike / no-strike for each pixel due to pixel to pixel variations. This task will prove to be much easier with the easy-to-detect large separation between high and low output voltages, demonstrated

above, and the static nature of the readout. These circuits will be fabricated on an FEDC mask set during the next year to experimentally verify the design.

4.3   Large Area Efficiency Simulations

A series of simulations in SoftWare for Optimization Of Radiation Detectors (SWORD) conducted to verify that our large area approach has a greater system efficiency compared with a portable Rad-Pack of ^{3}He proportional counters in a backpack form factor. Although our intrinsic efficiency is currently 5%, our detection array can be fabricated at reasonable cost over large areas by tiling 370 mm x 470 mm panels. This is the standard size of a Gen II flexible display or sensing array that can be fabricated at FEDC.

Because of the much larger capture area, the array can more readily detect neutrons than with a higher intrinsic efficiency but smaller detector area. For the simulations a 1 mCi ^{252}Cf neutron source was embedded within a container on a tractor-trailer, Figure 36. This was to model a possible real-life scenario in which nuclear material could be smuggled away discretely with cargo. The detector is a 6x12 array of panels each 370 mm x 470 mm. With 30 mm gaps between the panels, the overall area of the detection array is 2.4 m x 6 m. In the simulation, the array was located 3 m from the source.

Each panel is composed of 5 cm of polyethylene moderator in front and back, a 2.8 μm ^{10}B energy conversion layer, and a 10 μm CdTe detection layer. A SWORD simulation of 1.2x10^7 particles was run, and the spectrum of energy deposited in the CdTe layer was plotted, Figure 36. When defining counts as strikes with energy between 300 keV and 3000 keV, over 6,000 strikes were recorded.

Replacing the detection array with a Rad-Pack at the same 3 m distance resulted in only 63 counts in spite of the 50% intrinsic detection efficiency of the Rad-Pack, Figure 37. This is corresponds to an improvement of approximately 100x for the large area array compared to the RadPack.
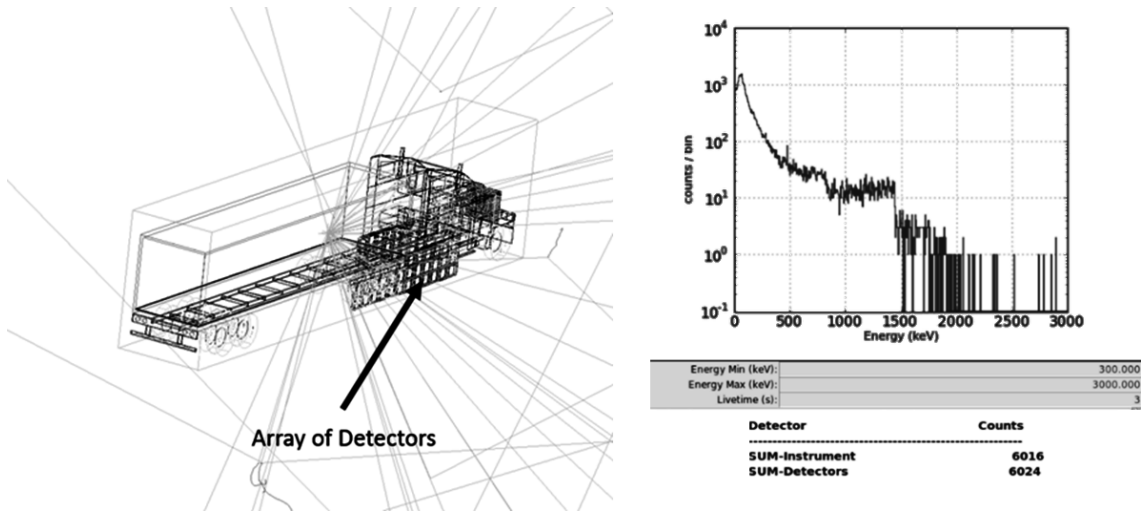
Figure 36: SWORD simulation of ^{252}Cf neutron source in a trailer with a large-area detection array 3 m away. The modeling image generated shows neutron tracks (left) and the energy spectrum for the particle simulation was plotted (right).
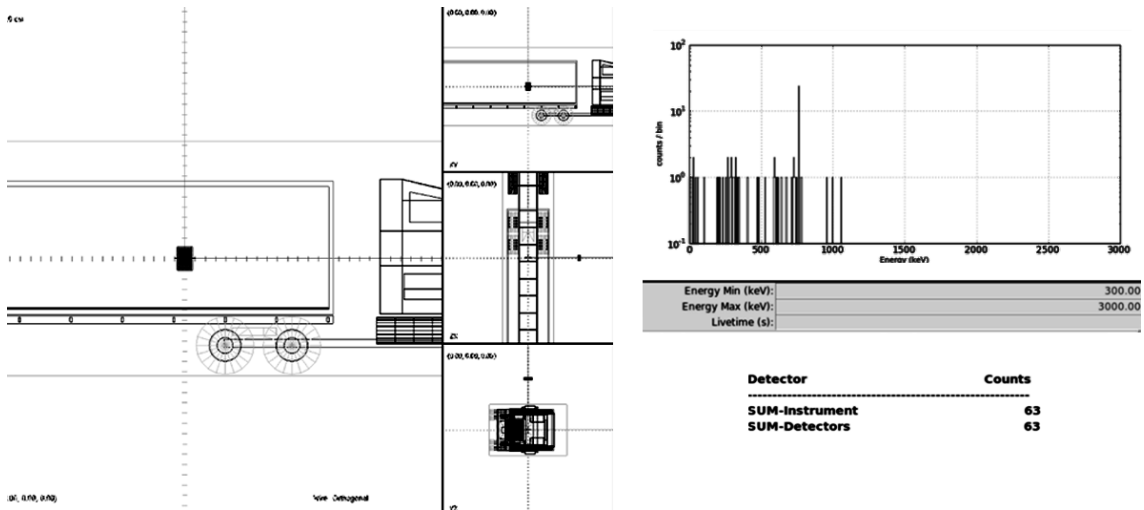
Figure 37: SWORD simulation of ^{252}Cf neutron source in a trailer with a Rad-Pack of ^{3}He proportional counters 3 m away. The SWORD image generated shows the testing environment model (left) and the energy spectrum for the particle simulation was plotted (right).
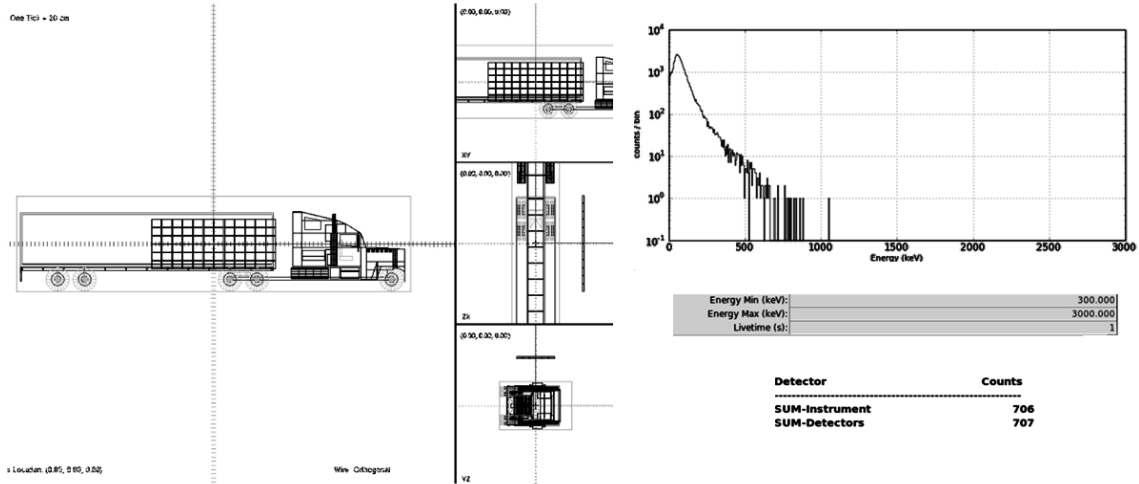
Figure 38: SWORD simulation of ^{252}Cf gamma ray source in a trailer with a large-area detection array 3 m away. The SWORD image generated shows the testing environment model (left) and the energy spectrum for the particle simulation was plotted (right).

These tests have shown significant counts for unshielded neutron sources in both GEANT and MCNP, two platforms used for radiation simulations. Shielded sources, however, show some discrepancy between MCNP and GEANT. This discrepancy cannot yet fully be explained and will be further investigated.

Moreover, the detection array is relatively insensitive to gamma rays. With a 1 mCi ^{252}Cf gamma ray source and the same conditions above, the energy spectrum is shown in Figure 38, and only 700 counts are recorded. In our current detectors, the CdTe layer is approximately 4 μm thick, which reduces the gamma-ray sensitivity by approximately 10x compared to the 10 μm thick diodes used in the simulation.

Chapter 5

FUTURE NEUTRON DETECTION WORK

This chapter covers potential avenues of research the neutron detection project can still take. Some of these approaches are currently under development and are nearing completion while others are working concepts. Ultimately, these efforts strive towards building a functioning prototype of a large-area array of compact and integrated APS units for neutron detection.

5.1 Continued Integration Efforts

The first and immediate step is to produce an integrated package using TFT-based amplifiers and PiN diodes. The two-pronged approach will continued to be pursued in this endeavor in which CdTe/CdS diodes will be combined with either ZnO or InGaZnO preamplifiers.

5.1.1 ZnO Amplifiers

The ideal route would be to have a fully integrated system using the ZnO TFT process from UTDallas. This approach is fully integrated because the entire system can be fabricated on the same substrate in which the thin film CdTe/CdS diodes can more easily be placed with their respective preamplifiers without the need for mechanical bonding. It also has the added benefit of being relatively cheap, having a quick turn-around rate, and being completely fabricated in one location.

For initial runs, however, a two-substrate approach will be used in which the diodes are fabricated separately from the amplifiers. Using indium bumps, the two substrates can be bonded together into a single package.

Preliminary experimental measurements show that reasonable and expected gain can be achieved with the ZnO amplifiers, demonstrated by the output of the first stage in a four-stage ZnO preamplifier. While the coupling capacitors experienced leakage that overwhelmed the circuit, improved devices from UTDallas suggest that this problem can be addressed. The new devices utilize a new dielectric material (HfO_2) which have produced coupling capacitors with leakage currents below 1 nA and breakdown voltages above 15 V. The devices will first have to be characterized for gain when fabricated and then implemented in a fully integrated APS.

5.1.2   InGaZnO Amplifiers

The alternative route is to fashion InGaZnO amplifiers made at FEDC with the CdTe/CdS PiN diodes from UTDallas into some unified package. Despite the obstacles encountered in the 3-dimensional integration approach, there is reason to believe that it is merely a minor setback due to the lower performance characteristics of the most recent batch of devices in particular.

This notion is further supported by the fact that a four-stage InGaZnO preamplifier and a CdTe diode has demonstrated to be capable of successfully detected alpha particles in previous experiments. The main suspect is the high parasitic capacitances on the newly packaged CdTe diodes. Calculations have shown that parasitic capacitances of 18-25 pF will reduce the voltage beyond the detectable threshold, Equation 2.8.

With continued efforts at UTDallas to further improve their fabrication process and replicate low capacitance diodes from previous runs, it is anticipated that suitable diodes will become available in the near future. They are also currently experimenting with other methods to reduce capacitance such as increasing the diode thickness and decreasing the diameter while still remaining in a reasonable region of operation.

FEDC will also have another mask run this year in which more preamplifiers will become available for testing. Once the devices are fabricated, more packages will be assembled.

64

Other form factors can also be explored, as opposed to a single pixel, by modifying the PCB layout to hold an array of sensors.

5.1.2.1   Detecting Neutrons

So far, all of the devices covered have been concerned with detecting alpha particles. Despite being titled as a "neutron detection" project, our APS has yet to demonstrate detecting a single neutron. The reasoning for this is that working with neutron radiation requires following a strict protocol with extensive measures for safety as neutron radiation can be harmful to the body. With the skin depth an alpha particle emitted from a ^{210}Po alpha source being not even strong enough to penetrate a piece of paper, working with ^{210}Po is not only fairly harmless, but also makes the bench test less unwieldy. Detecting alpha particles is still relevant as it is the product of the interaction between a neutron and the conversion layer.

Once a functioning integrated APS is produced, it will be placed in a neutron chamber at UTDallas with a ^{252}Cf source for testing. Detecting neutrons, however, should be a fairly trivial task once the APS is ready as the only necessary step is to apply a neutron conversion layer, e.g. ^{10}B or ^{6}Li, on the CdTe/CdS diode. Colleagues at UTDallas have demonstrated the ability to easily detect neutrons using their CdTe/CdS diodes using this method in the past when used with a conventional charge sensitive preamplifier.

5.2   Front-end Design: Current Mirror

While colleagues at UTDallas continue to improve the device characteristics of their diodes, alternative front-end topology is being explored at FEDC to produce a more robust amplifier that is resilient to the possibility of high parasitic capacitances in the PiN diode. The main limitation is that the new design cannot deviate too far from the known working schematic because space on wafers, let alone mask runs, is running low.
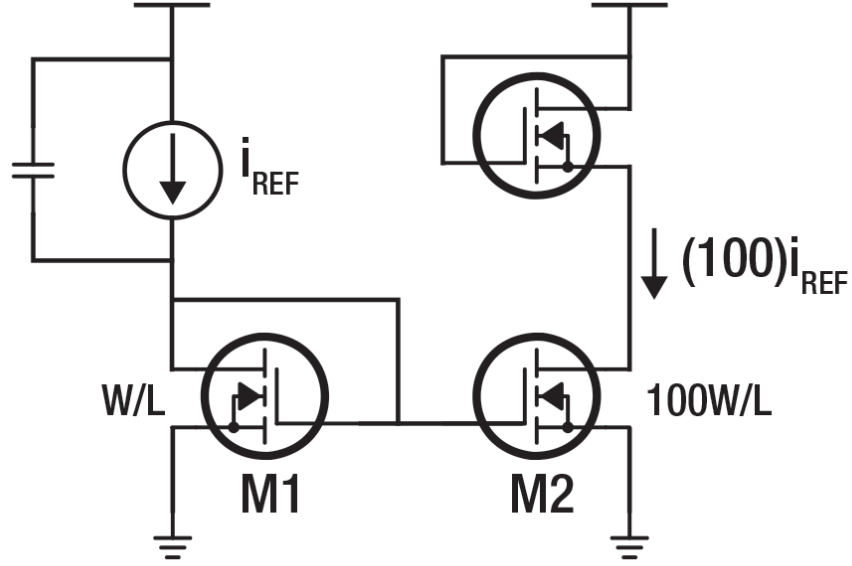
Figure 39: Simplified schematic of a current mirror front-end design.

$$i_{REF} = \frac{1}{2}k'(W/L)_1(V_{GS1} - V_{th})^2(1 + \lambda V_{DS1}) \tag{5.1}$$

$$i_{OUT} = \frac{1}{2}k'(W/L)_2(V_{GS2} - V_{th})^2(1 + \lambda V_{DS2}) \tag{5.2}$$

$$= i_{REF}\frac{(W/L)_2(1 + \lambda V_{DS2})}{(W/L)_1(1 + \lambda V_{DS1})} \tag{5.3}$$

The cascode stage did not seem to produce viable results, but it did present a paradigm shift to focus on amplifying current as opposed to voltage. Utilizing current is more robust because it is not as heavily impacted by the capacitance. This is why transimpedance amplifiers are normally used in photodiode applications. The current mirror is a topology, Figure 39, is currently being tested to see if it is a viable solution when using the InGaZnO process.

The rationale behind the current mirror is to copy the current through an active device regardless of loading. The current from the diode is modeled by a pulse from a current source

(i_{REF}) in parallel with the parasitic capacitance of the diode, Figure 39. Since the transistor receiving the reference current is diode connected, it should always be in saturation. In theory, the current through the second transistor (M2) should be identical to the reference current given that the transistors are exactly the same and is operating in saturation as they are matched under the same conditions.

Furthermore, the current through the matched transistor (M2) is proportional to the W/L ratios between the two transistors, Equations 5.1-5.3. Therefore, by making the width of M2 100 times larger than M1, we should theoretically get a current pulse that is not only less affected by the diode capacitance but also 100 times larger than the reference.

SPICE simulations have yet to verify this principle and, furthermore, a method to utilize the output current of the current mirror needs to be developed. If it suggests to be a feasible solution, the design will be fabricated on the next FEDC mask run for experimental testing seeing how the design is relatively simple without a need for many extra transistors.

5.3   System Level Design

Finally, work is still needed in designing schematics to consider operating in a full array as opposed to single pixel applications. The first task in doing so is developing reliable readout architecture. This is namely addressed with the charge storage and peak detector circuitry discussed and proven in concept with SPICE simulations in the previous chapter.

The next step is to fabricate said circuits on the upcoming FEDC mask run and test the samples experimentally to validate simulation results. Software drivers will also have to be written so that the system can intelligently read, classify, and process neutron strikes. Corresponding hardware to pull the readings and interact with the software drivers will also need to be developed.

Further modeling can also be done to exhibit the absolute efficiency of our system. Real-world scenarios can be modeled such as various nuclear materials under different forms shielding in an array of vessels, e.g. tractor-trailer, cargo ship, etcetera. The efficiency of our

detecting array can be compared to other standards in neutron detection such as proportional counters, scintillators, and even other semiconductor-based neutron detection solutions.

PART II: ELECTRIC FIELD IMAGING

Chapter 6

ELECTRIC FIELD SENSORS: D-DOT SENSOR

This chapter marks the beginning of Part II of this thesis which concerns imaging electric fields. The research presented focuses on quasi-static, VLF electric fields and the ability, for the first time, to image these fields. Topics of discussion in this chapter include the mechanisms of the electric charge induction sensor (also known as the D-dot sensor) and the motivation of studying VLF.

Relating back to the problem scenario presented in Chapter 1, such a device could be used in conjunction with a neutron detector to monitor, inspect, and classify concealed explosive devices. An electric field imager extends far beyond just bomb detection, and can be used in a plethora of other applications including imaging power lines at construction sites and (most notably) electromagnetic interference (EMI) detection.

6.1 Why VLF?

The electromagnetic VLF range is defined to be the frequency range between 300 Hz to 30 kHz [55]. Though the experiments in this manuscript go into frequencies below this range into the extremely low frequency (ELF) range, they are still relatively close ($\sim$100 Hz) and thus for simplicity will be regarded as VLF.

One of the greatest advantages of VLF, unlike MHz and GHz waves, is its ability to penetrate objects [55]. Submarines take advantage of VLF/ELF waves in underwater communication since they are capable of penetrating through the water [56]. It is also why VLF/ELF waves are frequently utilized in subterranean mapping whether it is geophysical prospecting for ore and oil or beach-goers with their metal detectors. This property is also important in our application since one of the objectives is to see through concealed containers

and that power lines are operated at low frequencies (e.g. 60 Hz in the Americas and parts of Asia and 50 Hz most other regions).

6.2   The D-Dot Sensor

D-dot sensors sense current proportional to the time derivative (dot) of the electric flux density (D), hence the name. They are very sensitive and have successfully detected high velocity bullets [27], [29] passing by that induced charge on the order of pC [27], [57]. Furthermore, D-dots are cost effective, compact, and elegant in design in which the most basic functioning design can be implemented simply with a flat conducting ground plate. Due to its high sensitivity and ease of fabrication, the D-dot sensor was chosen for the imaging array.

6.2.1   Electrostatic Theory

Charge distributions result in electric flux lines that terminate on opposite charges in the surrounding environment. In the presence of a D-dot sensor, some of these flux lines terminate on opposite charges on the upper conducting plate. The bottom plate of the sensor is a ground reference and the upper plate is held at a virtual ground with an operational amplifier, Figure 40. If the charge distribution above the sensor changes, the number of flux lines terminating on the upper plate changes.

Electric flux terminating on the metallic plate of the sensor induces charge and the time varying electric flux results in small currents flowing on and off the plate to provide the required charge. With the D-dot sensor held at a virtual ground using a transimpedance amplifier, the small required change in charge results in a current flowing through a large feedback resistor (e.g. 10 MΩ - 100MΩ) generating a time varying voltage, the amplitude of which is proportional to the strength of the electric field impinging on the upper plate.
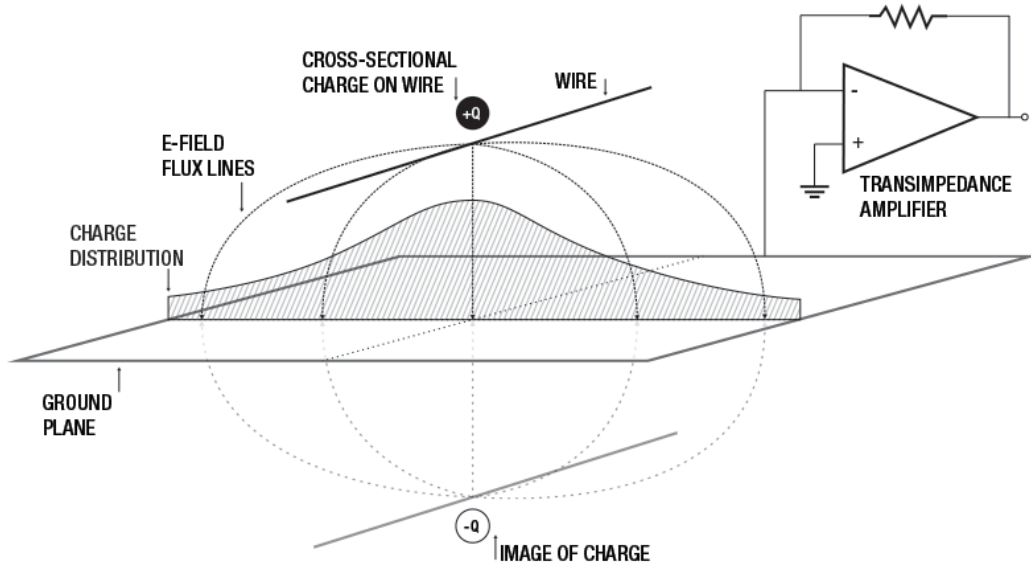
Figure 40: Diagram of the analytic model of a sample of electric flux lines radiating from a wire over a D-dot using the method of images.

6.2.1.1   Wire over D-dot

In the VLF range, the analysis is quasi-static and it is easily shown that the signal produced by a D-dot sensor is directly proportional to the frequency, sensor area, and field strength. Equations 6.1-6.4 demonstrate this relationship when modeling a wire hovering over a D-dot sensor such as the model seen in Figure 40. In the equations, $E_\perp$ is the electric field perpendicular to the D-dot sensor, λ is the charge per unit length of the wire, ϵ is the permittivity of free space, h is the height of the wire from the sensor, V is the voltage applied on the wire, f is the frequency of the signal in the wire, a is the radius of the wire, and A_{pixel} is the area of the D-dot sensor. Although the signal strength is proportional to electrode area, we have demonstrated sensitive electric field detection with small D-dot sensors both experimentally and in simulation.

$$E_\perp = \frac{\lambda}{\pi \epsilon h} \tag{6.1}$$

$$\lambda = \frac{2\pi \epsilon V(t)}{\ln(2h/a)} \tag{6.2}$$

$$V(t) = V\sin(2\pi f t) \rightarrow V'(t) = 2\pi f V \cos(2\pi f t) \tag{6.3}$$

$$i_{Ddot} = A_{pixel}\frac{d}{dt}\epsilon E_\perp \tag{6.4}$$

$$= \frac{A_{pixel}4\pi f \epsilon V'(t)}{h\ln(\frac{2h}{a})}$$

This derivation assumes that the radius of the wire, a, is much smaller than the height so that the center of the wire can be treated as the location of the wire. The current generated at the D-dot is again the time derivative of the electric flux density and is proportional to the area of the sensor, Equation 6.4. As a frame of reference, for a minimum detectable D-dot current of 0.5 pA, a 1 cm^2 sensor can detect a 0.5 mm radius wire energized with a 5 V, 97 Hz signal from as far as 1.2 m away.

The distribution of the electric field magnitudes across a ground plate can be modeled by using the method of images. By taking a cross-section of the setup, it is reasonable to treat the slice of wire over a conducting surface as a point charge in two dimensions.

By the method of images, the electric field along the surface is equal to calculating the net effect of polar charges equal in magnitude and distance from the surface location. After using Gauss Law and some simple algebra, the electric field strength can be calculated by Equation 6.9 in which x_0 is the offset of the point of interest and γ accounts for random noise.

$$E_r = 2\pi rh = \frac{\lambda h}{\epsilon} \text{ (Gauss Law)} \tag{6.5}$$

$$r = \sqrt{h^2 + (x - x_0)^2} \tag{6.6}$$

$$E_z = \frac{E_r h}{r} = \frac{\lambda h}{\epsilon 2\pi(h^2 + (x - x_0)^2)} \tag{6.7}$$

$$E = 2E_z \text{ (by symmetry)} \tag{6.8}$$

$$E = \frac{\lambda h}{\epsilon\pi(h^2 + (x - x_0)^2)} + (\gamma) \tag{6.9}$$

Theoretically, the electric field vectors should be orthogonal to the surface of the sensor. The D-dot sensors, however, have some height and are not perfectly uniform so some fringing is expected, especially on the edges. These deviations are minor and the dominant value is still the orthogonal component.

6.2.1.2   Multiple Wires over D-dot

Mathematically determining the resolution possible by calculating the electric field from multiple wires above a ground plane is another interesting calculation. This derivation is more subtle because each line charge depends on the voltage on all of the wires. Fortunately, this is a well-known problem in the calculation of the electric field around high power lines [58].

In the scenario of two wires above a ground plane, similar to Figure 41, the voltage on line k, $V_{line,k}$, is a function of both line charges Q_k and Q_m. Likewise, the voltage on line m, $V_{line,m}$, is a function of the both line charges. The distance between conductor i and the image conductor j is D_{ij} and the distance between two real conductors i and j is d_{ij}. When i equals j, d_{ij} is the wire radius.
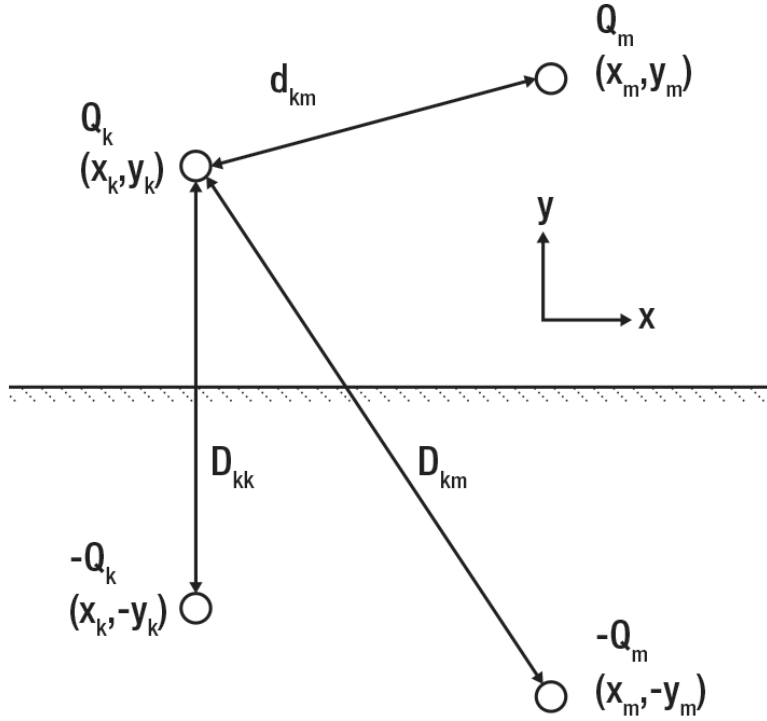
Figure 41: Diagram for determination of electric field for two wires above a ground plane.

$$V_{line,k} = p_{kk}Q_k + p_{km}Q_m \tag{6.10}$$

$$V_{line,m} = p_{mk}Q_k + p_{mm}Q_m \tag{6.11}$$

$$p_{ij} = \frac{1}{2\pi\epsilon}\ln(D_{ij}/d_{ij}) \tag{6.12}$$

$$d_{ij} = a \text{ when } i = j \tag{6.13}$$

These relations can be derived from electrostatics [58] and can be extended to any number of wires above a ground plane. The simultaneous equations become matrices and vectors, Equation 6.14, where V_{line} and Q are the line voltage and line charge vectors respectively

and P is the potential coefficient matrix. The line charges are determined by inverting the potential coefficient matrix, Equation 6.15. Once the line charges are determined, the electric field at point x is the vector sum of the electric fields from all wires including the image wires, Equation 6.16.

$$\mathbf{V}_{line} = \mathbf{PQ} \tag{6.14}$$

$$\mathbf{Q} = \mathbf{P}^{-1}\mathbf{V}_{line} \tag{6.15}$$

$$\mathbf{E}_x = \sum_n \frac{Q_n}{2\pi\epsilon\mathbf{r}_{nx}} \tag{6.16}$$
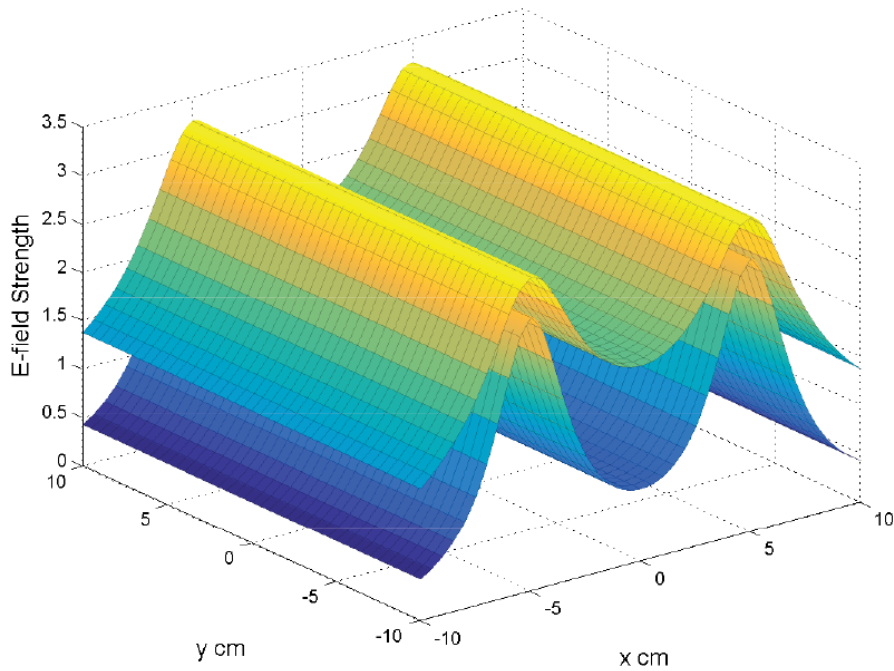
Figure 42: Electric field distributions of two wires 10 cm apart and 2 cm above a ground plane using multi-wire calculation (top) and the sum of the independent fields (bottom).

These equations were simulated with MATLAB to visualize the field strengths. The simulations covered a 20 cm×20 cm area in which two wires were separated 10 cm apart from each other. The wires were 0.1 cm thick and energized with 10 V. When wires are relatively far apart, the diagonal of the charge coefficient matrix is dominant. In this case, it is a reasonable approximation to treat the wires independently such that the total electric field is the independent average sum of the electric fields from each wire, especially in areas local to the peaks and when finding general shape to detect wires, Figure 42.

6.2.2   Simulation Results

The setup was modeled in ANSYS Maxwell 15.0.0, Figure 43, to verify the behavior of the electric fields. The electric field strength was consistent with the analytic model as the
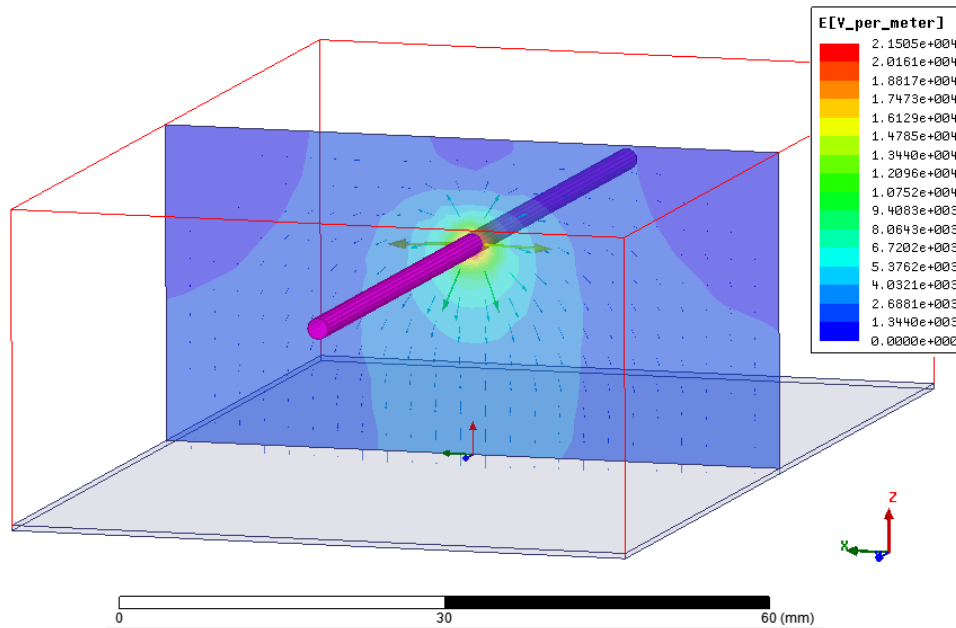
Figure 43: A cross-sectional electric field vector field and magnitude heatmap of a wire over a ground plane modeled in ANSYS Maxwell 15.0.0.

77

strength was greatest directly under the wire and tapered off in accordance to Equation 6.9 with a single wire.

Furthermore, simulations strongly suggested it was a reasonable estimation that multiple wires could be treated independently so as to sum the electric fields to find a net charge distribution, even more so than the more detailed multiple wire derivation, Figure 44. The simulation results are further supported by experimental measurements, covered in the following chapters.
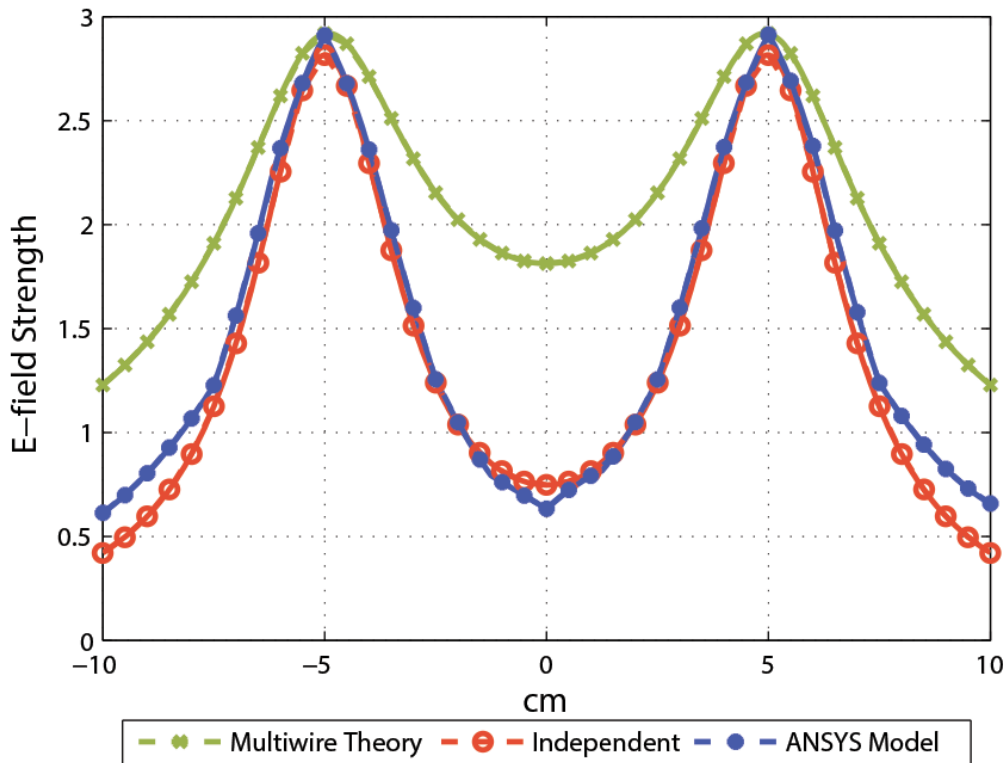
Figure 44: Comparison of cross-sectional electric field strengths when using the multiwire theory, independence assumption approximation, and ANSYS Maxwell 15.0.0 simulations.

6.2.3 Static Electric Fields

It is worth noting that D-dot sensors do not detect static electric fields because once the charge is established on the upper plate, no further current flows through the feedback resistor. Thus, no further voltage appears at the operational amplifier output. Mechanical approaches have been explored to distort electric flux lines by fluctuating the distance between the source and the sensor with devices such as MEMS [33]. An alternative method is spinning grounded blade rotating at a reference frequency to "chop" the electric field [59].

The principles of both of these methods were utilized to fashion a DC field imaging setup. To chop the field, a grounded blade was spun using an optical chopper. To distort the field by fluctuating height, D-dots were placed a solenoid. However, these methods will not be covered in detail in this manuscript since such bench tests required high-precision equipment that was not available during the course of this research.

6.3   The Big Picture

The objective of this research was to image electric fields. Taking advantage of the fact that the signal strength is proportional to the field strength and that the field is non-uniformly distributed, we implement an array of D-dot sensors, each sensor producing a signal proportional to the electric field strength in that position. The array was fabricated on both PCB and a flexible polyethylene naphthalate substrate, the latter which utilizes the same InGaZnO TFT process used in the neutron detection system from Part I.

Chapter 7

THE 1-DIMENSIONAL D-DOT ARRAY

This chapter covers the one-dimensional D-dot array that was fabricated as an initial proof of concept. The array was fabricated as a PCB and proved it would be possible to detect the different electric field strengths in space. Results were also used to verify calculations and simulations.

7.1   Board Layout

The original two layer PCB design was initially intended to be used as a two-dimensional 3×16 pixel array, Figure 45. The top layer consisted of 1 cm×1 cm metal pads, i.e. pixels, which were connected to a footprint designated for an access transistor. The transistor was intended for the two-dimensional architecture, covered in the following chapter, but for the initial run, the read lines were connected directly to the pads.

We decided to forgo the transistors for the initial run because the transistors chosen were in an ultra-small footprint package, so as to reduce the gap between pixels, and required time consuming third-party assembly. Since it was not very scalable to connect all of the pixels to
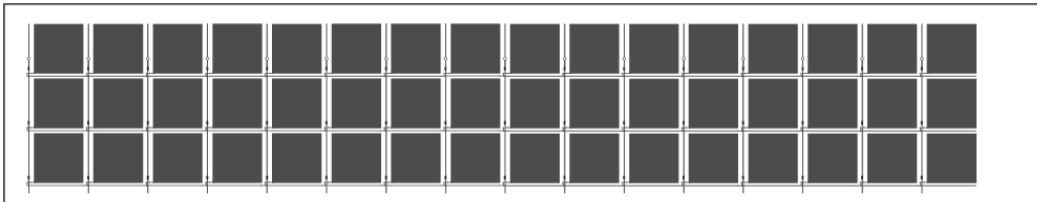
Figure 45: Original layout of a two-dimensional D-dot sensor array fabricated on a two layer PCB.

their own slot in the multiplexer, only one row was connected for preliminary measurements, hence the one-dimensional array. Furthermore, as seen from simulation, the extra rows would only extend the cross-sectional measurement in the two parallel wire setup of interest, and so no new information would be gained from the extra rows.

7.2   Bench Test Setup

Given that calculations and simulations run thus far were of cross-sections of parallel wires, a one-dimensional array measurement would be ideal for comparison. The wires were fashioned inside a plastic box 5 cm apart from one another and 2 cm above the array. The way the box was placed over the array, the wires were approximately above pixels 7 and 11 when counting from left to right.

Despite there being three rows on the board, only the top row was connected for readout. The pads were directly soldered to the unshielded read lines which were then connected to their respective channels in the Agilent 34921A Multiplexer module. The multiplexer was operated manually through the Agilent 34980A Multifunction Switch/Measure unit, though automation was in the works.

The output of the multiplexer was then fed into a low-noise transimpedance amplifier (DLPCA 200) which was then fed into a lock-in amplifier (Stanford SR830) via a coaxial cable. The reference signal for the lock-in amplifier was taken from the signal generator that also drove the wires. A diagram of the full setup can be seen in Figure 46 and photographs of the final setup can be seen in Figure 47.

The wires were energized with 20 V_{pp} AC signal. Some measurements were run at 97 Hz while others were at 970 Hz. These frequencies were chosen because 97 is a prime and is unlikely to interfere with ambient noise while 970 is an easy to calculate multiple of 97, allowing quick verification of theoretical calculations, namely that the signal strength is directly proportional to the frequency. They are also within or near the VLF range allowing the signal to easily penetrate the plastic container.

81
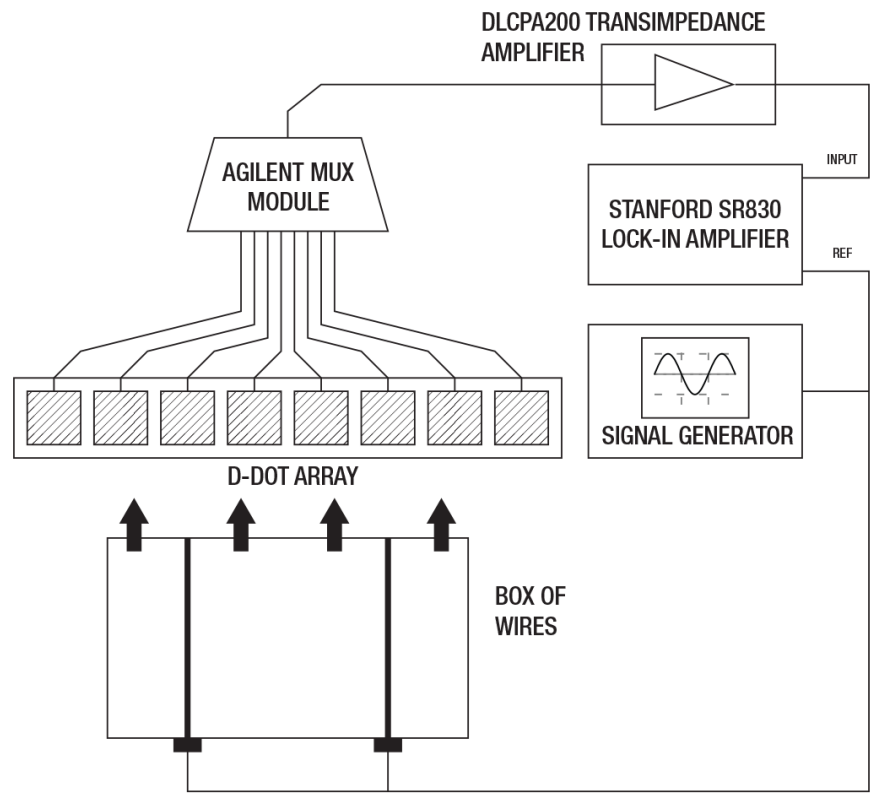
Figure 46: Diagram of the one-dimensional array testbench.
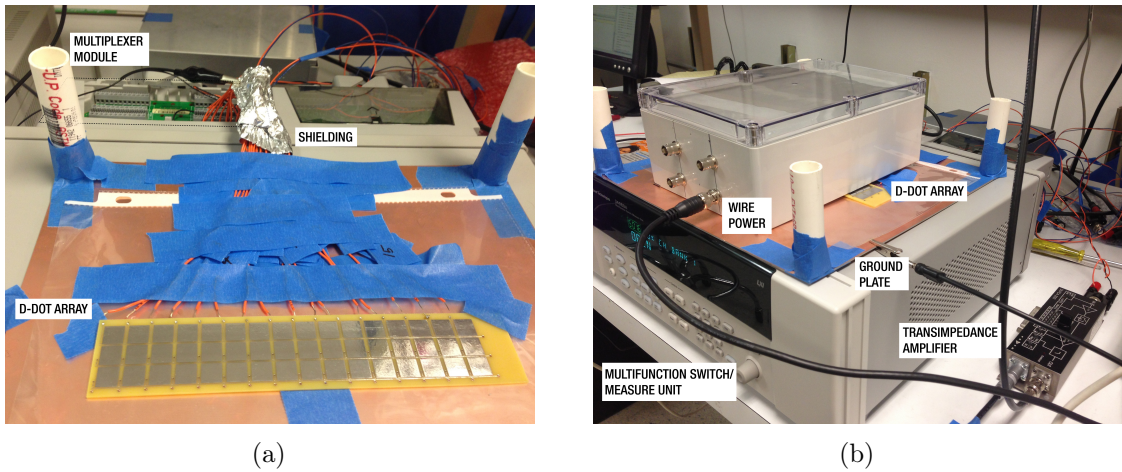
Figure 47: (a) Close-up photo of the D-dot sensor array in a one-dimensional configuration. (b) Photo of array with active wires and amplifying/readout circuitry.

7.2.1   The Lock-in Amplifier

At a high level, the lock-in amplifier takes the signal from the multiplexer and demodulates it to DC by multiplying the signal with a reference at the same frequency and its quadrature. It is then passed through a low-pass filter (within a bandwidth of one to a few Hz) to extract the signal strength with a DC voltage. This method dramatically reduces noise bandwidth and increases the probability of detection of very weak signals.

To better understand the mechanism behind the lock-in amplifier, we will first look at a single-channel lock-in amplifier, Figure 48. The two input signals, Equations 7.1 and 7.2, are multiplied together by the mixer, Equation 7.3. In the mixed signal, there are two components. The first component is at a frequency of zero (DC) while the other is at twice the reference frequency. The low-pass filter will then remove the latter term leaving Equation 7.4.

$$V_S = K \cos(2\pi ft + \phi_S) \tag{7.1}$$

$$V_R = \cos(2\pi ft + \phi_R) \tag{7.2}$$

$$V_M = K \cos(2\pi ft + \phi_S) \cos(2\pi ft + \phi_R) \tag{7.3}$$

$$= \frac{1}{2} Kg[\cos(\phi_S - \phi_R) + \cos(2\pi 2ft + \phi_S + \phi_R)]$$

$$V_{out} = \frac{1}{2} Kg \cos(\phi_S - \phi_R) \tag{7.4}$$

The output, Equation 7.4, is proportional to the signal amplitude, K. This is also under the assumption that the reference and the input signal are perfectly in phase, i.e. $\phi_S = \phi_R$. However, this is hardly ever a safe assumption to make. To address the phase shift, robust lock-in amplifiers utilize two mixers. One mixes the signal with the reference while the other
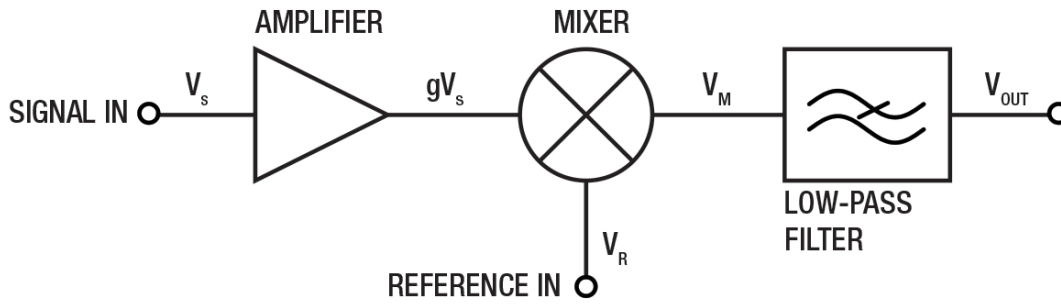
Figure 48: Diagram of simplified lock-in amplifier.
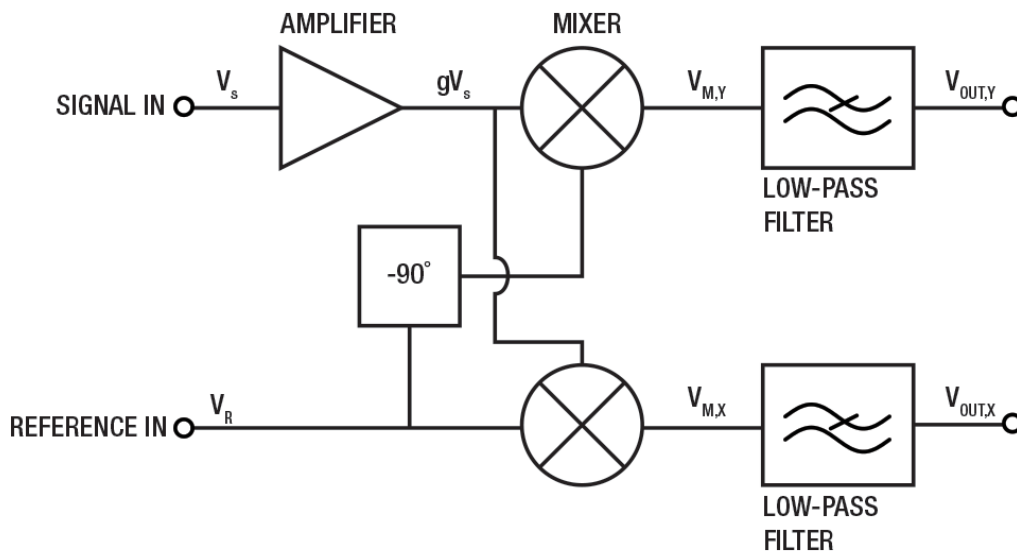
Figure 49: Diagram of simplified dual lock-in amplifier.

mixes the signal with the quadrature of the reference, i.e. the reference signal with a 90 degree phase shift.

Following a similar derivation, the two outputs become Equations 7.5 and 7.6. Taking advantage of the trigonometric property $(\sin^2 + \cos^2 = 1)$, both of the outputs can be squared, summed, and square rooted to get Equation 7.7, which will always be proportional to the strength of the signal of interest regardless of phase shift.

$$V_{out,X} = \frac{1}{2}Kg\cos(\phi_S - \phi_R) \tag{7.5}$$

$$V_{out,Y} = \frac{1}{2}Kg\sin(\phi_S - \phi_R) \tag{7.6}$$

$$V_{out} = \sqrt{V_{out,X}^2 + V_{out,Y}^2} = \frac{1}{2}Kg \tag{7.7}$$
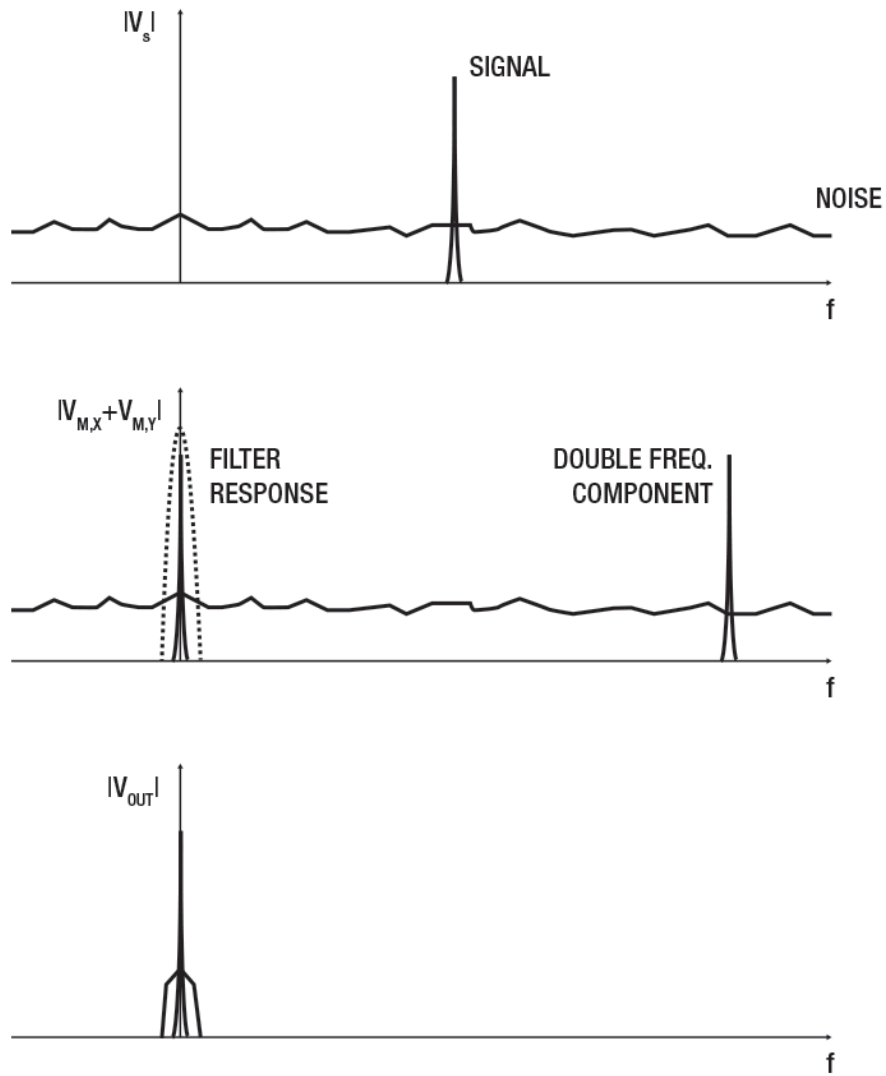
Figure 50: Diagram showing the spectra of various signals at different stages of the lock-in amplifier.

The low-pass filter not only retrieves the signal of interest, it also removes a lot of unwanted noise in the process. Observing Figure 50, the low-pass filter is able to effectively remove any noise outside the bandwidth of the filter. If spikes other than the double frequency component were present, they would otherwise dramatically distort the signal without the low-pass filter. These concepts are important to know since future designs plan to integrate the lock-in amplifier directly onto the imaging board.

7.3   Experimental Results

The resulting curves from the first set of experiments were far from the expected output, Figure 51. However, there was a high level of confidence that the fields were being measured since there were slight resemblance of peaks where it was expected and that the signal was almost exactly 10 times greater when using a 970 Hz signal versus a 97 Hz signal.

Similarly, the signal would reduce in half if the voltage was lowered from 20 V to 10 V. Futhermore, the experiment was highly repeatable given that the setup was not disturbed. It lead to the conclusion that array was simply very sensitive and was picking up unanticipated electric fields.

7.3.1   Correlated Double Sampling

To eliminate any potential noise outside from outside of the imager, the measurements were repeated with and without the D-dot sensor array. By taking the difference, only the signal directly measured from the imaging array would remain. This concept was inspired by the principles of correlated double sampling.

Since the presence of the imager itself can distort the electric fields, it was necessary to find a way to disconnect the pixels from the rest of the setup while moving as few components
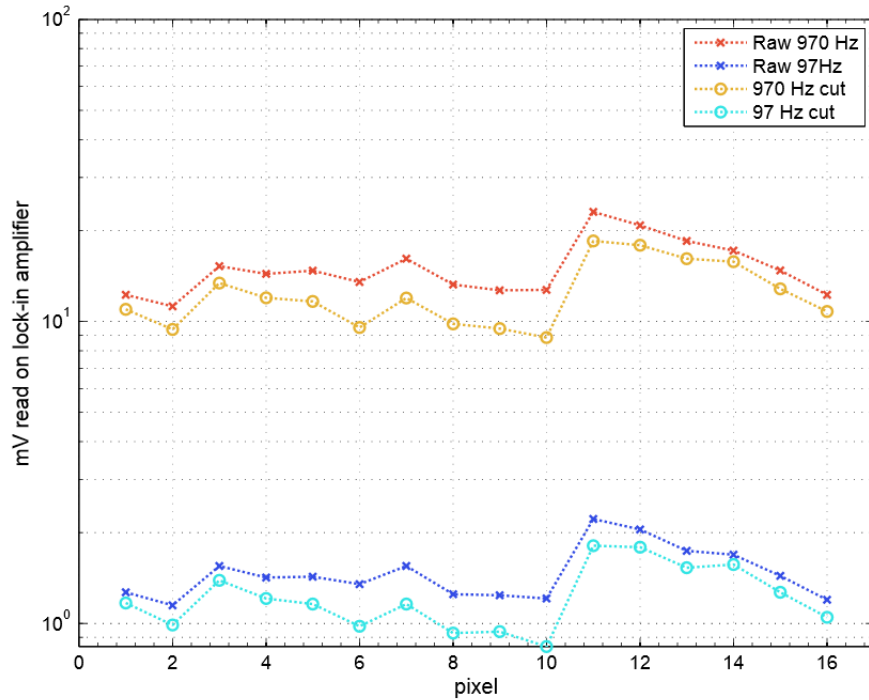
Figure 51: Plot of initial raw data (seen with the 'x' markers) along with the array output after the readlines were cute (seen with 'o' markers).

as possible. To achieve this, the read lines were physically cut near the pixels. Measurements were then repeated in the same manner.

The measurements after the wires were cut can be seen in Figure 51 and the output after correlated double sampling can be seen in Figure 52. It can clearly be seen that there is some offset that is collected by components outside of the D-dot array. The signal directly collected from the imaging array, however, correspond very closely to the theoretical model, demonstrated by the clearly resolved wires.

It was concluded that substantial parasitic signals were obtained from the wires connecting the pixels with the multiplexer. Since the wires were unshielded, the signal from the wires would capacitively couple into the read lines which could also distort the signal read at the imaging array. Further noise could also be from the wire between the multiplexer and transimpedance amplifier and possibly within the multiplexer box itself.
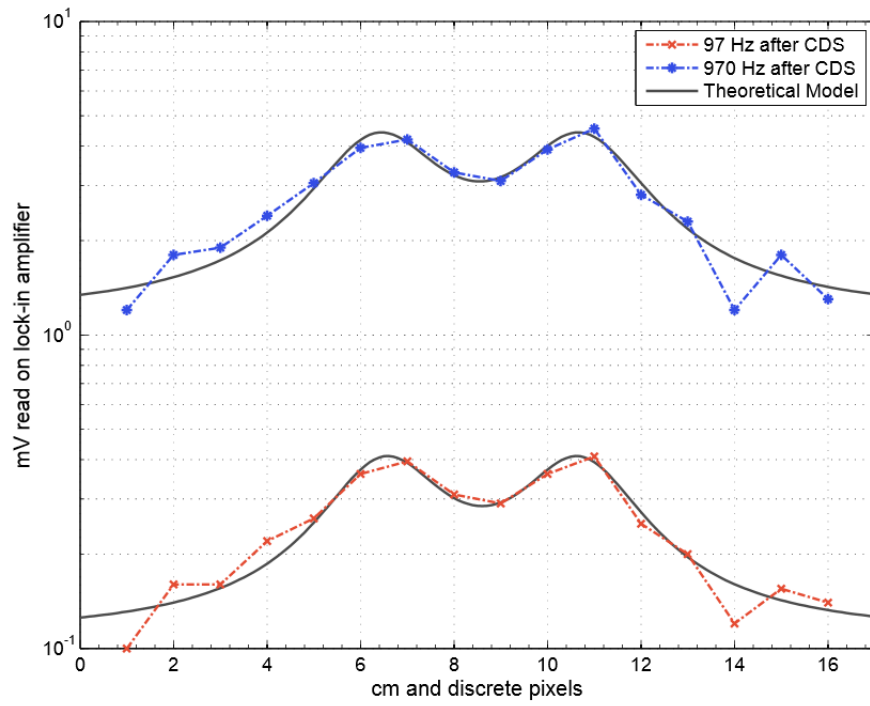
Figure 52: Plot of measurements after correlated double sampling compared to the theoretical model.

Chapter 8

THE 2-DIMENSIONAL D-DOT ARRAY

This chapter covers the two-dimensional electric field imaging architecture. It will first cover the mechanism behind the access transistor and go through the designs of both a flexible and rigid imager. The experimental results will also be discussed.

8.1 The Access Transistor

Each D-dot sensor in the two-dimensional array had an associated access transistor in order to read iteratively through all of the pixels with the corresponding driver. The access transistor functioned in a manner similar to DRAM architecture, Figure 53. The gate of the transistor was connected to a ROW line in which all of the D-dot sensors in the row were activated. The sensor was connected to the source of the transistor and the drain was connected to COLUMN lines which were fed into the transimpedance amplifiers and multiplexed to the lock-in amplifier.
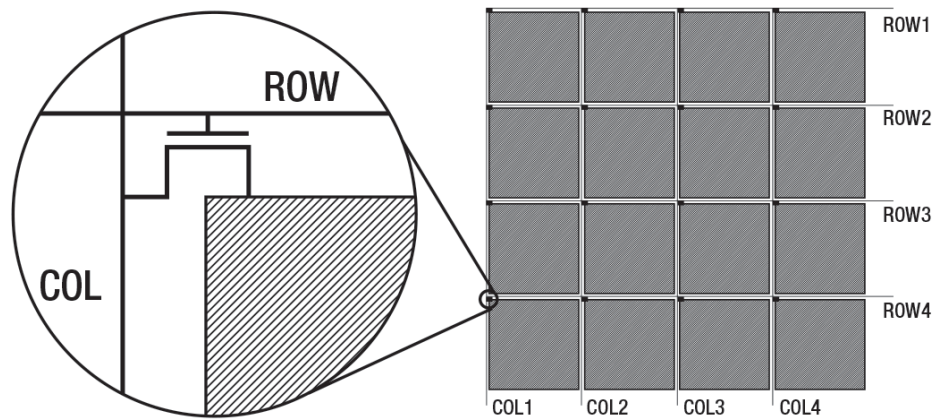
Figure 53: Diagram of the access transistor architecture in a 2-D imaging array.

8.2 Dedicated Transimpedance Amplifiers

The DLPCA200 low-noise transimpedance amplifier was replaced with LMC6001 operational amplifiers which were connected at the end of each column. A 10-20 MΩ feedback resistor was used to operate the operational amplifier in a transimpedance configuration. The smaller amplifiers were used at each column so as to reduce the noise seen by the read lines in the one-dimensional array. However, since the signal strength is very small, it was imperative that the amplifiers chosen had ultra low noise and input current, which the LMC6001 was capable of achieving.

The output of the amplifier is not greatly affected by outside noise sources because it is simply responsive to the activity seen by the virtual ground at the input. Therefore, by having the signals from the pixels physically travel a distance as short as possible to the virtual ground, there should be a dramatic reduction in coupling of extraneous noise. This conjecture was upheld with experimental results and the design practice was carried out with all subsequent imaging setups, rendering correlated double sampling unnecessary.

8.3 Flexible TFT Array

The motivation to develop a fully flexible imaging array is portable imaging in the field with a versatile form factor [36]. An active matrix 4×4 pixel array of 1 cm^2 metallic plates was fabricated on a flexible substrate, polyethylene napthalate (PEN) to demonstrate the concept. The access transistors are amorphous InGaZnO TFTs with a mobility of ∼20 cm^2/Vs. This was the same process 3-level metal, thin-film integrated circuit process used in the APS circuits in the neutron detection project and the flexible displays at FEDC [60].

8.3.1   Bench Test Setup

Many aspects of the bench test were very similar, if not identical, to the one-dimensional array bench test. Again the two frequencies of interest were 97 Hz and 970 Hz. The voltages used, however, were lower in the 1-10 V_{pp} range. Lower voltages were used because a thin wire was used and placed directly over the sensors to accommodate the smaller array size and lower resolution. Additionally, the aforementioned LMC6001 operational amplifiers were used. The signals were once again fed into the Agilent 34921A Multiplexer module and then fed into the lock-in amplifier.

The main difference in terms of operation was the use of the access transistors. When 10 V is applied to the gate to turn the transistor on, the channel resistance is approximately 100 kΩ. Negative 5 V is applied to completely turn off the transistor in which the off-resistance is approximately $10^{13}\Omega$ with a corresponding leakage current in the range of pA. Asserting a row in the array connects the D-dot sensors in that row to the columns where transimpedance amplifiers at the base of the columns amplify the current signals.

8.3.2   Experimental Results

A wide range of wire formations were tested with this array. This section will provide a shortened sample of results, for the sake of brevity, to exhibit the key findings during the course of the experiments. the first of the wire formations provided in a diagonal fashion over two columns of the array, Figure 54. The goal was to see the response and ensure that pixels with no wire above them would produce little to no signal at the output.

The sensitivity of the D-dot sensor was once again recognized as it was capable of picking up even slight deviations in the height of the wire from the array. Though a coarse image due to the high quantization error from the relatively large pixel size, Figure 54 shows how
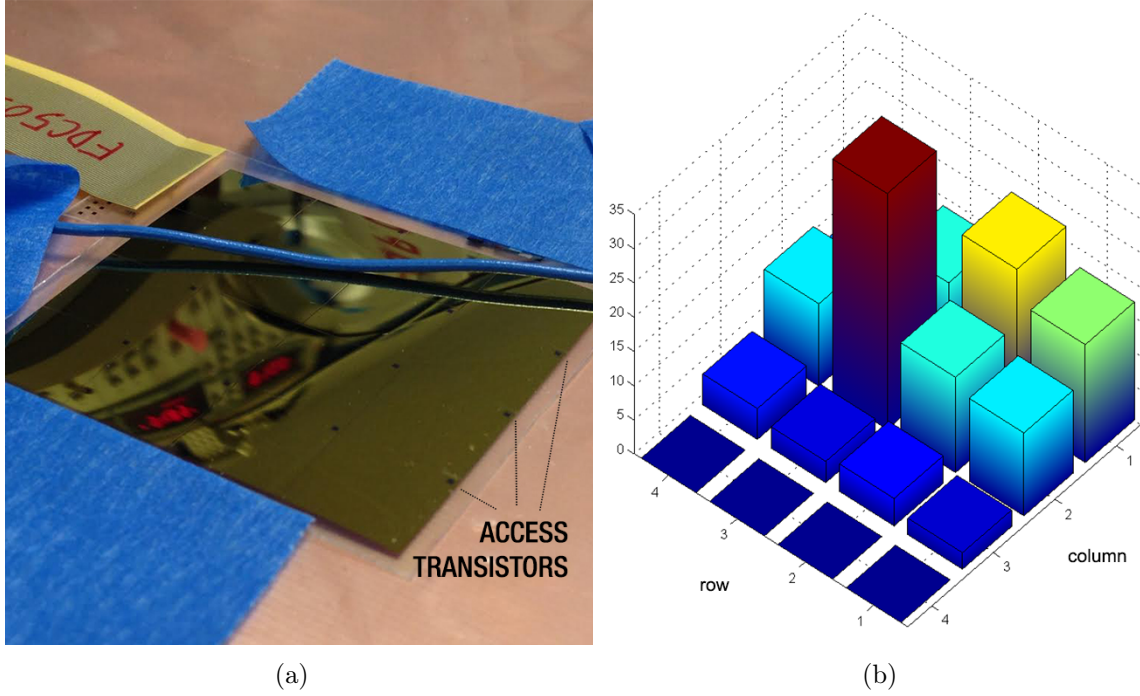
Figure 54: (a) Close-up photo of experimental setup of flexible imager emphasizing small deviation in the height of the wire carrying 10 V_{pp} at 970 Hz. (b) Histogram of corresponding output voltages.

only the pixels underneath the wire have the greatest signal strength with nearby pixels possibly collecting fringing fields.

Furthermore, the close up photo explains the disparity in signal strength such as the spike on row 3, column 2 where the wire is ∼1 mm closer to the sensor than the rest of the wire. Disparities could also be accounted for the total length of wire that is covered by each pixel as it is not uniformly distributed. There is also the possible issue of pixel to pixel offset errors due to process variations, an issue that was also seen in the APS circuits for the neutron detection project.

Stranded wire was also tested as opposed to a solid core because it was more flexible and could more easily be laid flat over the array. Figure 55 displays an experimental run of a stranded wire over column 3 where a much more uniform reading is seen. The wire, however, could not be laid perfectly flat and may explain the kink seen in the third row. The

92
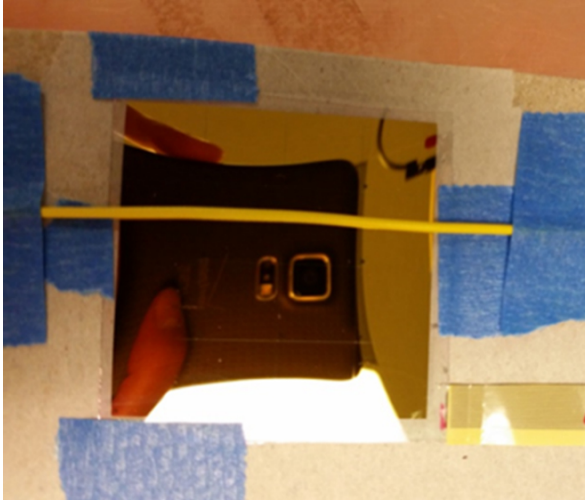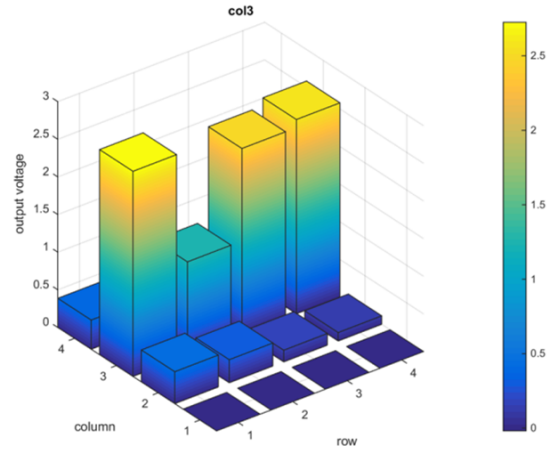
Figure 55: (a) Close-up photo of experimental setup of flexible imager with a wire carrying 2.5 V_{pp} at 970 Hz over column 3. (b) Histogram of corresponding output voltages.

discrepancy may also be explained by pixel to pixel offset errors, seeing how the difference is quite large. Nonetheless, as a proof of concept, there is promising potential that such an imager can be implemented in a flexible form factor.

8.4   PCB Array

In order to create an easily accessible, large-area imaging area, a similar approach was also done on a PCB with a 6×16 array of 1 cm^2×1 cm^2 pixels. To keep the pixels tight together, the Texas Instruments N-Channel FemtoFET (CSD13381F4) was used to take advantage of its ultra-small footprint.

8.4.1   Bench Test Setup

The bench test for the two-dimensional PCB array was even closer to the one-dimensional PCB array than the TFT counterpart. Once again, the 16-gauge wire was used to take

advantage of the larger area, and the wires were energized with 97 and 970 Hz signals at 10 and 20 V_{pp}. The two wires were 5 cm apart and 2 cm from the sensing array.

The two main notable differences include the use of the LMC6001 operational amplifiers, as previous described, and the use of the CSD13381F4 transistors. To operate the transistors, the Agilent 34951A Digital to Analog module was used to turn on and off rows of transistors. Once a row was activated, each column was iteratively read through the multiplexer.

8.4.2 Experimental Results

The arrays were capable to image AC electric fields from the two wires without the need of correlated double sampling. The lock-in voltage is plotted as a function of pixel number and clearly shows two electric field peaks corresponding to the position of the wires, Figure 56. However, it was only capable of imaging in one dimension. The image in Figure 56 is obtained regardless of whether one row, or all rows or even no rows are activated. With our TFTs having an off-leakage current in the pA range , there was not an issue individually accessing pixels, but the commercial off the shelf transistors had a leakage current in the tens of nA range. This caused no row to be truly "off." Therefore, a readout from a column was the summation of the signals from all of the rows intersecting with said column.

With circuit simulation, the problem was determined to be the relatively low off-resistance of the commercial silicon access FETs. D-dot sensors form very high impedance nodes and AC current induced on the sensor either flows through the sensor capacitance to ground or through the access transistor to the amplifying electronics, whichever impedance is less. Therefore, the off-resistance of the access transistor must be much greater than the impedance of the sensor capacitance at the frequency of interest in order to isolate an "off" sensor pad.

With 1 cm^2 sensor pads on a standard PCB detecting at 97 Hz, the off-resistance of the access transistors must be much greater than 600 MΩ. The off-resistance of the commercial FETs measured to be only 2-4 MΩ explaining why we observed all rows of the array being
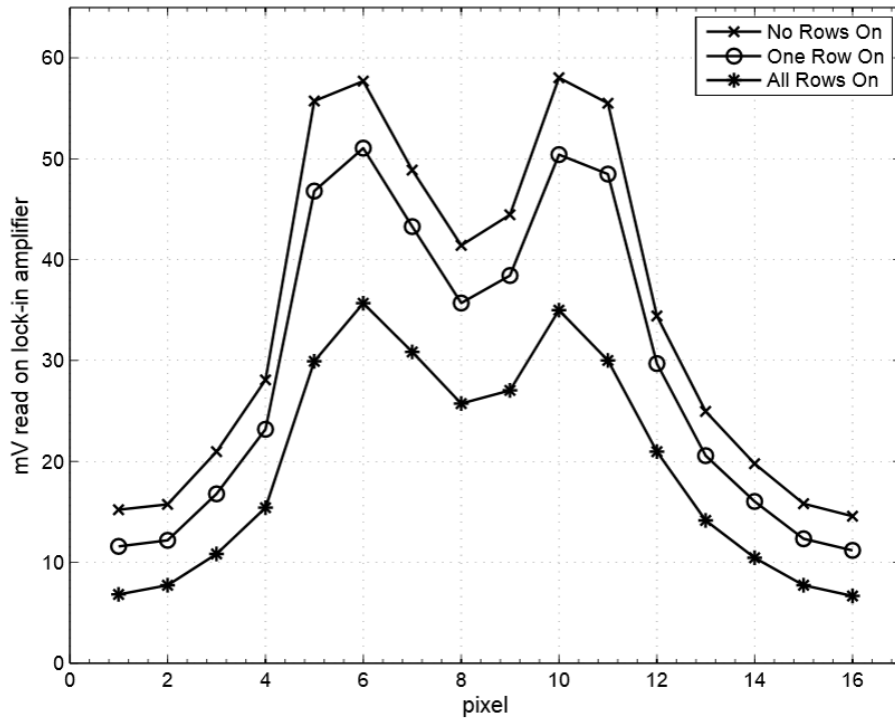
Figure 56: Electric field image obtained with the two-dimensional PCB array of two wires energized with a 97 Hz 20 V$_{pp}$ signal.

effectively on at all times. This required off-resistance is so high that it is unlikely that any single crystal semiconductor FET will be able to isolate a sensing pad from the array. Electromechanical switches that have an air gap in the off state might work, but we have not been able to find them in a sufficiently small package to surface mount on a two-dimensional array.

Finally, the data in Figure 56 is peculiar in that the signal is stronger with no rows on compared to all rows on which is counter-intuitive since more sensors connected to the amplifying electronics should result in a stronger signal. This result is still not fully understood, but it is hypothesized that it is due to the flux concentration on the column wires in the array when the sensor pads are connected through nominally off access transistors. Quasi-electrostatic simulations are needed to understand this phenomenon.

8.5 Remarks on 2-Dimensional Array

The D-dot sensor array on the flexible PEN substrate demonstrated potential to be a full imaging device. Such a device opens possibilities to unique applications such as flexible electric field imaging blankets and EEG/ECG wearable caps. Similar to the large-area neutron detector, the TFT-based array can leverage the cost-effective process of the display industry to make large panels for low cost. Unfortunately, we were unable to fabricate any more devices in-house at FEDC with very limited fabrication runs.

To continue the research of large-area electric field imaging, a PCB version was also fabricated due to its low cost and quick turnaround rate. Unfortunately, the active matrix layout was unsuccessful since no commercial off the shelf transistor with a small enough leakage current could be found, a problem the TFTs were capable of handling due to their very high off-resistance. Alternative methods were sought and are discussed in the following chapters. The pursuit for a full two-dimensional array is still very much alive, however, but integrating a surface mount operational amplifier directly to each pixel. The details of this design will be discussed in greater detail in Chapter 11.

Chapter 9

THE 1-DIMENSIONAL STEPPER ARRAY

This chapter covers the PCB one-dimensional stepper array used to address the issues of the leakage currents found in the access transistors of the two-dimensional array while managing to image large areas. The automated software driver written in MATLAB used to operate the imager is also discussed. This method was capable of clearly resolving electric fields from various wire formations, the results of which will be discussed.

9.1   Board Layout

Since the off-resistance of any single crystal commercial off the shelf transistor would not be sufficient to isolate the D-dot sensors, a "stepper" method was used in which a 16 pixel 1-D array was physically swept over the object of interest. The array was fabricated on a two layer PCB with 1 cm×1 cm pixels where each pixel was connected physically close to an LMC6001 operational amplifier, Figure 57.
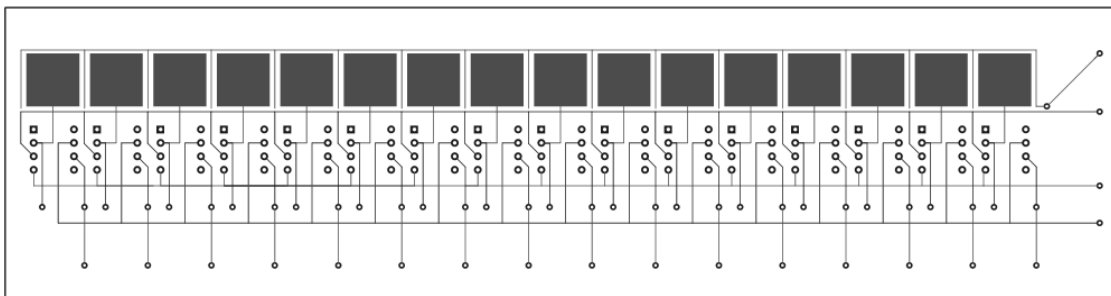
Figure 57: PCB layout of the 16×1 one-dimensional stepper array with 1 cm^2 pixels and independent operational amplifiers.
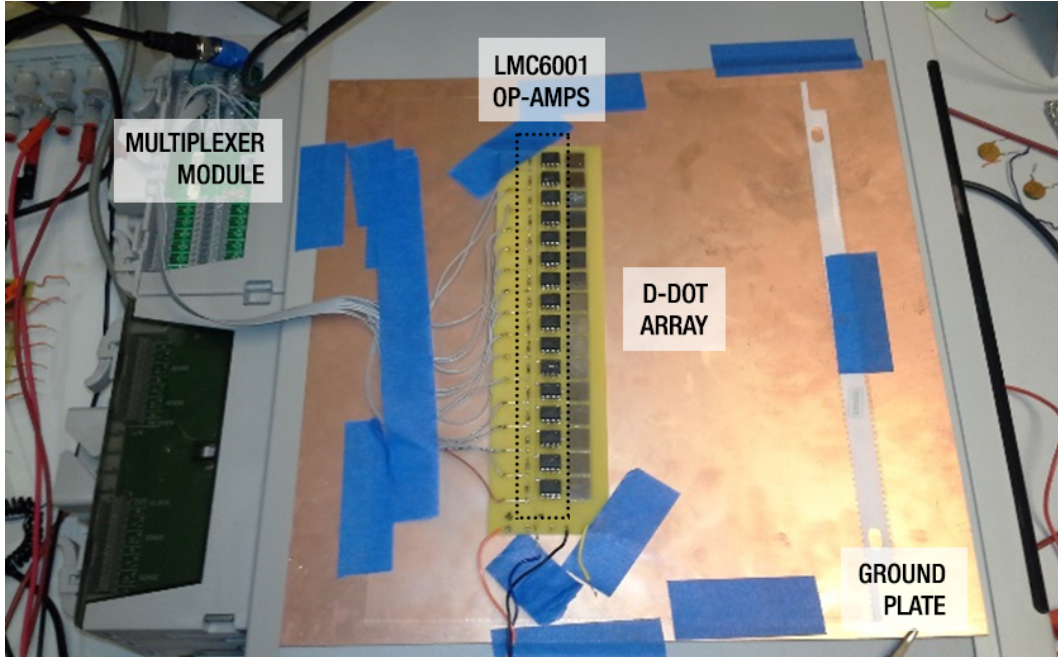
Figure 58: Photograph of the PCB stepper D-dot array.

A photograph of the actual array can be seen in Figure 58. For initial runs, the ground plate of the D-dot sensors was simply a large copper plate that was shorted to ground. A plastic insulating sheet was placed in between so as to not short any of the components.

9.2 Wires in a Box Experiment

To keep in line with previously conducted experiments, another set of measurements were made with wires in a concealed plastic box. The setup consisted of three 16-gauge wires separated by 5 cm from each other and placed 4 cm above the sensing array. The wires were placed and connected in a custom plastic box with BNC connectors for support and power. Additionally, the wires were constructed inside a plastic box to demonstrate they can be imaged through the container. Only the outer wires were charged with either a 97 or 970 Hz signal at 10 V_{pp}. An unenergized middle wire was included to prove the method images only energized wires.

(a)   (b)

Figure 59: (a) Setup 1: Experimental setup of a plastic box with 3 parallel wires. (b) Setup 2: similar setup but in which the top and bottom wires are connected with a jumper wire within the box.

Note: The central wire is floating in both configurations while the outer two are energized with a 10 V_{pp} 970 Hz signal.

Both a shielded and floating connecting wire were tested. The wire formation was then mechanically shifted over the one-dimensional array, which was fixed in position, at 1 cm increments to emulate a scanning wand. This was achieved by building a plastic elevated platform with engraved markings in a 0.5 cm grid[5]. Over the course of nine steps, the array yielded an image of 9 cm×16 cm.

9.2.1   Automation

The task of manually operating the Agilent 34980A Multifunction Switch/Measure unit and writing down the output values proved to be cumbersome and not scalable. In the 9×16 pixel images obtained, this process would requires nearly 150 steps of constant attention. To alleviate the task, a paradigm shift was established towards automation by using a National

---

[5]The platform was constructed by Steve Rednour, an engineer at FEDC.

Instruments Data Acquisition card to automatically record the output of the lock-in amplifier and store into a computer.

Custom software drivers were written in MATLAB[6] to communicate with both the data acquisition card and the Agilent 34980A. The full code can be found in the Appendix. The system could potentially be further automated by implementing a stepper motor which would shift the array.

9.2.2 Experimental Results

It is clear from the 3-D histogram of the lock-in output from Setup 1, Figure 59a, that the device is imaging the electric fields radiating from the two energized wires, Figure 60. The source resolution of the image is approximately 4 pixels, approximately 4 cm, and is roughly equal to the distance between the wires and the sensing array. The outlines of the box and wires are superimposed as a visual aid.

It can be seen that the electric field strength outside of the box is considerably weaker than the strength inside. Where the signal enters, there is almost no electric field signal because the incoming coaxial cable is grounded. The electric field strength outside of the box on the other end is non-trivial because the BNC connector was left open, allowing electric flux lines to leak out. Note that we also image portions of the coaxial cable with floating ground that connect the two wires on the bottom of the image.

A similar result, seen in Figure 61, is obtained from Setup 2, Figure 59b, in which the two wires were connected with an unshielded wire with alligator clips. All other factors were held constant including signal strength and frequency with 10 V_{pp} at 970 Hz and the distance from the array at 4 cm.

---

[6]The MATLAB driver was written in collaboration with my colleagues Weidong Ye and Sandeep Vora who at the time were in a senior design group at FEDC.
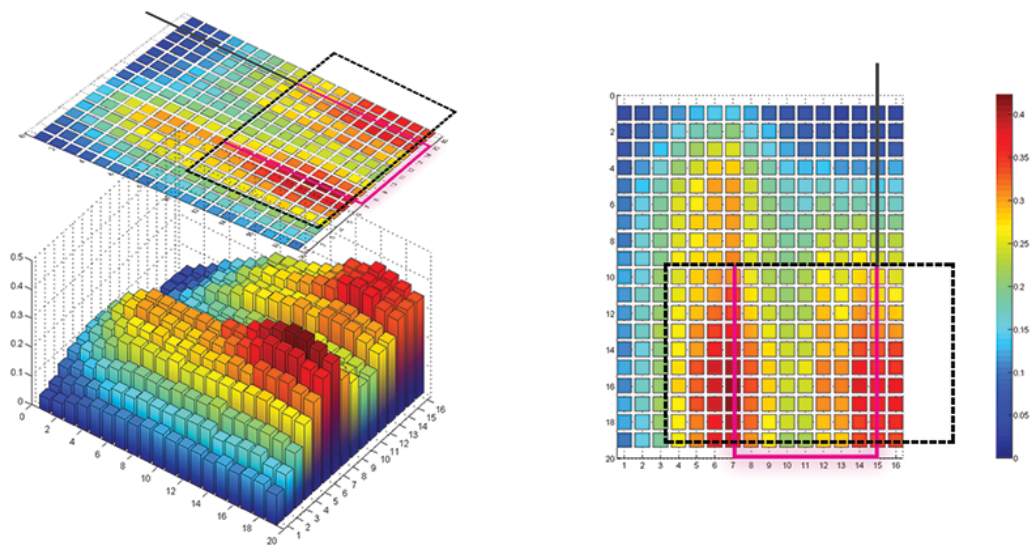
Figure 60: The electric field image for the box with a shielded connection. The outlines of the box and wires are superimposed in the angle view (left) to easily see the effect of the wires and 2-D heatmap is provided (right).
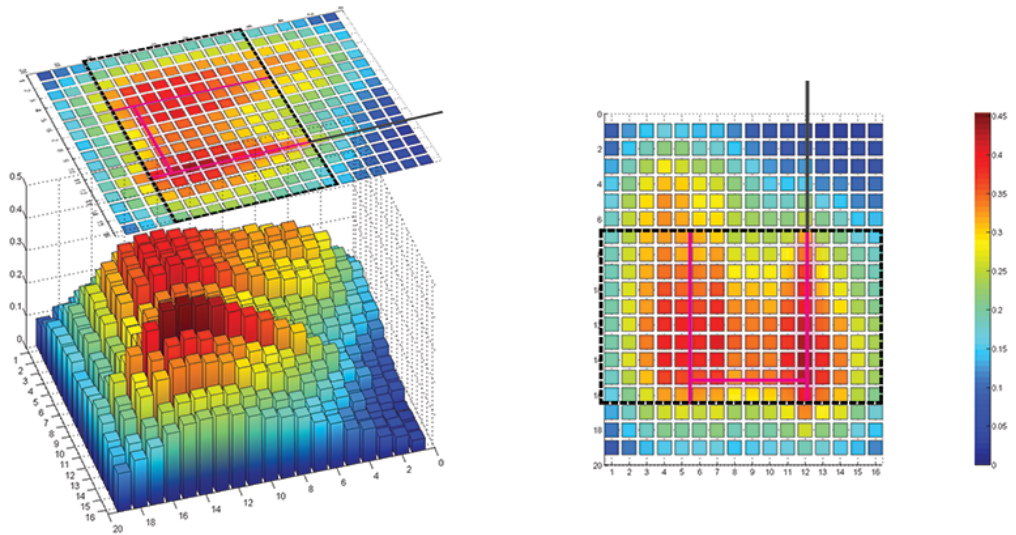
Figure 61: The electric field image for the box with a non-shielded connection at an angle view with images of the wires superimposed (left) and a 2-D heatmap from the top view (right).

Intrestingly, the strongest signal for the non-shielded jumper wire configuration comes from the bottom right in Figure 61. Upon inspecting the photo of the setup, Figure 59, the spike is due to the alligator clip extending a few millimeters below the wires, creating an increased capacitance to the sensing array. This again reflects on the accuracy and sensitivity of the imager.

9.3   Wires on Drywall

Another application of interest for this imager was for the ability to see power lines through walls, particularly at construction sites. To prove its feasibility, meandering wire formation was taped down onto a slab of drywall in accordance to the image seen in Figure 62. The frequencies tested were 97 and 970 Hz at voltages of 1, 3, and 9 V_{pp}. The wire hanging of the edge of the board was wrapped in aluminum foil and grounded in an effort to shield the portion of the wire that was not intended to be imaged.

There was also an interest to measure the wires at various heights for future reconstruction algorithms. The height was in units of drywall slabs (with an additional offset of 1 cm from the platform) in which each slab of drywall was approximately 1.5 cm. The measurements also provided insight in to the fringing effects based on height. We would expect less prominent peaks the further the object of interest is from the imager.

9.3.1   Experimental Results

Consistent with previous measurements, the signal strength was proportional to the voltage level and frequency. Knowing this, a small sample of results is provided to observe the effect of height. When the wires were 2.5 cm from the array, Figure 63, the electric field strength is relatively high. A large signal can also be seen where the wires are densely compact.
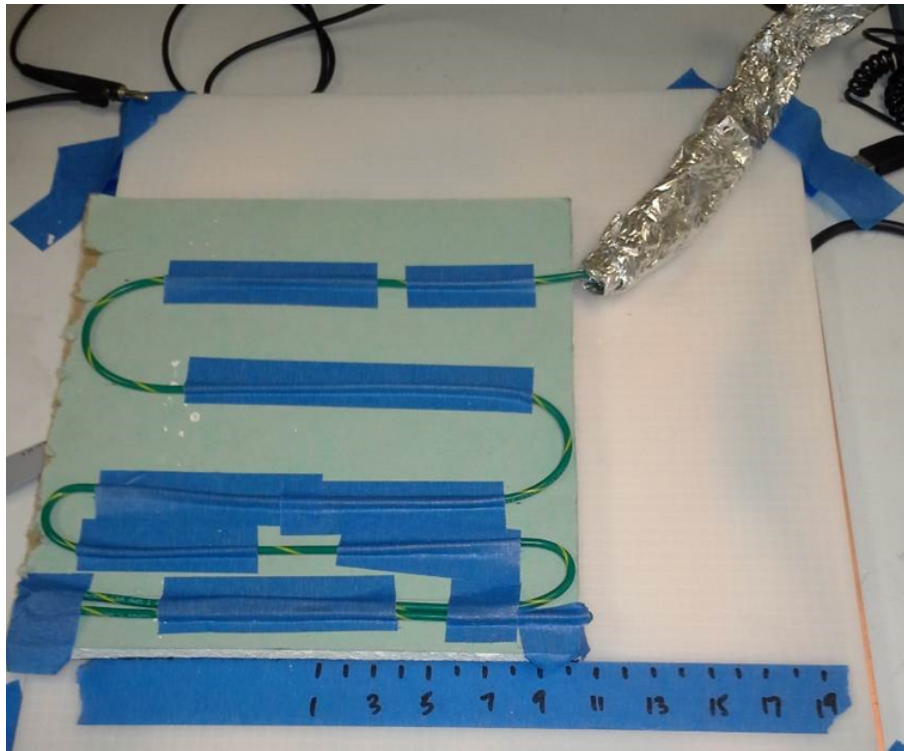
Figure 62: Photograph of the wire formation used on drywall.

When adding an additional 1.5 cm, Figure 64,the presence of the wires is still apparent though not resolved as clearly. Despite the colormap being the same, the value range is smaller. The electric fields can also not be as readily detected laterally, particularly in areas where the wires are not dense. The reconstruction algorithm in development uses the measurements by observing the spread of electric fields and extrapolate backwards to obtain additional information such as absolute height.
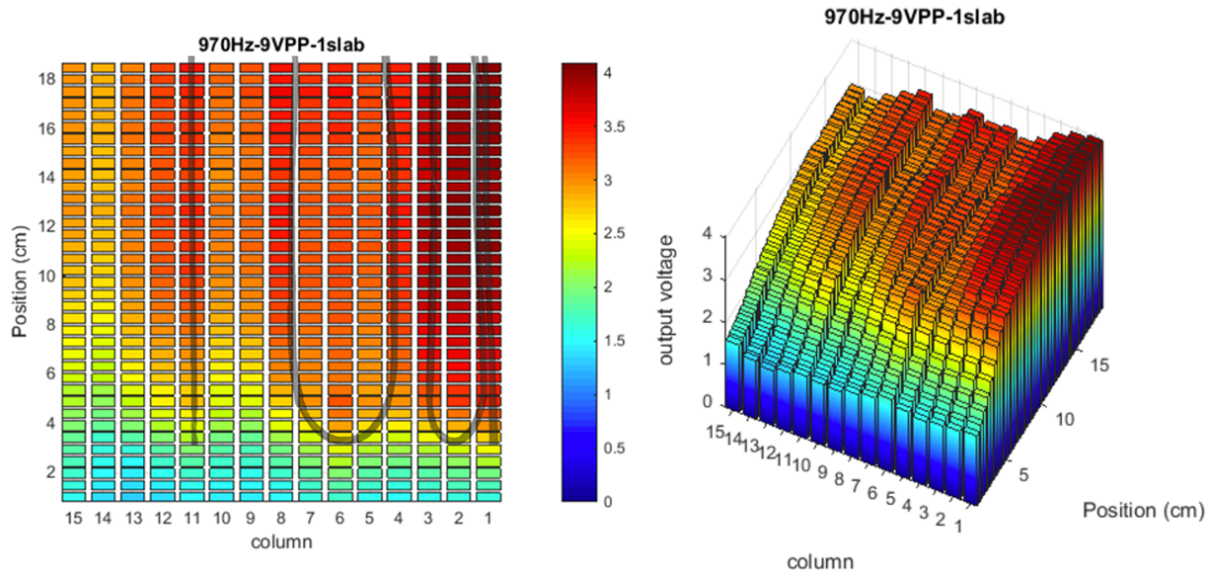
Figure 63: Electric field image of the meandering wire formation on one slab of drywall.

Source: These particular measurements were made by Weidong Ye and Sandeep Vora. The graphic was compiled by Anthony Wilson who was a summer intern at the FEDC.
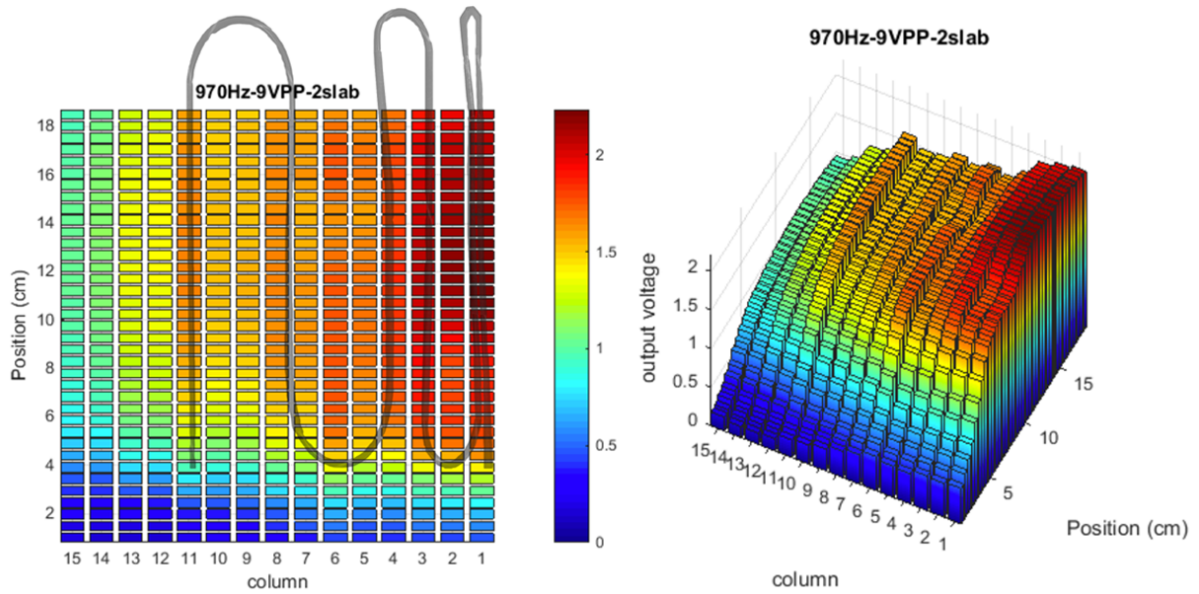
Figure 64: Electric field image of the wire formation on two slabs of drywall.

Source: These particular measurements were made by Weidong Ye and Sandeep Vora. The graphic was compiled by Anthony Wilson.

9.4 EMI Detection: Buck Converter

EMI is an expensive and ongoing issue that can severely degrade the performance of a circuit. The ability to detect EMI sources would help circuit designers find and rectify such portions of their design more efficiently. Power components are often susceptible to EMI due to the oscillating nature of operation. For openers, the one-dimensional stepper array was used to detect EMI from a 9 to 3 V DC to DC buck converter.

The buck converter was built around the Texas Instruments LM2576 simple switcher with a prominent electromagnetic emission. Though the chip operates at a switching frequency of 52 kHz, measurements with a spectrum analyzer revealed that it more closely operates at 50.25 kHz, Figure 67. Both a compact and expanded version, Figure 66, was constructed[7] to see if the imager could detect the buck converter in the compact configuration and see individual components in the expanded configuration. The full schematic used can be seen in Figure 65.
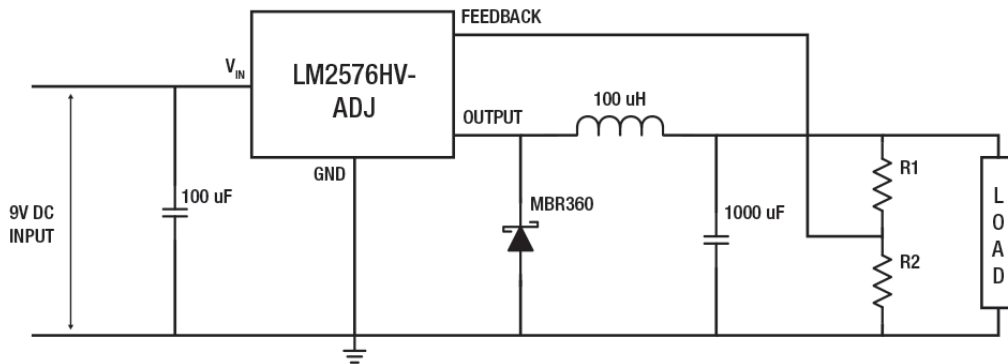
Figure 65: Schematic of the buck converter.

---

[7]Both boards were assembled by John Gorrie, Anthony Wilson, Matt Oman, and Clementina Reynolds who were undergraduate summer interns at FEDC
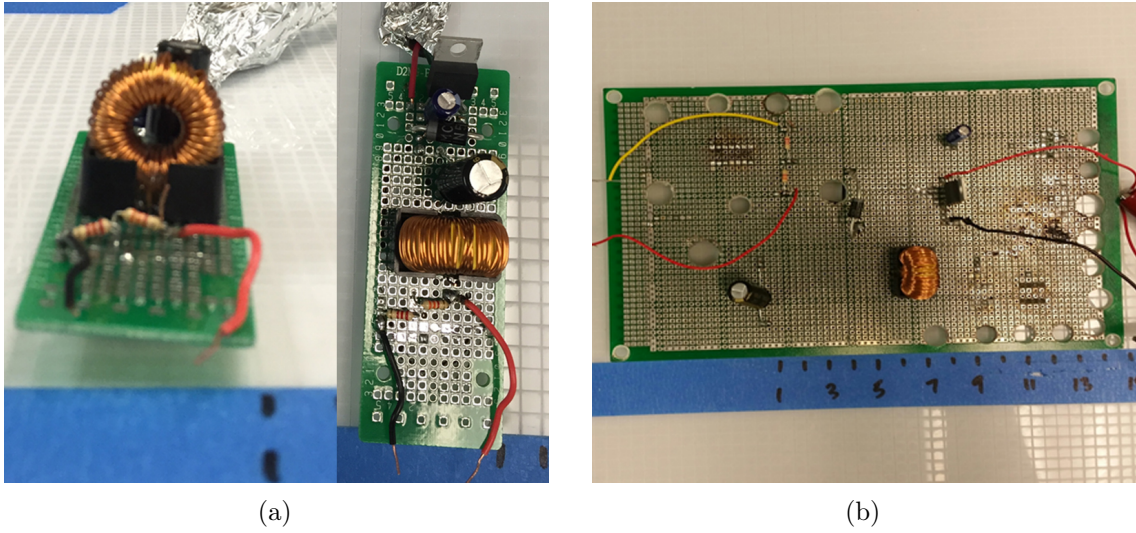
Figure 66: (a) Photograph of the compact buck converter at an angle (left) and top view (right). (b) Photograph of the expanded buck converter.
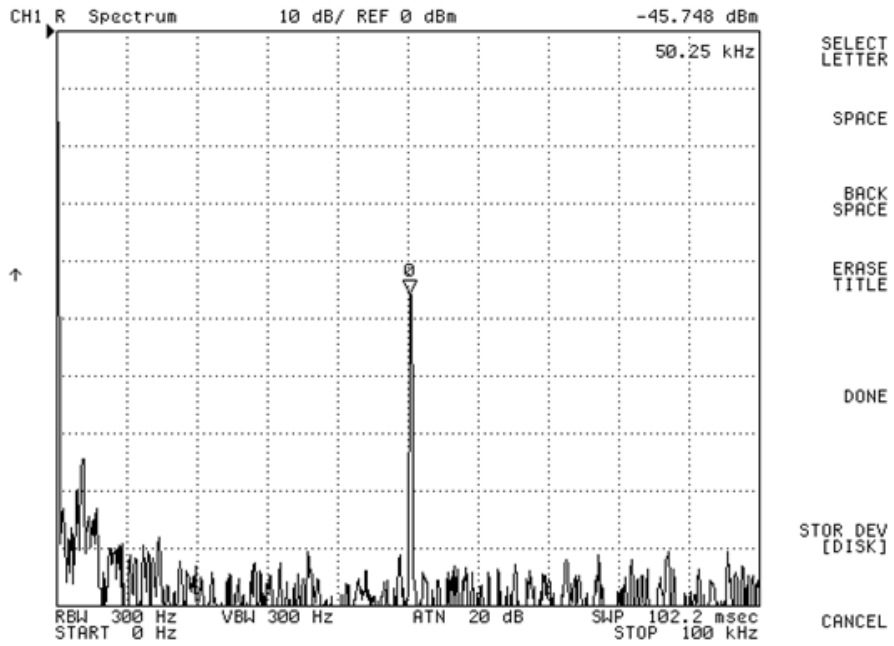
Figure 67: Frequency response of the buck converter output.

Source: These particular measurements were made by Anthony Wilson.
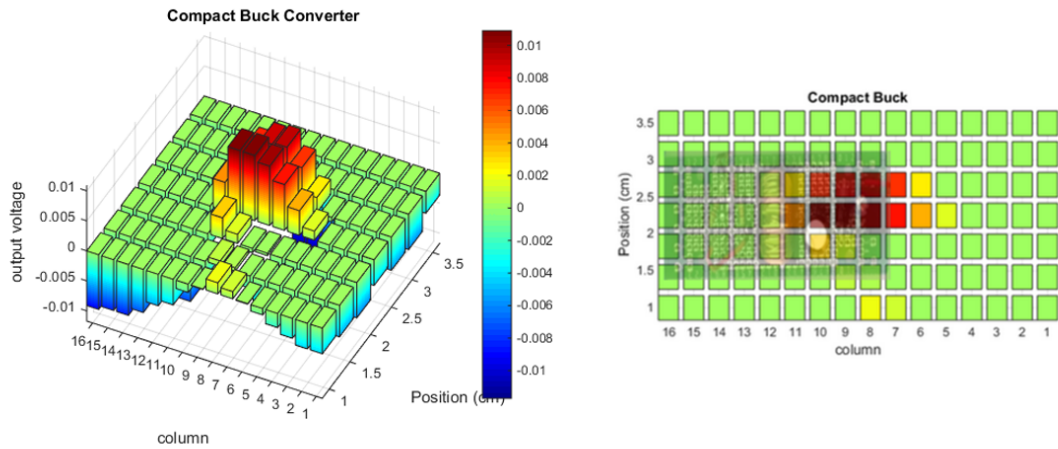
Figure 68: Electric field image of the compact buck converter (left) and birds-eye view with an overlay of the board (right).

Source: These particular measurements were made by the summer intern team of John Gorrie, Anthony Wilson, Matt Oman, and Clementina Reynolds.
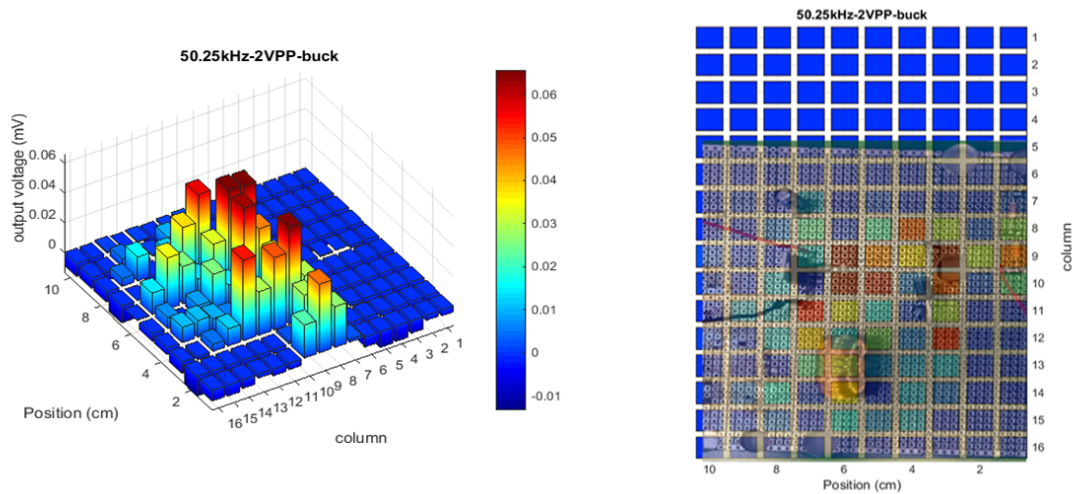
Figure 69: Electric field image of the expanded buck converter (left) and birds-eye view with an overlay of the board (right).

Source: These particular measurements were made by the summer intern team of John Gorrie, Anthony Wilson, Matt Oman, and Clementina Reynolds.

9.4.1 Experimental Results

It is evident from the images obtained, Figures 68-69, that the imager is capable of detecting EMI sources. Due to the coarse resolution, the imager is capable of detecting the compact buck converter but it is difficult to resolve individual components. With the expanded configuration, the imager managed to pick out individual sources, namely the switching unit, the output load, and the inductor. These measurements also demonstrate that we are capable of imaging AC signals without having direct access to the reference frequency. This is critical because the reference frequency will not always be available in real world applications.

Chapter 10

INVERSE IMAGING PROBLEMS

This chapter will cover inverse problems in imaging. The solution to an inverse problem is an underlying function for a given set of measurements. The underlying functions of interest had two implications: 1) the actual electric field strength, i.e. at infinite resolution, and 2) objects that were being imaged. An inverse problem would normally have to be well-posed, i.e. solutions are unique, a solution must exist for a given set of measurements, and solutions are stable [61]. Real applications, however, often violate these rules, particularly the uniqueness aspect. The goal here was to include additional information and develop robust algorithms to overcome these obstacles.

10.1   Computed Tomography

Computed Tomography (CT) is an algorithm most prominently used in X-Ray scans for medical imaging. The method takes multiple scans at incremental angles in a circular motion about the target and combines the data to reconstruct an image of the object. This method first sparked interest after the results seen in the original two-dimensional PCB D-dot array. Since all of the pixels in a given column were reading at the same time, the board in essence became an $1 \times N$ array of long parallel beams, much like X-ray beams in CT scans. Principles of CT were borrowed to develop and algorithm specific to our needs. First, the traditional CT procedure will be provided for background.

10.1.1   Radon Transform

The forward projection in tomography is known as the Radon Transform. For simplicity, we will discuss recovering a two-dimensional image from one-dimensional projections. Once

two dimensional projections are collected, it is simple to then recover a three-dimensional image from the same methodology. We will also, for openers, discuss specifically in the realms of X-Ray imaging in which the X-Rays are propagated in straight parallel lines.

$$p_\theta(r) = \int_{(\theta,t)line} f(x,y)ds \tag{10.1}$$

$$= \int_{-\infty}^{\infty} f(\mathbf{A}_\theta[r\ s]^T)ds \tag{10.2}$$

$$= \int_{-\infty}^{\infty} f(r\cos(\theta) - s\sin(\theta), r\sin(\theta) + s\cos(\theta))ds \tag{10.3}$$
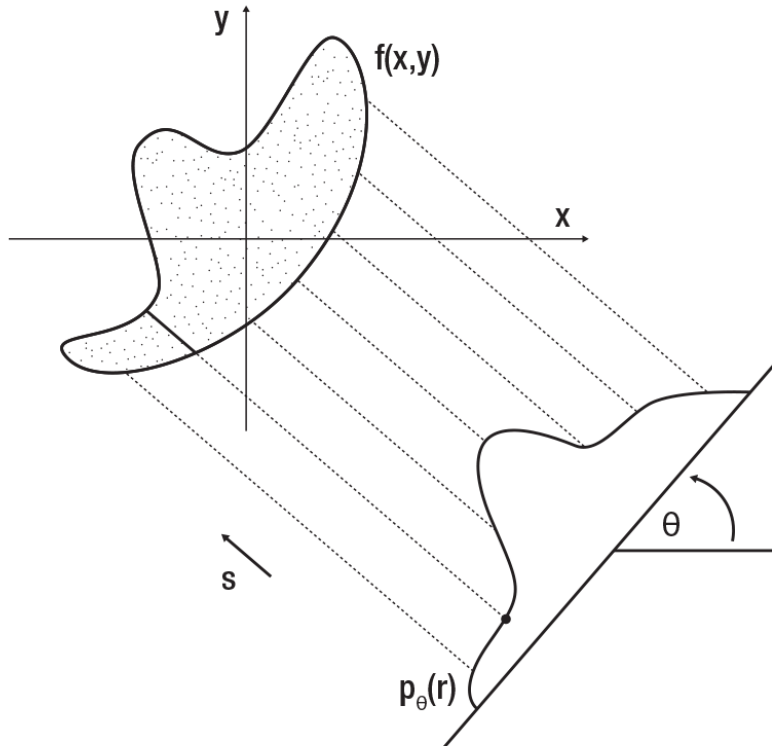
Figure 70: Geometric representation of the Radon Transform.

Projections are made about an object with density $f(x, y)$ at every specified angle θ and displacement r. The forward projection, $p_\theta(r)$ is known as the Radon Transform and can be explicitly written by Equation 10.3. The projection value is geometrically interpreted as the integral of the density function along the line orthogonal to the angle and intersecting with said point, Figure 70.

10.1.2   Fourier Slice Theorem

The Fourier Slice Theorem provides a mathematical basis to show the relationship between the Radon Transform and image reconstruction. The theorem posits that the Fourier transform of a projection, $p_\theta(r)$, is equal to the values along the two-dimensional Fourier transform of the density function, $f(x, y)$, at angle θ.

$$p_\theta(\rho) = CTFT\{p_\theta(r)\} \tag{10.4}$$

$$F(u, v) = CSFT\{f(x, y)\} \tag{10.5}$$

$$P_\theta(\rho) = F(\rho \cos(\theta), \rho \sin(\theta)) \tag{10.6}$$

The sample of the two-dimensional Fourier transform can be thought of as a "slice," hence the name. A summary of the theorem can be described by Equations 10.4-10.6. In the equations, CTFT and CSFT stands for Continuous Time and Continuous Space Fourier Transform respectively. Figure 71 provides a visual representation of what the Fourier Slice Theorem geometrically implies.

111
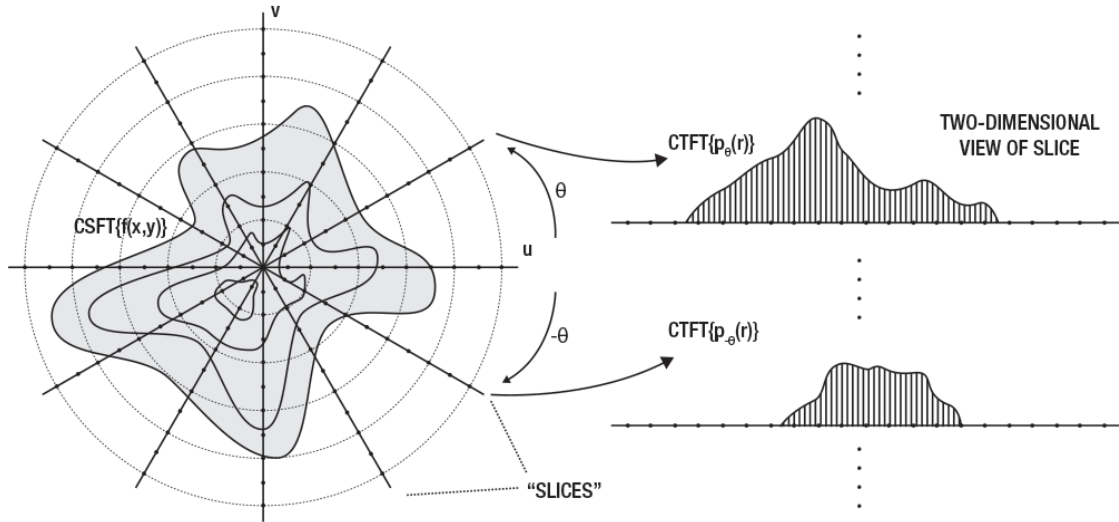
Figure 71: Geometric visualization of the Fourier Slice Theorem.

10.1.2.1 Proof

This proof of the Fourier Slice Theorem is a summary of the one provided by Kak and Slaney [62]. First, we will make a transformation of the coordinate system to better suit the various rotations each slice is in as follows:

$$
\begin{bmatrix} t \\ s \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta y \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} \tag{10.7}
$$

$$
S_\theta(\omega) = \int_{-\infty}^{\infty} P_\theta(t) e^{-2\pi i \omega t} dt \tag{10.8}
$$

$$
= \int_{-\infty}^{\infty} \left[\int_{-\infty}^{\infty} f(t,s) ds \right] e^{-2\pi i \omega t} dt \tag{10.9}
$$

$$
= \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} f(t,s) e^{-2\pi i \omega t} ds dt \tag{10.10}
$$

112

If the Fourier Transform of a projection is made using the alternative coordinate system, the equation above is determined. Already it is taking the form of the two-dimensional spacial Fourier Transform. By transforming the expression back to Cartesian coordinates, we get the following:

$$S_\theta(\omega) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} f(x,y) e^{-2\pi i \omega (x \cos\theta + y \sin\theta)} dx dy \tag{10.11}$$

$$= F(\omega, \theta) = F(\omega \cos\theta, \omega \sin\theta) \tag{10.12}$$

It can be seen how the Fourier Transform of a projection is a slice of the two-dimensional Fourier Transform of the original image. By the rotational property, with infinite rotations, we would obtain the full two-dimensional Fourier Transform. An inverse Fourier function can then be applied to recover the original image.

10.1.3   Convolution Back Projection

The Convolution Back Projection algorithm is a method to reconstruct the original image while borrowing concepts of the Fourier Slice Theorem. It is the reverse of projection, but it is not the inverse. This is important because finding the Inverse Fourier Transform of such large matrices while also interpolating between polar and Cartesian coordinates can prove to be very computationally expensive and impractical, so an iterative approach must be taken. A naive summary of Convolution Back Projection takes a set of projections, applies a filter to the projections, and then uses back projection to recover the original image. The theory is as follows.

$$f(x,y) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} F(u,v)e^{2\pi j(xu+yv)} \, dudv \tag{10.13}$$

$$= \int_{-\infty}^{\infty} \int_{-\infty}^{\pi} P_\theta(\rho)e^{2\pi j(x\rho\cos\theta + y\rho\sin\theta)}|\rho| \, d\theta d\rho \tag{10.14}$$

$$= \int_{-\infty}^{\pi} \left[\int_{-\infty}^{\infty} |\rho| P_\theta(\rho)e^{2\pi j\rho(x\cos\theta + y\sin\theta)} \, d\rho \right] d\theta \tag{10.15}$$

Assuming the two-dimensional Fourier Transform is given, to find the inverse in polar coordinate, the Jacobian of the polar coordinate transformation, $|\rho|$ must be used. This in combination with the properties found in the Fourier Slice Theorem allows Equation 10.14 to come from Equation 10.13. With a simple rearrangement, we obtain Equation 10.15.

$$g_\theta(t) = \int_{-\infty}^{\infty} |\rho| P_\theta(\rho)e^{2\pi j\rho t} \, d\rho \tag{10.16}$$

$$= CTFT^{-1}\{|\rho| P_\theta(\rho)\} \tag{10.17}$$

$$= h(t) * p_\theta(r) \tag{10.18}$$

The rearrangement was done to more easily see the portion within the brackets which can be described as a function $g_\theta(t)$ where $t = x\cos\theta + y\sin\theta$. In this form, it can be seen that $g_\theta(t)$ is simply the inverse Continuous Time Fourier Transform of $|\rho| P_\theta(\rho)$, Equation 10.17.

We find that $|\rho|$ actually acts as a high pass filter which is visually interpreted in Figure 72. The further the radius, the greater the area for $d\theta d\rho$. This theoretically goes on infinitely, but for practicality, the response is bandlimited by f_c. Knowing that the absolute value of the Jacobian is a high pass filter and that multiplication in the frequency domain is convolution in the time domain, we obtain Equation 10.18. This finally yields the expression below.

114
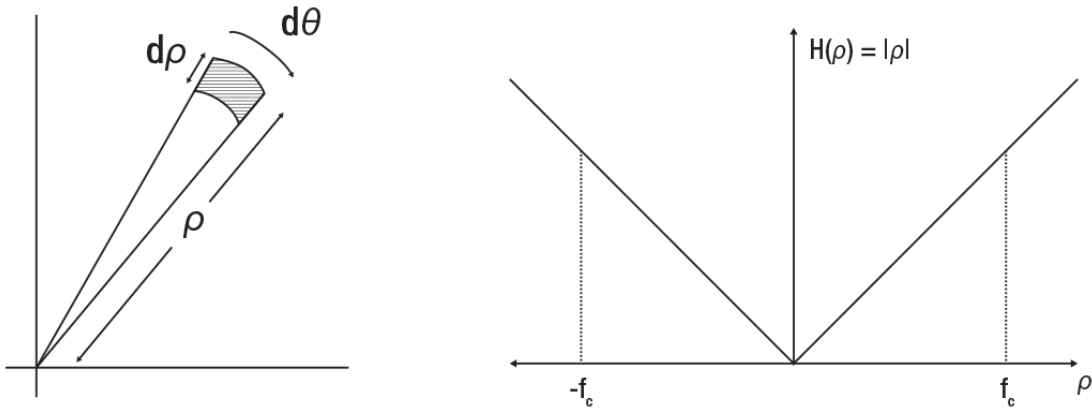
Figure 72: Visual explanation of the shape of the impulse response of the Jacobian of the polar coordinate transformation.

$$f(x,y) = \int_{-\infty}^{\pi} g_\theta(x \cos \theta + y \sin \theta) d\theta \tag{10.19}$$

A very high level explanation of this procedure is as follows. For a given projection, the high pass filter is applied. The filtered two dimensional response is then "stretched" into three dimensions in accordance to its angle. This is repeated for all of the projections and the sum of the "stretched" responses will yield the original image.

10.1.4   Modified CT: Scaling Map Summation

It was found that traditional methods may not be fully appropriate for the electric field imaging setup because the parallel "beam" resolution of our boards were not as fine as that of an X-Ray. Additionally, the board had gaps between pads due to board manufacturing restrictions. The computation in traditional CT also proved to be excessive considering the application was to simply detect and image sources of electric fields.

An algorithm was developed in MATLAB to make CT computations specific to our
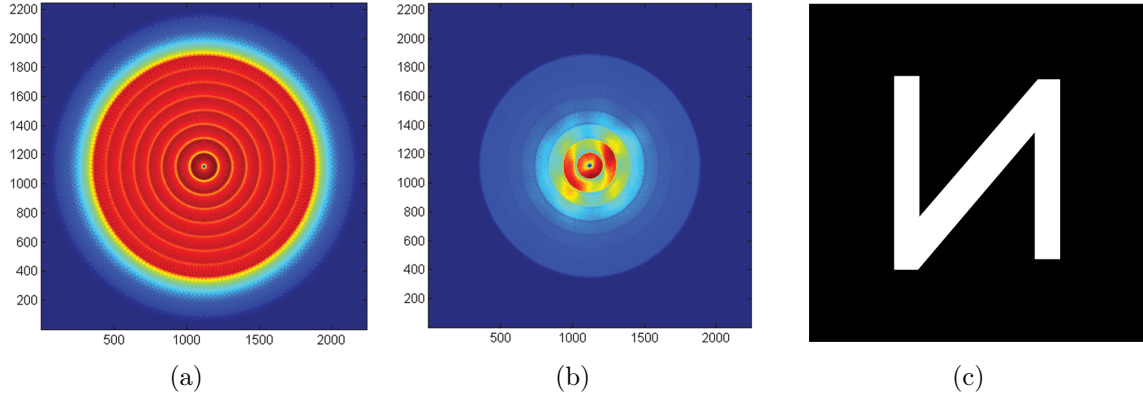
Figure 73: (a) Scaling coefficient map, (b) reconstructed image, and (c) original image with low pad resolution and high angular resolution.

board parameters. Many aspects of this algorithm borrowed the computationally conserving method of Convolution Back Projection. For openers, an even simpler computation method was implemented in which just the pad projections (with no target) at each angle were summed on the image space. This created a map of coefficients to scale the final image and correct for scaling offset.

The modified CT method greatly simplifies computation to simple summations which can be implemented on a PIC microcontroller while still being able to get reasonable images of electric fields relative to its environment. For the purpose of reconstructing a resemblance of the original image, it proved to be rather effective.

This algorithm was used to image an 'N' in both ideal and noisy conditions. Simulations took into account of pad length, width, and pitch. First, simulations were run to determine the effect of high angular resolution with poor pad resolution, Figure 73, and were followed by the best case scenario, Figure 74.

Even with very high angular resolution, it was found that it was not sufficient to compensate for low pad resolution. Gaps between pads proved to particularly detrimental to image quality seen by the artifacts in the reconstruction and even the scaling coefficient map, Figure 73. Ideal simulations showed that for a given square aspect ratio, at least 32 divisions

116

(a)   (b)   (c)
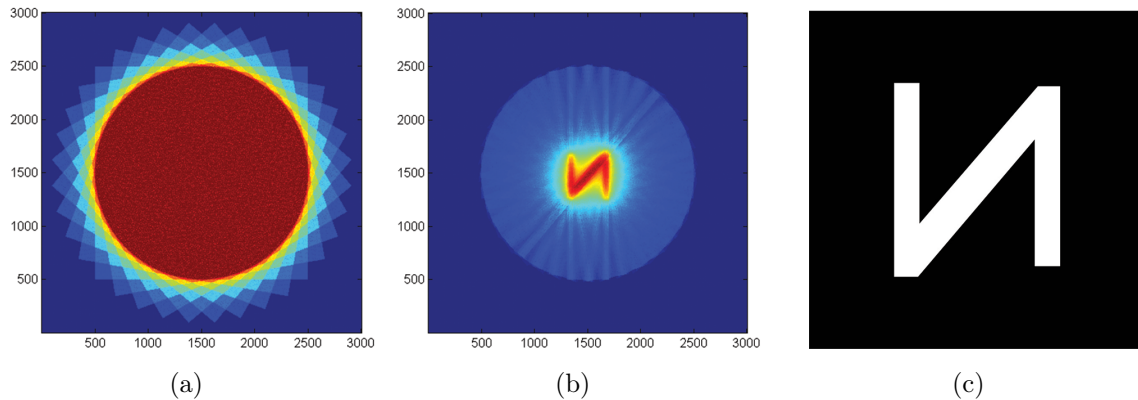
Figure 74: (a) Scaling coefficient map, (b) reconstructed image, and (c) original image with high pad resolution and high angular resolution.

(a)   (b)   (c)
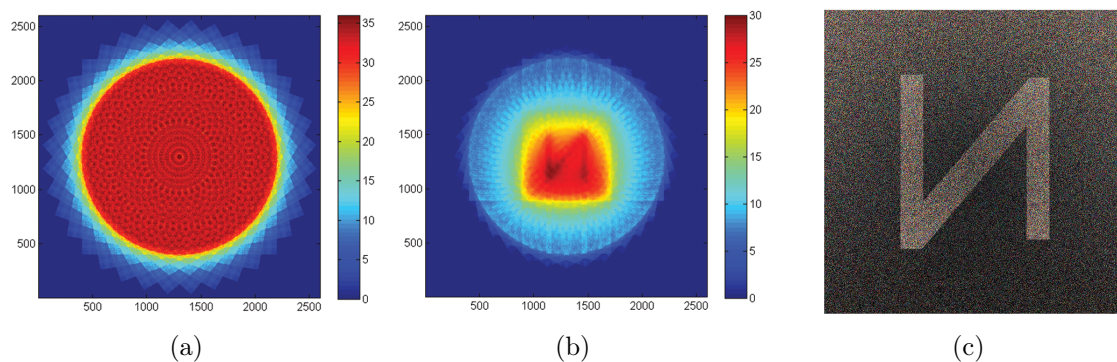
Figure 75: (a) Scaling coefficient map, (b) reconstructed image, and (c) very noisy original image with medium pad resolution and medium angular resolution.

(if limited to powers of two to be consistent with typical display driver configurations) were necessary to produce images that could be reasonably recovered.

To show that the algorithm was robust to handle noisy environments, the original image was buried in many layers of Gaussian noise, blurs, and gradients (simulating hotspots) to see if the 'N' shape could still be distinguished. A more practical medium pad/medium angular resolution combination was used for these simulations. The summing algorithm managed to perform admirably as it accurately reconstructs the noise but still manages to make the original image clearly detectable.

117

10.2   Wire Defocusing Algorithm

The underlying function to uncover may be representative of something other than the electric fields. For example, many applications this research is targeted towards is finding power in circuitry. Therefore, an algorithm can be developed to optimize extracting wires. As it has been seen, however, the electric fields from wires at a distance fringe, making the image of the wire blurry.

One possible way of extracting enough information to describe the wire is by fitting it to the analytic model. This, however, proves to not be very robust as the presence of multiple wires quickly complicates the model due to inter-capacitive coupling and other effects. This is only worsened when one needs to take into account of noise.

The first approach was to borrow principles of focus stacking. Focus stacking is commonly used in microscopy and even professional photography. The principle is to take multiple

(a)   (b)
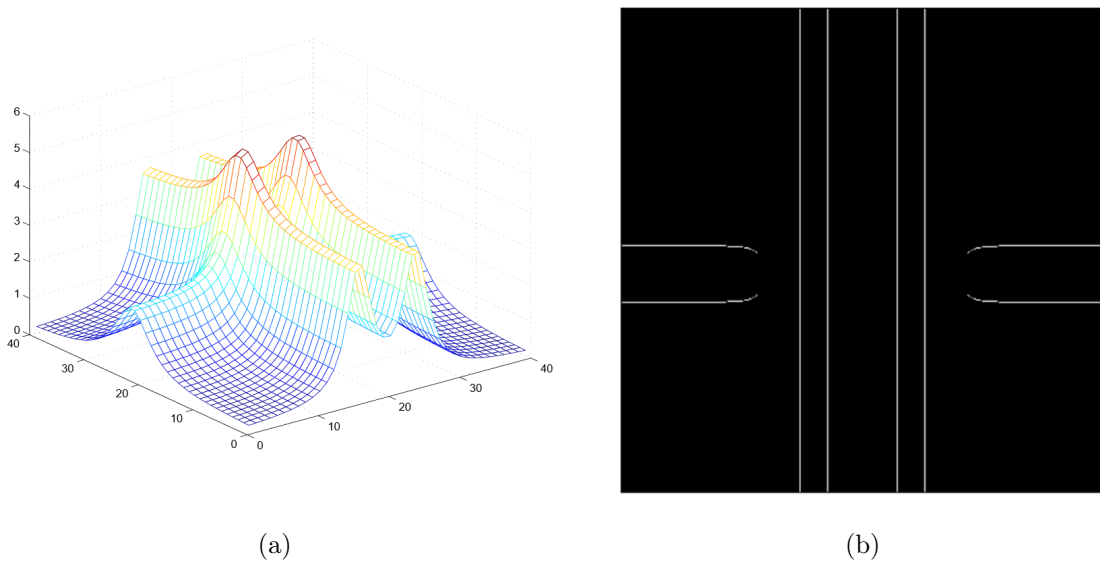
Figure 76: (a) Simulated electric fields from multilevel wires. (b) Extracted wire positions using edge detection.

Note: The three wires were placed at multiple levels in which the two parallel wires were at $x = -2$ and 2 cm at $z = 1$ while the perpendicular wire was placed at $y = 2$ and $z = 2$.

pictures of the same target at different focal lengths and reconstruct a new image using only the clear or sharp portions of the image.

$$e^{\frac{x^2}{2c^2} + \frac{y^2}{2c^2}}$$ (10.20)

$$-\frac{1}{pc^4}\left(1 - \frac{(x^2 + y^2)}{2c^2}\right)e^{-\frac{x^2 + y^2}{2c^2}}$$ (10.21)

The way it extracts the sharp regions follows this procedure. The image is first blurred by iteratively applying a Gaussian kernel, Equation 10.20, for each pixel about the image. A Laplacian Edge Detector kernel is then applied on the image in a similar fashion, Equation 10.21. The absolute value of the Gaussian/Laplacian result which quantifies the strength of an edge with respect to the kernels.

This method was simulated in a multilevel wire formation, Figure 76. The results show that it effectively managed to find the positions of the wires. Furthermore, the "blur" from the wire further away from the sensing array was greater, which would be expected given the behavior of the electric fields at a distance. It is possible to take multiple measurements at different distances, similar to the different focal distances in focal stacking, and extrapolate backwards to find even more detailed information about the wire such as absolute height from a point of reference.

Chapter 11

FUTURE WORK IN ELECTRIC FIELD IMAGING

Tremendous strides have been made in electric field imaging efforts at FEDC including building the world's first passive electric field imaging array, even on a flexible substrate. This chapter covers potential topics that research of eleectric field imaging could explore. Some of these subjects are already under development.

11.1   Board Improvements

While the current imager is functional, there are many design changes that can be made to enhance the performance and experience of the device. These modifications will make the possibility of making a production-ready imager more realistic.

11.1.1   Higher Specifications

Currently, the imager has a pixel size of 1 cm^2 and an array size of N$\times$16 when using the stepper approach. This greatly limits the resolution of images that can be obtained, especially if we are interested in imaging high density circuits such as motherboards for EMI detection. While a decreased pixel size correlates to a decrease in signal strength, the trade-off will have to be more thoroughly studied.

Sensor head design improvements can also be explored to increase signal strength. This will not only improve the signal to noise ratio but make low-signal strength applications possible. Possible solutions include corrugated D-dot sensors or use of dielectrics to increase the capacitance between the array and the object under test.

The method in which the array obtains data is also currently rather slow. Ultimately, the goal is to make the imager display electric fields in real-time. One possibility to approach

this goal is to reduce the time constant on the lock-in amplifier and use post processing techniques to still obtain a clear signal. It is also possible to run multiple readouts in parallel with dedicated multiplexers and decoders.

11.1.2 Integrated Components

The need of a large Agilent Switch/Measure Unit and external lock-in amplifier makes the setup unwieldy for field work, not to mention very expensive. Future designs plan to integrate a lock-in amplifier and multiplexer directly on to the imaging board. A custom lock-in amplifier designed with commercial off the shelf components has already been assembled and has proven to fare very well in performance for VLF measurements, even in comparison to high-end commercial lock-in amplifiers. Further post-processing may be implemented to achieve higher fidelity.
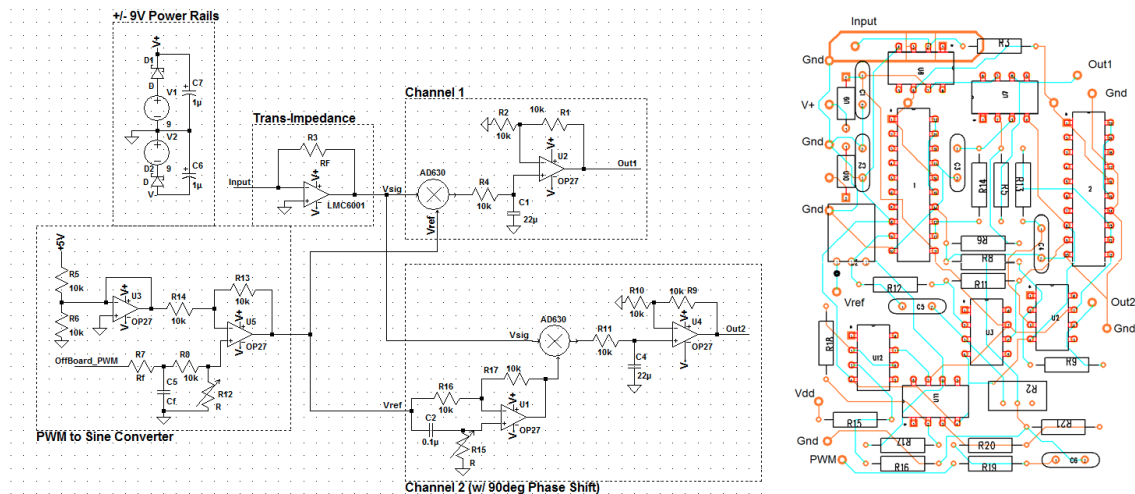
Figure 77: Schematic (left) and PCB layout (right) of a portable lock-in amplifier with commercial off the shelf components.

Source: This circuit was designed by my colleagues Jake Sciacca, Weidong Ye, Sandeep Vora, and Kegan Scowen for their senior design project through FEDC.
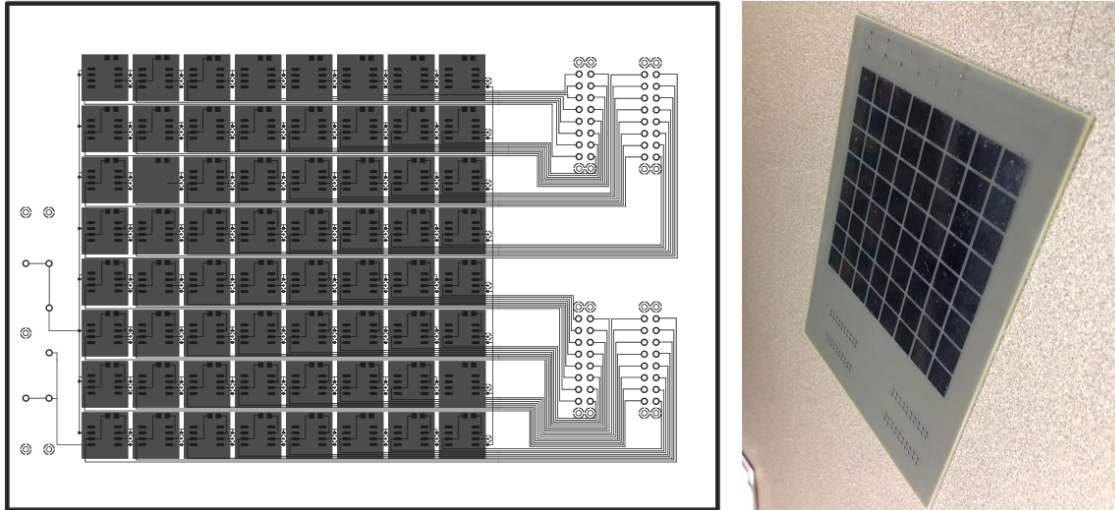
Figure 78: Schematic (left) and photograph (right) of an 8×8 two-dimensional electric field imager.

Source: This PCB was designed by Anthony Wilson.

11.1.3   Full Two-Dimensional Array

Despite having success with the one-dimensional stepper method, there is still a pursuit to build a fully two-dimensional array. This endeavor was recently realized in the form of an 8×8 array with 1 cm^2 pixels, Figure 78. The design required upgrading to a four-layer PCB as well as a switch from through-hole LMC6001 operational amplifiers to surface mount LMC6081 operational amplifiers of the same specifications. There are plans to make a series of measurements with the new array.

11.2   Software

Aside from hardware, improvements in software can help improve the accuracy of our devices as well as help make the boards run more efficiently. Post-processing will allow us to extract information from noisy signals, allowing for greater leniency on the hardware

specifications. It will also allow for optimized performance for a given application. Software is also key in improving the speed of automation, a feature that will be critical with the large amount of experiments to come.

11.2.1 Defocusing Algorithm

Imaging wires is still a great interest for future experiments. Such applications usually call for not only imaging the electric fields radiating from the wires but also the wires themselves. The groundwork for the defocusing algorithm to accomplish the latter task was introduced in the previous chapter. Improvements to the algorithm include accounting for artifacts (especially around peaks), adding resiliance to noise, and utilizing multi-level images for a better description of the wires. The information extracted from these methods can also provide parameters for a probabilistic fitting algorithm to gain even greater accuracy in the reconstruction.

11.2.2 Improved Drivers

Drivers are key in developing an efficient testbench. Drivers have already been written in the automation efforts and have dramatically reduced measurement times. There is still much room for improvement, however, as the current approach is very iterative rather than parallel. Software can also be optimized such as measurement times and lag times which are currently conservatively hardcoded to give ample time for the lock-in amplifier to settle.

11.3 Applications

The electric field imager presented in this thesis opens up a new realm of possibilities in terms of applications far beyond the ones mentioned in this manuscript. For example, with electric fields having such a close relationship with magnetic fields, magnetic field

measurements can greatly complement the electric field imager. A few other topics are discussed below.

11.3.1 Active Interrogation

Though the imager is advertised as a passive device, it can be used in conjunction with driving electrodes to stimulate objects to be imaged. The ability to image inactive wires is one such example. The inactive wire can collect charge from the driving electrode running at a reference frequency and then couple to pixels on the imager. Preliminary ANSYS Maxwell simulations and preliminary one-dimensional experimental results suggest this is a viable option, Figure 79. Preliminary measurements with active interrogation have also been done with the new two-dimensional array. A more systematic study of experimental results will have to be conducted to properly characterize the effect of different driving electrode parameters on the imager.
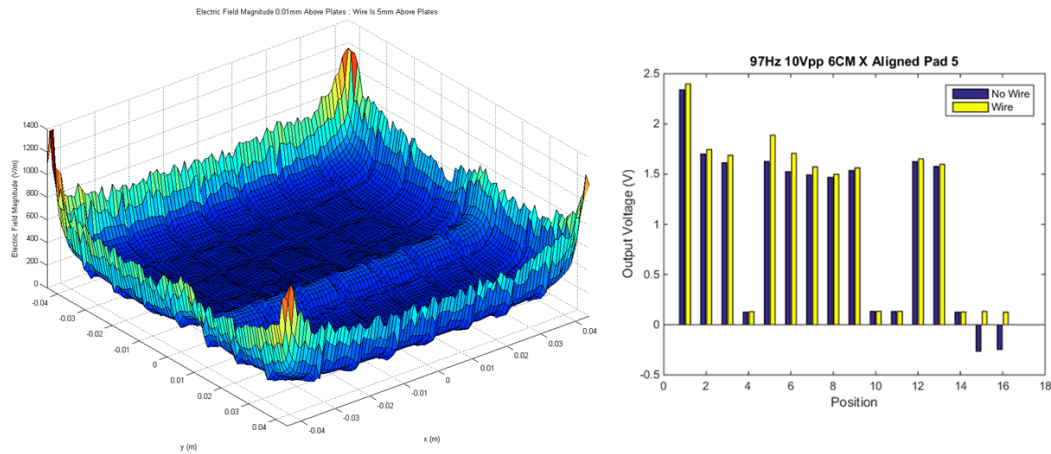
Figure 79: ANSYS simulation of imaging a floating wire with a D-dot array (left) and a one-dimensional comparison of electric field strengths with and without a wire (right).

Source: The ANSYS simulations were run by my colleague, Alex Lucas. The experimental measurements were made by my colleagues John Gorrie, Matt Oman, and Clementina Reynolds.

11.3.2 EMI Detection

Finally, EMI detection will continue to be a strong topic of interest in future research. This also allows for the opportunity to explore magnetic field radiation as well as frequencies greater than the VLF range. Success in this field will require a culmination of hardware, software, and methodology improvements.

Chapter 12

FINAL THOUGHTS

The paradigm of this research have been to build large area radiation sensing arrays by leveraging the low-cost TFT process used by the display industry. Doing so will allow for novel form factors that could prove especially useful for security and industrial applications. It also leaves open the possibility to fabricate on flexible substrates for devices that can be used in a wallpaper-like fashion and even wearable. The greatest challenge, however, in this effort is overcoming the performance limitations of TFTs compared to it's single-crystal counterparts , particularly in the lack of access to CMOS circuitry.

Work done in the neutron detection project to overcome these obstacles include novel ways of cascading NMOS-only amplification stages to build an amplifier with sufficient gain and low noise to detect alpha particles from a thin film PiN diode. We have proven that all of the individual components are sufficient to carry out the task at hand and the next step is to integrate all of the parts into one cohesive system. This implies modifications to front and back end circuitry as well as the active matrix architecture, requiring corresponding drivers for operation.

Research in electric fields yielded a comprehensive study in the theory, design, and VLF experimental results of D-dot array based electric field imagers. The results prove we are capable of imaging concealed energized wires with very high sensitivity and repeatability. Imaging wires is only the most basic of introductions to the topic as research can delve into many paths from device performance to high level EMI detection.

I plan to continue research in these two projects during my doctoral program and expect the work presented to culminate into a full demonstration unit. I also hope this work provides the foundation necessary to build bigger and faster production-ready large-area sensing arrays as well as provide insight to the theory and mechanisms behind these devices. It is a new and exciting field to be in with great implications for the future.

REFERENCES

[1]   G. LaFree, S. Presser, R. Tourangeau, A. Adamczyk, and J. Jay, "U.s. attitudes toward terorrism and counterterrorism," National Consortium of the Study of Terrorism and Responses to Terrorism, College Park, Maryland, Tech. Rep., Mar. 2013.

[2]   J. Risen and P. Shenon, "U.s. says it halted qaeda plot to use radioactive bomb," *The New York Times*, Jun. 2002.

[3]   D. Kotz, "Injury toll from marathon bombs reduced to 264," *The Boston Globe*, Apr. 2013.

[4]   A. C. Estes, A. Abad-Santos, and M. Sullivan, "Explosions at boston marathon kill 3 — now, a 'potential terrorist investigation'," *The Wire*, Apr. 2013.

[5]   R. Runkle, A. Bernstein, and P. Vanier, "Securing special nuclear material: Recent advances in neutron detection and their role in nonproliferation," *Journal of Applied Physics*, vol. 108, no. 11, Dec. 2010.

[6]   R. Kouzes, "The ^{3}He supply problem," Pacific Northwest National Laboratory, Tech. Rep. PNNL-18388, Apr. 2009.

[7]   T. Crane and M. Baker, "Passive nondestructive assay of nuclear materials," in. Springfield, VA: US Nuclear Regulatory Comission, 1991, ch. Neutron Detectors, pp. 379–406.

[8]   G. R. Kunnen, "Large area flexible thermal neutron detector," PhD thesis, Arizona State University, May 2013.

[9]   T. Baumann, "Neutron detection & spectroscopy," National Superconducting Cyclotron Laboratory at Michigan State University, Tech. Rep., Aug. 2001.

[10] G. F. Knoll, *Radiation Detection and Measurement*, 4th edition. Boston, MA: John Wiley Sons, Aug. 2010.

[11] *Portable gamma and thermal neutron detector using* ^{6}LiI(Eu) *crystals*, vol. 5198, ser. Hard X-Ray and Gamma-Ray Detector Physics V 11, Remote Sensing Laboratory and Special Technology Laboratories, Bechtel, NV: SPIE, Jan. 2004.

[12] D. McGregor, M. Hamming, Y. Yang, H. Gresch, and R. Klann, "Design considerations for thin film coated semiconductor thermal neutron detectors—i: Basics regarding alpha particle emittingneutron reactive films," *Nuclear Instruments and Methods in Physics Research*, vol. 500, pp. 272–308, Mar. 2003.

[13] R. Nikolic, A. Conway, C. Reinhardt, R. Graff, T. Wang, N. Deo, and C. Cheung, "6:1 aspect ratio silicon pillar based thermal neutron detector filled with 10b," *Applied Physics Letters*, vol. 93, no. 13, Sep. 2008.

[14] G. Kunnen, J. Smith, H. Chung, and D. Allee, "Tft-based, multi-stage, active pixel sensor for alpha particle detection," *Institution of Engineering and Technology Electronics Letters*, vol. 50, no. 9, pp. 705–706, Apr. 2014.

[15] D. Mentley, "State of flat-panel display technology and future trends," *Proceedings of the IEEE*, vol. 90, no. 4, pp. 453–459, Apr. 2002. DOI: 10.1109/JPROC.2002.1002520.

[16] D. Taylor, "Measuring techniques for electrostatics," *Journal of Electrostatics*, vol. 51-52, pp. 502–508, 2001.

[17] T. G. Zimmerman, J. R. Smith, J. A. Paradiso, D. Allport, and N. Gershenfeld, "Applying electric field sensing to human-computer interfaces," in *Proceedings of the SIGCHI Conference on Human Factors in Computing Systems*, ser. CHI '95, Denver, Colorado, USA: ACM Press/Addison-Wesley Publishing Co., 1995, pp. 280–287.

[18] J. R. Smith, "Electric field imaging," PhD thesis, Massachusetts Institute of Technology, Feb. 1999.

[19] *Proximity design guide*, Atmel, 2013.

[20] M. Kamogawa, J. Liu, H. Fujiwara, Y. Chuo, Y. Tsai, K. Hattori, T. Nagao, S. Uyeda, and Y. Ohtsuki, "Atmospheric field variations before the march 31, 2002 m6.8 earthquake in taiwan," *Terr. Atmospheric Ocean, Sci*, vol. 15, no. 3, pp. 397–412, Sep. 2004.

[21] B. Carlson and U. Inan, "A novel technique for remote sensing of thunderstorm electric fields via the kerr effect and sky polarization," *Geophysical Research Letters*, vol. 35, no. 22, Nov. 2008.

[22] W. Telford, L. Geldart, and R. Sheriff, *Applied Geophysics*, 2nd ed. Cambridge University Press, Oct. 1990.

[23] R. Harikumar, R. Prabu, and S. Raghavan, "Electrical impedance tomography (eit) and its medical applications: A review," *International Journal of Soft Computing and Engineering*, vol. 3, no. 4, pp. 193–198, Sep. 2013.

[24] T. Sullivan, S. Deiss, and G. Cauwenberghs, "A low-noise, non-contact eeg/ecg sensor," in *Biomedical Circuits and Systems Conference, 2007. BIOCAS 2007. IEEE*, Nov. 2007, pp. 154–157. DOI: 10.1109/BIOCAS.2007.4463332.

[25] J. Smith, E. Garcia, R. Wistort, and D. Krishnamoorthy, "Electric field imaging pretouch for robotic graspers," in *Proceedings of the IEEE/RSJ Intl. Conference on Intelligent Robots and Systems*, San Diego, CA, USA, Oct. 2007, pp. 676–683.

[26] R. Fano, L. Chu, and R. Adler, *Electromagnetic Fields, Energy, and Forces.* New York: John Wiley and Sons, 1960.

[27] C. Browning, S. Vinci, J. Zhu, and D. Hull, "An evaluation of electric-field sensors for projectile detection," *IEEE Sensors*, Nov. 2013.

[28] Z. Zhang, L. Li, X. Xie, D. Xiao, and W. He, "Optimization design and research character of the passive electric field sensor," *Sensors Journal, IEEE*, vol. 14, no. 2, pp. 508–513, Feb. 2014. DOI: 10.1109/JSEN.2013.2284201.

[29] B. Rhoades, S. Ramsey, and M. Noras, "A novel electric-field sensor for projective detection," in *Proc. 2012 Joint Electrostatics Conference*, 2012, pp. 1–17.

[30] D. Hull and S. Vinci, "Passive aircraft detection and noncooperative helicopter identification using extremely low frequency (elf) electric field sensors," in *Law Enforcement and Physical Security Symposium*, Boston, MA, USA: SPIE, Nov. 1998, pp. 1–11.

[31] X. Li, V. Inclan, G. Rowe, and A. Mamishev, "Parametric modeling of concentric fringing electric field sensors," in *Annual Report Conference on Electrical Insulation and Dielectric Phenomena*, IEEE, 2005, pp. 617–620.

[32] B. Mayton, L. LeGrand, and J. Smith, "Robot, feed thyself: Plugging in to unmodified eletrical outlets by sensing emitted ac electric fields," in *IEEE Intl. Conference on Robotics and Automation*, Anchorage, AK, USA, May 2010, pp. 715–722.

[33] S. Ghionea, G. Smith, J. Pulskamp, S. Bedair, C. Meyer, and D. Hull, "Mems electric-field sensor with lead zirconate titanate (pzt)-actuated electrodes," in *SENSORS, 2013 IEEE*, Nov. 2013, pp. 1–4. DOI: 10.1109/ICSENS.2013.6688131.

[34] S. Schultz, "Non-intrusive electric field sensing," *SPIE*, Jan. 2014.

[35] T. Sudo, H. Sasaki, N. Masuda, and J. Drewniak, "Electromagnetic interference (emi) of system-on-package (sop)," *Advanced Packaging, IEEE Transactions on*, vol. 27, no. 2, pp. 304–314, May 2004. DOI: 10.1109/TADVP.2004.828817.

[36] B. Gnade, M. Quevedo, D. Allee, S. Venugopal, C. Balanis, T. Jackson, H. McHugh, K. Baugh, E. Forsythe, and D. Morton, "Flexible integrated sensor systems," in *Special Operations Forces Industry Conference*, Tampa, FL, USA, Jun. 2009.

[37] D. Allee, L. Clark, B. Vogt, R. Shringarpure, S. Venugopal, S. Uppili, K. Kaftanoglu, H. Shivalingaiah, Z. Li, J. Ravindra Fernando, E. Bawolek, and S. O'Rourke, "Circuit-level impact of a-si:h thin-film-transistor degradation effects," *Electron Devices, IEEE Transactions on*, vol. 56, no. 6, pp. 1166–1176, Jun. 2009.

[38] M. Marrs, C. Moyer, E. Bawolek, R. Cordova, J. Trujillo, G. Raupp, and B. Vogt, "Control of threshold voltage and saturation mobility using dual-active-layer device based on amorphous mixed metal-oxide-semiconductor on flexible plastic substrates," *Electron Devices, IEEE Transactions on*, vol. 58, no. 10, pp. 3428–3434, Oct. 2011.

[39] K. Kaftanoglu, S. Venugopal, M. Marrs, A. Dey, E. Bawolek, D. Allee, and D. Loy, "Stability of izo and a-si:h tfts processed at low temperature (200 °c)," *Display Technology, Journal of*, vol. 7, no. 6, pp. 339–343, Jun. 2011.

[40] J. Smith, A. Couture, J. Stowell, and D. Allee, "Optically seamless flexible electronic tiles for ultra large-area digital x-ray imaging," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 4, no. 6, pp. 1109–1115, Jun. 2014. DOI: 10.1109/TCPMT.2014.2316477.

[41] T. Pochet, A. Ilie, A. Brambilla, and B. Equer, "Sensitivity measurements of thick amorphous-silicon p-i-n nuclear detectors," *Nuclear Science, IEEE Transactions on*, vol. 43, no. 3, pp. 1452–1457, Jun. 1996. DOI: 10.1109/23.507082.

[42] C. Hordequin, A. Brambilla, P. Bergonzo, and F. Foulon, "Nuclear radiation detectors using thick amorphous-silicon {mis} devices," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 456, no. 3, pp. 284–289, 2001. DOI: http://dx.doi.org/10.1016/S0168-9002(00)00575-1. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0168900200005751.

[43] J. W. Murphy, L. Smith, J. Calkins, G. R. Kunnen, I. Mejia, K. D. Cantley, R. A. Chapman, J. Sastré-Hernández, R. Mendoza-Pérez, G. Contreras-Puente, D. R. Allee, M. Quevedo-Lopez, and B. Gnade, "Thin film cadmium telluride charged particle sensors for large area neutron detectors," *Applied Physics Letters*, vol. 105, no. 11, 112107, 2014. DOI: http://dx.doi.org/10.1063/1.4895925.

[44] N. Hernandez-Como, F. Berrellez-Reyes, R. Mizquez-Corona, O. Ramirez-Esquivel, I. Mejia, and M. Quevedo-Lopez, "Cds-based p-i-n diodes using indium and copper doped cds films by pulsed laser deposition," *Semiconductor Science and Technology*, vol. 30, no. 6, p. 065 003, 2015.

[45] G. Bertuccio, P. Rehak, and D. Xi, "A novel charge sensitive preamplifier without the feedback resistor," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 326, no. 1–2, pp. 71–76, 1993. DOI: http://dx.doi.org/10.1016/0168-9002(93)90334-E. [Online]. Available: http://www.sciencedirect.com/science/article/pii/016890029390334E.

[46] F. Ramírez-Jiménez, E. Aguilera, R. López-Callejas, J. Benítez-Read, and J. Pacheco-Sotelo, "A novel application of a {pin} diode-preamplifier set for the measurement of charged particles," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 545, no. 3, pp. 721–726, 2005. DOI: http://dx.doi.org/10.1016/j.nima.2005.02.017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0168900205007606.

[47] A. Dey, A. Avendanno, S. Venugopal, D. Allee, M. Quevedo, and B. Gnade, "Cmos tft op-amps: Performance and limitations," *Electron Device Letters, IEEE*, vol. 32, no. 5, pp. 650–652, May 2011. DOI: 10.1109/LED.2011.2121891.

[48] P. Nayak, J. Caraveo-Frescas, Z. Wang, M. Hedhili, Q. Wang, and H. Alshareef, "Thin film complementary metal oxide semiconductor (cmos) device using a single-step deposition of the channel layer," *Scientific Reports, Nature*, vol. 4, pp. 1–7, Apr. 2014.

[49] K. Karim, A. Nathan, and J. Rowlands, "Amorphous silicon active pixel sensor readout circuit for digital imaging," *Electron Devices, IEEE Transactions on*, vol. 50, no. 1, pp. 200–208, Jan. 2003. DOI: 10.1109/TED.2002.806968.

[50] Y. Tsividis and P. Gray, "An integrated nmos operational amplifier with internal compensation," *Solid-State Circuits, IEEE Journal of*, vol. 11, no. 6, pp. 748–753, Dec. 1976. DOI: 10.1109/JSSC.1976.1050813.

[51] Y.-C. Tarn, P.-C. Ku, H.-H. Hsieh, and L.-H. Lu, "An amorphous-silicon operational amplifier and its application to a 4-bit digital-to-analog converter," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 5, pp. 1028–1035, May 2010. DOI: 10.1109/JSSC.2010.2043886.

[52] E. Lee, G. Kunnen, A. Dominguez, and D. Allee, "A low-noise dual-stage a-si:h active pixel sensor," *Electron Devices, IEEE Transactions on*, vol. 59, no. 6, pp. 1679–1685, Jun. 2012. DOI: 10.1109/TED.2012.2189403.

[53] G. Kunnen, D. Pressler, E. Lee, D. Allee, J. Murphy, I. Mejia, M. Quevedo, and B. Gnade, "Large area sensing arrays for detection of thermal neutrons," in *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2012 IEEE*, Oct. 2012, pp. 156–161. DOI: 10.1109/NSSMIC.2012.6551083.

[54] P. C. Hobbs, "Photodiode front ends: The real story," *Optics and Photonics News*, pp. 42–45, Apr. 2001.

[55] A. Tronson, "Single chip vlf magnetic field receiver," PhD thesis, Stanford University, May 2014.

[56] C. A. Altgelt, "The world's largest "radio" station," U.S. Navy, Tech. Rep., 2005.

[57] S. Vinci, J. Zhu, and D. Hull, "Analysis of electrostatic charge on small-arms projectiles," in *Proc. SPIE, Active and Passive Signatures*, G. Gilbreath and C. Hawley, Eds., vol. 8382, Anchorage, AK, USA, May 2012, pp. 715–722.

[58] G. Karady and K. Holbert, *Electrical Energy Conversion and Transport*, 2nd ed. Wiley-IEEE Press, 2013.

[59] *Electric field mill*, http://a-tech.net/ElectricFieldMill/, Accessed: 2014-03-15.

[60] J. Smith, A. Couture, and D. Allee, "Charge emission induced transient leakage currents of a-si:h and igzo tfts on flexible plastic substrates," *Electronics Letters*, vol. 50, no. 2, pp. 105–106, Jan. 2014. DOI: 10.1049/el.2013.3795.

[61] V. Isakov, *Inverse Source Problems (Mathematical Surveys and Monographs)*. American Mathematical Society, 1990.

[62] A. C. Kak and M. Slaney, *Principles of Computerized Tomographic Imaging (Classics in Applied Mathematics)*. Society for Industrial and Applied Mathematics, 2001.

APPENDIX A

MATLAB CODE

A.1 Read Driver

```matlab
1  % Sets on voltage value, off voltage value, and time in between changes
2  off = -5;
3  on = 15;
4  numrows = 1;
5  numcols = 16;
6  meas_rate=2;
7  lagtime = 5;
8  meas_duration=2;
9  v = off*ones(numrows) + (on-off)*eye(numrows);
10 data_array=zeros(numrows,numcols);
11 disp('Connection to Agilent...')
12 % Connect ot the Agilent 34980A
13 object = visa('agilent', 'USB0::2391::1287::my53152023::INSTR');
14 fopen(object);
15 disp('Connection to NI DAQ...')
16 %%
17 % Initialize NI DAQ
18 devices = daq.getDevices;
19 % create a session and add the four analog input channels
20 % 6009 syntax
21 % Ground pins 1 and 4
22 s = daq.createSession('ni');
23 % Pins 2(V+) & 3(V-)
24 s.addAnalogInputChannel('Dev2',1,'voltage');
25 % Pins 5(V+) & 6(V-)
26 % s.addAnalogInputChannel('Dev1',1,'voltage');
27 % session rate default 1000 scans/second
28 s.Rate = meas_rate;
29 %Set Duration
30 s.DurationInSeconds = meas_duration;
31
32 for n = 1:numrows
33     % Turn the nth row on
34     fprintf(object, 'SOUR:VOLT %d, (@4001)', v(1, n))
35     fprintf(object, 'OUTP:STAT ON,(@4001)')
36     fprintf(object, 'SOUR:VOLT %d, (@1002)', v(2, n))
37     fprintf(object, 'OUTP:STAT ON,(@1002)')
38     fprintf(object, 'SOUR:VOLT %d, (@1003)', v(3, n))
39     fprintf(object, 'OUTP:STAT ON,(@1003)')
40     fprintf(object, 'SOUR:VOLT %d, (@1004)', v(4, n))
41     fprintf(object, 'OUTP:STAT ON,(@1s004)')
42     n
43
44     for k = numcols:-1:1
45             k
46             %pad with zeros
47             temp = sprintf('%03d',k);
48             fprintf(object, 'ROUTe:CLOSe (@4%s)',temp)
49             pause(lagtime);
50             data_array(n,k)=f_daq_data(s);
```

```matlab
51                fprintf(object, 'ROUTe:OPEN (@4%s)',temp)
52        end;
53
54        % Turn all rows off
55        fprintf(object, 'SOUR:VOLT %d, plot(@4001:4016)', off)
56        fprintf(object, 'OUTP:STAT ON,(@4001:4016)')
57        pause(2);
58  end;
59
60  % Reset everything to zero
61  fprintf(object, 'SOUR:VOLT %d, (@6001:6004)', 0)
62  fprintf(object, 'OUTP:STAT ON,(@6001:6004)')
63
64  fclose(object);
65  csvwrite(strcat(filelocation,'.csv'),data_array)
66  plotgrid_save(data_array,filelocation,filename)
```

A.2 Modified CT Algorithm

```matlab
1  length_cm = 18;          % real world measurement (cm)
2  width_cm = .5;           % real world measurement (cm)
3  gap_cm = 0.05;           % real world measurement (cm)
4  pixel_dens = 100;        % N pixels per cm
5  pad_total = 32;          % number of pads
6  angle_res = 10;
7  angles = 0:angle_res:360-angle_res;
8
9
10 maps = cell(length(angles),1);
11
12 % length of space of interest after accounting for rotations
13 total_length_cm = ceil(sqrt(2)*length_cm);
14 if mod(total_length_cm,2) == 1
15     total_length_cm = total_length_cm + 1;
16 end
17
18 % convert from real world measurements to pixel length
19 length_pix = length_cm*pixel_dens;
20 width_pix = width_cm*pixel_dens;
21 gap_pix = gap_cm*pixel_dens;
22 total_length = total_length_cm*pixel_dens;
23 margin = (total_length - length_pix)/2;  %give some buffer
24
25 % determine coordinates for vertices of each pad and store in array
26 pad_indices_X = zeros(4,pad_total);
27 pad_indices_Y = zeros(4,pad_total);
28
29 % the space of pixels to be mapped
30 space = zeros(total_length, total_length);
31
32 % determine the initial vertex coordinates of all pads
33 for i = 1:pad_total
34     pad_indices_X_init(1,i) = (i-1)*(width_pix+gap_pix)+margin;
35     pad_indices_X_init(2,i) = (i-1)*(width_pix+gap_pix)+margin;
36     pad_indices_X_init(3,i) = (i-1)*(width_pix+gap_pix)+margin+width_pix;
37     pad_indices_X_init(4,i) = (i-1)*(width_pix+gap_pix)+margin+width_pix;
38
39     pad_indices_Y_init(1,i) = margin;
40     pad_indices_Y_init(2,i) = margin+length_pix;
41     pad_indices_Y_init(3,i) = margin+length_pix;
42     pad_indices_Y_init(4,i) = margin;
43 end
44
45 % determine the vertex coordinates of all pads
46 for i = 1:pad_total
47     pad_indices_X(1,i) = (i-1)*(width_pix+gap_pix)+margin;
48     pad_indices_X(2,i) = (i-1)*(width_pix+gap_pix)+margin;
49     pad_indices_X(3,i) = (i-1)*(width_pix+gap_pix)+margin+width_pix;
50     pad_indices_X(4,i) = (i-1)*(width_pix+gap_pix)+margin+width_pix;
```

```matlab
51
52      pad_indices_Y(1,i) = margin;
53      pad_indices_Y(2,i) = margin+length_pix;
54      pad_indices_Y(3,i) = margin+length_pix;
55      pad_indices_Y(4,i) = margin;
56  end
57
58
59
60  % reshape indices to be read in a Nx2 array
61  x = reshape(pad_indices_X,pad_total*4,1);
62  y = reshape(pad_indices_Y,pad_total*4,1);
63  xy = horzcat(x,y);
64
65  for j = 1:length(angles)
66      space = zeros(total_length, total_length);
67      tempspace = zeros(total_length, total_length);
68
69      test_angle = angles(j);
70      R = [cosd(test_angle), -sind(test_angle); sind(test_angle), cosd(...
            test_angle)];
71
72      indices = xy - margin - length_pix/2;
73
74      temp = R*indices';
75      temp = round(temp) + margin + length_pix/2;
76
77      [x, y] = size(temp);
78
79      pad_indices_X = reshape(temp(1,:),4,pad_total);
80      pad_indices_Y = reshape(temp(2,:),4,pad_total);
81
82      if R == [1,0;0,1]
83          for i = 1:pad_total
84              xmin = min(pad_indices_X_init(:,i));
85              xmax = max(pad_indices_X_init(:,i));
86              ymin = min(pad_indices_Y_init(:,i));
87              ymax = max(pad_indices_Y_init(:,i));
88
89              for xfill = xmin:xmax
90                  for yfill = ymin:ymax
91                      % space(yfill, xfill) = i;
92                      space(yfill, xfill) = 1;
93                  end
94              end
95          end
96
97  %          figure
98  %          imagesc(space)
99  %          set(gca,'YDir','normal');
100 %          axis square
101
102          maps{j,1} = space;
103
104
```

```matlab
105      elseif (R == [0,-1;1,0] | R == [-1,0;0,-1] | R == [0,1;-1,0])
106           for i = 1:pad_total
107               spacetemp = zeros(total_length, total_length);
108               xmin = min(pad_indices_X_init(:,i));
109               xmax = max(pad_indices_X_init(:,i));
110               ymin = min(pad_indices_Y_init(:,i));
111               ymax = max(pad_indices_Y_init(:,i));
112
113               for xfill = xmin:xmax
114                   for yfill = ymin:ymax
115                       spacetemp(yfill, xfill) = 1;
116                   end
117               end
118
119               [ytemp, xtemp] = find(spacetemp == 1);
120
121               indices = horzcat(xtemp, ytemp) - margin - length_pix/2;
122               temp = R*indices';
123               temp = temp + margin + length_pix/2;
124
125               for index = 1:length(temp)
126                   % space(temp(2, index), temp(1, index)) = i;
127                   space(temp(2, index), temp(1, index)) = 1;
128               end
129           end
130
131 %         figure
132 %         imagesc(space)
133 %         set(gca,'YDir','normal');
134
135           maps{j,1} = space;
136
137      else
138           for i = 1:pad_total
139               [z, uniquex] = unique(pad_indices_X(:,i));
140               [z, uniquey] = unique(pad_indices_Y(:,i));
141
142               if max(uniquex) == 4 ||  max(uniquey) == 4
143                   x_coord = pad_indices_X(:,i);
144                   y_coord = pad_indices_Y(:,i);
145
146                   [b_x, i_x] = sort(x_coord);
147
148                   slope1 = (y_coord(i_x(3))-y_coord(i_x(1)))/(x_coord(i_x(3))...
149                       -x_coord(i_x(1)));
                      slope2 = (y_coord(i_x(4))-y_coord(i_x(3)))/(x_coord(i_x(4))...
                          -x_coord(i_x(3)));
150
151                   x_bound1 = x_coord(i_x(1)):x_coord(i_x(3));
152                   y_bound1 = slope1*x_bound1 + y_coord(i_x(1)) - slope1*...
                          x_coord(i_x(1));
153                   x_bound2 = x_coord(i_x(2)):x_coord(i_x(4));
154                   y_bound2 = slope1*x_bound2 + y_coord(i_x(2)) - slope1*...
                          x_coord(i_x(2));
155
```

138

```matlab
156                    bound1 = round([x_bound1; y_bound1]);        %1 to 3
157                    bound2 = round([x_bound2; y_bound2]);        %2 to 4
158
159                    x_bound3 = x_coord(i_x(1)):x_coord(i_x(2));
160                    y_bound3 = slope2*x_bound3 + y_coord(i_x(1)) - slope2*...
                            x_coord(i_x(1));
161                    x_bound4 = x_coord(i_x(3)):x_coord(i_x(4));
162                    y_bound4 = slope2*x_bound4 + y_coord(i_x(3)) - slope2*...
                            x_coord(i_x(3));
163
164                    bound3 = round([x_bound3; y_bound3]);        %1 to 2
165                    bound4 = round([x_bound4; y_bound4]);        %3 to 4
166
167                    allbounds = [bound1, bound2, bound3, bound4];
168
169                    if slope1 < 0
170                        lowerbound = [bound1, bound4];
171                        upperbound = [bound3, bound2];
172                    else
173                        lowerbound = [bound3, bound2];
174                        upperbound = [bound1, bound4];
175                    end
176                end
177
178                for xfill = x_coord(i_x(1)):x_coord(i_x(4))
179                    ymax_i = find(upperbound(1,:) == xfill);
180                    ymin_i = find(lowerbound(1,:) == xfill);
181
182                    ymax = upperbound(2, ymax_i(1));
183                    ymin = lowerbound(2, ymin_i(1));
184
185                    for yfill = ymin:ymax
186                        %space(yfill, xfill) = i;
187                        space(yfill, xfill) = 1;
188                    end
189                end
190            end
191
192 %          figure
193 %          imagesc(space)
194 %          set(gca,'YDir','normal');
195 %          axis square
196
197            maps{j,1} = space;
198            space = zeros(total_length, total_length);
199        end
200
201 end
202
203 mapsum
204 image_ex
```

139

A.3   Defocusing Algorithm

```matlab
1  % Define Kernels
2  GK = [1,2,1;2,4,2;1,2,1];
3  LED = [-1, -1, -1; -1, 8, -1; -1, -1, -1];
4
5  % Form grid
6  x = -10:0.05:10;
7  y = -10:0.05:10;
8
9  % Form
10 pixels = zeros(40,40);
11
12 % Electric Field Strength given by
13 % lambda*C*h/(h^2+x^2)   where C = 1/epsilon*pi and lambda = charge on
14 % the wire
15
16 lambda = 1e-10;
17 epsilon = 8.854e-12;
18 C = 1/(epsilon*pi);
19
20 % Wire parameters: [height, offset]
21 wire1 = [1, 2];
22 wire2 = [1, -2];
23 wire3 = [2, 1];
24
25 wire1b = [2, 2];
26 wire2b = [2, -2];
27 wire3b = [5, 1];
28
29 % Preallocate space for real-space
30 z1 = zeros(length(y), length(x));
31 z2 = zeros(length(y), length(x));
32 z3 = zeros(length(y), length(x));
33
34 z1b = zeros(length(y), length(x));
35 z2b = zeros(length(y), length(x));
36 z3b = zeros(length(y), length(x));
37
38
39 % Fill in E-field strength of real space
40 % Wires Parallel to Y-axis
41 for i = 1:length(y)
42     z1(i,:) = lambda*C.*wire1(1)./(wire1(1).^2+(x-wire1(2)).^2);
43     z2(i,:) = lambda*C.*wire2(1)./(wire2(1).^2+(x-wire2(2)).^2);
44
45     z1b(i,:) = lambda*C.*wire1b(1)./(wire1b(1).^2+(x-wire1b(2)).^2);
46     z2b(i,:) = lambda*C.*wire2b(1)./(wire2b(1).^2+(x-wire2b(2)).^2);
47 end
48
49 % Wires Parallel to X-axis
50 for i = 1:length(x)
```

140

```matlab
51      z3(:,i) = lambda*C.*wire3(1)./(wire3(1).^2+(y-wire3(2)).^2);
52      z3b(:,i) = lambda*C.*wire3b(1)./(wire3b(1).^2+(y-wire3b(2)).^2);
53  end
54
55
56  %Combine e-field strength to see what image would look like
57  z_combined = z1 + z2 + z3;
58  z_combined_b = z1b + z2b + z3b;
59
60
61  % Plot vertical wires
62  figure
63  plot1 = surf(x,y, z1, 'EdgeColor','none','LineStyle','none');
64  hold on
65  plot2 = surf(x,y, z2, 'EdgeColor','none','LineStyle','none');
66  plot1b = surf(x,y,z1b, 'EdgeColor','none','LineStyle','none');
67  plot2b = surf(x,y,z2b, 'EdgeColor','none','LineStyle','none');
68  colormap(hot)
69  hold off
70
71  % Plot horizontal wires
72  figure
73  plot3 = surf(x, y, z3, 'EdgeColor','none','LineStyle','none');
74  colormap(copper);
75  hold on
76  plot3b = surf(x, y, z3b, 'EdgeColor','none','LineStyle','none');
77  colormap(hot);
78
79  % Plot all wires
80  figure
81  plot_combined = surf(x, y, z_combined, 'EdgeColor','none','LineStyle','...
        none');
82  hold on
83  plot_combined_b = surf(x, y, z_combined_b, 'EdgeColor','none','LineStyle',...
        'none');
84  colormap(copper(5000));
85
86  % Fill in the values of the pixel grid
87  for i = 0:39
88      for k = 0:39
89          pixels(i+1,k+1) = sum(sum(z_combined(10*i+1:10*i+10, 10*k+1:10*k...
                +10)));
90      end
91  end
92
93  pixels = pixels/100;
94
95  % Plot Mesh of Pixel Grid
96  figure
97  mesh(pixels);
98  print -painters
99
100 % Plot 3D bar graph/histogram of Pixel Grid
101 figure
102 b = bar3(pixels(12:28,12:28));
```

```matlab
103  for n=1:numel(b)
104      cdata=get(b(n),'zdata');
105      set(b(n),'cdata',cdata,'facecolor','interp','edgecolor','none')
106  end
107
108  % g = gradient(z_combined);
109  %
110  % figure
111  % surf(x, y, g, 'EdgeColor','none','LineStyle','none');
112  %
113  % [xs, ys] = find(g < 0.005 & g > -0.005);
114  % g_interest = zeros(401);
115  %
116  % for i = 1:length(xs)
117  %     g_interest(xs(i),ys(i)) = 1;
118  % end
119  %
120  % figure
121  % surf(x, y, g_interest, 'EdgeColor','none')
122
123  figure
124  temp = edge(z_combined, 'canny', .01);
125  imshow(temp)
```