Characterization of Interface State in Silicon Carbide Metal Oxide Semiconductor Capacitors

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved June 2015 by the
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August 2015

ABSTRACT

Silicon carbide (SiC) has always been considered as an excellent material for high temperature and high power devices. Since SiC is the only compound semiconductor whose native oxide is silicon dioxide (SiO_2), it puts SiC in a unique position. Although SiC metal oxide semiconductor (MOS) technology has made significant progress in recent years, there are still a number of issues to be overcome before more commercial SiC devices can enter the market. The prevailing issues surrounding SiC MOSFET devices are the low channel mobility, the low quality of the oxide layer and the high interface state density at the SiC/SiO_2 interface. Consequently, there is a need for research to be performed in order to have a better understanding of the factors causing the poor SiC/SiO_2 interface properties.

In this work, we investigated the generation lifetime in SiC materials by using the pulsed metal oxide semiconductor (MOS) capacitor method and measured the interface state density distribution at the SiC/SiO_2 interface by using the conductance measurement and the high-low frequency capacitance technique. These measurement techniques have been performed on n-type and p-type SiC MOS capacitors. In the course of our investigation, we observed 'fast interface states' at semiconductor-dielectric interfaces in SiC MOS capacitors that underwent three different interface passivation processes, such states were detected in the nitrided samples but not observed in PSG-passivated samples. This result indicate that the lack of fast states at PSG-passivated interface is one of the main reasons for higher channel mobility in PSG MOSFETs. In addition, the effect of mobile ions in the oxide on the response time of interface states has been investigated. In the last chapter we propose additional methods of investigation that can help elucidate the

origin of the particular interface states, enabling a more complete understanding of the SiC/SiO_2 material system.

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CHAPTER 1. INTRODUCTION

1.1. Silicon Carbide

In the past four decades, logic transistor scaling following Moore's Law has result in unprecedented in logic performance, with devices becoming smaller, faster and much more complicated over the years [1]. While the silicon transistor is getting close to its physical scaling limit, part of the industry's focus has been shifting towards making better high-temperature and high-power devices. For high-temperature and high-power devices, SiC is the leading contender among other wide bandgap semiconductors due to several reasons: (a) large SiC substrate wafer up to 6 inch are commercially available, (b) SiC can be homoepitaxally grown avoiding lattice mismatch, (c) it can be either doped during crystal growth or ion implantation to achieve both n- and p-type conductivity and (d) both Si- and C-face can thermally grow oxide films [2]. The fact that SiC is the only compound semiconductor which shares its native oxide SiO_2 [3] with Si makes SiC a unique semiconductor material and makes it possible to fabricate standard MOS device structures, benefitting from the experience of silicon industry.

Although there has been much progress in SiC in recent years, and successful operation of many SiC prototype devices, but only very few commercial SiC metal oxide semiconductor field effect transistor (MOSFET) have entered the market [4]. This is due to several problems of the SiC MOS devices including high interface state density (D_{it}) at the SiC-SiO_2 interface, low channel mobility, unstable threshold voltages, high fixed charge densities in the oxide, and high oxide leakage currents. In the following chapters,

some of the properties of SiC will be described, leading to the difference in electrical properties of the semiconductor-insulator interface between Si and SiC.

1.2. Polytypism

Silicon carbide exhibits a two-dimensional polymorphism called polytypism, being one of the most exciting features of silicon carbide [5]. Different polytypes have significantly different properties, thus they can be considered to be different materials.

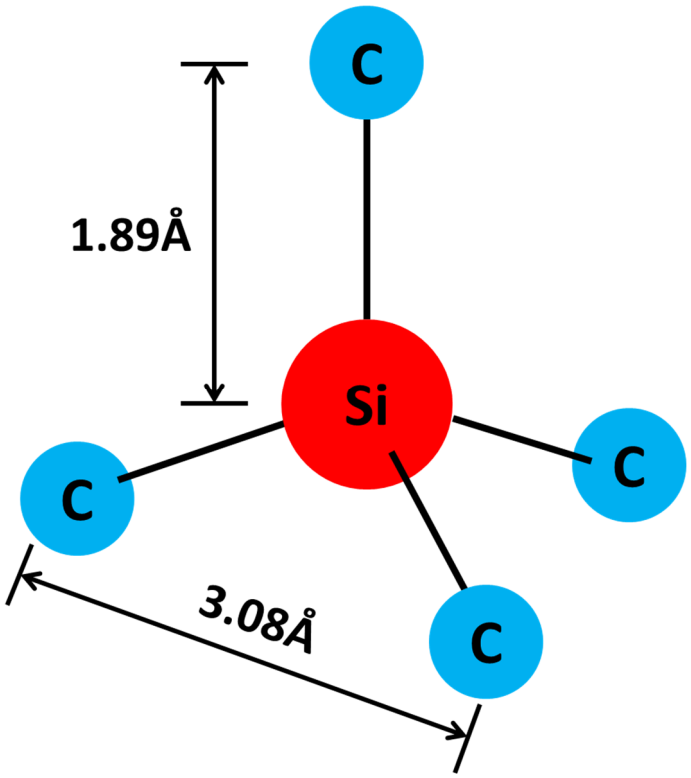


Fig. 1.1. The characteristic tetrahedron building block of SiC crystal. Four carbon atoms are covalently bonded with a silicon atom in the center. After ref. [5]

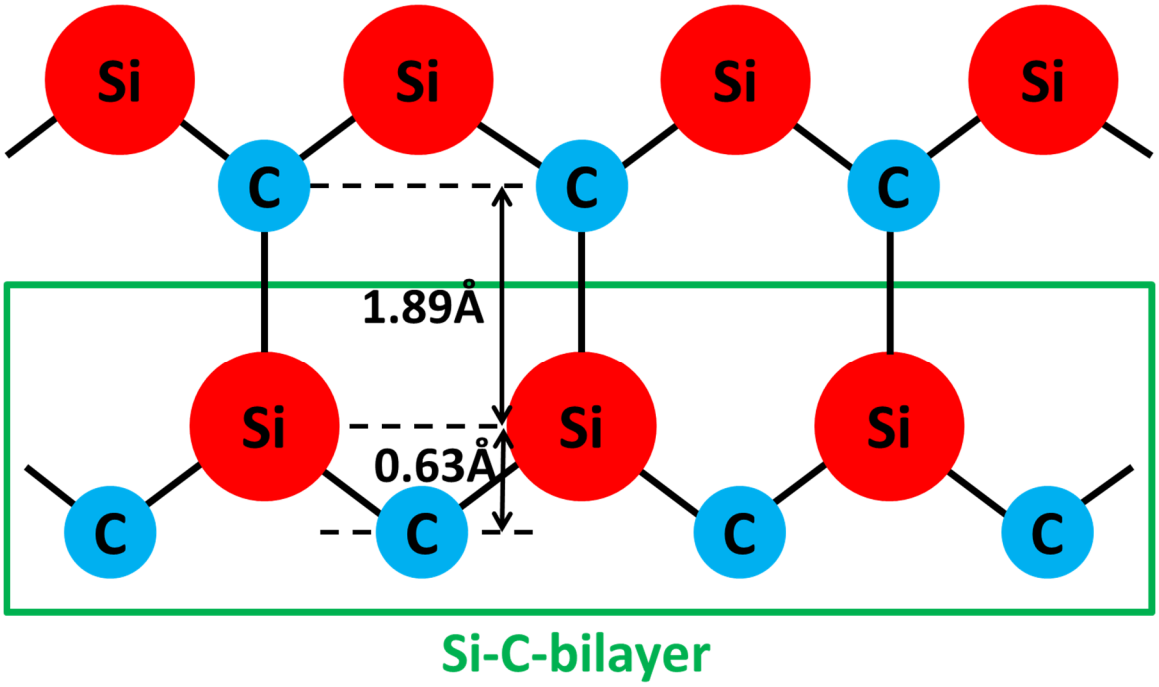


Fig. 1.2. Si-C-bilayer. After ref. [2]

Fig. 1.1 shows a tetrahedron of four carbon atoms with a silicon atom in the center, this is the basic building block of a SiC crystal [5]. Fig. 1.2 shows the layer structure of SiC, the tetrahedrally bonded silicon atoms linked to three C atoms within the bilayer and having a single bond linked to a carbon atom in layer above. The hexagonal frame of Si-C-bilayer is the basic component for the formation of polytypes [2]. Fig. 1.3 shows the same structure looking at it from above. In Fig. 1.3, the hexagonal frame is considered to be a close-packed layer of spheres which all have the same radius. The first layer which is at the very bottom is labeled as "A." The relative position of the next layer on the top of the first layer cannot be directly above the first one, it will be either in the position "B" or position "C" for energy optimization. Every subsequent next layer will have to follow the same rule.

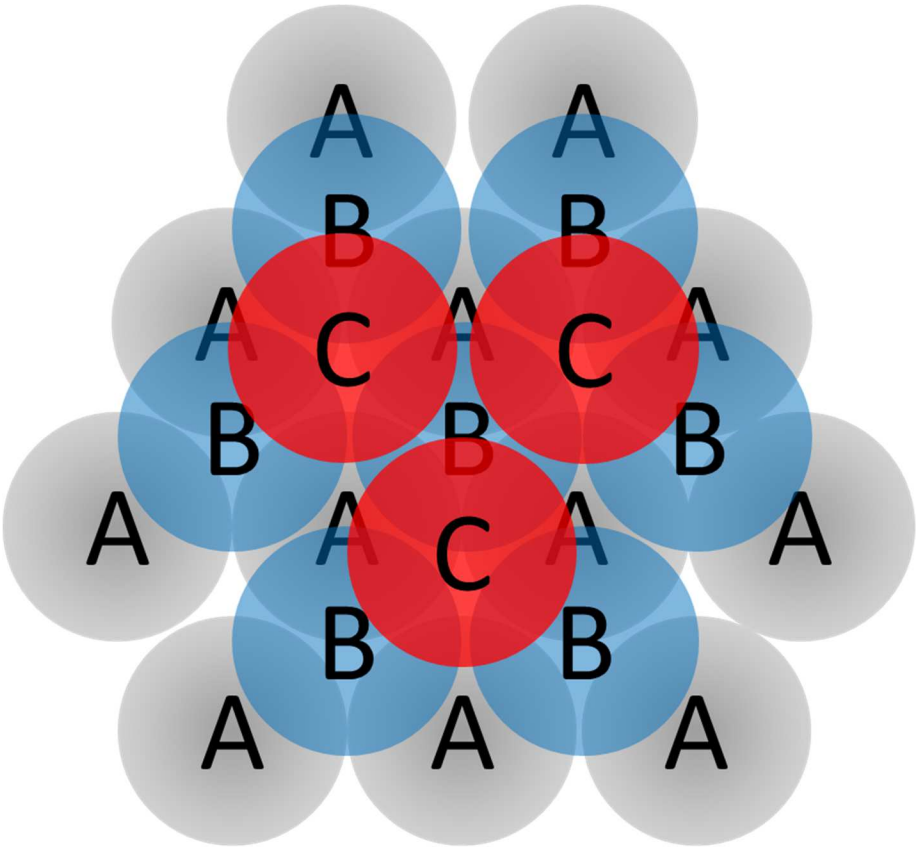


Fig. 1.3. Close packed spheres to visualize SiC stacking sequence. After ref. [5]

The Ramsdell notation is the most common naming convention used for SiC [6]. In the Ramsdell notation, the polytype's name consists of a number followed by a letter. The number represents the period of the stacking sequences and the letter represents the crystal structure which the polytype forms. For a different sequence, the structure may be cubic, hexagonal, or rhombohedral, which is denoted by C, H and R. Polytype 2H has the stacking sequence ABAB… The three important polytypes 3C-SiC, 4HSiC and 6HSiC have stacking sequences ABCABC…,ABCBABCB… and ABCACBABCACB… As mentioned above, SiC crystals never have any layer repeat due to energetic stability. Even with this restriction, infinitely many sequences are possible and in fact, over 200 have been

observed [7]. Table 1.1 listed some important material properties of 3C-SiC, 4HSiC and 6HSiC.

Material parameters	3C-SiC	4H-SiC	6H-SiC
Hexagonality	**0**	**0.33**	**0.5**
Lattice Constant (Å)	**4.34**	**a=3.073** **c=10.053**	**a=3.08** **c=15.117**
Bandgap (eV)	**2.36**	**3.2**	**3.0**
Electron Saturation Velocity (10^7cm/s)	**2.7**	**2.0**	**2.0**
Electron Mobility (cm2/V-s)	**800**	**900**	**400**
Hole Mobility(cm2/V-s)	**320**	**120**	**90**
Thermal Conductivity (W/cm-°C)	**3.6**	**3.7**	**4.9**

Table 1.1. Important material properties of 3C-SiC, 4HSiC and 6HSiC polytype. After ref. [2, 8, 9].

Each different polytype of silicon carbide has different electrical properties such as bandgap, electron saturation velocity and carrier mobility, due to its different crystal structure. Compared to 3C-SiC and 6H-SiC, the most common polytype of silicon carbide 4H-SiC has the highest mobility and the largest bandgap, this making 4H-SiC the best candidate for many applications. However, due to difficulties growing device quality 4H-SiC, in early days, 6H has been the more commonly used SiC polytype [10]. However, recently, 4H has become the dominant type.

1.3. Physical Properties

Property	Silicon	GaAs	4H-SiC	GaN
Band Gap (eV)	**1.12**	**1.42**	**3.2**	**3.44**
n_i at 300K (cm^{-3})	**10^{10}**	**1.8×10^{5}**	**$\approx10^{-8}$**	**$\approx10^{-9}$**
Electron Saturation Velocity (10^7cm/s)	**1.0**	**1.2**	**2.0**	**3.0**
Electric Breakdown Field (kV/cm)	**300**	**400**	**2200**	**5000**
Thermal Conductivity (W/cm-°C)	**1.3**	**0.55**	**3.7**	**1.3**
Electron Mobility (cm^2/V-s)	**1200**	**6500**	**800**	**1000**
Hole Mobility(cm^2/V-s)	**420**	**320**	**115**	**200**
Lattice mismatch to GaN (%)	**-17**	**-22**	**3.8**	**0**
2014 Commercial Wafer Diameter (mm)	**450**	**150**	**150**	**100**

Table1.2 Properties of common polytypes of SiC compared with Si, GaAs, and GaN; data from refs. [2, 8, 9, 11, 12]and references therein.

Compared to Si and gallium arsenide (GaAs), which have been considered the two most mature materials in the semiconductor industry, SiC possesses some exciting physical properties. The impressive physical properties of SiC include excellent high temperature tolerance, high saturation velocity, high breakdown electric field, excellent resistance to radiation and chemical attack, high thermal conductivity, a high hardness value and transparency in the optical wavelengths range [2, 9]. In the family of wide bandgap semiconductors, gallium nitride (GaN) is the most significant competing wide band gap material. Although GaN has some advantage in terms of some of the physical properties

compared to SiC, GaNis still not mature enough for the commercial market due to some technological issues. Table 1.1 listed some important physical properties of 4H-SiC in comparison with Si, GaAs and GaN.

1.4. Silicon carbide applications

The physical properties mentioned above make SiC an ideal choice for electrical device applications in many different areas, such as high temperature, high power and high frequency electronic devices. For standard commercial silicon devices, 125°C is usually specified as the upper limit for proper operation. Temperatures above 125°C are considered to be a high temperature environment for an electronic device [13, 14]. The increasing intrinsic carrier density with increasing temperature is the issue that limits the high-temperature functionality of the p-n junction in silicon devices. The intrinsic carrier density n_i of a semiconductor depends on temperature T, bandgap E_g and effective density of states N_c, N_v of the semiconductor as given by

$$n_i = (N_c \cdot N_v)^{1/2} exp\left(-\frac{E_g}{2kT}\right) \tag{1.1}$$

where k is the Boltzmann's constant.

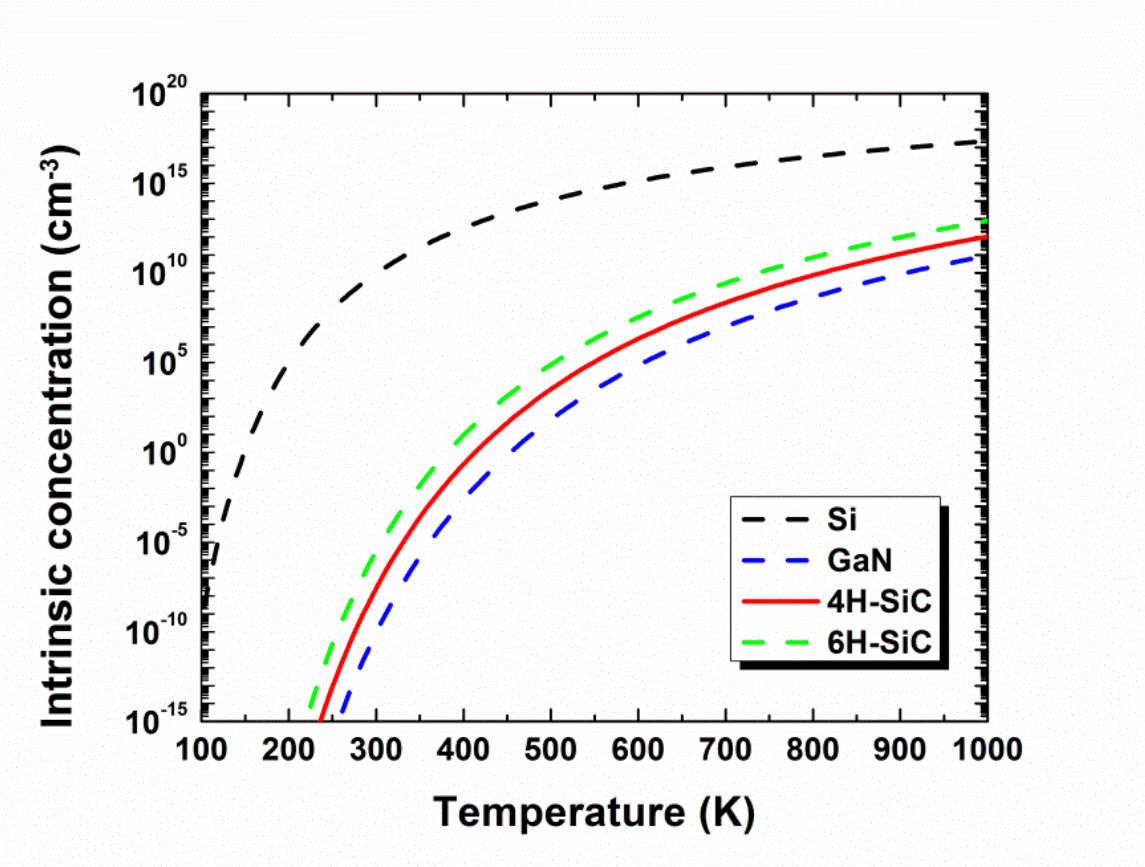


Fig. 1.4. Comparison of intrinsic carrier concentration versus temperature for Si, 4H-SiC, 4H-SiC, and GaN.

The intrinsic carrier concentration for Si, 4H-SiC, 6H-SiC and GaN as a function of temperature is shown in Fig. 1.4. For Si, when the temperature increases from room temperature to 300°C, n_i increases from the level of 10^{10} cm^{-3} to the level of 10^{16} cm^{-3} close to the dopant density level and most of the devices will not function properly. However, for 4H-SiC, at 300°C n_i is only at the level of 10^{5} cm^{-3} and thus the device can still function properly. Also, as shown in table 1.2, the thermal conductivity of SiC is

almost three times the thermal conductivity of Si. This means that SiC can remove heat much faster than Si. For the reasons mentioned above, SiC is ideal for high-temperature applications.

Being a wide bandgap semiconductor, SiC devices can be used in high-frequency applications due to their high saturation velocity and excellent thermal properties. SiC devices make an excellent high frequency oscillator. In fact, there are companies offering SiC MESFET devices for use in cellular base stations [5].

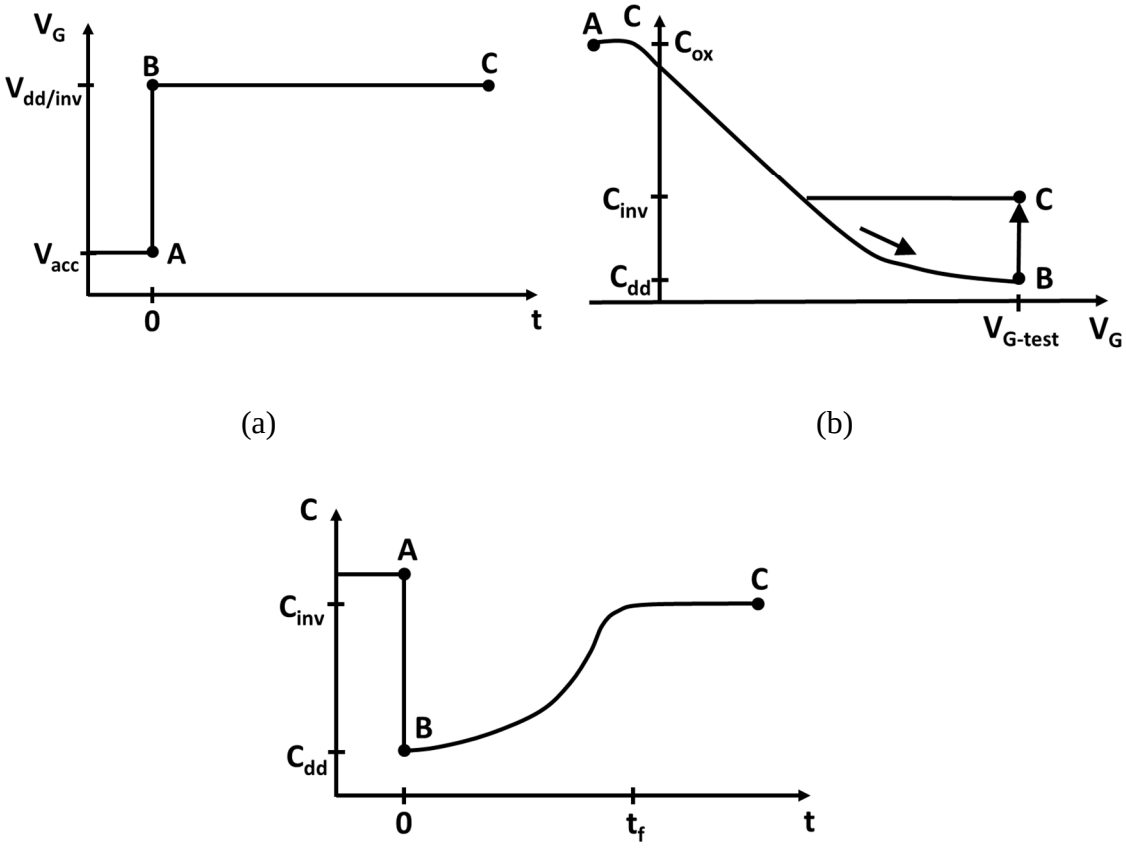
High-power applications are by far the biggest application area for SiC technology. For a power semiconductor device, the blocking voltage depends on the doping concentration. Decreasing the doping concentration will increase the blocking capability but result in an increased series resistance, leading to increased power loss. Compared to Si, SiC has a much higher breakdown electric field, thus at the same doping concentration, the SiC device blocking voltage is approximately 56.2 times higher than the blocking voltage of a Si device [15, 16]. SiC also has the highest thermal conductivity compare to any metal at room temperature [17], having the effect that it is much easier to cool down the device, eliminating the need for large size cooling system. Although SiC devices will be more expensive to manufacture compared to Si devices, the significant savings on the passive components and the cooling system will make the devices very attractive to a large customer base [5].

CHAPTER 2. CARRIER LIFETIMES IN 4H-SIC MOS CAPACITORS

2.1. Introduction

As mentioned in the last chapter, some of silicon carbide's physical properties make it an ideal material for several applications such as high-temperatures, high-frequency, and high power devices. In order to address the issues of current SiC MOS devices, it is necessary to develop a better understanding of the SiC/SiO_2 interface. Here, the silicon carbide metal-oxide-semiconductor capacitor is a powerful tool to study the SiC/SiO_2 properties. One of the properties that we can study using a SiC MOS capacitor is the generation lifetime, which we are going to discuss in this chapter. There are several technique for measuring the generation lifetime in semiconductors, one of the most powerful technique is the pulsed MOS capacitor lifetime measuring technique. This technique only needs a common MOS capacitor structure and is capable of measuring very short lifetimes. The original idea and its extensions can be found in [18-24] and a review of different method related to this technique can be found in Kang and Schroder [25]. Some work on characterizing the generation lifetime by using pulsed MOS capacitor measurement in SiC has been performed recently [26]. The pulsed MOS capacitor measurement can also be used to measure recombination lifetime. In this chapter, we are focusing on the pulsed MOS capacitor generation lifetime measurement in silicon carbide.

2.2. The Pulsed SiC MOS Capacitor



(a) (b)

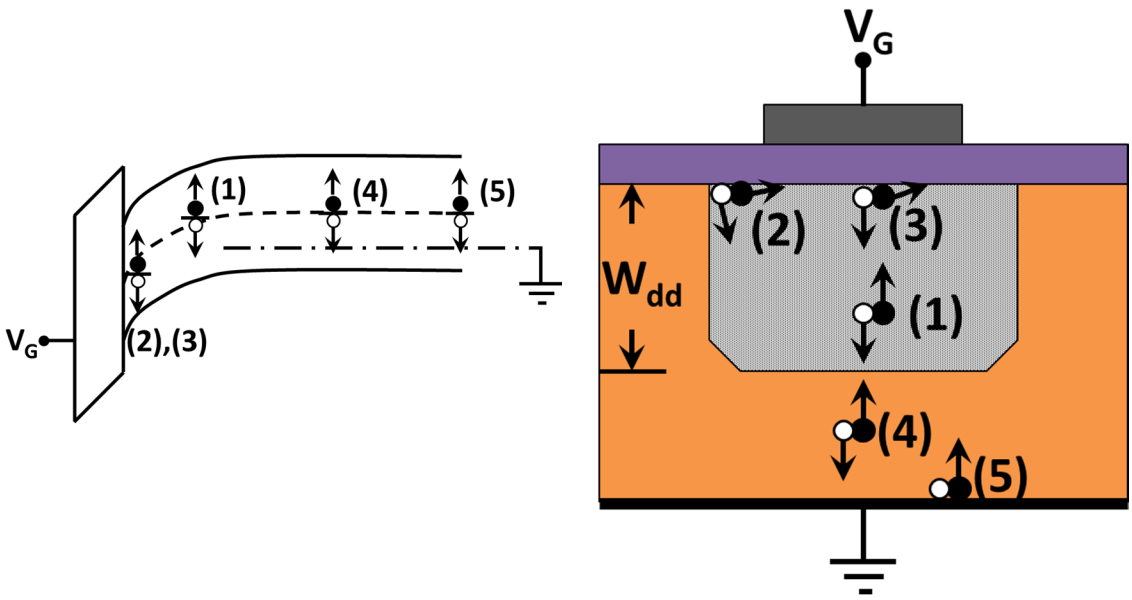
(c)

Fig. 2.1. Plot of (a) gate voltage versus time, (b) capacitance versus gate voltage and (c) capacitance versus time. After ref.[10, 27, 28].

For the pulsed MOS capacitor generation lifetime measurement, we measure the relaxation time of the MOS capacitor when it is puled to deep depletion. Fig. 2.1 illustrates the procedure of the pulsed MOS capacitor technique for a p-type substrate MOS capacitor. Before applying the voltage step, we assume the device is in accumulation and it is in equilibrium. A voltage step is applied at time 0 shown in Fig. 2.1(a), this will drive the

device from A to B in Fig. 2.1(b) and the device will be in deep depletion. In deep depletion, $np \ll n_i^2$ applies and the device is in a non-equilibrium state. Once the device in in deep depletion, thermally generated electron-hole pairs start to return the device back to equilibrium and form a full inversion layer, shown by the path B to C in Fig. 2.1(b). The recovery time t_f in Fig. 2.1(c) is determined by the thermal electron-hole pair generation mechanism.

There are several thermal generation components which are contributing to the recovery of the pulsed MOS capacitor, with every thermal generation component having a different generation rate. As shown in Fig. 2.2, the thermal generation components and its associated generation rates are (1) bulk generation in the space charge region characterized by the generation lifetime τ_g, (2) lateral surface space charge region generation adjacent to the gate characterized by the surface generation velocity s_g, (3) surface space charge region generation under the gate characterized by the surface generation velocity s'_g, (4) bulk generation in the quasi-neutral region characterized by the minority carrier diffusion length L_n and (5) surface generation at the back of the substrate characterized by the surface generation velocity s_c [28]. In our analysis, we assume that the substrate is thick enough that generation at the back contact is negligible. It is also assumed that surface generation adjacent to the gate and bulk generation in the space charge region depends linearly on the space-charge region width $W - W_{inv}$ and surface generation below the gate and bulk generation in the quasi-neutral region are assumed to be independent of this width.



(a) (b)

Fig. 2.2. Generation components described in the text which contribute to the recovery of the pulsed MOS-C depicted (a) on a band diagram and (b) in the device. After ref.[10, 27, 28].

For a pulsed MOS capacitor, the gate voltage is constant during the relaxation time, the capacitance change to the change in charge is [27]

$$\frac{\mathrm{d}Q_n}{\mathrm{d}t} = \frac{qK_S\epsilon_0 C_{ox} N_A}{C^3}\frac{\mathrm{d}C}{\mathrm{d}t} \tag{2.1}$$

where dQ_n/dt is the thermal generation rate in Fig. 2.2

$$\frac{\mathrm{d}Q_n}{\mathrm{d}t} = -\frac{qn_iW}{\tau_g} - \frac{qn_is_gA_S}{A_G} - qn_is'_g - \frac{qn_i^2D_n}{N_AL'_n} \tag{2.2}$$

where the area of the lateral space charge region $A_S = 2\pi rW,$ the gate area $A_G = 2\pi r$ and L'_n is the effective diffusion length. If we only consider the space charge region generation rates

$$\frac{\mathrm{d}Q_{n,scr}}{\mathrm{d}t} = -\frac{qn_i(W - W_{inv})}{\tau_{g,eff}} \tag{2.3}$$

where $W_{inv} = (4K_s\varepsilon_0\varphi_F/qN_A)^{1/2}$ and $\tau_{g,eff}$ is the effective generation rate in the space charge region. Also, the effective surface generation velocity is

$$s_{eff=}s'_g + \frac{n_iD_n}{N_AL'_n} \tag{2.4}$$

Eq. 2.2 can be rewritten as

$$\frac{\mathrm{d}Q_n}{\mathrm{d}t} = -qn_i\frac{W - W_{inv}}{\tau_{g,eff}} - qn_is_{g,eff} \tag{2.5}$$

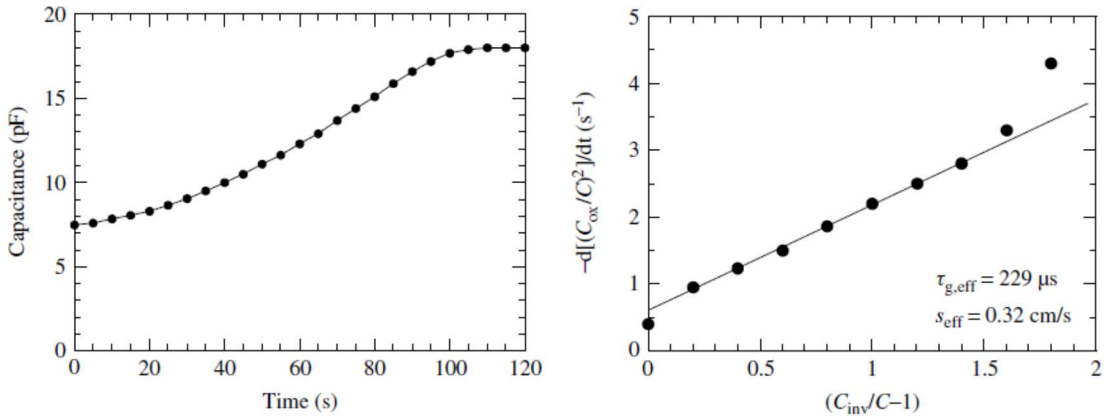
The space charge region width W as a function of capacitance C is

$$\mathrm{W} = K_s\varepsilon_0\frac{C_{ox} - C}{C_{ox}C} \tag{2.6}$$

By combining Eqns. (2.2), (2.5) and (2.6), we can get

$$-\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{C_{ox}}{C}\right)^2 = \frac{2n_i C_{ox}}{\tau_{g,eff} N_A C_{inv}}\left(\frac{C_{inv}}{C} - 1\right) + \frac{2K_{ox} n_i s_{g,eff}}{K_S t_{ox} N_A} \qquad (2.7)$$

Based on Eq. (2.7), we can plot $-\mathrm{d}/\mathrm{d}t\,(C_{ox}/C)^2$ versus $(C_{inv}/C - 1)$. This is the well-known Zerbst plot. From the slope of the Zerbst plot $2n_i C_{ox}/\tau_{g,eff} N_A C_{inv}$ we can extract the effective generation rate $\tau_{g,eff}$ and from the extrapolated intercept $2K_{ox} n_i s_{g,eff}/K_S t_{ox} N_A$ we can extract the effective surface generation velocity s_{eff}. In our analysis, we neglect several details of this technique, more complete versions are available in refs. [25] and [27]. An experimental room-temperature C-t curve is shown in Fig. 2.3(a) and the corresponding Zerbst plot, is shown in Fig. 2.3(b) [27].



(a) (b)

Fig. 2.3. (a) Typical *C-t* transients during inversion layer formation and (b) the resulting Zerbst plot [27].

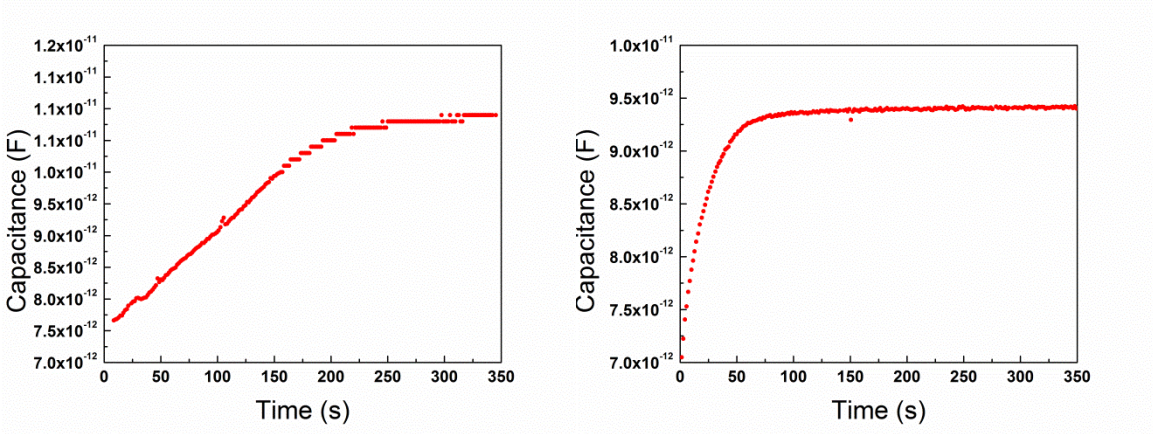
2.3. Experimental Details, Results and Discussion

For the research presented in this chapters, we used 4H-SiC n-type and p-type samples grown by Cree Inc.. Both n-type and p-type samples are squares with approximately 5 mm sides, the n-type samples have a 10 μm epilayer doped to about 10^{16} cm^{-3} and the p-type samples have a 5.2 μm epilayer doped to about $6.2x10^{15}$ cm^{-3}. The samples were oxidized by Tami Isaacs-Smith and Prof. John Williams of the Auburn University Physics Department. The oxide thicknesses are 50 nm and 100 nm for different samples. For each sample, there are three sizes of circular contacts of diameters 145, 298 and 599 μm.

We should note that lifetime measurements with the pulsed MOS-C technique on a Si/SiO_2 device are generally made at room temperature. However, compared to Si, SiC has a much lower intrinsic carrier concentration. The intrinsic carrierconcentration of SiC at 25 °C is only about 10^{-8} cm^{-3}, about 18 orders of magnitude lower than Si [8]. Thus, for making lifetime measurements with the pulsed MOS-C technique on a SiC/SiO_2 device, we have to raise the temperature in order to obtain reasonable recovery times.

In order to reduce series resistance, all the samples were cleaned with Acetone and IPA. After cleaning, the samples were attached to aluminum plates with silver paste. The aluminum plates were polished with sand paper on both sides and cleaned before attaching the samples. All the measurements were performed in an electrically isolated probe station with a maximum temperature of 400 °C. The capacitance was measured with an Agilent 4284 LCR meter and current measurements were made using an Agilent 4155C semiconductor parameter analyzer. Before making the C-t measurements, C-V measurements were done at room temperature for all the devices to analyze them.

For the C-t measurement, the SiC samples are first heated to and stabilized at 300°C, N_2 gas was flowing over the sample during the whole time. The C-t measurements are done in deep depletion of the capacitor. At 300°C, the recovery time of SiC capacitors is longer than 30min, in order to measure the recovery time, we heated the samples to 400°C for the C-t measurement. The devices we chose to measure are the ones with lower flat-band voltage shift ΔV_{fb} determined from the C-V measurements.

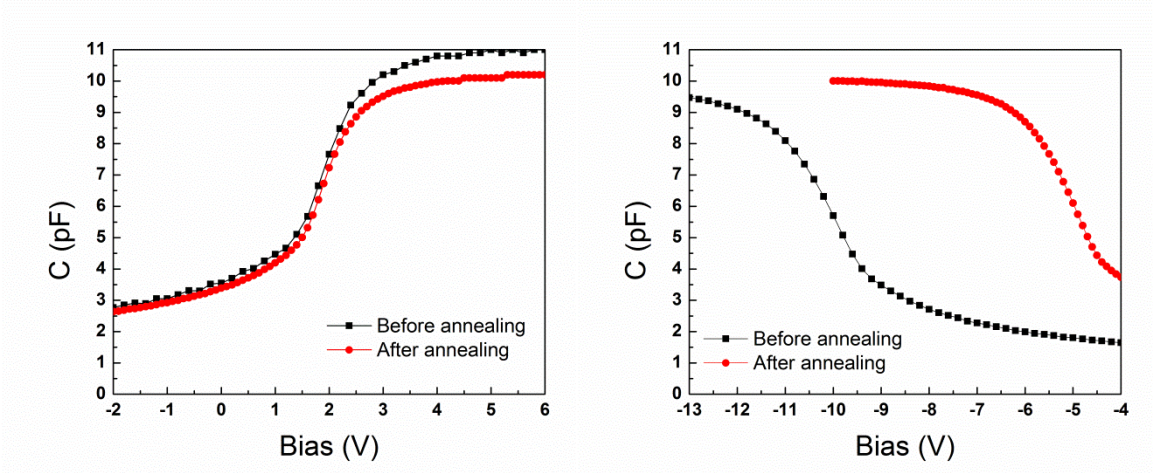


(a) (b)

Fig. 2.4. C-t response for (a) n-type and (b) p-type SiC MOS-C in deep depletion at 400°C.

Fig. 2.4 shows the C-t response for (a) n-type and (b) p-type SiC MOS-C at 400°C, and the recovery time for the p-type devices is about 4 times shorter than for n-type devices. The shorter recovery time is due to the high surface generation; the surface generation dominated the recovery process. This high surface generation is due to high interface state density and other defects in the oxide or at the oxide/semiconductor interface. Surface

generation can cause a highly nonlinear Zerbst plot [22] and is difficult to indicate bulk lifetime with such high surface generation. Hence, there is interest in the interface states at the SiC/SiO_2 interface, how high is the interface state density and how to extract it. More details about interface states at the SiC/SiO_2 interface will be discussed in the next chapter.



(a) (b)

Fig. 2.5. Comparison of C-V curves for (a) n-type and (b) p-type SiC MOS-C before and after annealing. T=400^{o}C.

It was also be found that some devices behave differently at 400°C than at room temperature. Fig 2.5 shows the changes of the C-V curves for both n-type and be type samples after heating to 400°C and cooling to room temperature, the ΔV_{fb} of the p-type device decreased dramatically, but the n-type devices show little or no decrease on ΔV_{fb}. For samples which were heated up to 400°C and cooled to room temperature several times, ΔV_{fb} decreases each time it is heated up and cooled. The ΔV_{fb} decrease is due to the high temperature that anneals the interface states and oxide charges of the device. Fig. 2.6 shows

the C-t response for p-type SiC MOS-C after annealing. The surface generation is much lower than before annealing, but the surface generation still dominates at the beginning of the measurement before significant inversion charge has been generated. Further treatment has to be done to the device in order to lower the defects and determine the bulk lifetime form the pulsed MOS capacitor lifetime measuring technique.

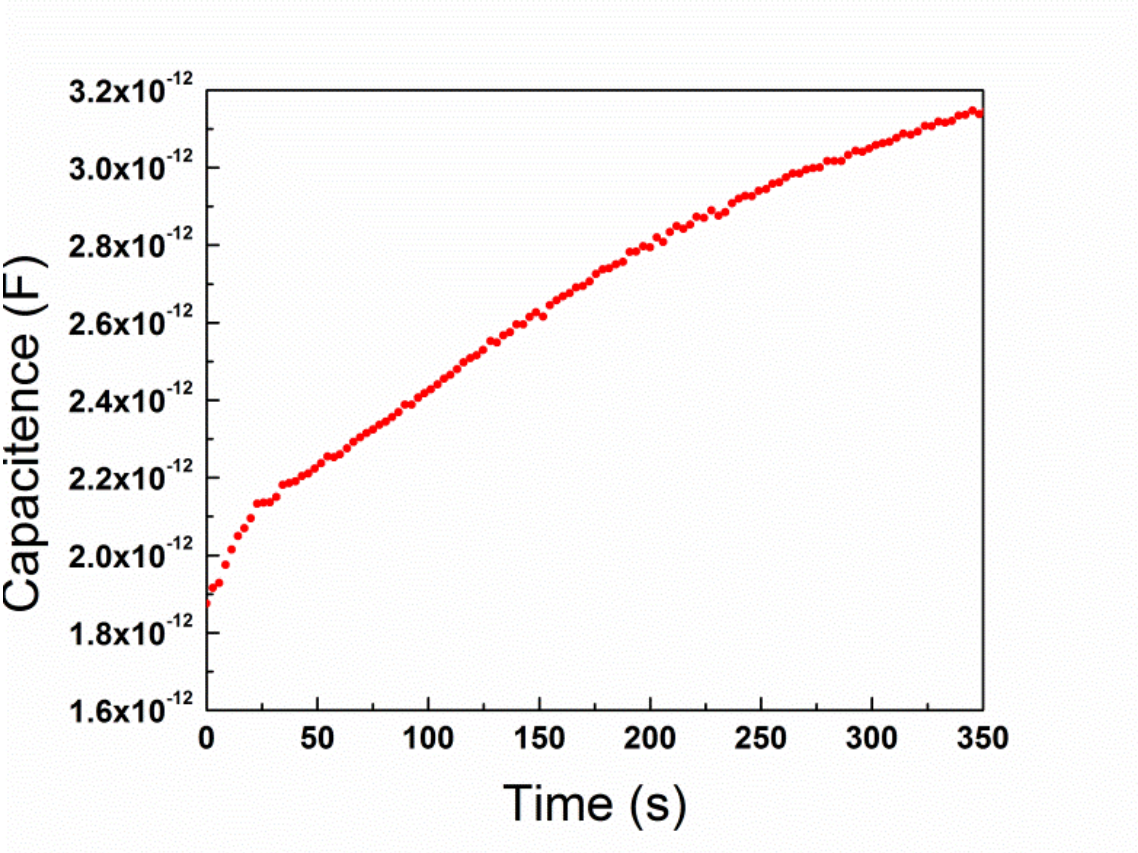


Fig. 2.6. C-t response for p-type SiC MOS-C after heated up to 400°C and cooled down to room temperature 3 times.

CHAPTER 3. INTERFACE PASSIVATION FOR SILICON DIOXIDE LAYERS ON SILICON CARBIDE

3.1. Introduction

As mentioned in the first chapter, silicon carbide has the unique advantage in MOS technology compared to other wide-bandgap materials that SiO_2 can be grown as a native oxide by using thermal oxidation techniques similar to those used to grow SiO_2 on Si. Because of that, a major goal of the SiC research and development community is the development of SiC MOSFETs. However, in early days, the inversion channel mobility of 4H-MOSFETs has been surprisingly low, less than 10 cm^2/V s, which is approximately two orders of magnitude lower than the bulk mobility. It has been suggested the low inversion channel mobility of 4H-MOSFETs is due to the large number of interfacial defects at the SiO_2/SiC interface [29]. A lot of research efforts are focused on how to passivate the SiO_2/4H-SiC interface, and a variety of passivation methods has been proposed. In this chapter, we discuss recent passivation techniques for SiO_2/SiC interface passivation.

3.2. Nitrogen Passivation Annealing

For passivating the SiO_2/4H-SiC interface, efforts have been focused on oxidation procedures and post-oxidation anneals in various ambients such as NO, N_2O, NH_3 and H_2 [30]. Because of its ability to passivate Si dangling bonds at the SiO_2/Si interface, hydrogen has received much attention early on. However, introducing nitrogen at the SiO_2/4H-SiC interface by using post-oxidation anneals in NO and N_2O has rendered the best passivation

results [30]. It has been reported that effective channel mobilities are approaching 80 cm^2/V s for SiC MOSFETs by nitridation using NO and N_2O [31]. The interface trap density (D_{it}) near the conduction band edge reduces from larger than $10^{13} cm^{-2} eV^{-1}$ to around $10^{12} cm^{-2} eV^{-1}$ following nitidation [30].

NO passivation anneal is usually carried out at 1175°C for 2 hours at a flow rate of 0.5 liters/min [30]. Fig. 3.1 shows the interface trap density under different passivation conditions, the interface trap density is extracted by high-low frequency capacitance method using MOS capacitors. Details of the high-low frequency capacitance method will be explained in the next chapter.

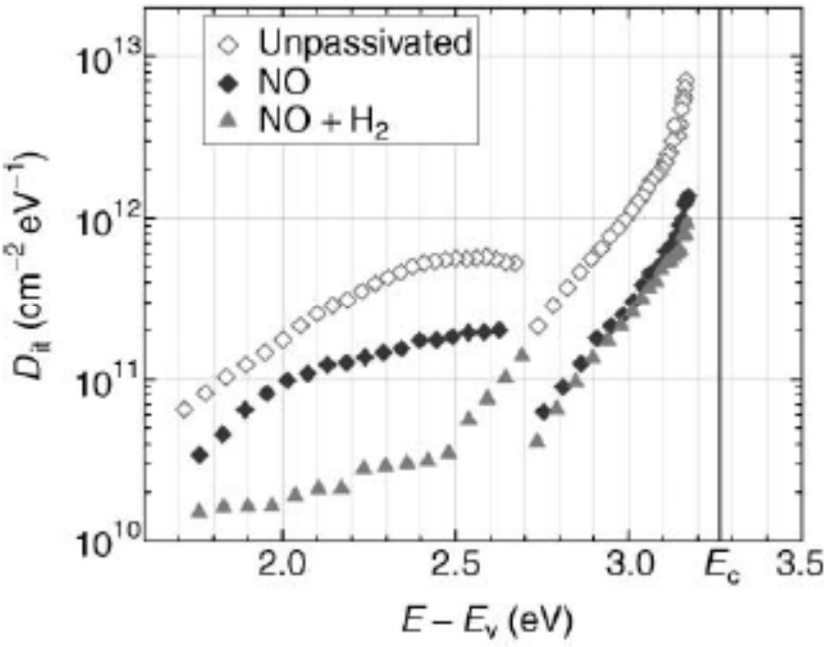


Fig. 3.1. Interface trap density in the upper 4H-CiC bandgap for unpassivated samples and sample passivated with NO and NO+H_2. [30]

As shown in Fig. 3.1, D_{it} measured on the passivatied samples has been reduced by about an order of magnitude compare to the unpassivated samples. The D_{it} can be further reduced by annealing the NO-passivated oxide in hydrogen atomsphere. Also, shown in Fig. 3.2, the effective channel mobility of passivated n-channel MOSFET samples was usually an order of magnitude higher compare to the unpassivated samples. Samples fabricated using the $NO+H_2$ annealing process show 25% to 30% higher Field-effect mobilities than samples using only the NO annealing process [30].

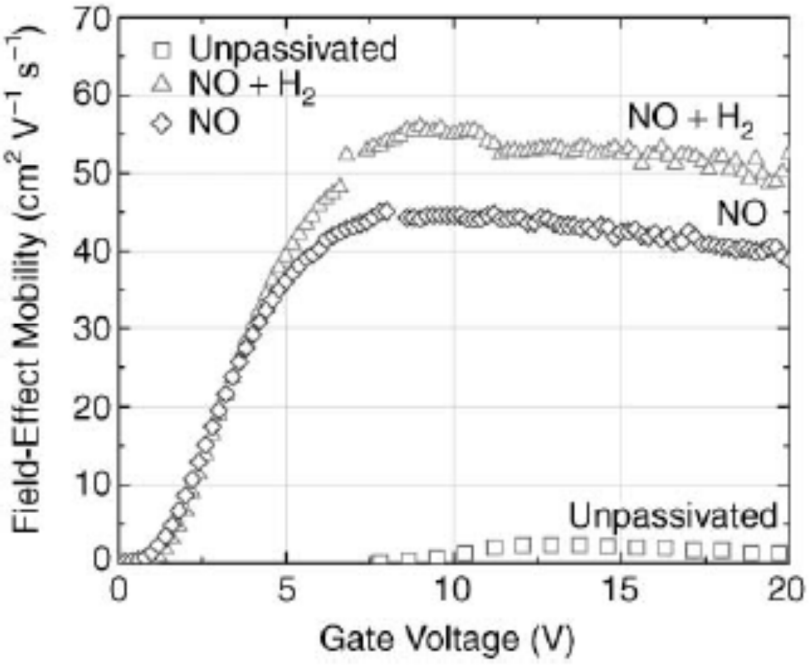


Fig. 3.2. Field-effect mobility before and after passivation for lateral MOSFETs. [30]

During the high-temperature NO passivation annealing process, additional oxide growth will occur and new defects will be generated by this unwanted oxidation. The trap density may not be lowered further due to the competition between defect passivation by

NO and defect generation by unwanted oxidation. This might be a limitation for the NO passivation annealing process. By using a proprietary process that introduces nitrogen without unwanted oxidation, lower trap density and higher channel mobility has been reported by Cree Inc. [30].

3.3. Phosphorus-Doped Gate Oxide

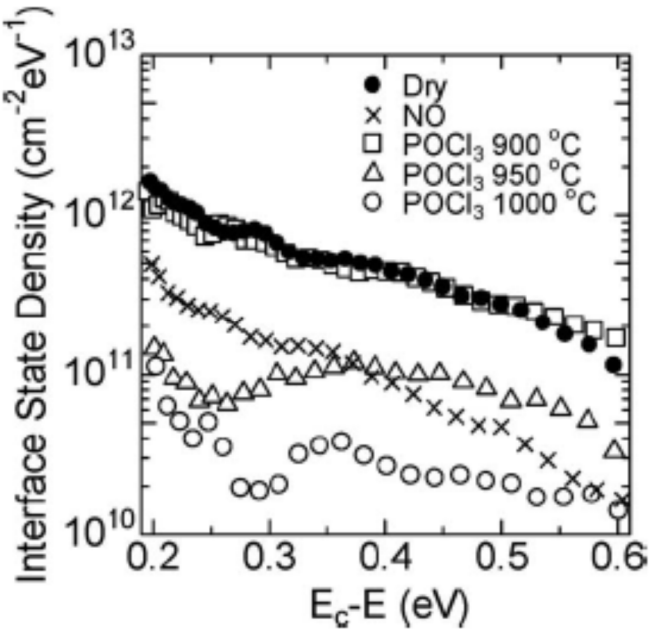


Fig. 3.3. Interface trap density in the upper 4H-CiC bandgap for unpassivated samples, NO passivated samples and PSG passivated samples under different passivation temperature [32].

Recently, Okamoto proposed a new technique for fabricating 4H-SiC MOSFETs with high inversion channel mobility [32]. In this technique, P atoms were incorporated into the

SiO_2 side of the interface by using phosphoryl chloride ($POCl_3$) during post-oxidation annealing.

For this technique, an oxide layer on 4H-SiC is formed by dry oxidation at 1200°C. Then, the samples were annealed in a gas mixture of $POCl_3$, O_2 and N_2 for 10 minute at 900°C, 950°C and 1000°C. Following this, the samples were annealed for 30 minute in N_2 at the same temperature. The oxide thickness is nearly unchanged during the annealing process. The P-doped oxide layer at the interface has a dielectric constant around 3.8 to 4.1, which is close to the dielectric constant for SiO_2 (3.9). After the contact metal deposition, the samples were annealed again for 30 minute in N_2 at 400°C [32].

Fig. 3.3 shows the interface trap density under different PSG passivation temperature conditions, compared to samples with NO passivation and without any passivation. The interface trap density has been extracted by the high-low frequency capacitance method using MOS capacitors. As shown in Fig. 3.3, the D_{it} value does not change for a PSG passivation anneal at 900°C, but the D_{it} value will decrease if the annealing temperature is 950°C or higher. The D_{it} value is smaller compared to NO passivated samples when the samples were annealed at 1000°C.

Fig. 3.4 shows the field-effect mobility of 4H-SiC MOSFETs fabricated with PSG passivation annealed at 1000°C compare with 4H-SiC MOSFETs fabricated with NO passivation annealing and unpassivated 4H-SiC MOSFETs. As shown in Fig. 3.4, the peak field-effect mobility is significantly higher than for samples with NO passivation annealing or those without any annealing.

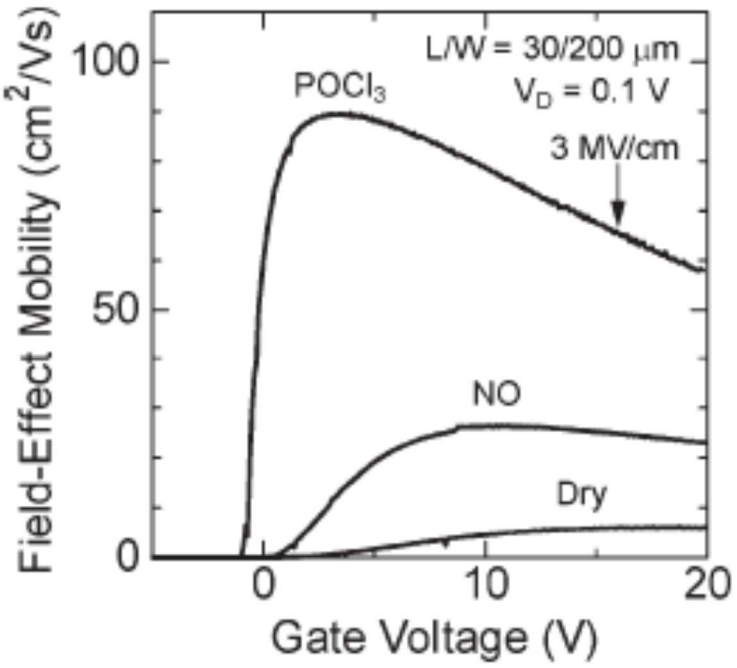


Fig. 3.4. Field-effect mobility for unpassivated samples, NO passivated samples and PSG passivated samples.[32]

3.4. Nitrogen Plasma Annealing

As mentioned earlier in this chapter, introducing nitrogen at the interface by using NO passivation annealing results in lower D_{it} and a higher effective channel mobility improving the devices sufficiently for commercialization. However, there are limitations to NO passivation annealing due to the unwanted oxidation during the annealing process. Therefore, a process which could introduce more nitrogen at the interface and minimized the unwanted oxidation is needed to decrease the D_{it} and increase effective channel mobility.

Recent reports show that using nitrogen plasma anneal to create a nitrogen containing layer at the SiO_2/SiC interface will reduce the D_{it} of MOS capacitor [33]. The

nitrogen plasma annealing process was expected to improve the device performance for the following reasons: First, the unwanted oxidation can be reduced to minimum due to lack of oxygen in the nitrogen plasma. Second, carbon being interstitially injected into the SiC during oxidation, suspected to inhibit MOSFET carrier mobility, is correspondingly reduced [34]. Third, and most important, it can obtain higher N interface coverage. However, it has been reported that increasing the N interface coverage will potentially create “fast traps” [35].

The nitrogen plasma process flow is the following: A thin thermal oxide (~15nm) was first grown in O_2 ambient at 1150°C in atmospheric pressure, follow by Ar post-oxidation annealing for 30 minutes. Then, the samples were annealed by nitrogen plasma passivation for various hours in a different furnace. The nitrogen plasma passivation was performed under the condition of 1160°C, 3.0/min N_2 flow, 2.3 torr of pressure and 2kW of microwave power. This was followed by a 2 hour plasma recovery anneal at 1160°C in nitrogen ambient under atmospheric pressure. After the plasma treatment, another layer if SiO_2 was deposited by LPCVD at 700°C, 0.5 torr, following by a 2 hour densification anneal at 850°C in nitrogen.

CHAPTER 4. INTERFACE STATES AT THE SIC/SiO_2 INTERFACE

4.1. Interface States

It is often said that the real magic of silicon technology lies not in the silicon crystalline material but in silicon dioxide and its interface with silicon [36]. Silicon dioxide is often treated as an ideal insulator, where there are no unwanted charges and states at the interface of silicon and silicon dioxide. But in reality, the silicon/silicon dioxide interface and the bulk silicon dioxide in a device are far from electrically neutral. This may be caused by (1) interface trap charges at the silicon/silicon dioxide interface, (2) fixed charges, (3) oxide trapped charges and (4) mobile ionic charges trapped within the oxide itself, which are often created during the fabrication process. These four general types of charges are shown in Fig. 4.1. For a device which has a semiconductor/oxide interface, the electronic properties are very sensitive to the quantity of the interface state and how it distributed in the semiconductor bandgap.[36]

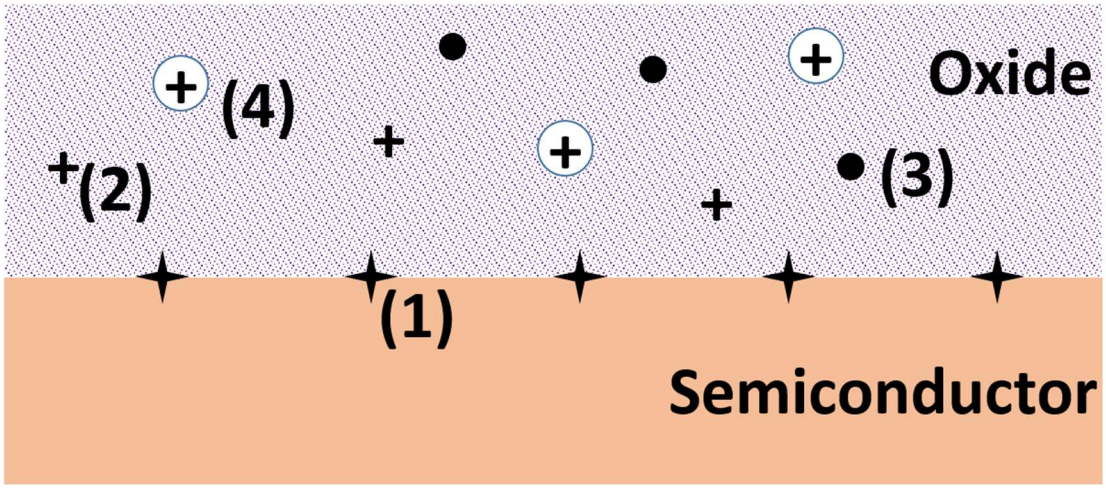


Fig. 4.1. Charges and their locations in an oxide/semiconductor cross sections.

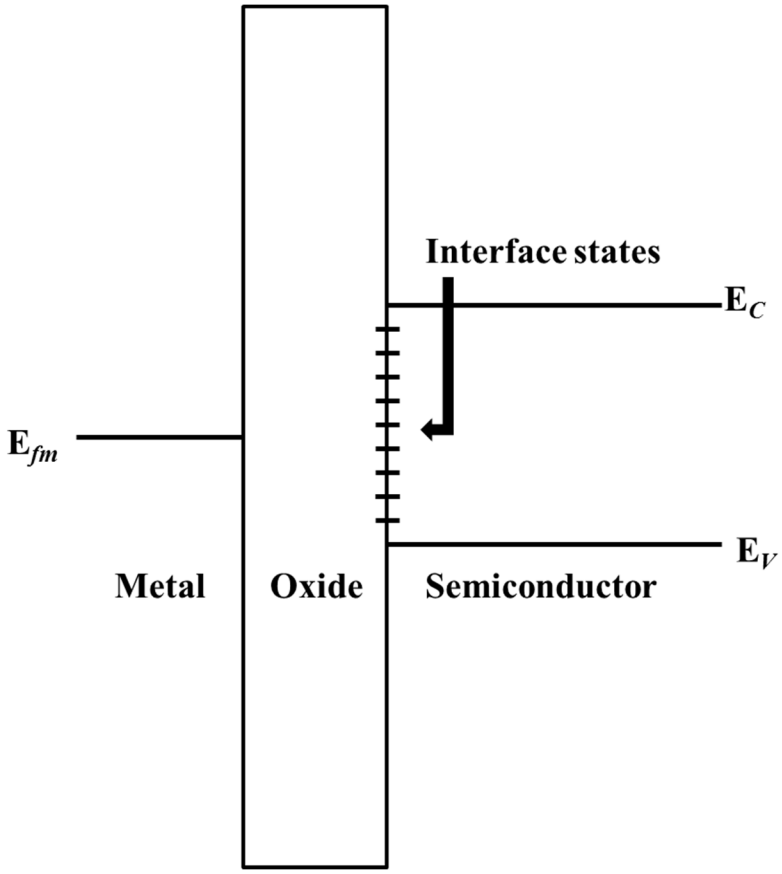


Fig. 4.2. Energy-band diagram of a MOS structure, depicting the distribution of interface states in the bandgap of the semiconductor at the oxide/semiconductor interface.

As shown in Fig. 4.1 and Fig. 4.2, interface states are located at or very close to the oxide/semiconductor interface and have an energy distribution within the bandgap and even extend into the conduction and valence band of the semiconductor. The interface states are attributed to dangling bonds, vacancies, atom-like bonds and anti-site defects ant the oxide/semiconductor interface. When electrons or holes are trapped in these interface states, they will act like positive or negative charges at the interface. Just like the impurity energy states in the bulk of a semiconductor, the probability for an interface state to be

occupied by an electron or hole depends on the energetic location of the interface state relative to the Fermi level at the interface. As shown in Fig. 4.2, the energetic location of the interface states are fixed relative to the semiconductor band edges at the interface, so when the surface potential changes, which means the Fermi level at the interface changes, the interface states occupation probability by electron or holes will also changes.

Presumably, there are two types of interface states, donor states and acceptor states. A donor state is neutral when occupied by an electron and becomes positively charged when empty. On the other hand, an acceptor state is neutral when empty and becomes negatively charged when accepting an electron. The distribution function (occupancy) for donor states is

$$F_{SD}(E_d) = \frac{1}{1 + 2\exp[\frac{E_F - E_d}{kT}]} \tag{4.1}$$

and the distribution function (occupancy) for accepter states is

$$F_{SA}(E_a) = \frac{1}{1 + 4\exp[\frac{E_a - E_F}{kT}]} \tag{4.2}$$

where E_d is the energy of the donor state, and E_a is the energy of the acceptor state.

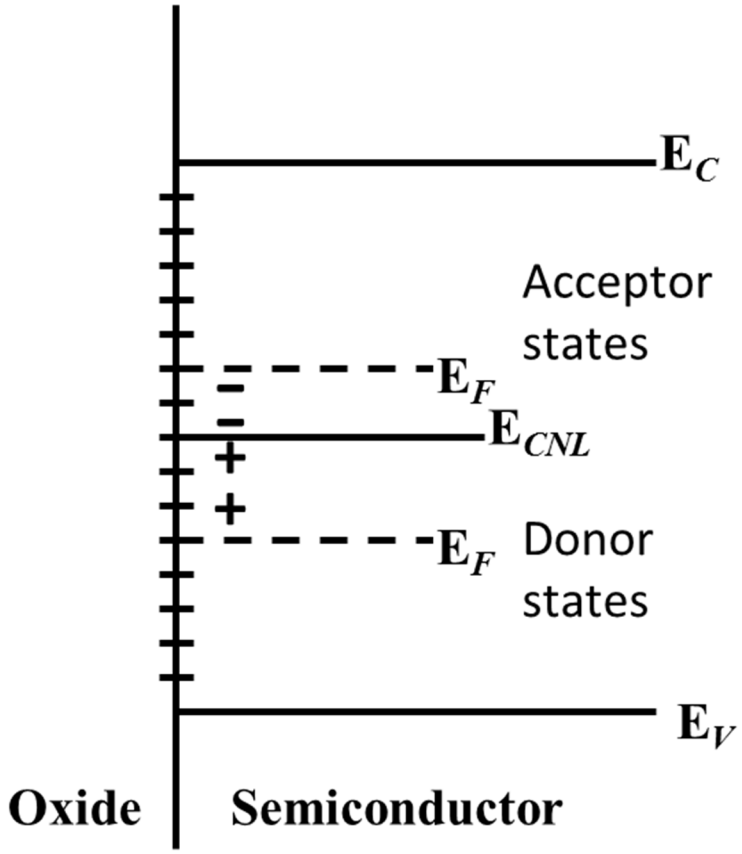


Fig. 4.3. General interface states system consisting of both donor and acceptor states. This is often expressed by an equivalent distribution with a charge-neutrality level E_{CNL} above which the states are acceptor type and below which they are donor type. When E_F is above (below) E_{CNL}, net charge is –(+).

For a given interface, it is usually considered that it has both donor states and acceptor states. The interface state density (D_{it}) is the most common unit to quantify interface states, and it is convenient to express the interface states using an equivalent interface state density (D_{it}) energy distribution, associated with the energy band diagram. In Fig. 4.3, there is an energy level called the charge-neutrality level E_{CNL}. Interface states which energy levels are above the E_{CNL} are to be considered as acceptor states, since when the Fermi level E_F

at the interface is above E_{CNL}, the states below E_F are occupied by electrons and negatively charged. Interface states which energy levels are below the E_{CNL} are to be considered as acceptor states, since when the Fermi level E_F is below E_{CNL}, the states above E_F are empty and positively charged. When E_F is right at E_{CNL} at the interface, all the states are neutral.

By assuming that the occupancy of an electron for a trap takes a value of 0 when above E_F and 1 when below E_F at room temperature, we can calculate the concentration of trapped charge at the interface Q_{it} by:

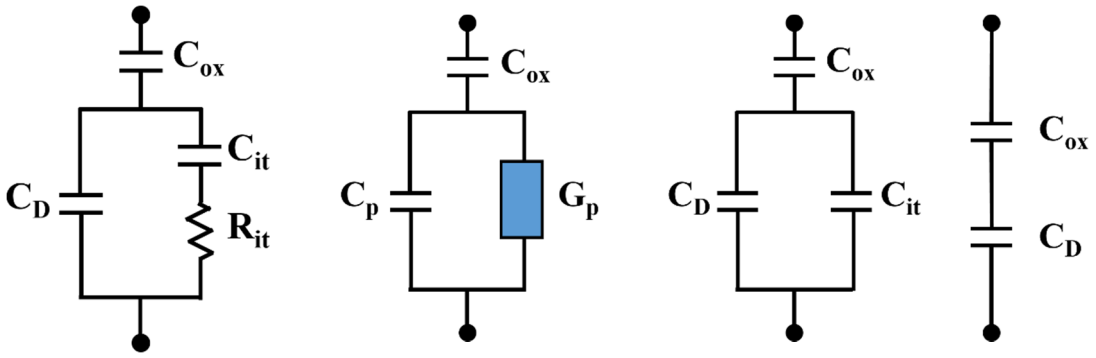
$$\begin{aligned} Q_{it} &= -q \int_{E_{CNL}}^{E_F} D_{it} dE \qquad E_F \text{ above } E_{CNL} \\ &= q \int_{E_F}^{E_{CNL}} D_{it} dE \qquad E_F \text{ below } E_{CNL} \end{aligned} \tag{4.3}$$

The unit of Q_{it} is C/cm^2. Also, the interface state density D_{it} are distributed across the energy bandgap at the interface and its distribution can be expressed as:

$$D_{it} = \frac{1}{q} \frac{dQ_{it}}{dE} \qquad \text{\# of traps/cm}^2\text{-eV} \tag{4.4}$$

In Eq. 4.4, the change in Q_{it} is determined by the movement of E_F at the surface, in other words, changes in surface potential ϕ_s can be used to determine D_{it}. More details will be discussed in the next section [37]. When applying a voltage to the gate of an MOS structure, ϕ_s will be changed by the bias, thereby the charges at the interface will also be changed. As mentioned above, the oxide/semiconductor interface states will be positively charged, negatively charged or neutral, depending on the location of the Fermi level at the

interface. The charge balance between Q_{it} and the space charge Q_{SC} in the space-charge region will determine the band bending within the semiconductor.



(a) (b) (c) (d)

Fig. 4.4. (a) (b) Equivalent circuits including interface state effects, C_{it} and R_{it} [38]. (c) Low-frequency limit. (d) High-frequency limit. After ref. [27]

For Silicon, the interface state density can have a value as high as 10^{14} cm^{-2} due the atom area density at the interface. The distribution of the interface states typically has an energy range from 0.1 eV to the entire bandgap, this makes the interface state density per unit energy as high as 10^{15} cm^{-2} eV^{-1}. When the interface has such high D_{it}, the Fermi level E_F will be pinned at a certain energy level. This effect is known as Fermi level pinning. Fermi level pinning depends on the energy distribution of the interface states. E_F is usually pinned very close to the charge-neutrality level E_{CNL}. The further E_F deviates from E_{CNL}, more interface states will be charged. As a consequence, the space charges within the semiconductor will not be able to compensate the high value of interface state charges at the interface. Even with changing the external electric field by changing the gate voltage,

E_F can only shift for a small amount within the band of interface states with respect to the charge-neutrality level [39].

As the energy location of the Fermi level E_F changes at the oxide/semiconductor interface, the interface trap charge density, Q_{it} will also change. Such increase or decrease of charges at the interface will affect the MOS capacitance and modify the ideal MOS curve. Fig. 4.4 shows the basic equivalent circuit that incorporates the effect of the interface states [38]. In Fig 4.4 (a), C_{ox} represents the oxide capacitance and C_D represents the space-charge region capacitance in the semiconductor in a MOS device. The capacitance and resistance associated with interface states are represented by C_{it} and R_{it}, C_{it} and R_{it} are also energy dependent. $C_{it}R_{it}$ product will define the interface trap life time τ_{it} that can be defined by the product of C_{it} and R_{it}. By using the trap life-time τ_{it}, the frequency behavior of the interface states can be determined. Fig. 4.4 (a) can be converted into an equivalent circuit as shown in Fig. 4.4 (b), C_p and G_p represent the frequency-dependent capacitance and the frequency-dependent conductance. C_p and G_p can be calculated from

$$C_p = C_D + \frac{C_{it}}{1 + \omega^2 \tau_{it}^2} \tag{4.5}$$

and

$$\frac{G_p}{\omega} = \frac{C_{it}\omega\tau_{it}}{1 + \omega^2 \tau_{it}^2} \tag{4.6}$$

Also, the equivalent circuits for the low-frequency and high-frequency limits are shown in Fig. 4.4 (c) and Fig. 4.4 (d). As shown in Fig. 4.4 (c), for the low-frequency limit, R_{it} is

set to zero, and C_D is parallel to C_{it}. As shown in Fig. 4.4 (d), for the high-frequency limit, the C_{it} –R_{it} branch is ignored or open. We assume that the low-frequency signal is low enough that all of the interface states will respond and the high-frequency signal is high enough that interface trap life time τ_{it} is not short enough to respond. The low-frequency C_{LF} and the high-frequency C_{HF} can be determined from [37]:

$$C_{LF} = \frac{C_{ox}(C_D + C_{it})}{C_{ox} + C_D + C_{it}} \tag{4.7}$$

$$C_{HF} = \frac{C_{ox}C_D}{C_{ox} + C_D} \tag{4.8}$$

For different semiconductors, the energy position of the charge-neutrality level, E_{CNL} is different. The energy location of E_{CNL}, bandgap E_g and electron affinity in various semiconductors are listed in Table 4.1. The energy value of the charge-neutrality level (CNL) is respected to the valance band energy level, E_V. More details on calculating CNL for compound semiconductor materials can be found in [40, 41].

	Gap (eV)	EA (eV)	CNL (eV)
Si	1.12	4.05	0.2
Ge	0.67	4.13	0.1
3C-SiC	2.35	4.55	1.3
6H-SiC	3.05	3.85	1.55
4H-SiC	3.25	3.65	1.55
AlP	2.56	2.8	1.3
GaP	2.25	3.2	0.74
InP	1.34	4.4	0.82
AlAs	2.16	3.54	0.92
GaAs	1.45	4.15	0.54
InAs	0.36	4.9	0.60
AlSb	1.7	3.6	0.4
GaSb	0.75	4.06	0.16
InSb	0.17	4.59	0.29
InN	0.7	5	1.58
GaN	3.2	3.3	2.32
AlN	6.2	0.6	3.3
ZnO	3.4	4.6	3.27

Table 4.1 Parameters for the various semiconductors – bandgap, electron affinity (EA) and charge-neutrality level (CNL). After ref. [40, 41].

4.2. Conductance Measurement

There are several techniques being employed to measure and characterize the interface states in a MOS structure. Two popular techniques we performed in our work will be discussed in this and the next section. The two techniques are the conductance measurement and the high-low frequency capacitance method. Other techniques have not been used because of their respective shortcomings and the limitations of our instruments and sample device.

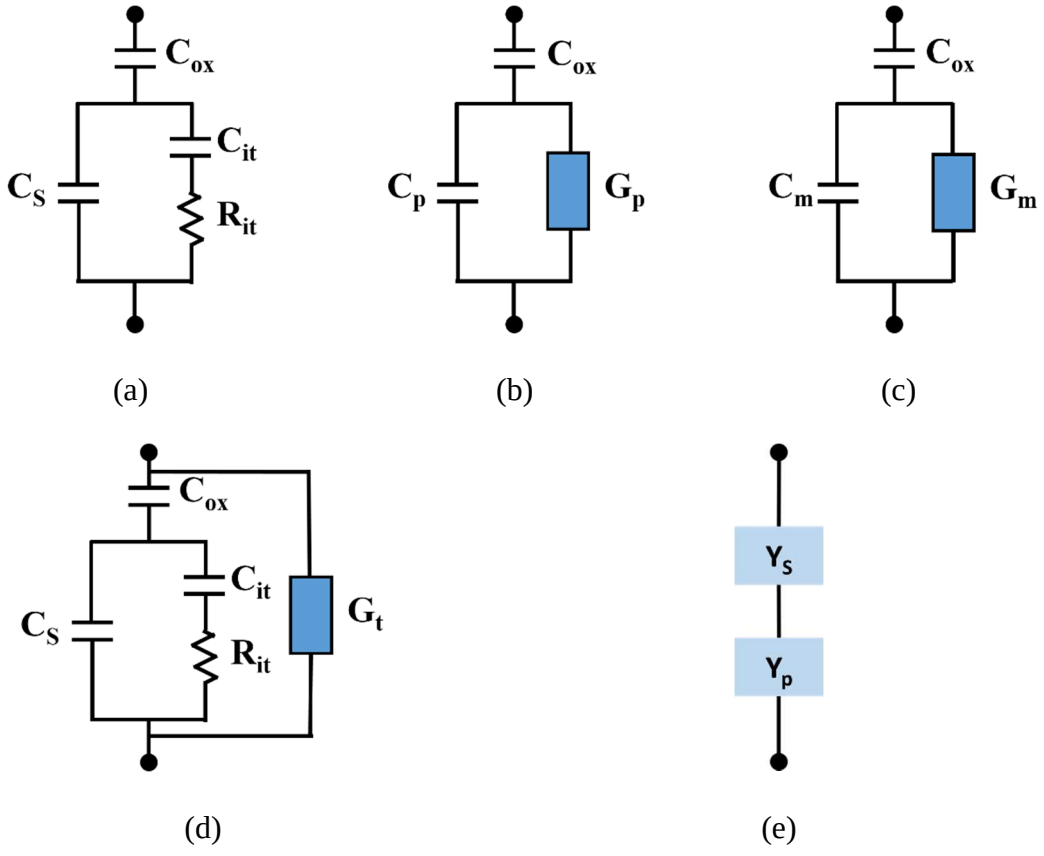


Fig. 4.5. Equivalent circuits for conductance method; (a) standard MOS capacitor, (b) simplified circuit of (a), (c) measured circuit, (d) including series resistance r_s and tunnel conductance G_t and (e) admittance circuit. After ref. [27]

The conductance method was first proposed by Nicollian and Goetzberger in 1967, it is one of the most complete, sensitive and accurate methods to evaluate the interface trap density D_{it} [42, 43]. The conductance method can be used to measure D_{it} values on the order of $10^9 cm^{-2}eV^{-1}$ and sometimes even lower. By using the conductance method, we can not only extract the D_{it} value in both the depletion and weak inversion portion of the bandgap, the capture cross-section of the interface states and the fluctuation of the surface potential ϕ_s can also be extracted as well. The conductance method is based on measuring the conductance G_m and capacitance C_m of a MOS capacitor as a function of bias voltage and frequency, and subsequently calculating the parallel conductance G_P by solving the small signal equivalent circuit. G_P represents the loss mechanism occurring when the interface states capture and emit carriers, and is used to extract the interface state density.

Fig. 4.5 shows the equivalent circuits of an MOS capacitor used for the conductance method [27]. In Fig. 4.5 (a), C_{ox} is the oxide capacitance, C_S is the semiconductor capacitance, C_{it} is the interface trap capacitance and R_{it} is the resistance representing the loss mechanism when the interface states capture and emit carriers. In order to obtain the parallel conductance G_P, we can replace the circuit of Fig. 4.4(a) by the circuit of Fig. 4.4(b), in which C_P and G_P are given by

$$C_P = C_S + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \tag{4.9}$$

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \tag{4.10}$$

where $C_{it}=q^2D_{it}$, $\tau_{it}=R_{it}C_{it}$ and $\omega= 2\pi f$ (f is the measurement frequency), τ_{it} is the interface state time constant. Further details of τ_{it} will be discussed in the next chapter. For Eq. (4.9) and Eq. (4.10), it is assumed that the interface state is a single energy level trap in the energy gap. However, the interface states have a continuous distribution in energy within the semiconductor energy gap at the semiconductor/oxide interface. For interface states, the capture and the emission primarily happens within a few kT/q above or below the Fermi level E_F, therefore, a time constant dispersion and normalized conductance is given by [42]

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln[1 + (\omega\tau_{it})^2] \tag{4.11}$$

In practical measurements, the impedance meters will assume that the device consists of a parallel C_m-G_m combination as the equivalent circuit shown in Fig. 4.5(c) [27], where C_m is the measured capacitance and G_m is the measured conductance. By converting the circuit in Fig. 4.5(c) to the circuit in Fig. 4.5(b), we can express G_P/ω in terms of C_m, C_{ox} and G_m as

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2(C_{ox} - C_m)^2} \tag{4.12}$$

Here, we assume the series resistance is negligible.

In order to extract the D_{it} value, the conductance and capacitance are measured as a function of frequency and plotted as G_P/ω versus ω [27]. For Eq. (4.10), the maximum G_P

occurs at $\omega=2/\tau_{it}$ where $D_{it}=2.5G_P/q\omega$, and for Eq. (4.11), the maximum G_P occurs at $\omega=1/\tau_{it}$ where $D_{it}=2G_P/q\omega$. In the G_P/ω versus ω plot, the D_{it} and τ_{it} value can be determined by the peak G_P and its peak frequency ω. Fig. 4.6 shows a series of G_P/ω under different bias in the depletion region for a silicon MOS capacitor.

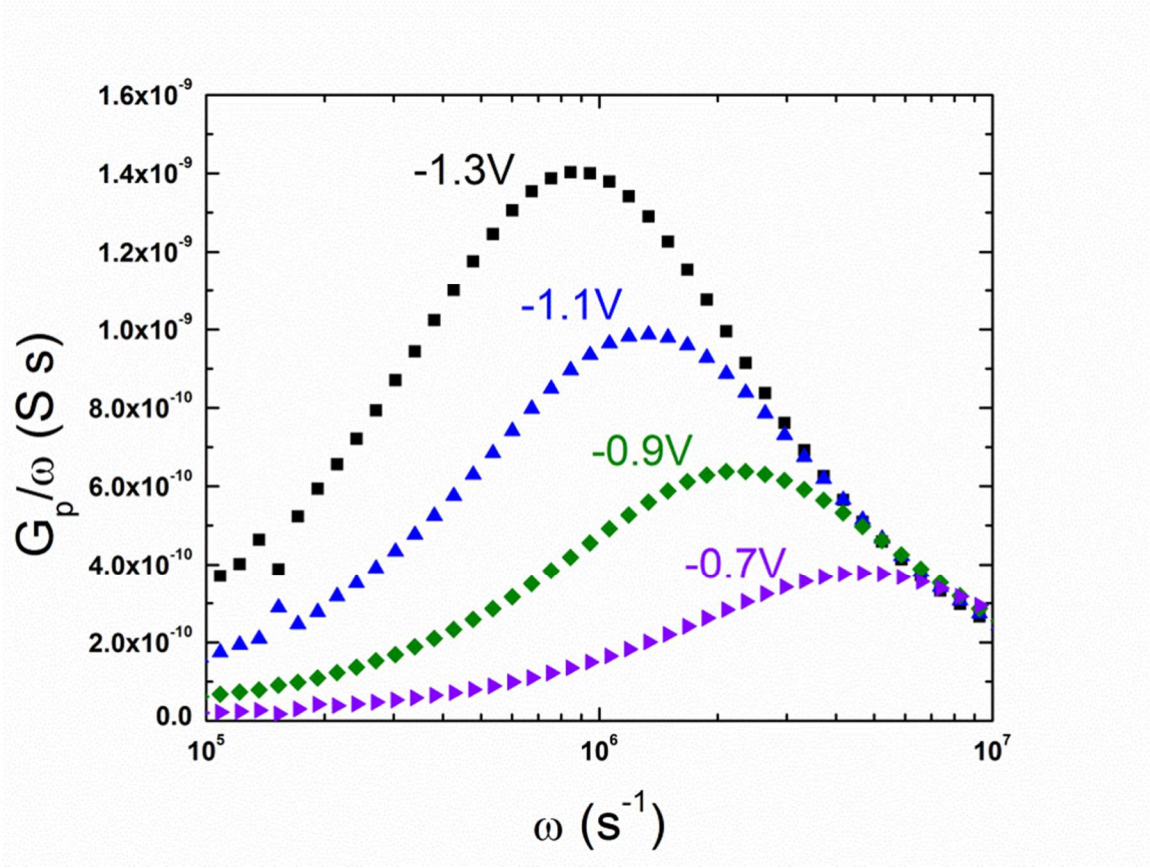


Fig. 4.6. G_P/ω versus ω in under different bias measured on a silicon MOS capacitor.

Fig. 4.7 shows a comparison of an experimental data measured from a Si/SiO_2 interface and the calculated G_P/ω by using Eq. (4.10) and Eq. (4.11). As shown, the experimental curve is much broader compare to two calculated curves. In a real MOS device there will always be surface potential fluctuations due to non-uniformities in interface traps, oxide

charge and doping density. The surface potential fluctuations will cause dispersion of the interface trap time constant and result in a broader curve [27]. The analysis of the experimental data will become more complicated by considering the surface potential fluctuations, and Eq. (4.11) becomes [43]

$$\frac{G_P}{\omega} = \frac{qD_{it}}{\sqrt{2\pi\sigma_{us}^2}} \int_{-\infty}^{\infty} \frac{\ln[1 + (\omega\tau_{it}e^{-\Delta U_s})^2]}{2\omega\tau_{it}e^{-\Delta U_s}} e^{\frac{-\Delta U_s^2}{2\sigma_{us}^2}} d\Delta U_s \qquad (4.13)$$

where ΔU_s is the difference of the normalized surface potential U_s and the normalized mean surface potential $\overline{U}_s$, and σ_{us} standard deviation of the surface potential.

The surface potential fluctuations are now considered by fitting Eq. (4.13) to the experimental data. During the fitting process, we can not only extract the accurate D_{it} value but also determine the interface state time constant τ_{it} and the standard deviation of the surface potential σ_{us}. In addition, the interface state capture cross section can be obtained by using the extracted τ_{it}. Further details will be discussed in the next chapter.

In order to determine the energy level of the extracted interface state relative to the valence band, the surface potential ϕ_s under the bias condition is calculated using [44]

$$\phi_s = \frac{qK_s\varepsilon_0 N_B A^2}{2C_d^2} \qquad (4.14)$$

and

$$E - E_V = \frac{E_g}{2} - (kT)\ln\left(\frac{N_B}{n_i}\right) + \phi_s \qquad (4.15)$$

where K_S is the semiconductor dielectric constant, N_B is the semiconductor substrate doping concentration and A is the measured area.

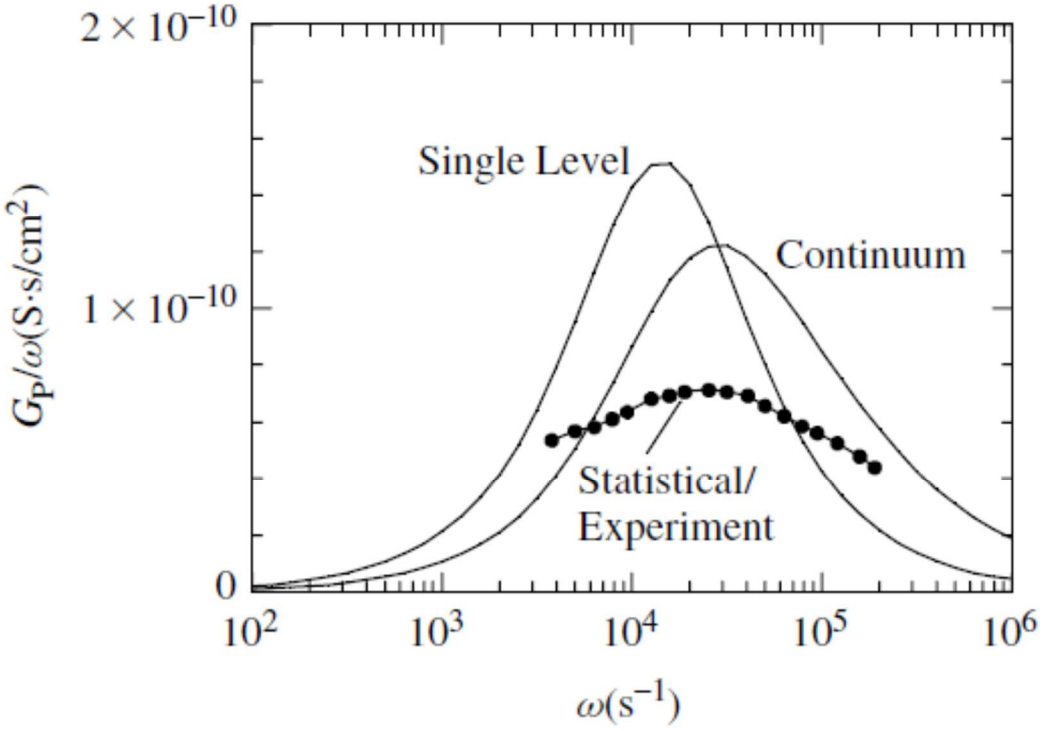


Fig. 4.7. G_P/ω versus ω for experimental data measured from Si/SiO_2 interface, single level [equation(4.10)] and continuum [equation(4.11)]. For all curves: $D_{it}=1.9\times10^{9}cm^{-2}eV^{-1}$, $\tau_{it}=7\times10^{-5}s$ [27].

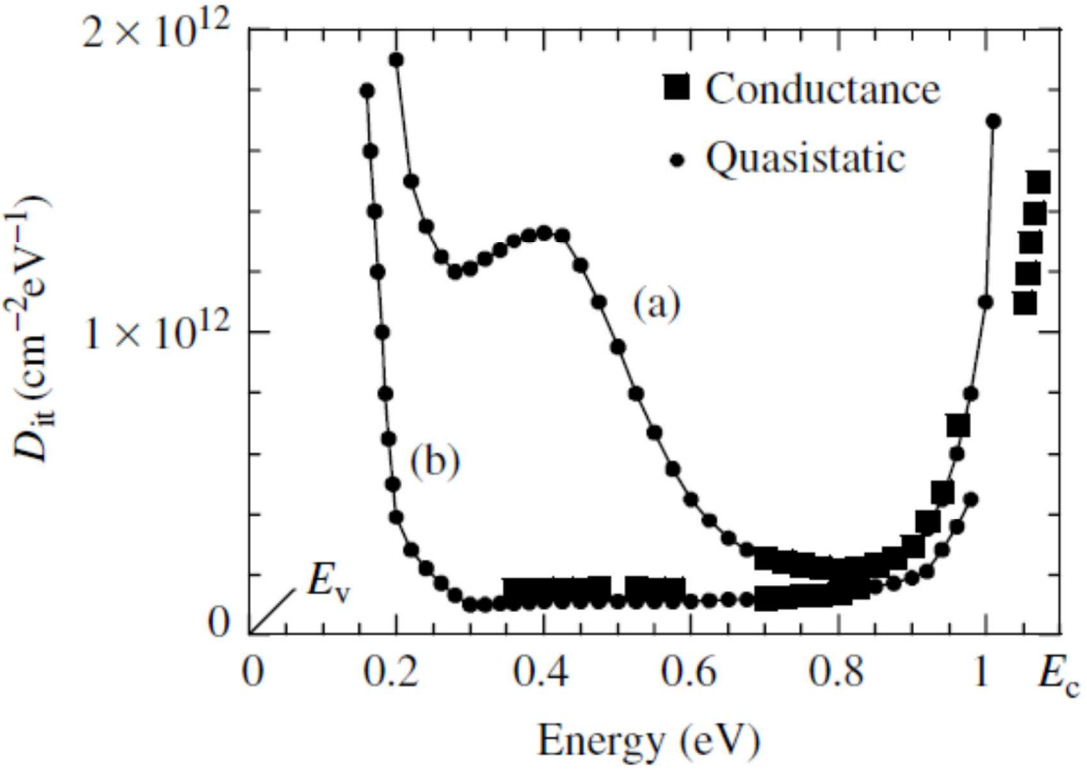


Fig. 4.8. Interface trap density D_{it} versus energy for quaasi-static and conductance method on (a) (111) n-Si and (b) (100) n-Si. [27]

For the conductance measurement, a wide range of measurement frequencies is needed. Using such a wide measurement frequency range allows extraction of a broader energy range for the interface states. Fig. 4.8 shows the comparison of the extracted interface trap density D_{it} measured by the conductance measurement and the quasi-static method on (111) and (100) n-type Silicon [27, 45, 46]. More details of the quasi-static method will be discussed in the next section. Although the two methods agree well with each other in the overlapping energy range, as shown Fig. 4.8, the D_{it} data measured by the quasi-static method cover a much broader extracted energy range. Compared to the quasi-static method, the conductance measurement can only extract D_{it} for a much narrower energy

range, only being able to measure D_{it} in the depletion and weak inversion region of the MOS capacitor. In order to have a more accurate result in terms of energy resolution, the signal amplitude of the applied small AC signal should be kept around 50mV or lower to prevent the rise of unwanted conductance from the harmonics of the signal frequency.

When measuring a MOS capacitor which has a thin oxide, the oxide leakage current and the series resistance will no longer be negligible. In order to take the oxide leakage current and the series resistance in to account, a more complete equivalent circuit model is needed. Fig 4.5 (d) shows the equivalent circuit includes the tunnel conductance G_t and the series resistance r_s, hence Eq. (4.12) becomes [47, 48]

$$\frac{G_P}{\omega} = \frac{\omega(G_c - G_t)C_{ox}^2}{G_c^2 + \omega^2(C_{ox} - C_c)^2} \tag{4.16}$$

where

$$C_c = \frac{C_m}{(1 - r_s G_m)^2 + (\omega r_s C_m)^2} \tag{4.17}$$

and

$$G_c = \frac{\omega^2 r_s C_m C_c - G_m}{r_s G_m - 1} \tag{4.18}$$

The series resistance r_s can be determined by biasing the MOS capacitor into the strong accumulation and using [43]

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{4.19}$$

where G_{ma} and C_{ma} represents the measured conductance and capacitance in accumulation mode. The tunnel conductance can be determined as $\omega \rightarrow 0$ in Eq (4.18) [43].

In order to reduce the unwanted parasitic effects due to the contact, device design and the measurement setup, Prof. James A. Cooper of the Purdue University Electrical and Computer Engineering Department proposed a parasitic reduction method. By biasing the device into strong accumulation, we measure the real and imaginary parts of the admittance as a function of frequency. This represents C_{ox} in series unwanted parasitic and shown as Y_S in Fig. 4.5 (e). And then subtract this series admittance from the measured admittance at each frequency, this leave us with the depletion admittance Y_p that represents G_p and C_p in Fig.4.5 (b). G_p and C_p now become

$$G_P = \frac{\left(\frac{G_m}{{G_m}^2 + \omega^2 {C_m}^2}\right) - \left(\frac{G_{ma}}{{G_{ma}}^2 + \omega^2 {C_{ma}}^2}\right)}{\left[\left(\frac{G_m}{{G_m}^2 + \omega^2 {C_m}^2}\right) - \left(\frac{G_{ma}}{{G_{ma}}^2 + \omega^2 {C_{ma}}^2}\right)\right]^2 + \omega^2 \left[\left(\frac{C_m}{{G_m}^2 + \omega^2 {C_m}^2}\right) - \left(\frac{C_{ma}}{{G_{ma}}^2 + \omega^2 {C_{ma}}^2}\right)\right]^2} \tag{4.20}$$

And

$$C_P = \frac{\left(\frac{C_m}{{G_m}^2 + \omega^2 {C_m}^2}\right) - \left(\frac{C_{ma}}{{G_{ma}}^2 + \omega^2 {C_{ma}}^2}\right)}{\left[\left(\frac{G_m}{{G_m}^2 + \omega^2 {C_m}^2}\right) - \left(\frac{G_{ma}}{{G_{ma}}^2 + \omega^2 {C_{ma}}^2}\right)\right]^2 + \omega^2\left[\left(\frac{C_m}{{G_m}^2 + \omega^2 {C_m}^2}\right) - \left(\frac{C_{ma}}{{G_{ma}}^2 + \omega^2 {C_{ma}}^2}\right)\right]^2} \quad (4.21)$$

where G_{ma} and C_{ma} are the measured conductance and capacitance in accumulation mode.

4.3. High-low Frequency Capacitance method

There is another interface state measuring technique for extracting the interface state density by measuring the capacitance at a fixed high and a fixed low frequency, known as the high-low frequency capacitance method. Compared with the conductance measurement discussed in the last section, the high-low frequency capacitance method is easier and faster to perform. The idea behind the high-low frequency capacitance method is intuitively simple, measure the capacitance at a high enough frequency that no interface state can respond to the high frequency signal and measure the capacitance at a low enough frequency that all of the interface states will respond to the low frequency signal, the interface state density D_{it} can be extracted from the difference of the two capacitance-voltage curves.

For discussing the detail theory of the high-low frequency capacitance method, we first need to address some useful terms. The interface state associated capacitance C_{it} and interface state density D_{it} has a relationship of,

$$C_{it} \equiv \frac{dQ_{it}}{d\phi_s} \quad (4.21)$$

$$= q^2 D_{it}$$

where $dQ_{it} = qD_{it}dE$ and $dE = qd\phi_s$. Q_{it} represents the interface state charges. Also, by using the low-frequency equivalent circuit in Fig. 4.4(c), we can obtain relationship between the surface potential ϕ_s versus applied voltage V curve and the interface states

$$\frac{d\phi_s}{dV} = \frac{C_{ox}}{C_{ox}+C_d+C_{it}} \tag{4.22}$$

where $V = V_{ox} + \phi_s$. By substitution of Eq. (4.21) into Eq. (4.22), Eq. (4.22) now becomes

$$D_{it} = \frac{C_{ox}}{q^2}\left[\left(\frac{d\phi_s}{dV}\right)^{-1} - 1\right] - \frac{C_D}{q^2} \tag{4.23}$$

Then we can calculate the D_{it} value by obtain the $\phi_s - V$ relationship from the capacitance measurement [37].

Three different capacitance methods have been commonly used for measuring D_{it}, they are called the high-frequency method, the low-frequency method and the high-low frequency method. The high-frequency method was purposed by Terman in 1962 [49]. For the high-frequency method, the high-frequency equivalent circuit shown in Fig. 4.4(d) does not contain the component of the interface state associated capacitance C_{it}. By measuring the capacitance at high frequency, the depletion-layer capacitance C_d can be determine by the capacitance C_{HF} using [37]

$$C_{HF} = \frac{C_{ox}C_d}{C_{ox}+C_d} \tag{4.24}$$

Also, the surface potential ϕ_s can calculated by using Eq. (4.14), and by using the $\phi_s - V$ relationship, the D_{it} value can be determined by using Eq. (4.23).

The low-frequency method sometimes called quasi-static method was purposed by Berglund in 1967 [50]. Different than the high-frequency method, the $\phi_s - V$ relationship is determine by the capacitance C_{LF} measured at low frequency. Based on the low-frequency equivalent circuit in Fig. 4.4(c) and Eq. (4.22),

$$\begin{aligned} \frac{d\phi_s}{dV} &= \frac{C_{ox}}{C_{ox}+C_D+C_{it}} \\ &= 1 - \frac{C_D+C_{it}}{C_{ox}+C_D+C_{it}} \\ &= 1 - \frac{C_{LF}}{C_{ox}} \end{aligned} \tag{4.25}$$

By integrating equation (4.25) over two applied voltage we get

$$\phi_s(V_2) - \phi_s(V_1) = \int_{V_1}^{V_2} \left(1 - \frac{C_{LF}}{C_{ox}}\right) dV + constant \tag{4.26}$$

For Eq. (4.26), the surface potential can be determined at any applied voltage by integrating Eq. (4.25). The constant in Eq. (4.25) represents the starting point of the ϕ_s either in the accumulation or the strong inversion region, ϕ_s has a weak dependence on the supply

voltage in these two regions [37]. By knowingϕ_s, the depletion-layer capacitance C_d can be determined using Eq. (4.14) with the semiconductor substrate doping concentration.

In 1971, Castagne and Vapaille purposed the high-low frequency method which combines the high-frequency and the low-frequency method [51]. The advantage of the high-low frequency method is that no theoretical calculation is needed for comparison, since especially for non-uniform doping profiles such theoretical calculation is highly complicated. With the low-frequency capacitance C_{LF} in Fig. 4.4(c)

$$C_{LF} = \frac{C_{ox}(C_D+C_{it})}{C_{ox}+C_D+C_{it}} \tag{4.27}$$

and Eq. (4.24), we can express

$$\begin{aligned} C_{it} &= \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - C_D \\ &= \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \end{aligned} \tag{4.28}$$

By defining the difference in capacitance between high-frequency and low-frequency as $\Delta C \equiv C_{LF} - C_{HF}$, and Eq. (4.21), the interface state density D_{it} can be directly obtained by [37]

$$D_{it} = \frac{C_{ox}}{q^2}\left[\left(\frac{1}{\Delta C/C_{ox} + C_{HF}/C_{ox}} - 1\right)^{-1} - \left(\frac{1}{C_{HF}/C_{ox}} - 1\right)^{-1}\right] \quad (4.29)$$

$$= \frac{\Delta C}{q^2}\left(1 - \frac{C_{HF}+\Delta C}{C_{ox}}\right)^{-1}\left(1 - \frac{C_{HF}}{C_{ox}}\right)^{-1}$$

at each bias. Fig. 4.9 shows the capacitance measured at high frequency and low frequency on a Silicon capacitor.

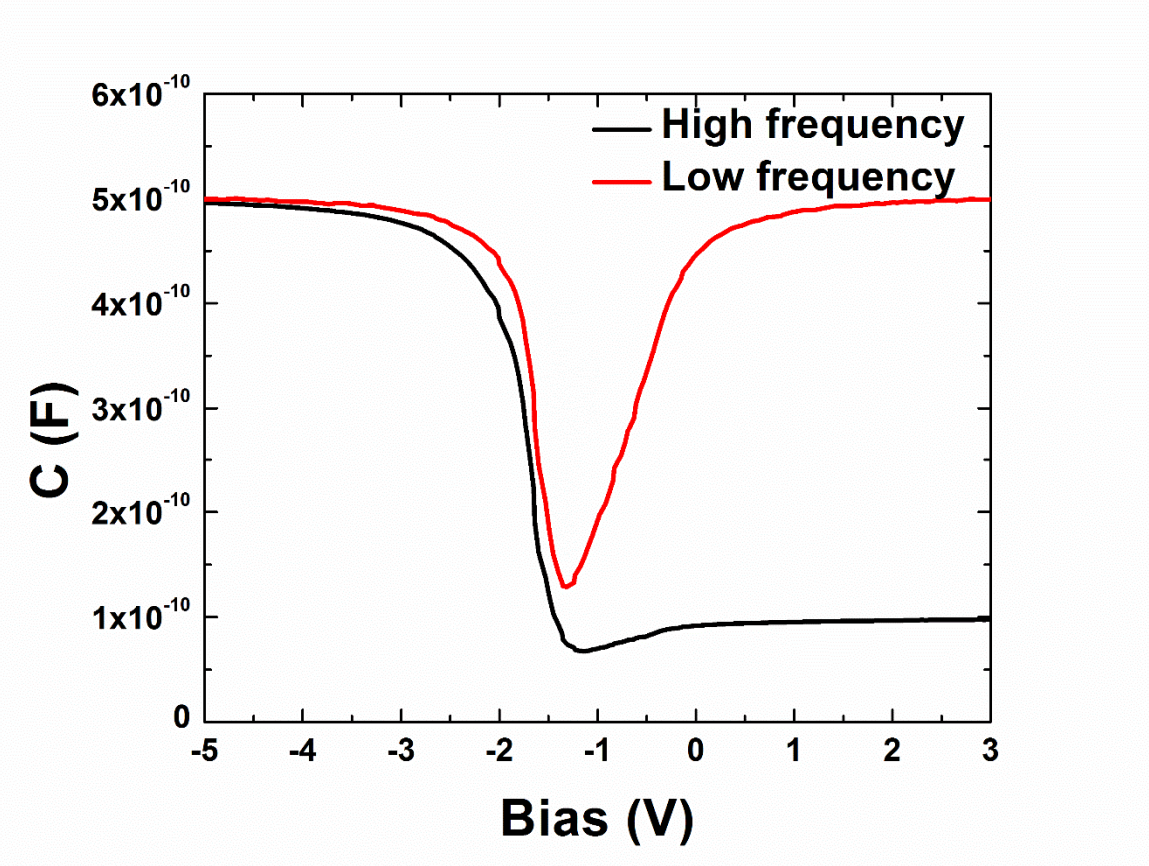


Fig. 4.9. Capacitance measured on silicon MOS capacitor at high and low frequency.

The energy level of the extracted interface state must to be known in order to obtain the D_{it} profile. Similar to the conductance method, the energy level of the extracted interface state can be calculated from the capacitance measured at high frequency using Eq. (4.14) and Eq. (4.15). Fig. 4.10 shows the D_{it} profile extracted from the capacitance data in Fig. 4.9.

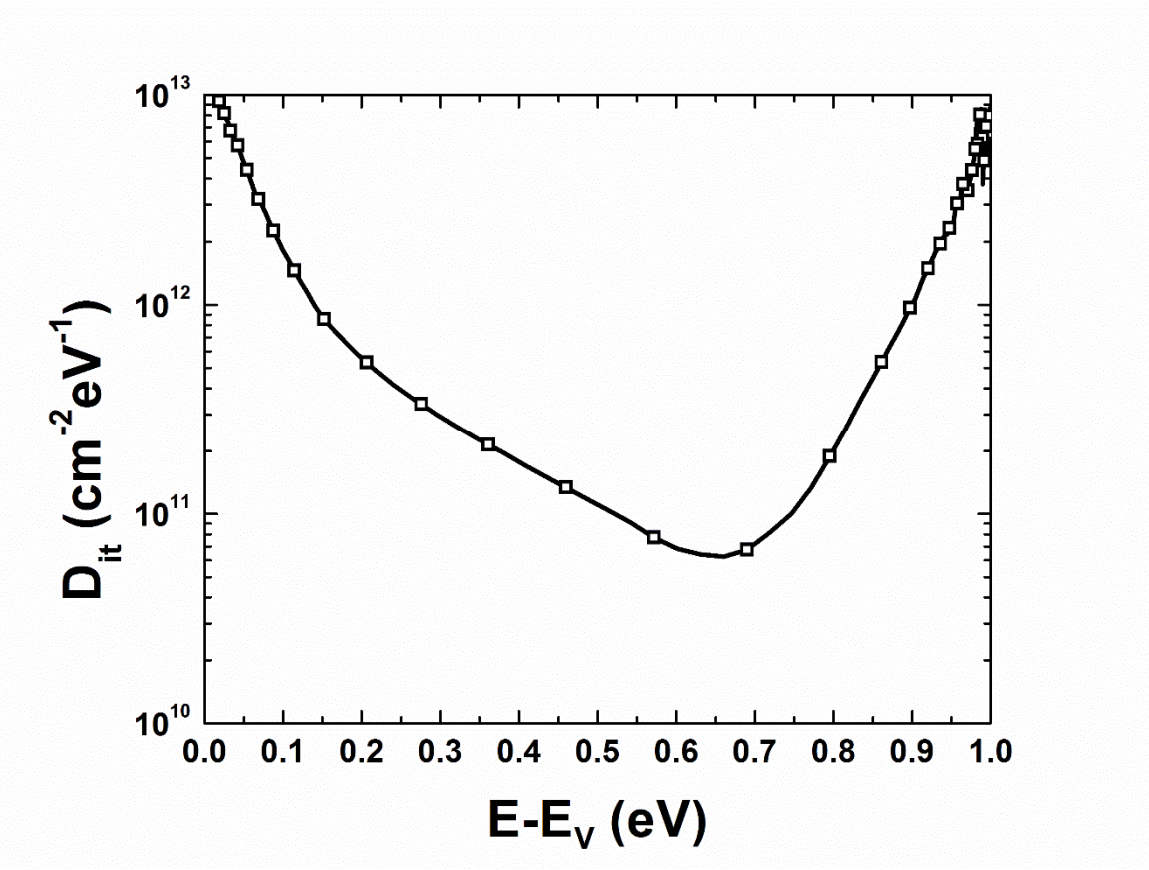


Fig. 4.10. D_{it} profile measured using high-low frequency method on silicon MOS capacitor.

4.4. Conductance Measurement of SiC MOS-C

	Substrate	Doping (cm^{-3})	t_{ox} (nm)	Contact Metal	Anneal
N2(2)	n-type	10^{16}	100	Mo	NA
P5	p-type	6.2×10^{15}	100	Mo	NA
Cree 1	n-type	10^{16}	100	Poly-Si	No information
NO0218	n-type	10^{16}	60	Mo	NO
PSG225	n-type	10^{16}	68	Mo	PSG
Cree 2	n-type	10^{16}	55	Poly-Si	No information
Cree 3	n-type	10^{16}	43	Al	NA
Cree 4	n-type	10^{16}	43	Al	NA
142	n-type	5.5×10^{15}	60	Mo	N plasma
143	n-type	5.5×10^{15}	60	Al	N plasma
144	n-type	5.5×10^{15}	60	Mo	N plasma
145	n-type	5.5×10^{15}	60	Al	N plasma

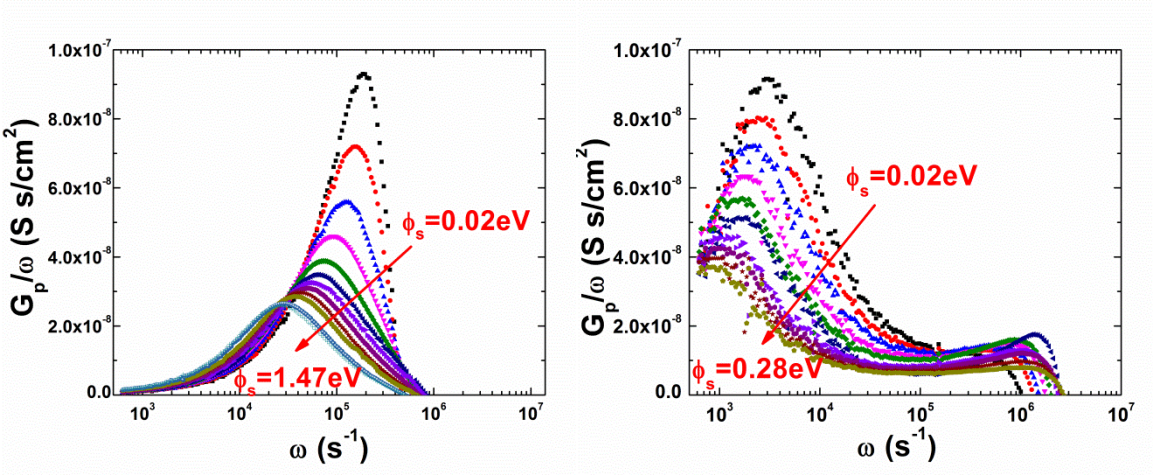
Table 4.2. Basic sample information used for this research.

Table 4.2 shows the basic information of the samples used for the research presented in this chapter. We used 4H-SiC n-type and p-type samples grown by Cree Inc.. Samples N2(2), P5 NO0219, PSG225, 142, 143, 144 and 145 were oxidized by Prof. Sarit Dhar of the Auburn University Physics Department. All these samples underwent the NO passivation during the fabrication process. Sample Cree 1, Cree 2, Cree 3 and Cree 4 were

oxidized by Cree Inc.. Sample N2(2) and P5 are used to make lifetime measurements and were heated to 400°C several times.

In order to minimize the effect of gate leakage current, we choose a device on the samples which had a low gate leakage current for the conductance measurement. Both n-type and p-type substrate samples were measured. The capacitance and conductance data were measured with an Agilent 4294A impedance meter, with a frequency range of 40Hz to 110MHz.

In order to accurately identify the conductance peak, the frequency of the peak point should be at least 5 times above (or below) the minimum (or maximum) measurement frequency. We measured the conductance and the capacitance with a frequency sweep range of 40Hz to 10MHz to minimize the noise at high frequencies.



(a) (b)

Fig. 4.11. Small signal ac interface state conductance G_p/ω as a function of ω on (a) P5L01 and (b) P5L04 at room temperature.

Fig. 4.11 shows the data of interface state conductance G_p/ω as a function of ω on two different devices on P5 at room temperature. In order to determine the energy of the interface states relative to the valence band energy, the surface potential ϕ_s is calculated by using Eq. (4.14) and the energy is then calculated using Eq. (4.15).

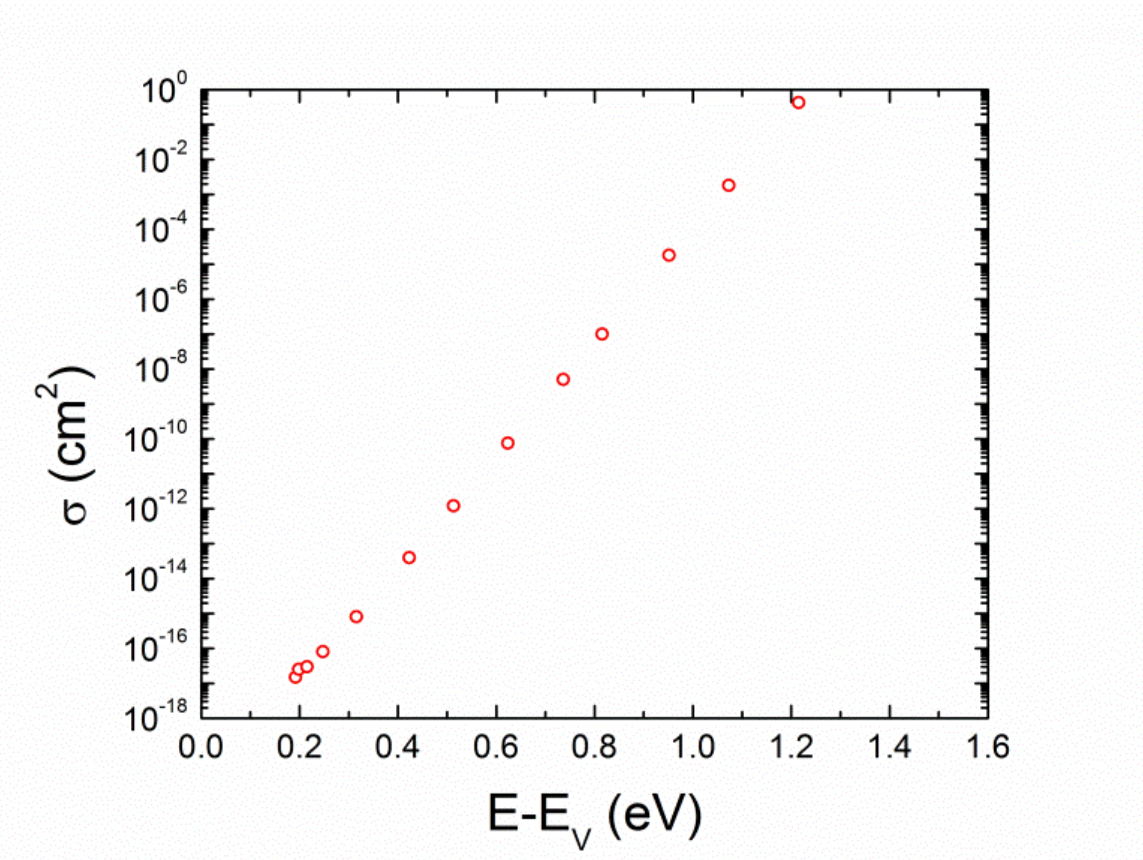
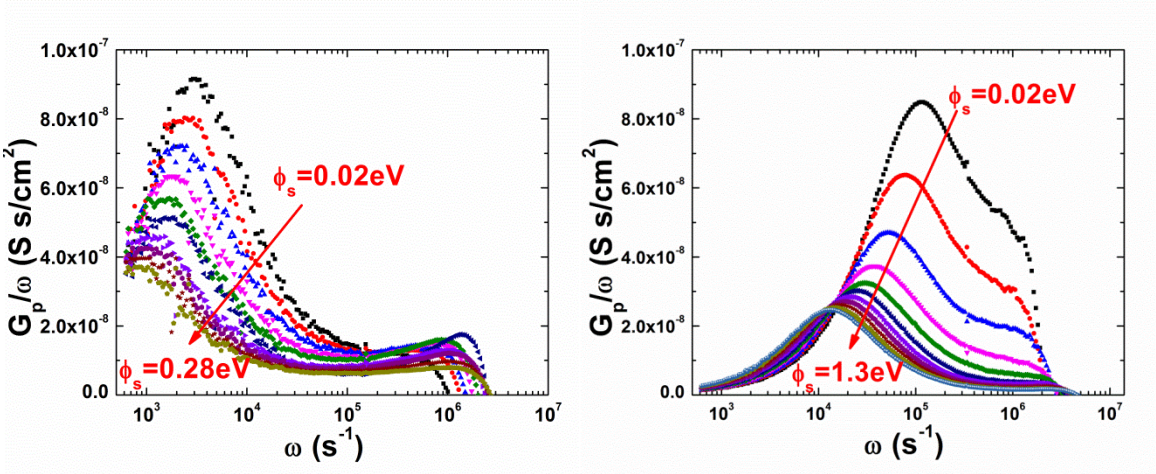


Fig. 4.12. Interface trap capture cross-section vs energy for P5L05.

Fig. 4.12 shows the interface trap carrier capture cross-section extracted by using curve fitting on the conductance data for P5L05. As shown in Fig. 4.12, the interface trap capture cross-section increases exponentially as the energy of the interface traps increases. With

increasing interface trap energy close to mid-gap, the capture cross-section becomes unrealistically large.

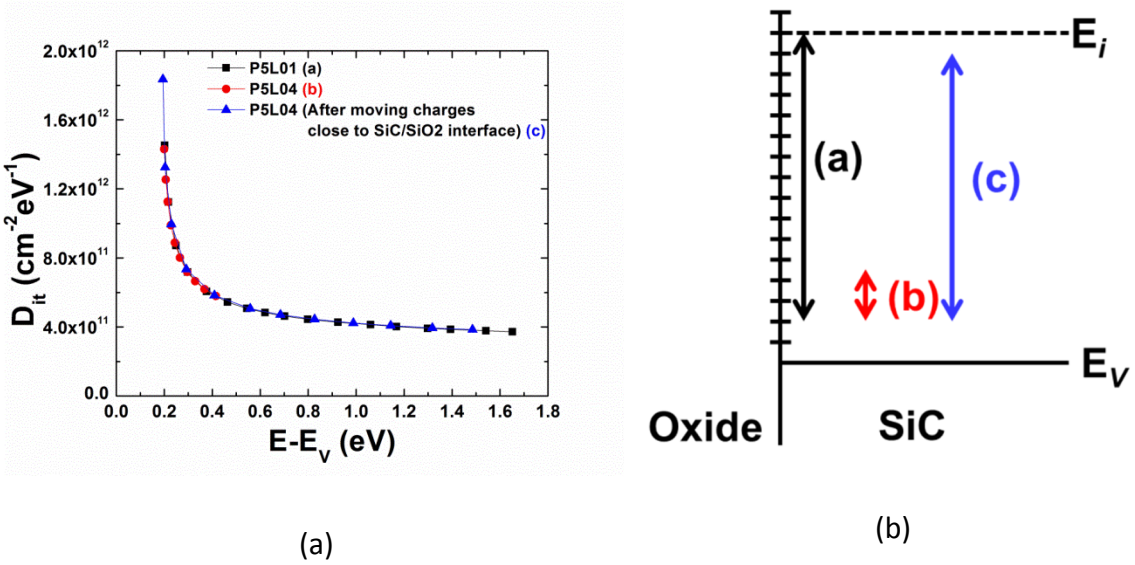
As shown in Fig. 4.11, for P5L01, interface traps responded at higher frequencies and we extracted D_{it} for a larger energy range compared to P5L04. P5L01 has a larger flatband voltage shift than P5L04, which can be attributed to mobile ions in the oxide closer to the SiC/SiO_2 interface. To determine the oxide mobile ion density, we conducted bias temperature stress (BTS) measurements on P5, N2(2) and Cree 1 samples. P5 and N2(2) show $Q_m \approx 10^{12} cm^{-2}$ and Cree1 shows only $Q_m \approx 10^{10} cm^{-2}$. However, after Cree 1 was heated to 400°C and cooled to room temperature, the mobile ion density dramatically increased to $Q_m \approx 10^{12} cm^{-2}$.



(a) (b)

Fig. 4.13. Small signal ac interface state conductance G_p/ω as a function of ω on P5L04 (a) before and (b) after moving the ions close to the interface.

In order to understand how the mobile ions in the oxide affect the conductance measurement, we moved the mobile ions with BTS and repeated the conductance measurements the following day. During BTS, we first heated the sample to 200°C and applied either +5 V or -5 V for 5 minutes to move the ions close to or away from the SiC/SiO_2 interface. After 5 minutes of applying bias at 200°C, we turned the heater off to cool the sample, still applying the bias during cool down. The bias is removed when the sample temperature is lower than 40°C.



(a) (b)

Fig. 4.14. (a) Extracted D_{it} profile and (b) energy range at different conditions on P5 sample.

Fig. 4.13 shows the conductance for P5L04 before and after moving the ions in SiO_2 close to the SiC/SiO_2 interface by BTS. As shown in Fig.4.13, after moving the ions close to the SiC/SiO_2 interface, the interface traps responded at higher frequencies and allowed us to extract D_{it} over a larger energy range. The energy range increased from 0.26 eV to 1.28 eV. Fig. 4.14 shows the extracted D_{it} profile and the extracted range for P5 under

different conditions. As shown in Fig. 4.14, although the extracted energy range is different, the extracted D_{it} matches within the measured range. We were not able to measure P5L04 after moving the ions away from the interface because P5L04 failed during BTS.

We also performed the same procedure on Cree 1. Fig. 4.15 shows results of conductance measurements for Cree 1-3L04 before and after moving the ions in the SiO_2 close to or away from the SiC/SiO_2 interface. Same as P5, Cree1 also shows increased extracted energy range when the mobile ions in the oxide are closer to the SiC/SiO_2 interface. Fig. 4.16 shows the extracted D_{it} profile and the extracted range for Cree 1 under different conditions.

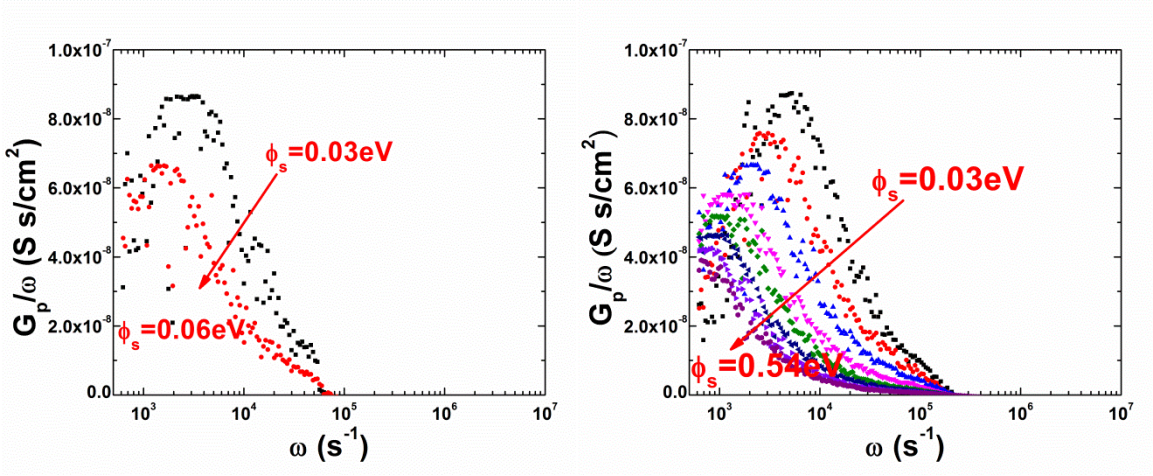
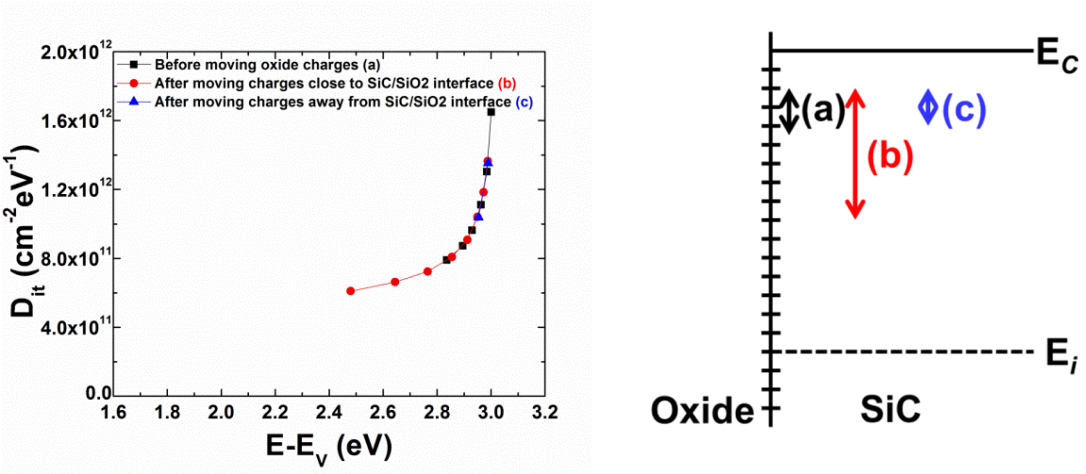


Fig. 4.15. Small signal ac interface state conductance G_p/ω as a function of ω on Cree1-3L04 after moving the ions (a) away from and (b) close to the interface.

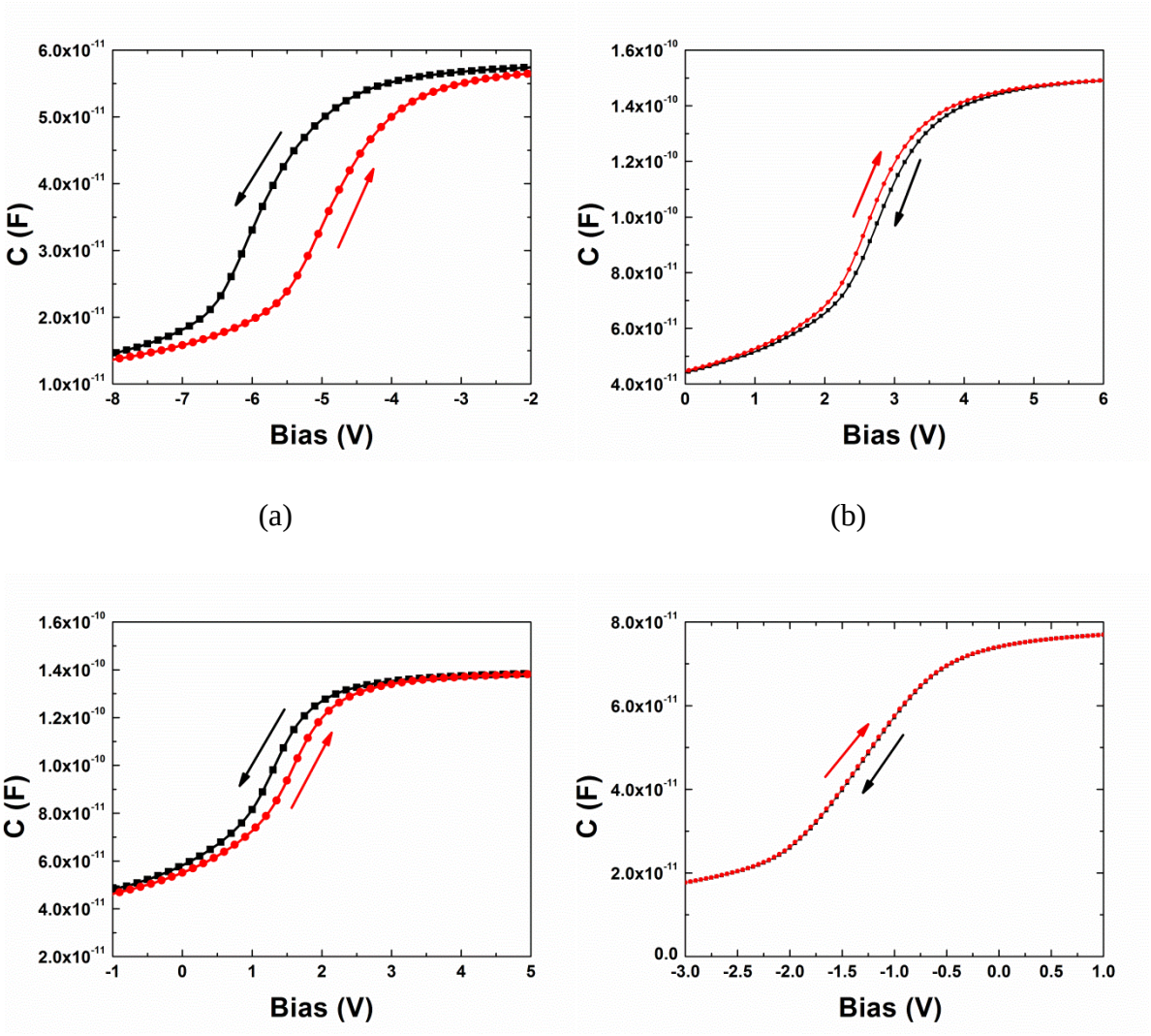


(a) (b)

Fig. 4.16. (a) Extracted D_{it} profile and (b) energy range at different conditions on Cree1 sample.

In order to understand the oxide charge behavior at room temperature, we measured the C-V by sweeping in different directions on Cree 1, NO0219 and PSG0225. Fig. 4.17 summarizes the results with Cree 1 and PSG0225 showing ion drift behavior in the oxide, NO0219 showing electron injection and Cree 2 showing almost no oxide charge behavior.

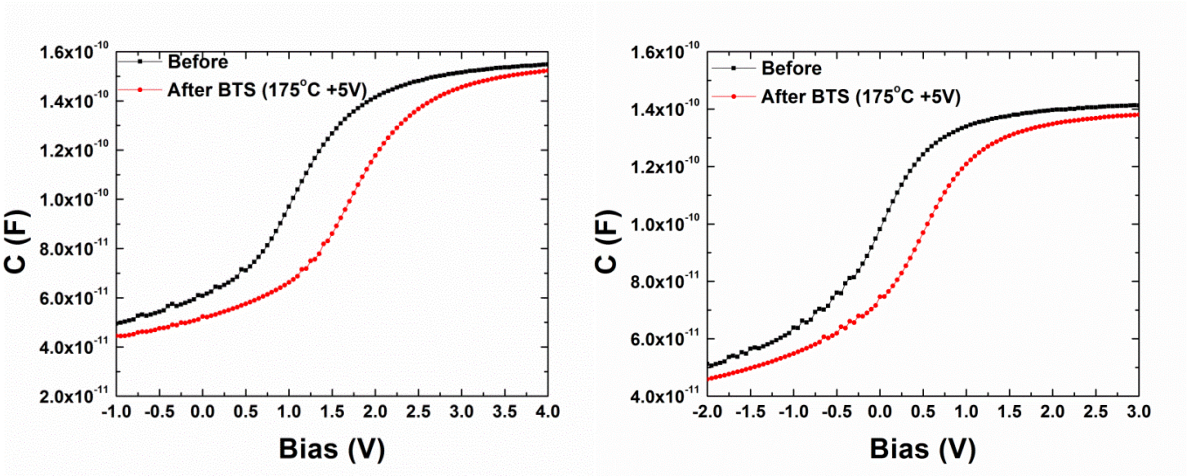
We also measured BTS on NO0219 and PSG0225 after heating the sample to 200°C at +5V for 5 minutes, and turning the heater off with the bias applied during cool down. Fig. 4.18 shows the C-V curves for NO0219 and PSG0225 after BTS. As shown in Fig. 4.18, the C-V curve for both samples has a positive voltage shift after BTS. Both samples show electron injection behavior, while PSG0225 shows ion drift behavior at room temperature before BTS.



(a) (b)

(c) (d)

Fig. 4.17 C-V curve measured by sweeping towards different directions on (a) Cree1, (b) NO0219, (c) PSG0225 and (d) Cree 2.



(a) (b)

Fig. 4.18. C-V after BTS for (a) NO0219-12 and (b) PSG0225-12.

Table 4.3 summarizes the oxide charge behavior of P5, Cree1, NO0219 and PSG0225. P5 and Cree1 were previously heated to 400°C for lifetime measurements before the oxide charge behavior study.

	Before BTS at room temperature	After BTS
P5	ion drift	ion drift
Cree1	ion drift	ion drift
NO0219	electron injection	electron injection
PSG0225	ion drift	electron injection
Cree2	no oxide charge behavior	NA
Cree3	electron injection	NA

Table 4.3. Oxide charge behavior before and after BTS.

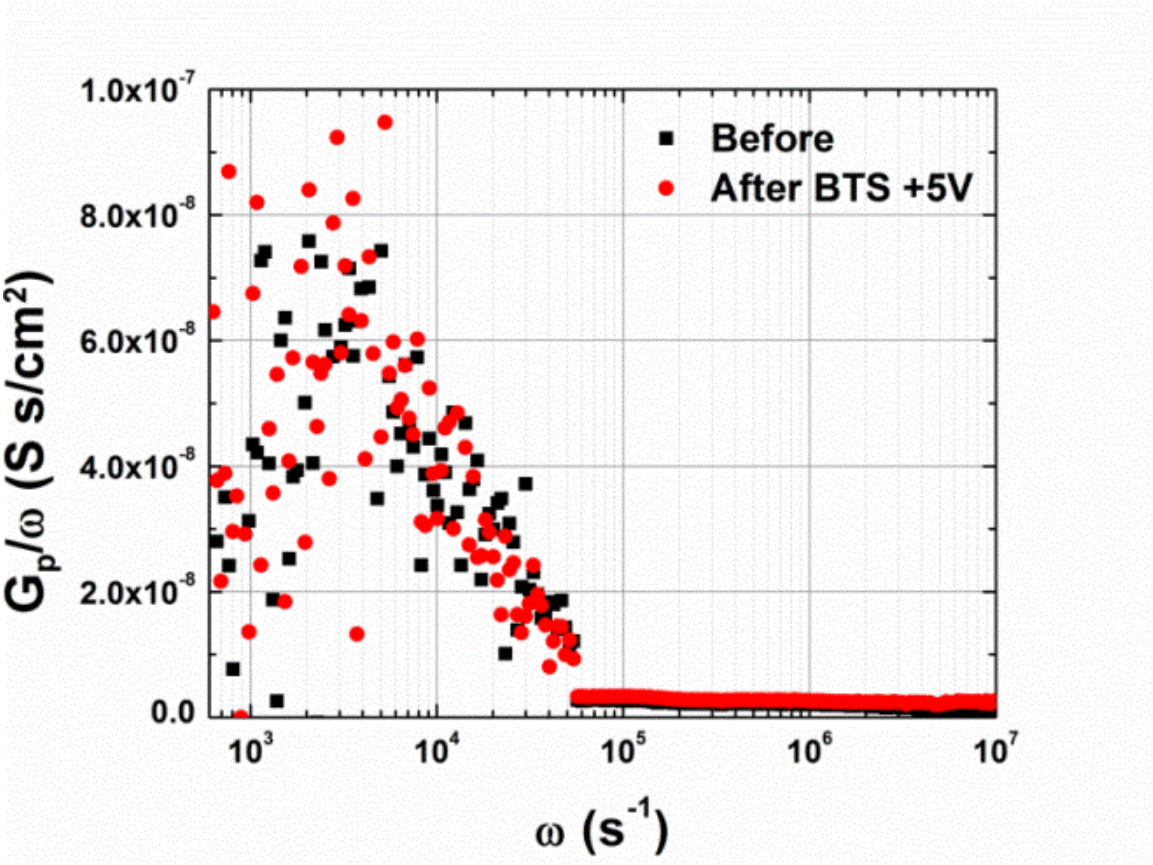
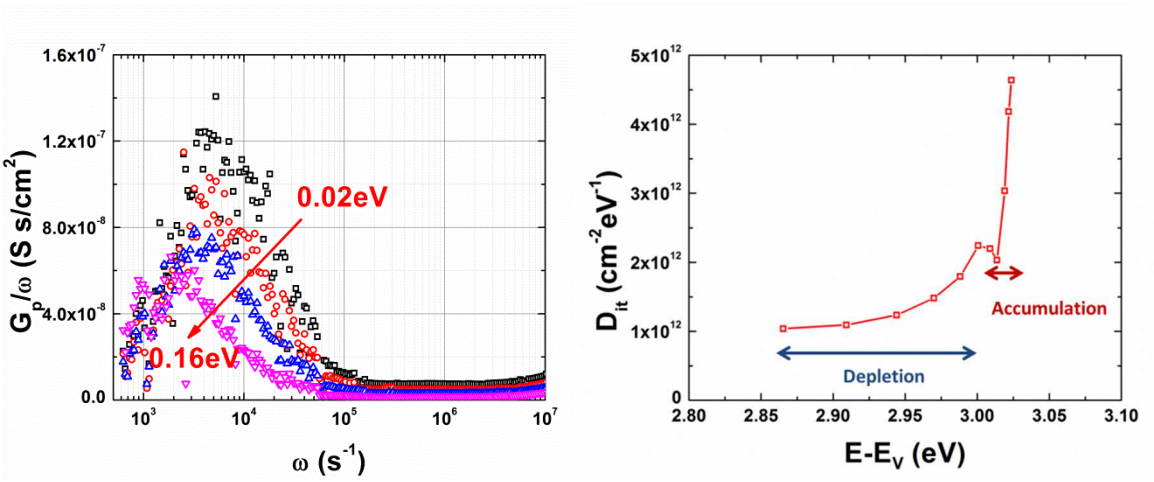


Fig. 4.19. Small signal ac interface state conductance G_p/ω as a function of ω on NO0219-12 before and after BTS at $\varphi_s \approx 0.09eV$.

We measured the conductance on NO0219 and Cree 3 which shows electron injection before and after BTS. Fig. 4.19 shows the conductance results for NO0219 before and after BTS under almost the same surface potential. As shown in Fig. 4.19, the interface response time does not change after BTS. Devices with electron injection behavior do not increase the D_{it} extraction energy range after positive bias BTS as for devices with ion drift.

Fig. 4.20 shows the conductance results in the depletion region and the extracted D_{it} profile for NO0219. As shown in Fig. 4.20(b), the extracted D_{it} profile curve has a

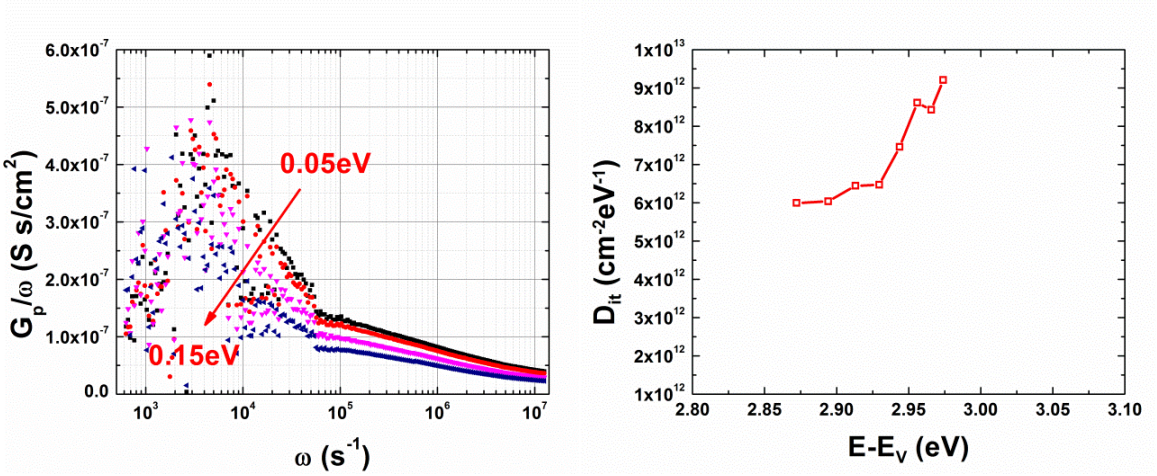
discontinuous point between depletion and accumulation region. The discontinuity appears because the model we used only fits in the depletion region, not in the accumulation region.



(a) (b)

Fig. 4.20. (a) Small signal ac interface state conductance G_p/ω as a function of ω in the depletion region on and (b) extracted D_{it} profile for NO0219.

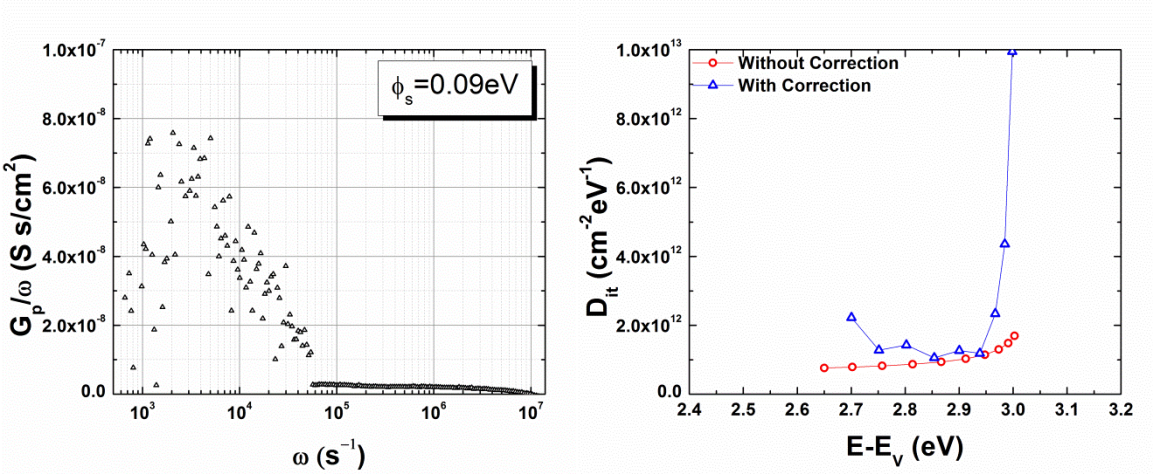
Fig. 4.21 shows the conductance results and extracted D_{it} profile for Cree 3. Cree 3 is an unpassivated sample, as we expected, the extracted D_{it} for Cree 3 is higher than any other sample we have measured.



(a) (b)

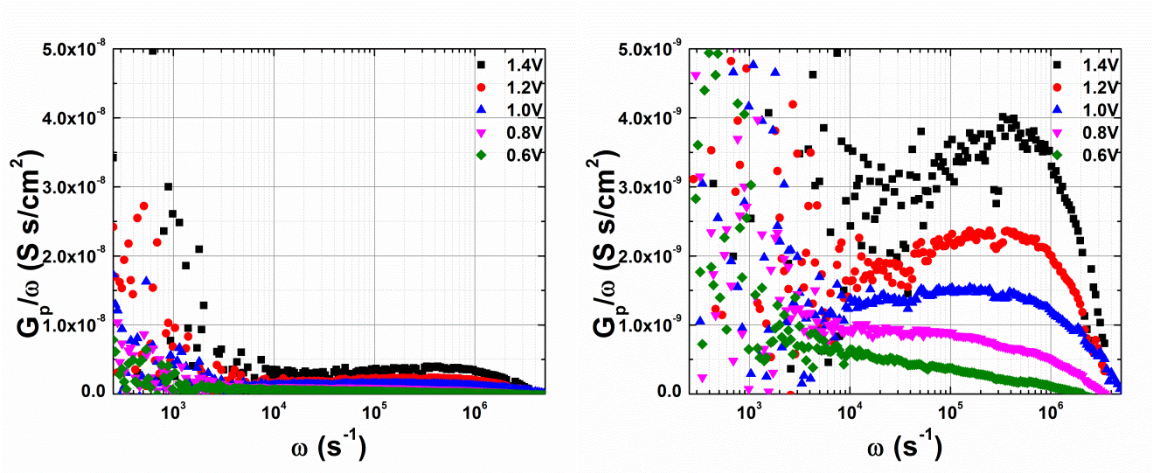
Fig. 4.21. (a) Small signal ac interface state conductance G_p/ω as a function of ω and (b) extracted D_{it} profile for Cree3.

Fig. 4.22 shows the conductance results and extracted D_{it} profile using this parasitic reduction method compared with the D_{it} result derived without using the parasitic reduction method for the samples NO0219. Fig. 4.22 only shows G_p/ω v.s. ω at one bias point because the data is too noisy to be able to distinguish between multiple bias point data in the same figure. As shown in Fig. 4.22(b), the D_{it} result using the parasitic reduction method is only slightly higher than the result without using the parasitic reduction method.



(a) (b)

Fig. 4.22. (a) Small signal ac interface state conductance G_p/ω as a function of ω at φ_s=0.09 and (b) extracted D_{it} profile with and without parasitic reduction for NO0219.



(a) (b)

Fig. 4.23. Small signal ac interface state conductance G_p/ω as a function of ω scale to

(a) low frequency peak, (b) high frequency peak for PSG225.

Fig. 4.23 shows the conductance results for PSG225. As shown Fig. 4.23(a), the conductance peak is at lower frequency and out of our measurement range. The fact that the peal is not fully accessible within the range of measurement frequencies makes it impossible to determine the D_{it} value from the low frequency peak. However, there is second peak at higher frequency with lower magnitude. In Fig. 4.23(b), the peak can be observed by changing the G_p/ω scale. We can fit the conductance curve to this higher frequency peak using Eq. (4.13) and extract the D_{it} value. The D_{it} profile extracted by curve fitting is shown in Fig. 4. 24.

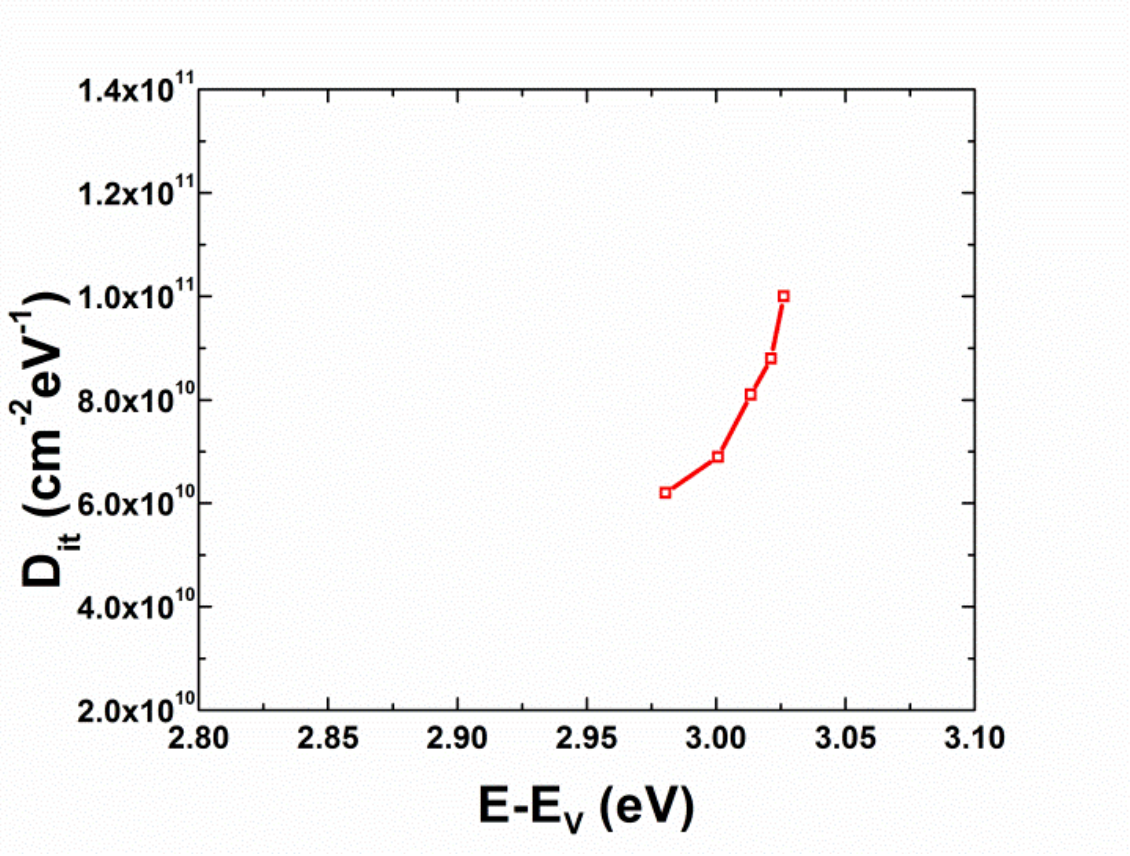
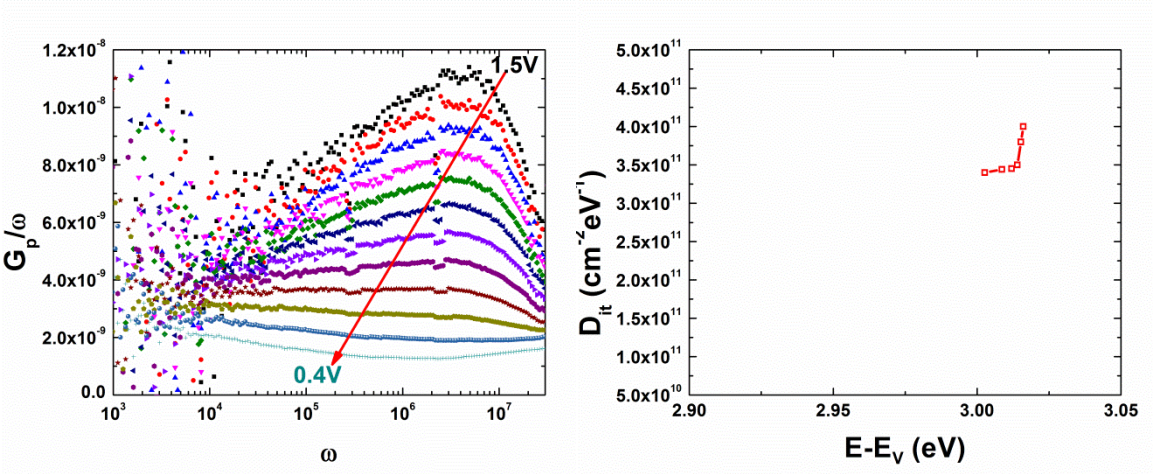


Fig. 4.24. extracted D_{it} profile for PSG225.

Fig. 4.25 shows the conductance results and extracted D_{it} profile for sample 142. Similar to PSG225, the conductance peak for sample 142 at lower frequency is out of our measurement range, but the sample exhibits another peak at higher frequency with lower magnitude as well. In Fig. 4.25(a), the high frequency peak can be observed by changing the G_p/ω scale. By fitting the conductance curve with Eq. (4.13) we can extract the D_{it} value. The D_{it} profile extracted by curve fitting is shown in Fig. 4.25(b). In case of sample 142 we can only extract the D_{it} profile for a very small energy range due to the conductance peak being small and only measurable for a small range of voltage bias values.



(a) (b)

Fig. 4.25 (a) Small signal ac interface state conductance G_p/ω as a function of ω and (b) extracted D_{it} profile for 145.

4.5. High-low Frequency Capacitance Method on SiC MOS-C

For high-low frequency capacitance measurement, we used samples NO0219, PSG225 and 145. All of the samples listed in table 4.1 are n-type samples. In order to minimize the effect of gate leakage current, we selected the device on the samples which had the smallest gate leakage current for the high-low frequency capacitance measurement. The capacitance data were measured with a Keithley package 82 system.

The Keithley package 82 system is a computer-controlled system of instruments designed to simultaneously measure quasistatic and high frequency CV on semiconductors. Keithley package 82 system includes a Keithley model 590 CV analyzer for high-frequency CV measurements, a model 595 quasistatic CV meter along with the necessary input coupler and low noise cables. A model 230-1 voltage source providing the DC bias voltage is also included. The package 82 system is controlled by a LabVIEW program.

Fig.4.26 shows the extracted D_{it} profile from high-low frequency capacitance measurement, compared to a conductance measurement for sample NO0219. As shown in Fig.4.2+, the extracted D_{it} profile from the high-low frequency capacitance measurement is lower than the profile derived from the conductance measurement within the same energy range. This is due to the frequency limit of the Keithley package 82 system. With high frequency only being 100 kHz the frequency is not high enough so that some fast traps will still respond, resulting in underestimating the D_{it} value. However, the high-low frequency capacitance measurement technique allows us to extract the D_{it} profile for a larger energy range.

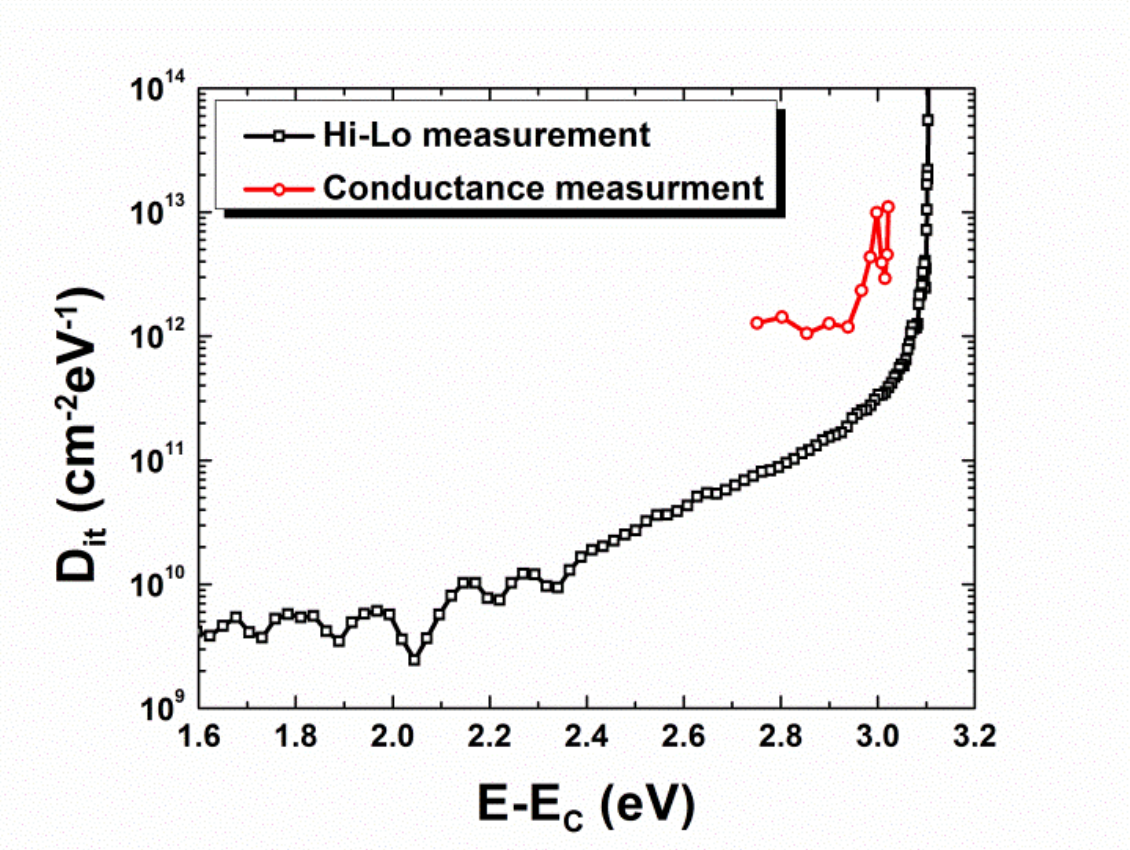


Fig. 4.26. Interface trapped charge density versus energy from the high-low frequency and conductance capacitance measurement on NO0219.

Fig. 4.27 shows the extracted D_{it} profile from high-low frequency capacitance measurement and conductance measurement on PSG225. As shown in Fig.4.27, for the same reason, the extracted D_{it} profile for the high-low frequency capacitance measurement is lower for the same energy range. Compare to NO0219, both high-low frequency capacitance measurement and conductance measurement technique show lower D_{it} values.

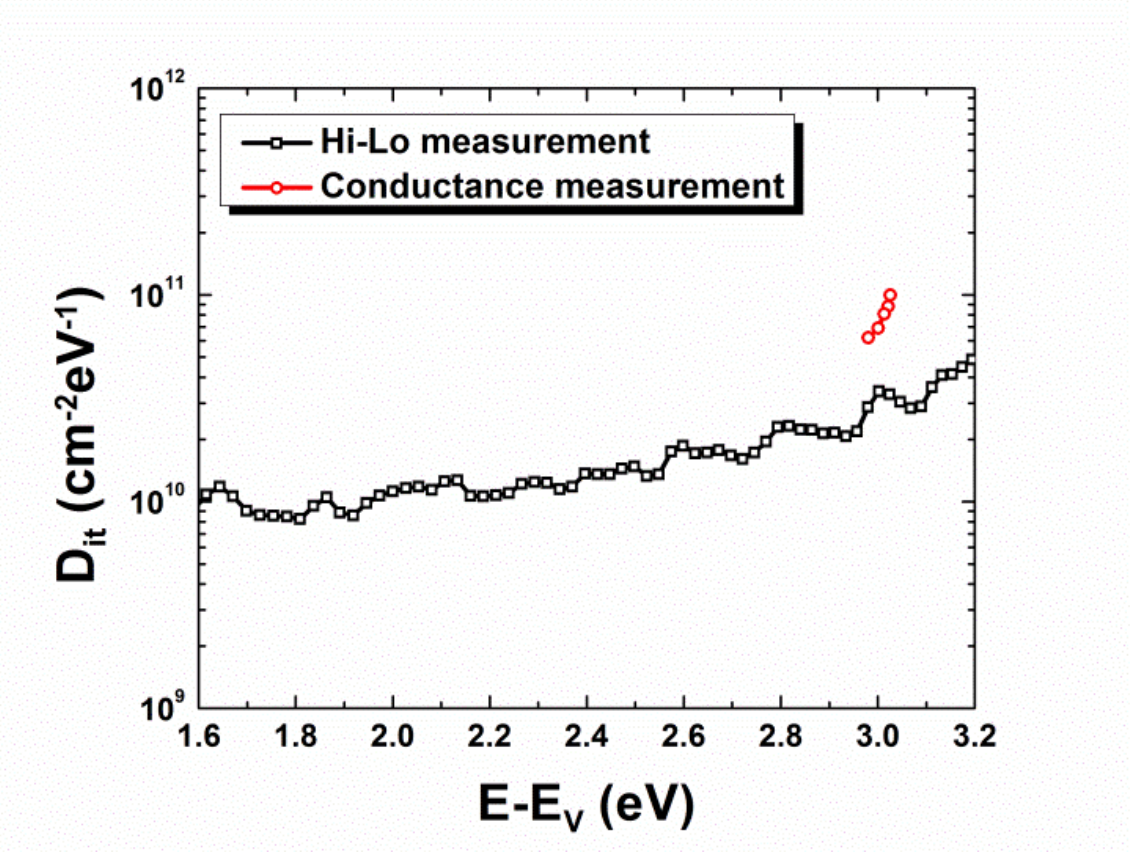


Fig. 4.27. Interface trapped charge density versus energy from the high-low frequency and conductance capacitance measurement on PSG225.

Fig.4.28 shows the extracted D_{it} profile from high-low frequency capacitance measurement and conductance measurement on sample 145. As shown in Fig.4.28, the extracted D_{it} profile for the high-low frequency capacitance measurement is higher than the value derived from the conductance measurement. This can be explained by the high-low frequency capacitance measurement measuring the traps responding at lower frequencies that can be probed via the conductance measurement as indicated in Fig. 4.25(a).

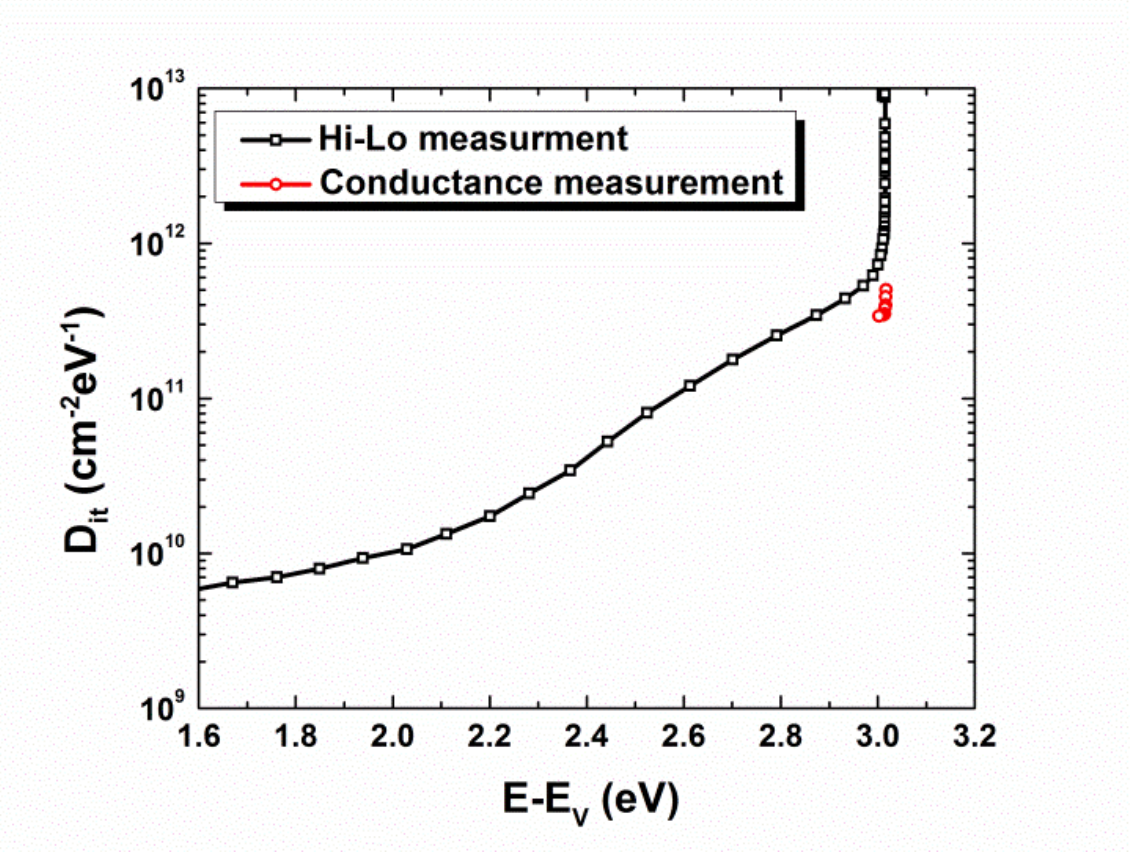


Fig. 4.28. Interface trapped charge density versus energy from the high-low frequency and conductance capacitance measurement on 145.

CHAPTER 5. FAST INTERFACE STATES IN NITROGEN- AND PHOSPHORUS-TREATED 4H-SIC MOS CAPACITORS

5.1. Fast Interface States

In the last chapter, we introduced the origins of the interface states at the oxide/semiconductor interface, discussed the methods to measure interface state density D_{it} used in this work and presented the measurement results obtained at room temperature or at elevated temperature. As mentioned in the first chapter, despite the progress in SiC device technology in recent years, the inversion channel mobility of 4H-SiC MOSFETs has been surprisingly low, still being much lower than the bulk mobility. The low inversion channel mobility of 4H-SiC MOSFETs has been suggested to be mainly due to the high density of interface states at the SiO_2/SiC interface [29]. As we discussed in chapter 3, the most common passivation method is to introduce nitrogen at the SiO_2/4H-SiC interface by using post-oxidation anneals in NO or N_2O [30]. Another nitridation method that limits the unwanted oxidation during NO annealing process is annealing in nitrogen plasma [52]. A lower D_{it} value has been reported by using these nitrogen based passivation methods. However, in some cases, although the measured D_{it} has been low, the effective channel mobility still remained low, contradicting the theory that the interface defect density is responsible for reduced channel mobility [31, 53].

It has been reported recently that increasing the nitrogen coverage at the interface during nitrogen post-oxidation annealing will potentially create additional fast interface states at the interface. These fast interface states have a shorter response time compared to

the conventional interface states. Due to the short response time of these states they are not detected by conventional D_{it} characterization techniques and protocols. In this chapter, we conducted measurements on samples at temperatures down to 100K using both the high-low frequency and conductance methods. As we lower the measurement temperature, the time constant of the interface states increases, shifting the response frequency into the experimentally accessible measurement range, allowing us to evaluate the D_{it} of the fast interface states. Assessing the samples at different temperatures enables characterization of the interface states at different energy levels. Similar to the analysis performed in the last chapter, the capture cross section of the fast interface states was extracted from the frequency of the peak conductance. The measurements were repeated on samples passivated with phosphorus to determine if PSG-SiO_2 also contains fast interface states.

5.2. Response Time of Interface States in Wide Bandgap Semiconductor

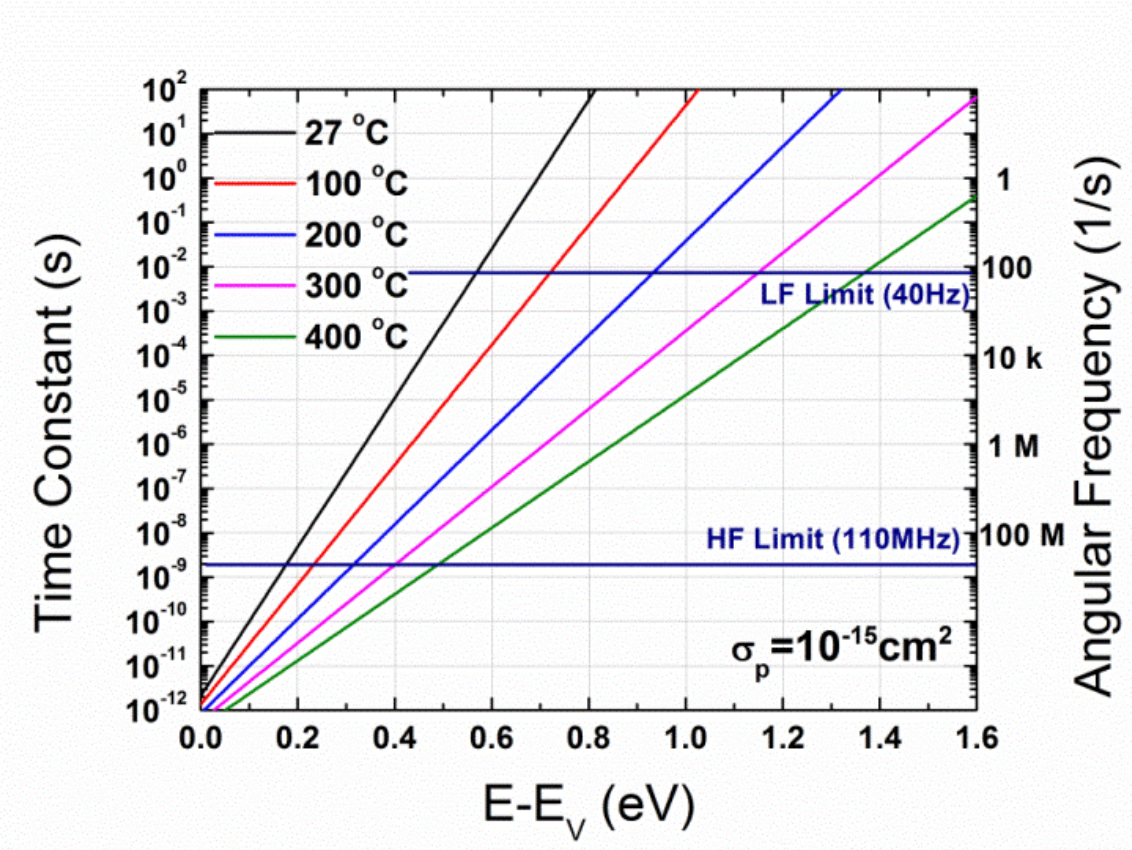


Fig. 5.1. Time constant for holes to emit from an interface state to the valence band in a p-type 4H-SiC. Capture cross section for holes is 10^{-15} cm^2. The horizontal lines indicate the frequency limitation of the Agilent 4294 impedance meter.

In this section, we discuss the response time of the interface states in a silicon carbide MOS device. Response times of interface states increases exponentially with the energy from the band edge towards the middle of the bandgap. The response times of interface states deep in the bandgap can be extremely long in wide bandgap semiconductors such as

silicon carbide. The time constant for an interface state to emit a hole to the valence band in a p-type semiconductor is given by [3]

$$\tau_p(E) = \frac{1}{\sigma_p v_T N_V} exp\left(\frac{E-E_V}{kT}\right) \quad (5.1)$$

where σ_p is the capture cross section for holes, v_T is the electron thermal velocity, N_V is the valence band effective density-of-states, k is Boltzmann's constant, T is the absolute temperature and $(E - E_V)$ is the energy of the interface state relative to the energy of the valence band edge.

The time constants for holes to emit from an interface state to the valence band in a p-type semiconductor for several temperatures are calculated with Eq. (5.1) and plotted in Fig. 5.1. The right-hand axis is the angular frequency corresponding to the interface state time constant. In Fig. 5.1, we assume that the interface state capture cross section for holes σ_p is constant throughout the entire bandgap, although σ_p has different values for different energies. Here we chose $\sigma_p = 10^{-15}\ cm^2$, which is a reasonable number for Silicon MOS devices. The horizontal lines indicate the frequency limitation of the Agilent 4294A impedance meter.

In the past, in order to extract the conventional interface state density D_{it} for a wider energy range, people had to decrease the interface states response time by increasing the measurement temperature. Theoretically, we should be able to extract D_{it} throughout the entire bandgap by elevating the measurement temperature to 400 °C and measuring on both n-type and p-type samples. The capture cross section for both electrons σ_n and holes σ_p can also be extracted using n-type and p-type samples. As the result shown in the last

chapter, we are able to extract D_{it} of our 4H-SiC samples for a wider range at room temperature due to the effect of the mobile ions in the oxide layer.

For measuring the fast interface states and extracting its D_{it}, instead of increasing the measurement temperature to decrease the interface state response time, we have to decrease the measurement temperature to increase response time of the fast interface states. Also, the capture cross section of the fast interface states can be extracted as well when the sample is cooled. More details of how to measure the fast interface states will be discussed later in this chapter.

5.3. Measurements of Fast Interface States

Before discussing how to measure the fast interface states, we first have to address some details of the sample preparation. The MOS capacitor samples investigated in this chapter were fabricated by Prof. Sarit Dhar of the Auburn University Physics Department. These MOS capacitor samples underwent the following interface passivation processes: (1) NO annealing (2) N plasma annealing (3) phosphosilicate glass (PSG) treatment. The basic ideas behind these three passivation processes have been discussed in chapter 3. A dry oxide layer was grown at 1150°C for the NO and PSG capacitor samples, the oxide thicknesses are ~60 nm. For the NO capacitor sample, following the oxidation process, nitric oxide annealing was performed at 1175°C for 2 hours. In case of the PSG capacitor samples, the oxides were annealed at 1000°C in N_2, which itself was bubbled through a $POCl_3$ bubbler maintained at 15°C. During this annealing, oxygen flowed simultaneously into the furnace tube. For comparison, there were two different $POCl_3$ annealing times were used: Sample 'PSG11' was annealed for 10 min and sample 'PSG12' for 15 min. For sample PSG11 and PSG12, the effective oxide thicknesses (EOT) were 61 nm and 70 nm respectively. The larger oxide thickness of PSG12 compared to PSG11 can be attributed to additional thickening of the oxide in $POCl_3$ [32]. Following the $POCl_3$ annealing, both PSG capacitor samples were annealed at 1000°C in pure N_2 (PSG11 for 30 minutes and PSG12 for 50 minutes). As for the N plasma process capacitor sample, first, a thin ~15 nm oxide layer has been formed by dry oxidation, then the sample was annealed in a N plasma annealing system at 1160°C for 4 hours. After the sample was annealed in N plasma, a TEOS-based LPCVD process was used to deposit additional oxide, the total oxide

thickness for the N plasma process capacitor sample is about ~60 nm. For all capacitor samples, molybdenum metal was sputtered for gate metallization and the contacts were defined using photolithography [54].

In this chapter, the samples were measured using an Agilent 4294A impedance analyzer for the conductance measurement and the Keithley system 82 for the high-low frequency capacitance method. Details of these two D_{it} extraction method has been discussed in the last chapter. In order to measure the samples at low temperature, the samples were mounted inside a LakeShore cryostat LTS-21 with the measurement instruments connected to the device under test via coaxial cables wired into the chamber via SMA vacuum feedthroughs. The temperature was controlled by a LakeShore temperature controller DRC-84C. The samples were measured at different temperatures from room temperature to 100K [54].

For the conductance measurement, the frequency sweep from 40Hz to 10MHz at different gate voltages with a 25 mV small-signal voltage. The capacitance and conductance were measured at all measurement frequencies in strong accumulation to determine the parasitic correction. This admittance was then subtracted from measurements taken in depletion [44]. The interface state density D_{it} and the interface state time constant τ have been extracted by fitting the experimental results with Eq. (4.13) [38, 42, 43]. For the samples studied in this chapter, the standard deviation of surface potential σ ranges between values of 2.5 to 4. The energy level of the extracted interface state was calculated from the depletion layer capacitance using Eq. (4.14) and Eq. (4.15). The capture cross section σ_c of the extracted interface state was calculated from τ by using Eq. (5.1). By

lowering the measurement temperature below room temperature, τ increased, allowing the conductance peak to shift within the measurable frequency range [54].

For the high-low frequency capacitance method, the high frequency we used was 100 kHz. In our case, we can only extract the interface states that respond faster than the low-frequency signal and slower than the high-frequency signal [55]. Similar to the case of the conductance measurement, by lowering the measurement temperature, the fast responding interface state time constants can be shifted to lie in our accessible measurement range [54].

For of the MOS capacitor samples that underwent an NO anneal, a distinct peak in the G_p/ω versus ω plot was not observable at room temperature within the range of applied bias voltages. Biasing the MOS capacitor into strong accumulation did not cause a sufficient surface potential change that would result in a shift of the peak into the measurement frequency range. The fact that no distinct peak can be observed in the samples presented here can be interpreted by the interface states either responding faster than the maximum or slower than the minimum measurement frequency. By lowering the measurement temperature, fast interface states can be slowed down in response, shifting them into the measurement frequency range. Fig. 5.2 plots the conductance G_p/ω versus ω at four different temperatures lower then room temperature. We first observed a G_p/ω peak at 220K. By lowering the temperature further, we were able to observe more G_p/ω peak which represents the interface states closer to the conduction band edge. As shown in Fig. 5.2, for the interface states closer to the conduction band edge, its G_p/ω peak value is higher [54].

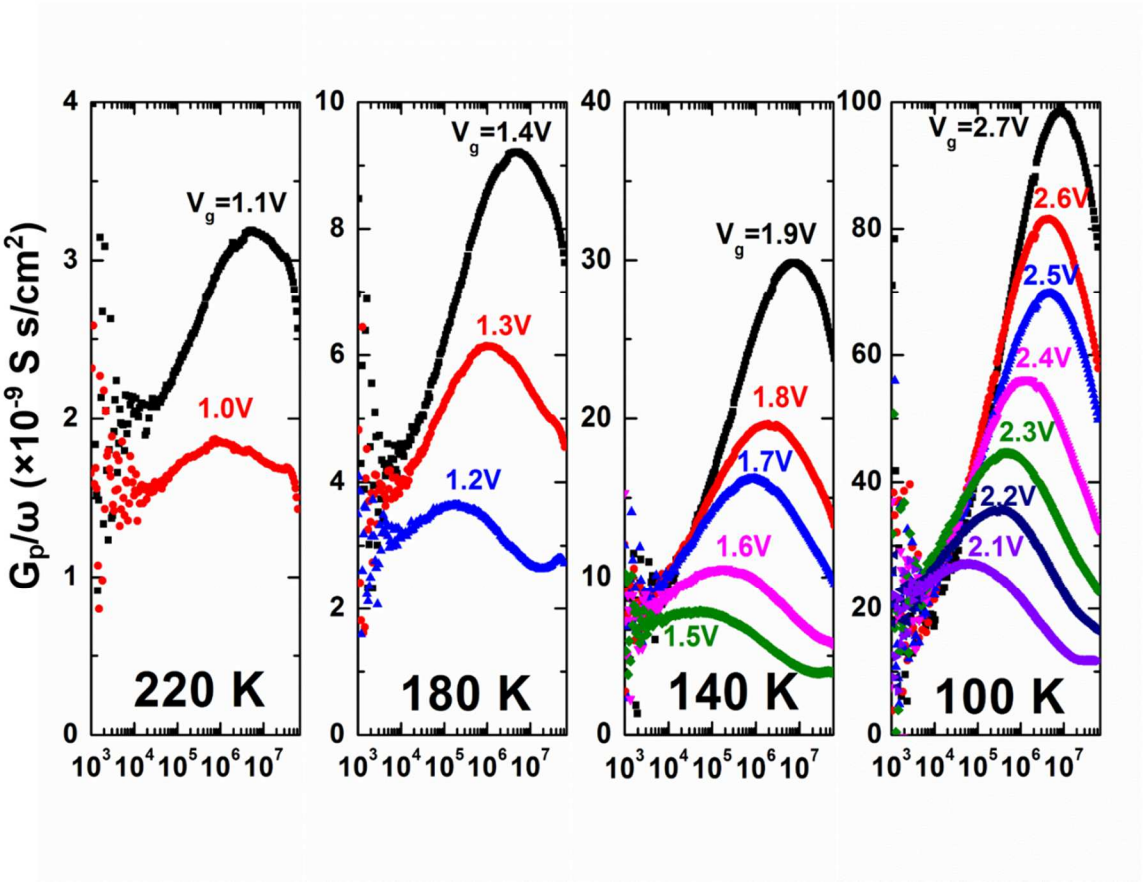


Fig. 5.2. The conductance G_p/ω versus ω at 220 K, 180 K, 140 K and 100 K measured on NO passivated sample [54].

For the MOS capacitor samples that underwent a nitrogen-plasma anneal, we found similar results with the MOS capacitor samples that underwent an NO anneal. There is no G_p/ω peak could be observed at room temperature. Fig. 5.3 shows the conductance G_p/ω versus ω at different temperatures measured on the N-plasma sample. G_p/ω peaks were observed at 220 K, 180 K, 140 K and 100 K. Similar to the NO-annealed sample, the peaks

measured at lower temperatures exhibit a higher G_p/ω peak value and represent interface states close to the conduction band [54].

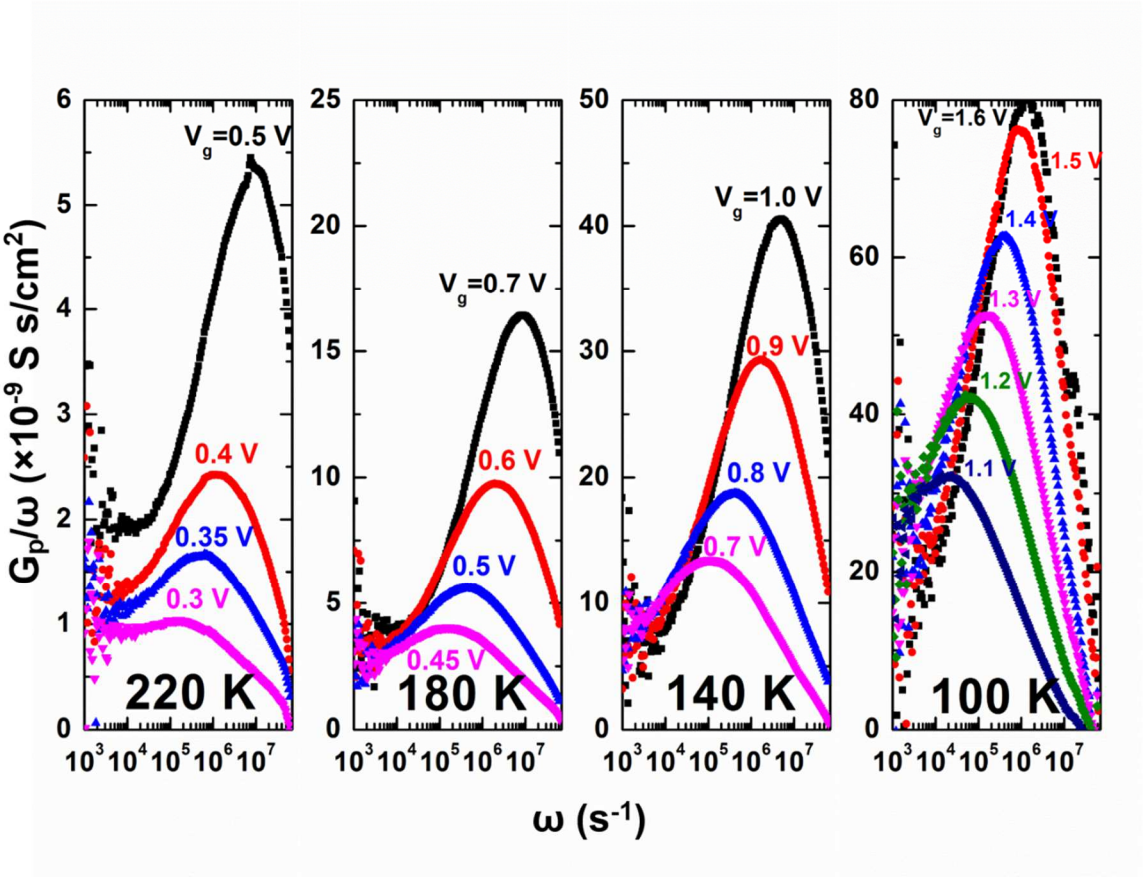


Fig. 5.3. The conductance G_p/ω versus ω at 220 K, 180 K, 140 K and 100 K measured on N-plasma passivated sample [54].

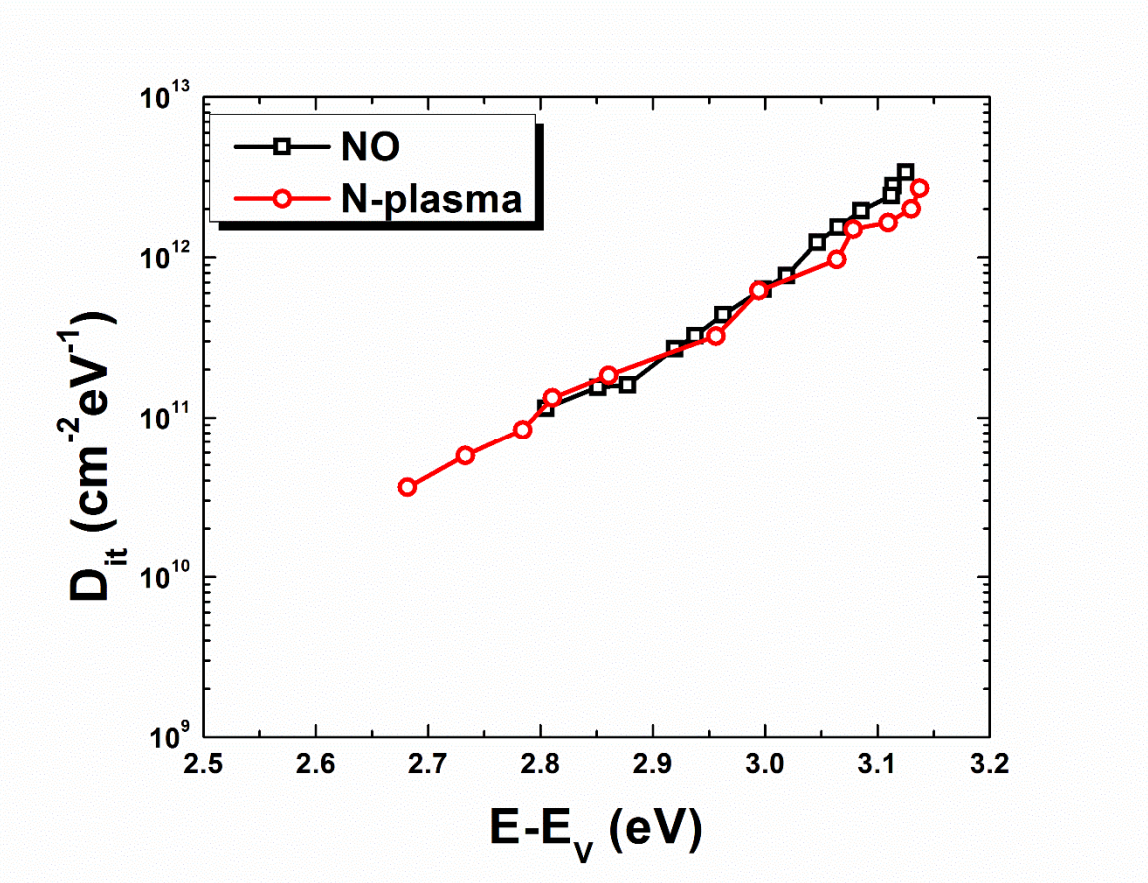
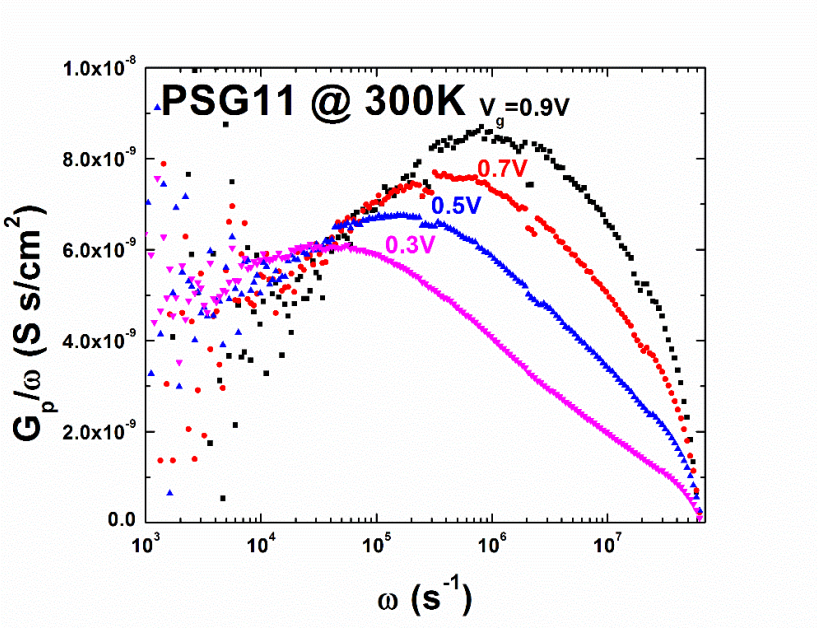
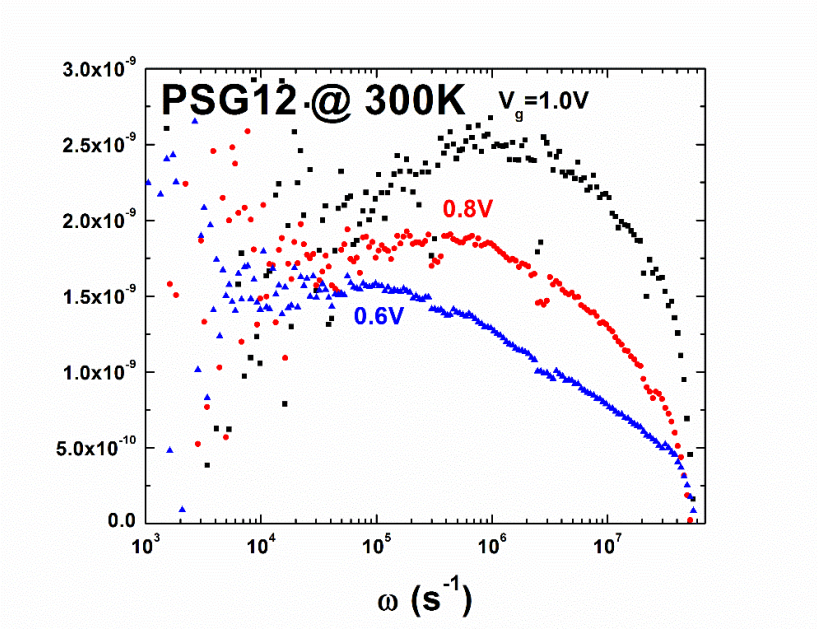


Fig. 5.4. Interface state density for NO and N-plasma sample extracted from the curves in Figs. 5.2 and 5.3 [54].



(a)



(b)

Fig. 5.5. The conductance G_p/ω versus ω at room temperature measured on sample (a) PSG11 and (b) PSG 12 [54].

Fig. 5.4 shows the extracted D_{it} values for NO and N-plasma samples. As shown in Fig. 5.4, the D_{it} values are very similar for the two different nitrogen-based passivation methods, with the N-plasma sample exhibiting a D_{it} that is slightly lower close to the conduction band edge [54].

For the MOS capacitor samples that underwent PSG passivation, contrary to the nitrogen passivated samples showed above, distinct peaks in the G_p/ω versus ω plot were observable at room temperature. Fig. 5.5 shows conductance G_p/ω versus ω at room temperature measured from PSG11 and PSG12. The interface states in the PSG samples could be detected at room temperature in our measured frequency range, suggesting that the interface states in the PSG passivated samples have a larger interface state time constant than the ones we measured in the nitrogen passivated samples. The curves in Fig. 5.5 represent interface states 0.2 to 0.3 eV below the conduction band edge. Further biasing into depletion moved the Fermi level deeper in the bandgap, resulting in the disappearance of a distinct peak in our measured frequency range due to the longer response time of the interface state deeper in the bandgap. The G_p/ω peaks shown in Fig. 5.5 for the PSG samples are lower than in the nitrogen passivated samples at the same energy level (shown in Fig. 5.2 and Fig. 5.3). This suggests that the D_{it} value is lower for the PSG samples. Also, the PSG12 sample shows a lower G_p/ω peak than the PSG11 sample at the same energy level, implying the PSG12 has a lower D_{it} value. As we lowered the measurement temperature, for both PSG11 and PSG12 sample, no distinct peak in the G_p/ω versus ω plot was observable within the range of applied bias voltages. This suggests that there are

no fast-responding interface states present the PSG/SiC interfaces, result in higher mobility for a PSG passivated sample [54].

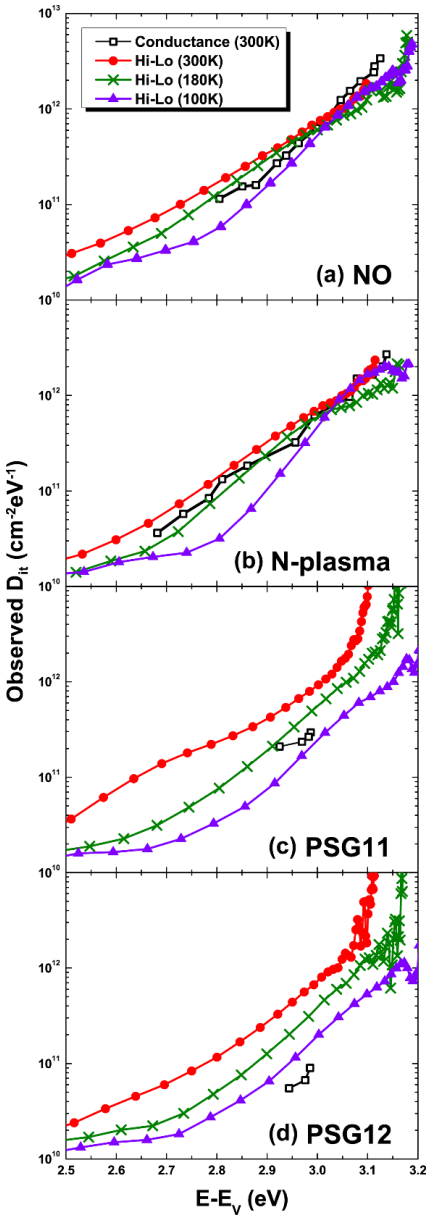


Fig. 5.6. Observed interface state density for (a) NO, (b) N-plasma, (c) PSG11 and (d) PSG12 sample extracted from the conductance method and the high-low capacitance method [54].

The D_{it} profile extracted from the NO- and N-plasma annealed samples as well as those from the PSG (PSG11 and PSG12) samples using both the conductance method and high-low frequency capacitance method are shown in Fig 5.6. For the NO and N-plasma passivated samples, the D_{it} value derived from the high-low frequency capacitance method at room temperature has a higher value compare to the D_{it} value derived from the conductance method for most of the measured energy range. As we lower the measurement temperature, the D_{it} value derived from the high-low capacitance method starts to decrease and falls below the value obtained using the conductance method. The high-low capacitance method integrates the interface states with different time constants in the measured frequency range. Thus, the extracted data reflects the combination of different types of interface states. In case of the room temperature measurements, the high-low capacitance method has the ability to probe interface states that are too slow for the conductance method to detect, since the lowest measurement frequency of Agilent 4924A is 40 Hz. By lowering the measurement temperature the already slow time constant interface/near interface states will react even slower, eventually becoming too slow for the high-low method to be able to detect it, since the integration time of the quasistatic capacitance meter is finite as well. This causes the D_{it} values derived from the high-low technique to decrease with temperature. On the other hand, lowering the measurement temperature will cause the fast time constant interface states to slow down to lie within our measurement frequency range. Thus, the D_{it} values in Fig. 5.6 extracted from the conductance method at low temperatures represent the contribution of fast interface states [54].

As shown in Fig. 5.6, for samples PSG11 and PSG12, as we lower the measurement temperature, the D_{it} value derived from the high-low capacitance method decreases faster compared to the nitrogen passivated samples. This is due to the lack of fast interface states in the PSG passivated samples. At room temperature, the D_{it} value derived from the high-low capacitance method is much higher than the D_{it} value derived from the conductance method, this indicates that there are interface states which have a response times that are too slow for the conductance method to detect, but these slower interface states can be measured by the high-low capacitance method at room temperature. As we decrease the measurement temperature, these slow interface states will then become too slow for both the high-low capacitance method and the conductance method to detect. These results indicate that the higher channel mobility in PSG MOSFETs is due to a lower D_{it} value of fast interface states at the PSG/SiC interface. This is consistent with recent publication that reports the correlation between the channel mobility and the fast interface state in nitrogen passivated MOSFETs fabricated on a different crystal face of 4H-SiC [54].

Fig. 5.7 shows observed D_{it} extracted by high-low capacitance measurement at 300 K for the NO- and N-plasma annealed samples as well as those from the PSG PSG11 and PSG12 samples, the observed D_{it} value does not show much of a difference at room temperature [54].

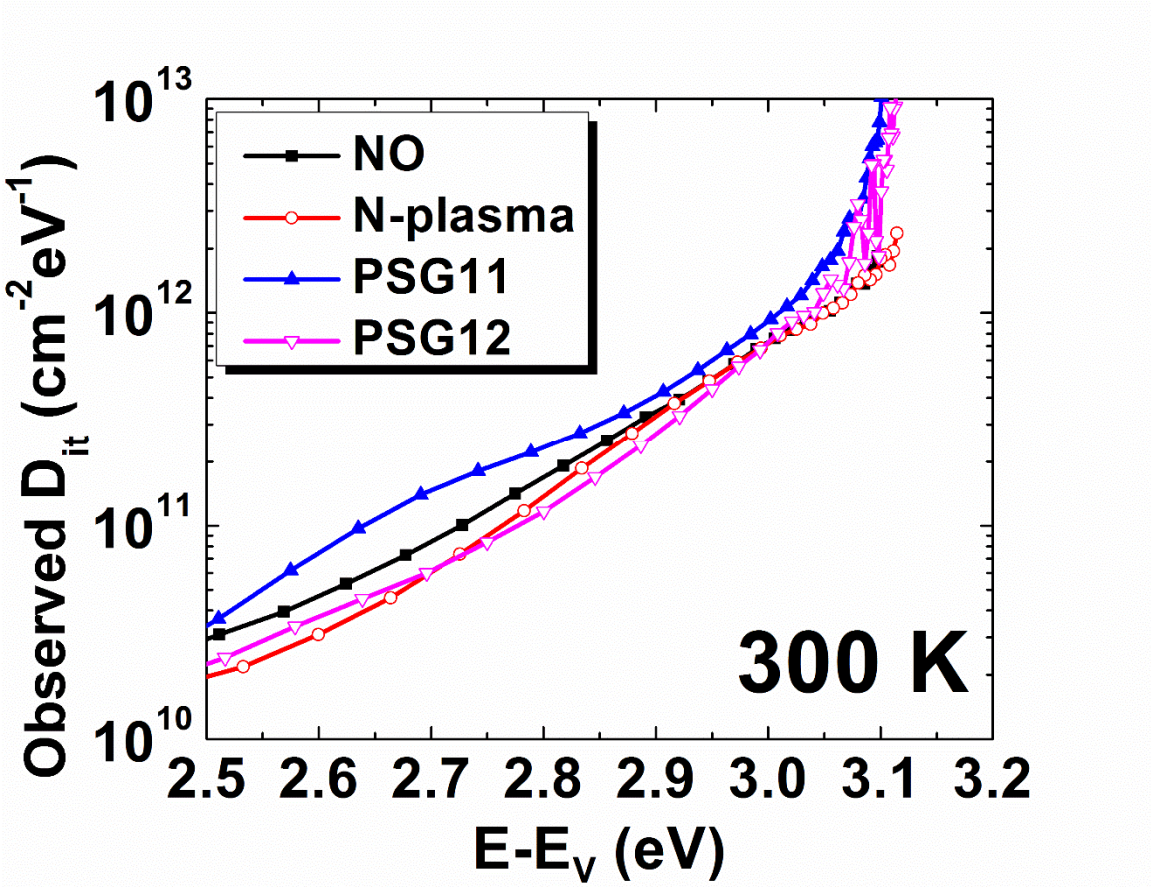


Fig. 5.7. Comparison of observed interface state density for NO, N-plasma, PSG11 and PSG12 samples extracted by high-low frequency capacitance measurement at 300 K [54].

The interface state capture cross-section (σ_c) for the NO, N-plasma and PSG annealed samples are also extracted by using the conductance method. As shown in Fig. 5.8, σ_c for the NO and N-plasma annealed samples has an exponential dependence on energy and ranges from 10^{-17} to 10^{-10} cm^2 in the measured energy. Such large values of σ_c have also been reported by other gropes [35, 56]. For the PSG annealed samples, the extracted σ_c value are in the lower 10^{-18} cm^2 range, which is much smaller compared to the values for

the nitrogen-based annealed samples in the same energy range. This indicates that the interface states which are measured by using the conductance method for the nitrogen-based annealed samples and the PSG annealed samples are different types of interface states [54].

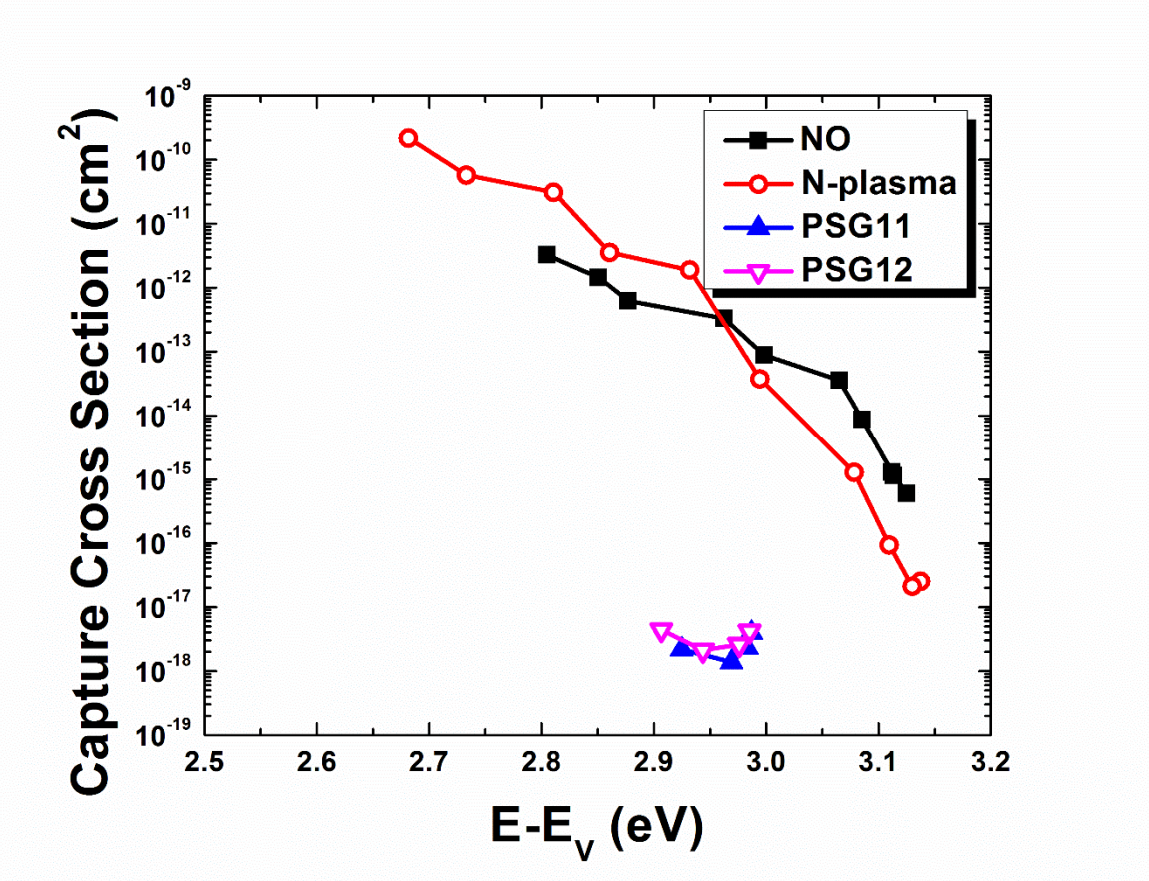


Fig. 5.8. Capture cross-section for fast interface states in NO and N-plasma samples and regular states in PSG samples [54].

5.4. Conclusion

In this chapter, we have measured the interface state densities at the SiO_2/SiC interface from room temperature to 100K using both the conductance and the high-low frequency methods for various SiC MOS samples. These samples were passivated by two nitrogen-based techniques (NO and nitrogen-plasma) and the PSG technique. We have successfully measured and confirmed the existence of fast interface states in the SiC MOS samples which underwent nitrogen-based passivation, the D_{it} profiles for these samples has been extracted by both conductance and high-low frequency measurements. On the other hand, no fast interface states were observed in PSG-passivated samples using the same characterization methods. However, conventional interface states with time constants similar to the interface states found in silicon samples have been observed at room temperature [54].

Based on our findings, there are two types of interface states present at the SiC/SiO_2 interface. These two types of interface sates shows different energy dependencies of the capture cross section, this indicates that these two types of interface states have different origins. For the fast interface states, its capture cross section has an exponential dependence on energy, and for conventional interface states, the capture cross section does not show a clear dependence on energy. Furthermore, compared to the fast interface states, the conventional interface state density is several orders of magnitude smaller. Also, the interface states which have very long response times in all the samples can only be detected by the high-low frequency capacitance method but not by the conductance method [54].

CHAPTER 6. FUTURE WORK

6.1. Future work

In this work, we successfully measured the interface state density D_{it} for various energy ranges for both n- and p-type substrate SiC MOS capacitors using the conductance measurement and the high-low frequency capacitance method under different conditions and protocols. The D_{it} profile extracted from samples which underwent different passivation process has also been compared side by side for the purpose of determining the better passivation method. The presence of fast interface states has been confirmed and their D_{it} profile has been extracted from the samples that underwent nitrogen based annealing processes. On the contrary, no fast interface state were found in the samples that underwent the PSG annealing. We also discovered the effect of mobile ions in the oxide layer on the response time of the interface states. Although this work helps us to understand some important features of a SiC MOS system, it also points out several topics that still cannot be fully explained. Thus additional work is required in order to understand and further resolve these topics. We list some of the topics and our suggestions on how to move forward:

1. It remains unclear where exactly the near-interface state are located in a SiC MOS device, i.e if these states are in the substrate or in the oxide layer close to the SiC/SiO_2 interface. The profile of these near-interface states can potentially be extracted by using deep-level transient spectroscopy (DLTS) and the charge pumping method. The challenge using these two methods is that both methods require a MOSFET structure to yield meaningful results. Thus, SiC MOSFET

samples need to be fabricated and characterized in the future. An introduction to the DLTS technique is presented in the next section.

2. The origin and the chemical nature of the fast interface states remains largely unknown. It has been suggested that nitrogen at the interface and the near interface oxide will potentially increase the concentration of fast interface states. More work has to be done to fully understand the nature of the fast interface states.
3. Interface states which respond slower than conventional interface states have also been observed. In order to completely measure and extract the density profile, different methods or protocols must be applied. Increasing the measurement temperature and/or lowering the measurement frequency might allow us to obtain the density profile of these slow interface states.
4. The nature of how mobile ions effect the response time of the interface state isn't fully understood yet. However, exploring this effect allows us to extract the D_{it} profile for a much larger energy range and can potentially be used for other wide bandgap materials in the future.
5. The lack of fast interface states in the samples that underwent PSG passivation leads to higher field-effect mobility. Different dopants could be used in the future to avoid creating fast interface states and potentially achieve higher field-effect mobility and a more robust oxide layer.
6. By benefiting from advances in Si technology, other alternative insulators besides SiO_2 could be employed within the SiC MOS system. For example, a high-k dielectric on top of the native SiO_2 might achieve higher gate control and lower gate leakage current.

6.2. Deep-Level Transient Spectroscopy

4.7.1 Conventional Deep-Level Transient Spectroscopy

Sah and his students developed the early C-t and I-t measurement and methods [57, 58]. The initial method were single-shot measurements, the measurement was time-consuming and tediously long. In 1974, Lang proposed the dual-gate integrator or boxcar approach named Deep-Level Transient Spectroscopy (DLTS), it was the first one among these DLTS techniques [59-61].

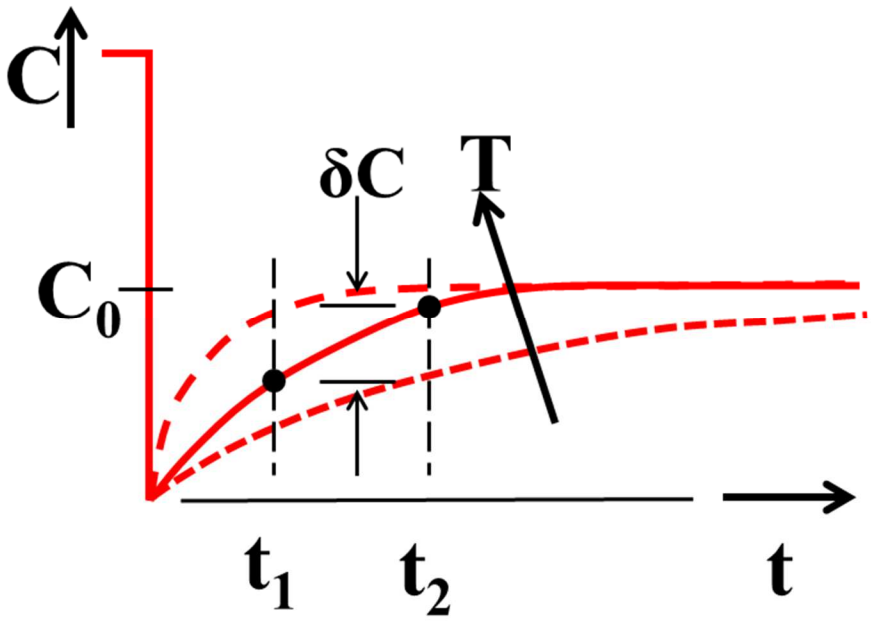


Fig. 6.1. Capacitance versus time at different temperature. t_1 and t_2 are the sampling time.

For this technique, the rate window concept was introduced to the deep level impurity characterization. Here we use the capacitance transients to explain DLTS. Assuming the C-t transient follows the exponential time dependence [27]

$$C(t) = C_0\left[1 - \frac{n_T}{2N_D} exp\left(-\frac{t}{\tau_e}\right)\right] \quad (6.1)$$

where C_0 is the capacitance of a device with no deep-level impurities at reverse bias, τ_e depends on temperature as

$$\tau_e = \frac{exp((E_c - E_T)/kT)}{\gamma_n \sigma_n T^2} \quad (6.2)$$

When the temperature increases, the time constant τ_e decreases, shown in Fig. 6.1.

During the measurement, the capacitance decay waveform is usually corrupted by noise, thus the ability to extract the signal from the noise in an automated manner is the core of DLTS. DLTS is a correlation technique, the correlator output is

$$\delta C = \frac{1}{T}\int_0^T f(t)w(t)dt = \frac{1}{T}\int_0^T \left(1 - \frac{n_T(0)}{2N_D} exp\left(-\frac{t}{\tau_e}\right)\right) w(t)dt \quad (6.3)$$

where T is the period, $w(t)$ is the weighting function and we use Eq. (6.1) for $f(t)$.

For boxcar DLTS, the capacitance difference between $t=t_1$ and $t=t_2$ as shown in Fig 6.1 is a standard output feature of a double boxcar instrument, i.e. $\delta C = C(t_1) - C(t_2)$. The device is pulsed between zero and reverse bias repetitively when the temperature is scanning slowly. At low and high temperature, there is almost no capacitance difference between $t=t_1$ and $t=t_2$ due to very slow and very fast transients. As you scan through the

temperature, capacitance difference δC will pass through a maximum value as a function of temperature. By using $(t) = \delta(t - t_1) - \delta(t - t_2)$, Eq. (6.3) become

$$\delta C = C(t_1) - C(t_2) = \frac{n_T(0)}{2N_D} C_0 \left(exp\left(-\frac{t_2}{\tau_e}\right) - exp\left(-\frac{t_1}{\tau_e}\right) \right) \qquad (6.4)$$

where $T = t_1 - t_2$ in Eq. (6.3).

The maximum capacitance difference δC_{max} occurs at a particular temperature. By differentiating Eq. (4.37) with respect to time constant τ_e and setting the result to zero, we can get the maximum time constant $\tau_{e,max}$ at δC_{max} as

$$\tau_{e,max} = \frac{t_2 - t_1}{\ln(t_2/t_1)} \qquad (6.5)$$

The signal baseline does not need to be known, because in Eq. (6.5), $\tau_{e,max}$ is independent of the capacitance magnitude. For a given gate setting t_1 and t_2, we can generate a series of C-t curves at different temperatures and generate one value of τ_e corresponding to a particular temperature. This will give us one point on a $\ln \tau_e T^2$ versus $1/T$ plot. By changing to another gate setting t_1 and t_2 and a repeat of the measurement sequence, we can generate another point. After several times of repeating the sequence, we can obtain a series of points that allows us to generate an Arrhenius plot. Fig. 6.2 shows an example of the δC-t plot with the t_2/t_1 fixed for varies of t_1 and t_2 values.

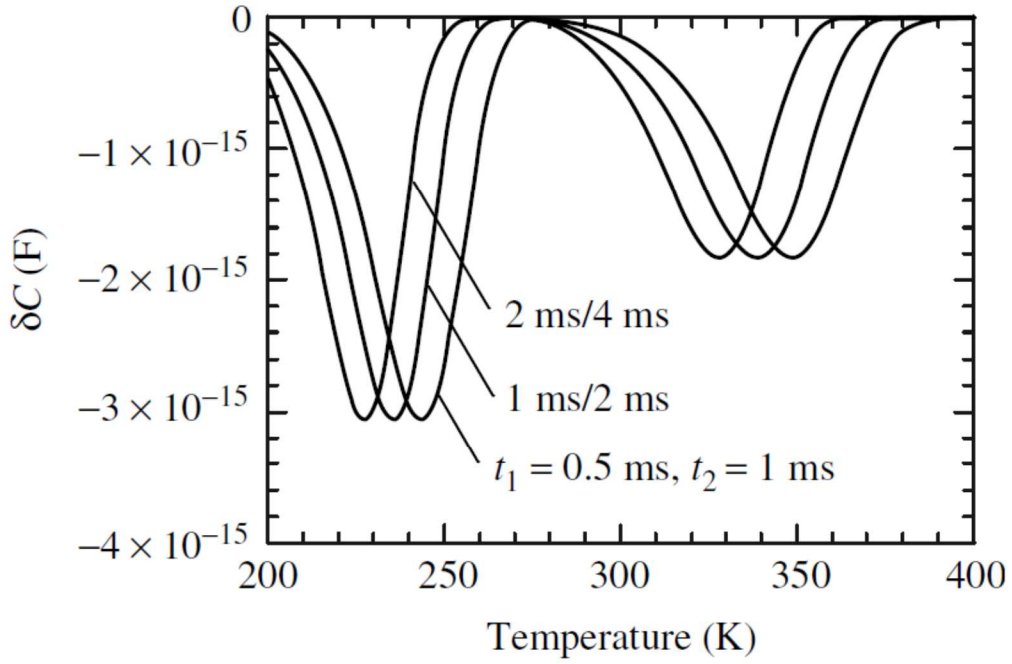


Fig. 6.2. DLTS spectra for fixed t_2/t_1 and different t_1 and t_2. [27]

The signal to noise ratio is proportional to the square root of the gate width. In order to lower the noise, the gate width should be relatively wide [62]. Eq. (6.5) then needs to be modified to

$$\tau_{e,max} = \frac{(t_2+\Delta t)-(t_1+\Delta t)}{\ln((t_2+\Delta t)/(t_1+\Delta t))} \tag{6.6}$$

where Δt is the gate width [63].

We can derive the impurity density from the maximum capacitance difference δC_{max} of the C-t curves, with $\delta C_{max} = \delta C$, assuming $n_T(0) = N_T$. We can derive N_T from Eq. (6.5) and Eq. (6.6)

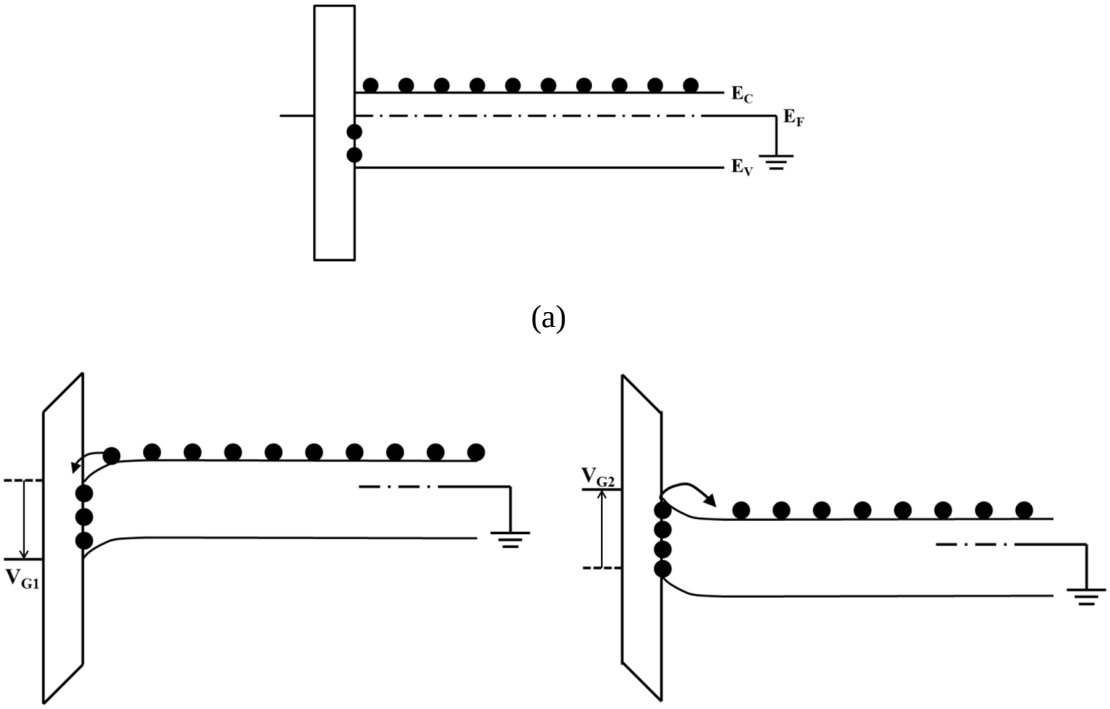
$$N_T = \frac{\delta C_{max}}{C_0} \frac{2N_D exp\{[r/(r-1)]\ln(r)\}}{1-r} = \frac{\delta C_{max}}{C_0} \frac{2r^{r/(r-1)}}{1-r} N_D \qquad (6.7)$$

where $r = t_2/t_1$. $r = 2$ is a common ration for this measurement.

$\delta C_{max}/C_0 \approx 10^{-5}$ can be detected by a DLTS system, allowing us to determine trap densities on the order of $10^{-5}N_D$. $\delta C_{max}/C_0$ as low as 10^{-6} can be measured by a high-sensitivity bridge. Also, capacitance meters should feature modified response times in order to measure faster transients [64].

4.7.2 Interface Trapped Charge DLTS

Interface trapped charge DLTS employs identical instrumentation to what is used for bulk deep-level DLTS. Because interface traps have an energy distribution throughout the band gap and bulk traps have discrete energy levels, the data interpretation for interface trapped charge DLTS is different than bulk deep-level DLTS. Fig. 6.3 illustrates the concept of interface trapped charge majority carrier DLTS for the MOS capacitor. In Fig. 6.3 (b), electrons are captured and occupy the interface traps when a positive bias is applied. In Fig. 6.3 (c), electrons are emitted from the interface traps to the conduction band in deep depletion when a negative bias is applied. The emitted electrons will result in a capacitance, current or charge transient. The emission of the electrons from interface traps in the upper band gap will dominates, although electrons are emitted over a broad energy spectrum. DLTS is a very sensitive technique, it can measure the interface trap density on the order of 10^9 $cm^{-2}eV^{-1}$.



(a)

(b) (c)

Fig. 6.3. n-substrate MOS capacitor band diagram with (a) no bias, (b) positive bias and (c) negative bias. After ref. [27]

This technique was first implemented using MOFETs [65]. As a three terminal device, MOSFETs as a test device have an advantage over MOS capacitors as a test device. By reverse biasing the source and drain, minority holes will be collected by the source and drain and will not interfere with the majority electrons that are captured and emitted. This allows us to characterize the interface traps located in the upper band gap by majority electrons. Also, by forward biasing the source and drain and forming an inversion layer, the interface traps will be filled with minority holes. This allows us to characterize the interface traps located in the lower band gap by minority holes. Without source and drain, this is impossible to accomplish with just a MOS capacitor due to lack of a minority carrier

source. The majority carrier interface trap DLTS measurements will be interfered within an inversion layer in MOS capacitor because of thermal electron-hole-pairs generation, especially under high temperature and high electron-hole-pairs generation rates.

Nevertheless, MOS capacitors were used for interface trap characterization [66, 67]. Interface trapped charge DLTS measurements are independent of surface potential fluctuations, unlike the conductance measurement discuss earlier. Compare to diodes, MOS capacitors require a more complex derivation of the capacitance expression. For $q^2 D_{it} = C_{it} \ll C_{ox}$ and $\delta C = C_{hf}(t_1) - C_{hf}(t_2) \ll C_{hf}$ [27]

$$\delta C = \frac{C_{hf}^3}{K_s \varepsilon_0 N_D C_{ox}} \int_{-\infty}^{\infty} D_{it} \left(e^{-t_2/\tau_e} - e^{-t_1/\tau_e} \right) dE_{it} \qquad (6.8)$$

Where

$$\tau_e = \frac{e^{(E_C - E_{it})/kT}}{\gamma_n \sigma_n T^2} \qquad (6.9)$$

E_{it} is the energy of the interface traps. Eq. (6.5) gives us the maximum emission time for an interface trap, when $\tau_{e,max}$ corresponds to $E_{it,max}$, Eq. (6.9) become

$$E_{it,max} = E_C - kT \ln \left(\frac{\gamma_n \sigma_n T^2 (t_2 - t_1)}{\ln(t_2/t_1)} \right) \qquad (6.10)$$

where $E_{it,max}$ is a sharp peak. In Eq. (6.10), the electron capture cross-section is not a strong function of energy. In Eq. (4.41), D_{it} can be considered as a constant if the D_{it} value changes slowly in a few kT energy range around $E_{it,max}$. D_{it} can be then taken outside of the integral and the remaining integral will become

$$\int_{-\infty}^{\infty}\left(e^{-t_2/\tau_e}-e^{-t_1/\tau_e}\right)dE_{it}=-kT\ln(t_2/t_1) \tag{6.11}$$

and Eq. (6.8) becomes

$$\delta C\approx-\frac{C_{hf}^3}{K_s\varepsilon_0 N_D C_{ox}}kTD_{it}\ln(t_2/t_1) \tag{6.12}$$

From Eq. (6.12), D_{it} is

$$D_{it}=-\frac{K_s\varepsilon_0 N_D C_{ox}}{kTC_{hf}^3\ln(t_2/t_1)}\delta C \tag{6.13}$$

Eq. (6.13) is determined by the interface trap emitted electrons in time Δt in the energy interval $\Delta E=kT\ln(t_2/t_1)$ at $E_{it,max}$. By varying t_1 and t_2, we can plot D_{it} versus energy. For a chosen t_1 and t_2 set, D_{it} and E_{it} can be obtained from Eq. (6.13) and Eq. (6.9). For samples containing both interface and bulk traps, we can distinguish interface traps from the bulk traps by the shape and the peak temperature of the DLTS plot [68].

Constant capacitance DLTS is another DLTS technique that has been used to measure interface traps [69]. For constant capacitance DLTS,

$$D_{it} = \frac{C_{ox}}{qkTA\ln(t_2/t_1)}\Delta V_G \tag{6.14}$$

where A is the device area and ΔV_G is the value of how much the gate voltage has to be changed to maintain a constant capacitance. Compared to Eq. (6.13), Eq. (6.14) is easier to use because there is no high-frequency capacitance and doping density needed to derive D_{it}.

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