Modeling and Simulation Tools for Aging Effects in Scaled CMOS Design

by

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ABSTRACT

The aging process due to Bias Temperature Instability (both NBTI and PBTI) and Channel Hot Carrier (CHC) is a key limiting factor of circuit lifetime in CMOS design. Threshold voltage shift due to BTI is a strong function of stress voltage and temperature complicating stress and recovery prediction. This poses a unique challenge for long-term aging prediction for wide range of stress patterns. Traditional approaches usually resort to an average stress waveform to simplify the lifetime prediction. They are efficient, but fail to capture circuit operation, especially under dynamic voltage scaling (DVS) or in analog/mixed signal designs where the stress waveform is much more random. This work presents a suite of modelling solutions for BTI that enable aging simulation under all possible stress conditions. Key features of this work are compact models to predict BTI aging based on Reaction-Diffusion theory when the stress voltage is varying. The results to both reaction-diffusion (RD) and trapping-detrapping (TD) mechanisms are presented to cover underlying physics. Silicon validation of these models is performed at 28nm, 45nm and 65nm technology nodes, at both device and circuit levels. Efficient simulation leveraging the BTI models under DVS and random input waveform is applied to both digital and analog representative circuits such as ring oscillators and LNA. Both physical mechanisms are combined into a unified model which improves prediction accuracy at 45nm and 65nm nodes. Critical failure condition is also illustrated based on NBTI and PBTI at 28nm. A comprehensive picture for duty cycle shift is shown. DC stress under clock gating schemes results in monotonic shift in duty cycle which an AC stress causes duty cycle to converge close to 50% value. Proposed work provides a general and comprehensive solution to aging analysis under random stress patterns under BTI.

Channel hot carrier (CHC) is another dominant degradation mechanism which affects analog and mixed signal circuits (AMS) as transistor operates continuously in saturation condition. New model is proposed to account for e-e scattering in advanced technology nodes due to high gate electric field. The model is validated with 28nm and 65nm thick oxide data for different stress voltages. It demonstrates shift in worst case CHC condition to $V_{gs}=V_{ds}$ from $V_{gs}=0.5V_{ds}$. A novel iteration based aging simulation framework for AMS designs is proposed which eliminates limitation for conventional reliability tools. This approach helps us identify a unique positive feedback mechanism termed as Bias Runaway. Bias runaway, is rapid increase of the bias voltage in AMS circuits which occurs when the feedback between the bias current and the effect of channel hot carrier turns into positive. The degradation of CHC is a gradual process but under specific circumstances, the degradation rate can be dramatically accelerated. Such a catastrophic phenomenon is highly sensitive to the initial operation condition, as well as transistor gate length. Based on 65nm silicon data, our work investigates the critical condition that triggers bias runaway, and the impact of gate length tuning. We develop new compact models as well as the simulation methodology for circuit diagnosis, and propose design solutions and the trade-offs to avoid bias runaway, which is vitally important to reliable AMS designs.

DEDICATION

To my parents and loving sister

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CHAPTER 1

INTRODUCTION

1.1 Overview: Reliability and Variability

Moore in 1965 predicted that the number of transistors that can be placed on an integrated circuit will be approximately doubled every two years as shown in Figure 1.1 [1]. Moore's law has been the driving force for technological advancement and innovation in the semiconductor industry for over 5 decades and is expected to self-fulfill this prophecy for another decade or perhaps more.

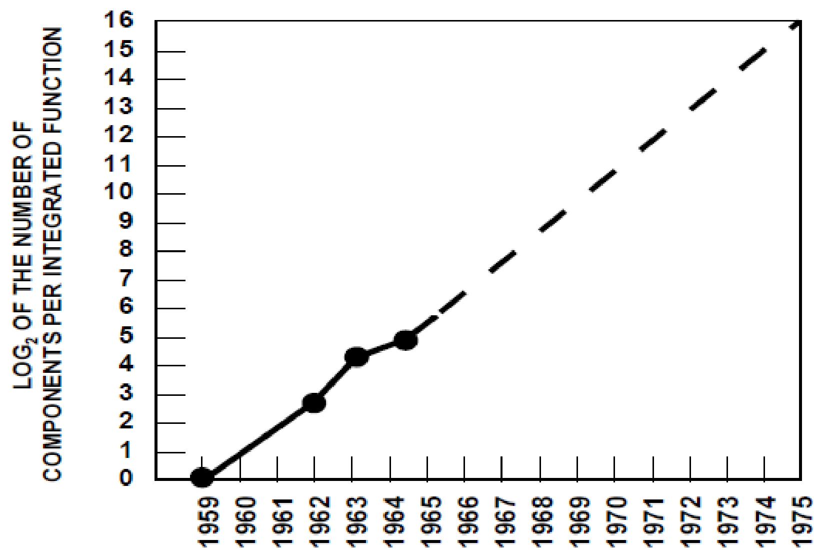


Figure 1.1. Doubling of transistor vs years with technology scaling [1].

According to ITRS 2013 report, device cost and performance will continue to be strongly correlated to dimensional and functional scaling of CMOS as information processing technology is driving the semiconductor industry into a broadening spectrum of new applications [2]. Extreme nano-scaled devices pushing physical limits at 7nm and

5nm are expected to go into high volume manufacturing by year 2017 and 2019 respectively [2]. The increased transistor count has directly led to improved capabilities in the digital devices such as processing speed, power, memory capacity etc. At present microprocessors pack close to a billion transistors and have processing speeds of up to 4GHz and above. Integrating of both analog and digital circuits on a single platform called System on Chip (SoC) allows designers to extract high performance.

However, aggressive scaling of CMOS technology brings forth multiple variability and reliability issues. The variability effects observed with technology scaling are layout dependent stress, high-K metal gate effects (HK/MG), random dopant fluctuations (RDF), line edge roughness (LER), and random telegraph noise (RTN) which primarily affects the threshold voltage or drain current of a device to a first order as seen in Figure 1.2 [4][5]. These effects are exhibited after the fabrication process can be statistically characterized before deploying on-field. Process variation such as doping fluctuation, line edge roughness and gate-oxide thickness is typically reported to be 10% to 30% across wafers and 5% to 20% across dies [5].

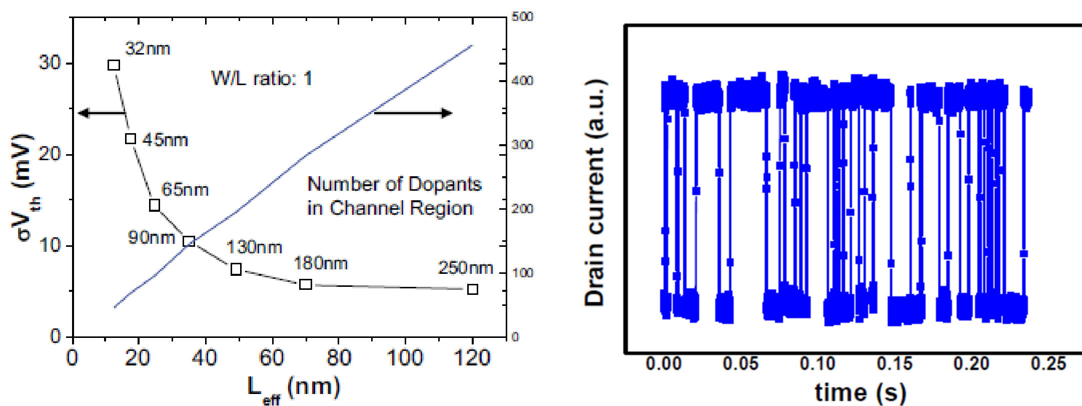


Figure 1.2. (a) Variation in V_{th} due to RDF [4] (b) Impact on drain current due to RTN.

Apart from the initial effects, once chips are put into use device parameters start to degrade gradually over time. As an aftermath of individual device degradation, circuit functionality degrades over time affecting performance metrics which is called **circuit aging**. Such effects are Negative Bias Temperature Instability (NBTI), Channel Hot Carrier (CHC), Time Dependent Dielectric Breakdown (TDDB) etc. are briefly described in Figure 1.3. These mechanisms have known to affect the transistors since the 1970s but have become more pronounced in the nano-scale regime due to processing and scaling changes introduced to improve device and circuit performance [6-14]. Introduction of new technology such as High-K Metal Gate (HK-MG) brings forth issues of Positive Bias Temperature Instability (PBTI) below 28nm.

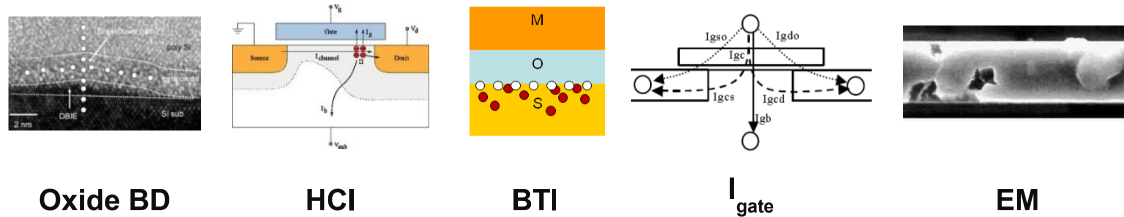


Figure 1.3. Aging effects gradually affecting device over lifetime

1.2 Device and Circuit Lifetime Criteria

As the reliability concerns become more severe with continuous scaling, it is critical to understand, simulate and mitigate their impact during the circuit design stage. Among different aging effects, NBTI and CHC are primary reliability mechanisms which limits the circuit life time. Figure 1.4 shows the plot of critical voltage as a function of the gate oxide thickness [15]. Digital circuits, which have lower oxide thickness and channel length, are primarily limited by both NBTI and PBTI, while AMS circuits with higher channel lengths and oxide thickness are affected by CHC.

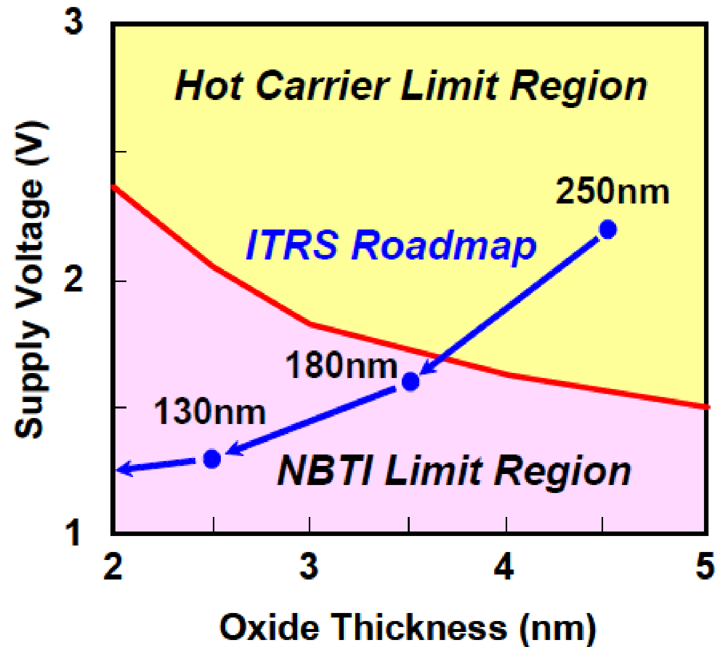


Figure 1.4. BTI becomes the dominant aging mechanism for digital designs as technology scales while CHC is still a threat for AMS designs [15].

Aggressive gate oxide scaling and less aggressive operating supply voltage scaling have exacerbated impact of reliability issues of BTI and CHC degradation. Thin oxide thickness and relatively high supply voltage results in increase of vertical and

electric field, which leads to more severe degradation. Further, to maintain the drain current, High-K materials are used for gate oxide which improves oxide capacitance without decreasing oxide thickness, but introduces more defects elevating reliability issues of PBTI in NMOS for sub 28nm technology nodes. V_{th} of a device can shift up to 50mV in magnitude over years, translating to more than 20% degradation in circuit speed or other performance metrics.

Aging concerns such as oxide breakdown and electro-migration (EM) are evaluated by an empirical threshold of performance shift, as shown in Figure 1.5 [16]. Since these effects usually induce sudden failures, the exact value of threshold only has a marginal impact on the lifetime (Figure 1.5, left). But for BTI and CHC, their effect is gradual (Figure 1.5, right). If a fixed threshold is still used to define the lifetime, a large amount of variations will be seen, depending on the process, workload, and the threshold value. Thus BTI and CHC present a unique challenge for circuit lifetime estimation.

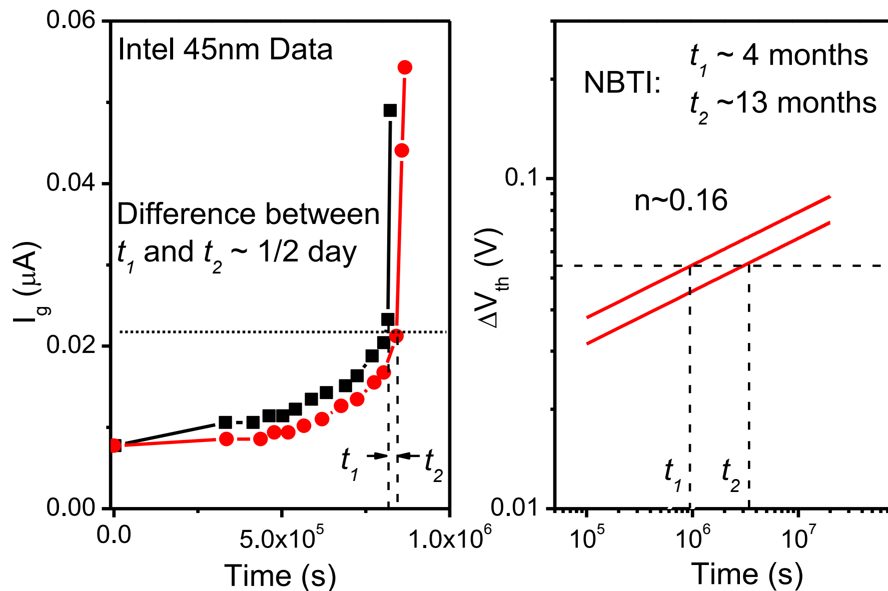


Figure 1.5. Traditional definition of reliability is appropriate for sudden failures (e.g., TDDB), but not applicable to gradual shift (BTI and CHC) [16].

1.3 Impact of Device Degradation at Circuit Performance

At the device level, the primary and major impact of BTI and CHC is the increase in absolute value of threshold voltage as shown in Figure 1.6. Mobility is also affected due to the larger Coulomb scattering and sub-threshold slope increases due to aging.

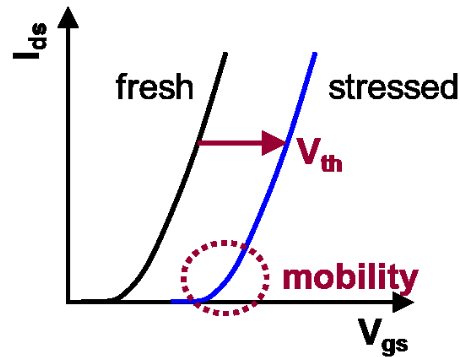


Figure 1.6. Impact on threshold voltage and mobility with aging due to aging.

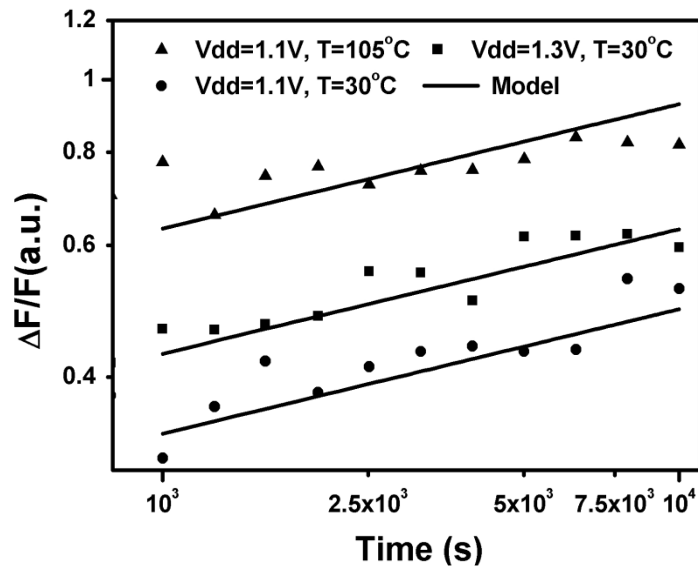


Figure 1.7. Shift in the frequency of 11 stage ring oscillator due to NBTI under various stress voltages and temperatures.

At the circuit level, aging affects both analog and digital circuits [17-23]. In digital designs, aging primarily affects operating frequency (speed), power, noise margin, data stability etc. Shift in frequency of 11 stage ring oscillator due to NBTI is shown in Figure 1.7 for different operating voltages and temperatures. Similarly, device degradation causes shift in retention voltage of SRAM cell array as described in Figure 1.8(a). Typical parameters affected due to aging are gain, unity-gain frequency, offset, matching, linearity (INL and DNL), etc. Figure 1.8(b) demonstrates the shift in Integral Non-Linearity (INL) for a 6-bit DAC caused by CHC aging of NMOS devices [23]. Design for reliability thus becomes a central and inherent goal of IC design particularly at scaled technology nodes. Identifying, simulating and mitigating impact of aging on circuit performance is critical for a successful IC product in a competitive market.

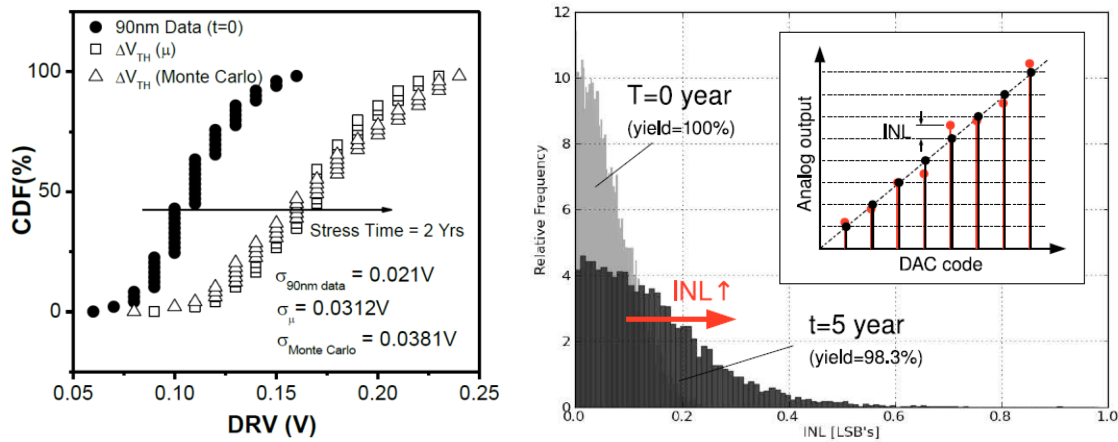


Figure 1.8. (a) Distribution of DRV illustrating the impact of aging on SRAM cell array (b) 6-bit DAC performance shift over 5 years of operation [23].

1.4 Previous Research on Modelling and Simulating Aging Effect

To date, research work on modelling of aging mechanisms has mainly focused on device and reliability physics [6-14]. Typically, a large set of aging data is collected from discrete devices which are used to calibrate an empirical or a physical model. This model is then used to determine approximate guard-band based on the worst case conditions. Circuit parameters are then fixed based on these pessimistic guidelines to ensure functionality over lifetime. Traditional worst case estimation does not consider certain aging properties, which causes an excessive amount of over-margining.

Some design techniques have been proposed to minimize NBTI effect, such as gate or transistor level sizing [7], input vector control [24-25], technology mapping and logic synthesis [26]. The implementation of these techniques relies on the worst case estimation of the circuit performance degradation during the design stage. In a contemporary SoC, a wide variety of circuit operation patterns co-exists. The diversity of circuit operation presents a unique challenge to predict lifetime under the aging effect: A device operating under constant stress voltage needs a static aging model; different from static stress, devices under AMS operation may experience totally random stress during their lifetime. Digital circuits, employ Dynamic Voltage Scaling (DVS) extensively to balance the workload and power consumption. Under such an operation, a static model is insufficient to accurately determine circuit aging. Further, statistical nature of aging aggravates worst case aging condition. Over-margining using worst case condition severely hinders designers to exploits full potential of advanced technology nodes. Therefore, a model which can analyze aging under any random input stress pattern is necessary. Different from AMS circuits or random DVS conditions, large-scale logic

designs encounter periodic inputs with different duty cycles and frequency. Although a random stress model can handle such situations, a long-term aging simulation is not efficient and requires expensive simulation time. To improve the efficiency, a long-term aging model is preferred which predicts an upper bound of threshold voltage shift for a periodic input. In summary, a set of new aging models are needed to improve circuit reliability prediction in both VLSI and AMS design under any dynamic operations.

Previous research work is more focused on understanding underlying physics and modelling aging effect isolated within the device communities compared to the development of efficient and accurate CAD tool. This is partially due to its complexity and emerging status, lack of design knowledge and CAD tools for managing the device degradation. The lack of design knowledge and CAD tools further creates the barrier for managing impact of device degradation on circuit performance. Such knowledge needs to be propagated into circuit design and CAD tools to assess the impact of device degradation on various circuit performance metrics. Proprietary efforts exist in leading industrial companies to develop their own reliability models and tools. These tools, however, are usually proprietary and customized to a specific technology, not available for general usage.

Commercially available aging tools [27-30] suffer from issues of inaccuracy in aging prediction mainly due to their extrapolation method. One example is conventional lifetime prediction tools based on Berkeley reliability simulation framework [27]. Figure 1.9 presents a typical flow of such tools. In this flow, several reliability parameters are needed at the device level. These device parameters are extracted from the silicon data collected by stressing devices at high temperature and voltage to accelerate the aging

process. In addition to device parameters, reliability simulators require design schematic or netlist files, as well as their input stimulus. Simulation of the input files reveals their operating voltages and thereby dynamic stress conditions. Based on the simulations performed at these stress conditions and using extracted parameters from short-term measurements, the aging rate and the lifetime are predicted using the extrapolation method (Figure 1.9).

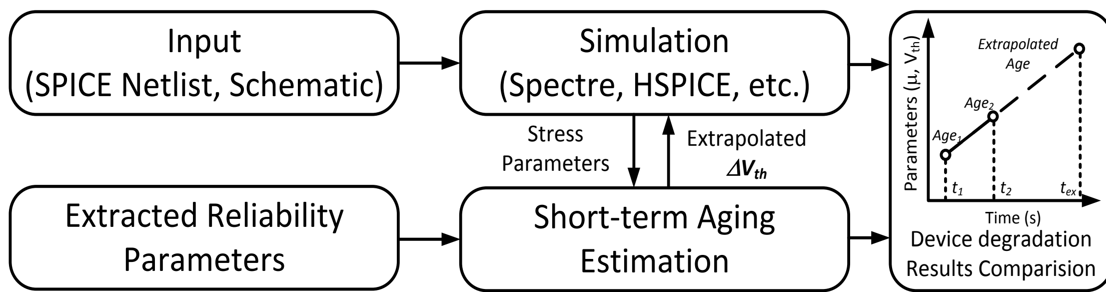


Figure 1.9. The simulation flow employed by conventional reliability tools. The extrapolation method is used for long-term lifetime prediction.

The tracking of stressed parameters through SPICE simulations makes these tools computationally expensive, as it consumes a large portion of the memory. While these tools can calculate the degradation of circuits with a limited number of transistors, performance evaluation of large-scale designs with millions of gates is impractical. To overcome these problems, a generic simulation tool that efficiently predicts the degradation would be extremely useful. A good circuit-aging simulator requires capabilities such as high capacity, high speed and high accuracy. The simulation of aging in large logic designs is difficult, since circuit degradation rate depends on both process and operation conditions such as V_{dd}, temperature (T), and input signal duty cycle (α)

[31]. These parameters are not spatially or temporally uniform, but vary significantly from gate to gate and from time to time due to the uncertainty in circuit topologies and operations. A simple static analysis may provide an extremely pessimistic estimate and consequently, result in over-margining. To estimate the degradation bound under various α's, a rudimentary approach resorts to exhaustive simulations. Yet such a method is inhibitive in computation cost, especially for circuits with a large number of inputs.

Lifetime prediction in AMS design is even more challenging than in digital logic circuits [32]. While aging induced V_{th} shift does not change the operating conditions in logic gates, parameters in AMS designs, such as the bias condition, offset and gain, are more vulnerable to V_{th} shift. The extrapolation method based on pre-stressed model parameters does not account for the changing operating conditions during aging which may lead to overly optimistic results. Furthermore, small AC signals affect the device degradation which is not accounted in current aging models. Hence, commercial tools inaccurately estimate the aging in AMS designs.

In summary, it is necessary to develop new models and simulation methodology in order to improve circuit reliability prediction in both VLSI and AMS design under dynamic operations.

1.5 Contribution of this work

BTI and CHC aging effect are dominant aging mechanisms that affect circuit operation over lifetime. BTI in both PMOS and NMOS devices exhibits stress and recovery behavior which presents a unique challenge.

A device operating under constant stress voltage needs a static aging model. Different from static stress, devices under AMS operation experiences totally random stress during lifetime. Current digital circuits employ DVS extensively to balance workload and power consumption. Under such an operation, a static model is not sufficient to accurately determine lifetime of a circuit. A model which can identify aging under any random input stress pattern is needed. Unlike AMS circuits, large scale logic design encounters periodic input for different duty cycles and frequency. Although a random stress model can handle such circuit situations, aging simulation is not efficient and requires higher simulation time. To increase efficiency, a long-term BTI model is required which can predict upper bound of threshold voltage shift for a periodic input. The proposed model facilitates designers to avoid time consuming atomistic simulations to predict aging.

In this work, we propose compact aging models based on the widely accepted Reaction-Diffusion theory (RD) and summarize similar set of aging models based on Trapping/Detrapping (TD) mechanism. As an important contribution of this work, a complete set of R-D based models are proposed for static, random input and long-term condition which covers all aspect of circuit operation. We also exploit TD based models to explain statistical nature of aging, predicting the aging variability over time. Finally we demonstrate that combination of both physical mechanisms: Reaction-diffusion and

Trapping/Detrapping can greatly enhance prediction accuracy of the aging model at both device and circuit level.

CHC is essential for AMS reliability as devices used for designs are typically long-channel and operate continuously in saturation region. Previous technology nodes rely on lucky electron model to predict channel hot carrier degradation. Based on this model, as the device is driven more into saturation, it experiences higher CHC stress. Advanced technology nodes have shifted worst case condition for channel hot carrier which was explained by lucky-electron model. This work presents modified CHC model which incorporates the modified degradation rate.

Besides having accurate device level degradation models for digital and AMS circuits, it is essential to have an efficient simulation methodology to predict aging effect of various circuit parameters and estimate lifetime at the design stage. Extrapolation of lifetime based on initial circuit parameters leads to optimistic results, as degradation in threshold voltage changes the operation condition and in effect the degradation itself. These limitations are catastrophic in case of AMS designs. A new aging analysis tool is proposed for AMS designs which eliminate extrapolation of lifetime giving accurate aging estimate. In large scale logic circuits, the timing paths which meet timing requirements in the fresh circuit may turn critical over time due to aging, leading to a timing violation. In this work, System level Reliability Analyzer (SyRA) tool developed earlier is modified to incorporate complex logic gates. The tool is used to estimate the guard banding overhead when DVS condition is applied to critical logic paths.

This thesis presents a complete cross-layer solution of reliability analysis from device level to system level aging, as shown in Figure. 1.10. Physical mechanisms

contributing for the aging are investigated at the device level. Device level compact aging models that predict the V_{th} shift of the transistor under any operating conditions are proposed. The entire approach transfers the microscopic understanding of underlying physics of reaction-diffusion and trapping/de-trapping into system level reliability.

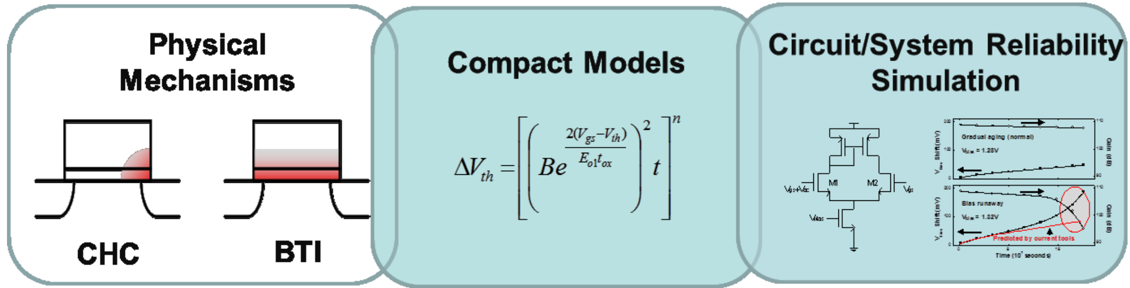


Figure 1.10. A complete cross-layer solution for proposed reliability analysis.

Accurate models and efficient simulation tools allow further insight in evaluating aging impact on circuit performance. Proposed methodology helps us identify critical feedback conditions in both AMS and digital design. In AMS design, the feedback between CHC degradation and gate-drain connected NMOS can accelerate aging of a device. This effect is termed as Bias Runaway. In order to enable proper guard-banding, we propose a boundary condition to identify the critical operating voltage for the biasing circuits to mitigate bias runaway. Similar feedback is seen in clock tree paths for logic circuits. Clock gating used to optimize power performance induces static stress causing shift in duty cycle. Further, depending on the ratio of static and dynamic stress, the duty cycle will to converge to 50% value. These critical feedbacks identified in CMOS designs based on proposed aging models and simulation methodologies underline the importance of this work for resilient and robust circuit design.

1.6 Thesis Organization

The organization of the thesis report is as follows: Chapter 2 presents the background of NBTI effect and presents new RD models for any type of stress condition. This complete suite of compact models is well validated with 45nm device level data. Chapter 3 presents Trapping/De-trapping physics along with summary of compact aging models. Model validation is shown at 65nm technology node. Further, RD and TD are empirically combined to improve aging prediction at both 45nm and 65nm. Chapter 4 proposes a new modified CHC model to account for e-e scattering at advanced technology nodes. This effect and model is validated with 65nm thick oxide device data. Further a simple de-coupling of PBTI and CHC is shown in this chapter along with validation of BTI and CHC at 28nm HK-MG node. Using the new model for BTI and CHC, circuit level validation is performed using 45nm ring oscillator and 90nm single ended LNS structures in Chapter 5. Chapter 6 proposes a new simulation framework for AMS lifetime estimation by eliminating extrapolation of V_{th} shift which improves the lifetime prediction accuracy. A positive feedback mechanism called bias runaway which is potentially dangerous for biasing circuits is characterized leveraging proposed CHC model and simulation framework. A boundary condition is derived which helps designers to protect the basing circuit from this phenomenon. Further in digital circuit, duty cycle shift under DC and AC stress condition is also demonstrated. Chapter 7 summarizes this report as well as presents future work that needs to be carried out.

CHAPTER 2

REACTION DIFFUSION BASED AGING MODELS

2.1 Underlying Reliability Physics: Two Mechanisms

The primary impact of BTI at the device level is the gradual increase in transistor V_{th}, whereas the degradation of other device parameters are less pronounced. Since the threshold voltage directly affects the delay of a digital gate, operating frequency of a logic path decreases temporally. Similarly, in AMS circuits, shift in V_{th} degrades the gain, trans-conductance and other performance metrics. To estimate circuit aging rate, the fundamental step is to model device V_{th} shift under given stress voltage and temperature. In this section, RD and TD based theories are explained as later it is shown that combining both mechanisms can help improve prediction accuracy.

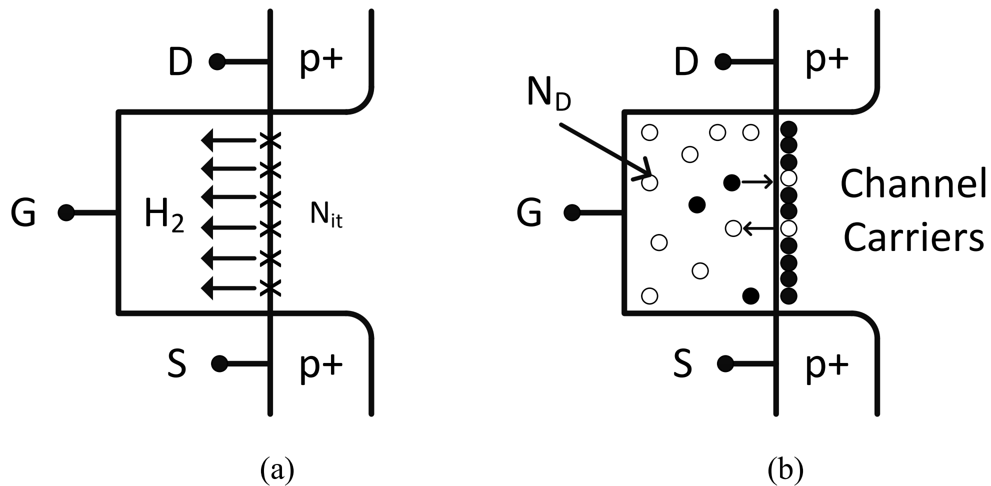


Figure 2.1. Two aging mechanisms for BTI: (a) Reaction Diffusion (RD), and (b) Trapping/Detrapping (TD).

Two prevalent theories: Reaction-Diffusion and Trapping/Detrapping explains the V_{th} shift in PMOS device. Figure 2.1 shows the cross section of a device which explains the difference between both mechanisms. RD is a two-step process namely: Reaction and Diffusion as shown in figure 2.1 (a). According to RD theory [6-10][13-14][33-45], the stress voltage causes covalent bonds (Si-H) at interface to break, which is *Reaction*. In the *Diffusion* step the broken hydrogen atoms combines to form H_2, which diffuses towards gate. For current thin oxide devices, diffusion in poly-gate dominates the V_{th} shift incremental behavior. The interface states left at Si-SiO_2 due to diffusion of H_2 increases the threshold voltage. This leads to a power law relation (t^n) with time exponent (n) ~ 1/6, which should be independent of process parameters. Magnitude response of ΔV_{th} exponentially depends on voltage and temperature.

According to the TD theory [46-59] shown in Figure 2.1 (b), there exist number of defect states with different energy levels and capture and emission time constants. Threshold voltage of a device increases when a trap captures a charge carrier from conducting channel of a MOS device. Reduced number of channel carrier causes drain current to decrease over time. The probability of trapping depends on capture time constants and that of detrapping depends on emission time constants. The gradual change in the number of traps occupied results in a logarithmic time evolution of V_{th} shift, different from power law behavior of RD. Voltage and temperature holds exponential relation which is same to RD theory.

2.2 Reaction-Diffusion Based Static Model

Till date, the RD model is the only model that successfully explains the power-law dependence of shift in the threshold voltage due to NBTI. This model assumes that when a gate voltage is applied, it initiates a field dependent reaction at the semiconductor-oxide interface that generates interface traps by breaking the passivized Si-H bonds. Figure 2.1(a) shows the cross-section of a transistor to illustrate RD model. There are two critical phases described in RD model

There are two critical steps based on Reaction – Diffusion theory. *Reaction*: Si-H or Si-O bonds at the substrate/gate oxide interface are broken under the electrical stress for a given oxide thickness [6-7][10]. The interface charges are induced in gate oxide and further in poly-gate, which cause the increase of V_{th}. Given the initial concentration of the Si-H bonds (N_0) at the interface and the concentration of inversion carriers (P), the generation rate of the interface traps is given by [6][7]:

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT})P - k_R N_H N_{IT} \tag{2.1}$$

where, k_f and k_r are forward and reverse reaction rates. The generation rate is exponentially dependent on stress voltage and temperature. During the initial phase of stress period, the trap generation is slow with respect to time. Thus dN_{IT}/dt ~0 and $N_{IT} << N_0$, reducing Equation (2.1) to:

$$N_H N_{IT} = \frac{k_f}{k_r} N_0 P \tag{2.2}$$

With the continuation of forward reaction, H is produced and two H atoms combine to form H_2 molecule. The concentration of H_2 (N_{H2}) is related to the concentration of H (N_H) using

$$N_{H_2} = k_H N_H{}^2 \tag{2.3}$$

where k_h is the rate constant.

Diffusion: Generated hydrogen species diffuse away from Si-SiO$_2$ interface towards gate. This diffusion is driven by the gradient of the density uniformly across the entire channel of a device. This process is governed by following equation [6][7]:

$$\frac{dN_H}{dt} = C\frac{d^2N_H}{dx^2} \tag{2.4}$$

C is the diffusion constant for hydrogen molecule in poly-Si which depends on activation energy. Driven by the gradient of the generated H_2 density, the H_2 current diffuses into the oxide and is governed by Equation (2.4). After a time t, the diffusion front is at a distance of $\sqrt{Ct}$ from the Si-SiO$_2$ interface. The total number of interface charges produced after time (t) is twice the number of H_2 molecules generated during that time since there are two hydrogen atoms in the hydrogen molecule.

To solve differential Equation (2.1) and (2.4) to derive a compact model, an approximate profile of H_2 concentration in gate oxide and poly-Si is assumed as shown in Figure 2.2. N_{H2} is the concentration of hydrogen molecules at distance 'x' from Si-SiO$_2$ interface at time (t), where x is given by $\sqrt{Ct}$. Diffusion of H_2 molecules in oxide is much

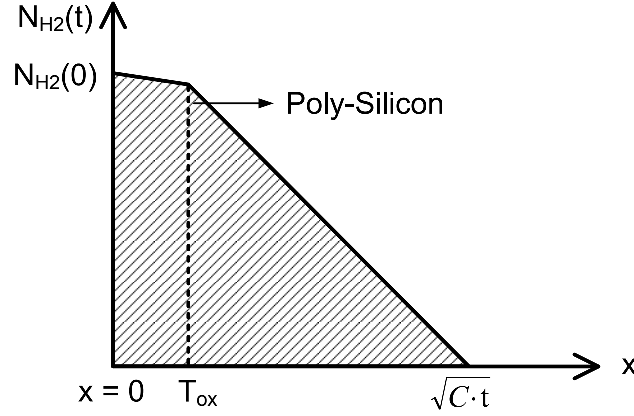


Figure 2.2. Approximate diffusion profile of hydrogen atoms under constant stress.

faster than poly-Si. The total number of interface traps generated for a given stress time is given as:

$$N_{IT} = 2\int_{0}^{x(t)} N_{H_2}(x)dx \tag{2.5}$$

H_2 diffusion is divided in silicon oxide and poly-gate. Fast diffusion of H_2 in oxide and small thickness of dielectric leads to a very small difference between H_2 concentration at Si-SiO_2 interface and SiO_2-Poly interface. A fitting parameter δ is introduced to account for fraction drop of H_2 concentration, using which Equation (2.5) can be written as

$$\begin{aligned} N_{IT} &= 2\int_{0}^{t_{ox}} N_{H_2}(x)dx + \int_{t_{ox}}^{\sqrt{Ct}+t_{ox}} N_{H_2}(x)dx \\ &\approx 2\left(\frac{1}{2}(1+\delta)\cdot N_{H_2}(0)\cdot t_{ox} + \frac{1}{2}N_{H_2}(0)\cdot\sqrt{Ct}\right) \end{aligned} \tag{2.6}$$

$N_{H2}(0)$ is H_2 concentration at Si-SiO_2 interface while $\delta N_{H2}(0)$ is density at Si-Poly interface. Finally using $N_{H2} = k_h N_H^2$, N_{IT} can be represented as

$$N_{IT} = \left(\frac{\sqrt{k_h} k_f N_0 P}{k_r} \right)^{\frac{2}{3}} \left((1+\delta) t_{ox} + \sqrt{Ct} \right)^{\frac{1}{3}} \tag{2.7}$$

Where, inversion hole density $P = C_{ox} (V_{gs}\text{-}V_{th})$. Based in the interface charges, threshold voltage shift can be derived as: $\Delta V_{th} = qN_{IT} / C_{ox}$. This RD based model predicts the V_{th} shift under any given constant stress voltage, temperature and time. The final form of RD based compact model is given as:

$$\begin{aligned} \Delta V_{th} &= \frac{qN_{IT}}{C_{ox}} = A \cdot \left((1+\delta) t_{ox} + \sqrt{Ct} \right)^{2n} \\ A &= \left(\frac{qt_{ox}}{\varepsilon_{ox}} \right) \sqrt[1/2n]{K_2 C_{ox} (V_{gs} - V_{th}) \exp\left(\frac{2E_{ox}}{E_0} \right)} \end{aligned} \tag{2.8}$$

C is the diffusion constant which incorporates the temperature dependence. Time exponent n is 1/6 when the diffusion species is H_2. Figure 2.3 shows model validation.

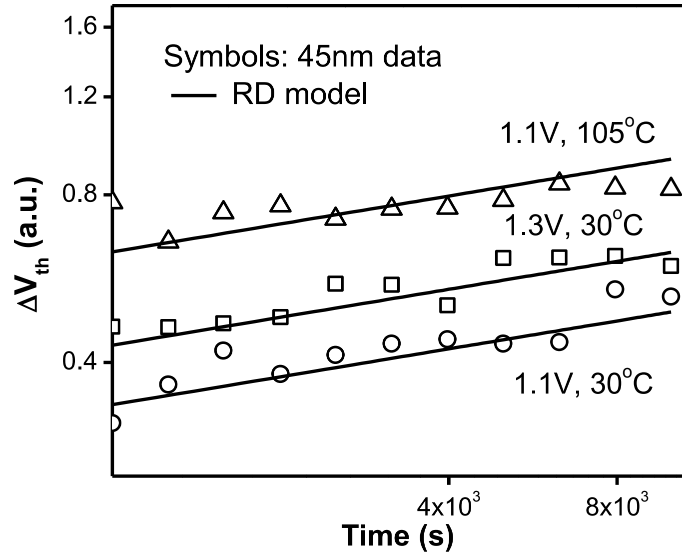


Figure 2.3. RD based compact static model matches 45nm silicon data under constant stress for different voltage and temperature.

2.3 Reaction-Diffusion Based Random Input Stress Models

Today's circuits typically have a reduced activity factor (or duty cycle) and dynamic voltage scaling (DVS), to reduce power consumption [20][33][36]. Therefore, a significant portion of the operation is under lower supply voltage, resulting in large recovery. Since the degradation is highly sensitive to the stress voltage, DVS leads to different amounts of circuit aging. For a random stress pattern, it is necessary to derive voltage dependent recovery to accurately predict V_{th} shift. Previous aging models do not account for voltage dependent recovery which is critical for ΔV_{th} shift under DVS.

The hydrogen atoms that are generated during stress phase recovers if the stress voltage is removed completely. Atoms close to Si-SiO_2 interface anneals the broken Si-H bond while atoms deep in Poly-gate continues to diffuse away leading to recovery of V_{th}. Approximate profile of hydrogen species is shown in Figure 2.4. Hydrogen atom diffuses quickly in oxide which anneals some of Si-H bonds very quickly. If stress voltage applied

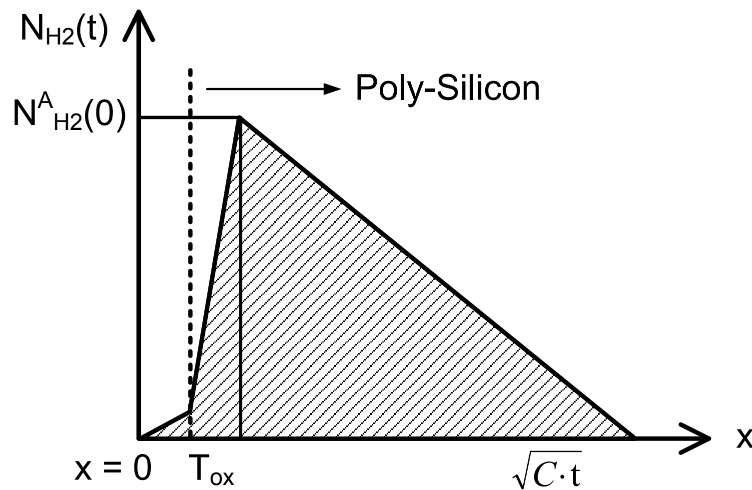


Figure 2.4. Approximate diffusion profile of hydrogen atoms under recovery.

is removed after time (t_1), the interface charges generated for the given time are $N_{IT}(t_1)$. The total number of charges to be annealed is given by $N^A{}_{IT}(t)$. Interface charges at a given time t is given by

$$N_{IT}(t) = N_{IT}(t_1) - N_{IT}^A(t) \tag{2.9}$$

From Figure 2.4, the number of annealed traps can be divided in to two parts: (1) recombination of H_2 in oxide and (2) back diffusion of H_2 in poly-gate [6]. Thus we have,

$$N_{IT}^A(t) = 2\left(\xi_1 t_e + \frac{1}{2}\sqrt{\xi_2 C(t - t_1)}\right) N_{H_2}(0) \tag{2.10}$$

ξ_1 and ξ_2 are the back diffusion constants. From Equations (2.7) and (2.10), we get

$$N_{IT}^A(t) = N_{IT}(t)\left(\frac{2\xi_1 t_e + \sqrt{\xi_2 C(t - t_1)}}{(1+\delta)t_{ox} + \sqrt{Ct}}\right) \tag{2.11}$$

Substituting Equation (2.11) in (2.9) and simplifying the equations and using $\Delta V_{th}=qN_{IT}/C_{ox}$, we get recovery model as:

$$\Delta V_{th}(t) = \Delta V_{th}(t_1)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t - t_1)}}{(1+\delta)t_{ox} + \sqrt{Ct}}\right) \tag{2.12}$$

Above equation represents V_{th} recovery when stress voltage is completely removed. This model cannot predict V_{th} behavior when stress voltage is lowered or increased. Under DVS operation, the stress voltage is changed to a lower V_{DD} from higher V_{DD}. Diffusion profile of hydrogen atoms in a device when voltage changes from high to low is different in relation to the voltage change from low to high. Time-dependent diffusion profiles are shown in Figure 2.5 for a voltage change from high (V_1)

to low (V_2) at time (t_0). The resulting V_{th} shift is divided in to two components. The first component is the diffusion due to the lower voltage (V_2) which is the un-shaded region in the figure. The shaded part is the recovery component that gradually decreases with time.

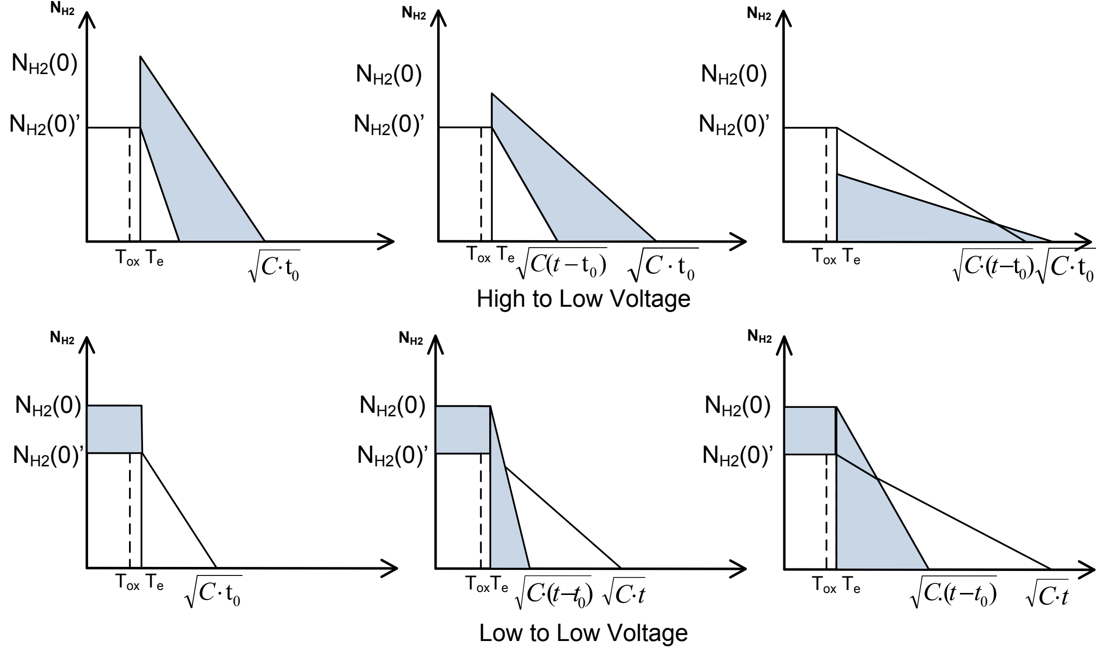


Figure 2.5. Approximate diffusion profile of hydrogen atoms in PMOS under dynamic stress: (a) Voltage change from high to low (b) low to high.

Eventually, the ΔV_{th} curve is driven by the lower voltage. To derive a closed form solution, we start with the ΔV_{th} under lower voltage:

$$\Delta V_{th}(t) = A_2\left((1+\delta)t_{ox} + \sqrt{C(t-t_0)} + s(t)\right)^{2n} \tag{2.13}$$

where A_2 is the function of lower voltage (V_2). $s(t)$ is time dependent initial distance of hydrogen diffused shown as shaded area in first graph of Figure 2.5(a). As time progresses, these hydrogen atoms recovers given by following equation:

$$\Delta V_{thr}(t) = \Delta V_{th}(T)\left(1 - \frac{2\xi_1 T_e + \sqrt{\xi_2 C(t-t_0)}}{(1+\delta)t_{ox} + \sqrt{Ct}}\right) \qquad (2.14)$$

By substituting $t=t_0$ in Equation (2.13) and equating the results with Equation (2.14), we get a compact model which predicts V_{th} shift when stress voltage changes from a high to low voltage during a DVS operation.

$$\Delta V_{th}(t) = \left(\sqrt[2n]{A_2}\sqrt{C(t-t_0)} + \sqrt[2n]{\Delta V_{th}(t_0)\left(1 - \frac{2\xi_1 T_e + \sqrt{\xi_2 C(t-t_0)}}{(1+\delta)t_{ox} + \sqrt{Ct}}\right)}\right)^{2n} \qquad (2.15)$$

ξ_1 and ξ_2 are back diffusion constants, same as recovery model. This equation is capable of predicting the non-monotonic behavior of initial recovery and eventually converging with rising V_{th} shift due to lower voltage.

For voltage change from low (V_2) to high (V_1) voltage at time (t_0), the diffusion profile approximation is shown in Figure 2.5(b). In this case, there is no recovery component. The diffusion due to low voltage continues to diffuse at the same rate. However, the diffusion front due to higher voltage is dominant, and V_{th} shift eventually converges. We start from Equation (2.13) for the derivation. In this case, A_2 is the function of higher voltage (V_1). The diffusion profile of hydrogen under V_1 follows the shaded region in Figure 7b. V_{th} shift under lower voltage (V_2) at time (t_0) is given by:

$$\Delta V_{th}(t_0) = A_1\left((1+\delta)t_{ox} + \sqrt{Ct_0}\right)^{2n} \qquad (2.16)$$

Substituting $t=t_0$ in Equation (2.13) and equating with above equation we arrive at the model which describe the behavior when voltage transits from low to a high value:

$$\Delta V_{th}(t) = \left[\sqrt[2n]{A_2}\left((1+\delta)t_{ox} + \sqrt{C(t-t_0)}\right) + \sqrt[2n]{A_1}\left((1+\delta)t_{ox} + \sqrt{Ct}\right)\right]^{2n} \qquad (2.17)$$

Table 1 summarizes the new proposed random input stress models [60]. Figure 2.6 and 2.7 validates the model prediction with 45nm silicon data under a random stress pattern. The efficacies of stress and recovery of threshold voltage are accurately captured when device is stressed under arbitrary voltage. In Figure 2.6, the device is initially stressed and then recovered which is accurately captured by the new random input

Table 1: Summary of RD based compact aging models

Constant stress	$\Delta V_{th}(t) = A \cdot t^n$
Random Input Stress	*Low to high voltage transition*: $\Delta V_{th}(t) = \left[\sqrt[2n]{A_2}\left((1+\delta)t_{ox} + \sqrt{C(t-t_0)}\right) + \sqrt[2n]{A_1}\left((1+\delta)t_{ox} + \sqrt{Ct}\right)\right]^{2n}$ *High to low voltage transition*: $\Delta V_{th}(t+t_0) = \left(\sqrt[2n]{A_2}\sqrt{C(t)} + \sqrt[2n]{\Delta V_{th}(t_0)\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t)}}{(1+\delta)t_{ox} + \sqrt{C(t+t_0)}}\right)}\right)^{2n}$

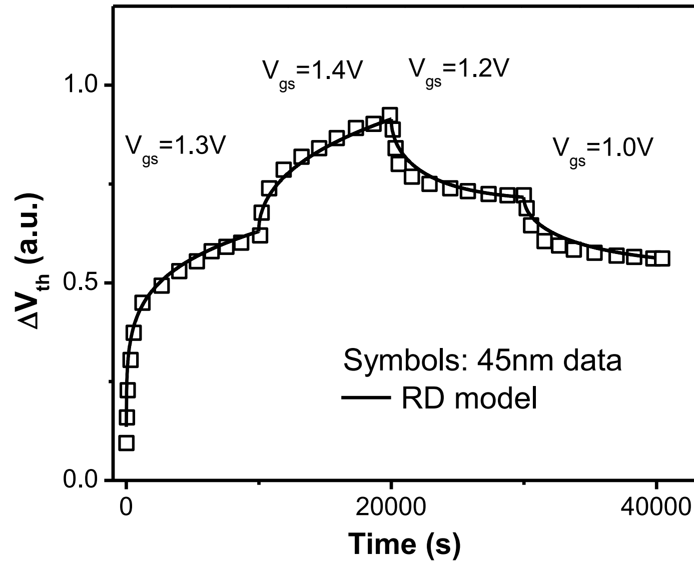


Figure 2.6. Random stress pattern of a device validating the model prediction at different voltages and stress input.

models. In Figure 2.7, a device is stressed under 1.3V for initial 1000 seconds and then stress voltage is lowered to 1.2V. As a result of higher stress, the device initially recovers. However, the continuous stressing at 1.2V eventually leads to V_{th} increase. This non-monotonic behavior is well predicted by new RD based models.

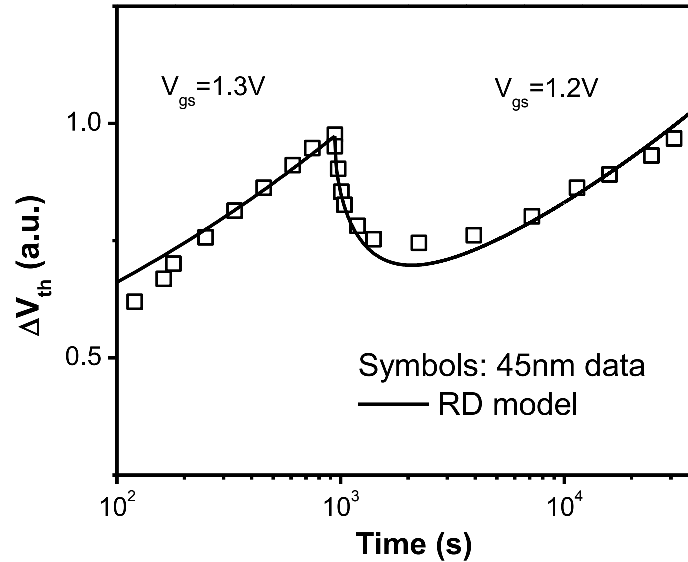


Figure 2.7. RD based V_{th} shift model validation. V_{th} initially recovers under voltage change and eventually converges to the t^n curve due to lower voltage.

2.4 Reaction-Diffusion Based Long-term Model

Under the extensive usage of DVS, accurate V_{th} shift can be predicted using the random input stress models derived in previous section. However for a large scale logic designs, applying such random stress models will not be efficient simulation method. Most digital circuits operates at a regular frequency periodically with a given duty cycle. A long-term model that directly estimates aging at the end of a given operation time, without tracking the stress-recovery over many cycles help in effective aging prediction. This long-term model predicts a tight upper bound under multi-cycle operations under DVS. Based on the multi-cycle model in the previous section, stress ($\Delta V_{ths,m}$) and recovery ($\Delta V_{ths,m+1}$) in Figure 2.8 can be connected to derive long-term model.

It is possible to obtain a closed form solution to predict the upper bound of ΔV_{th}

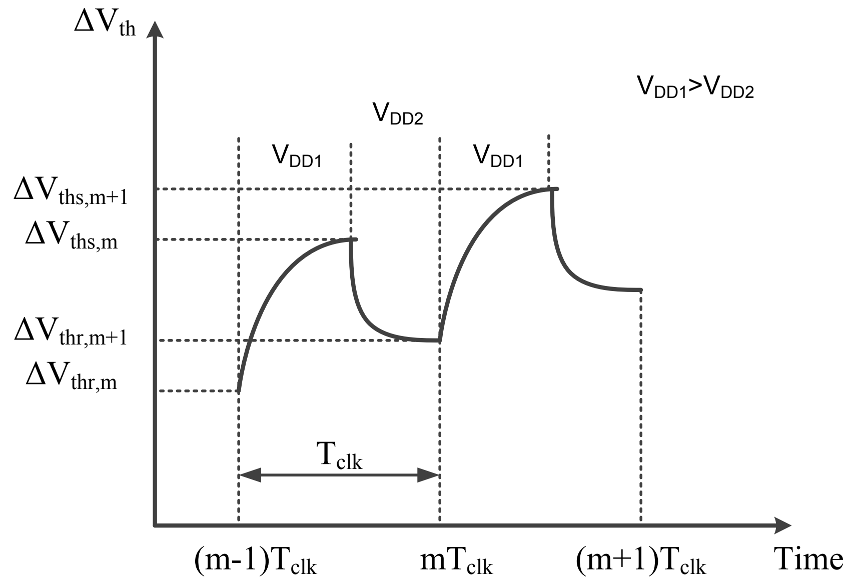


Figure 2.8. The V_{th} shift during the stress and recovery, in typical digital circuits under periodic stress input.

for different clock cycle (T_{clk}), duty cycle (α) and stress time for a circuit oscillating between two voltages. To derive a closed form solution, $\Delta V_{ths,m}$ and $\Delta V_{ths,m+1}$ are connected iteratively using random stress models as:

$$\Delta V_{ths,m+1} = \begin{bmatrix} \sqrt[2n]{A_2}\,X\left(1+\beta_m^{1/2n}+\beta_m^{1/2n}\beta_{m-1}^{1/2n}+\ldots\right)+ \\ \sqrt[2n]{A_1}\left(Y+\sqrt{C\alpha T_{clk}}\right)\left(1+\beta_m^{1/2n}+\beta_m^{1/2n}\beta_{m-1}^{1/2n}+\ldots\right) \end{bmatrix}^{2n} \quad (2.18)$$

where,

$$X=(1+\delta)t_{ox}+\sqrt{C\alpha T_{clk}}, \qquad Y=\sqrt{C(1-\alpha)T_{clk}}$$
$$\beta = 1-\frac{2\xi_1 t_e+\sqrt{\xi_2 C(1-\alpha)T_{clk}}}{(1+\delta)t_{ox}+\sqrt{CmT_{clk}}} \quad (2.19)$$

Using $\beta_1 < \beta_2 < \ldots.\ \beta_{m-1} < \beta_m$ and geometric series approximation, the upper bound of degradation is derived as:

$$\Delta V_{ths,m+1} = \left[\sqrt[2n]{A_2}\,X\left(\frac{1}{1-\beta^{1/2n}}\right)+\sqrt[2n]{A_1}\left(Y+\sqrt{C\alpha T_{clk}}\right)\left(\frac{1}{1-\beta^{1/2n}}\right)\right]^{2n} \quad (2.20)$$

The new long-term model is capable of predicting the upper bound of ΔV_{th} for cycle of two non-zero voltages. Figure 2.9 confirms that for multiple cycles, the new model under random input predicts the same result as the long-term model, if the pattern is stable with a constant duty cycle. Such model predicts tight upper-bound of the periodic stress for large scale digital circuit improving simulation efficiency.

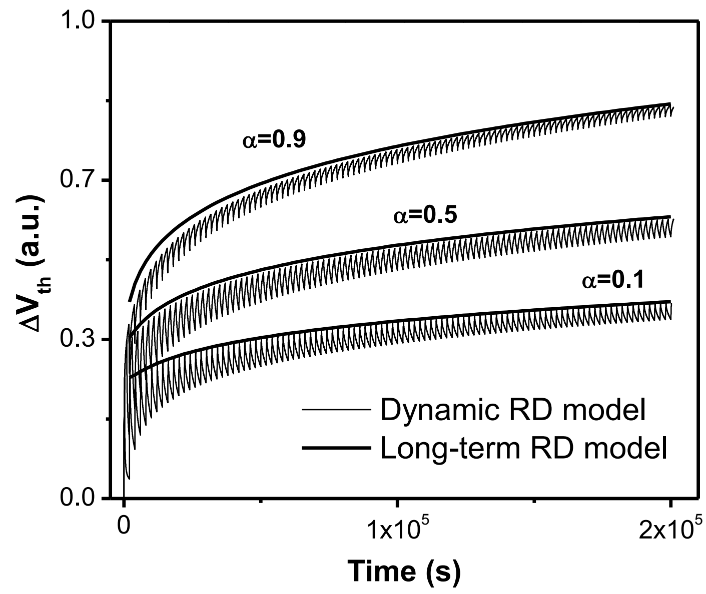


Figure 2.9. Under constant duty cycles, the model for random input is consistent with long-term model.

CHAPTER 3

TRAPPING/DETRAPPING BASED AGING MODELS

3.1 Need for Trapping/Detrapping Based Models

Several works show the role of charge trapping/de-trapping mechanism in NBTI degradation [46-59]. Clear steps showing single trapping or de-trapping events have been reported through discrete V_{th} shifts [61]. Figure 3.1 shows the measured V_{th} of a device under pure recovery with discrete V_{th} shifts due to trapping/de-trapping events. Fast trapping/de-trapping events confirm the necessity to include TD based physics for reliable aging prediction. Many research work shows that the final V_{th} shift is a result of fast TD events and a relatively slow RD process [62-65]. However, the dominance of either mechanism depends on the fabrication technology. This chapter summarizes previously derived compact aging models for all operating conditions based on TD theory. Adding new feature, RD models proposed in previous chapter are combined with TD models to improve accuracy of aging prediction especially under DVS operation.

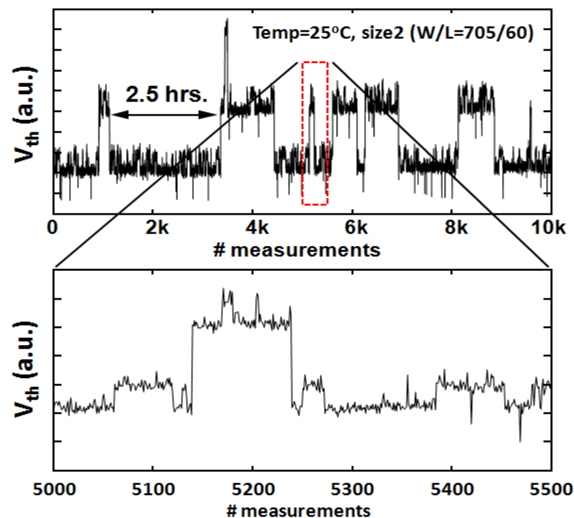


Figure 3.1. PMOS V_{th} measurement under pure recovery; discrete V_{th} shifts observed due to trapping and de-trapping events.

3.2 Trapping/Detrapping Based Static Aging Model

TD mechanism has come into light due to discrete V_{th} shift observed during the recovery phase in NBTI with the fast measurement techniques [66][67]. Figure 3.2 illustrates the physical picture of TD: when a negative bias voltage is applied to the gate of a PMOS device, the trap energy is modulated. If the trap gains sufficient energy, it may capture a charge carrier, thus reducing the number of available carriers in the channel [48]. The charged trap state modulates the local V_{th} and acts as a scattering source, reducing the effective mobility [48]. Faster traps (with shorter time constants) having a higher probability of capturing carriers; the occupation probability increases with voltage and temperature. Trapping and de-trapping events are stochastic in nature and hence a compact model is based on the statistics of trap properties.

The basic modeling assumptions based on TD theory are the same as the ones used in modeling of low-frequency noise, since the charge trapping dynamics (capture

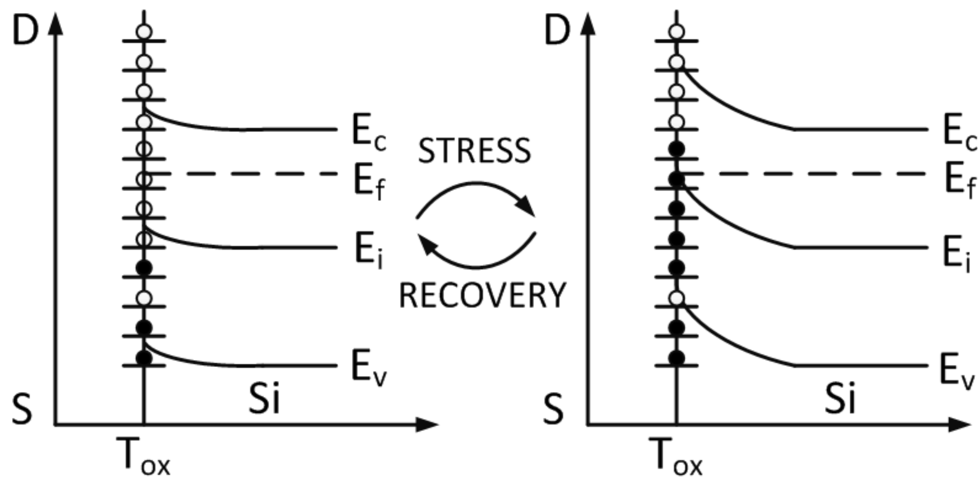


Figure 3.2. Illustration of statistical trapping/de-trapping process in gate oxide for a PMOS device, leading to threshold voltage shift

and emission time statistics) that contribute to the degradation of device performance over time is similar to that causing low-frequency noise [46][50-55]. The main assumptions of the trap properties are:

- The number of traps follows a Poisson distribution, which is common for a discrete process.
- Capture and emission time constants are uniformly distributed on the logarithmic scale. This microscopic assumption is critical to derive the logarithmic time evolution at the macro scale.
- The distribution of trap energy is approximated as a U-shape, which is verified by silicon measurement and key to the voltage and temperature dependence of the aging effect.

Based on the T-D theory, the V_{th} shift at a given stress time is the result of number of traps ($n(t)$) occupied by the channel carriers. The probability of a particular trap, initially empty (0), to be occupied (1) after an elapsed time t is given by $P_{01}(t)$. This occupation probability can be calculated by observing that

$$P_{01}(t+dt) = P_{01}(t)p_{11}(dt) + P_{00}(t)p_{01}(dt) \tag{3.1}$$

where $p_{01}(dt)$=1/τ_c and $p_{11}(dt)$=1- p_{10}(dt)=1/τ_e. Integrating it from t_0 to t [58]:

$$P_{01}(t+t_0) = \frac{\tau_{eq}}{\tau_c}\left(1 - e^{-t/\tau_{eq}}\right) + P_{01}(t_0)e^{-t/\tau_{eq}} \tag{3.2}$$

where $1/\tau_{eq}=1/\tau_c+1/\tau_e$. τ_c, τ_e are random in nature, representing capture and emission time constants respectively, and dependent on bias point and temperature. The values are determined by [48][58]:

$$\tau_c = 10^p(1+e^{-q}) \text{ and } \tau_e = 10^p(1+e^{+q}) \tag{3.3}$$

where $p \in [p_{min}, p_{max}]$. p_{min} and p_{max} define the time constants for fastest and slowest traps respectively (p_{min}~1 and p_{max}>10). Since p is assumed to be uniformly distributed, the characteristic time constants are uniformly distributed on logarithmic scale. The parameter q is given by $(E_T-E_F)/kT$, where E_T is the trap energy and E_F is the Fermi energy level. The trap energy is a function of applied electric field. Consequently, τ_c and τ_e are dependent on voltage and temperature.

The occupation probability of the trap at time t, assuming that it is under constant stress from time t_0=0 is obtained by substituting $P_{01}(0)$=1-$P_{01}(0)$=0 in Equation (3.2), integrating $P01$ and multiplying with the number of available traps, the average number of occupied traps obtained by substituting the logarithmic distribution of time constants, and the U shaped distribution of trap energies [48][58]:

$$n(t) = \frac{N}{\ln 10(p_{\max} - p_{\min})} \int_0^{E_{T\max}} \frac{g(E_T)dE_T}{1 + \exp\left(-\frac{E_T - E_F}{kT}\right)} \cdot \int_{10^{-p\min}t}^{10^{-p\max}t} \frac{e^{-u} - 1}{u} du \qquad (3.4)$$

where $g(E_T)$ is the trap energy distribution, The trap energy, E_T changes as a function of electric field (E_{ox}). Assuming p_{min}~1 and p_{max}>10, and E_T~1/E_{ox} [58],

$$n(t) = \frac{N}{\ln 10(p_{\max} - p_{\min})} \exp\left(\frac{\beta V_g}{T_{ox} kT}\right) \exp\left(\frac{-E_0}{kT}\right) \left[A + B \log 10^{-p\max} t\right] \qquad (3.5)$$

Equation (3.5) describes the aging under a constant stress voltage and temperature. Similar as RD model, it is an exponential function of the stress voltage, temperature and t_{ox}. Furthermore, it has a statistical nature with N, an index for the number of traps per device. For the simplicity, Equation (3.5) is written as:

$$\Delta V_{th}(t) = \phi\left[A + B \log(1 + Ct)\right] \qquad (3.6)$$

Figure 3.3 presents the validation of TD model under various constant stress voltages. From the figure, it is evident that the degradation has an exponential relation with stress voltage. Such an exponential dependence on voltage is similar to that predicted by the RD model. Figure 3.3 shows the linear dependence with time when the x-axis is plotted in log scale, implying the logarithmic dependence on stress time. The time dependence of degradation is the major difference between RD and TD based compact aging models.

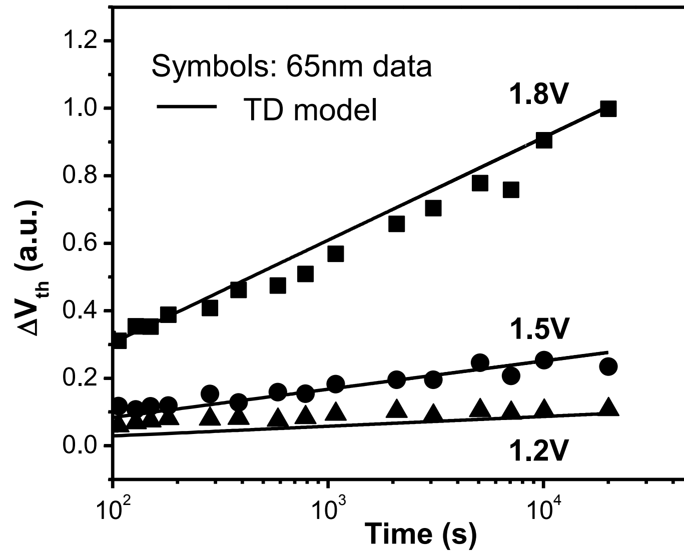


Figure 3.3. The TD based compact model matches the logarithmic time dependence and exponential voltage dependence.

3.3 Trapping/Detrapping Based Random Input Aging Model

In this section, trapping/de-trapping based models are presented which can handle random stress waveform. Since the degradation is highly sensitive to the voltage, dynamic voltage scaling leads to different amounts of circuit aging. To handle voltage transitions, using Equation (3.2) and a non-zero time, t_0, to calculate the occupation probability at time t (time elapsed after t_0), as shown in Figure 3.4 [58].

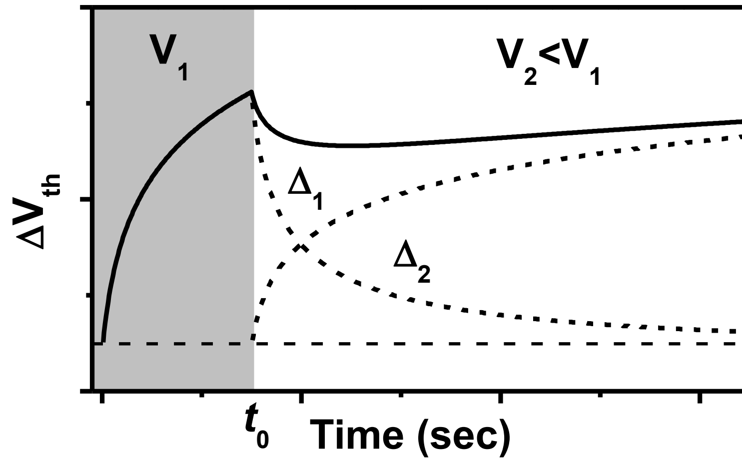


Figure 3.4. V_{th} shift under DVS is non-monotonic; when the stress voltage is changed from V_1 to V_2 (assuming $V_2 < V_1$).

To handle such a voltage transition, using a non-zero time, t_0 to calculate the occupation probability at time t (time elapsed after t_0) using Equation (3.2):

$$P_{01}(t+t_0) = \frac{\tau_{eq2}}{\tau_{c2}}\left(1-e^{-t/\tau_{eq2}}\right) + P_{01}(t_0)e^{-t/\tau_{eq2}} \tag{3.7}$$

where τ_{eq2}, τ_{c2} represent the time constants under voltage V_2. Using Equation (3.3), $\tau_{eq1}=\tau_{eq2}$, since τ_{eq} depends only on parameter p, which is independent of the voltage. Substituting this property in Equation (3.7):

$$P_{01}(t+t_0)=\frac{\tau_{eq}}{\tau_{c1}}\left(1-e^{-t/\tau_{eq}}\right)-\frac{\tau_{eq}}{\tau_{c2}}\left(e^{-t/\tau_{eq}}-e^{-(t+t_0)/\tau_{eq}}\right) \tag{3.8}$$

where τ_{c1} and τ_{c2} correspond to voltages V_1 and V_2. Following similar steps as in static model derivation, we arrive at a closed form solution [58]:

$$\Delta V_{th}(t)=\phi_2\left[A+B\log(1+Ct)\right]+\phi_1.B\left[\log\left(\frac{1+C(t+t_0)}{1+Ct}\right)\right] \tag{3.9}$$

where ϕ_1 corresponds to the voltage V_1 and ϕ_2 corresponds to V_2. The degradation in Equation (3.9) is physically interpreted as a sum of two components, Δ_1 and Δ_2 which are proportional to ϕ_1 and ϕ_2 respectively. When the voltage is changed to a lower voltage, traps emit some of the charge carriers, and the number of occupied traps reaches a new equilibrium. Δ_2 dominates initially, which contributes to the recovery. If the operation under V_2 continues for a longer time, Δ_1 eventually takes over and ΔV_{th} increases. Such a non-monotonic behavior is correctly predicted. Table 2 presents the summary of static and dynamic models based on trapping/de-trapping theory [58]. When the voltage is increased, the degradation rate rises at the point of voltage change. Figure 3.5 validates the dynamic model. Non monotonic behavior when stress voltage transition to a lower

Table 2. Summary of TD based compact aging

Constant stress	$\Delta V_{th}(t)=\phi\cdot[A+B\log(1+Ct)]$
Random Input Stress	$\Delta V_{th}(t+t_0)=\Delta_1+\Delta_2$ $\Delta_1=\varphi\left(A+B\log(1+Ct)\right),$ $\Delta_2=\Delta V_{th}(t_0)\left(1-\frac{k+\log(1+Ct)}{k+\log(1+C(t+t_0))}\right)$

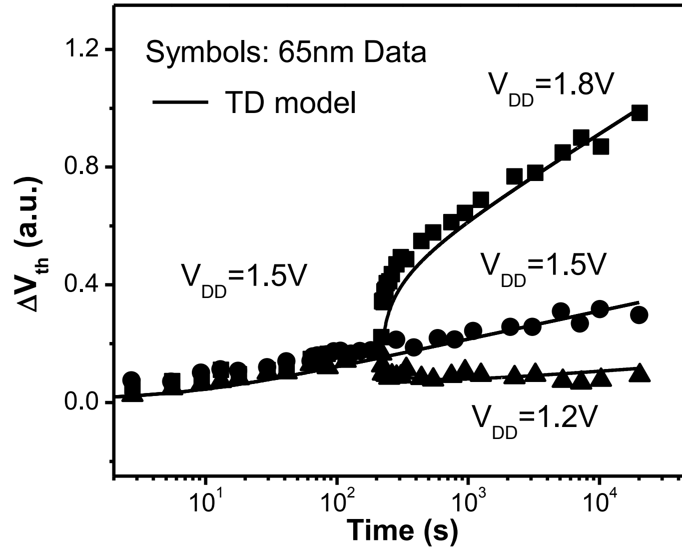


Figure 3.5. The T-D model predicts the dynamic behavior under voltage tuning, and the convergence to the constant stress condition.

value is correctly predicted by TD based random input model. Under this condition, the device experience recovery period, before the stress goes back to the equilibrium condition. Eventually, the degradation rate goes to the same as the constant stress under the lower voltage. This behavior is predicted from Equation (3.9), where the second component dominates initially, resulting in the recovery; after t>>200s, the second component decays down and the first component takes over, leading to the stress behavior under the second voltage. Experimental results from the test chip well validate these non-monotonic behaviors, as shown in Figure 10, supporting further study on aging prediction under DVS. The two components in Equation (3.9) play an important role in long-term prediction under multiple cycles.

Higher recovery is seen when the device is stressed at 1.8V compared to 1.65V as more traps are captured under higher stress voltage. The TD model captures such behavior. As stress voltage continues to be 1.2V after 200 seconds, the temporary recovery is overwhelmed by the capture of traps under lower stress voltage. Increasing stress time causes the degradation to converge to this constant stress voltage at 1.2V. This behavior is predicted from Equation (3.9), where the second component dominates initially, resulting in the recovery, while the second component decays down and the first component takes over, leading to the stress behavior under the second voltage. Figure 3.6 evaluates the model prediction, with different periods under the same voltage. In this study, the device is initially stressed under 1.8V, for 50s or 200s; then the voltage is switched to 1.65V. As the stress voltage is lowered, a temporary recovery behavior is observed due to the emission of excessive amount of trapped charges. The T-D model

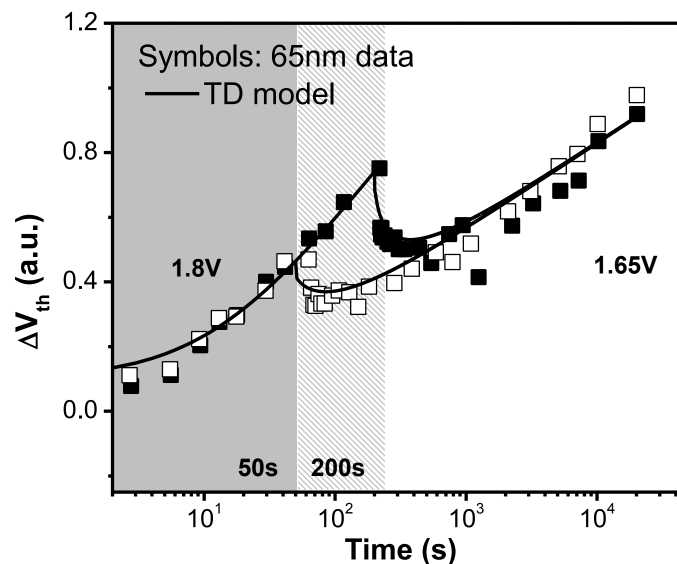


Figure 3.6. V_{th} shift under voltage tuning from 1.8V to 1.65V. The shift eventually converges to the final voltage, weakly dependent on previous stress history.

captures such behavior in both cases. In the case where the device is first stressed under 1.8V for 200s, the stress time is higher as compared to the case where the initial stress is 50s causing higher V_{th} shift. However, since in both cases, the device is later stressed for a much longer time (~10ks) at 1.65V, the degradation converges to the constant stress condition at 1.65V. This validation helps predict the aging under various switching activities (α) much needed for aging evaluation of digital circuits.

Random input models derived in this section are thoroughly validated with 65nm data. These models provide an accurate and efficient way to identify aging under arbitrary stress patterns, allowing designers to adequately guard-band their design. Such models can be more beneficial to AMS designs where the number of transistors is less than that in a digital design and the input is highly random. However for large scale digital circuits, using random stress models is insufficient to predict the lifetime of a high-speed design. Thus, long-term aging models based on TD theory is derived which is similar to RD derivation. This model can estimate a tight upper bound of aging, without tracking the behavior cycle by cycle.

3.4 Trapping/Detrapping Based Long-term Aging Model

Similar to the derivation of the RD model, a long-term model based on the TD theory is obtained. Based on the cycle-to-cycle model in the previous sub-section, $\Delta V_{ths,m}$ and $\Delta V_{ths,m+1}$ as seen in Figure 2.8 are connected by:

$$\begin{aligned}\Delta V_{ths,m+1} &= \phi_1\left[A + B\log(1 + C\alpha T_{Clk})\right] + \phi_2\left[A + B\log(1 + C(1-\alpha)T_{Clk})\right]\beta_{1,m} \\ &\quad + \Delta_{Vths,m}(1-\beta_{1,m})(1-\beta_{2,m})\end{aligned} \tag{3.10}$$

Using Equation (3.10) and repeatedly replacing the $\Delta V_{ths,m+1}$ by $\Delta V_{ths,i}$ for $i=m,\ldots,1$:

$$\begin{aligned}\Delta V_{ths,m} &= \phi_1\left[A + B\log(1 + C\alpha T_{Clk})\right]\left(1 + \sum_{i=1}^{m}\prod_{j=m-i+1}^{m}\beta_{1,.j}.\beta_{2,.j}\right) \\ &\quad + \phi_2\left[A + B\log(1 + C(1-\alpha)T_{Clk})\right]\beta_{1,m}\left(1 + \sum_{i=1}^{m}\prod_{j=m-i+1}^{m}\beta_{1,.j-1}.\beta_{2,.j}\right)\end{aligned} \tag{3.11}$$

Since obtaining a closed-form solution for Equation (3.11) is not straight-forward, we use the property $\beta_{1,m-1} < \beta_{1,m}$ and $\beta_{2,m-1} < \beta_{2,m}$,

$$\begin{aligned}\Delta V_{ths,m+1} &\le \phi_1\left[A + B\log(1 + C\alpha T_{Clk})\right]\left(1 + \beta_{1,.m}.\beta_{2,.m} + (\beta_{1,.m}.\beta_{2,.m})^2 + \ldots\right) \\ &\quad + \phi_2\beta_{1,m}\left[A + B\log(1 + C(1-\alpha)T_{Clk})\right]\left(1 + \beta_{1,.m}.\beta_{2,.m} + (\beta_{1,.m}.\beta_{2,.m})^2 + \ldots\right)\end{aligned} \tag{3.12}$$

Equation (3.12) is a geometric series and the upper bound of degradation is:

$$\begin{aligned}\Delta V_{ths,m} &= \phi_1\left[A + B\log(1 + C\alpha T_{Clk})\right]\frac{1}{1-\beta_{1,.m}.\beta_{2,.m}} \\ &\quad + \phi_2\left[A + B\log(1 + C(1-\alpha)T_{Clk})\right]\frac{\beta_{1,.m}}{1-\beta_{1,.m}.\beta_{2,.m}}\end{aligned} \tag{3.13}$$

Equation (3.13) is sensitive to the duty cycle, α (ratio of time under V_1 to time under V_2), time period (sum of operation times under V_1 and V_2 for a single cycle), and the stress voltage [58]. The long term model captures the tight upper bound of cycle-to-cycle prediction. Furthermore, experimental data is collected for 40 cycles under 1.8V, 1.2V stress and the cycle-to-cycle model captures the dynamic V_{th} shift (Figure 3.7). The

long term model captures the tight upper bound of cycle-to-cycle prediction, as illustrated in Figure 3.7 [58].

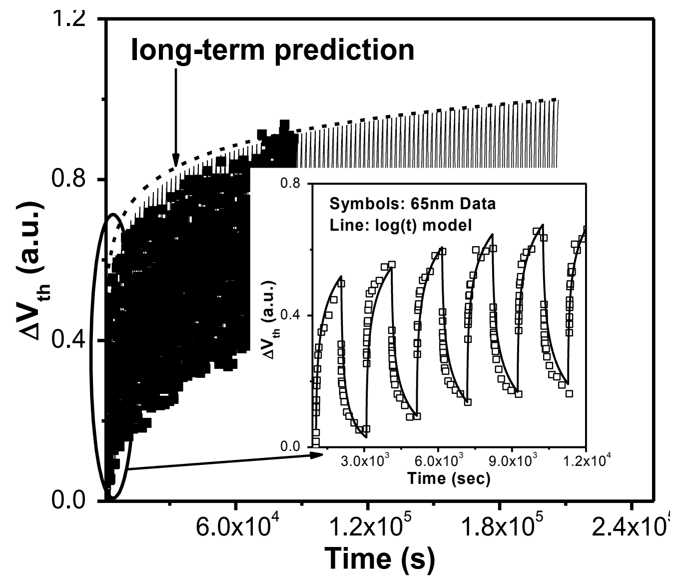
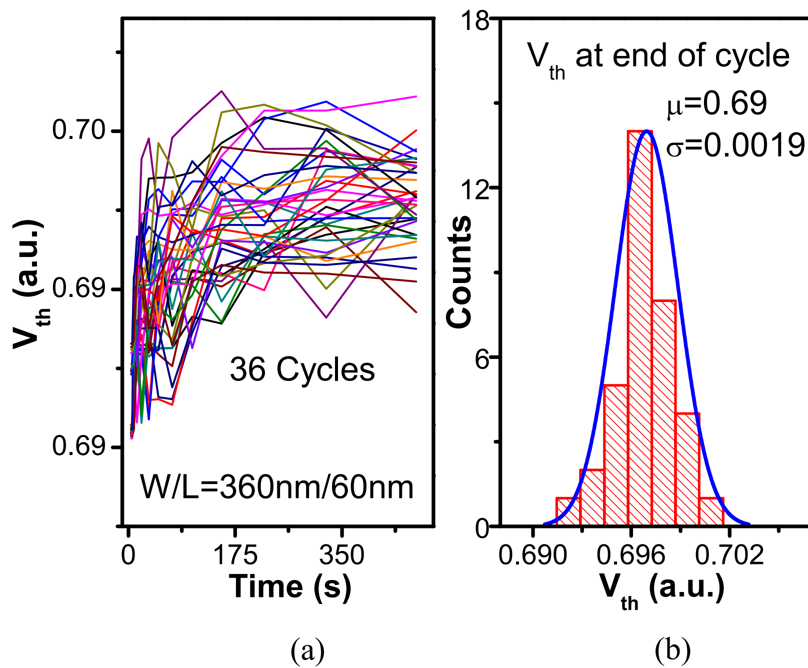


Figure 3.7. Cycle-to-cycle model predicts the dynamic degradation under 1.8V, 1.2V stress and long-term model tracks the upper bound of dynamic shift.

3.5 Aging Statistics Based on Trapping/Detrapping

With improvement in measurement technologies, evidence of charge Trapping/Detrapping (TD) for PMOS degradation has been accumulating. To correlate aging statistics based on TD process, a single 65nm device is dynamically stressed under a sequence of 1.8V and 0V, with 36 stress and recovery cycles [68]. The device is allowed sufficient recovery time before it is stressed again. In Figure 3.8a, the V_{th} degradation of the same device shows the stochastic nature caused by random charge trapping/de-trapping. V_{th} at the end of stress time (Figure 3.8b) follows a normal distribution, showing no history dependence of previous recovery. The degradation during the stress phase instantaneously recovers when the voltage is tuned to 0V,



(a) (b)

Figure 3.8. (a) Multiple stress (V_{gs} = -1.8V) cycles on the same device after sufficient recovery time; (b) Randomness at the end of the stress phase follows a normal distribution.

showing the process of de-trapping in BTI. The recovery cycles in Figure 3.9 clearly exhibits several discrete levels and time constants, confirming fast TD explains aging statistics.

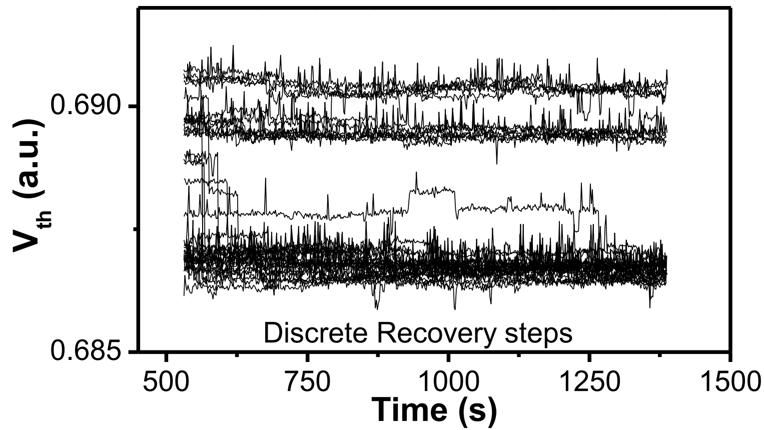


Figure 3.9. Discrete recovery steps in the amplitude and time constants without any history effect, implying the role of discrete charge trapping/de-trapping.

Stress time plays an important role in extraction of the model parameters for both RD and TD based compact models. It is desirable to extract the model parameters with minimum cost in terms of stress time. Thus it is important to evaluate the stability of model parameter with respect to stress time. Figure 3.10 shows the stability of time exponent (n) for RD model and parameters A, ϕ and C for TD model when extracted for different stress time. The value of n approaches 0.16 when the stress time used is long, which is consistent with RD theory prediction. But it exhibits much higher values when shorter stress time is used. Parameters ϕ, A and C for TD based *log(t)* model are considerably stable even for shorter stress time.

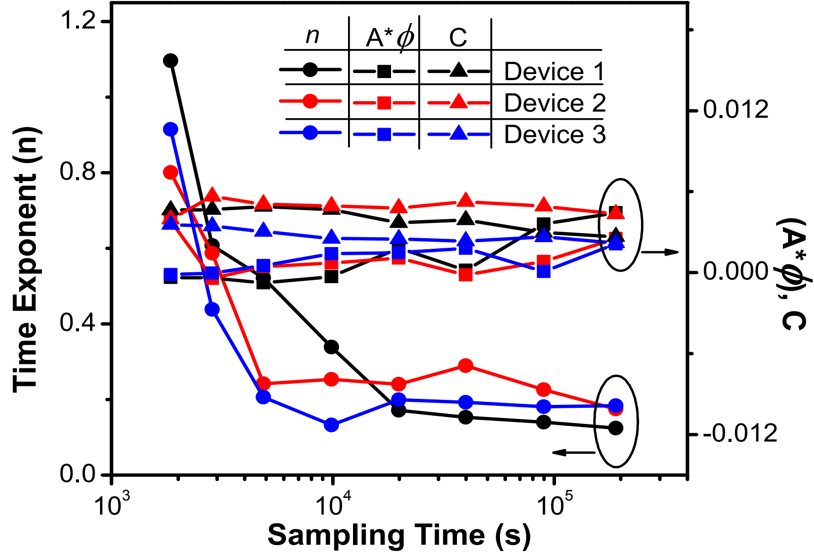
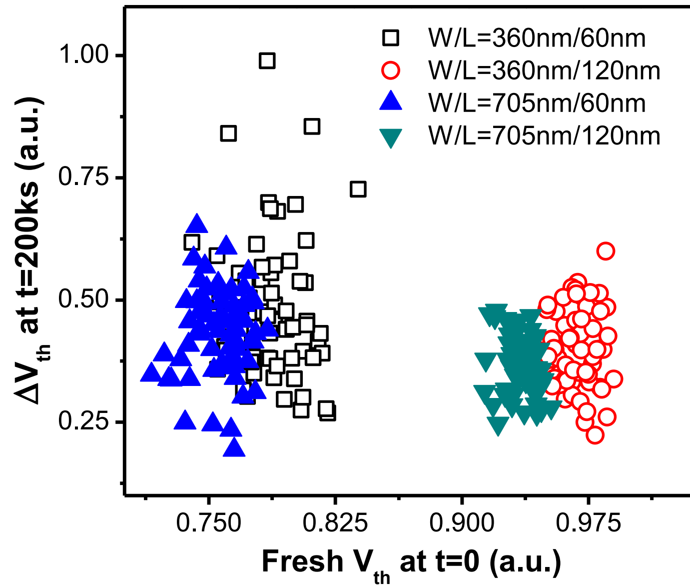


Figure 3.10. Model parameter for RD model requires higher stress time to converge to expected value of 0.16. Model parameters A, ϕ and C for TD based *log(t)* model can be extracted accurately from shorter stress time.

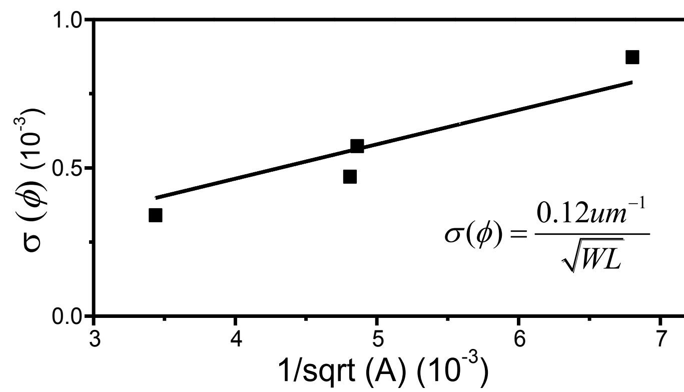
The randomness in the initial V_{th} of different PMOS devices explained by variation in trap numbers is reflected in the V_{th} shift under aging. The correlation plot in Figure 3.11(a) shows that ΔV_{th} has no correlation with fresh V_{th} and device size [69]. The variability in initial V_{th} (t=0) and ΔV_{th} decreases as the device size increases. Further evaluation of variation as a function of device size is conducted, as shown in Figure 3.11(b). The randomness is inversely proportional to the square root of the transistor area and the variation slope is 0.12μm^{-1}. The relation is given as [70],

$$\sigma(\phi) = \frac{0.12\mu m^{-1}}{\sqrt{WL}} \tag{3.14}$$

Above equation predicts that the aging variability increases with scaling of technology nodes and the device dimensions. This variability factor helps designers to estimate worst case degradation and accurately guard-band their design.



(a)



(b)

Figure 3.11. (a) No correlation between fresh V_{th} (t=0) and V_{th} shift. (b) Decrease in ϕ variation with increase in transistor sizing.

3.6 Combining RD and TD Principles

Previous sections focuses on developing and validating RD and TD models based on 45nm and 65nm data. With such comprehensive validation and backing of solid physical theories, once cannot isolate either RD or TD for accurate prediction. Relative dominance of RD or TD theory depends on the fabrication technology used. This is clearly reflected in the data set presented previously. The 45nm dataset favors RD theory which suggests cleaner process. 65nm data used to validate the TD models has higher number of traps in the oxide causing logarithmic behavior. Many research work shows that the final V_{th} shift is a result of fast TD events and a relatively slow RD process [62-65]. Thus it is indeed important to combine RD and TD principle for a unified model which greatly enhances lifetime prediction accuracy. In this work, a preliminary approach is used to combine two mechanisms in an effort to pave a future path for BTI modelling. In this work, we have combined both RD and TD principles by:

$$\Delta V_{th} = \frac{q\Delta N_{IT}}{C_{ox}} + \frac{q\Delta N_{OT}}{C_{ox}} \tag{3.15}$$

N_{IT} and N_{OT} are the interface charges and the oxide trap charges responsible for RD and TD induced threshold voltage shift in a device. Based on this equation, the ΔV_{th} can be summed together to combine both principles to the first order.

$$\begin{aligned} &\Delta V_{th} = \Delta V_{th}(RD) + \Delta V_{th}(TD) \\ &\Delta V_{th}(RD) = A_{RD} \cdot t^{n} \\ &\Delta V_{th}(TD) = A_{TD}\phi \end{aligned} \tag{3.16}$$

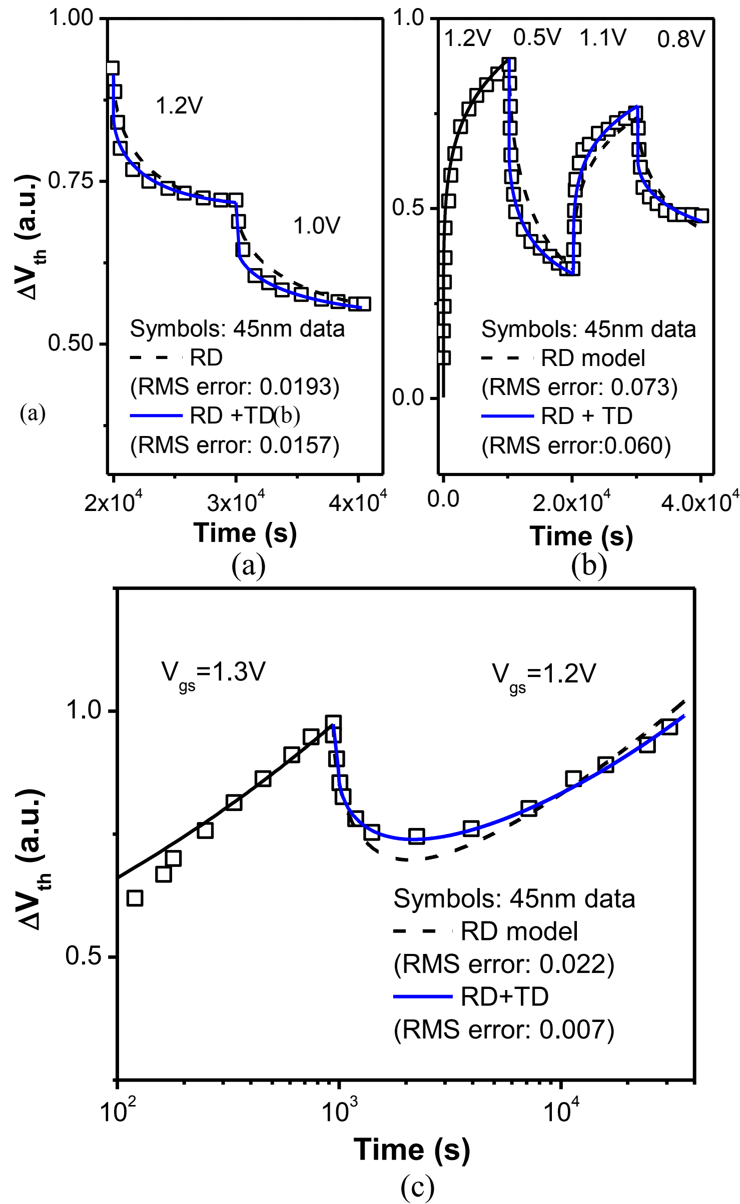


Figure 3.12. Improved recovery prediction in combining the RD and TD components. The TD component is mainly responsible for the fast recovery.

Trapping/de-trapping is typically a fast mechanism; as a result we add only the constant parameter ($A_{TD}\phi$) to RD based models while neglecting the *log(t)* part which is responsible for the slower trap components. This helps capture the fast stress or recovery component due to charge trapping/detrapping during DVS or random input stress

conditions. Although this is an empirical addition, the underlying physics is accurately captured in the model. To demonstrate the improvement in prediction accuracy, Figure 3.12(a) shows the re-fitted prediction for recovery in Figure 2.6. RMS error clearly shows the improvement in the prediction accuracy. In Figure 3.12(b), a device is subjected to more changing stress voltage. In this case, ΔV_{th} prediction by RD based model shows mismatch with the data. However, on adding the fast trapping component to RD models the error is significantly reduced. Similar improvement is show in Figure 4.1(c) for non-monotonic behavior. These results shows accuracy enhancement in 45nm technology node which is dominated by RD. Prediction accuracy of the model Equation (3.16) is shown in Figure 3.13 for 65nm data. This technology node shows dominance for TD as seen in previous chapter. All the comprehensive validation and results indicates final BTI aging model should be a unified with RD and TD theory for accurate lifetime prediction.

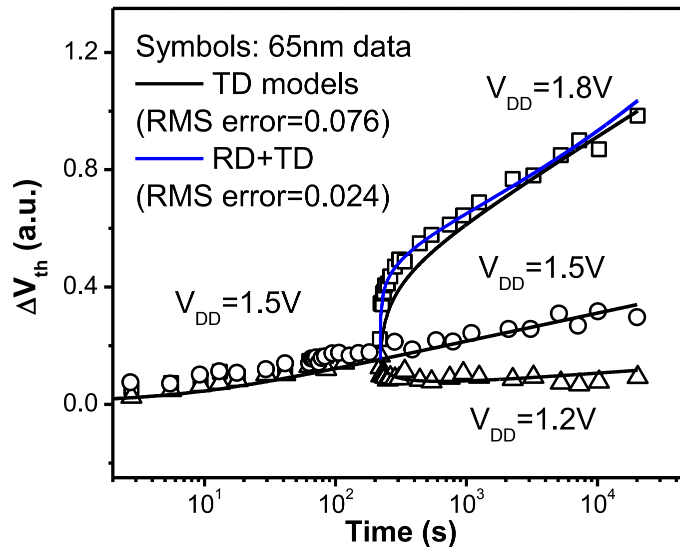


Figure 3.13. Improvement in the prediction accuracy by combining RD and TD principles for 65nm technology which is dominated by TD.

CHAPTER 4

COMPACT AGING MODEL FOR CHANNEL HOT CARRIER

4.1 Motivation for CHC Modelling

AMS circuits are typically biased in saturation region to attain high linearity for the small signal during power ON mode. However, such condition leads to continuous CHC degradation leading to a shift in threshold voltage as well as circuit parameters over time. Figure 4.1 presents the increment in threshold voltage (ΔV_{th}) due to both CHC and NBTI, indicating different shifts in analog and digital circuits. Compact model of CHC is essential for AMS circuits. In order to enable proper guard-banding of AMS designs, we investigate the underlying physics collecting stress data from 65nm thick-oxide devices, under various gate lengths and bias conditions.

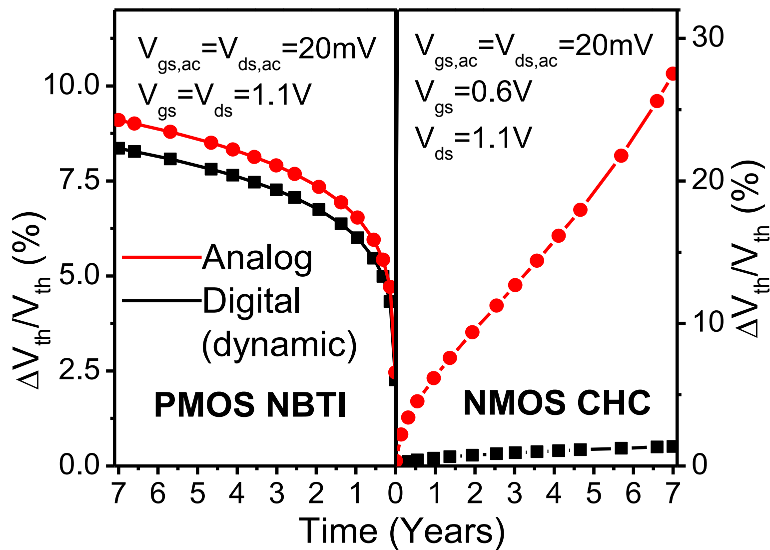


Figure 4.1. Different aging in analog and digital circuits due to NBTI and CHC.

4.2 Compact Aging Model for Channel Hot Carrier

This section presents the development of the CHC aging model for power ON mode of AMS circuits. Channel hot carrier is degradation mechanism observed in nMOSFETs. The main source of the hot carriers are the energetic carriers that leads to impact ionization within the substrate and the generated electrons or holes inside the channel can be injected in to the gate oxide. During this process, the injected carriers can generate interface or bulk oxide defects and as a result, the device characteristics like on-state current, threshold voltage, trans-conductance, etc. degrade over time.

CHC effect is comparatively less for digital gates but for AMS designs, transistors degrade continuously as they operate in saturation region. CHC can be physically described as the generation of charges in the region close to the Si/SiO_2 interface. Charge generation is localized to drain region rendering CHC to be a strong function of drain-source (lateral field dependence) voltage. Figure 4.2 shows the difference in the 2D hydrogen atom diffusion at drain end for CHC degradation compared to 1D diffusion for BTI effect of a transistor [10].

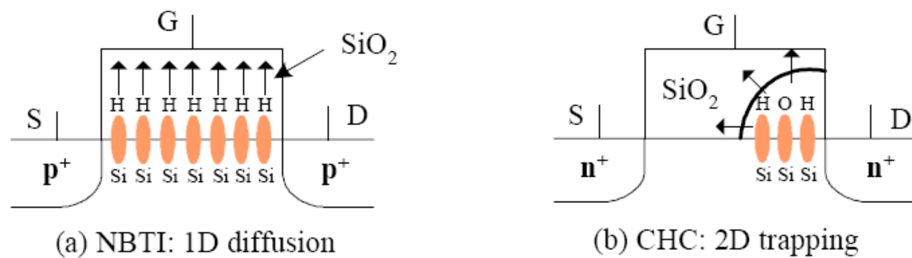


Figure 4.2. The reaction-diffusion mechanism (a) NBTI: 1D hydrogen species diffusion (b) CHC: 2D hot carriers trapping

Reaction-Diffusion model can be accurately used to predict V_{th} shift due to CHC. The interface trap generation rate for CHC can be written as a balance between dissociation and annealing rates of Si-H bonds [10]:

$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT}) - k_R N_H N_{IT} \tag{4.1}$$

Where, N_0 is the initial concentration of the Si-H bonds, P is concentration of the inversion hole, N_{IT} is the interface traps, k_R and k_F are the reaction rates and N_H is the hydrogen density. During the initial period of the stress phase, trap generation is slow. Hence, $dN_{IT}/dt = 0$ and $N_{IT} << N_0$, we get

$$N_H N_{IT} = \frac{k_F}{k_R} P \cdot N_0 \tag{4.2}$$

Integrating Equation (4.2) for a given stress time and assuming interface trap generation for CHC occurs at drain end we can derive the close form equation for V_{th} shift of a device under CHC stress [10]. This compact model aligns with the lucky electron model which advocates higher degradation when device is in deep saturation. Thus for a constant gate voltage, increasing drain voltage results in higher V_{th} shift. Under this condition, the worst case CHC is observed at $V_{gs} \sim (1/3)V_{ds}$ for gate voltage higher that threshold voltage. However, role of e-e scattering is reported for CHC for advanced technology nodes [71][72]. At higher V_{gs} for thin oxide devices, the electric field across oxide increases which causes higher scattering of electrons for the same drain voltage. Because of the effect of e-e scattering, the worst stress condition for CHC is shifted to V_{gs}=V_{ds}. In Equation (4.2), parameter k_R depends on lateral and vertical electric

field across the channel. We modify the lateral electric field component to reflect the e-e scattering as presented in [71][72]. Final compact model is [73]:

$$\Delta V_{th}(t) = \frac{q}{C_{ox}} K_2 \sqrt{Q_i} \exp\left(\frac{E_{ox}}{E_0}\right) \exp\left(a \cdot \frac{E_m - \varphi_{it}}{\lambda}\right) t^n \tag{4.3}$$

In above equation, E_{ox} is the vertical electric field (V_{gs} dependence), E_m is the lateral electric field given as $(V_{ds}-V_{dsat})/l$, φ_{it} is the minimum energy in eV required by hot electron to create impact ionization and λ is the mean free path. E_0 is the activation energy and $Q_i \sim (V_{gs}-V_{th})$. K_2 and a are the fitting parameters. Figure 4.3 shows the model prediction versus silicon data for device length of 1.0μm. This figure shows dominance of e-e scattering and its effect due to which worst case CHC condition is at $V_{gs}=V_{ds}$. This shift in worst case condition is not favorable for AMS designs especially for biasing circuits using diode connection.

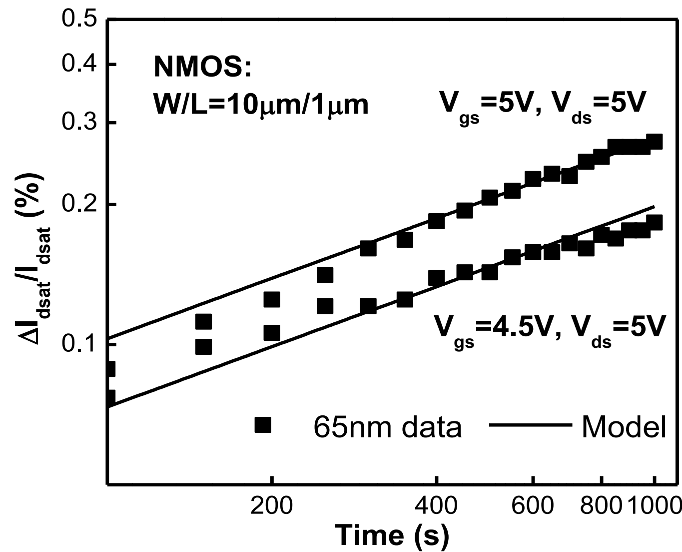


Figure 4.3. Compact model of the CHC effect is validated with 65nm data. The worst condition is observed at $V_{gs}=V_{ds}$, at the room temperature.

4.3 Model Validation in 28nm Technology Node

This section presents model validation at 28nm technology node. To examine the impact of aging, silicon data is collected from 28nm HK-MG devices at the minimum channel length. As a result of HK-MG technology, PBTI in NMOS devices also becomes relevant aging issue. BTI models based on RD or TD theories presented in previous chapters can be used to characterize PBTI at 28nm as the underlying physics remains the same. Figure 4.4 shows the device configuration used for NBTI, PBTI and CHC stress.

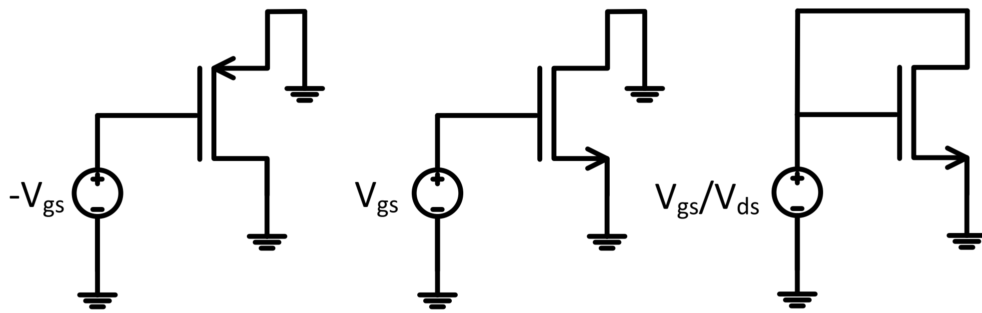


Figure 4.4. Stress conditions of discrete devices for various aging mechanisms. (a) NBTI stress condition for a PMOS; (b) PBTI stress condition for a NMOS; (c) Worst case CHC stress condition for NMOS with diode connection

To characterize voltage dependence, PMOS is stressed at different gate voltages. Figure 4.5 presents NBTI data along with the model prediction for different stress conditions. V_{th} shift demonstrates an exponential dependence on stress voltage which is consistent with RD or TD prediction for previous nodes. With introduction of the HK-MG technology, PBTI issues in NMOS become relevant along with prevailing CHC, which further aggravates the issue of aging in both digital and AMS designs. To collect

the silicon data, drain and source terminals are grounded. PBTI model is calibrated in Figure 4.6. PBTI also exhibits exponential dependence on stress voltage.

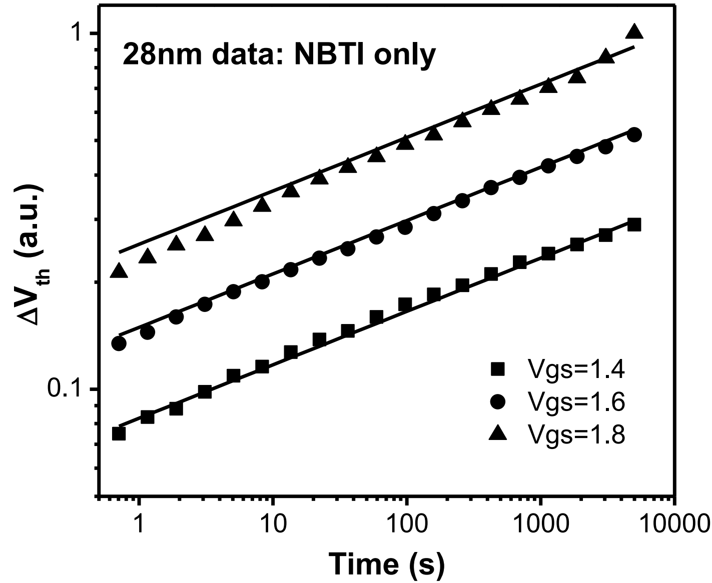


Figure 4.5. Static NBTI model calibrated with 28nm HK-MG data for different voltages and stress time.

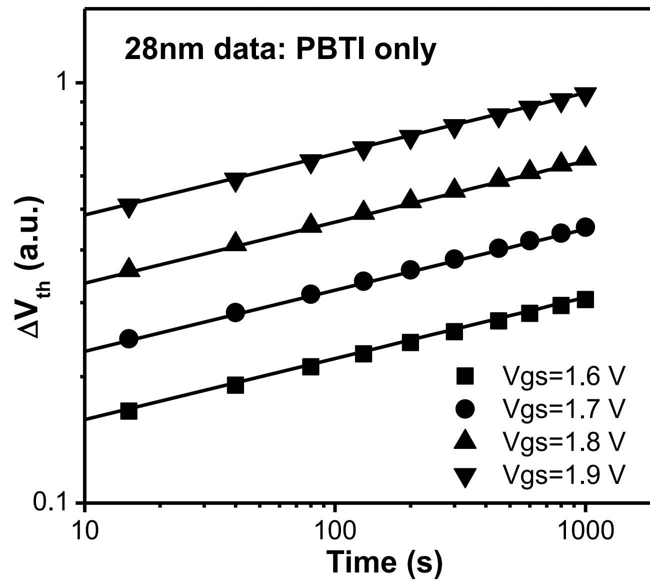


Figure 4.6. Static PBTI model calibrated with 28nm HK-MG data for different voltages and stress time.

A device is stressed in diode configuration which represents worst case for CHC to collect silicon data. However, aging data composed in this configuration is a combined result of PBTI and CHC. An empirical power law model is fitted against the collected data as demonstrated in Figure 4.7. Stress voltage follows the exponential dependence but the time exponent is significantly lowered than expected value for only CHC aging. To evaluate circuit aging due to intrinsic CHC component, it is important to decouple both aging mechanisms (PBTI and CHC). To extract the intrinsic CHC component, PBTI data in Figure 4.6 is subtracted from the coupled data in Figure 4.7. The CHC model in Equation (4.3) is then calibrated using the extracted intrinsic component shown in Figure 4.8 which eventually helps in evaluating aging model at 28nm technology node. The time exponent of extracted CHC is ~0.34 which is of the expected range. Further exploring the time exponent (n) shows initial device degradation is dominated by PBTI shown as k

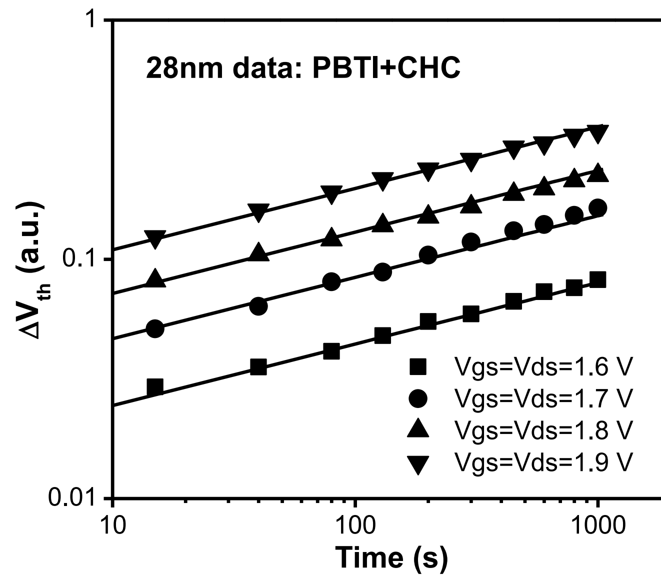


Figure 4.7. Coupled data due to PBTI and CHC stress at 28nm. Empirical power law model is used to fit the silicon data.

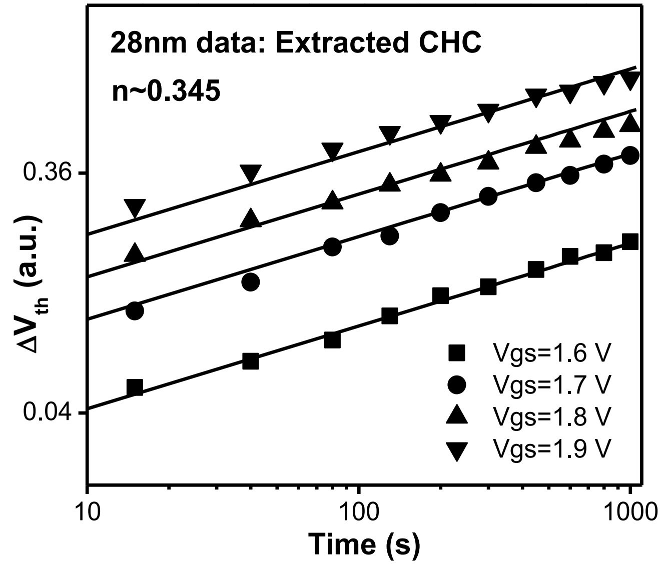


Figure 4.8. Decoupled CHC data and model calibration using data in Figure 4.7 and subtracting the PBTI component in Figure 4.6.

shaded area in Figure 4.9 where n~0.23. Eventually as the stress time increases, time exponent increases to 0.25 due to increasing impact of CHC. However, the final time slope remains lower than intrinsic CHC degradation in this technology node.

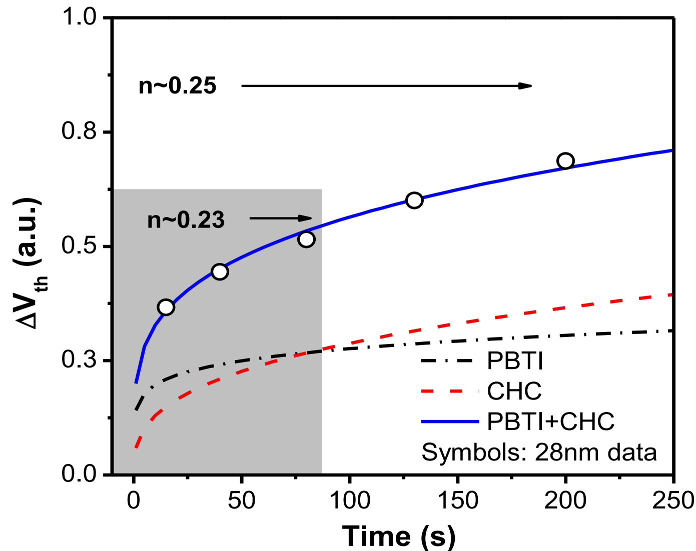


Figure 4.9. Time exponent of PBTI + CHC is initially dominated by PBTI and eventually by CHC. The overall time exponent will be lower that final CHC.

CHAPTER 5

VALIDATION OF AGING EFFECT AT CIRCUIT LEVEL

New proposed RD based models for all static, dynamic and long-term operating conditions are comprehensively validated with discrete device data at 28nm, 45nm and 65nm technology nodes in previous chapter. Often, the circuit aging can differ from device level aging due to higher operating frequency of designs compared to testing procedures. It is therefore important to validate the accuracy of the proposed aging models by estimating the performance degradation at circuit level.

In order to estimate impact of aging, a sub-circuit module is implemented in SPICE as illustrated in Figure 5.1. A voltage controlled voltage source subtracts the V_{th} shift calculated by model from V_{gs} emulating aging of a device. Proposed models are implemented in Verilog-A. Stress time is the simulation time from SPICE. To improve the simulation speed, input voltages are quantized into discrete levels for random input models. As a result, there is a trade-off between simulation speed and the voltage levels. Some AMS simulation requires static models where quantization is not required. Thus appropriate models should be used for efficient aging estimate.

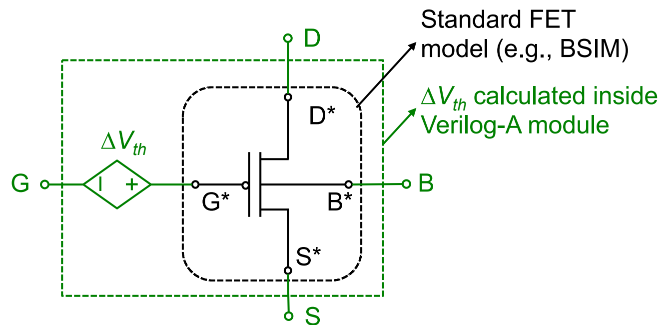


Figure 5.1. Verilog-A VCVS sub-circuit implementation.

5.1 Aging in Digital Circuits

A wide array of circuit operations co-exists on present day SoC. Different circuit operations presents unique challenges to identify lifetime under BTI stress. A device operating under constant stress voltage needs a static aging model. Different from static stress, digital circuits employ DVS extensively to balance workload and power consumption as shown in Figure 5.2. Under such operation, random input stress model is needed. Furthermore, large scale logic design encounters periodic input for different duty cycles and frequency. To increase efficiency, a long-term BTI model is used which can predict upper bound of threshold voltage shift for a periodic input. Previous chapter presented a complete suite of RD and TD based equations for aging simulation. Combining both mechanism yields improved prediction accuracy.

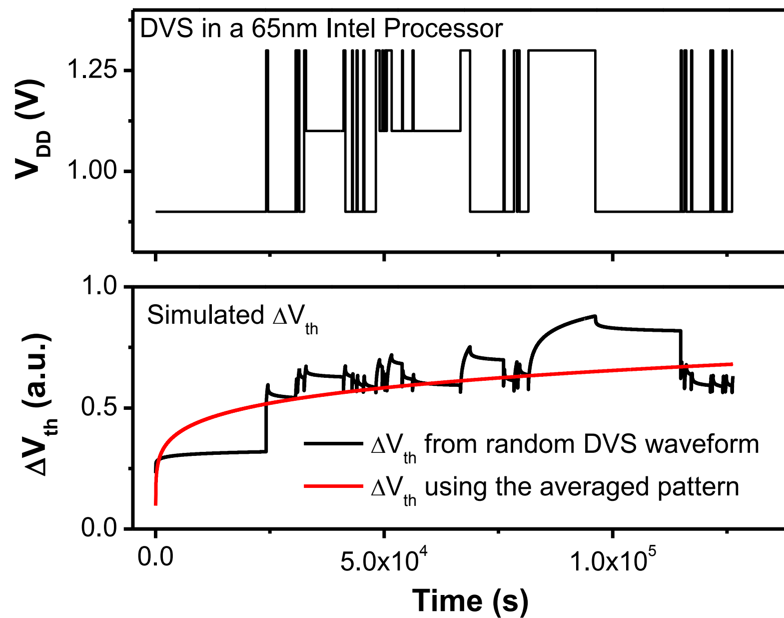


Figure 5.2. ΔV_{th} predicted from the averaged pattern significantly deviates that from dynamic aging simulation.

To validate the new models in digital circuit, silicon data is measured from 45nm ring oscillator (RO). The frequency change (ΔF/F) of RO is measured as a direct index of the degradation, which is proportional to PMOS threshold voltage change under NBTI. Figure 5.3 presents the test circuit of RO used for aging analysis. Frequency change in 11 stage ring oscillator is monitored during the test. The ring oscillator is activated by the enable (V_{enable}) pin. Different from traditional RO based aging test, the supply voltage of this circuit, V_{RING}, is switched between V_{DD} (stress mode) and 0 (recovery mode) at different duration, in order to emulate dynamic voltage scaling (DVS) encountered in logic circuits. The data is collected at regular intervals at multiple supply voltages and temperature. The pin, V_{DIV} is implemented to control the frequency divider and output buffer. It also helps to eliminate the impact on frequency shift of RO due to aging of peripheral circuits, thus giving a clean data [35].

ΔV_{th} of a device in RO has a strong dependence on the dynamic scaling of supply voltages due to recovery effects. Figure 5.4(a) shows the basic test pattern in a ring oscillator with alternate active and sleep modes, each for 5000 seconds duration. The

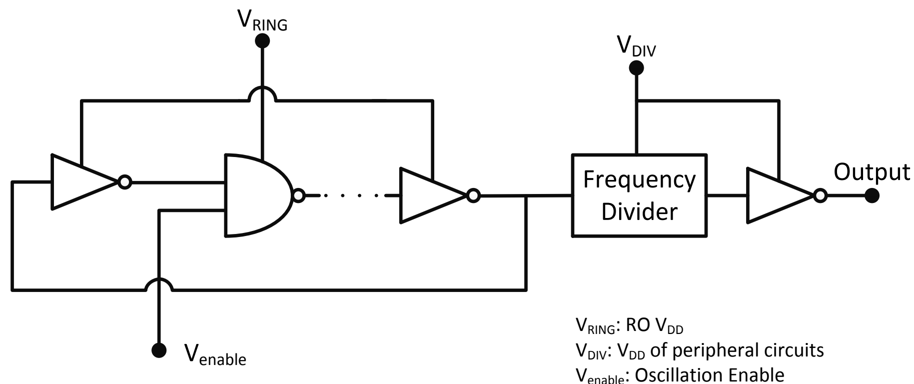


Figure 5.3. Test circuit at 45nm used for the validation.

increase of frequency degradation in the active mode and its decrease in the sleep mode are well predicted by the new random stress models. Further to enhance accuracy, a TD component is added to the RD model for frequency change prediction. Figure 5.4(b) shows the impact of the recovery on the frequency shift of RO. Although the stress times are same for both patterns, the recovery in PMOS device causes over all degradation to be less. These effects are successfully captured by the proposed aging models.

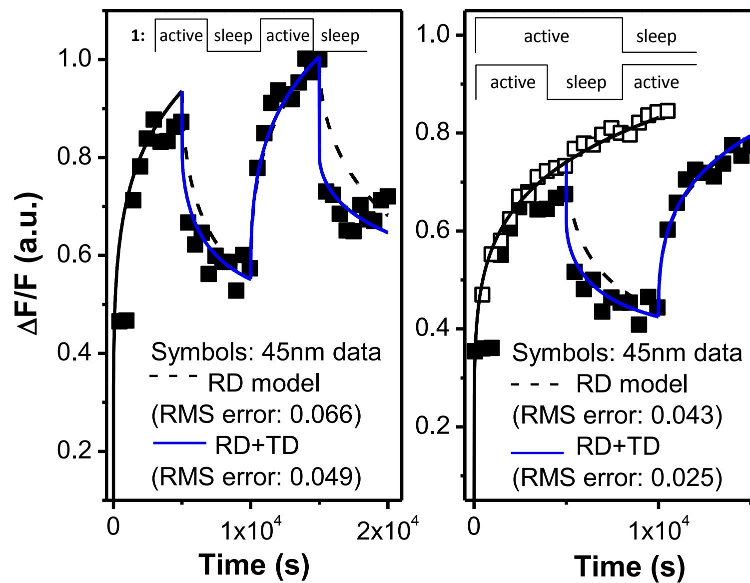


Figure 5.4. (a) Validation of model with circuit-level DVS data. (b) Different stress pattern captured by models.

5.2 Aging in AMS Circuits

Analog/mixed signal circuits encounter more complex stress patterns. Further, degrading device changes the DC biasing conditions, which in turn change circuit performance. Figure 5.5 shows the real-time impact of NBTI on a PMOS input differential amplifier. The stress input of a device is an AC signal with two different frequencies. Conventional prediction with an average static pattern fails to capture amplitude distortion (Figure 5.5(b)). Using new random input stress models, an accurate aging analysis on differential amplifier can be performed for the lifetime analysis. Accurate aging prediction has a trade-off with simulation time in SPICE. Real time stress and recovery causes SPICE to increase the internal time steps which take longer simulation time compared to the average aging stress pattern.

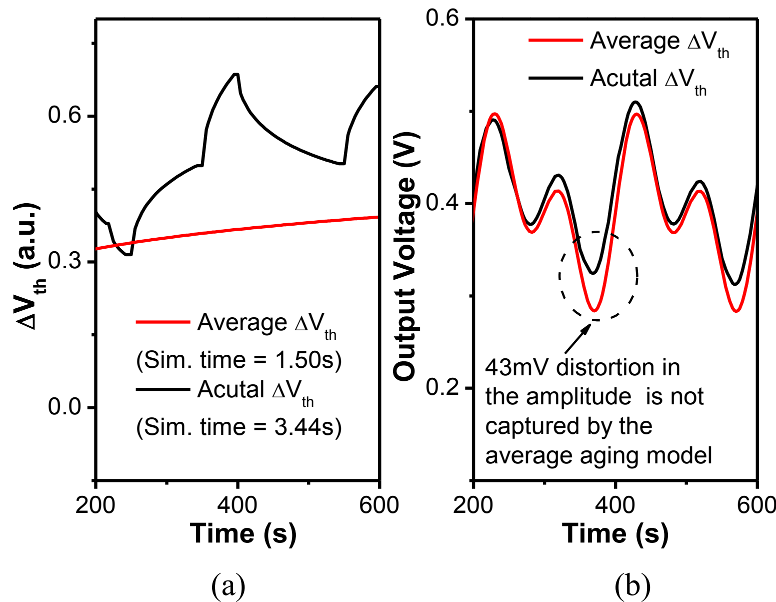


Figure 5.5. (a) V_{th} shift prediction (b) Output voltage of amplifier. Average analysis fails to capture the distortion.

To present application of the aging models in AMS design, silicon data is collected from a complete analog circuit block, i.e. LNA in 90nm CMOS (Figure 5.6(a)). Aging models calibrated with discrete device data are used to estimate the degradation of gain and noise figure (NF) of single ended LNA shown in Figure 5.6(b).

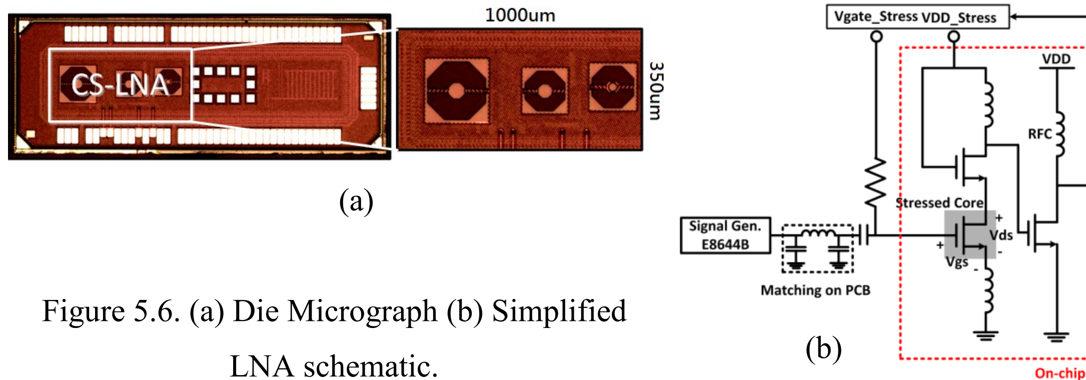


Figure 5.6. (a) Die Micrograph (b) Simplified LNA schematic.

The shaded device (DUT) is stressed by applying gate and drain voltage. As a result, the LNA degradation is caused by static stress and appropriate models needs to be used. CHC model accurately predicts the performance under aging effects measured at the center frequency, 1.65GHz. Cadence - Spectre is used for the simulation of LNA with Verilog-A language used to code the static aging models in design environment. Figure 5.7 present the gain and NF shifts over 48 hours stress test. Note that the measured data exhibits two larger deviations from the model prediction. It is due to the temperature sensitivity of the noise source (Agilent 346A), as it cannot be placed inside the oven. This phenomenon regularly occurs over different chips during the night time when the lab temperature drops. According to the calibrated model prediction, the overall V_{th} shift is close to hundred mV after stress.

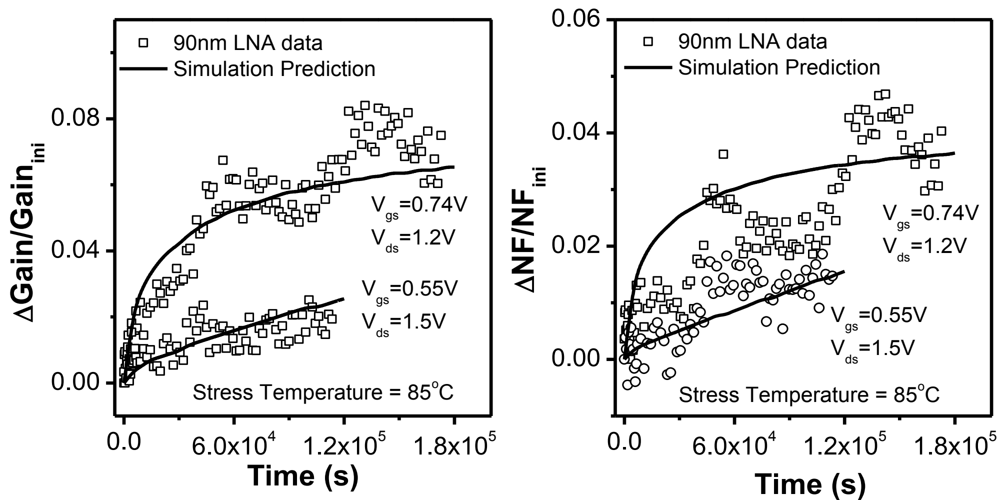


Figure 5.7. Measured data vs. CHC model prediction of gain degradation and NF degradation for single ended 90nm CMOS LNA structure

This section presents the implementation of RD/TD based aging models in either SPICE or CADENCE environment. The circuit structures used for aging simulations are simple and experience constant stress and the performance is measured at particular operating condition. While the simulation setup described is ideal for model validation, it is not realistic. In AMS circuits, the stress on a device will cause the operating condition to shift which in effect changes the degradation rate. Similarly, SPICE or CADENCE-ADE setups are not suitable for simulation of VLSI designs. Aging simulators provided by commercial companies have certain limitations which yields inaccurate lifetime analysis [28-30]. Thus, there is a dire need for new simulation tools for both AMS and digital designs apart from accurate aging models. Next chapter proposes new aging simulation tool for AMS designs by mitigating drawbacks of existing reliability tools and identifies critical aging phenomenon in AMS and digital structures.

CHAPTER 6

RELIABILITY TOOLS FOR LIFETIME ESTIMATION

6.1 Simulation Framework for AMS Design

To facilitate resilient design practice, the understanding of certain critical effects such as bias runaway and duty cycle shifts needs to be integrated into the simulation environment. However, current aging prediction methods fail to account for the wide operation range of AMS and digital designs. Figure 6.1 shows the framework of RelXpert (extended version of *Berkeley reliability simulator*), a commercial reliability tool. Commercial tools [28-30] uses SPICE simulator to generate sufficient samples of pre-aged models for all transistors. Based on the sampled stress information, pre-aged degradation models for each transistor are extracted. The extracted models are used to extrapolate the degradation to the end of lifetime, as a result temporal shift of operating conditions due to circuit degradation are not considered. This method may work for the gradual degradation, but is incapable to track the fast change when feedback between

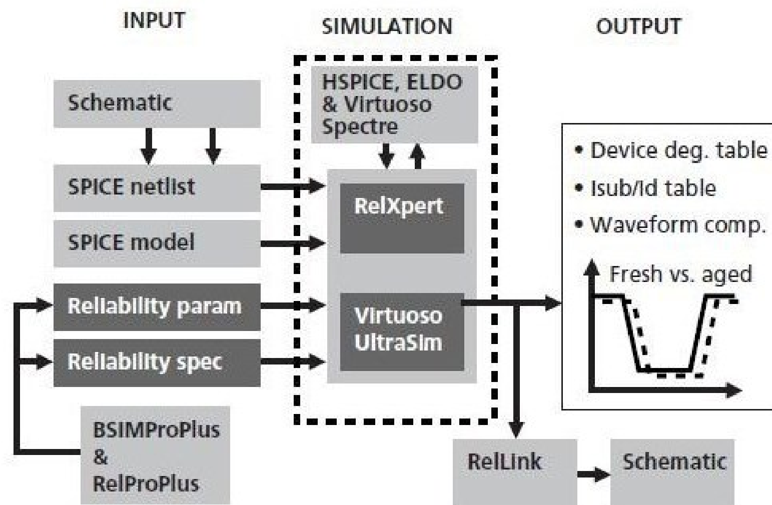


Figure 6.1. Framework of RelXpert, a commercial reliability tool.

aging and circuit topology happens. This leads to inaccurate aging prediction especially in the circuits where the shifted node voltages accelerate the degradation; similar to bias runaway. Further, this tool is computationally expensive and consumes large portion of the memory usage. In this context, a new, iterative approach is indispensable, which eliminates the reliance on the extrapolation and directly predicts the shift toward the end of the lifetime.

In this work, we propose new simulation methodology to overcome the barriers presented by conventional method as shown in Figure 6.2 [74][75]. As a cornerstone, we use proposed aging models with the proposed framework for accurate and efficient aging prediction of AMS circuits and identify bias runaway. In this approach, we start with a test bench and input conditions which are input to SPICE simulator to obtain the operation voltages and transient conditions. The aging models use the extracted node voltages and input conditions to predict threshold voltage shift for all transistors in the

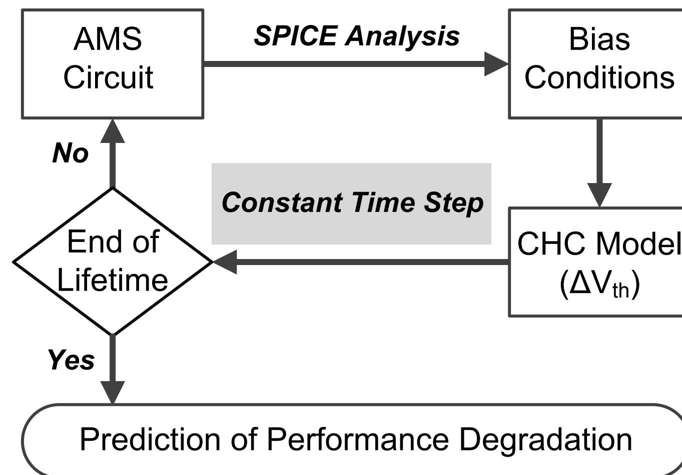


Figure 6.2. Iteration based simulation approach captures the feedback behavior.

circuit. The aged models can predict the degradation for a given stress time. However, the lifetime estimate is performed iteratively with constant time steps. For each time steps, threshold voltages of transistors are updated and corresponding new circuit conditions are used as an input to aging models for subsequent iterations. This process is repeated for N (life time/step size) times for the entire period of specified lifetime without any extrapolation of V_{th} to the end. This approach promises to track any feedbacks in design. The conventional tool underestimates the degradation due to extrapolation as shown in Figure 6.3. The inset figure shows the circuit used for aging comparison.

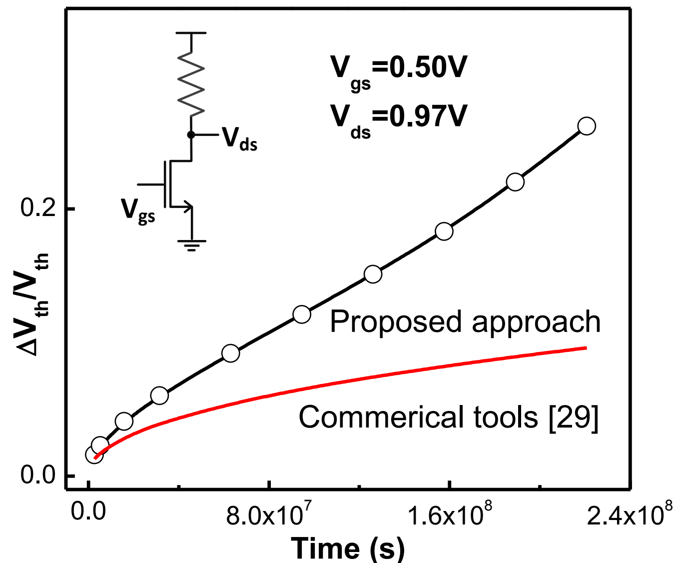


Figure 6.3. Conventional reliability tools, which are based on the extrapolation method, fail to capture the rapid change.

Based on the proposed methodology and aging models, next sections highlights few critical phenomenon occurring in AMS and digital circuits and presents valuable design insight for accurate lifetime analysis.

6.2 Bias Runaway in AMS Designs

6.2.1 Physical Analysis

Constant current sources used in AMS circuits are difficult and expensive to design; as a result AMS circuits typically have one reference current source per chip to bias entire design. Current mirroring circuits are extensively used to copy reference current or generate a stable biasing voltage as per the requirement. As discussed in previous section, the diode connection of a device causes worst case degradation. This situation is further aggravated by a feedback loop in this configuration. This significantly limits the lifetime of the AMS designs under such inherent feedbacks.

The bias circuit must be reliable, since it needs to stably generate either a voltage or a current reference for other AMS units. Figure 6.4 explains the details for feedback loop: bias runaway. Under biasing voltage (V_{bias}) for a given biasing current (I_{bias}), the NMOS transistor subjects to the worst CHC. Such voltage condition at gate and drain causes degradation which manifests as threshold voltage increases. V_{th} increases due to

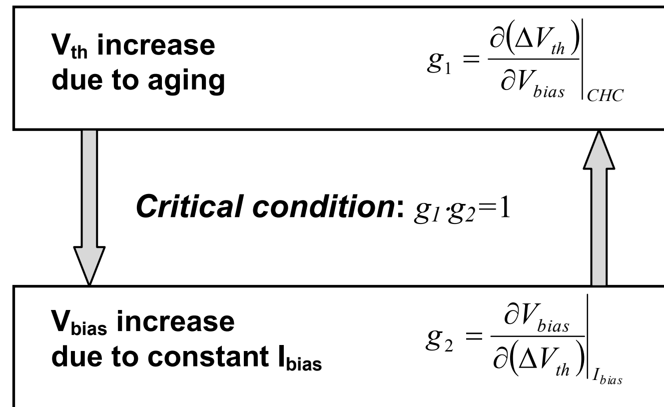


Figure 6.4. The physical basis for bias runaway: A feedback loop exists between the CHC effect and the bias condition to maintain a constant I_{bias}.

CHC causes V_{bias} to a higher voltage in order to maintain the same constant bias current, I_{bias}, which in turn accelerates the degradation rate of CHC. As this process continues, there is a risk that such a feedback loop becomes unstable, i.e., into an uncontrolled positive feedback. Any accelerated reliability threat to biasing circuit can increase V_{bias} such that entire design fails. Thus it is very important to guard-band designs appropriately. We evaluate bias runaway to derive a critical boundary condition which helps designers to identify initial V_{bias} which avoids bias runaway.

Mathematically, the boundary condition of the positive feedback is described by the loop gain, as shown in Figure 6.4. CHC degradation dependence on V_{bias} represents gain g_1, while relation between shifts in V_{bias} due to V_{th} change is represented by g_2. V_{bias} is a linear function of V_{th} causing $g_2 \sim 1$. Stability of such system is dependent on the feedback factor g_1. For a system to be stable g_1 is a small value, which is the case when V_{bias} has low value. For system to become unstable, g_1 has positive value for higher V_{bias}. Thus, we can derive the boundary condition for bias runaway condition (Equation 6.1) by using $\boldsymbol{g_1 . g_2 \sim 1}$. Solving boundary condition helps designers to identify initial start of life V_{bias} to avoid bias runaway. The boundary equation is a function of oxide thickness, device length as well as model parameters of CHC equation. The parameters from CHC model remains same as calibrated with static stress condition [75].

$$V_{critical} = \left[-\ln\left(C_1\right) + C_2 \right] / C_1 \tag{6.1}$$

where, $C_1 = a/\lambda + \left(t_{ox}E_0\right)^{-1}$, and $C_2 = V_{th} / \left(t_{ox}E_0\right) + a \cdot \left(\varphi_{it} + V_{dsat}\right)/\lambda$. Note that for NBTI, $g_1 . g_2$ is always <1, since its sensitivity to V_{bias} (i.e., g_1) is much lower. The boundary equation is used to evaluate the loop gain at different initial V_{bias} for a bias circuit as

shown in Figure 6.5. Indeed, with higher V_{bias}, the loop gain can be larger than 1, triggering the runaway behavior. From this perspective, a critical V_{bias}, $V_{critical}$, is defined at $g_1 g_2=1$ (Figure 6.5). Moreover, a compact model of $V_{critical}$ is derived, as a function of device and CHC parameters. If the initial value of V_{bias} is much lower than $V_{critical}$, then the circuit will only experience a gradual shift, without the risk of bias runaway. Once V_{bias} is close to $V_{critical}$, even a small increase will destruct the feedback system. This is shown in Figure 6.6, where the initial biasing voltage determines if there will be a runaway or not. If the initial V_{bias} is higher than $V_{critical}$, positive feedback dominates causing a rapid increase in the bias voltage. Boundary equation accurately defines $V_{critical}$ after which positive feedback severely limits operation (Figure 6.6) of AMS designs. Therefore, it is essential to have a sufficient margin in V_{bias}. The new model provides a convenient guideline for reliable design of bias circuits.

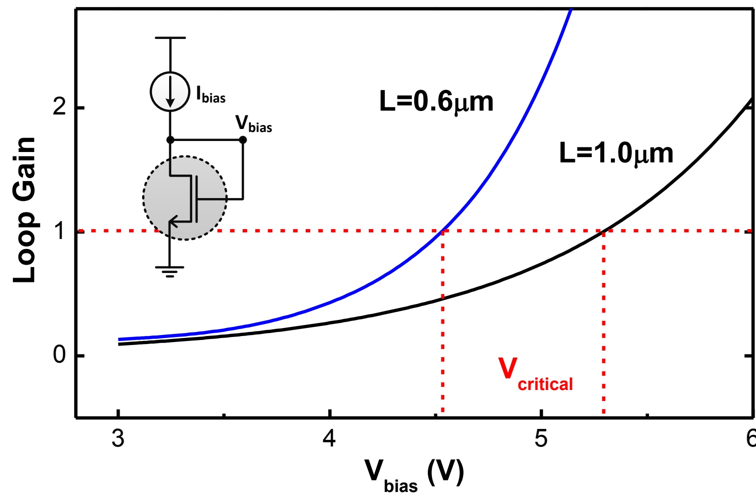


Figure 6.5. The loop gain may exceed 1 as V_{bias} increases, creating a positive feedback. Thereafter, the bias runaway happens for higher loop gain.

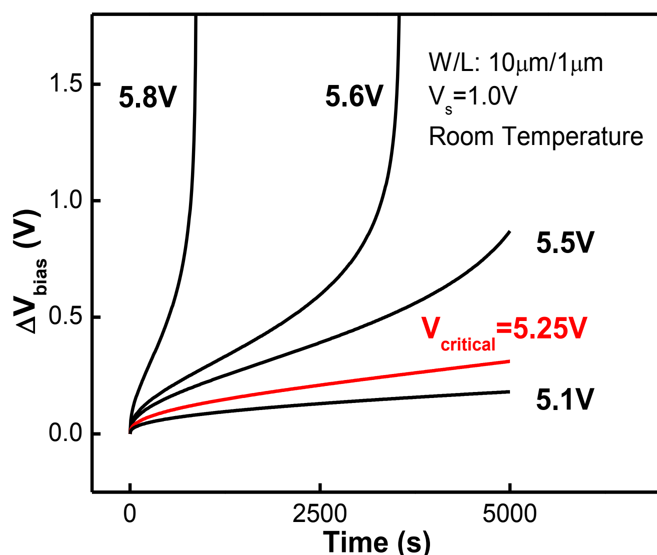


Figure 6.6. The transition to the bias runaway is highly sensitive to the initial bias condition (V_{bias}) at time=0.

6.2.2 Bias Runaway: Silicon Validation

In previous sections, bias runaway is thoroughly analyzed and a critical boundary equation is presented. Along with newly identified positive feedback, a new CHC aging model and simulation framework are also developed to overcome existing challenges.

A thorough validation of the CHC aging model, bias runaway and methodology is required. Stress data from 65nm thick-oxide devices, under various gate lengths (0.28μm-1.0μm) is collected to calibrate CHC aging model and thereby the boundary condition for bias runaway. It is shown that bias runaway occurs when initial bias voltage is higher than critical voltage and typical gradual degradation ($V_{bias}<V_{critical}$). Thick-oxide devices are extensively used in applications such as high speed IOs, telecommunication systems, and medical instruments. Most of these applications have the operating voltage from 0-10V or higher, and demand a long lifetime under high stress voltages. To evaluate our

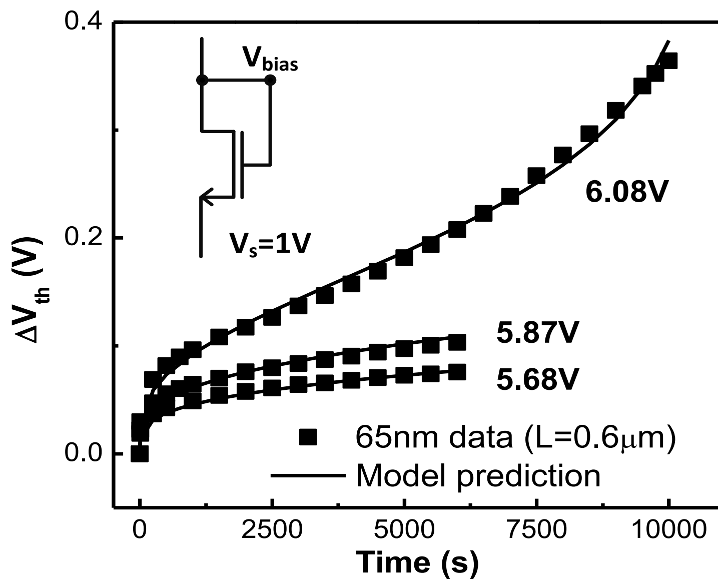


Figure 6.7. Validation of the proposed analysis of bias runaway with 65nm data, at various initial V_{bias}.

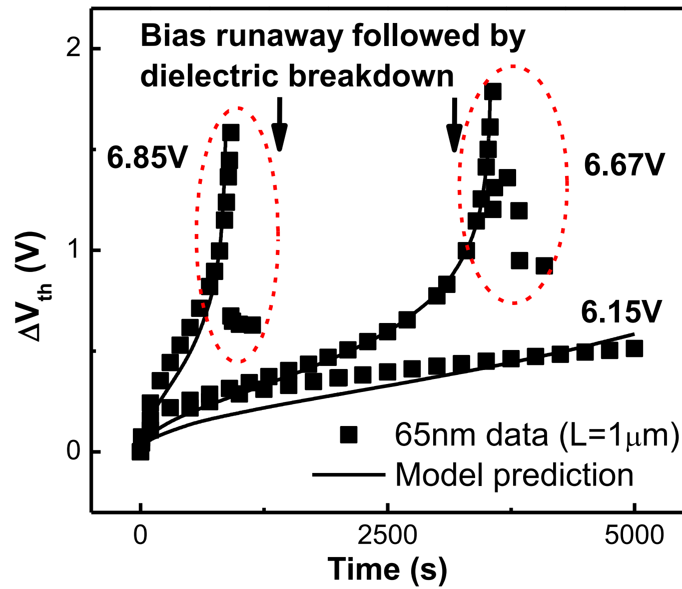


Figure 6.8. Validation of bias runaway with 65nm data for L=1μm, at various initial V_{bias}. Increase in V_{bias} due to bias runaway causes oxide breakdown

analysis of bias runaway in those applications, 65nm thick-oxide IO devices are configured as biasing circuits employed in typical AMS designs for aging test, as shown in Figure 6.7 (inset). All tests are conducted at the room temperature. The source voltage is elevated to emulate a realistic bias design, such as a transistor stack used in cascode configuration. Figure 6.7 presents silicon data with model prediction for device gate length of 0.6μm. It confirms existence of the positive feedback, if V_{bias} is high enough and gradual degradation if V_{bias} is low. Similar positive feedback is observed for gate length of 1.0μm as seen in Figure 6.8. In fact, as bias runaway leads to a rapid increase in both V_{gs} and V_{ds} of the transistor, dielectric breakdown eventually happens, as observed in the silicon measurement. Such catastrophic failure can severely limit lifetime of AMS designs. $V_{critical}$ decreases with shorter gate length, implying an increasing threat as CMOS technology scales.

To investigate the evolution of bias runaway at advanced technology nodes, this work investigates bias runaway at 28nm High-K metal gate. The intrinsic CHC degradation component is extracted based on the method described in chapter 4. As seen in Figure 6.9, the simulation based on calibrated model shows bias runaway behavior at 28nm. However, when the PBTI degradation is combined with intrinsic CHC, bias runaway is absent even for longer time. The main reason is due to lowering of the overall time exponent (n~0.25) of the degradation compared to only CHC (n~0.34). Proposed model and simulation method well capture such aging characteristics, for both gradual and bias runaway conditions helping designers to accurately guard-band their designs.

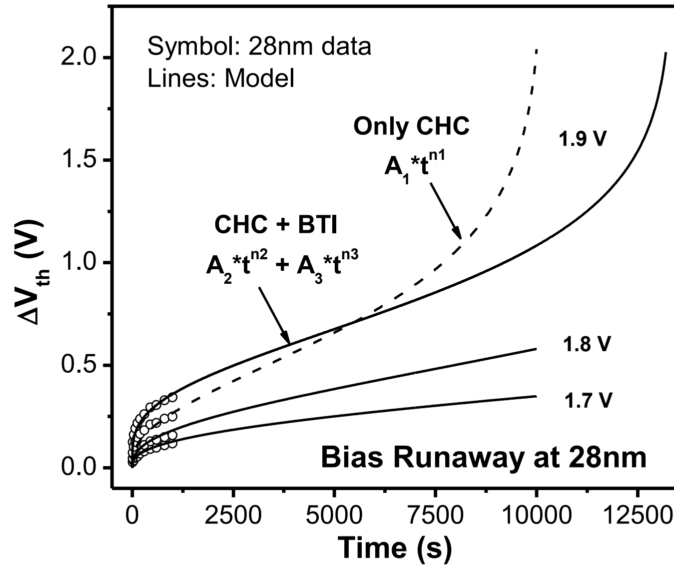


Figure 6.9. The reduction in time exponent due to coupling of PBTI and CHC reduces risk of bias runaway.

6.2.3 Bias Runaway: Circuit Analysis and Design Benchmarking

Finally, based on the aging models and simulation methodology, design solutions to mitigate bias runaway are investigated. The critical boundary equation is also evaluated and verified using the silicon measurements which guides design of reliable biasing circuits. As there is only one transistor involved in this case, a promising solution is by tuning gate length (L) to achieve required performance for given constraints. The study is performed for two representative types of bias circuits that are used extensively in AMS designs:

First topology represents current mode configuration as shown in Figure 6.10 inset, which mirrors I_{bias} to other current branches. This configuration is common in current mode circuits, such as the current amplifier, the current comparator, etc. For reliability perspective, a shorter L is preferred for a fixed I_{bias}. Short channel helps reduce

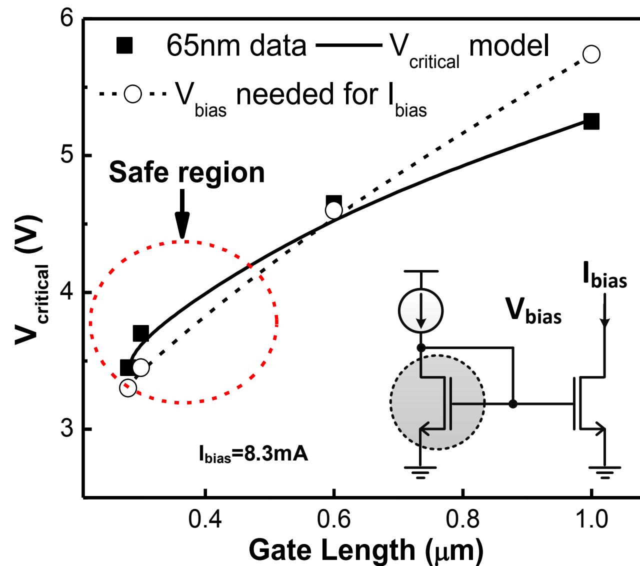


Figure 6.10. Current mode where a shorter length helps reduces V_{bias} and keeps the circuit away from $V_{critical}$ (bias runaway).

V_{bias} and therefore reduces electrical fields, keeping the circuit in the safe region which is immune to bias runaway as demonstrated in Figure 6.10. On the other side, a shorter channel length degrades the intrinsic gain of the device. Moreover, the matching quality between two transistors is poorer with a shorter L and thus, reduces the quality of bias generation and mirroring. Thus there exist a trade-off between lifetime and matching for current mirroring circuits. Based on the system requirement, designers need to identify appropriate channel length to avoid bias runaway. Figure 6.10 also validates the critical boundary equation with silicon measurements at different gate lengths. Second topology is the voltage mode configuration presented in Figure 6.11 inset. In this mode, a device is biased with a current source to produces a constant bias voltage. Channel length and biasing current value can be varied to achieve same bias voltage. Longer L is desirable to reduce I_{bias} and position the device in the safe region. This also provides an added

advantage of less power consumption as I_{bias} is reduced. However, safeguarding requires an area overhead for the design. Similar to current mode, the voltage mode configuration also requires designers to identify the design trade-offs for reliability. Further an amplifier is simulated to demonstrate impact of bias runaway in Figure 6.12.

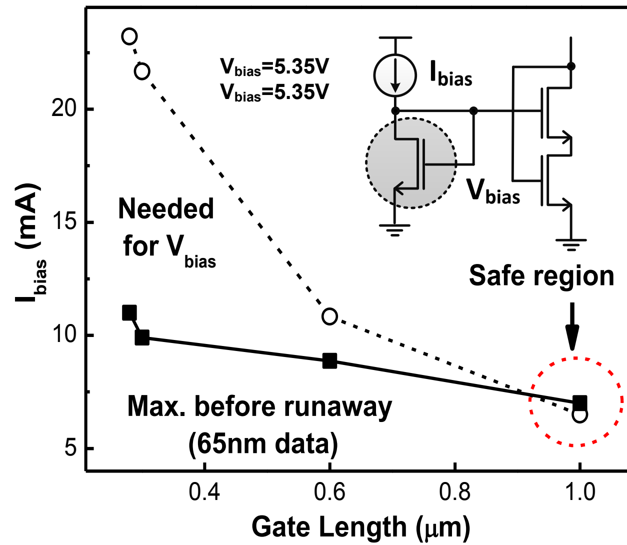


Figure 6.11. Voltage mode where a longer length is required to provide V_{bias} without triggering the runaway.

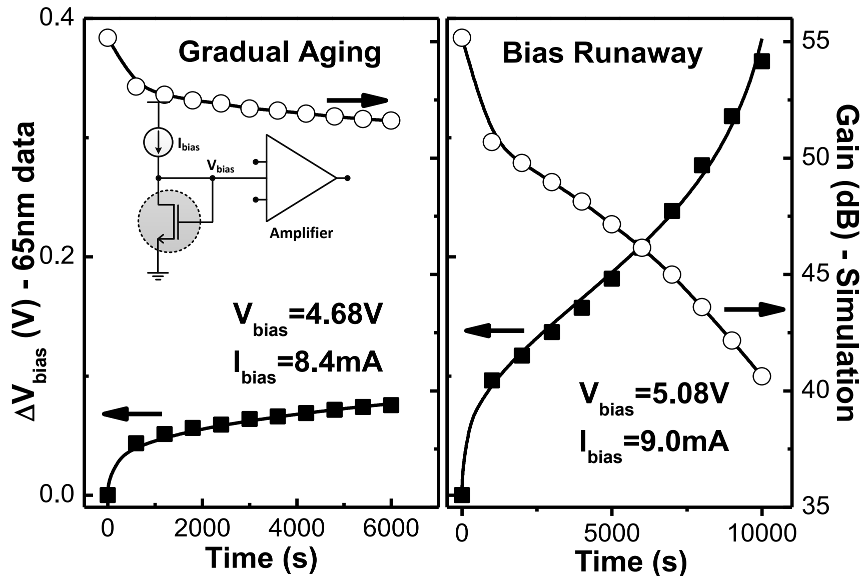


Figure 6.12. Biasing circuit for folded cascode amplifier and difference in degradation due to different biasing.

6.3 Duty Cycle Shift in Logic Circuits

6.3.1 Asymmetric Aging

The aging analysis needs to be performed at the critical instant during circuit operation. At critical moments, the aging effect is prominent and has the maximum impact on circuit performance. One particular instant under the BTI effect happens during the standby mode in digital circuits. For instance, this can be the end of clock gating, when both the logic path and the clock tree have no switching activity, but still experience static stress. The resulted delay shift only occurs at the rising edge of signal switching, but has no impact on the falling edge [22][75]. This phenomenon is called asymmetric aging. For a logic path, it increases path delay, depending on the type, size and number of gates in the path. For a clock tree, it further shifts the duty cycle as shown in Figure 6.13. In today's synchronous design, such behaviors lead to possible timing error and logic failure, including both setup and hold violations.

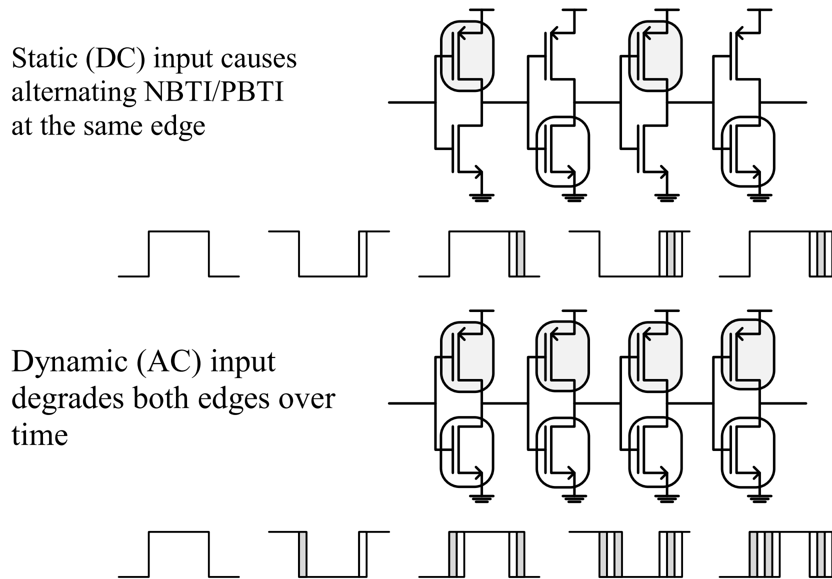


Figure 6.13. Edge shift in static (DC) and dynamic (AC) stress conditions.

6.3.2 *Duty Cycle Shift under Static/Dynamic Aging*

Asymmetric aging causes delay shift to accumulate over a single edge and PBTI makes the situation worse. As explained in Figure 6.13, an inverter chain is stressed in a static (idle) condition where the input is not toggling. This results in alternating DC NBTI and PBTI stress condition. In particular, aging due to PBTI and NBTI is accumulated at the edge from high-to-low transition. This change of a single edge shifts duty cycle. This phenomenon is validated at 65nm in [76] using ring oscillator structures. Accounting for duty cycle degradation is an important aspect for designs relying on both rising and falling edge. Different from static stress, when input of the inverter chain structure is continuously toggling, both edges are impacted by AC BTI stress. Such a behavior helps anneal previous shift in duty cycle and promote the convergence to 50%.

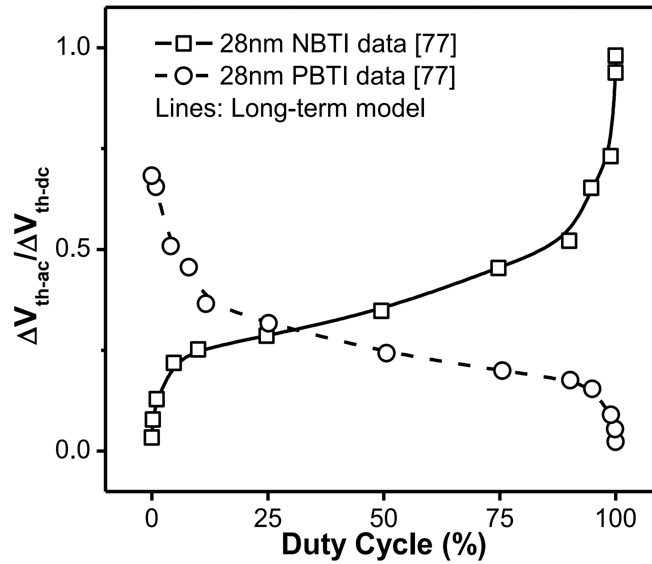


Figure 6.14. Duty cycle dependence of V_{th} shift for NBTI and PBTI at 28nm technology node [77].

Figure 6.14 shows the duty cycle dependence of V_{th} shift for both NBTI and PBTI [77]. V_{th} change is given by the long-term model equation derived in previous chapters based on either RD or TD theory. The number of stages in the clock path affects duty cycle shift. Degradation of duty cycle under static DC stress conditions is a monotonic function as described in Figure 6.15. Thus a longer clock gating scheme will result in higher failure rate. Transition from static to dynamic mode has a significant impact on long-term aging analysis due to the difference in V_{th} shift at different duty cycles for PBTI and NBTI. Dynamic mode after static mode averages duty cycle shift. Figure 6.16 illustrates two different cases where the inverter chain initially suffers different duty cycle shift. As the inverter chain experiences AC stress, the stronger devices are stressed more due duty cycle shift (Figure 6.14) and thereby experience higher V_{th} change. This leads to convergence effect, eventually bringing duty cycle closer to 50%, depending on the relative ratio of NBTI and PBTI.

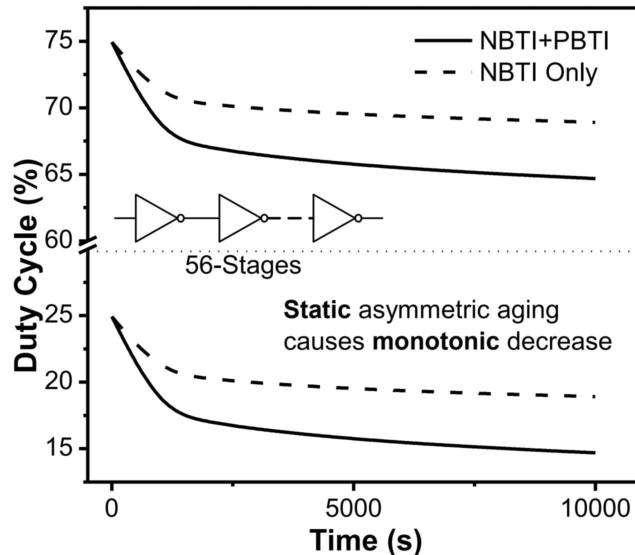


Figure 6.15. Duty cycle degrades monotonically under static (DC) stress condition under BTI.

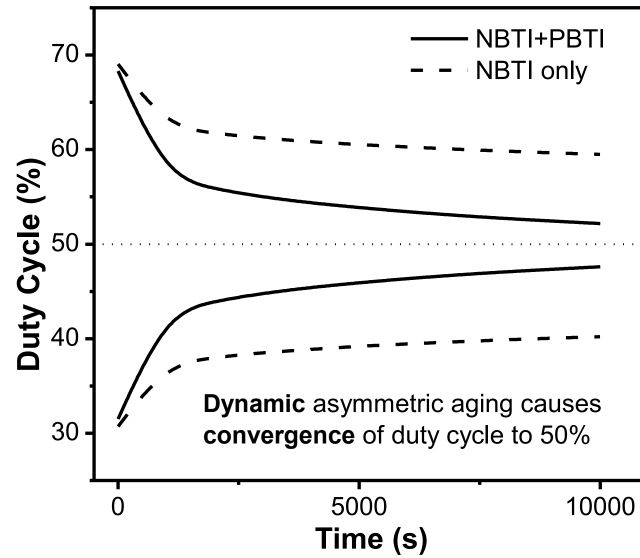


Figure 6.16. Duty cycle converges close to 50% value under dynamic (AC) stress condition.

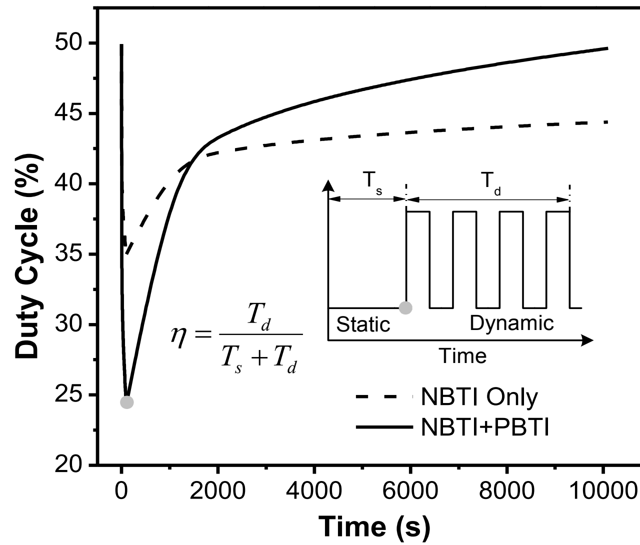


Figure 6.17. Comprehensive picture of duty cycle degradation under periodical DC and AC stress. The addition of PBTI speeds up the convergence rate.

Figure 6.17 show a complete representation of duty cycles shift when inverter chain is subjected to a cycle of static and dynamic stress. As a result of DC stress, the duty cycle reduces from the initial value of 50%. Dynamic operating mode helps recover duty cycle close to the initial value, depending on AC stress time. A parameter η is

defined as a ratio of DC and AC stress time in one cycle, as shown in the inset of Figure 6.17. For η close to 0.1, DC stress dominates over AC stress (Figure 6.18(a)). As a result, duty cycle cannot converge. Under this condition, clock path experiences a larger change in duty cycle and more functional failure. Thus a longer clock gating scheme does not favor long-term reliability. On the other hand, if η is close to 0.9 as shown in Figure 6.18(b), AC stress component dominates and thus, helps duty cycle to converge close to 50% value. This ensures correct functionality of latch based circuits, at the price of less clock gating and more power consumption.

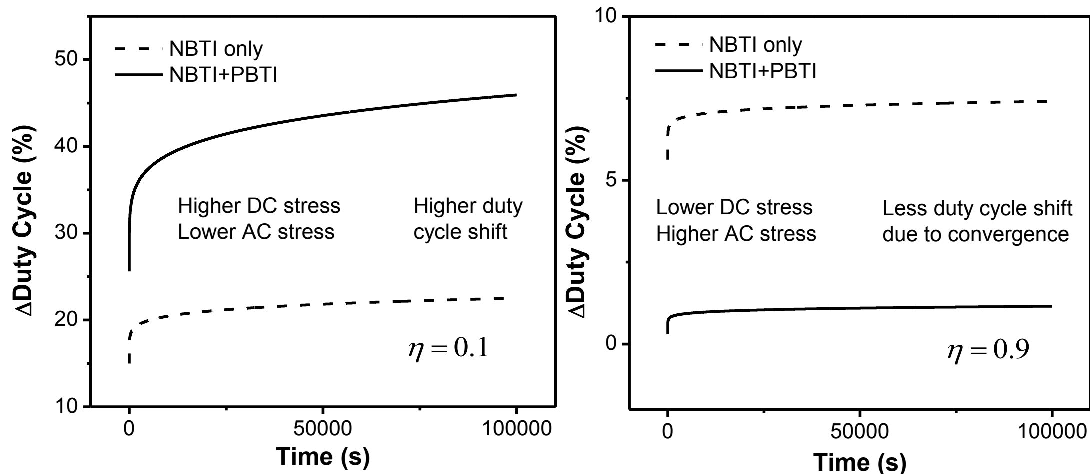


Figure 6.18. The impact of ratio-η between static (DC) and dynamic (AC) stress: (a) For $\eta \sim 0.1$, DC stress dominates causing higher shift in duty cycle and more severe asymmetric aging; (b) For $\eta \sim 0.9$, AC stress allows duty cycle to converge causing less functional failure due to asymmetric aging.

CHAPTER 7

SUMMARY AND FURTURE WORK

7.1 Thesis Conclusions

This work presents a comprehensive solution needed for accurate and efficient aging analysis in scaled CMOS circuits. To accomplish this, a complete suite of static, dynamic and long-term aging models based on RD theory are proposed along with TD theory. Novel simulation tool for aging analysis of AMS designs is proposed eliminating limitation of existing commercial tools. Based on new models and tools, unique critical failure conditions are identified in AMS and digital circuits. This work helps designers to accurately guard-band/design for required lifetime.

- Chapter 1 gives an overview of aging at device level and its impact on circuit performance along with technology scaling. It highlights the essential needs for reliability analysis in scaled CMOS designs.
- Chapter 2 presents the degradation models for BTI using Reaction-Diffusion theory which can predict V_{th} shift under any input stress conditions. The new proposed models are comprehensively validated with device and circuit level silicon data for at 45nm technology node. Novel random input models based on RD theory accurately predicts V_{th} shift under any conditions including the non-monotonic behavior under DVS.
- Chapter 3 presents the need for charge trapping/detrapping theory and summarizes TD based compact models for all operating conditions. Aging statistics are demonstrated in this chapter. Efficient technique to accurately extract model parameters for both RD and TD is also presented. Finally RD

and TD principles are combined to improve prediction accuracy of compact aging models. This is validated with 45nm and 65nm silicon data.

- Chapter 4 proposes new model for channel hot carrier. Advance technology nodes shows e-e scattering causes to shift in worst case condition at $V_{gs}=V_{ds}$. Due to this condition, the biasing circuits that are widely used in AMS circuits is affected. The model is well validated by 65nm silicon data. Further, this chapter exhibits a preliminary de-coupling method to for PBTI and CHC at 28nm HK-MG technology node. Proposed BTI and CHC models are validated at 28nm for different stress conditions.
- Chapter 5 implements the compact aging models in circuit simulation environment. Silicon data at circuit level matches the aging prediction for 45nm digital RO under DVS and 90nm CMOS single ended LNA.
- Chapter 6 proposes new iteration based simulation tool for AMS lifetime estimation. Leveraging BTI and CHC aging models, critical circuit failure conditions such as Bias Runaway and Duty Cycle shift are identified and validated with silicon data. Boundary condition for bias runaway is derived helping designers to properly guard-band designs.

7.2 Future Work

Bias Temperature Instability (BTI):

Empirical and simplistic results by combining RD and TD theory are proposed in this work. Detailed analysis can be done to physically derive the final equation for a comprehensive unified model improving prediction capability. This will be particularly helpful for design guard-banding under DVS and random input stress conditions.

Positive Bias Temperature Instability (PBTI) + Channel Hot Carrier (CHC):

With technology advancement (below 28nm and High-K Metal gates), PBTI concerns have increase along with CHC especially for NMOS devices. Typical device testing techniques for CHC at 28nm High-K and below will present convoluted results from PBTI and CHC. An empirical method is demonstrated in this work which can be further expanded by including the V_{ds} dependence for CHC aging. Temperature and BTI recovery can be used as de-coupling parameters apart from drain voltage.

Early Life Failure (ELF):

Early life failures are eliminated by traditional Burn-In process. However, due to thermal runaway, this technique is no longer reliable. There is a dire need to identify infant mortality as soon as possible. There is a possibility to leverage positive feedback (similar to bias runaway) for a fast screening method. In this technique, power supply can be adaptively tuned to keep a given performance metric (frequency, delay etc.) constant.

7.3 Tape-Outs

In order to have a solid verification of Long-term models, we have undertaken several tape-outs. The technology nodes are:

1.) IBM9SF: 90nm
2.) IBM32SOI: 32nm SOI
3.) IBM10LP: 65nm
4.) 28nm High-K Metal gate

These tape-outs will enable verification of aging models by gathering experimental results from the silicon itself at device and circuit level and thus making aging models more accurate. Tape-out will also aid in identification of bias runaway and similar behavior at circuit level. It will also help us validate the simulation methodology for faster prediction of ELF failures. These chips contains

1.) Discrete devices for different channel length and widths.
2.) Inverter based ring oscillators.
3.) Reference VCO to enable differential measurements to eliminate noise for peripheral circuits and substrate noise.
4.) Amplifiers, band-bap references and different analog components to characterize aging.

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