New Model for Simulating Impact of Negative Bias Temperature Instability (NBTI) in CMOS Circuits

by

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ABSTRACT

Negative Bias Temperature Instability (NBTI) is commonly seen in p-channel transistors under negative gate voltages at an elevated temperature. The interface traps, oxide traps and NBTI mechanisms are discussed and their effect on circuit degradation and results are discussed. This thesis focuses on developing a model for simulating impact of NBTI effects at circuit level. The model mimics the effects of degradation caused by the defects.

The NBTI model developed in this work is validated and sanity checked by using the simulation data from silvaco and gives excellent results. Furthermore the susceptibility of CMOS circuits such as the CMOS inverter, and a ring oscillator to NBTI is investigated. The results show that the oscillation frequency of a ring oscillator decreases and the SET pulse broadens with the NBTI.

Dedicated to my parents

Murali Padala and Rajeswari Padala

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LIST OF ABBREVIATIONS

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
nMOSFET	n-channel MOSFET
pMOSFET	p-channel MOSFET
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
BTI	Bias Temperature Instability
CMOS	Complementary Metal–Oxide–Semiconductor
PMOS	p-Channel Metal-Oxide-Semiconductor
NMOS	n-Channel Metal-Oxide-Semiconductor
D_{it}	Density of Interface Traps
N_{ot}	Density of Oxide Traps
DOS	Density of States
BTS	Bias Temperature Stress
TCAD	Technology Computer Aided Design
SET	Single Event Transient

CHAPTER 1

INTRODUCTION

Negative-bias temperature instability (NBTI) is a main reliability issue in MOSFETs. The NBTI effect is more seen in a p-channel MOSFET when stressed with negative gate voltages at elevated temperatures. The NBTI causes the absolute value of threshold voltage to increase and consequent decrease in drain current and decrease of other important parameters like trans-conductance, channel mobility of a MOSFET. The same effects can be seen in n-channel MOSFET's too but the degradation is very less compared to that of a p-channel MOSFET. Therefore it is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage like in an inverter and ring oscillator.

There are two main types of traps which contribute to NBTI:

- Interface traps: These traps cannot be recovered over a reasonable time of operation. In the case of NBTI, it is believed that the Si–H bonds located at the silicon-silicon dioxide interface are broken when interacted with the protons coming from substrate [42]. The dangling bonds contribute to the threshold voltage degradation.
- Oxide traps: When gate stress is applied, some holes are pulled into the oxide from channel of PMOS. These traps can be emptied when the stress voltage is removed. The threshold voltage degradation can be recovered over time.

A new model to simulate the circuit level degradation subjected to negative bias temperature instability (NBTI) has been developed in this thesis work. A very basic

fundamental ring oscillator circuit is studied to evaluate the impact of NBTI on CMOS digital circuit performances.

The change in threshold voltage is modeled as a defect potential and is applied at gate. The defects dependence on time and gate voltage is modeled in the defect potential.

CHAPTER 2

OVERVIEW OF THE DEFECTS

Before even discussing about the defects, let us discuss about the basic MOSFET operation like the channel formation, regions of operation and the threshold voltage.

2.1 MOSFET ANALYSIS

2.1.1 The Basic MOSFET Operation

A metal–oxide–semiconductor field-effect transistor (MOSFET) is basically a device which controls and modulates the charge by a capacitance between a body terminal and a gate terminal. The gate of the MOSFET is located on the top of the body substrate and it is insulated from other regions by a field oxide, such as silicon dioxide. The body of the MOSFET is generally doped by silicon. The p-channel MOSFET substrate is doped by n-silicon, whereas the n-channel MOSFET substrate is doped by p-silicon. The silicon surface and gate terminal acts like two terminals of the capacitance and the dielectric is silicon dioxide [12].

In nMOSFET, the source and drain regions are "n+" type and the body substrate is "p" type silicon as shown in Figure 1. In the case of a pMOSFET, the source and drain are "p+" regions and the body is an "n" region. In pMOSFET, the source and drain regions are “p” type and body substrate is “n” type silicon.

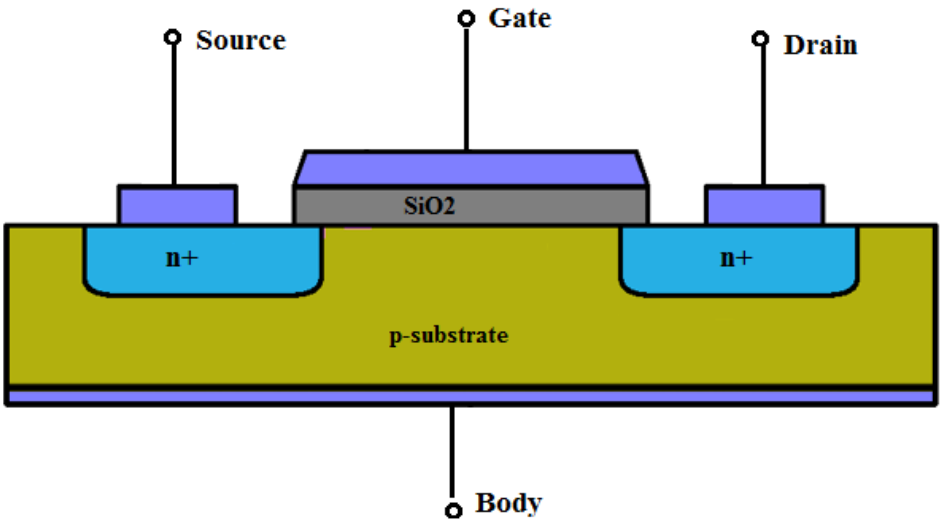


Figure 1: Basic p-MOSFET Structure

Let us see how a channel is formed in an nMOSFET. The same theory applies to pMOSFETs.

In nMOSFET, the substrate is “p” type where holes are the majority carriers. When a positive voltage is applied to the gate, it repels the positively charged holes away from the substrate. A depletion region is formed when the holes move further deep into the substrate. When the positive voltage is applied at the gate, it attracts electrons from the source and drain which are “n+” regions and have excess of electrons, into the channel region. As the number of electrons accumulate near the surface of the Si-SiO_2, an n region is in created, connecting the source and drain regions as shown in Figure 2. If a voltage is now applied at the drain of the MOSFET, current starts flowing through this channel. Thus a channel is formed between drain and source and current flows in a MOSFET [13].

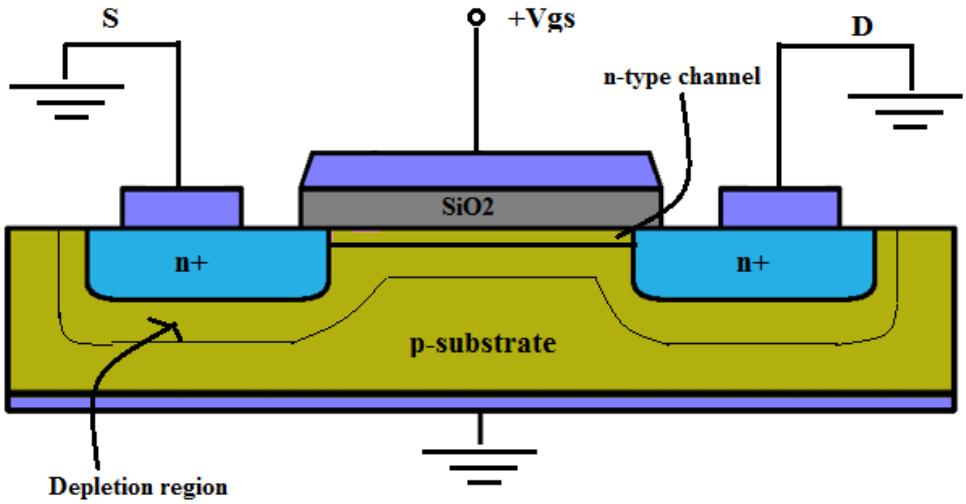


Figure 2: Channel Formation in p-Substrate

2.1.2 MOSFET Region of Operations

The MOSFET operates in different regions depending on the gate voltage.

Cutoff, Sub threshold, or weak inversion mode:

When $V_{GS} < V_{th}$,

In this region, the transistor is turned off, and there is no current flowing between drain and source. But there is a weak sub threshold current which is exponentially dependent on the gate source voltage [12].

$$I_D = I_{D0} e^{\frac{(V_{GS} - V_{th})}{nV_T}} \quad (1)$$

Where I_{D0} = current at $V_{GS} = V_{th}$, the thermal voltage $V_T = kT/q$ and the slope factor n is given by

$$n=1+\frac{C_D}{C_{ox}} \quad (2)$$

Where C_D = capacitance of the depletion layer and C_{ox} = capacitance of the oxide layer. This equation is generally used, but is only an adequate approximation for the source is connected to the body.

Triode mode or linear region:

$$\text{When } V_{GS} > V_{th},\ V_{DS} < V_{GS} - V_{th}$$

In this region the transistor is turned on, and a channel has been formed allowing the current to flow from drain to source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages.

The drain current is,

$$I_{ds} = \mu C_{ox}\frac{W}{L_{eff}}(V_{gs} - V_{th} - \frac{V_{ds}}{2})(1 + \lambda V_{ds}) \quad (3)$$

Where μ is the effective mobility, W is the width of the device, L_{eff} is the effective gate length and λ is the channel length modulation parameter.

In Saturation region, where

$$V_{gs} > V_{th} \text{ and } V_{ds} > V_{gs} - V_{th}$$

The transistor is turned on, and a channel has been created, which allows current to flow between the drain and source [12].

The drain current is,

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L_{eff}}(V_{gs} - V_{th})^2\ (1 + \lambda V_{ds}) \quad (4)$$

The threshold voltage of a MOSFET is given by the equation (5)

$$V_{th} = V_{To} + \gamma(\sqrt{2\phi_B - V_{BS}} - \sqrt{2\phi_B}) + \frac{Q_{it}+Q_{ox}}{C_{ox}} \quad (5)$$

Where V_{To} is the threshold voltage when $V_{BS} = 0$, C_{ox} is the capacitance per unit area of the oxide, Q_{it} is the interface charge, Q_{ox} is the oxide charge and γ is the body-effect parameter, defined as

$$\gamma = \frac{\sqrt{2\varepsilon_s q_o N_A}}{C_{ox}} \quad (6)$$

Here, ε_s is the permittivity of the silicon substrate and N_A the acceptor doping concentration. The potential in the neutral p-type region ϕ_B is evaluated as

$$\phi_B = \frac{KT}{q} \ln \frac{N_A}{n_i} \quad (7)$$

During NBTI, the interface defects and oxide traps will be formed which degrades the performance of the transistor and the threshold voltage is shifted by ΔV_{th} obtained from (5)

2.1.3 Interface and Oxide Charges

The threshold voltage shift (ΔV_{th}) is contributed mainly because of the changes in interface and oxide charges (ΔQ_{it} and ΔQ_{ox}) and is given by,

$$\Delta V_{th} = \frac{\Delta Q_{it} + \Delta Q_{ox}}{C_{ox}} \quad (8)$$

In the context of NBTI interface charges are usually the result of charged interface defects D_{it}. The interface charge depends on the Fermi-level E_F and the trap occupancy *f* and can be calculated as [43]

$$Q_{it} = q\int_{E_v}^{E_c} D_{it}(E) f(E_f, E) dE . \quad (9)$$

Charged oxide traps D_{ox} contribute to the threshold voltage shift depending on their position in the dielectric. The resulting, effective, Q_{ox} can be evaluated as

$$Q_{ot} = q\int_0^{t_{ox}} \rho(x)\frac{x}{t_{ox}} dx , \quad (9)$$

where t_{ox} is the oxide thickness.

2.1.4 NBTI Related Models

The important parameter which changes because of NBTI is the trans-conductance (g_m). As the drain current changes with the trapped charges, so does the trans-conductance.

$$g_m = \frac{\Delta I_d}{\Delta V_g} \quad (11)$$

Devine et al. proposed a trans-conductance shift versus interface trap (N_{it}), relation as [45]

$$\Delta g_m = g_{mo} \frac{\alpha N_{it}}{1+ \alpha N_{it}} \quad (12)$$

Where α is a processing related parameter.

The mobility model proposed by Devine et al. [45] is

$$\mu = \frac{\mu_o}{1+ \alpha N_{it}} \quad (13)$$

Therefore the mobility and trans-conductance decreases with increase in the interface traps. The NBTI also increase the threshold voltage. Decrease in carrier mobility and

trans-conductance and increase in absolute value threshold voltage leads to the reduction of drain current and the performance of the transistor is degraded [20].

2.2 The Silicon/Silicon Dioxide Interface

One of the most important things that led to the enormous success and continuous improvement of the CMOS technology are the excellent properties of the thermally grown Si/SiO_2 interface.

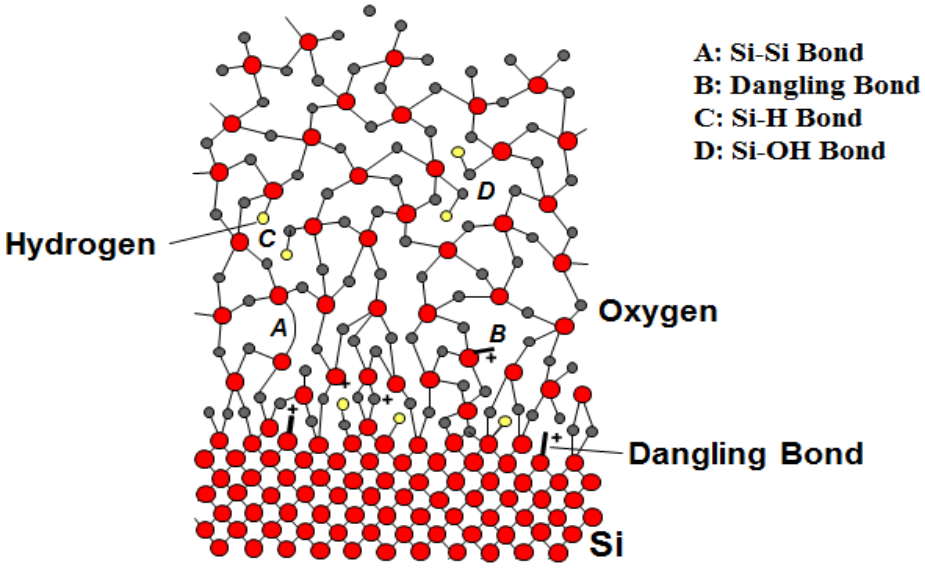


Figure 3: Si-SiO2 Interface and Oxide Defect Structure [53]

Silicon dioxide (SiO_2) is formed when the silicon surface is exposed to oxygen. This process is called oxidation. Silicon dioxide is a very good electrical insulator and hence we use it for the electrical isolation of the devices, and also as a component in MOS transistors. It acts like a dielectric in the MOS capacitance, the two plates being

the gate and body electrodes. Figure 3 shows the Si/SiO_2 interface and various types of bonds that exist at the interface and in the oxide.

2.2.1 Silicon Dangling Bonds

The silicon atom has four valence electrons and hence it wants to bond with four atoms to be stable. In the silicon crystal each silicon atom bonds with four other silicon atoms but at the surface there are no silicon atoms to bond with and hence traps are formed as shown in Figure 4. The density of these interface states, D_{it} is approximately 10^{14} cm^{-2} eV^{-1}. When the silicon surface is oxidized, some of the silicon atoms at the surface are bonded with the oxygen atoms as shown in Figure 5. The density of interface traps then reduces a bit and is approximately $D_{it} = 10^{12}$ $cm^{-2}eV^{-1}$ [46].

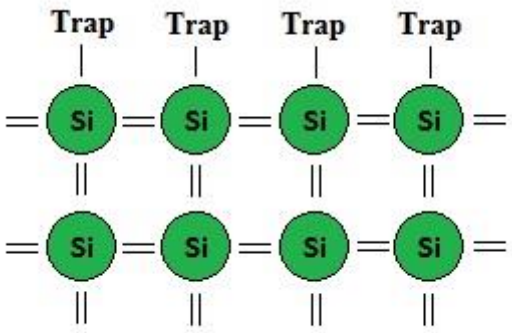


Figure 4: The Valence Electrons Forms Active Interface Traps at the Surface.

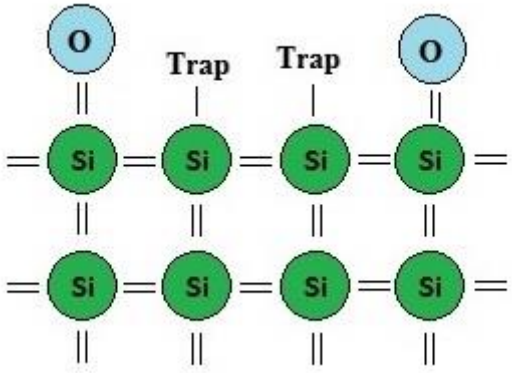


Figure 5: The Interface Traps are Reduced After Oxidation.

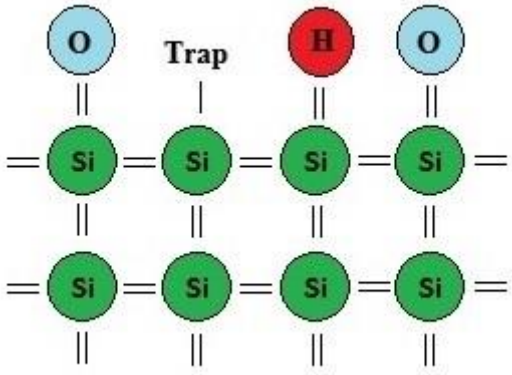


Figure 6: The Interface Traps are More Suppressed After Hydrogen Passivation.

There can still be a lot of defects present which causes the circuit degradation. So it is very important that the defects need to be reduces and passivated at the interface in a transistor. The interface traps causes degradation of transistor parameters like the threshold voltage, the trans-conductance, the on-current, and the carrier mobility at device level and increases the delay time at circuit level. These interface traps can be reduced more by annealing the surface with hydrogen gas. The remaining silicon dangling bonds react with hydrogen forming Si-H bonds and thus the defects are reduced to more extent. After the hydrogen passivation the density of interface defects

can be reduced to around $D_{it} = 10^{10}$ $cm^{-2}eV^{-1}$ [46]. These Si-H bonds can break at high temperatures or with the negative gate stress, forming interface traps [22] as discussed in the further sections.

2.2.2 Oxide Traps

Oxygen vacancies are the major hole trapping mechanisms. Because of the manufacturing defects, oxygen vacancies are formed in the oxide which traps the positively charged holes. When the Si-H bonds break with the gate stress or at high temperatures, the hydrogen atoms diffuse into the oxide and holes can be trapped [22]. When the gate stress is applied, there will be an electric field in vertical direction which causes the holes to be trapped. The threshold voltage is degraded because of the charge accumulated by these holes in the oxide. When the stress is removed, the oxide traps will be annealed and the threshold voltage can be annealed up to some extent.

The mechanisms for the formation of interface traps and oxide traps are discussed in the further sections.

2.2.3 Oxide Charges/Interface Traps

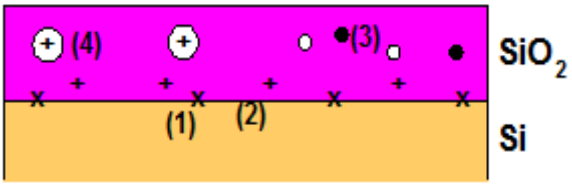


Figure 7: Oxide Charges and the Interface Traps [53]

Table 1 gives more details like the causes and effects of the oxide charges and interface traps which were shown in Figure 7.

Table 1: Oxide Charges/Interface Traps [53]

Charge	Type	Location	Cause	Effect on Devices
(1) $D_{it}(cm^{-}2eV^{-1})$, N_{it}, Q_{it}	Interface Trap Charge	SiO_2/Si Interface	Dangling Bonds	Junction Leakage Current Noise, Threshold Voltage Shift, Sub Threshold Slope
(2) N_f, Q_f cm^{-2}, C/cm^2	Fixed Charge	Close to SiO_2/Si Interface	Si^+	Threshold Voltage Shift
(3) N_{ot}, Q_{ot}	Oxide Trapped Charge	In SiO_2	Trapped Electrons and Holes	Threshold Voltage Shift
N_m, Q_m	Mobile Charge	In SiO_2	Na, K, Li	Threshold Voltage Shift

In this work, only interface trap charges and oxide trap charges are considered and their time dependence and gate voltage dependence are modeled to simulate the impact of NBTI at circuit level.

CHAPTER 3

NEGATIVE BIAS TEMPERATURE INSTABILITY (NBTI)

Bias temperature instability (BTI) is a degradation phenomenon affecting mainly MOS field effect transistors. The highest impact is observed in p-MOSFETs. Either Negative voltages or high temperatures can cause NBTI, but a faster and stronger effect is produced with negative stress and high temperature together. The stress conditions for this negative bias temperature instability (NBTI) typically lie below 6MV/cm for the gate oxide electric field and temperatures ranging 100-250 ˚C. A very interesting thing about NBTI is its capability to anneal to a certain extent when the stress is removed [18].

The important transistor parameters which degrade because of NBTI are:

- Trans-conductance (g_m) decreases
- Linear drain current and saturation current (I_{dsat}) decreases
- Channel mobility (μ_{eff}) decreases
- Sub-threshold slope (S) decreases
- Absolute value of the threshold voltage (V_{th}) increases

At the circuit level the switching speeds are reduced and the delay times are increased as the charging time for load capacitances or the parasitic capacitances are increased.

The NBTI is first reported many years ago [49], but gained much attention in recent years [3, 11, 18, 48] due to modern semiconductor technologies.

The following aspects are the main factors that lead to the increasing NBTI [20]:

- higher oxide electric fields due to oxide scaling
- higher temperatures due to higher power dissipation
- high performance IC's during routine operation

3.1 Physical Mechanisms of NBTI

The negative bias temperature instability (NBTI) effect has been reported many years ago by several groups [49, 50, 51], there is still a lot to understand the exact mechanisms behind the NBTI degradation. The general theory says that when MOSFETs are stressed with a gate voltage at an elevated temperature, charge builds up because of the interface traps and the oxide traps at the interface and oxide respectively. This charge leads to degradation of the transistor performance [20]. PMOS transistors are more susceptible to the degradation as they always operate with negative gate source voltage.

3.1.1 Reaction Diffusion Model

The reaction-diffusion (R-D) model is been proposed by several groups [7, 8, 9] states that when a p-MOSFET is in strong inversion, the holes in the inversion layer reacts with Si-H bonds at the Si-SiO_2 interface and weakens the bonds. At high temperatures, these Hydrogen bonds dissociate forming active interface traps (N_{it}). Initially the generation rate of interface traps depends on the dissociation of the Si-H bonds. This process is reaction. Later the generation of interface traps depends on the

diffusion of hydrogen atoms. This is the diffusion step [22]. Figure 8 shows the reaction diffusion model for NBTI.

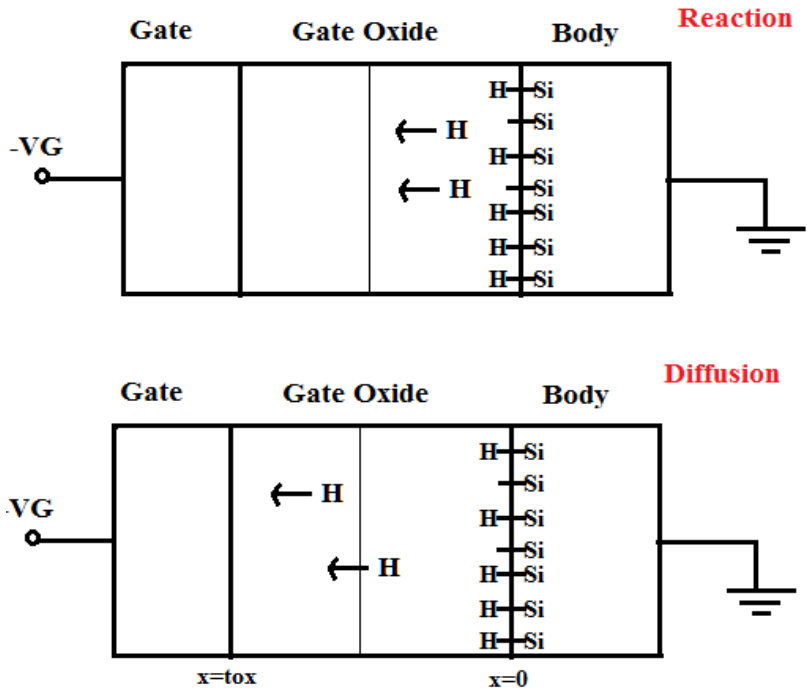


Figure 8: Reaction-Diffusion Model

$$\frac{dN_{it}}{dt} = K_f(N_{Si\text{-}H} - N_{it}) - K_r N_{it} N_H(x=0) \quad (14)$$

Where K_f, K_r, $N_{Si\text{-}H}$ and $N_H(x=0)$ are bond-breaking rate, hydrogen annealing rate, Si-H density before stress and hydrogen density at the interface respectively [22].

3.1.2 Hydrogen Model

The hydrogen atoms from the Si substrate migrate to the Si/SiO_2 interface. These hydrogen atoms are produced when the Phosphorous-Hydrogen bonds (n-

substrate) or the Boron-Hydrogen bonds (p-substrate) break. The hydrogen atoms when migrating towards are the interface traps a hole and becomes H^+. The positive hydrogen atoms depassivate the Si-H bonds at the Si/SiO_2 interface forming H_2 and an interface trap [42] as shown in Figure 9. In the process, some H^+ can go into the oxide, hence forming oxide traps (N_{ot}).

$$Si_3{\equiv}Si\text{-}H + H^+ = Si_3{\equiv}Si\bullet + H_2 \quad (15)$$

Si• is a dangling bond.

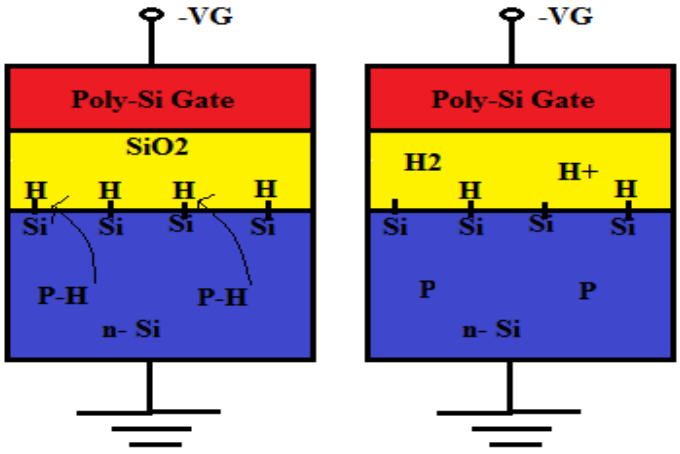


Figure 9: Hydrogen Model [18]

When the stress is removed the H_2 can passivate the dangling bonds and the degradation is reduced.

3.1.3 Experimental Setup for NBTI

The gate is biased with a negative voltage, while the drain, source, and bulk are grounded.

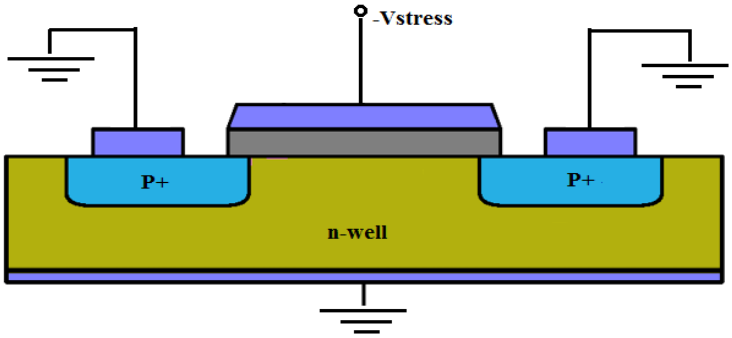


Figure 10: The Setup for NBTI Experiment.

The set-up for the negative bias temperature instability (NBTI) at a device level is shown in Figure 10. The bulk of the transistor is grounded. The source and drain contacts are also grounded. A negative gate voltage stress is applied to the gate at elevated temperatures, typically ranging between 100 and 250 ˚C, for a certain period of time. To measure the degradation, the threshold voltage can be measured by plotting the drain current with respect to source gate voltage.

3.2 How p-MOSFET are different from n-MOSFET

NBTI is observed both in PMOS and NMOS transistors; however PMOS shows more degradation in their performance compared to the NMOS. Figure 11, presenting data from Huard et al. [3], shows that the threshold voltage degradation is more in PMOS transistors with negative gate voltage stress. When a positive gate voltage is applied to PMOS, the degradation is very less compared to that of negative voltage stress and also the effects in NMOS transistors for both positive and negative voltage are less too.

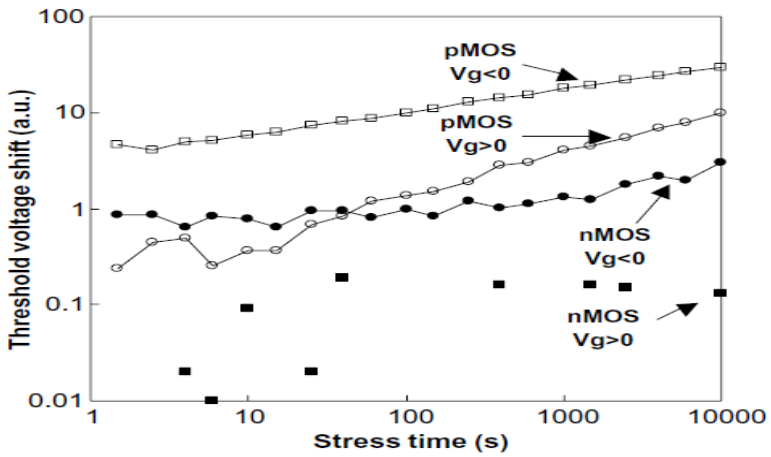


Figure 11: BTI in PMOS and NMOS Transistors [3].

In the next sections we will discuss the other possible reasons for the different degradation performance in PMOS and NMOS transistors.

3.2.1 Occupancy of Interface Traps

A donor trap can be either positive or neutral. A donor trap is positively charged when empty and neutral when filled. An acceptor trap can be either negative or neutral. An acceptor trap is neutral when empty and negatively charged when filled. The donor traps usually lie near the valence band and the acceptor traps usually lie near the conduction band. Figure 12 shows the polarities of the interface trap charge in both PMOS and NMOS transistors. The lines are the energy states of interface traps and the solid ones are filled energy states. The charge state of the interface traps depends on the Fermi level. All the energy states below the Fermi level are filled. The charge polarity of the interface traps at the Si/SiO_2 interface in inversion is important as the threshold voltage depends on this charge [10].

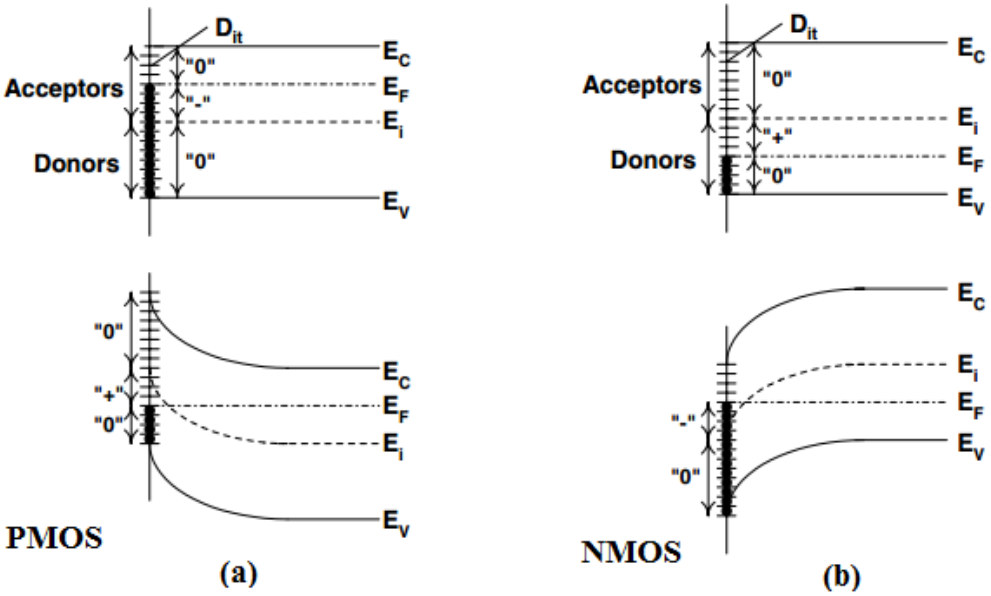


Figure12: Band Diagram Showing the Polarities of Interface States. (a) n- Substrate at Flat Band and in Inversion. (b) p-Substrate at Flat Band and in Inversion. [10]

In the case of a PMOS, it's an n substrate. At flat band the acceptor traps are filled and hence it's negatively charged. In inversion, the Fermi level is below the intrinsic energy level and hence the donor traps are empty which means it is positively charged as shown in Figure 12(a). Hence for an n-substrate in inversion, the charge because of interface traps is positive [10].

$$Q_{Dit} = + Q_{it} \tag{16}$$

In the case of an NMOS the situation is different. Figure 12(b) shows the energy diagram of an NMOS in flat band and in inversion. At the flat band, the donor traps are empty and hence it is positively charged but in inversion, the Fermi level is above the intrinsic energy level. So the acceptor traps are filled and hence negatively charged. Hence in inversion the net charge because of interface traps for p-substrate is negative [10].

$$Q_{Dit} = - Q_{it} \quad (17)$$

The Oxide traps are mainly because of the holes getting trapped in the oxide. In both NMOS and PMOS the mechanism is the same that is the hole gets trapped in oxide and hence it is positively charged in both cases. Therefore the charge contribution because of oxide traps is almost same in both PMOS and NMOS and it is positive.

$$Q_{Not} = + Q_{ot} \quad (18)$$

So when we add the net charge contributions caused by interface traps and oxide traps for PMOS and NMOS, we get

$$Q_{total} = Q_{Dit} + Q_{Not} \quad (19)$$

For PMOS,

$$Q_{total} = Q_{it} + Q_{ot} \quad (20)$$

For NMOS,

$$Q_{total} = - Q_{it} + Q_{ot} \quad (21)$$

In PMOS, the interface traps and the oxide traps contribute to the threshold voltage shift whereas in NMOS the interface traps reduces the shift caused by the oxide traps and the effect of NBTI is therefore less seen in NMOS compared to PMOS devices.

3.2.2 Breaking of Si-H Bonds

Tsetseris et al. [42] proposed a model explaining the different degradation behavior in p-MOSFETs and n-MOSFETs. The positively charged hydrogen or

proton, H^+ is responsible for the breaking of Si-H bonds at the interface. The hydrogen is originated from the phosphorous-hydrogen bonds in the n-substrate in the case of a p-MOSFET. The hydrogen atom then picks up a hole to form H^+ and then reacts with the Si-H bond at the interface to form H_2 and leaved behind a silicon dangling bond which is an interface trap and the H_2 diffuses into the oxide as shown in Figure 13.

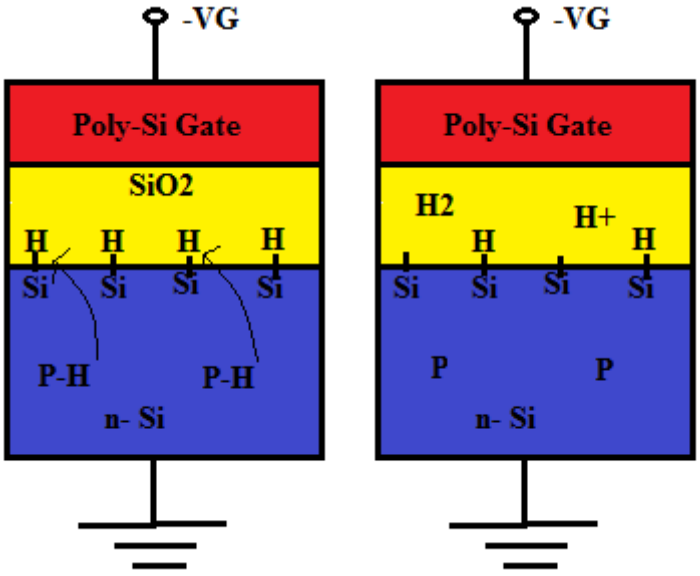


Figure 13: Interface Trap Creation Due to Hydrogen [10]

When the stress is removed, the H_2 can diffuse back to the interface and hence passivate the silicon dangling bond.

The activation energy for dissociation of P-H bonds is usually high. The bonds can be broken only in the depletion region. During negative bias stress a p-MOSFET is in strong inversion and a depletion region is formed in the substrate. Hydrogen atoms can break and cause degradation at the interface. But when there is a positive stress depletion region is not formed. Therefore the protons are not available from the P-H bonds, and the interface traps are not formed.

In the n-MOSFET the substrate is doped with boron and it is more difficult to break the boron-hydrogen bonds as their binding energy is much higher.

3.2.3 Surface potential-gate voltage behavior

The different degradation behavior of p- and n-channel MOSFETs can be because the gate voltages can be different for a given oxide electric field [18].

The Fermi-level of a p-type poly gate lies approximately at the valence band edge $E_F = E_V$ while the Fermi-level of an n-type poly gate is located at the conduction band edge energy $E_F = E_C$. For NBT stress the p-type poly gate of the p-channel device is depleted while the n-type poly gate of the n-channel device is driven into accumulation.

Oxide and interface charges generated by NBTI degradation further shift the relevant gate voltages.

This asymmetry in n-type and p-type gate contacts, the oxide electric fields are not the same for a given gate voltage and at a given oxide electric field the gate voltages are different. This effect has to be accounted while comparing between p-channel MOSFET's and n-channel MOSFET's [20].

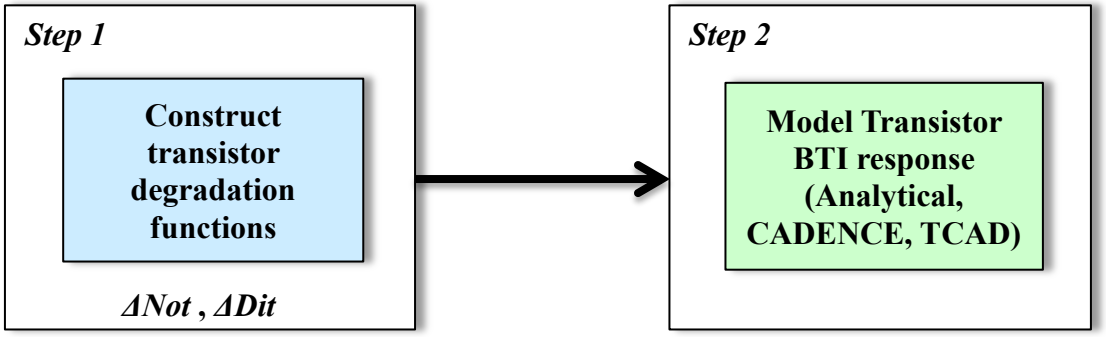
CHAPTER 4

MODELING OF NBTI

As we have discussed in previous sections, charge build up with the defects and which degrades the threshold voltage of the transistor. A model has been developed for simulating impact of Negative Bias Temperature Instability (NBTI) at circuit level.

4.1 Modelling the defects in a PMOS transistor

If ΔN_{ot} and ΔD_{it} are able to be measured experimentally as a function of bias stress and time, their effects be simulated in Cadence at the circuit level



The approach is to utilize external voltages (ΔV) in series with the transistor gate stimulus that mimic effects of time and bias dependent defects.

The degradation model is developed using the drain current equation in the sub threshold region. The sub threshold model works for strong inversion too with slight modifications.

$$I_{D,pre} \propto \exp\left(\frac{V_{SG} - V_{t,pre}}{m\phi_t}\right) \tag{22}$$

$$I_{D,pst} \propto \exp\left(\frac{V_{SG} - V_{t,pst}}{m\phi_t}\right) \tag{23}$$

$$\text{where} \quad V_{t,pst} = -\Delta V + V_{t,pre} \tag{24}$$

$$I_{D,pst} \propto \exp\left(\frac{V_{SG} + \Delta V - V_{t,pre}}{m\phi_t}\right) \tag{25}$$

$$I_{D,pst} \propto \exp\left(\frac{V_{SG}^{*} - V_{t,pre}}{m\phi_t}\right) \tag{26}$$

$$\text{where } V_G^{*} = V_G - \Delta V \tag{27}$$

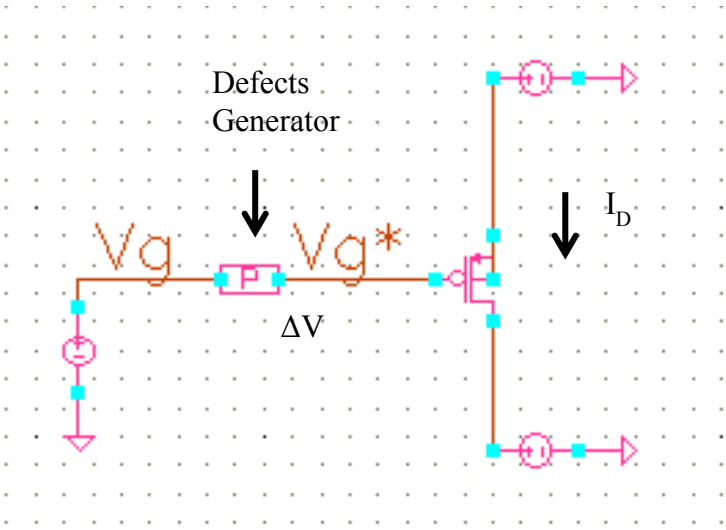


Figure 14: Simulation Setup for PMOS with the Degradation Model

Figure 14 shows the simulation setup for PMOS transistor. ΔV is the defect potential.

From (19), we know that for a PMOS transistor the total charge accumulated because of the interface traps and oxide charge is

$$Q_{total} = Q_{ot} + Q_{it} \tag{28}$$

Therefore

$$\Delta V = -\frac{qN_{ot}}{C_{ox}} - \frac{qD_{it}(\psi_S - \phi_B)}{C_{ox}} \tag{29}$$

$$\Delta V = -\frac{qN_{ot}}{C_{ox}} + \frac{qD_{it}\phi_B}{C_{ox}} - \frac{qD_{it}\psi_S}{C_{ox}} \tag{30}$$

From (43) $$\psi_S \approx \frac{C_{ox}}{C_{dm} + \xi C_{ox}}\left(V_{t,pst} - V_G\right) + 2\phi_B$$

where

$$\xi = 1 + \frac{qD_{it}}{C_{ox}} \tag{31}$$

and $\psi_S - 2\phi_B$ is small

$$\therefore \quad \Delta V \approx -\frac{qN_{ot}}{C_{ox}} - \frac{qD_{it}\phi_B}{C_{ox}} - \frac{qD_{it}}{C_{dm} + \xi C_{ox}}\left(V_{t,pst} - V_G\right) \tag{32}$$

Now

$$V_{t,pst} \approx -\frac{qN_{ot}}{C_{ox}} - \frac{qD_{it}\phi_B}{C_{ox}} + V_{t,pre} \tag{33}$$

So

$$\Delta V \approx -\frac{qN_{ot}}{C_{ox}} - \frac{qD_{it}\phi_B}{C_{ox}} - \frac{qD_{it}}{C_{dm} + \xi C_{ox}}\left(-\frac{qN_{ot}}{C_{ox}} - \frac{qD_{it}\phi_B}{C_{ox}} + V_{t,pre} - V_G\right) \tag{34}$$

The derivation for surface potential (ψ_S)

$$V_G = V_{FB} - \xi\psi_S - \gamma\sqrt{\psi_S} \tag{35}$$

if

$$\psi_S = 2\phi_B - \Delta\psi \text{ and } \Delta\psi << 2\phi_B$$

$$V_G = V_{FB} - \xi(2\phi_B - \Delta\psi) - \gamma\sqrt{2\phi_B - \Delta\psi} \tag{36}$$

$$V_G = V_{FB} - \xi(2\phi_B - \Delta\psi) - \gamma\sqrt{2\phi_B}\sqrt{1 - \frac{\Delta\psi}{2\phi_B}} \tag{37}$$

$$V_G \approx V_{FB} - \xi(2\phi_B - \Delta\psi) - \gamma\sqrt{2\phi_B}\left(1 - \frac{1}{2}\frac{\Delta\psi}{2\phi_B}\right) \tag{38}$$

$$V_G \approx V_{FB} - \xi(2\phi_B) + \xi\Delta\psi - \gamma\sqrt{2\phi_B} + \gamma\frac{1}{2}\frac{\Delta\psi}{\sqrt{2\phi_B}} \tag{39}$$

$$V_G \approx V_{th} + \xi\Delta\psi + \gamma\frac{1}{2}\frac{\Delta\psi}{\sqrt{2\phi_B}} \tag{40}$$

$$V_G \approx V_{th} + \xi(2\phi_B - \psi_S) + \frac{C_{dm}}{C_{ox}}(2\phi_B - \psi_S) \tag{41}$$

where,

$$C_{dm} = \sqrt{\frac{\varepsilon_s q N_a}{4\phi_B}} \tag{42}$$

$$\therefore \psi_S \approx \frac{(V_{th}-V_G)}{\xi+\frac{C_{dm}}{C_{ox}}}+2\phi_B=\frac{C_{ox}}{C_{dm}+\xi C_{ox}}(V_{th}-V_G)+2\phi_B \tag{43}$$

We know that

$$\frac{qD_{it}}{C_{dm}+\xi C_{ox}}=\frac{qD_{it}}{C_{dm}+C_{ox}+qD_{it}}=\frac{qD_{it}/(C_{dm}+C_{ox})}{1+qD_{it}/(C_{dm}+C_{ox})}=\frac{qD_{it}}{mC_{ox}} \tag{44}$$

If, $qD_{it} << C_{dm}+C_{ox}$, so using Tylor series

$$\frac{qD_{it}}{mC_{ox}} \approx qD_{it}/(C_{dm}+C_{ox})-[qD_{it}/(C_{dm}+C_{ox})]^2 \tag{45}$$

The function $\frac{qD_{it}}{mC_{ox}}$ is a rational function, so it is approximated.

$$\Delta V \approx -\frac{qN_{ot}}{C_{ox}}-\frac{qD_{it}\phi_B}{C_{ox}}+\frac{qD_{it}}{mC_{ox}}\left(V_{GB}-V_{t,pre}+\frac{qN_{ot}}{C_{ox}}+\frac{qD_{it}\phi_B}{C_{ox}}\right) \tag{46}$$

In Strong Inversion,

For $V_{SG} \geq V_{t,post}$

$$\Delta V(V_G) \approx -\frac{qN_{ot}}{C_{ox}}-\frac{qD_{it}\phi_B}{C_{ox}}+\frac{qD_{it}}{mC_{ox}}\left(V_{GB}-V_{t,pre}+\frac{qN_{ot}}{C_{ox}}+\frac{qD_{it}\phi_B}{C_{ox}}\right)$$

The terms crossed out should be shorted out with a switch.

The shift ΔV in threshold voltage should be fixed to

$$\Delta V \approx -\frac{qN_{ot}}{C_{ox}}-\frac{qD_{it}\phi_B}{C_{ox}} \tag{47}$$

This captures the fact that in strong inversion the surface potential is "pinned" at ϕ_B. Thus the threshold voltage shift shows no more dependence on V_G.

For the 0.25u tsmc technology,

Oxide Thickness t_{ox} = 5.8nm.

Threshold Voltage V_{THo} = 0.4308V.

Substrate Doping N_{CH} = 2.35x10^{17} cm^{-3}.

Therefore Bulk potential $\phi_B = \frac{kT}{q} \ln\left(\frac{N_{CH}}{n_i}\right)$ =0.456V.

$C_{dm} = \sqrt{\frac{\varepsilon_s q N_a}{4\phi_B}}$ = 4.8x10^{-7} F/cm^2.

Figure 15 shows the degradation model developed in cadence.

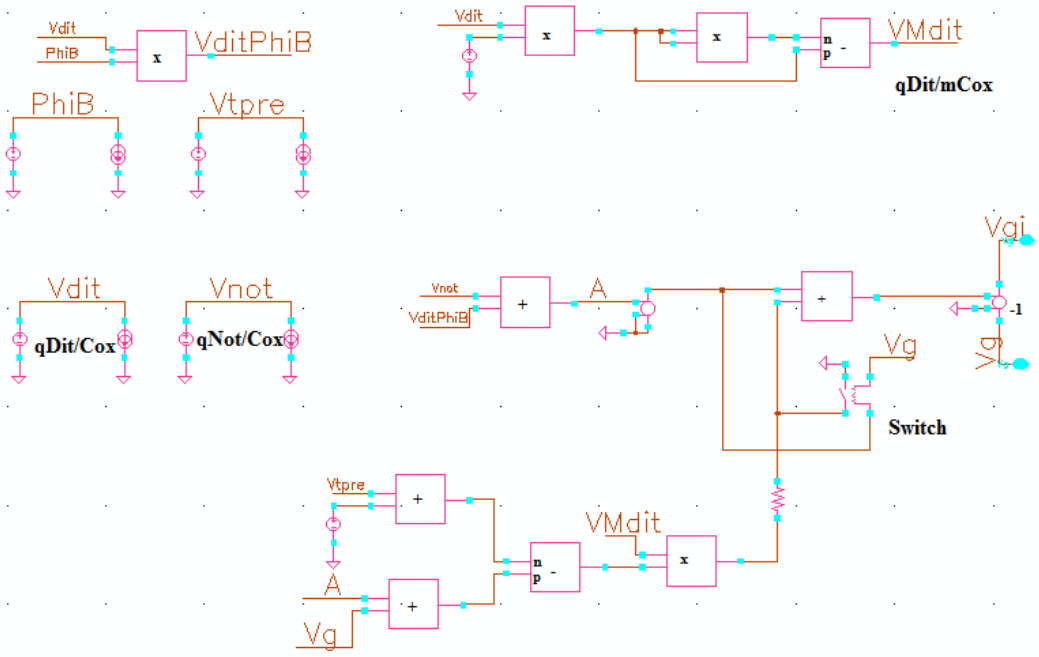


Figure 15: Degradation Model Schematic for a PMOS Transistor

4.2 Modelling of defects in NMOS transistor

The same approach used for PMOS applies for NMOS transistor too with slight changes as shown below.

The total charge accumulated because of defects in NMOS from (21) is

$$Q_{total} = Q_{ot} - Q_{it}$$

Therefore the threshold voltage shift is

$$\Delta V = -\frac{qN_{ot}}{C_{ox}} + \frac{qD_{it}(\psi_S - \phi_B)}{C_{ox}} \tag{48}$$

After substituting for surface potential and solving for ΔV, we get the defect potential as

$$\Delta V \approx -\frac{qN_{ot}}{C_{ox}} + \frac{qD_{it}\phi_B}{C_{ox}} + \frac{qD_{it}}{mC_{ox}}\left(V_G - V_{t,pre} + \frac{qN_{ot}}{C_{ox}} - \frac{qD_{it}\phi_B}{C_{ox}}\right) \tag{49}$$

In Strong Inversion,

For $V_{GS} \geq V_{t,post}$

$$\Delta V(V_G) \approx -\frac{qN_{ot}}{C_{ox}} + \frac{qD_{it}\phi_B}{C_{ox}} + \frac{qD_{it}}{mC_{ox}}\left(V_G - V_{t,pre} + \frac{qN_{ot}}{C_{ox}} - \frac{qD_{it}\phi_B}{C_{ox}}\right)$$

The crossed out terms are shorted out with a switch in strong inversion.

The shift ΔV in threshold voltage should be fixed to

$$\Delta V \approx -\frac{qN_{ot}}{C_{ox}} + \frac{qD_{it}\phi_B}{C_{ox}} \tag{50}$$

4.3 Validation and Results

The PMOS transistor is modelled in Silvaco (Atlas) as shown in Figure 4.3. The model parameters are taken from the compact models of 0.25u CMOS technology and then the I-V characteristics of a transistor are compared both in Cadence (0.25µ) and TCAD. Once both the curves fit each other, the degradation model is developed in cadence according to the equation (46). The degradation block is then inserted before the gate of the transistor and the post stress simulations are done. Similarly in TCAD the post stress simulations are done with the interface and oxide traps and the I-V characteristics are compared till both fit each other. The block diagram for validating the degradation model with TCAD is shown in Figure 16. We validate the model by fitting the IV curves in cadence model and in TCAD simulations. The comparison is done for four different values of interface and oxide traps. The same process is repeated for NMOS transistor.

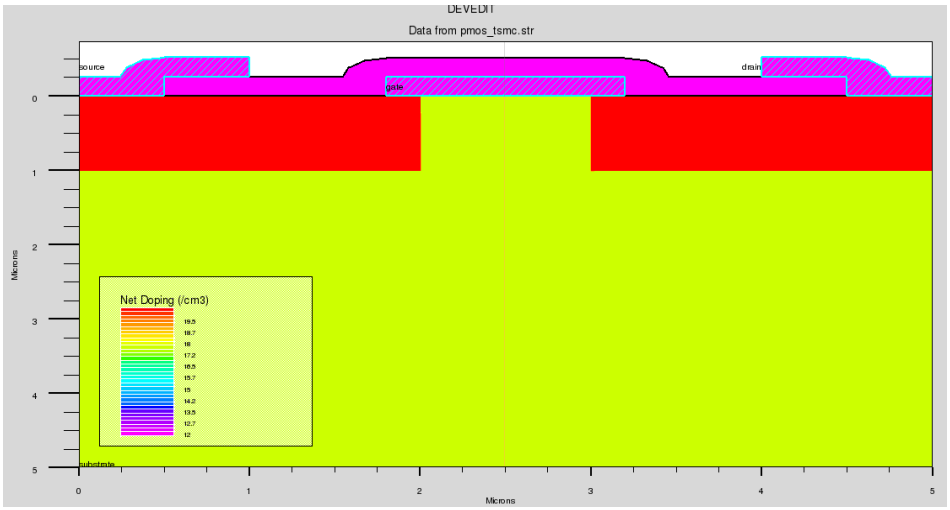


Figure 16: p- Channel MOSFET Silvaco Structure

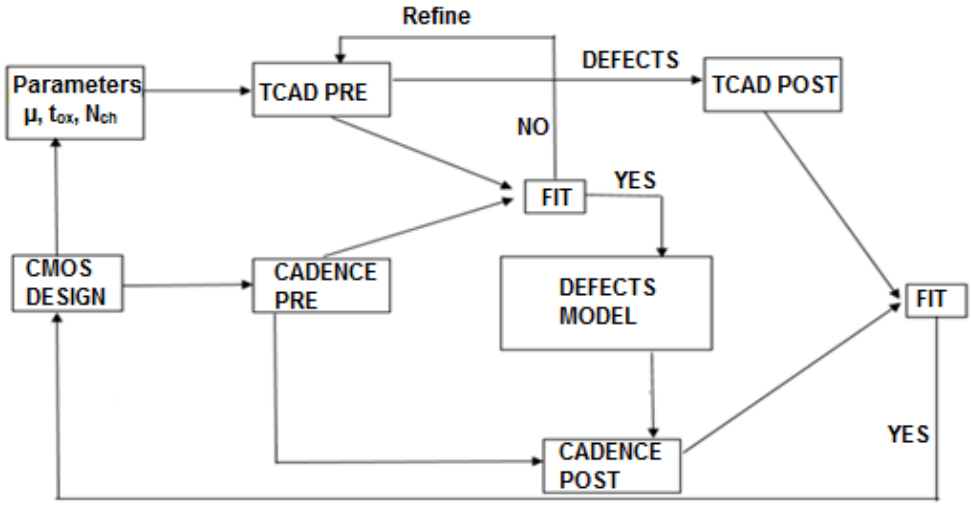


Figure 17: Validation Model Block Diagram

The model parameters for the TCAD structure are taken from the compact model of tsmc 0.25u technology. Figure 17 shows the block diagram of validating the model.

4.3.1 IV characteristics

The current voltage characteristics are plotted when the gate voltage is swept from 2.5V to 0.

(a) For N_{ot} = 0 and D_{it} = 0

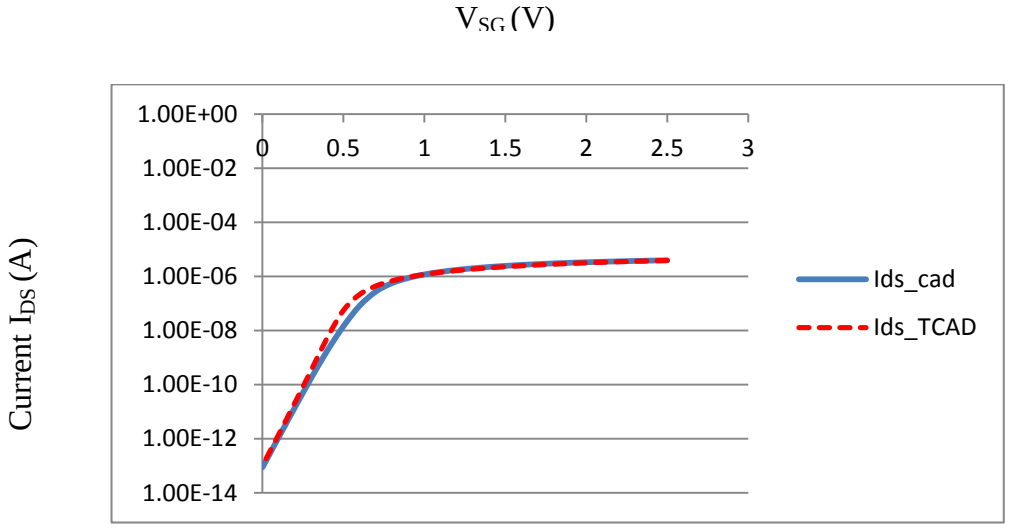


Figure 18: I-V Curves of PMOS for N_{ot} = 0 and D_{it} = 0.

(b) For N_{ot} = 1.2 x 10^{12} cm^{-2} and D_{it} = 1 x 10^{12} cm^{-2}

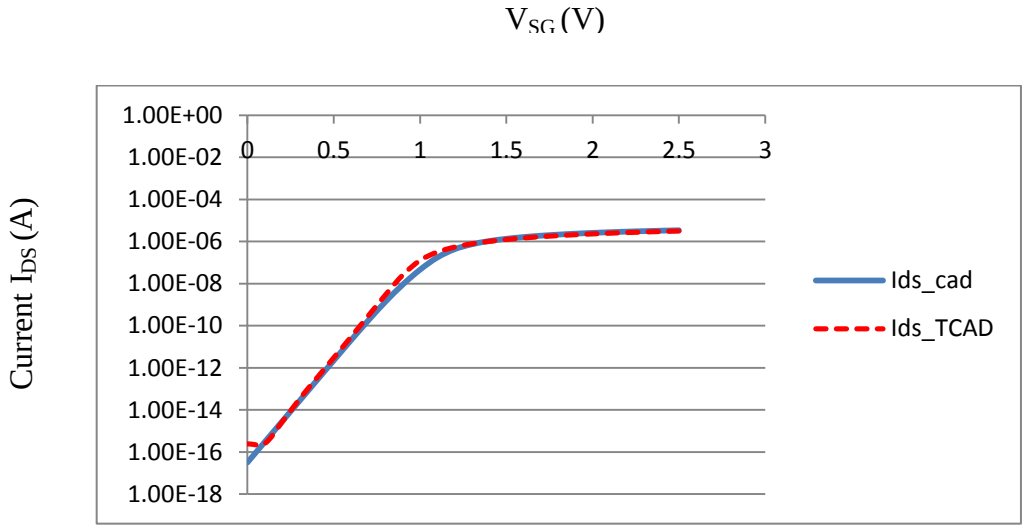


Figure 19: I-V Curves of PMOS with N_{ot} = 1.2 x 10^{12} cm^{-2} and D_{it} = 1 x 10^{12} cm^{-2}.

(c) For N_{ot} = 0 and D_{it} = 1 x 10^{12} cm^{-2}

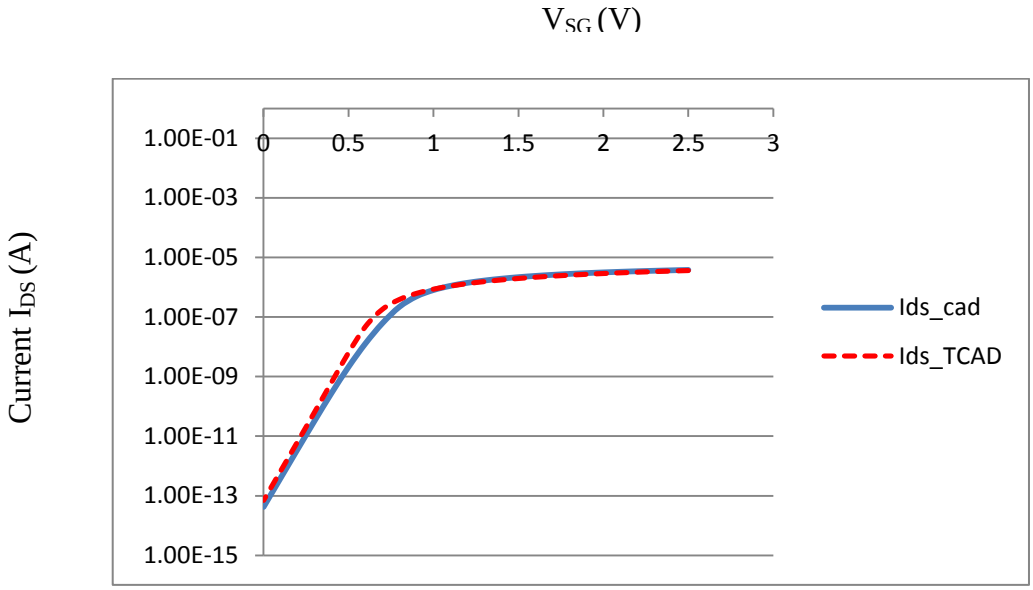


Figure 20: I-V Curves of PMOS with N_{ot} = 0 and D_{it} = 1 x 10^{12} cm^{-2}.

(d) For N_{ot} = 1.2 x 10^{12} cm^{-2} and D_{it} = 0

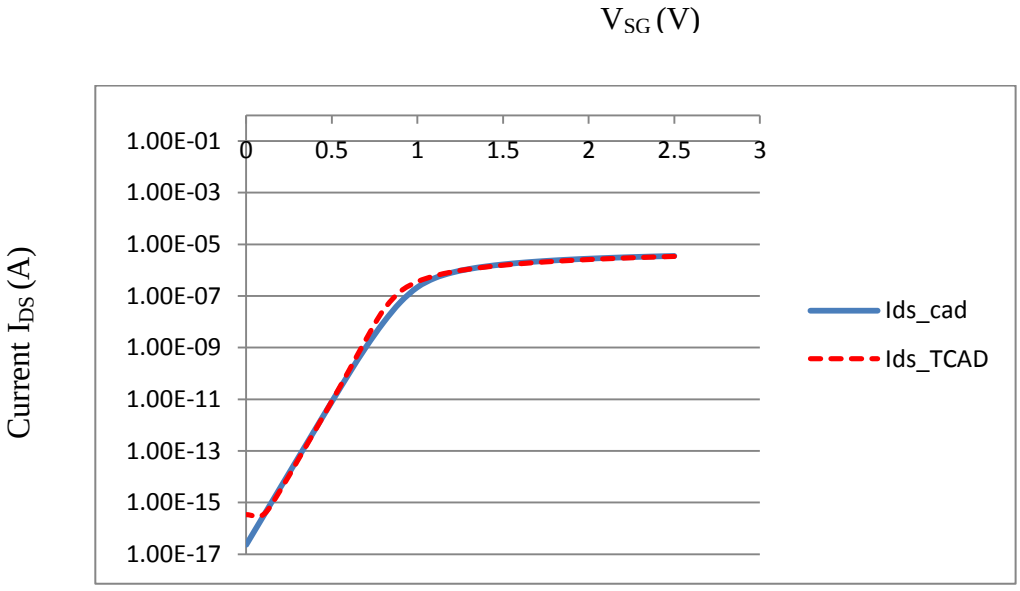


Figure 21: I-V Curves of PMOS with N_{ot} = 1.2 x 10^{12} cm^{-2} and D_{it} = 0.

As we see from the above curves, the I-V characteristics of the PMOS closely fit each other in cadence and TCAD. The comparison is made first without any defects and then with defects for four different cases. In all the cases the degradation model mimics the defects very well.

4.3.2 Threshold Voltage Shift

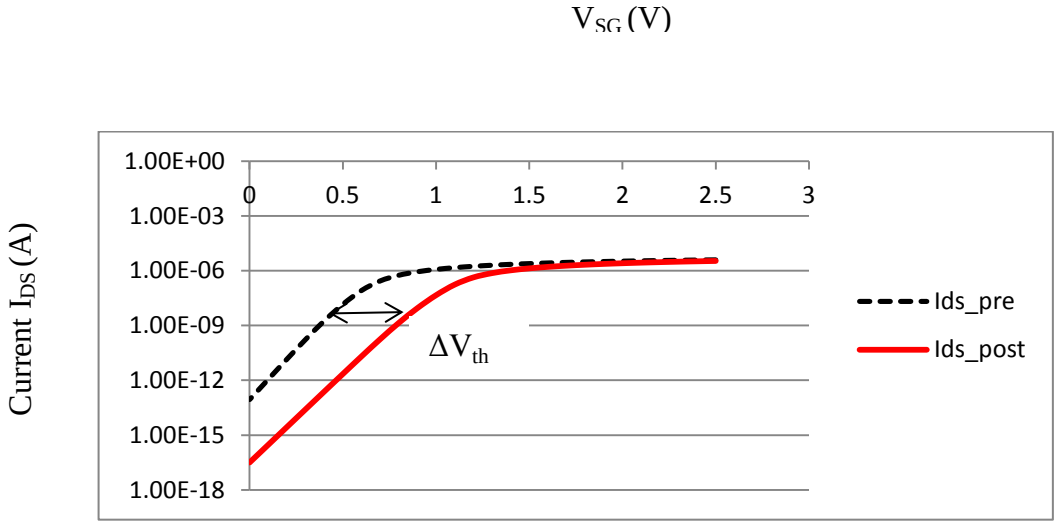


Figure 22: Threshold Voltage Before and After the Degradation Model

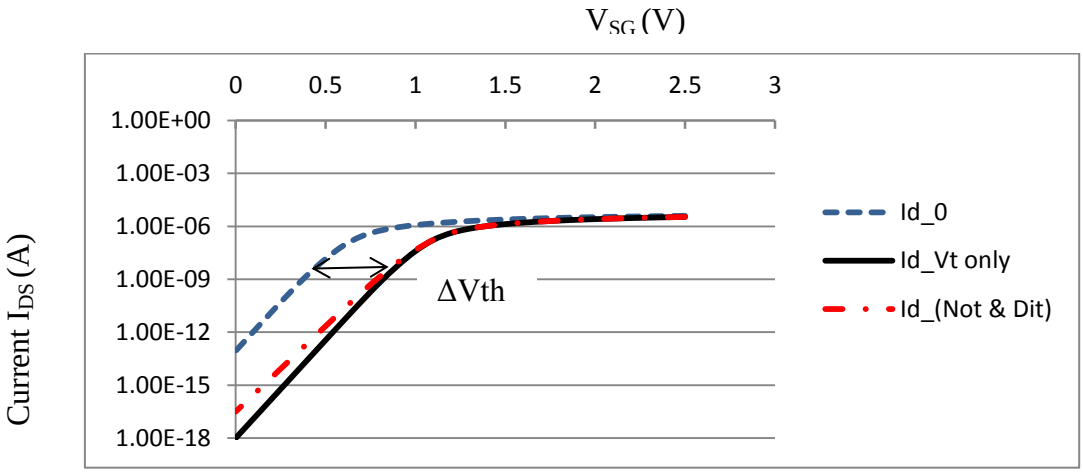


Figure 23: Threshold Voltage Shift- Defect Model and Vt Only

The Current-Voltage curves are generated for a PMOS with and without the degradation model. We see a threshold voltage shift in the Figure 22, which is caused by the defects.

Figure 23 shows the current-voltage plots with and without gate bias dependence of the defects. In the Vt only plot, the change in threshold voltage is given by the equation (47). Whereas in the other current plot the defects are dependent on gate voltage in the sub threshold region and the threshold voltage difference is given by the equation (46).

4.4 Modeling Defect Generators

4.4.1 Interface Traps (D_{it}) Generator

For interface traps the response profile increases with stress, but remains virtually constant once the stress is removed. Figure 24 shows the ideal response of interface traps during stress and when the stress is removed.

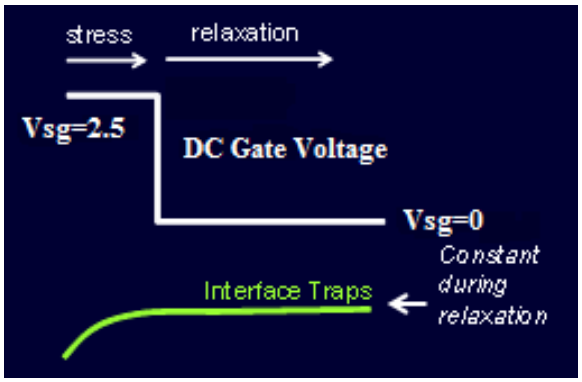


Figure 24: Ideal Response of Interface Traps during Stress and Relax

This may also be captured by the transient equation but instead with a very large delay time constant.

$$V_{Dit}(t) = V_{pb}[(1\text{-}\exp(-\frac{t}{\tau_1}))u(t) - (1 - \exp(-\frac{t-T}{\tau_2}))u(t\text{-}T)] \quad (51)$$

where

$$V_{Dit}(t) = \frac{qD_{it}(t)}{C_{ox}} \quad (52)$$

The equation (51) can be implemented in cadence as shown in Figure 25.

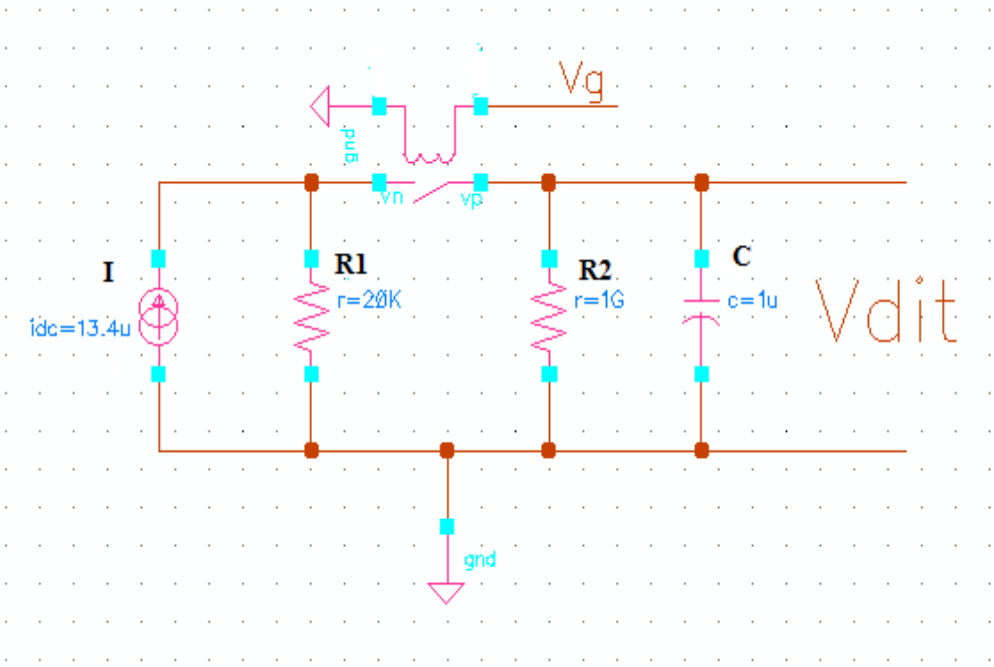


Figure 25: Nit Defect Generator Schematic

The maximum value of D_{it} is taken to be $1x10^{12}$.

Therefore $V_{Dit} = \frac{qD_{it}}{C_{ox}} = 268mV$.

During Stress, the switch is closed and the time constant $\tau_1 = (R1||R2)C$.

During Relax, the switch is open and the time constant $\tau_2 = (R2)C$.

We want the delay time constant to be very large, so R2 is a big value.

So one can select values R2 = 1GΩ and C = 1uF.

Since $V_{max} = 268mV = I(R1||R2)$.

So accordingly one can select values R1 = 20kΩ and I = 13.4u.

When Vg = 0 i.e. Vsg=2.5 and hence it is a stress and the Interface Trap voltage increases with time and when Vg=2.5 i.e. Vsg=0, it is relax and hence the voltage remains constant as shown is Figure 26. The interface traps don't anneal during relax.

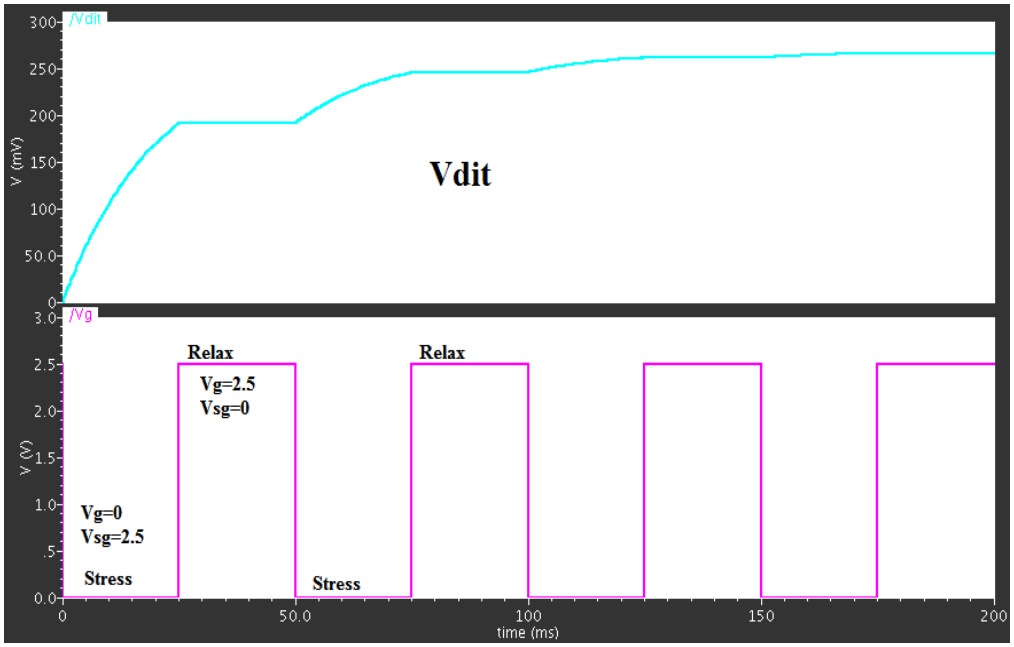


Figure 26: Interface Trap Voltage with Time and Gate Bias

4.4.2 Oxide Traps (N_{ot}) Generator

In response to gate voltage stress, the fixed trapped charge density may be assumed to follow a double exponential response profile. Figure 27 shows the ideal response of the oxide traps during stress and when the stress is removed.

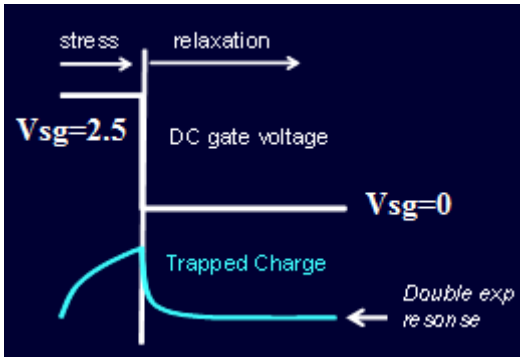


Figure 27: Ideal Response of Oxide Traps During Stress and Relax

The above response can be captured by the transient equation

$$V_{Not}(t) = V_{pb}[(1-\exp(-\frac{t}{\tau_1}))u(t) - (1 - \exp(-\frac{t-T}{\tau_2}))u(t-T)] \quad (53)$$

Where

$$V_{Not}(t) = \frac{qN_{ot}(t)}{C_{ox}} \quad (54)$$

The above equation can be generated in a circuit by a gate voltage-controlled switch and an RC network shown in Figure 28.

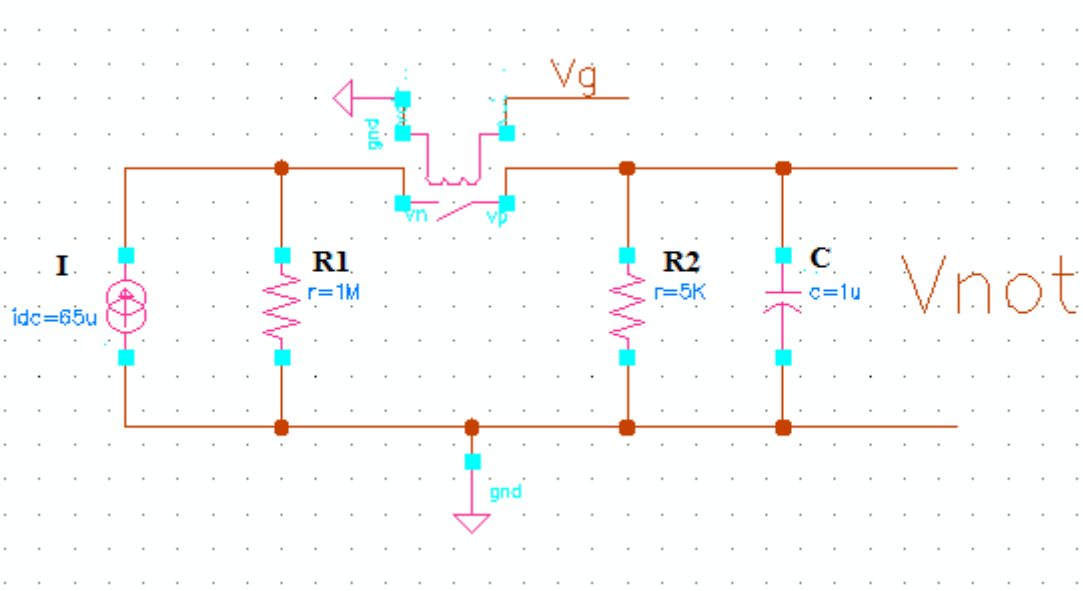


Figure 28: Not Defect Generator Schematic

The maximum value of N_{ot} is taken to be $1.2x10^{12}$.

Therefore $V_{Not} = \frac{qN_{ot}}{C_{ox}}$ = 322mV.

During Stress, the switch is closed and the time constant τ_1 = (R1||R2)C.

During Relax, the switch is open and the time constant τ_2 = (R2)C.

Since V_{max} = 322mV = I(R1||R2).

So accordingly one can select values R1 = 1MΩ, R2 = 5kΩ, C=1uF and I = 65u.

When Vg = 0 i.e. Vsg=2.5 and hence it is a stress and the Oxide Trap voltage increases with time and when Vg=2.5 i.e. Vsg=0, it is relax period and hence the voltage decreases as shown is Figure 29. The Oxide traps anneal when the stress is removed.

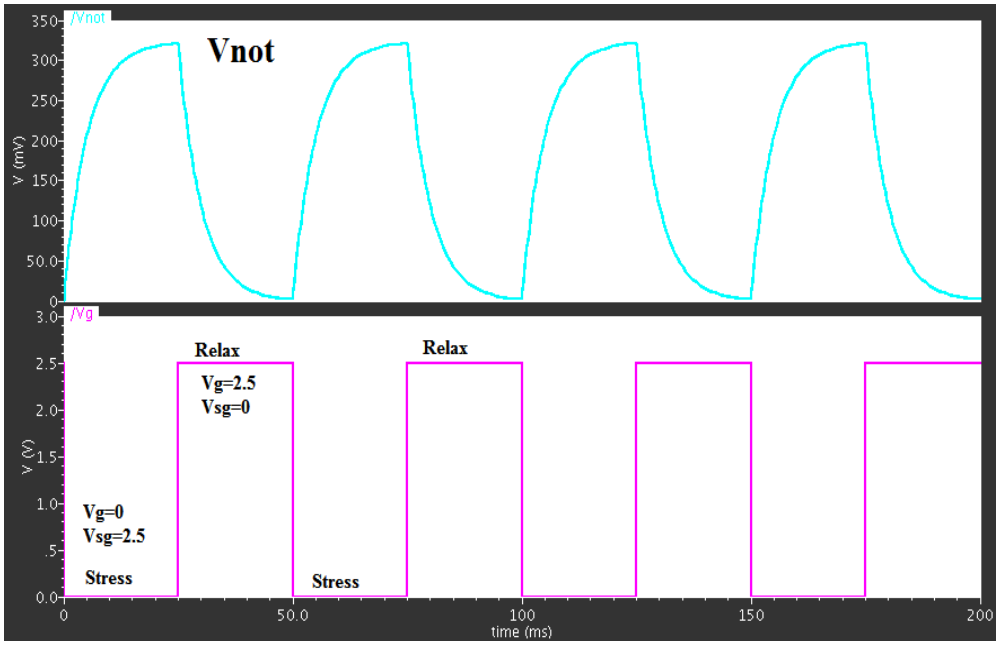


Figure 29: Oxide Trap Voltage with Time and Gate Bias

4.5 Static NBTI

In static NBTI, the gate of the PMOS transistor is stressed for a long time and the change in threshold voltage is observed with respect to time. The threshold voltage increases monotonically with time as the defects keeps on increasing. The threshold voltage shift shows two asymptotes: the slow response and the fast response [32]. The inrerface traps (D_{it}) voltage is very slow and takes a lot of time to reach its maximum value, whereas the oxide traps (N_{ot}) voltage reaches its saturation value way before the Interface trap voltage. Using the model developed in this work, a similar pattern is observed for the threshold voltage shift. Figure 30 shows the threshold voltage shift generated using our model. The time constants used in the equations (51) and (53) are chosen in such a way that the final value of oxide trap voltage saturates much before the final value of the interface trap voltage.

The change in threshold voltage varies with time as a power-law [32].

$$\Delta V_{th} \propto t^{n}$$

The value of n varies depending of what type of defects dominates.

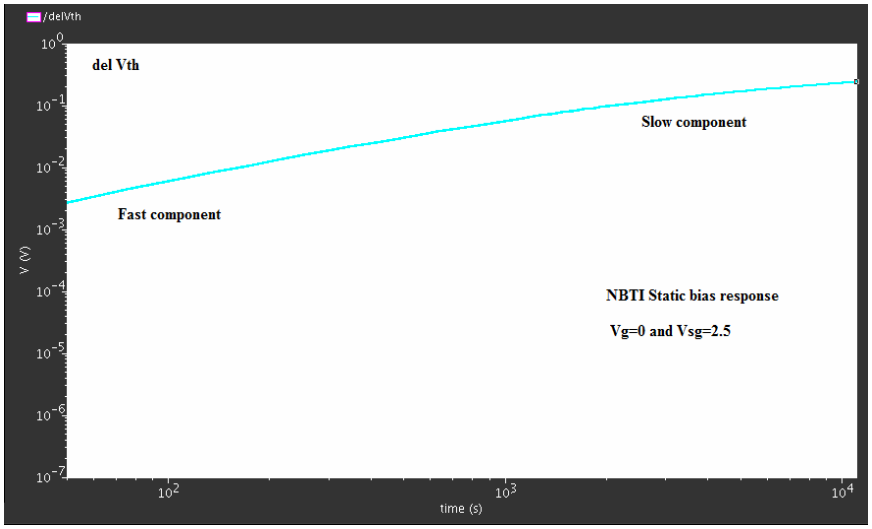


Figure 30: Static NBTI

4.6 Dynamic NBTI

In Dynamic NBTI, the gate of the PMOS transistor is allowed to switch from 0 to V_{DD}. When the source gate voltage is 0, the transistor is in strong inversion and because of the gate stress oxide traps and interface traps are formed. When the stress is removed i.e. if the source gate voltage is V_{DD}, then the defects are annealed up to certain extent because the trapped holes will be de-trapped as discussed in the earlier sections. The interface traps are fixed but the oxide traps anneal when the stress is removed. Therefore the threshold voltage degradation is annealed up to some extent.

Figure 31 shows the threshold voltage with time using the degradation model. The fast component is because of the oxide traps whereas the slow component is due to the interface traps [32].

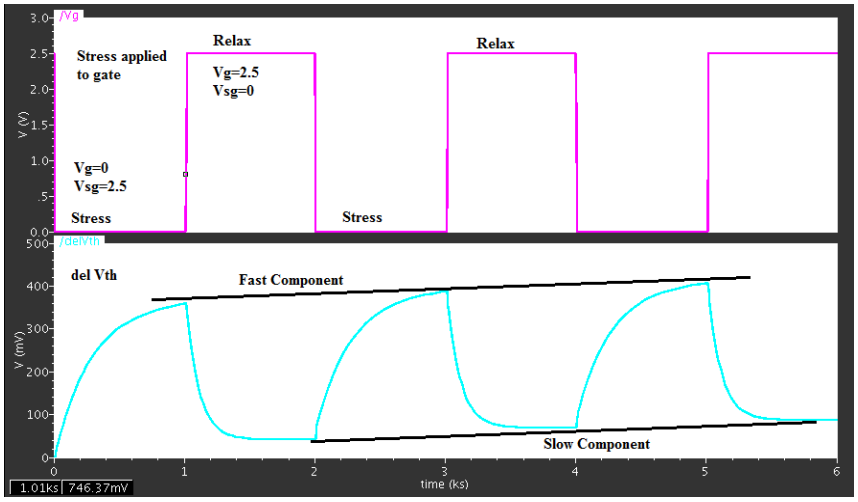


Figure 31: Dynamic NBTI

CHAPTER 5

NBTI EFECTS IN CMOS CIRCUITS

5.1 CMOS Inverter

The CMOS inverter is a basic building block for digital circuit design. The input to the inverter is connected to both a PMOS transistor and an NMOS transistor. When the voltage of input A is low, the NMOS transistor is turned off and its channel is in a high resistance state. The PMOS transistor is strongly on and its channel is in a low resistance state and it allows the current to flow from the V_{DD} to the output. It charges the load capacitance. As the resistance between the supply voltage and output is low, the voltage drop between the supply voltage and output due to a current drawn from output is small resulting in a high voltage at the output [27].

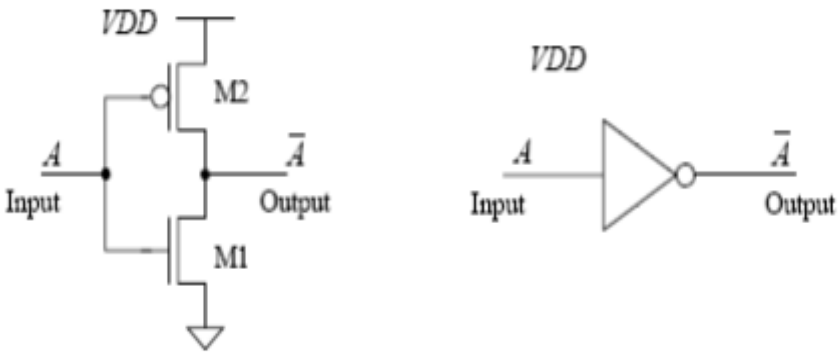


Figure 32: CMOS Inverter

On the other hand, when the voltage of input A is high, the PMOS transistor is turned off so it would not allow the current to flow from the V_{DD} to the output, while the NMOS transistor is completely turned on and, allowing the current to flow from output to ground. The low resistance between output and ground keeps the voltage

drop due to a current drawn into output very small. This low drop results in a low output voltage [27].

In short, inverter is a circuit where the output is inverted, such that when the input is high (V_{DD}), the output is low (0), and when the input is low, the output is high. The NMOS and PMOS transistor goes through different regions as the input swings from 0 to V_{DD}. The threshold voltage of both the transistors is important as the propagating signal depends on the threshold voltage.

This CMOS inverter transfer characteristics is shown in Figure 33.

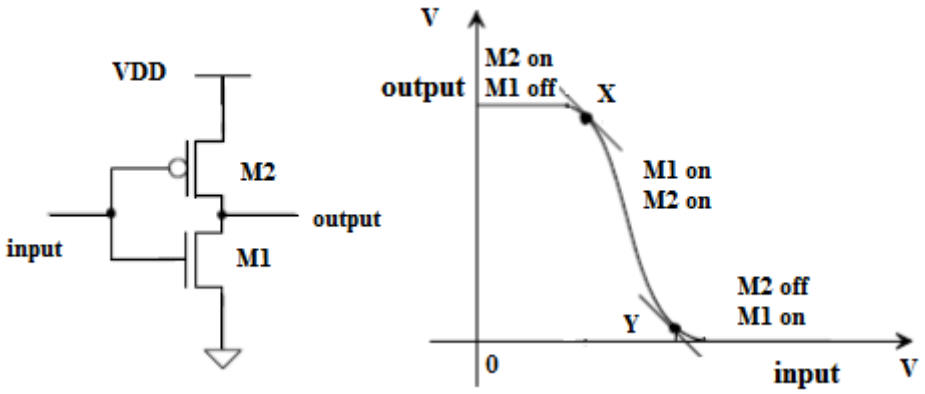


Figure 33: The CMOS Inverter Voltage Transfer Characteristics

There are various regions of operation when the input goes from 0 to V_{DD}. When the input is low, the M2 transistor is turned on while the M1 transistor is off. In the mid values of input, both the transistors are turned on. When the input is high, the M2 transistor is off and M1 transistor is turned on. X and Y are the transition points. The total intrinsic propagation delay of an inverter is given by $t_d = (t_{pHL} + t_{pLH})/2$, where t_{pHL} and t_{pLH} are explained in Figure 34.

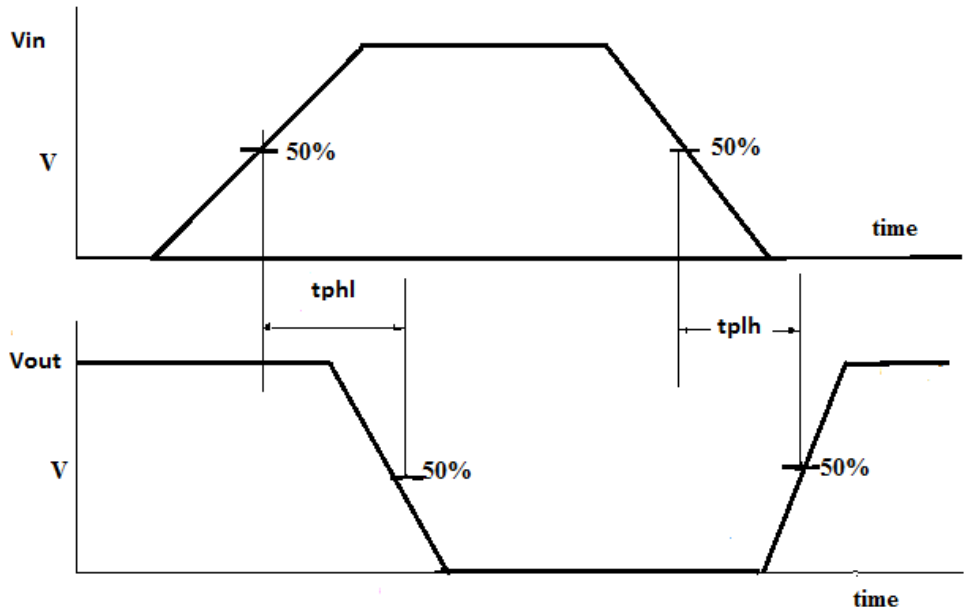


Figure 34: Inverter Propagation Delay

The propagation delay depends on almost all the parameters like supply voltage, threshold voltage, width, effective length, channel mobility etc.

5.1.1 NBTI Effects in CMOS Inverter

NBTI primarily occurs in p-channel MOSFET's when a negative gate voltage is applied and it is almost negligible when a positive voltage is applied. When the source gate voltage is high, the transistor is in stress and when source gate voltage is zero, the transistor is off. Although the defects increase with stress, but when the stress is removed then interface traps are going to be annealed which recovers the threshold voltage. This leads to an increase in the propagation delay. The NBTI can also cause a spread in signals. The increase in spread of signals can cause serious malfunction of the logic circuits and hence they will be failed [18].

The delay time t_d [53] is

$$t_d = \frac{CV_{DD}}{I} = \frac{C}{\frac{1}{2}\frac{W}{L}\mu_{eff}C_{ox}V_{DD}\left(1-\frac{V_{th}}{V_{DD}}\right)^2} \quad (55)$$

Therefore current decreases and delay time increases when threshold voltage increases and mobility decreases.

In an inverter the NBTI causes a propagation delay and when a chain of inverters are connected like in a ring oscillator circuit, the total propagation delay increases and which causes the frequency of the ring oscillator to change.

Table 2 shows the phases of bias temperature instability in a CMOS inverter.

Table 2: Bias Stress Temperature in Inverter [53]

V_{in}	V_{out}	NMOS	PMOS
0	V_{DD}	Relax(off)	NBTI(stress)
V_{DD}	0	PBTI(stress)	Relax(off)

Figure 35 illustrates the various phases of NBTI in a CMOS inverter when the gate voltage is swinging from 0 to V_{DD}.

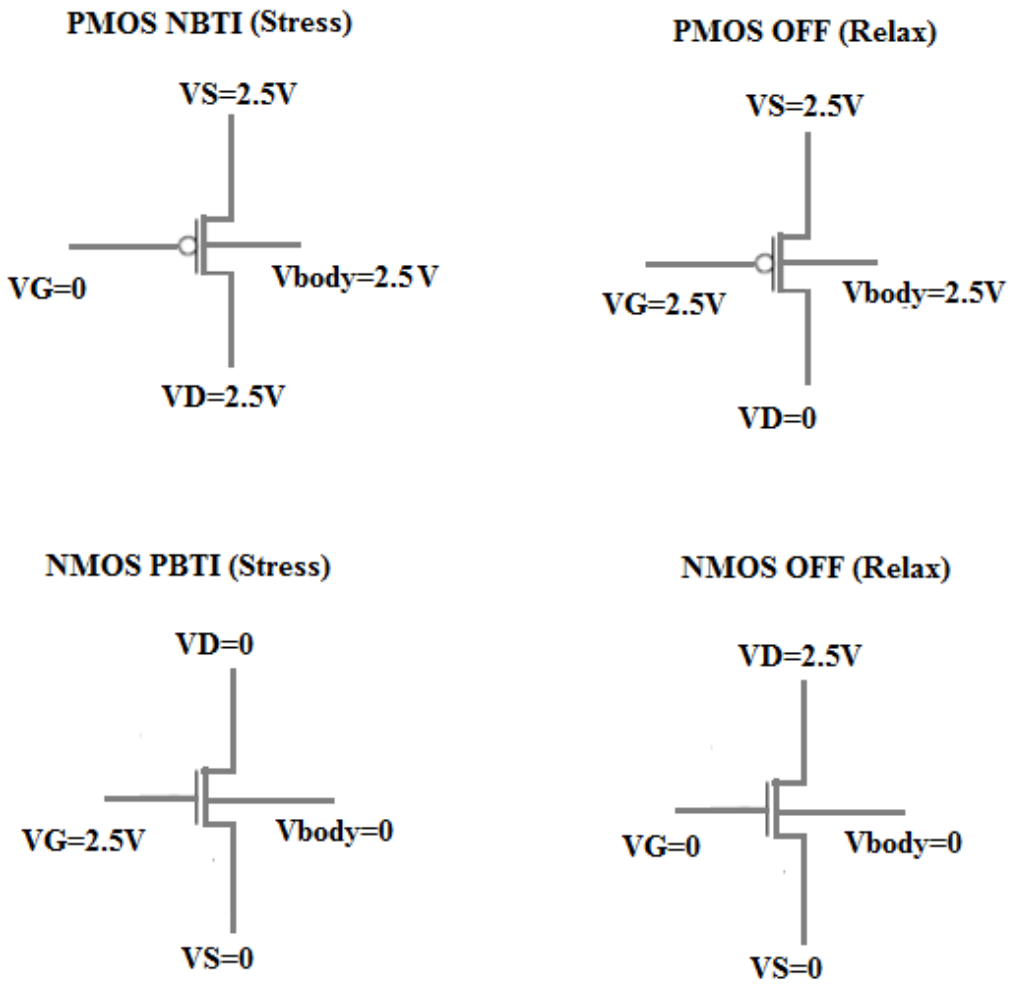


Figure 35: CMOS Inverter Degradation [53]

5.1.2 Inverter with the degradation model

The defect model developed in this model is connected to the gate terminals of both PMOS and NMOS in the inverter. Although the PBTI effect in NMOS is very less compared to that of NBTI in PMOS, the defect model for NMOS is also connected.

When the gate voltage is 0V, the source gate voltage for PMOS is V_{DD} hence it is stress condition. When gate voltage is V_{DD}, the PMOS is in off condition. Similarly when the gate voltage is 0, the NMOS is off and when the gate voltage is V_{DD} then the NMOS is under stress. Although the PBTI effects are very minimum compared to NBTI, both the effects are considered in this inverter simulation.

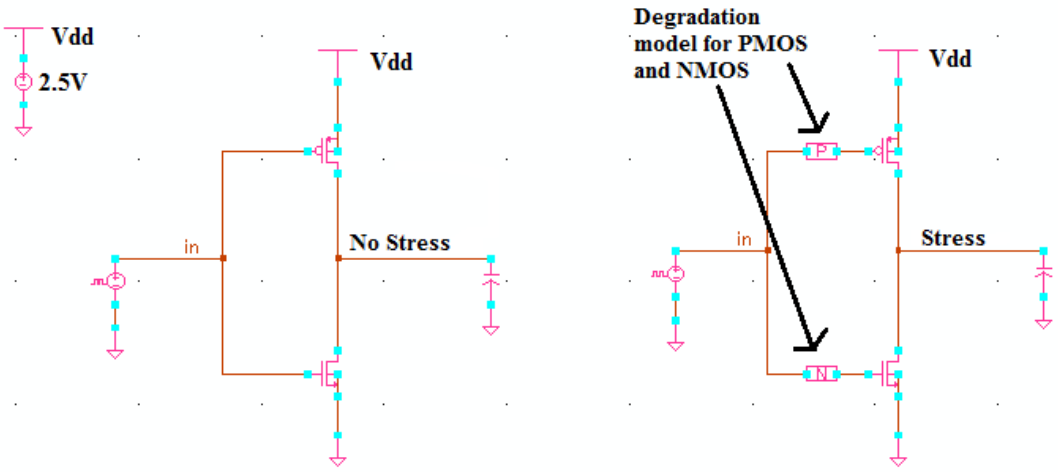


Figure 36: CMOS Inverter with and Without Degradation Models

Table 3: Component parameters of Inverter

W_p(nm)	12000
W_n(nm)	4000
L(nm)	1000

Inverter with and without the degradation model are shown in Figure 36. The degradation model mimics the effects of NBTI in PMOS. The width and lengths of PMOS and NMOS used in the inverter design are shown in table 3. When the stress is applied, interface traps and oxide traps are formed which degrades the performance of

the PMOS by reducing its mobility and increasing absolute value of threshold voltage. This causes a propagation delay in the inverter as shown in Figure 37. Although the defects models are modeled for both PMOS and NMOS, the only major factor contributing for propagation delay is the NBTI effect of PMOS transistors as the PBTI in NMOS contributes very less effect. As the simulation results shows that the defects cause an asymmetry in the rise and fall times and the propagation time for the signal increases causing a delay. So when the inverters are connected in a chained fashion like in a ring oscillator, the total propagation delay increases and frequency of the ring oscillator decreases.

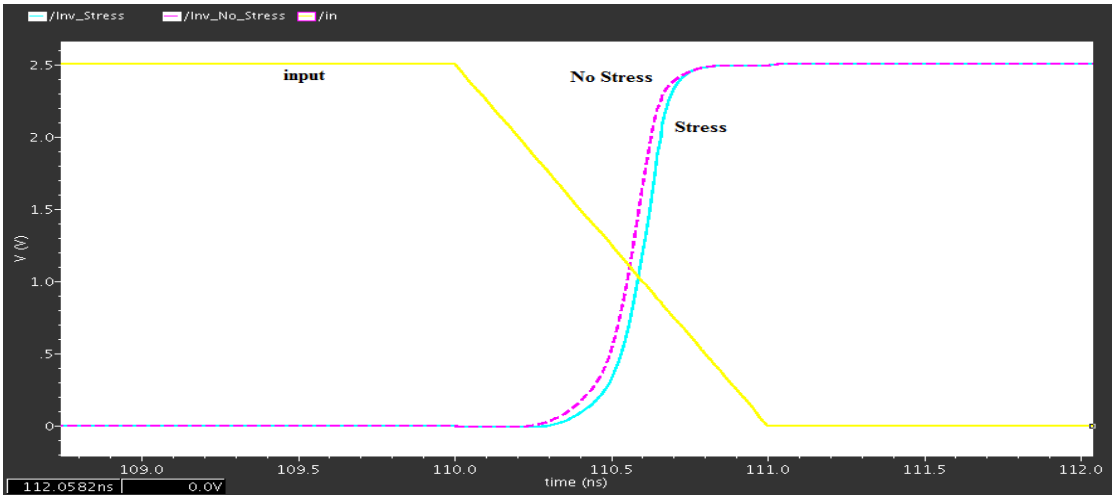


Figure 37: CMOS Inverter Output with and Without Stress

5.2 Ring Oscillator

A ring oscillator is a device composed of an odd number of Inverters connected in a positive feedback loop, whose output oscillates between two voltage levels 0 and V_{DD}. A block diagram of an n-stage inverter ring oscillator is shown in Figure 38.

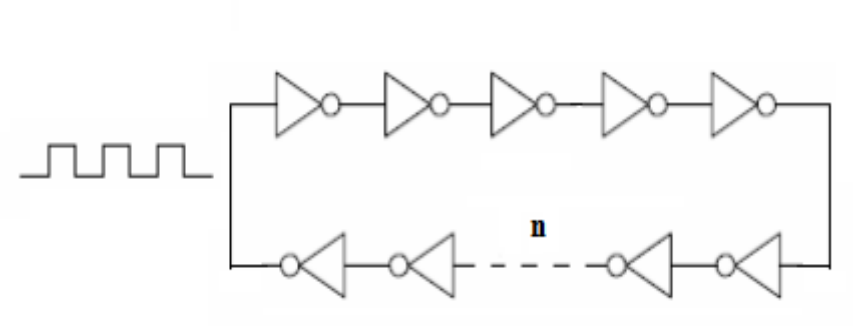


Figure 38: An n-Stage Ring Oscillator

The inverters are connected in a chain fashion in stages; the inverters are basically connected in cyclic order, so that the output of the last inverter is fed back as an input to the first inverter of the chain. As there will be an inversion for every stage of inverters, the output will also be inverted if the number of stages is an odd number. There is a certain time delay for every inverter for the signal to pass from input to output. It is also the same time to charge and discharge the capacitance at the output node. Thus every inverter in the chain has a time delay for its output to show up. As the number of inverters increase, the gate delay increases which decreases the frequency of the ring oscillator. The main reason for the oscillation is the odd number of inverters and output of last inverter feeding back into the input. A real ring oscillator is almost a self-start circuit which only requires power to operate; above a certain threshold voltage, oscillations begin spontaneously. To increase the frequency of oscillation, ring oscillator should be made from a smaller number of inverters.

The frequency of oscillation at each stage is inversely proportional to the number of stages in the ring oscillator circuit and the gate delay of each individual gate. As the number of stages increase, the frequency of oscillation decreases.

$$f_{osc} = \frac{1}{2nt_d} \quad (56)$$

Where "n" denotes the number of inverters used, t_d is the time delay of each inverter.

The frequency of the ring oscillator depends on process parameters like the width, length, threshold voltage etc. The propagation delay of an inverter circuit can be obtained by measuring the time period of the oscillator.

With the gate stress and at elevated temperatures, the interface traps and oxide traps are formed which degrades the performance of the transistor by increases the threshold voltage and degrading other important parameters. As the threshold voltage increases, the value of (V_{DD}–V_{th}) decreases and hence it increases the delay according to the equation (55).

In this work, a ring oscillator circuit of 5 inverters chain is designed as shown in Figure 39 and is simulated with and without the stress. In spectre simulations, an initial condition is given to the output node and then the output oscillates automatically. The results are also compared with the results of only V_t mode. The frequency of the ring oscillator without stress is 246.5MHz and we observed that the frequency with stress as decreased. The frequency of the ring oscillator with stress i.e., when the defects model is applied is 204MHz. The frequency when just the V_t model is applied is 198.5MHz.

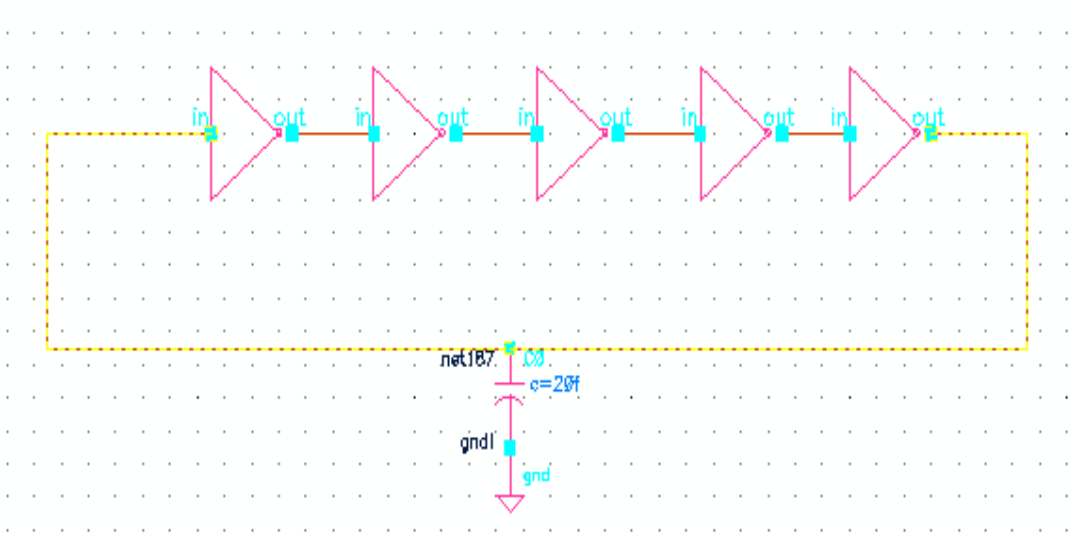


Figure 39: Ring Oscillator Schematic with 5 Inverters

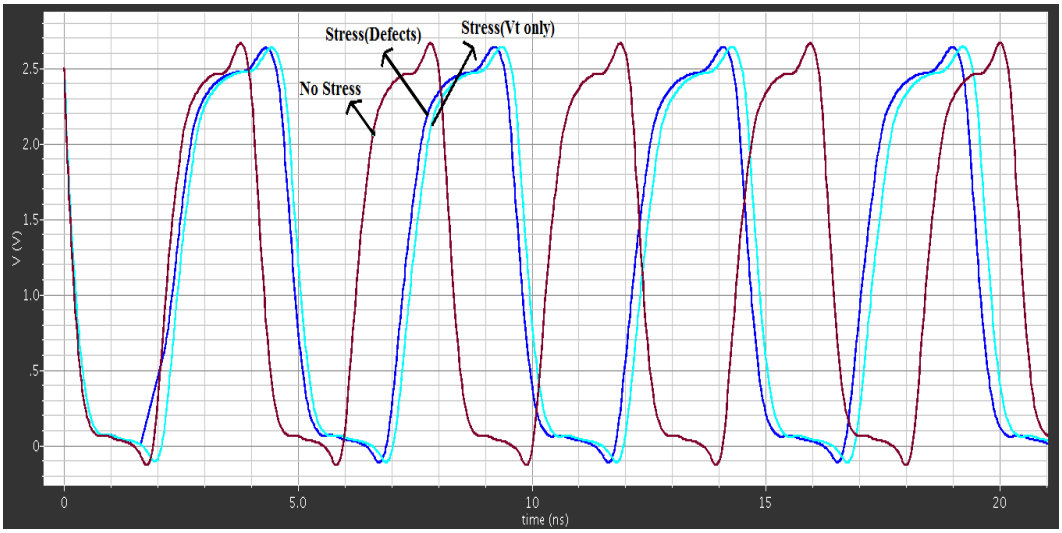


Figure 40: Ring Oscillator Output Waveform with and Without Stress

The transient response with and without stress are shown in Figure 40. In the V_t model, the gate bias dependency in the subtreshold region is not considered. The frequency response is compared in Figure 41 and Figure 42 respectively.

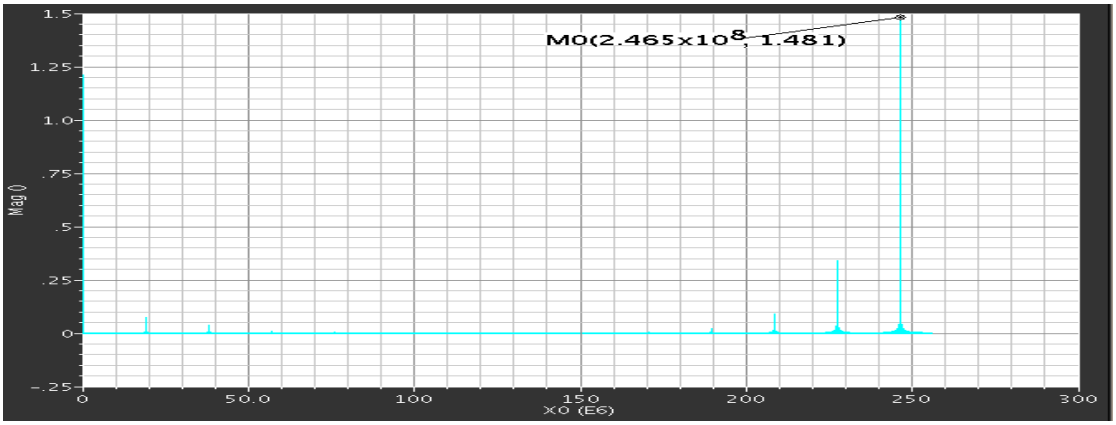


Figure 41: Frequency Response without Stress

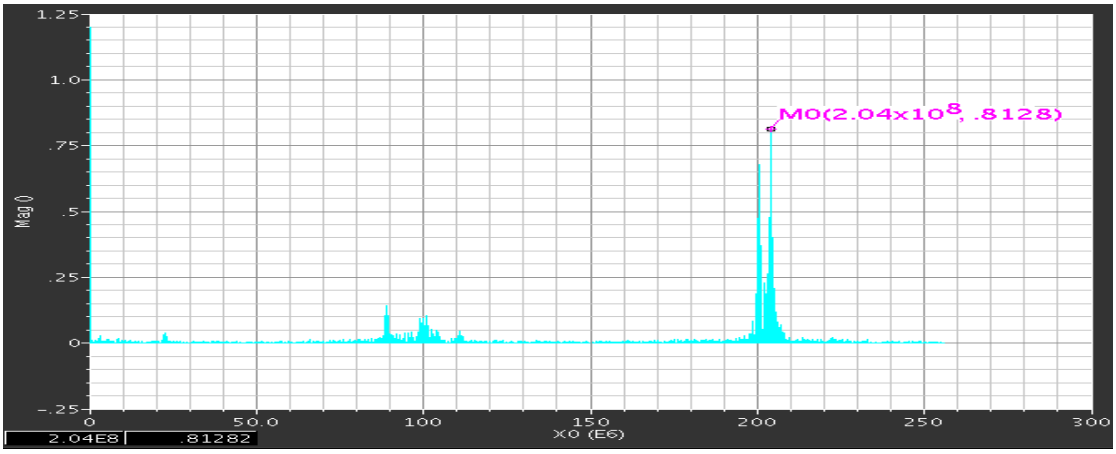


Figure 42(a): Frequency Response with Stress (Defects Model)

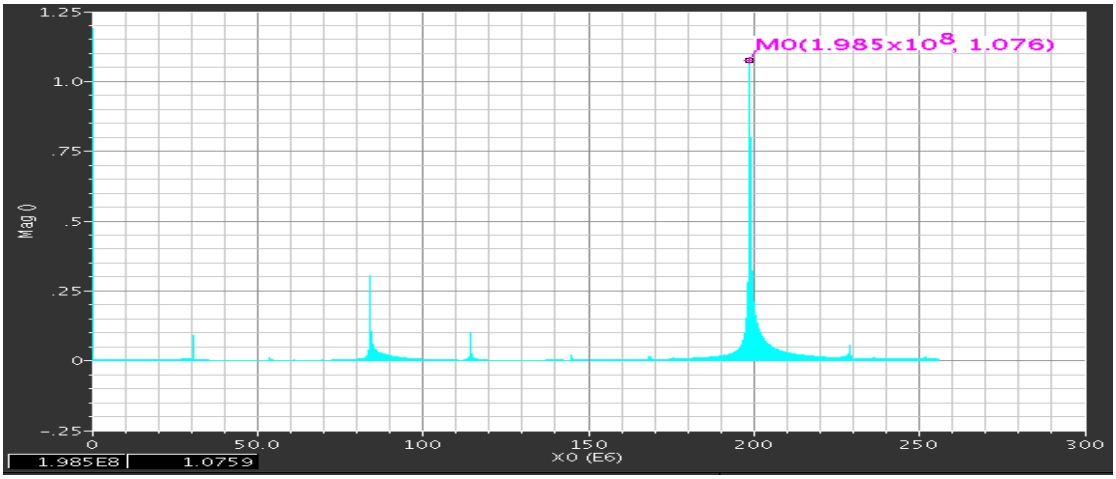


Figure 42(b): Frequency Response with Stress (V_t Model)

The model is also applied to test the single event transient (SET) pulse broadening and we see the pulse broadening with stress as shown in Figure 45.

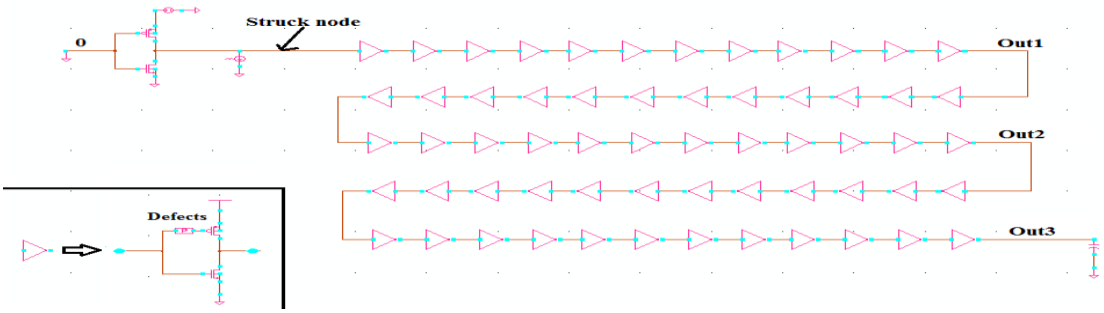


Figure 43: Modeling SET Pulse Broadening

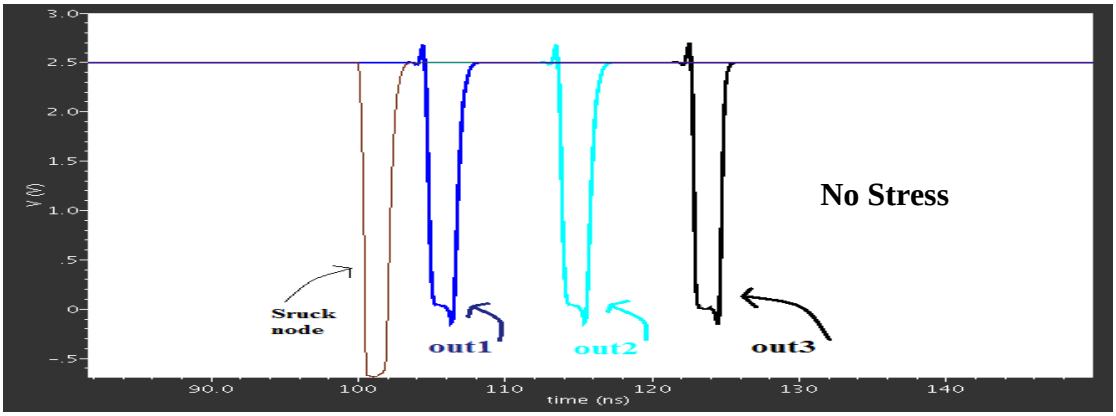


Figure 45(a): SET Pulse Broadening Without Stress

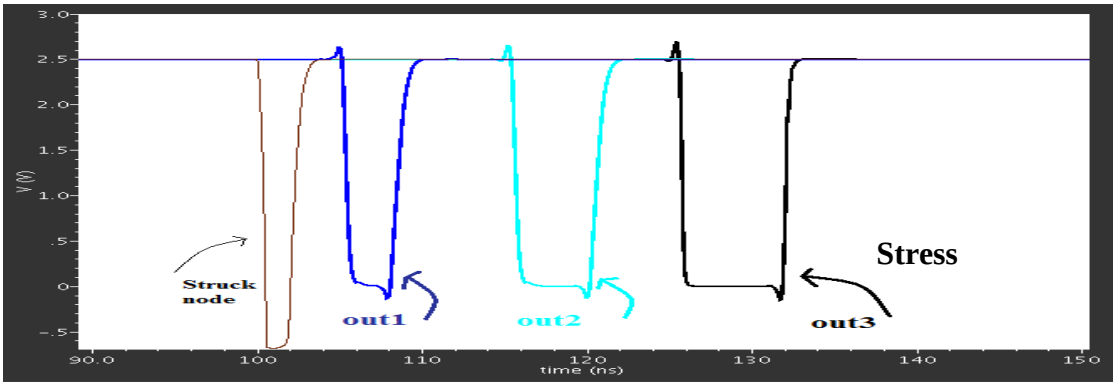


Figure 45(b): SET Pulse Broadening with Stress

CHAPTER 6

CONCLUSION

Negative bias temperature instability (NBTI) is a serious problem in PMOS transistors. The defects caused by the gate stress and elevated temperatures should be considered in the circuit simulations. But the defects change with time and they are not constant, so it is very hard for the designer to include the defects every time. So in this work a model is developed to which the inputs are the maximum value of the density of interface traps and oxide traps. The model generates a defect potential which is exactly the change is threshold voltage caused by the defects. The defects are gate voltage and time dependent.

The MOSFET Sub-threshold current method is used to evaluate the interface traps and oxide traps in PMOS transistor. The degradation model in modeled in cadence and validated the same with the simulations in Silvaco. The current-voltage curves in both cadence and Silvaco are compared and both the results fit each other. A shift is observed in the threshold voltage when the degradation model is introduced which is obvious as the shift is caused by the interface traps and the oxide traps. The simulation results produced by the model discussed in this work are compared to various other results by other authors. The same methodology is replicated for NMOS transistor and a degradation model is developed for NMOS transistor. After the device level simulations, the degradation models were introduced at the gate terminal of PMOS and NMOS in an inverter. The threshold voltage degradation is very less for a NMOS transistor. A ring oscillator circuit of 5 inverters chain is designed and the frequency of the ring oscillator is observed with and without stress. The frequency of

ring oscillator is decreased by applying stress which is because of the increase in threshold voltage and hence increase in gate delay. The V_t only model result is also compared with that of the defects model. There is a change is frequency in both the models. The V_t only model doesn't include the gate voltage dependency in the subtreshold region. The model is also used to see the single event transient pulse broadening and it gave a satisfactory result as observed by some authors.

This model captures transistor response using fixed trapped charge (N_{ot}) and interface traps densities (D_{it}) as the input parameters. The model is external to the transistor, thus easily implemented with time and bias dependence but without modifications to compact model. This is very advantageous to the designers.

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APPENDIX A

TCAD CODE

```
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# D is Niti/.023 where .023 eV = phiB/20 and PhiB=.46 for the nmos2 str

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mesh inf=pmos_tsmc.str

model print SURFMOB

material region=1 eg300=1.12 nc300=3.2e19 nv300=2e19 mun=455.3
mup=158.7 permittivity=11.7 affinity=4.05 taun0=1 taup0=1

contact name=source neutral

contact name=drain neutral

contact name=gate workfun=5.17

interface qf=$Not

method 2nd tol.time=1e-6

output con.band val.band band.params charge

solve init

save outf=pmos_0V_$"Not"_$"Niti".str

# save structure for off state Vds=50mV

solve vdrain=-0.05 name=drain

save outf=pmos_sd_p05V_$"Not"_$"Niti".str

solve vgate=0

# save IV for dc Id-Vgs linear response

log outf=T_PMOS_1pe12_1e12.log

solve vgate=0 vstep=-0.1 vfinal=-2.5 name=gate

# save structure for strong-inv, linear Vds=50mV

save outf=pmos_tsmc_2p5.str

quit
```