Output Bandwidth Limitations of Basestation Power Amplifier Design and Its Implementation Using Doherty Amplifier

by

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ABSTRACT

This thesis is a study of Bandwidth limitation of basestation power amplifier and its Doherty application. Fundamentally, bandwidth of a power amplifier (PA) is limited by both its input and output prematch networks and its Doherty architecture, specifically the impedance inverter between the main and auxiliary amplifier. In this study, only the output prematch network and the Doherty architecture follows are being investigated. A new proposed impedance inverter in the Doherty architecture exhibits an extended bandwidth compared to traditional quarterwave line.

Base on the loadline analysis, output impedance of the power amplifier can be represented by a loadline resistor and an output shunt capacitor. Base on this simple model, the maximum allowed bandwidth of the output impedance of the power amplifier can be estimated using the Bode-Fano method. However, since power amplifier is in fact nonlinear, harmonic balance simulation is used to loadpull the device across a broad range of frequencies. Base on the simulated large signal impedance at maximum power, the prematch circuitry can be designed. On a system level, the prematch power amplifier is used in Doherty amplifier. Two different prematch circuitries, T- section and shunt L methods are investigated along with their comparison in the Doherty architecture at both back off power and peak power condition. The last section of the thesis will be incorporating the proposed impedance inverter structure between the main and auxiliary amplifiers.

The simulated results showed the shunt L prematch topology has the least impedance dispersion across frequency. Along with the new impedance inverter structure, the 65% efficiency bandwidth improves by 50% compared to the original impedance inverter structure at back off power level.

ACKNOWLEDGEMENTS

I would like to thank professor George Pan, who given me the opportunity to work on this thesis. He was a mentor not only with the work involved with in this thesis, but also guidance during many stressful moments in both work and school. Many encouragements was given by professor Pan when things did not seem to be working out by joggling between family, work, and school. I am also grateful to his patient and tolerance in making the completion of this degree possible.

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Thirdly, I would also like to thank my managers in various stages during the pursuing of this degree. Their understanding of the loads of school works and allowing flexible schedule to attend the classes at ASU make the completion of this degree possible.

I would also like to thank my dear wife for the completion of this thesis. During the five years of the master program, she gave birth to our two daughters and bears a tremendous load of responsibility in raising the children and taking care of her husband while he is occupied at work and with school. Her patients and forbearance displayed goes beyond words can described.

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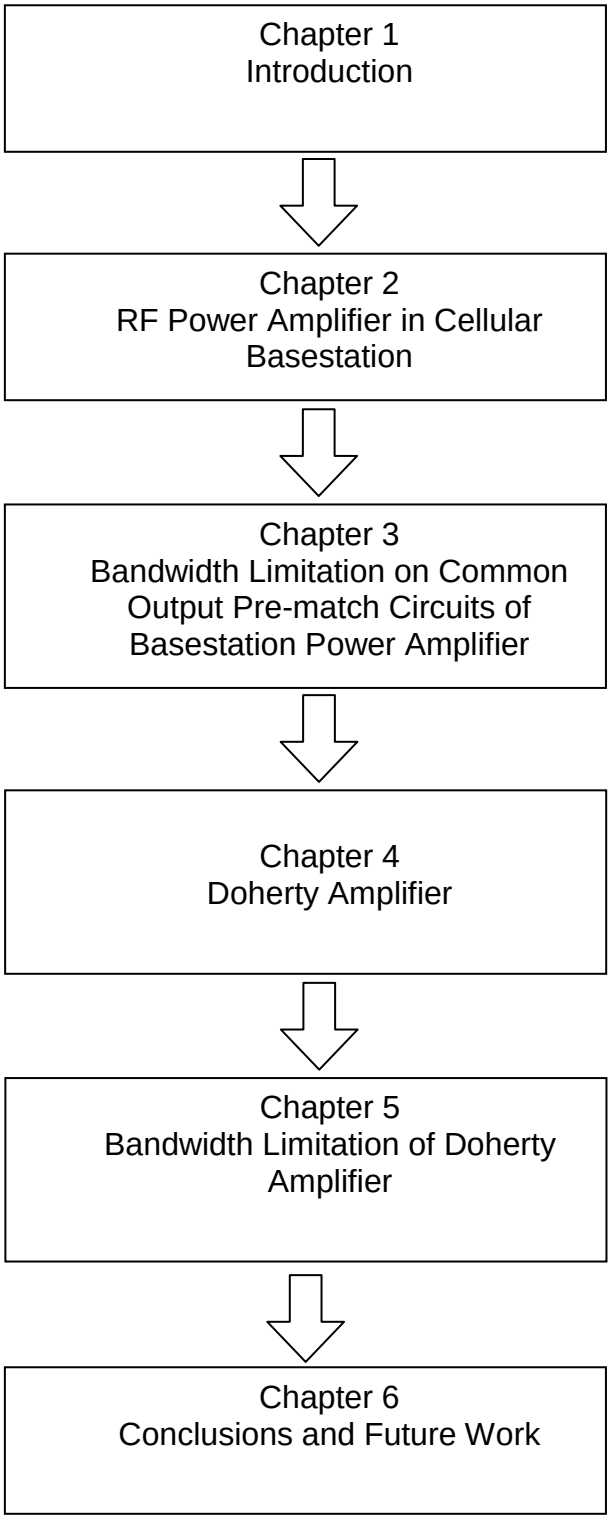
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Chapter 1

Introduction

1.1 Cellular base station

A cellular base station is a wireless system allows communication between cellular to cellular or cellular to traditional land line. The antenna of the base station is mounted on top of the station tower to maximize radio transmission range to the cellular users on the ground.[1]

Figure 1.1 Cellular Base Station Tower.

Base station can be categorized by its coverage radius. Larger coverage radius requires higher output RF power level.

Base Station Type	Typical Coverage Radius	Typical Use
Femtocell	10 m	Home or office use
Domestic Repeater	100 m	Home, office or factory use
Picocell	200 m	High rise building, hotel or car park use
Microcell	1-2 km	Shopping centers, city block.
Macrocell	5-32 km	Suburban, city and rural use

Figure 1.2: Coverage Radius of Different Type of Base Station Tower.

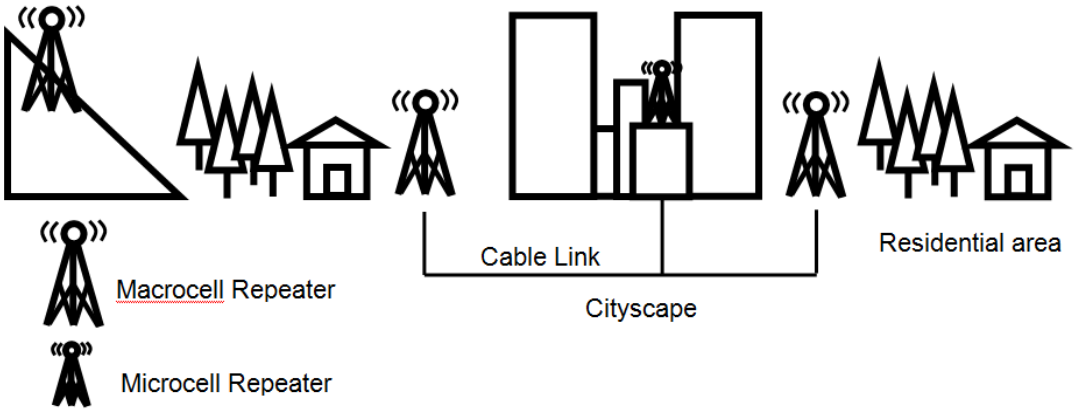

Figure 1.3: Base Stations – Cellular Coverage.

Base station tower has been evolved in the recent year in order to reduce power consumption by the long RF feeder cable to the passive antenna. The figure below gives a description of how each configuration evolves and their change in configuration. RRH stands for remote radio head where the RF circuitry is placed next to the cellular antenna.

BTS Types	Description
Ground based BTS	Historical BTS where all electronics including RF PA's & LNA are ground based with long RF feeder cables to passive antenna.
Distributed BTS	Better known as RRH (Remote Radio Head) where all of the digital electronics are ground based but run fiber cables to RF RRH where the small signal, LNA, PA are mounted in close proximity to the antenna.
Compact BTS	Known as a small cell AiO (All in One) unit. Where all essential functions of the BTS are included in a very small enclosure (~5L). Small cell AiO include digital functions (Layer 1 & 2 call processing), small signal RF, PA, LNA, WiFi, ect.

Figure 1.4: Different BTS Types as They Evolve and Their Description.

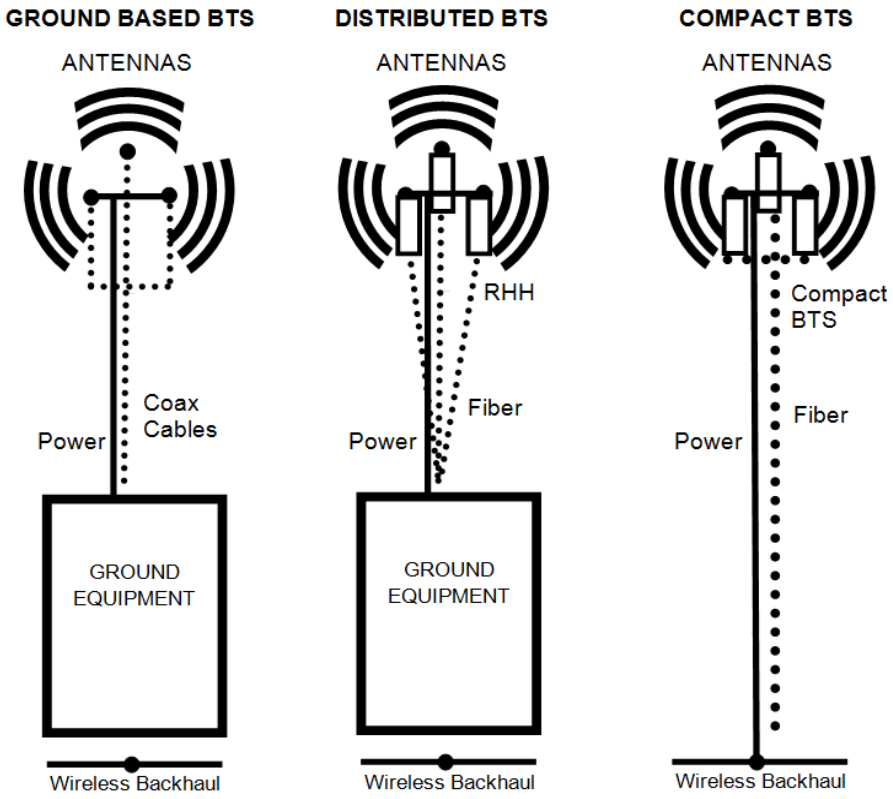

Figure 1.5: Base Station Tower Evolution.

In the distrusted BTS, the RF and digital system are separated in order to reduce transmission loss from ground equipment to antenna on the top of the tower. The RF transmitter is mounted right next to the antenna, where the digital signal is being fed from the ground equipment. The traditional ground based equipment requires larger power amplifier in order to overcome the loss associates with coax cable, which are typically around 3 dB. By mounting the RF transmitter on the top of the tower will reduce the size of the power amplifier in half. However, one need to taking into consideration the cooling of the RF power amplifier. On top of the tower, wind is usually the main source of cooling to the RF power amplifier. As the heat builds up, the efficiency of the amplifier degrades significantly.

As the global population urbanized over the recent decades, especially in developing countries [2], the demands of cellular usage also increase. As population density increase in a given area,

single cellular base station will not be unable to meet the demand of the overwhelming cellular users per coverage area. In the following figure, an illustration of cellular coverage of base station towers is shown.

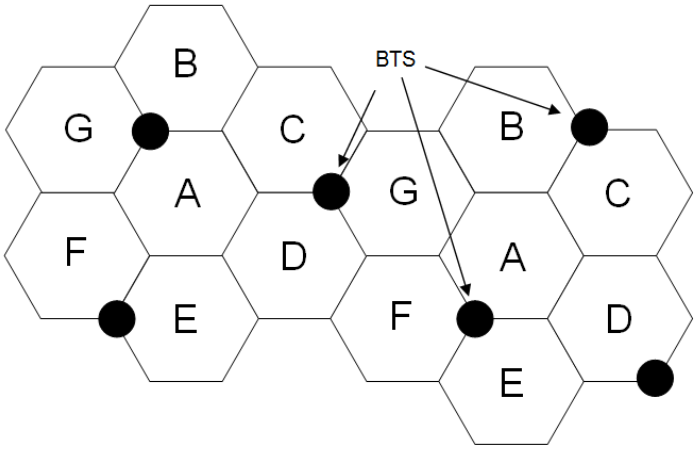

Figure 1.6: Cellular Coverage of Base Station Towers.

From figure 1.6, the BTSs are placed at the conjunction of cell grids. As the users increases, the BTS's user capacity increases and some of the users will begin to experience call drops. This phenomenon is more severe at the juncture where there is no BST. One of the solutions is to place compact BTS in the empty nodes as shown below.

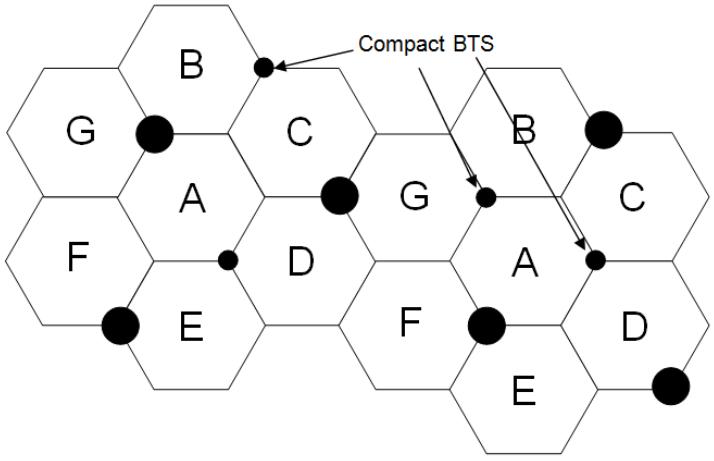

Figure 1.7: Additional Compact BTS for Coverage Improvement.

In the base station equipment, there exists a complete wireless communication transceiver shown below.[3]

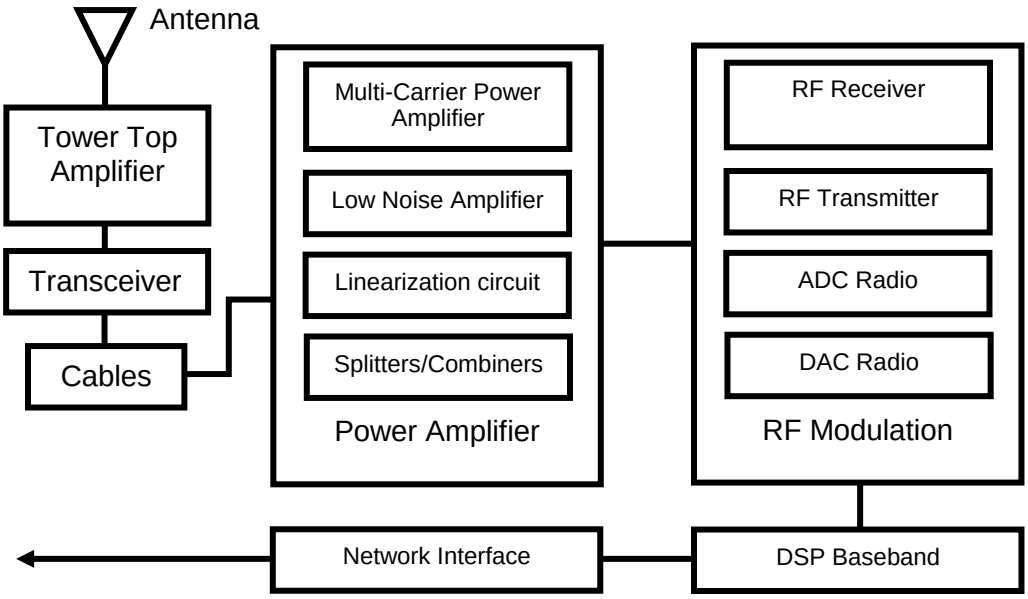

Figure 1.8: Block Diagram of a Typical Base Station.

1.2 Frequency Bandwidth

After the introduction of iphone in 2007, cellular industry sees its data traffic doubling year over year. The traffic of voice and data usage is displayed in below figure.[4]

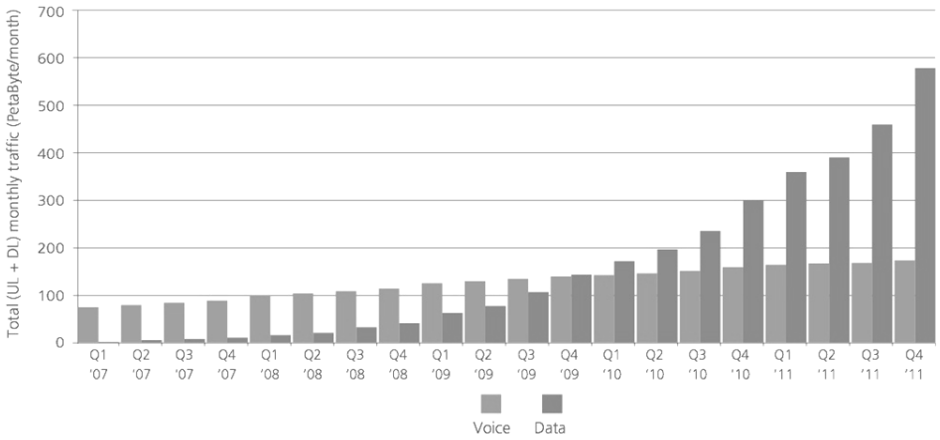

Figure 1.9: Total Monthly Mobile Voice and Data as Measured by Ericsson From 2007 to 2011.

The trend of usage of smart phone along with its data hogging nature forces cellular basestation provider to develop more sophisticated hardware to linearize modulated signal with high peak-to-average power ratio(PAPR). This linearization technique is applied through Digital Pre-Distortion(DPD) scheme, which is simply a feedback network between the output of a power amplifier to its baseband through demodulation and analog to digital convertor. A pre-distorted signal is then feed back into the power amplifier.

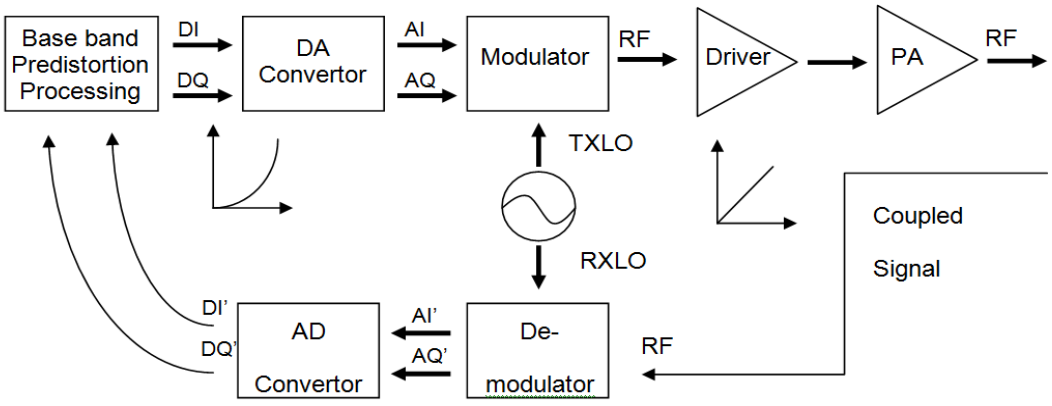

Figure 1.10: Base Station Digital Predistortion Diagram.

In order to properly distort or “correct” the level nonlinearity in the amplifier’s signal, a fifth order correction is often required for the DPD system to process and re-input pre-distorted signal to linearize the PA. This means the captured bandwidth needs to be in the order five times greater than the input signal bandwidth. For the 4G LTE advance platform, this means while the input signal is 100MHz, the required output bandwidth needed for DPD correction is 500MHz. [5][6]

1.3 Device technology use in power amplifier

Below is a figure showing the different device technologies that are being used in power amplifier designs according to their frequency range and power rating. Currently LDMOS, lateral diffused mosfet, is still the dominate device architecture being employed in basestation amplifier

industry today. [7] However, Gallium Nitride has been gaining traction in the base station amplifier due to its high power density and capability to operate at higher frequency.

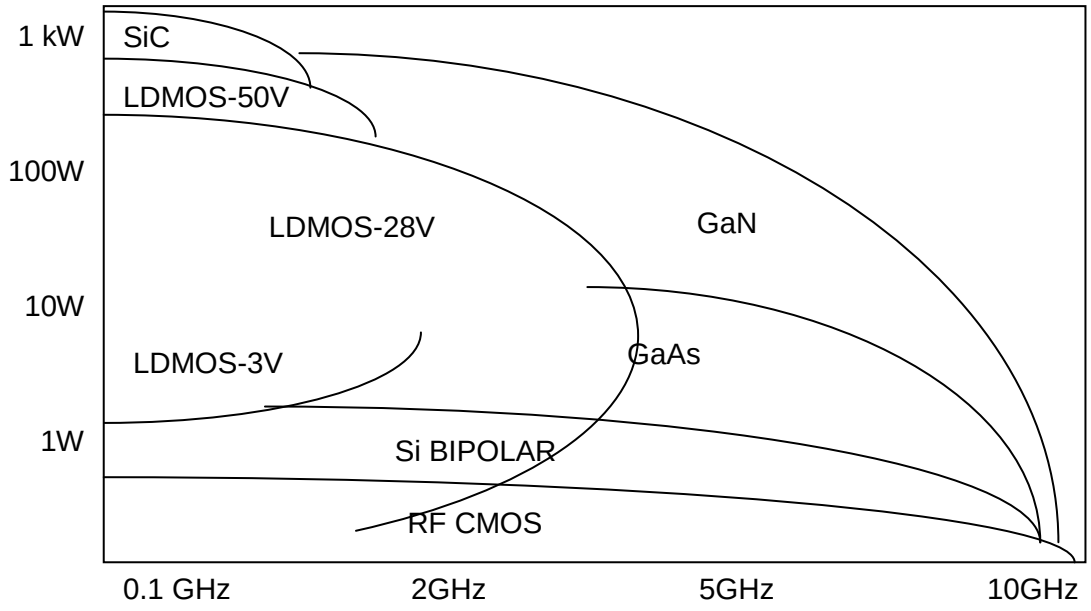

Figure 1.11: Device Technology Used in Various Power Application and Frequency Spectrum.

Chapter 2

RF Power Amplifier Design in Cellular Basestation

2.1 Device technology used in cellular base station amplifier

Before mid-1990s, the cellular base station power amplifier used bipolar transistor or gallium arsenide MESFETs for power amplification from sub GHz to 1~2 GHz. The main challenge of implementing the amplifier with silicon mosfet resides within the power dissipation through the silicon substrate and the large breakdown voltage requirement of base station power amplifier. For heat dissipation, additional ground wires are added to the source or emitter to prevent the amplifier from overheating. It wasn't until the mid 1900, RF device engineer begin explore the possibility of implementing base station amplifier in silicon substrate.[3]

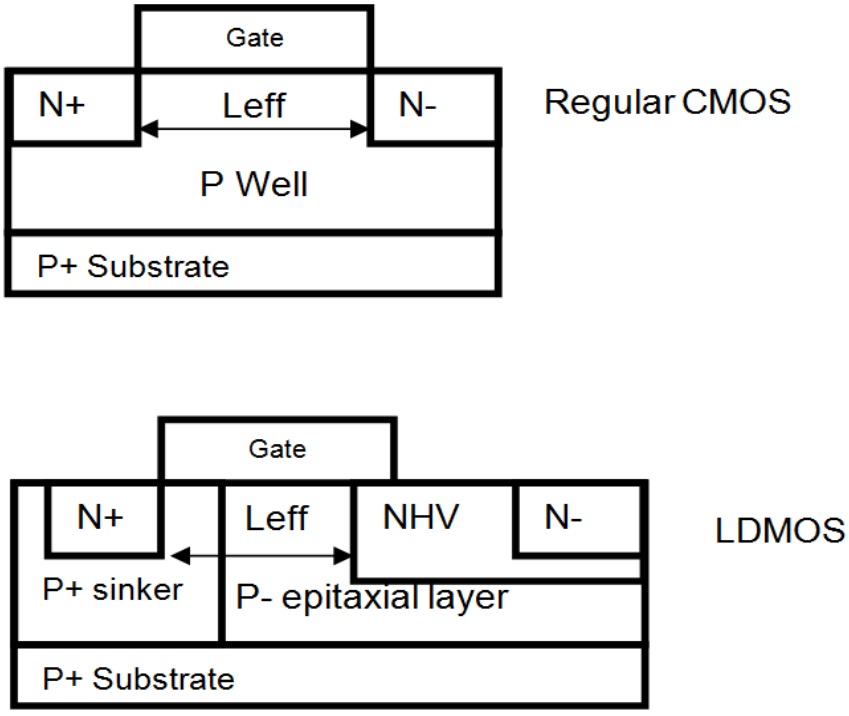

Figure 2.1: Comparison Between Regular CMOS and Laterial-Diffused MOSFETs .

The key distinguishment of lateral-diffused MOSEFET compared to a regular CMOS is the addition of NHV, which is a lightly doped drain region between the gate and the drain terminal of

MOSFET. The NHV enables high voltage operation of the power amplifier and also increase the breakdown voltage of the transistor (75-80 Volt). In order to avoid using bondwire for heat dissipation, a P+ sinker acts as a low loss conductor connecting the back metal ground source to the source terminal of the MOSFET itself. This greatly reduce the complexity of semiconductor fabrication process, which translates to lower cost and it also enable more integration by removing the ground wires that were required for heat dissipation purpose.

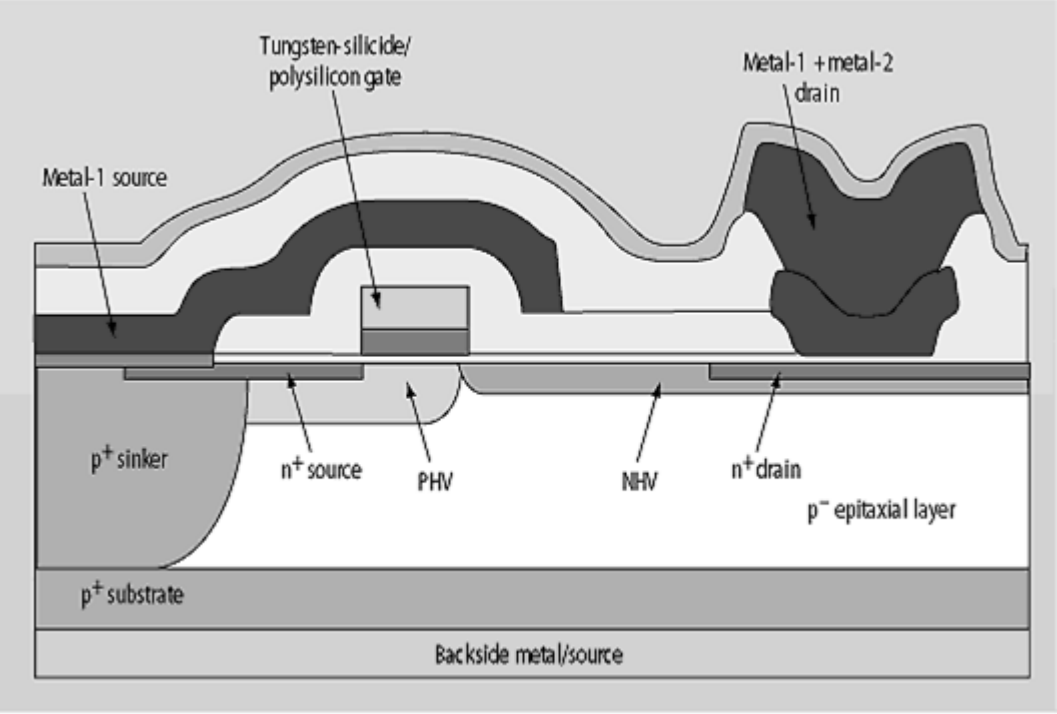

Figure 2.2: Freescale's(Ex Motorola's Semiconductor Sector) Fifth-Generation Process, HV5.[8]

A further detail of the LDMOS structure is shown in figure 2.2. The metal 1 faraday shields over the gate structure prevents the forming of high electric field at the gate edge, which causes change in the threshold voltage of the device over time. The shield is grounded to the source through the P plus sinker, prevents the coupling between the gate edge and the drain potential. Lastly, it reduces the feedback capacitance, Cgd, which is the main cause of RF leakage from the drain to the gate.

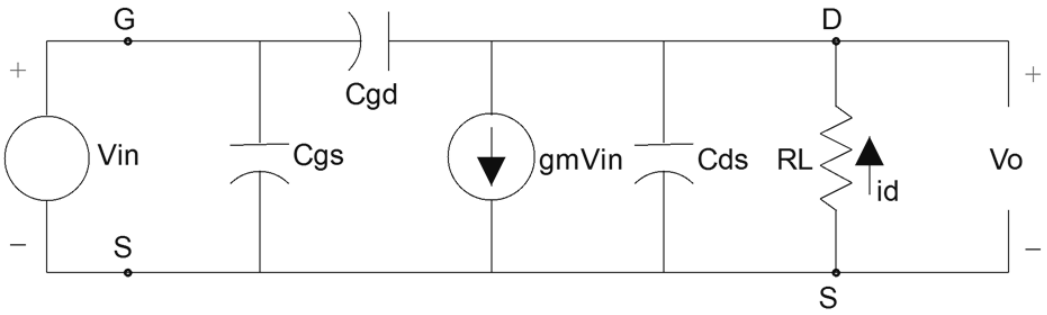

Figure 2.3: Equivalent Circuit for a MOSFET/LDMOS Including Feedback Capacitance.

2.2 Class of operation of power amplifier

Depending on the application of power amplifier, different classes of operation have been designated base on the conduction angle of the output current. By changing the bias current of the amplifier, the different class of amplifier operation can be categorized as followed

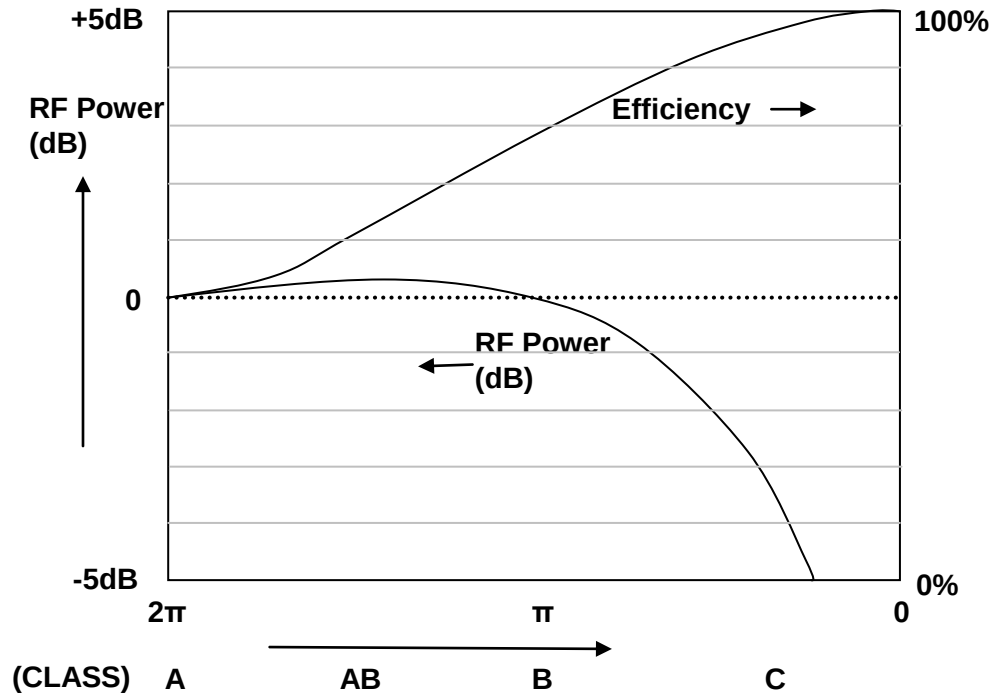

Figure 2.4: RF Power and Efficiency as a Function of Conduction Angle; Optimum Load and Harmonic Short Assumed.

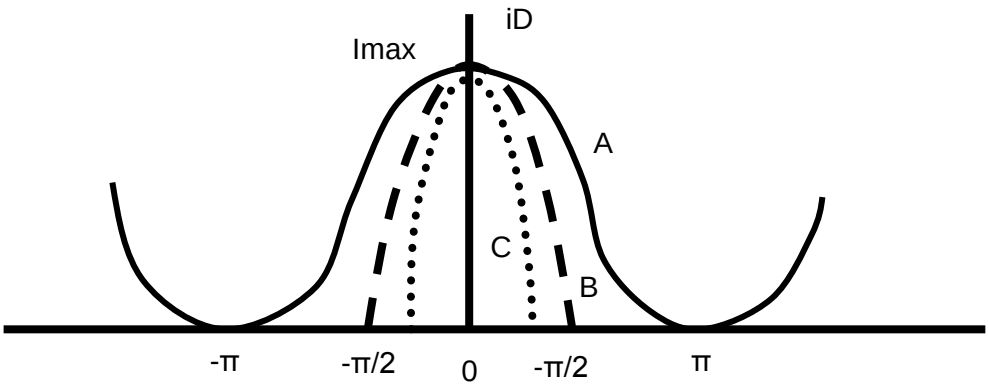

Figure 2.5: Class of Operation Represented by Current Conduction Angle.

In the class A amplifier, the conduction angle is the greatest which results in worst effinciency. However because there is no clipping in the RF current swing, the linearity of the class A amplifier has the best linear performance which is ideal in a driver amplifier design. A driver amplifier provides the gain needed before the RF signal enters into the high power amplifier

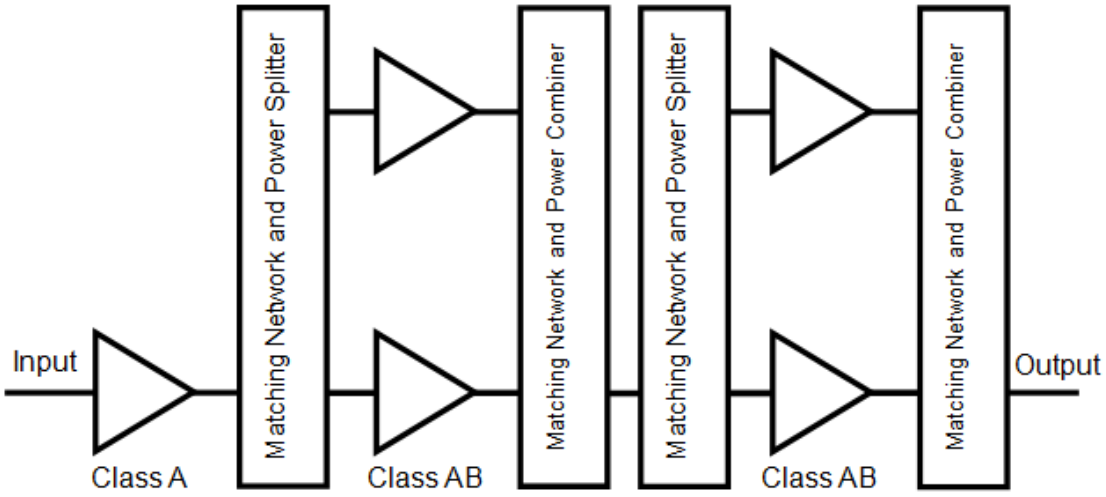

Figure 2.6: Multi-Stage Power Ampflier.

In the earlier generation of cellular network, class AB amplifiers were used for effinciency improvement due to reduction in conduction angel. Further effieciency improvement can be

achieve if conduction angle of current continue to decrease; however, amplifier linearity will suffer. The current cellular network uses both class AB and class C amplifier to create the Doherty amplifier, which will be discussed next.

2.3 RF Power Amplifier and Doherty Topology for Basestation application

RF power amplifier is a key component in wireless communication system, especially for the cellular basestation. Linearity and efficiency are the two crucial design criteria because of signal integrity and energy conservation. As the input signal drive increases, the amplifier enters into compression where the output voltage waveform starts to clip due to the limitation of the device. The voltage waveform is bounded on its lower limits by the knee voltage and its upper limits by twice of the drain voltage supply. The amplifier current is limited by maximum current of device. Figure 2.8 and 2.9 shows boundary limits of both voltage and current as input power drive increase and enters compression.

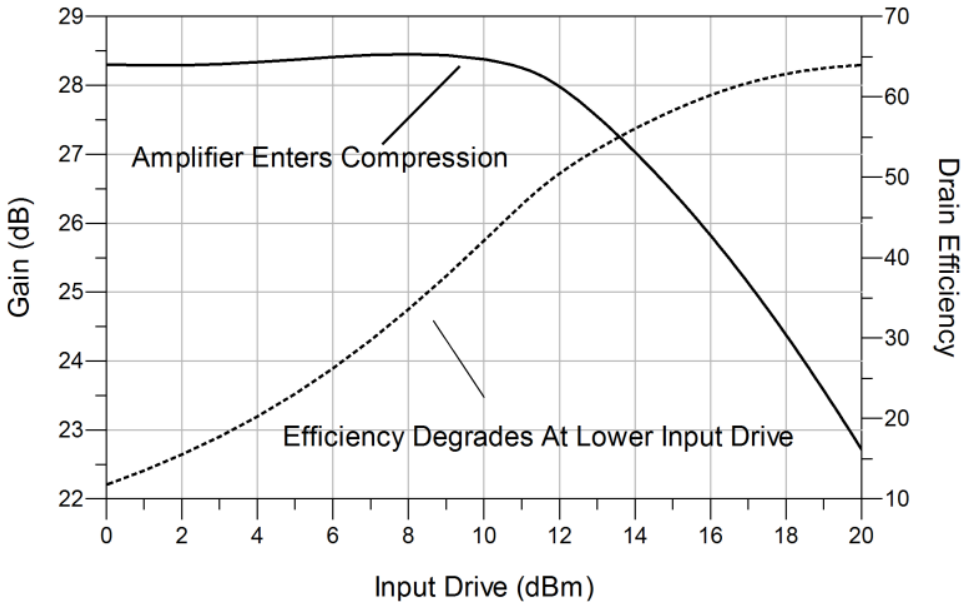

Figure 2.7: Gain and Efficiency of PA Over Input Drive.

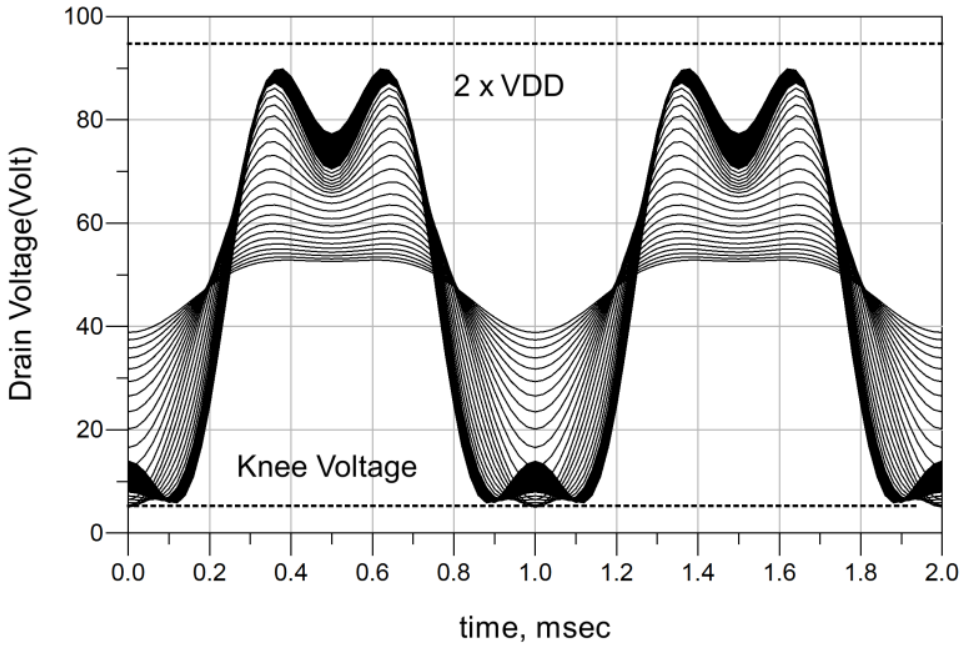

Figure 2.8: Output Voltage Waveform of PA Over Input Drive.

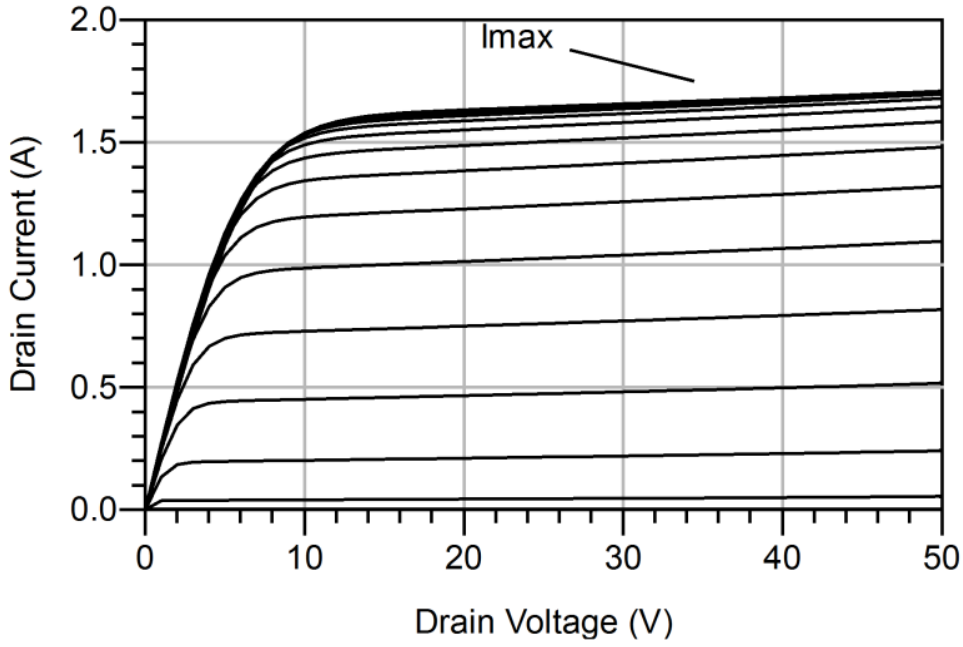

Figure 2.9: DC Current and Voltage Characteristic of PA.

If the input power drive continues to increase which translates to high output voltage swing, the device will experience catastrophic failure beyond breakdown voltage. Although the

device compressing region yield better efficiency, the linearity becomes worst due to harmonic content generated by the amplifier as shown in figure 2.10 and figure 2.11. The design criterion is often met be trading off between linearity and the efficiency of the power amplifier.

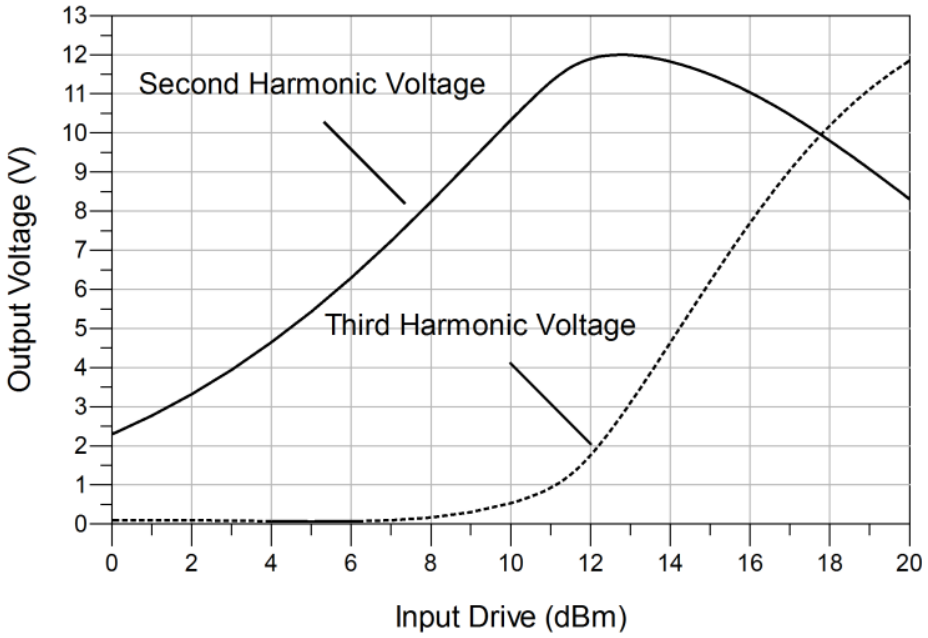

Figure 2.10: Harmonic Voltage of Power Amplifier.

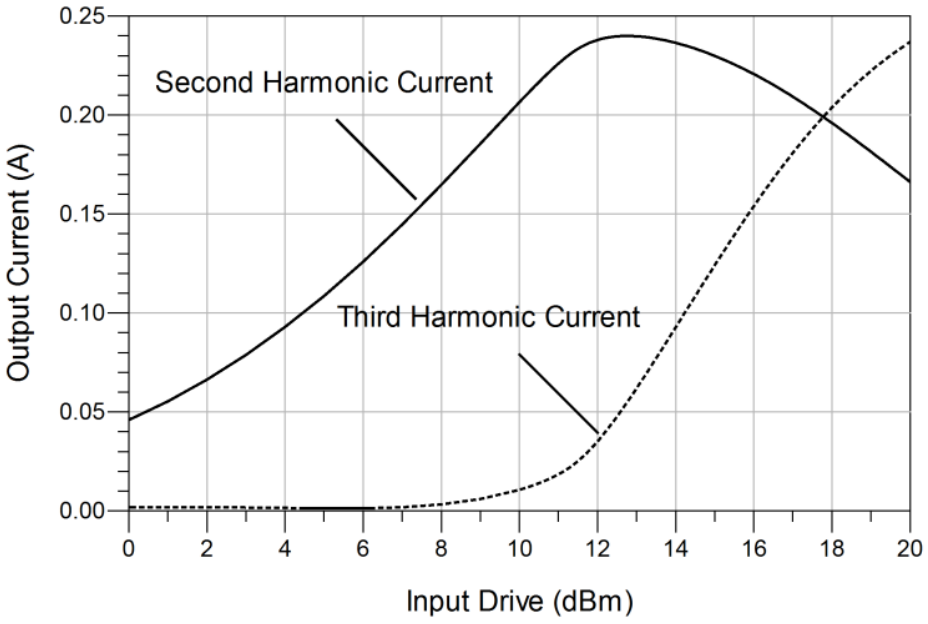

Figure 2.11: Harmonic Current of Power Amplifier.

In order to solve the dilemma on tradeoff between efficiency and linearity in basestation amplifier performance, Doherty amplifier was introduced to provide higher efficiency at lower input drive level while maintaining the linearity of the device [11]. In figure 2.12, the Doherty amplifier consists of two amplifiers operates at 90 degrees phase shift on both the input and output of its topology.

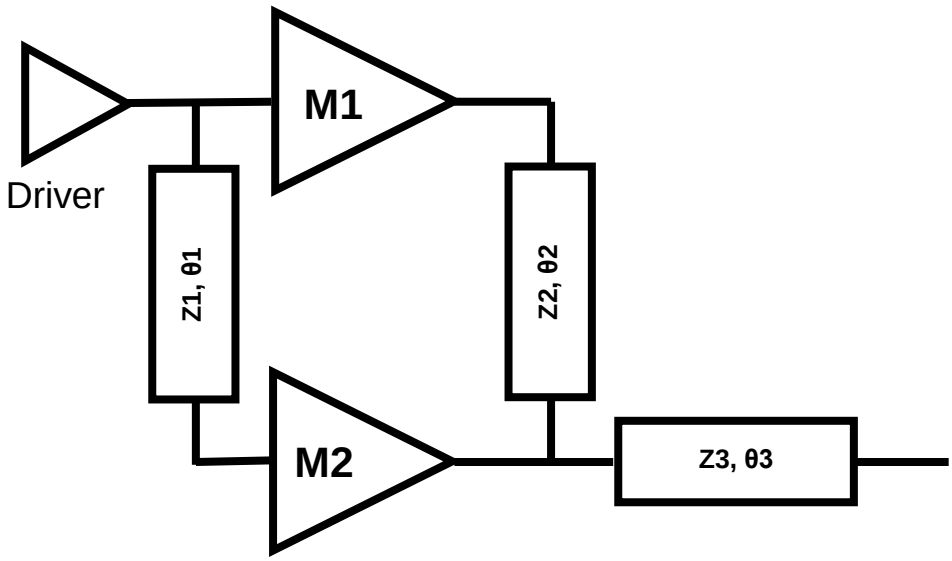

Figure 2.12: Doherty Amplifier.

The main amplifier, M1, provides the high efficiency is needed at back off power level where linearity is good. The peaking amplifier, M2, is biased slightly above threshold and it is technically “off” when M1 is operating at the average power of the high peak to average modulation signal output. As M1 enter into compression, M2 then slowly turns on to provide the power that is needed in order to sustain the peak of the modulation signal output. Figure 2.13 depicts the overall operation of M1 and M2 over input drive. Today, Doherty amplifier architecture is the most common design for basestation amplifier. More details of Doherty amplifier will be discussed in chapter 4 of this thesis.

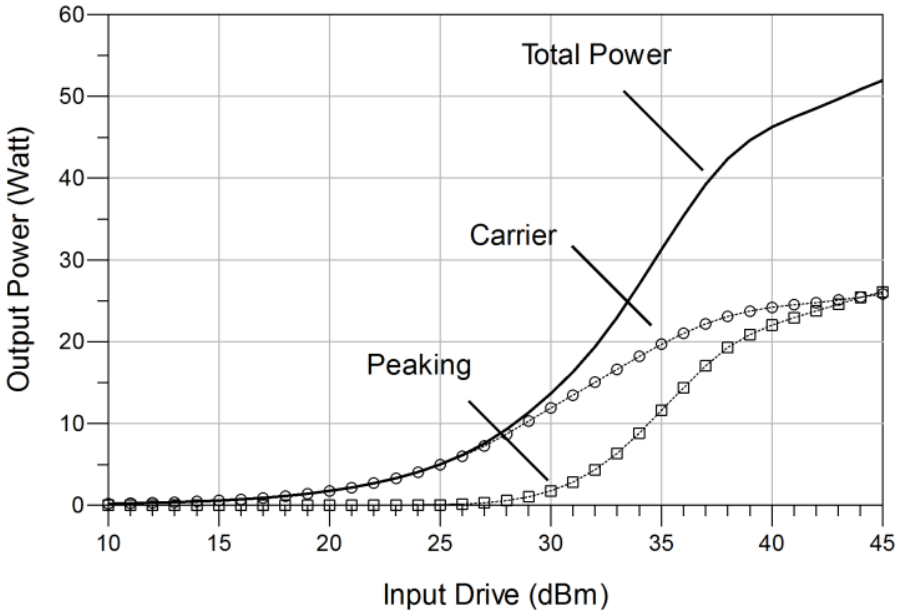

Figure 2.13: Doherty Power Output Vs Input Power.

2.4 Design process

In order to understand the involvement in power amplifier design, one needs to gain an insight in its design process from the beginning. Before any device is fabricated, the physical structure of device needs to be first model by TCAD, Technology Computer Aided Design, such as Synopsys[9]. Parameters of the device are review and set base on the demands from cellular basestation market. When the devices are fabricated base on the specifications, the device characteristic will be extracted using a small periphery device through techniques described in [10]. These extracted device parameters are feed in order to create compact model used by the PA designers. A flowchart of PA design process is shown in figure 2.14.

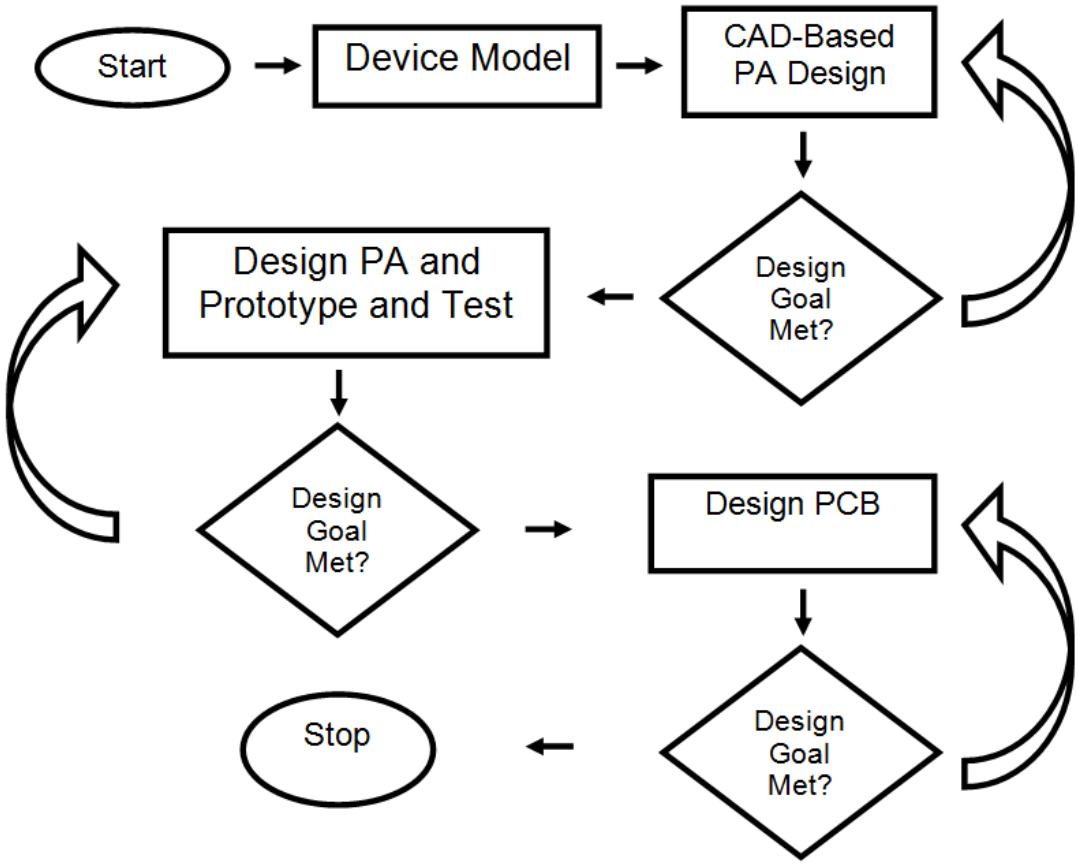

Figure 2.14: PA Design Flow Chart.

2.2 Loadline theory and its application in power amplifier design

Before the introduction of accurate compact model, in order to design the impedance matching for the output impedance of RF amplifier, an alternative design approach was proposed in 1983[11]. In the proposal, it states that the first order approximation of amplifier's output impedance of maximum deliver power can be calculated from loadline method. The loadline resistor of the power match condition has a value of

$$Ropt = Vds/(\frac{Imax}{2}) \quad (2.1)$$

If the knee voltage, Vknee, is considered, then

$$Ropt = (Vds - Vknee)/(\frac{Imax}{2}) \quad (2.2)$$

If the output power is known, then

$$Ropt = \frac{(Vds-Vknee)^2}{2*Pout} \quad (2.3)$$

For instant, Freescale's AFV09P350 basestation power amplifier has a Drain voltage of 48 Volts, Knee Voltage of 3 Volts, and 274 Watt output power, so Ropt can be calculated using the above formula

$$Ropt = \frac{(48-3)^2}{2*274} \cong 3.69\Omega \quad (2.4)$$

If the output capacitance of the transistor is known, one then can reach a relative accurate linear approximation of device's output impedance.

$$Zout = Ropt + J * Xc \quad (2.5)$$

Where Xc is the output parasitic capacitance of the amplifier, which can be obtained through measurement.

2.3 Loadpull simulation

In order to acquire more accurate output impedance, loadpull measurement is used to determine the terminal impedance of the amplifier for max power transfer [13]. Designers can validate the accuracy of the loadpull measured result with the calculated output impedance obtained from previous section.

Using the previous Freescale's device, at 900MHz, the loadline theory approximates Zout to be 2.588-j*1.689, the actual loadpull data measured is displayed below,

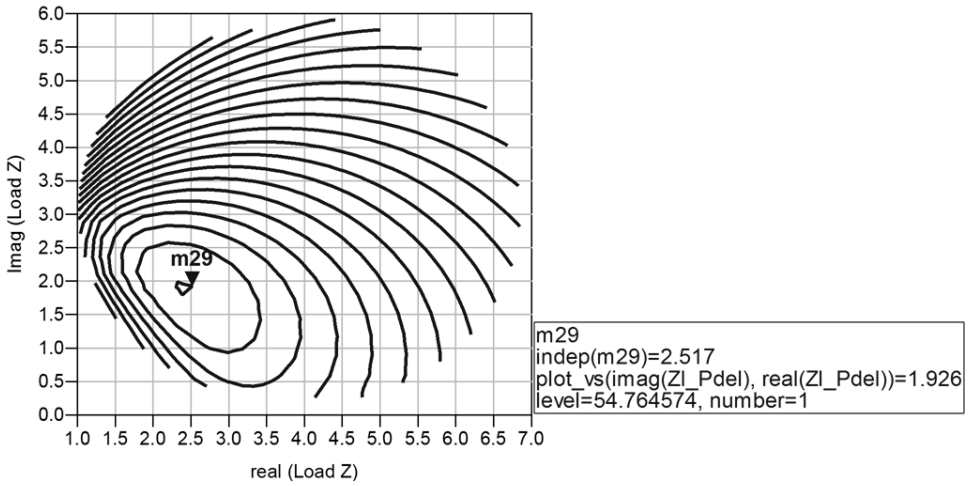

Figure 2.15: Simulated Loadpull Impedance of Freescale's AFV09P350 Basestation Power Amplifier.

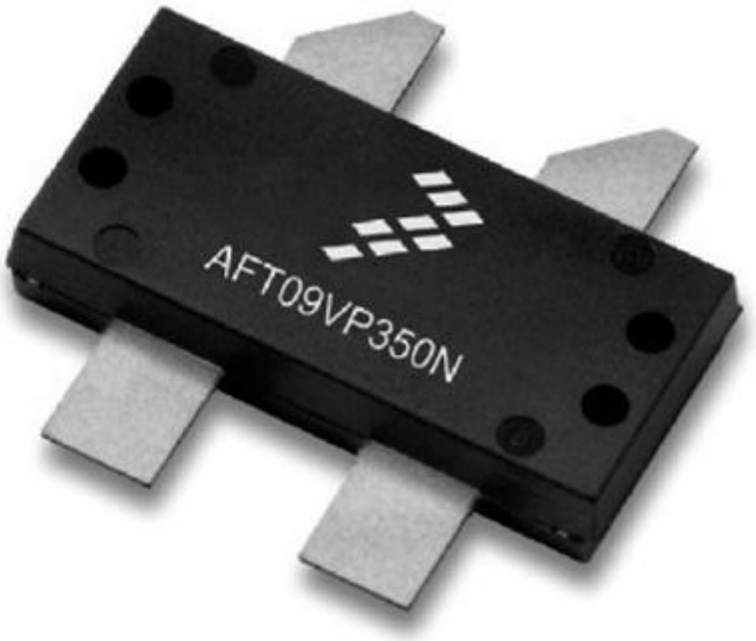

Figure 2.16: The 48 V AFT09VP350N.

Comparing the approximated impedance value with the result obtained through harmonic balance simulation, the loadline approximation is in good agreement with simulated result. Based on the information obtained, one can readily begin designing matching network for amplifier output.

2.4 Bandwidth limitation of transistor output

As the output capacitor varies with frequency, it places limitation on the maximum allow bandwidth on the power amplifier. The output of a FET transistor can be implemented with simple large signal circuit.

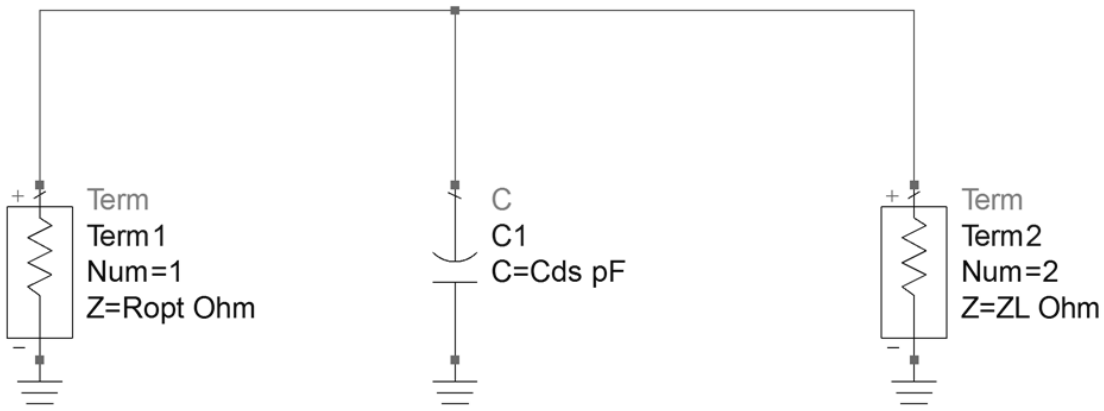

Figure 2.17: Output Circuit Implementation of Power Amplifier.

In a first glance, one can readily identify figure 10 is a parallel RC. To find the maximum allow bandwidth, Bode-Fano Criterion states its Bode-Fano limit is [12]

$$\int_0^\infty In\frac{1}{|\Gamma|}dw = \int_{\Delta w}\frac{1}{\Gamma_m}dw = \Delta w In\frac{1}{\Gamma_m} \leq \frac{\pi}{RC} \tag{2.6}$$

Where for a given R, C, and Γ_m , bandwidth Δw can be determined.

As the periphery of the device increases, the value of Ropt would decrease while Cds would increase. This results in further limitation on the bandwidth capacity of the device. In the effort of broadening the maximum bandwidth, device engineer endeavor their effort in either reducing the output parasitic capacitance of the device or increase the output voltage swing.

Chapter 3

Bandwidth Limitation on Common Output Pre-match Circuits of Basestation Power Amplifier

Base on the assessment made in previous chapter, output bandwidth limitation of power amplifier (PA) mainly comes from its parasitic capacitance and the allowed voltage swing on the drain termination of power PA. With high power application, large number of transistors, or transistor fingers, is required to deliver the power needed for cellular tower transmission. The output impedance of the device reduces as more transistors are being parallel connected as shown in figure 2.1.

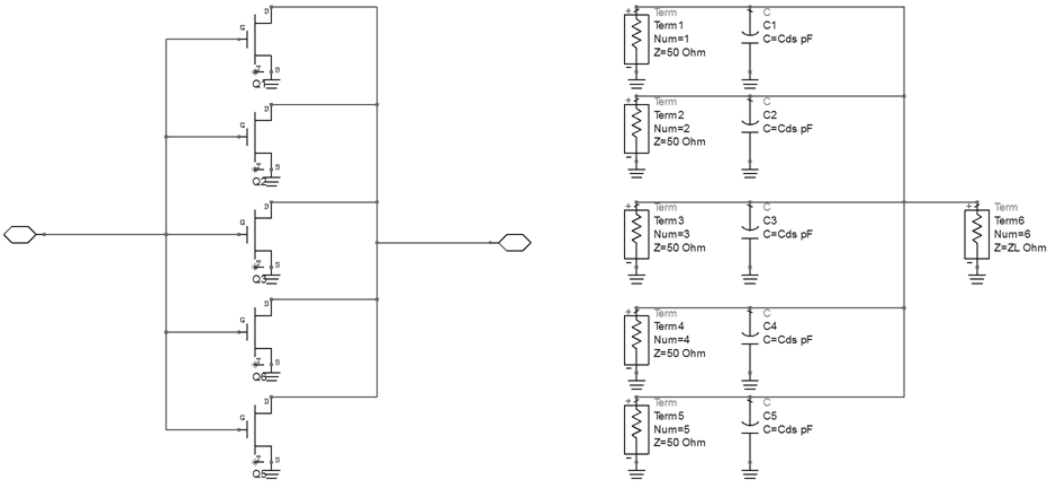

Figure 3.1: Parallel Connected Transistors.

Due to the small output impedance, pre-matching circuits are needed in order raise the output impedance of PA. This enables the device efficiently transfer RF power to the outside world. Moreover, these pre-match circuits are usually constructed with the transistors inside a RF package.

Depending on the technology and size of the transistor, different output prematch circuitries are utilized by the designer for impedance matching. Some of the most common pre-math circuitries are shown in figure 3.2.

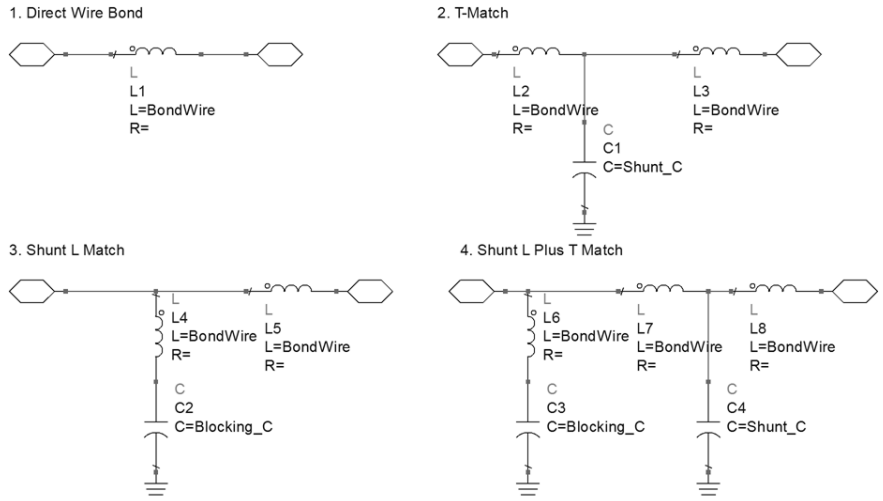

Figure 3.2: Common Prematch Circuitries.

Due to limited design space within package, pre-match circuit are usually consists of lump inductor and capacitor instead of distributed circuit element such as microstrip line. For lump inductor, bondwires are usually used due to its high quality factor which induces minimal loss.

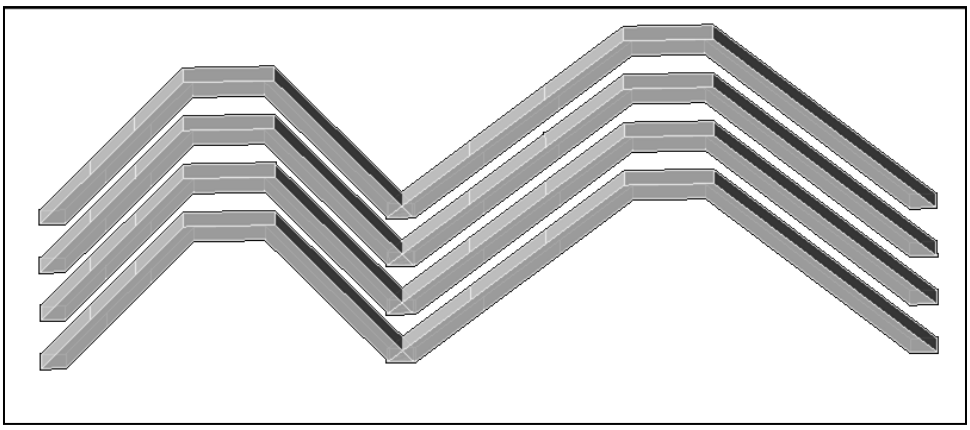

Figure 3.3: Bondwire Used Inside of RF Package.

The lump capacitors are either implemented with MOSCAP or integrated passive device.

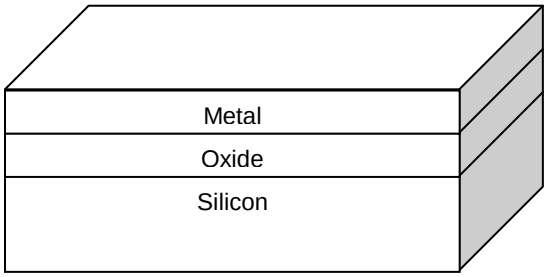

Figure 3.4: MOSCAP.

The next objective will be deriving the bandwidth capability of these pre-match circuitries. The package impedance will place limitation on the bandwidth that can be achieved by external PCB matching.

3.1 Direct Wire Bond

Depending on the device technology and device periphery size, sometimes direct wire bonds are sufficient to connect the transistor to the outside world with proper terminal impedance.

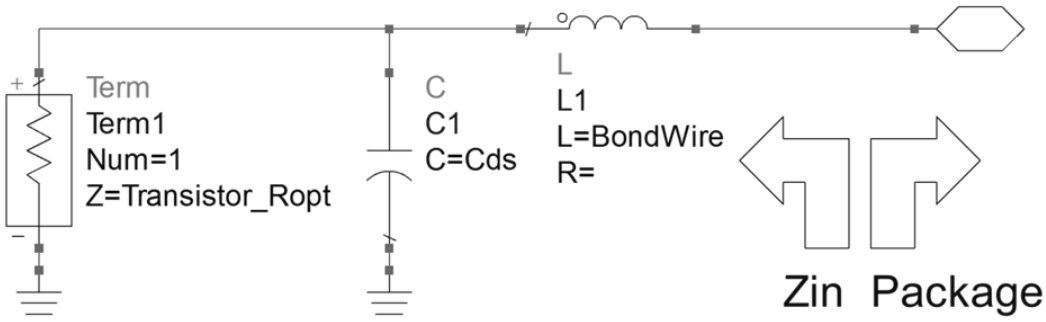

Figure 3.5: Direct Wirebond.

Along with output circuit of the transistor, the ABCD matrix can be written as follow:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & jwL \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwCds & 1 \end{bmatrix} \begin{bmatrix} I_2 * Ropt \\ I_2 \end{bmatrix} \quad (3.1)$$

After multiplication, Zin has the expression of

$$Zin\_DWB = \frac{R(1-w^2LC_{ds})+jwL}{R(jwC_{ds})+1} = \frac{R+jwL-w^2RLC_{ds}}{1+jwRC_{ds}} \quad (3.2)$$

The reflection coefficient is

$$\Gamma = \frac{Zin\_DWB-Zo}{Zin\_DWB+Zo} \quad (3.3)$$

The reflection coefficient magnitude is

$$|\Gamma| = \Gamma_m \quad (3.4)$$

The bandwidth can be found by

$$\Delta w \leq \frac{\pi}{RC} \times \left(In\frac{1}{\Gamma_m}\right)^{-1} \quad (3.5)$$

Simulated result is also shown,

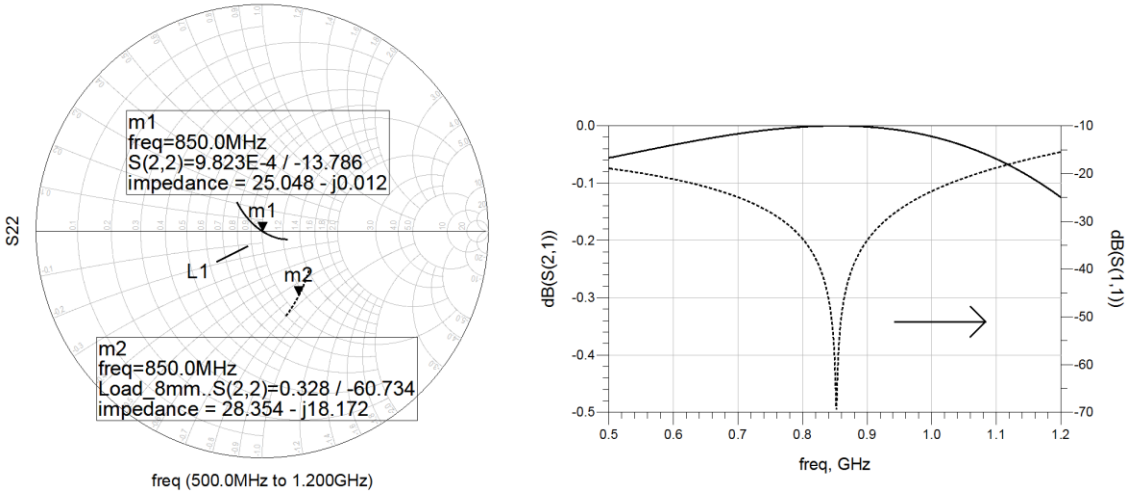

Figure 3.6: Simulated Result of Direct Wire Bond.

3.2 T-Math topology

T-match impedance transformation is considered a low pass topology. The transformation is mainly carried out by the first section inductor and shunt capacitor that follows. The advantage of using a T-match is that it can be treated as a lump equivalent of a transmission line which then be integrated with the microstrip outside of the package.

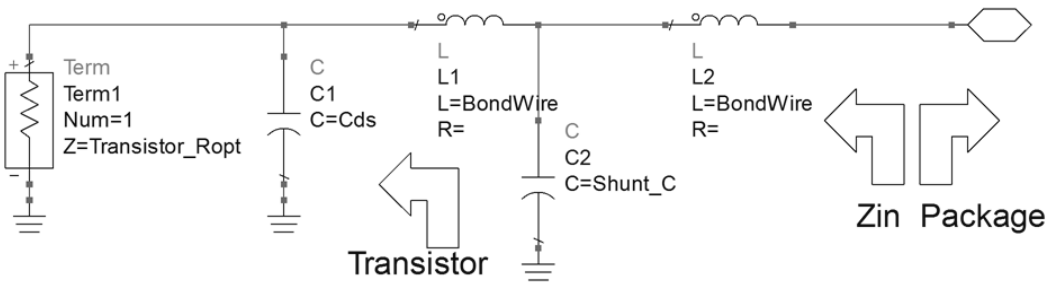

Figure 3.7: T Section Prematch Topology.

The ABCD matrix of the T match transformer along with the transistor can be written as follow:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & jwL_2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwC_{shnt} & 1 \end{bmatrix} \begin{bmatrix} 1 & jwL_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwC_{ds} & 1 \end{bmatrix} \begin{bmatrix} I_2 * Ropt \\ I_2 \end{bmatrix} \quad (3.6)$$

After multiplication, Zin has the expression of

$$Zin\_Tmatch = \frac{R_{opt}\left(1-w^2L_2C_{shnt}-w^2L_1C_{ds}\left(1-w^2L_2C_{shnt}\right)-w^2L_2C_{ds}\right)+jwL_1\left(1-w^2L_2C_{shnt}\right)+jwL_2}{R_{opt}*jw(C_{shnt}-w^2L_1C_{shnt}+C_{ds})-w^2L_1C_{shnt}+1} \quad (3.7)$$

The reflection coefficient is

$$\Gamma = \frac{Zin\_Tmatch-Zo}{Zin\_Tmatch+Zo} \quad (3.8)$$

The reflection coefficient magnitude is

$$|\Gamma| = \Gamma_m \quad (3.9)$$

The bandwidth can be found by

$$\Delta w \leq \frac{\pi}{RC} \times \left(In\frac{1}{\Gamma_m}\right)^{-1} \quad (3.10)$$

Simulated result is also shown,

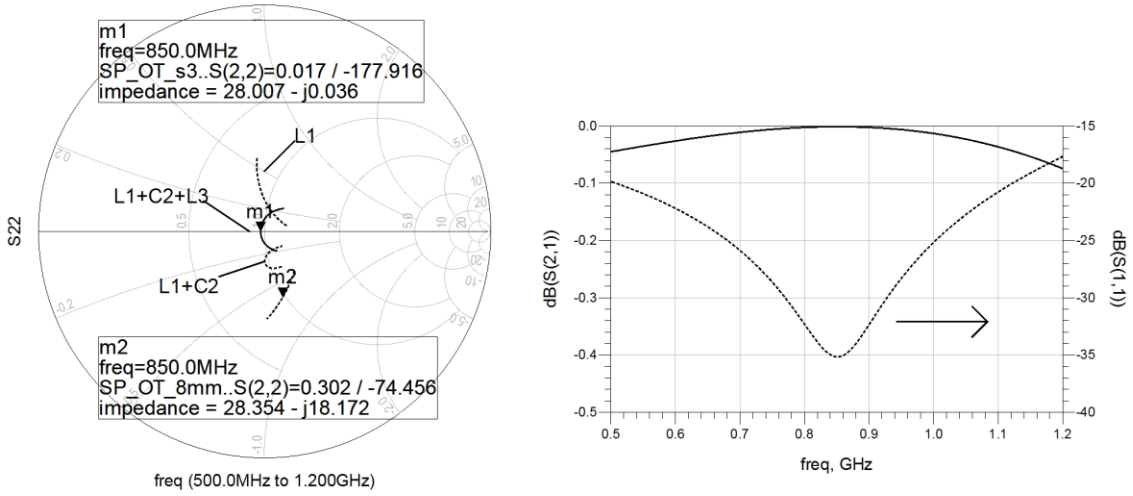

Figure 3.8: Simulated Result of T Section Match.

3.3 Shunt L topology

A shunt L impedance transformation is considered a high pass topology. The shunt L inductance cancels out the transistor's drain to source capacitance, thus raising the impedance level back to Ropt. The shunt inductor is connected to a blocking capacitor, which prevents shorting out the DC current and creates a open circuit at operating frequency.

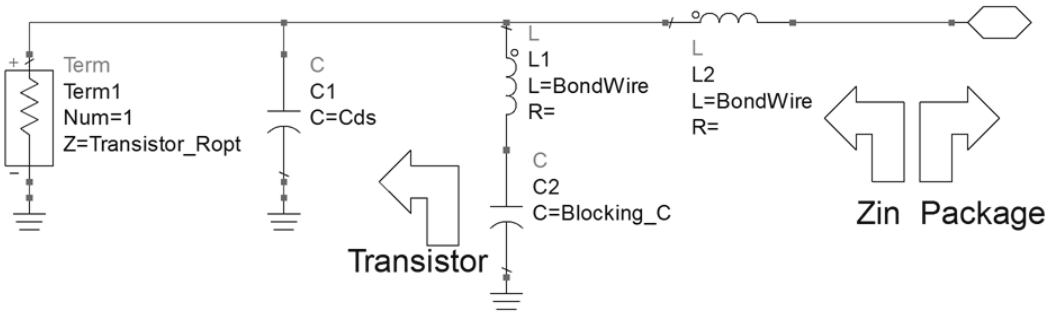

Figure 3.9: Shunt L Prematch Topology.

The ABCD matrix of the shunt L transformation along with the transistor can be written as follow:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & jwL_2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{jwC_{blk}}{-w^2 L_{sh} C_{blk}+1} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwC_{ds} & 1 \end{bmatrix} \begin{bmatrix} I_2 * Ropt \\ I_2 \end{bmatrix} \quad (3.11)$$

After multiplication, Zin has the expression of

$$Zin = \frac{R_{opt}\left(1-w^2 L_2 C_{blk} - w^2 L_1 C_{ds}\left(1-w^2 L_2 C_{blk}\right) - w^2 L_2 C_{ds}\right) + jwL_2}{R_{opt}\left(\frac{jwC_{blk}}{1-w^2 L_{shnt} C_{blk}} + jwC_{ds}\right)+1} \quad (3.12)$$

The blocking capacitor is usually a large capacitance value, thus the ABCD matrix can be simplified to be

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & jwL_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{jwL_{shnt}} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwC_{ds} & 1 \end{bmatrix} \begin{bmatrix} I_2 * Ropt \\ I_2 \end{bmatrix} \quad (3.13)$$

And the Zin has the expression of

$$Zin\_shuntL = \frac{R_{opt}\left(1-w^2 L_2 C_{blk} - w^2 L_1 C_{ds}\left(1-w^2 L_2 C_{blk}\right) - w^2 L_2 C_{ds}\right) + jwL_2}{R_{opt}\left(\frac{jwC_{blk}}{1-w^2 L_{shnt} C_{blk}} + jwC_{ds}\right)+1} \quad (3.14)$$

The reflection coefficient is

$$\Gamma = \frac{Zin\_shuntL - Zo}{Zin\_shuntL + Zo} \quad (3.15)$$

The reflection coefficient magnitude is

$$|\Gamma| = \Gamma_m \quad (3.16)$$

The bandwidth can be found by

$$\Delta w \leq \frac{\pi}{RC} \times \left(In \frac{1}{\Gamma_m}\right)^{-1} \quad (3.17)$$

Simulated result is also shown,

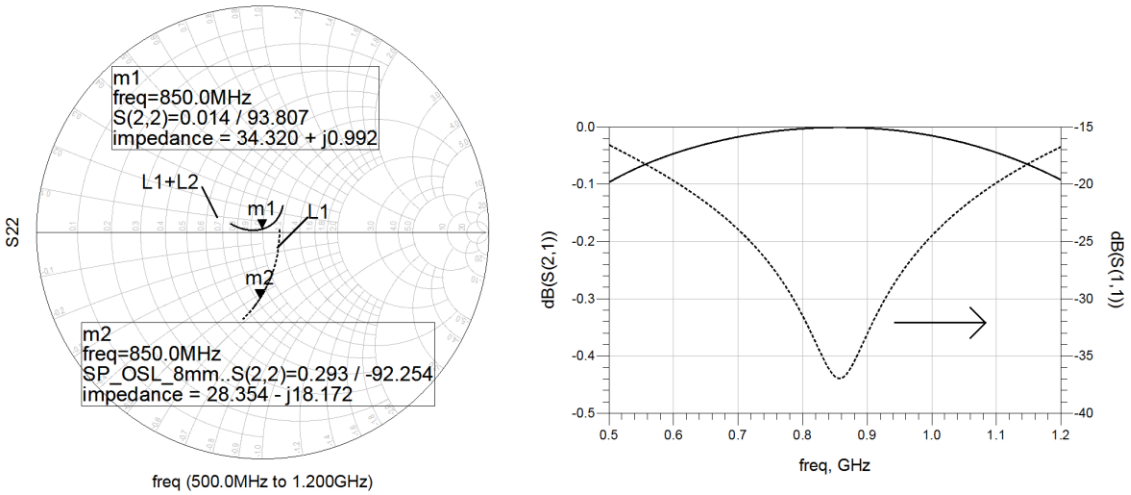

Figure 3.10: Simulated Result of Shunt L Match.

At the first look, the shunt L match might seem to be inferior to the T section prematch with constant impedance load. However, the transistor output impedance is dynamic at different input drive level which causes the static impedance prematch circuit transform the impedance quite differently depend on the different output power level.

3.4 Shunt L plus T match topology

In the case of large gate periphery power transistor, where the shunt L transformation is not adequate to raise the reference impedance at the package plane, an additional T match section is added.

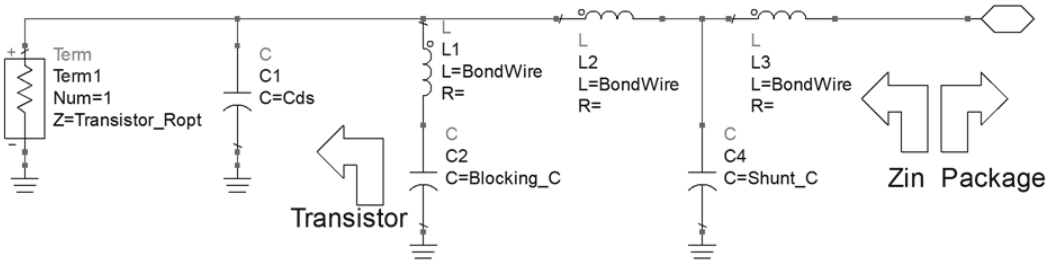

Figure 3.11: Shunt L Plus T Section Prematch Topology.

The ABCD matrix of the shunt L transformation along with the transistor can be written as follow:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & jwL_3 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwC_{shnt} & 1 \end{bmatrix} \begin{bmatrix} 1 & jwL_2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{jwL_{shnt}} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwC_{ds} & 1 \end{bmatrix} \begin{bmatrix} I_2 * Ropt \\ I_2 \end{bmatrix} \quad (3.18)$$

To simply the calculation, the blocking capacitor is ignored. After multiplication, Zin has the expression of

$$Zin = see\ appendix \quad (3.19)$$

The reflection coefficient is

$$\Gamma = \frac{Zin - Zo}{Zin + Zo} \quad (3.20)$$

The reflection coefficient magnitude is

$$|\Gamma| = \Gamma_m \quad (3.21)$$

The bandwidth can be found by

$$\Delta w \leq \frac{\pi}{RC} \times \left(In \frac{1}{\Gamma_m} \right)^{-1} \quad (3.22)$$

Simulated result is also shown,

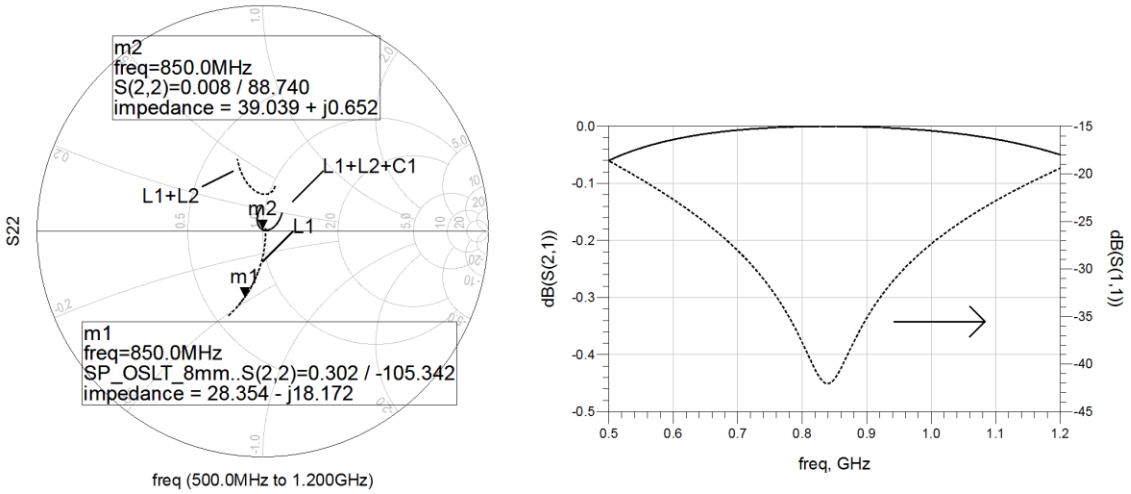

Figure 3.12: Simulated Result of Shunt L Plus T Section Match.

Tablet the result of the four different prematch circuits issue in

Prematch Topology	Transformed Impedance @850 MHz	Original Impedance	Mismatch loss on bandedge
Direct Wire Bond	25.0 Ω	28.3-j18.2 Ω	1.4 dB
T section	28.0 Ω	28.3-j18.2 Ω	0.8 dB
Shunt L	34.3+j1.0 Ω	28.3-j18.2 Ω	1.0 dB
Shunt L plus T	39.0+j0.6 Ω	28.3-j18.2 Ω	0.6 dB

Figure 3.13: Simulated Summary of the Prematch Circuits.

Both the direct wirebond and T section prematch have the minimal transformation if the Q is kept below 1. The shunt L plus T will give the highest transformed impedance and lowest mismatch loss after prematch; however, all simulated result assumed the circuit is lossless in nature. In lossy medium, more prematch section equals greater loss.

Chapter 4

Doherty Amplifier

4.1 Introduction

In chapter 2 section 1, Doherty amplifier was briefly introduced as today's basestation amplifier architecture. In this chapter, its architecture will be examined in more detail. The discussion will start with the two main devices namely the main and peaking amplifier, and then the focus will turn to the passive components which are within and surrounds them.

4.2 States of operations of a Doherty amplifier

The advantage of a Doherty amplifier laid within the load modulation that the main amplifier, M1, experience as the auxiliary amplifier, M2, is turning on with the increase of the input drive level. M1 is said to be "loadpull" by M2, which injects RF current to the combining node across the combiner. [11] In figure 4.1, main amplifier is replaced with generator one and auxiliary amplifier with generator 2. Each generator comprised of its prematch circuitry and impedance transformer thereafter. Generator one represents the main amplifier, and generator two represents the auxiliary amplifier.

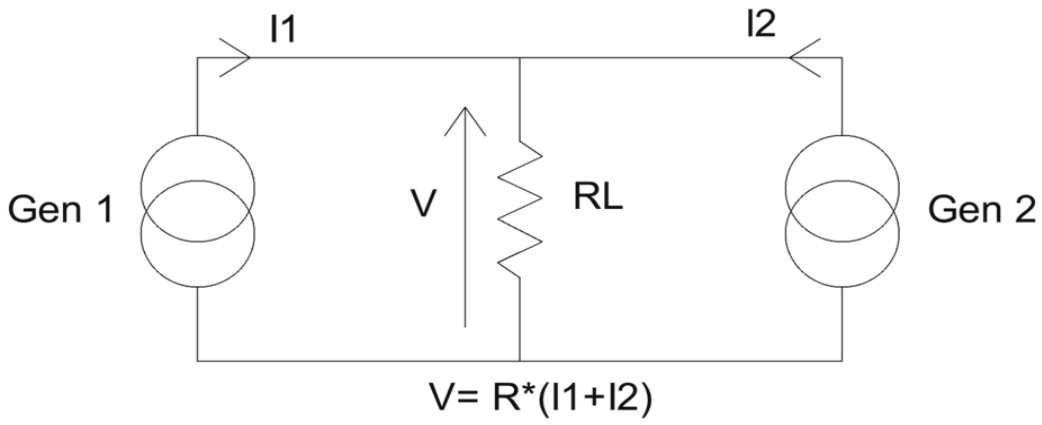

Figure 4.1: Load Modulation.

Generator one would see an impedance value of

$$Z_1 = R_L\left(\frac{I_1+I_2}{I_1}\right) \quad (4.1)$$

And generator two would see an equivalent impedance value of

$$Z_2 = R_L\left(\frac{I_1+I_2}{I_2}\right) \tag{4.2}$$

Rearrange (4.1), one obtains

$$Z_1 = R_L\left(1+\frac{I_2}{I_1}\right) \tag{4.3}$$

If I2 is in phase with I1, Z1 sees an increase in resistive value, where if I1 and I2 are anti-phase a less value is observed. Therefore I2 is loadpulling the impedance seen by generator one. In figure 4.2, the two generators are replaced with the actual main and auxiliary amplifier.

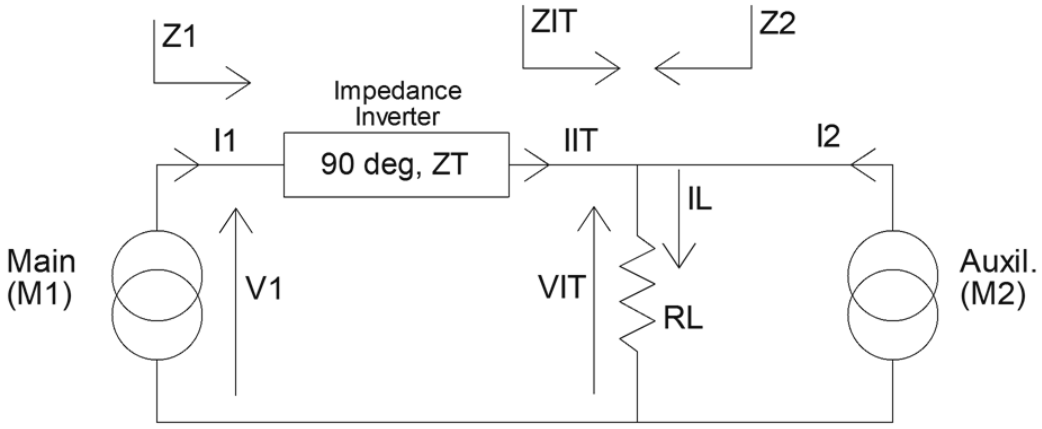

Figure 4.2: Doherty Schematic.

If the quarterwave line is replaced with its equivalent ABCD- parameter, then the voltage at the combining node is related to voltage across of the main amplifier in the following expression

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_T\sin\theta \\ j\left(1/Z_T\right)\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} V_{IT} \\ I_{IT} \end{bmatrix} \tag{4.4}$$

At the center frequency, fc, where θ=90, the above expression is reduced to

$$V_{IT} = -jZ_T I_1 \tag{4.5}$$

To solve for any θ, first VIt can be replaced in (4.4) with following expression

$$V_{IT} = R_L I_L = R_L(I_2 + I_{IT}) \tag{4.6}$$

Then (4.4) becomes

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_T \sin\theta \\ j\left(1/Z_T\right)\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} R_{opt}/2\,(I_2 + I_{IT}) \\ I_{IT} \end{bmatrix} \tag{4.7}$$

IIT, the current coming out of the transmission line can be found from above equation

$$I_L = \frac{I_1 - jI_2(R_L/Z_T)\sin\theta}{j(R_L/Z_T)\sin\theta + \cos\theta} \tag{4.8}$$

And the voltage, V1, across the main device is

$$V_1 = I_2 R_L \cos\theta + I_{IT}(R_L \cos\theta + jZ_T \sin\theta) \tag{4.9}$$

To find the impedance seen by main and auxiliary amplifiers

$$Z_1 = V_1/I_1 \tag{4.10}$$

$$Z_2 = V_{IT}/I_2 \tag{4.11}$$

For identical main and auxiliary amplifier, they have the same maximum linear current swing of Imax, and their fundamental amplitude for each device will be Imax/2 as depict in figure 4.3

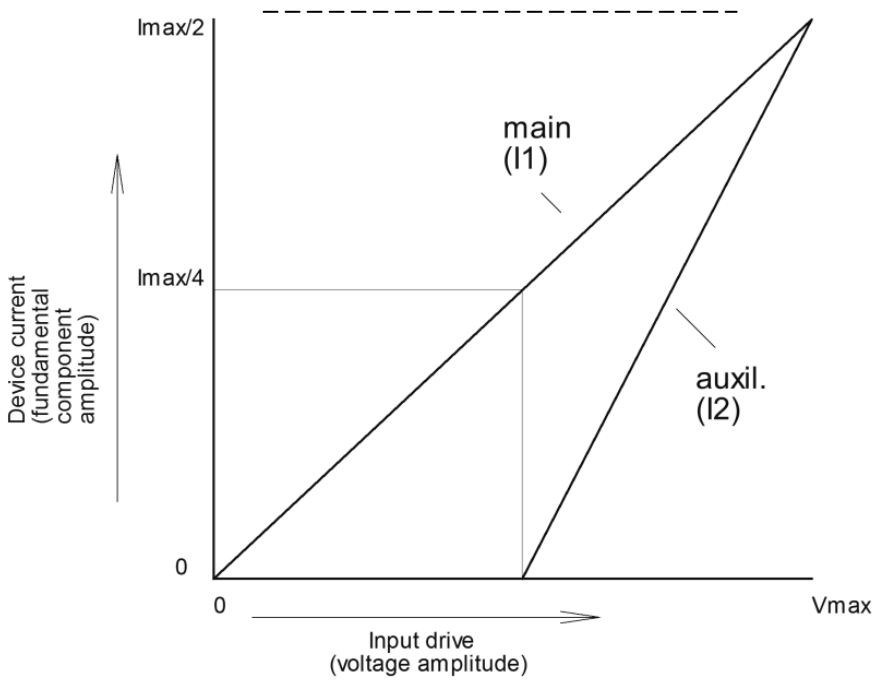

Figure 4.3: RF Current Amplitude Versus Input Voltage Amplitude.

I1 presents the current coming out of the main amplifier and I2 from auxiliary respectively. Now, knowing I1 and I2, which are 90 degrees apart at the center frequency, (4.10) is

$$Z_1 = \left(\frac{Z_T}{R_L} - \frac{I_2}{I_1}\right) Z_T \tag{4.12}$$

At 6dB backoff from peak power, Z1 see an impedance of 2Ropt and Ropt at peak power. Ropt is the optimal impedance at max power [11]

$$R_{opt} = \frac{V_{dc}}{\frac{I_{max}}{2}} \tag{4.13}$$

At peak power, (4.12) becomes

$$R_{opt} = \frac{Z_T^2}{R_L} - Z_T \tag{4.14}$$

And at 6dB backoff from peak power, (4.12) becomes

$$2R_{opt} = \frac{Z_T^2}{R_L} \tag{4.15}$$

Use (4.14) and (4.15) to solve for ZT and RL results

$$Z_T = R_{opt} \tag{4.16}$$

$$R_L = R_{opt}/2 \tag{4.17}$$

However, the phase condition between I1 and I2 must satisfies

$$< I_1 - < I_2 = 90^o \tag{4.18}$$

In the next two sections, both main and auxiliary amplifier will be examined separately at both 6dB backoff and peak power conditions.

4.3 Main amplifier

At 6dB backoff from peak power, the auxiliary amplifier contributes no current into the combining node and I2=0. As it was mentioned in the previous section, Z1 sees an impedance of 2Ropt after the impedance inverter, ZT, shown in figure 4.4

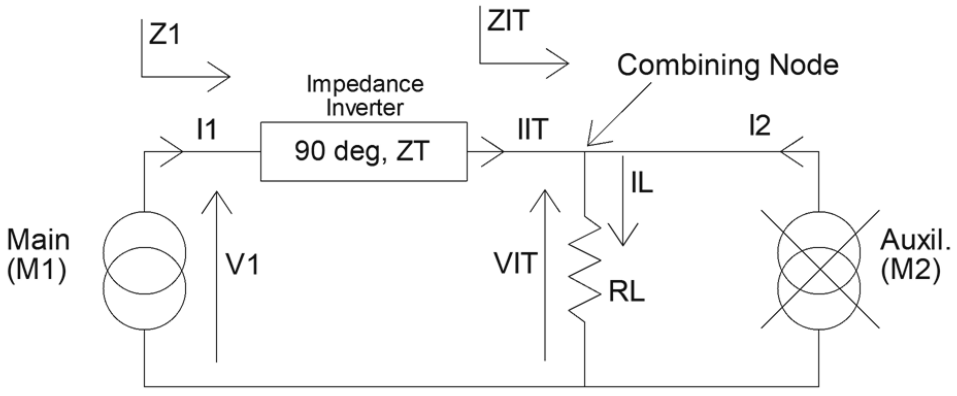

Figure 4.4: Doherty Schematic at 6dB Backoff From Peak Power.

The impedance inverter, ZT, transforms Z1 from 2*Ropt to Ropt/2, which equals the RL in (4.17).

When the Doherty amplifier is at its maximum power condition, both I1 and I2 contribute equal amount of current and they are 90 degree apart in phase. At the combining node IIT is in phase with I2 with equivalent current magnitude shown in figure 4.2. Because the current is equal and in phase, ZIT and Z2 each see 2xRL at combining node, which results in

$$Z_{IT} = Z_2 = 2 * R_L = R_{opt} = |Z_1|(\theta\text{=-90}) \qquad (4.19)$$

This shows the impedance inverter acts as a simple 90 degree phase shifter. It is expected that the main amplifier will see its impedance spreading more across frequency at backoff condition versus what it sees when the Doherty amplifier operates at maximum power condition.

4.4 Auxiliary amplifier

Ideally, the function of auxiliary amplifier is like a peak power generator which output power when Doherty amplifier is operating at maximum power condition. When Doherty amplifier is at its 6 dB backoff condition, there is no current flowing into the combining node in figure 4.4. Therefore, I2=0, and Zoff=∞.

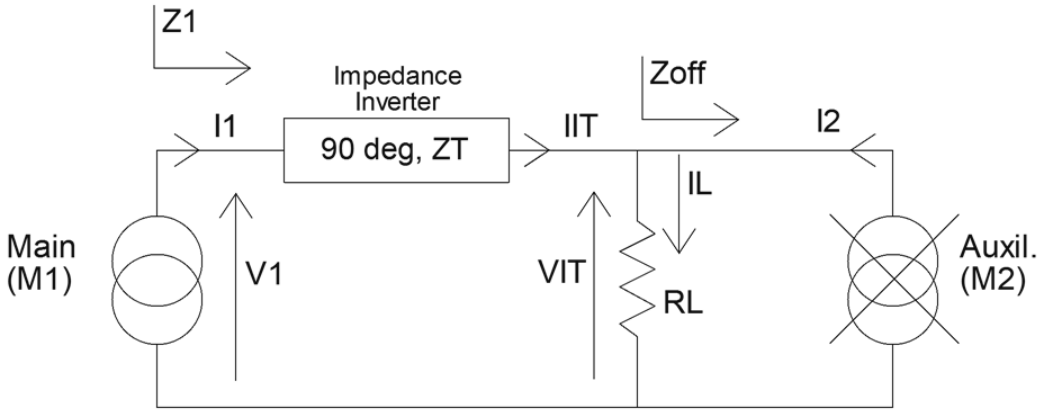

Figure 4.5: Impedance Looking Into Auxiliary Amplifier.

4.5 Impedance inverter and output power combiner

In Doherty amplifier, the impedance inverter is usually implemented using a quarterwave transformer. However, the 90 degree phase shift between main and auxiliary amplifiers needs to take account of the intrinsic parasitic capacitance of device output. In reality, the 90 degree line is typically shorter as discussed in [14] due to the incorporation of the capacitance. This can be shown in figure 4.7.

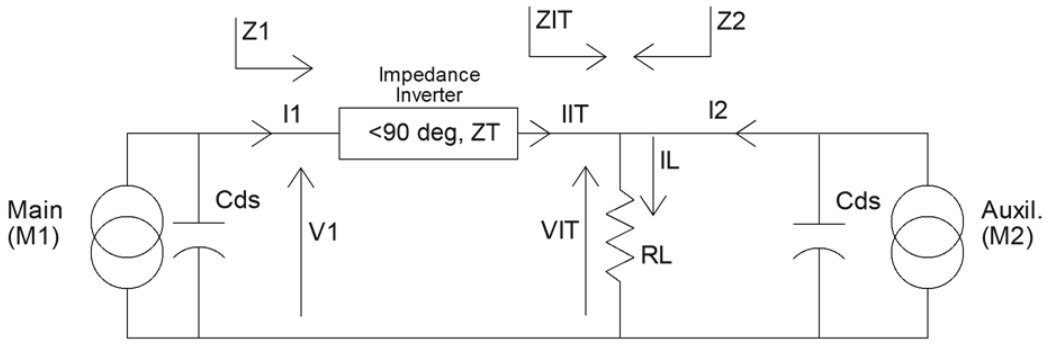

Figure 4.6: Doherty Amplifier With Device Parasitic Capacitance.

So far, RL, the combining terminal impedance is assumed to be a single fixed value across frequency. However, in practice, a quarterwave transformer is used to transform system 50 Ohm impedance to RL. This will also be explored further in next chapter.

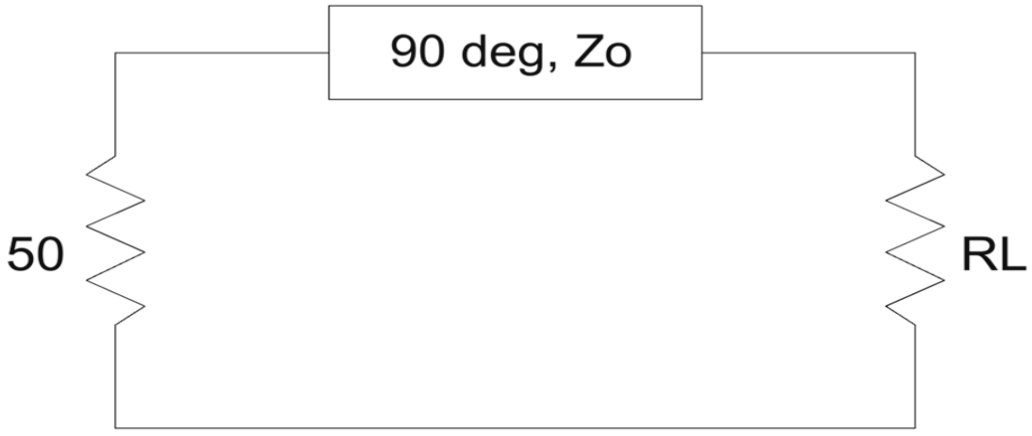

Figure 4.7: Quarterwave Transformer Used Between System Impedance and Combining Node of Doherty.

Chapter 5

Bandwidth Limitation of Doherty Amplifier

In previous chapter, a general description was given on Doherty amplifier with its operating characteristic at both peak power and backoff power conditions. In this chapter, a more detail discussion will be given on some of the practical implementations and their bandwidth limitation. First, the main amplifier with the two matched circuitry will be compared at both the 6dB back-off and peak power conditions. Next, the impedance inverter network will be added to the main amplifier.

5.1 Prematch circuitry in the main amplifier

In chapter three, series of output prematch topologies were discussed for basestation amplifiers. Amplifier designers are quite familiar with static impedance matching, which means matched impedance does not alter over course of amplifier operation. However, according to discussion in chapter 4, as the auxiliary amplifier is turning on and its RF current are being injected into combining node in figure 4.2, the impedance seen by Z1 change from 2Ropt to Ropt as the Doherty amplifier reaches its maximal power condition. Adding to the complication, the parasitic capacitance shown in figure 4.7 causes the impedance becomes dispersive seen at the intrinsic current source of the main amplifier. According to (2.6), bandwidth is inversely proportional to R, so as R changes from Ropt to 2Ropt, it reduces the maximum allowed bandwidth by 50%.

$$\Delta W_{6db} = \frac{\pi}{2RC} = \frac{1}{2} * \Delta W_{peak} \qquad (5.1)$$

Following is an example of how the impedance spread over frequency

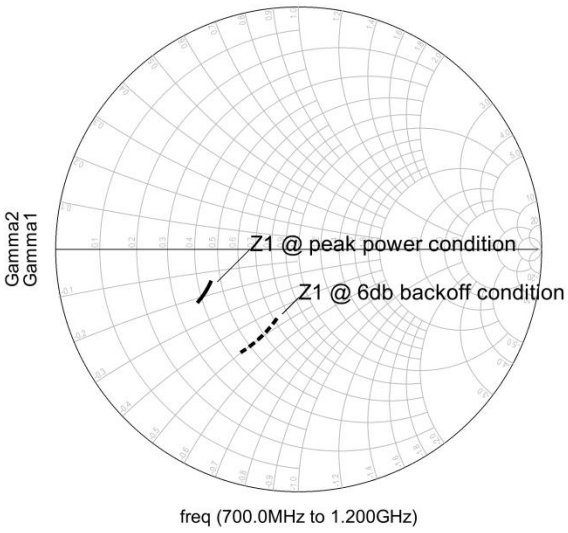

Figure 5.1: Impedance Dispersion at Both Peak Power and 6 dB Backoff Condition.

Two of the most common prematch circuits are T match and shunt L topologies, and each has its benefits. For the T section prematch, it can be easily integrated as part of the transmission line, which has the lump equivalent as follow

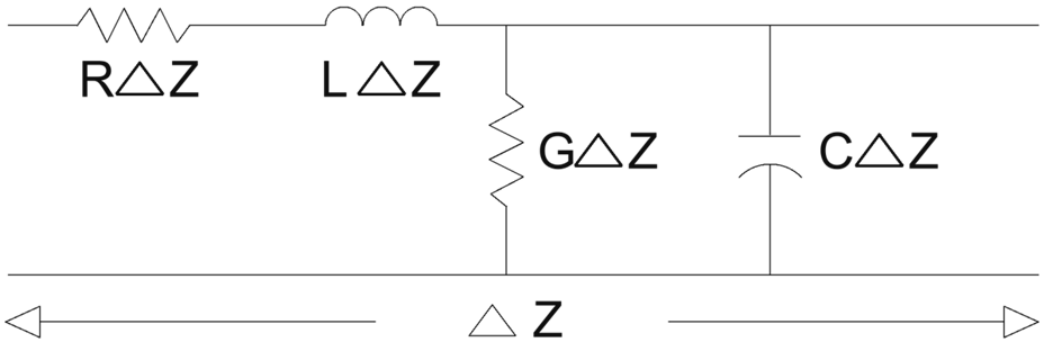

Figure 5.2: Equivalent Circuit for Incremental Length of Transmission.

If the T section is incorporated with the transmission line by cascading to the transmission equivalent circuit, then

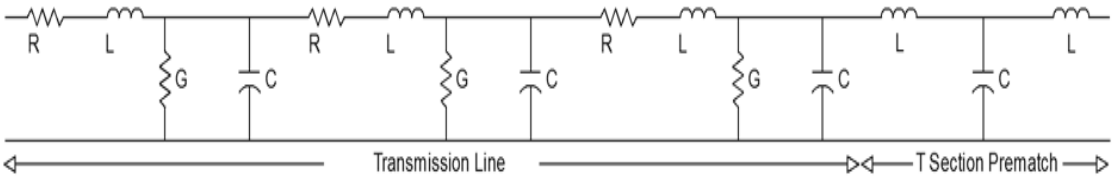

Figure 5.3: Transmission Line With T Section Prematch.

Moreover, the parasitic capacitance, Cds, of the active device can be absorbed into the entire matching topology as it was discussed in [14]

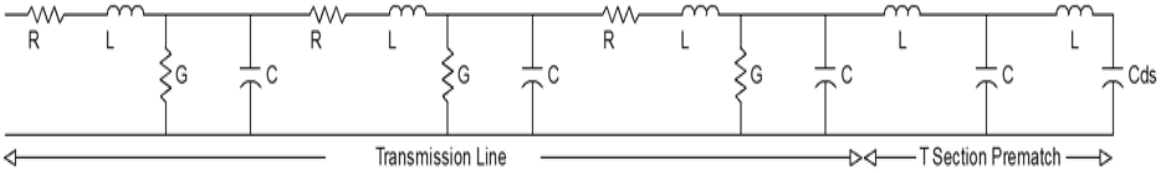

Figure 5.4: T section prematch incorporated transmission line with Cds.

Impedance transformation of the main amplifier performed in both 6 dB backoff and peak power condition is illustrated as following

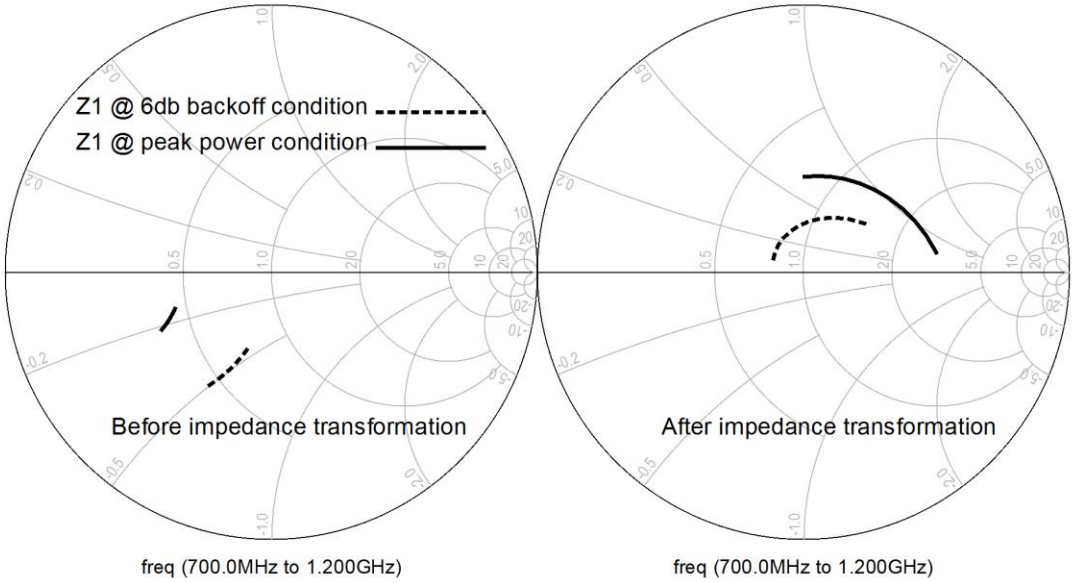

Figure 5.5: Impedance Transformation of T Section Prematch of the Main Amplifier at Both 6 dB Backoff and Peak Power Condition.

For shunt L prematch, the shunt inductance resonates out the Cds at both backoff and peak power conditions. During the impedance transformation, the main amplifier sees a less dispersive impedance spread comparing to T section prematch topology.

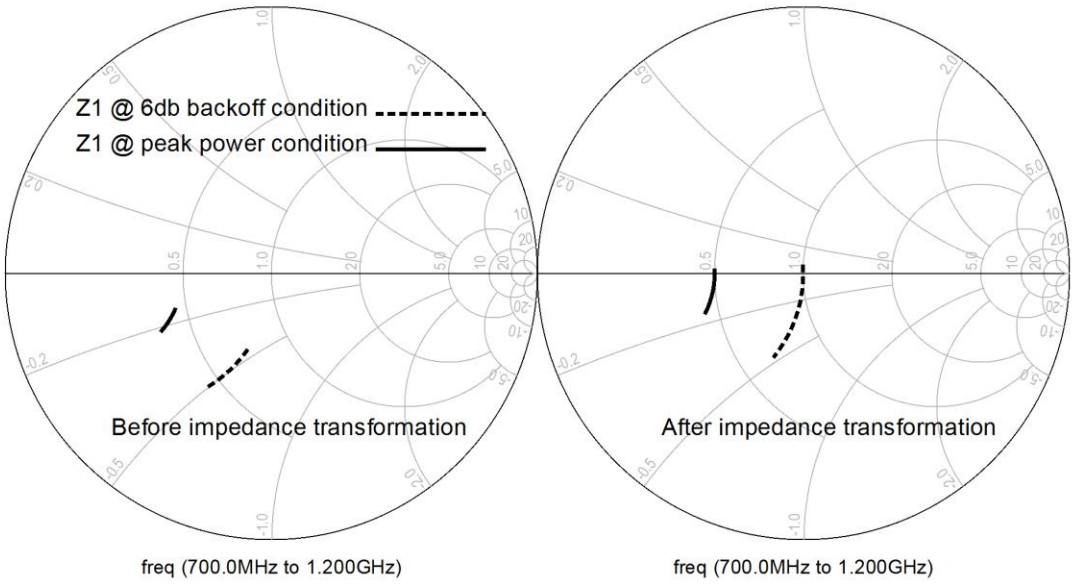

Figure 5.6: Impedance Transformation of Shunt L Prematch of the Main Amplifier at Both 6dB Backoff and Peak Power Condition.

5.2 Prematch circuitry in auxiliary amplifier

The auxiliary amplifier, in theory, has the same impedance transform characteristic during the peak power condition since both main and auxiliary amplifier contribute same amount of RF current into combining described in figure 4.2. However, at 6 dB back off operating condition, because of the parasitic capacitance of the device, Zoff does not see an open circuit as shown in figure 5.7. The result will cause the RF current from the main amplifier flowing into the auxiliary amplifier instead of the combiner node and degrades the amplifier's efficiency.

If T section prematch is applied to the auxiliary amplifier, then it will rotate Zoff impedance in figure 4.2 closer to a short circuit.

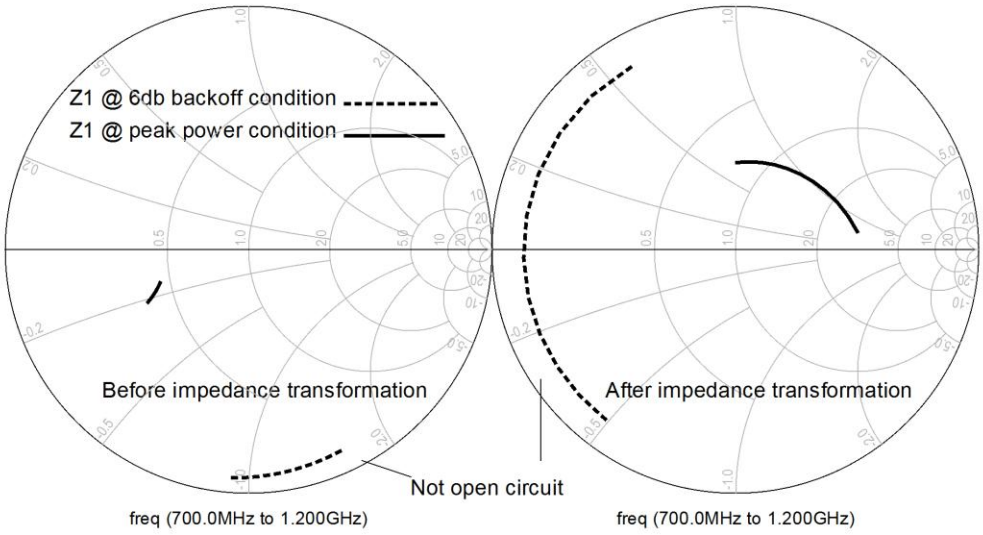

Figure 5.7: Impedance Transformation of T Section Prematch of the Auxiliary Amplifier at Both 6 dB Backoff and Peak Power Condition.

Although this can be compensated by adding a 90 degree line and transform the short to an open circuit again, it will however add loss and create impedance dispersion across frequency. Next, the shunt L prematch is applied to auxiliary amplifier and because the shunt L resonant out the parasitic capacitance of the device, Zoff sees an open circuit looking into the auxiliary amplifier's output prematch circuit

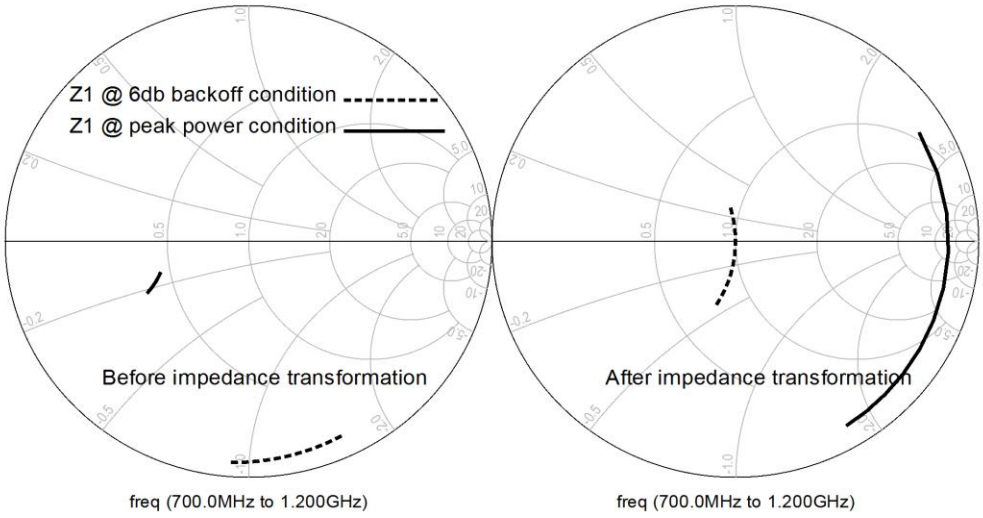

Figure 5.8: Impedance Transformation of Shunt L Prematch of the Auxiliary Amplifier at Both 6 dB Backoff and Peak Power Condition.

The auxiliary amplifier can be connected directly to the combining node with no additional phase compensation compared to T section prematch.

5.3 Prematched main amplifier with impedance inverter using quarterwave transformer

In figure 4.4, the main amplifier is connected to an impedance inverter, which acts as impedance transformer at backoff power condition and as 90 degree phase shifter with no impedance transformation at peak power condition. As for the prematch topology, shunt L will be utilized so a less dispersive impedance match can be realized as discussed in 5.1.

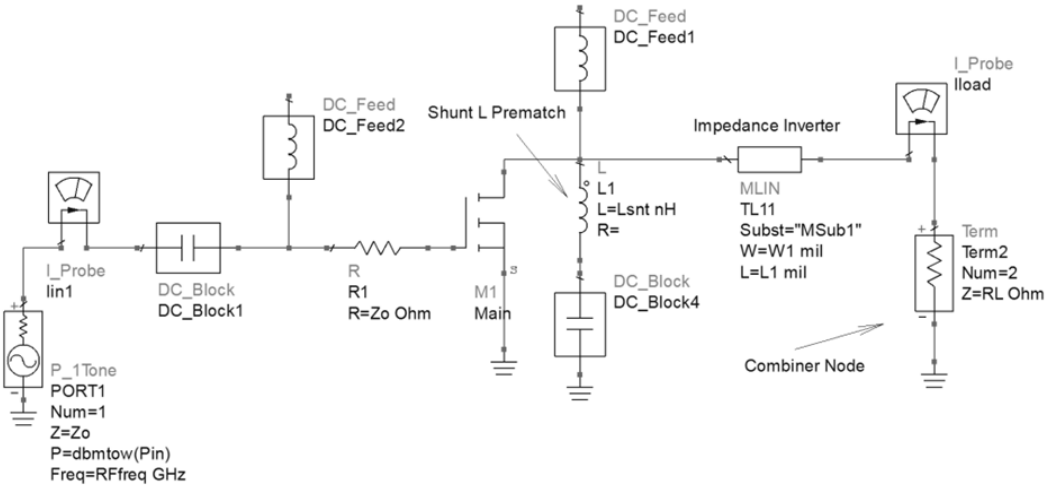

Figure 5.9: Main Amplifier With Quarterwave Impedance Inverter.

The device being used has a peak power of 31.6 watt and has an output parasitic capacitance of 1.46 pF. The shunt L inductance value used for the prematch is 10 nH. The large signal frequency response of the main amplifier with just the shunt L at backoff power and peak power condition is shown below

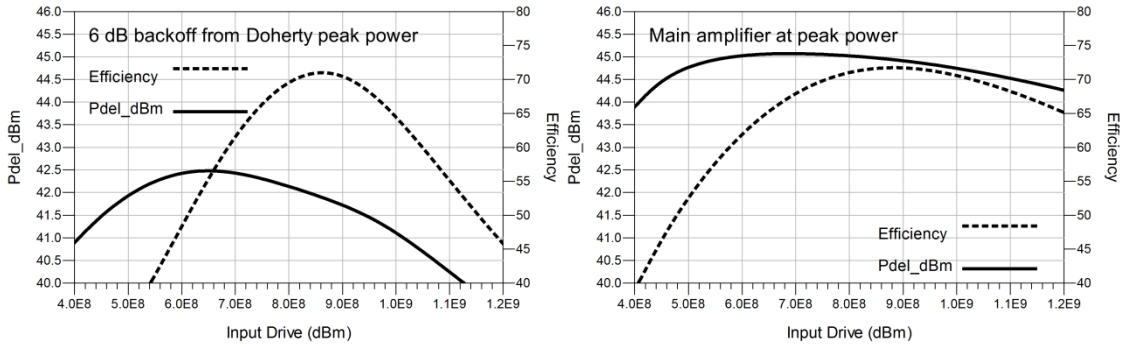

Figure 5.10: Main Amplifier With Shunt L Prematch at Both Backoff and Peak Power Condition.

Since only one half of the Doherty amplifier namely the main amplifier is being observed, the total peak power of the Doherty would be 48dBm. The backoff power would be 42dBm at Fo, 850MHz.

Notice how the power maxima and the efficiency maxima are not located near the same frequency range. In fact, the maximum power impedance stay relative broadband compared to the maximum efficiency impedance. One of the reasons is that efficiency of the amplifier is heavily depending on its harmonic impedance which will not be investigated in this thesis.
If the impedance inverter is added as shown in figure 5.9, the larger signal frequency response is shown to be

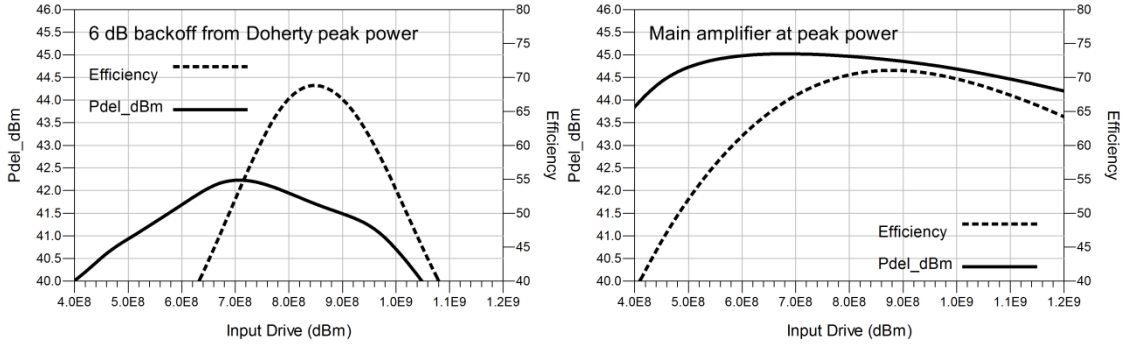

Figure 5.11: Main Amplifier With Shunt L Prematch and Impedance Inverter at Both Backoff and Peak Power Condition.

It can be seen the bandwidth of the amplifier started to narrow with the addition of quarter wave microstrip line. Also there is about 0.2dB PCB loss which translates to 4% loss of efficiency at backoff power level.

5.4 Alternative implementation of the impedance inverter in Doherty amplifier

In section 5.3, it was observed when the Doherty operates at the 6 dB backoff power condition, the bandwidth is further limited with the impedance inverter placed between the main amplifier and the combiner node. In this section, an alternative quarterwave transformer is being explored. In many broadband filter applications, in order to achieve broadband a feedback circuit is often required. The proposed circuit implementation is shown below

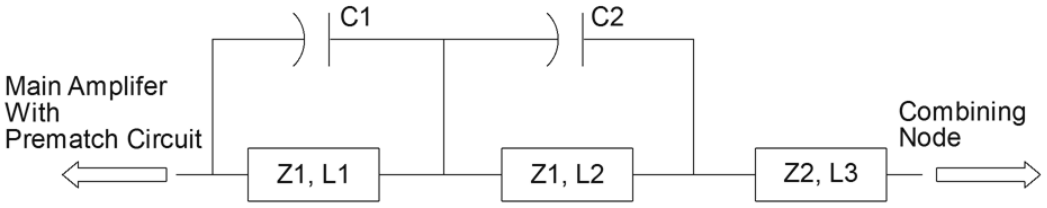

Figure 5.12: Proposed Impedance Inverter With Capacitive Feedback.

The transmission line is in parallel with the series capacitor, the ABCD matrix can be obtain by first combining them in their Y parameter, then convert back to their ABCD matrix as follow

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A^T & B^T \\ C^T & D^T \end{bmatrix} \begin{bmatrix} I_2 * R_{Comb} \\ I_2 \end{bmatrix} \tag{5.2}$$

A single feedback structure has the ABCD expression as follow

$$A = \frac{(wC_{fbk}Z_o tab\beta l - 1)cos\beta l}{wC_{fbk}Z_o sin\beta l - 1}, B = \frac{jZ_o sin\beta l}{1 - wC_{fbk}Z_o sin\beta l}$$

$$C = |Y| \frac{1 - wC_{fbk}Z_o sin\beta l}{jZ_o sin\beta l}, D = \frac{(wC_{fbk}Z_o tab\beta l - 1)cos\beta l}{wC_{fbk}Z_o sin\beta l - 1} \tag{5.3}$$

$$|Y| = \left(\frac{1 - wC_{fbk}Z_o tan\beta l}{jZ_o tan\beta l}\right)^2 - \left(\frac{1 - wC_{fbk}Z_o sin\beta l}{jZ_o sin\beta l}\right)^2 \tag{5.4}$$

Cascading the two feedback structures with additional transmission line yields

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} A_3 & B_3 \\ C_3 & D_3 \end{bmatrix} \begin{bmatrix} I_2 * R_{Comb} \\ I_2 \end{bmatrix} \quad (5.5)$$

Where A1, B1, C1, and D1 represents the first feedback structure associate with Z1, L1, and A2, B2, C2, and D2 represents the second feedback structure associate with Z2, L2, and A3, B3, C3, and D3 represents the last section of the transmission line, Z3, L3.

Following figure shows the impedance inverter feedback structure after the prematched main amplifier

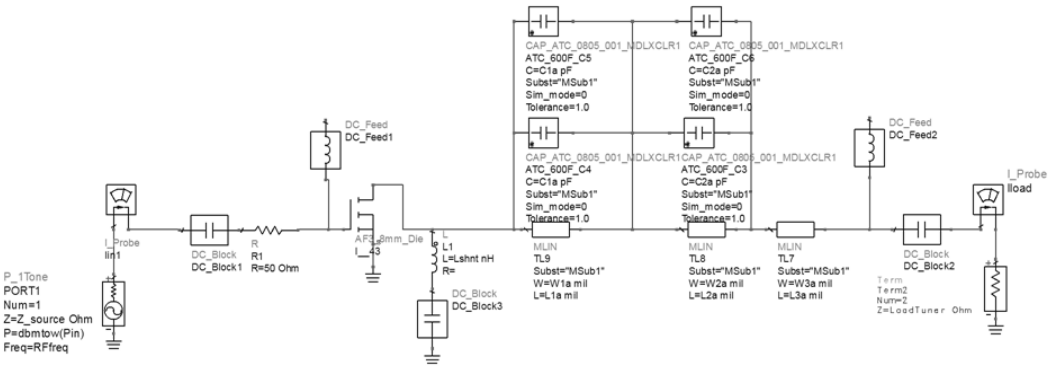

Figure 5.13: Main Amplifier With Proposed Impedance Inverter With Capacitive Feedback.

Additional parallel capacitors are placed to reduce the series resistance and inductance across the ceramic capacitor. The PCB material is Roger's RO4350, which is typically used in cellular base station design. The large signal frequency response of the amplifier is shown in the following figures

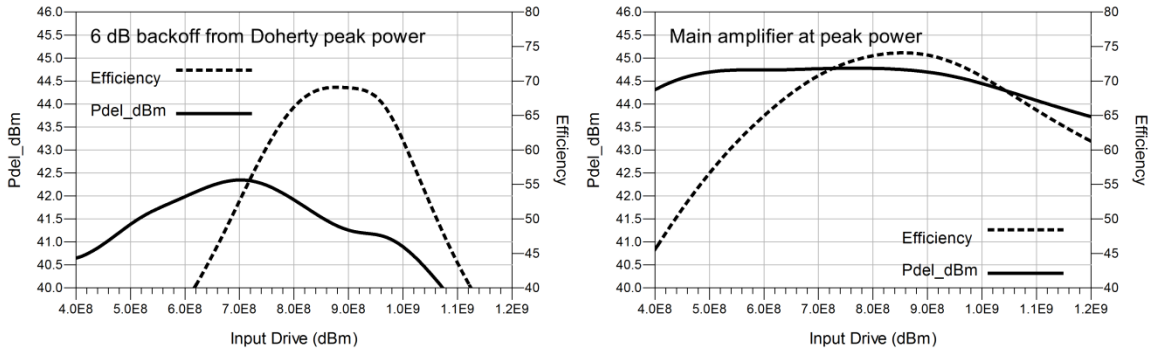

Figure 5.14: Prematched Main Amplifier With the New Propose Impedance Inverter at Both Backoff and Peak Power Condition.

At back off power condition, the 65% efficiency bandwidth increase to 180MHz from 120MHz by utilizing the impedance inverter with capacitive feedback. The drawback of this circuitry is the 0.2dB loss of peak power across band at peak power condition.

The comparison between traditional impedance inverter and the proposed inverter structure with feedback is tablet in below figure.

Inverter Structure	65% efficiency bandwidth @ 6dB backoff (MHz)	44.5 dBm output power bandwidth @ P3dB compression (MHz)
Traditional quarter wave inverter	120	610
Proposed impedance inverter with capacitive feedback	180	550

Figure 5.15: Comparison Between Traditional Quarterwave Impedance Inverter Vs Proposed Impedance Inverter With Capacitive Feedback.

Chapter 6

Conclusion and Future Work

In this thesis, the design methodology of a basestation power amplifier is explored. Loadline theory was introduced as the initial estimation of amplifier's output impedance match to the maximal power performance. Next, the derivations of the prematch network of the power amplifier using the ABCD matrix were carried out to express the bandwidth limitation of each topology. The transformation of each prematch circuitry were also simulated and compared.

Next stage of discussion was on the application of basestation power amplifier. The Doherty amplifier was introduced and explained with its unique ability to sustain both the high efficiency at a back-off power level and the peak power required at maximum power condition. It was shown that such topology is limited in its bandwidth due to the impedance inverter network between the main and auxiliary amplifiers. This thesis presents an alternative implementation of the impedance inverter network by using a capacitive feedback especially when the Doherty amplifier is operating at the backoff power condition.

LDMOS was used as the device technology to implement the Doherty amplifier. The reason being is that it is still the dominate technology used today for basestation amplifier design. However, as GaN, Gallium Nitride is gaining traction in the basestation industry; it is foreseen as a possible substitute of LDMOS in the near future. Device such as GaN is sensitive to the harmonic loading, because of their low output parasitic capacitance compare to LDMOS on a same power rating. As it was mentioned in limited context in this thesis, a proper harmonic impedance loading, namely second and third harmonic impedance, will have a significant impact on the amplifier’s efficiency. It was observed the efficiency improved by 3~4 % by using the new impedance inverter network due to its harmonic termination at second and third harmonic frequency at peak power condition. Moreover, the proposed feedback impedance inverter structure will need to be implemented with integrated IC to ensure a real to real impedance transformation from the main amplifier to the combining node with the auxiliary amplifier in the Doherty architecture.

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APPENDIX A

ZIN CALCULATION FOR SHUNT L PLUS T SECTION PREMATCH IN SECTION 3.4

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & jwL_3 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwC_{shnt} & 1 \end{bmatrix} \begin{bmatrix} 1 & jwL_2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{jwL_{shnt}} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jwC_{ds} & 1 \end{bmatrix} \begin{bmatrix} I_2 * Ropt \\ I_2 \end{bmatrix} \quad \text{(A1)}$$

Multiply out the matrix issues in

$$Zin = \frac{V_1}{I_1} = \frac{R_{opt}X_4 + X_2(R_{opt}C_{ds} + 1)}{R_{opt}X_5 + X_3(R_{opt}jwC_{ds} + 1)} \quad \text{(A2)}$$

Where

$$X_1 = 1 + (jw)^2 L_3 C_{shunt} \quad \text{(A3)}$$

$$X_2 = jwL_2(1 + (jw)^2)L_3 C_{shunt} + jwL_3$$

$$X_3 = (jw)^2 L_2 C_{shunt}$$

$$X_4 = X_1 + \frac{X_2}{jwL_{shunt}}$$

$$X_5 = jwC_{shunt} + \frac{X_3}{jwL_{shunt}}$$