

Monocrystalline ZnTe/CdTe/MgCdTe Double Heterostructure Solar Cells

Grown on InSb Substrates by Molecular Beam Epitaxy

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved October 2014 by the
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December 2014

ABSTRACT

There has been recent interest in demonstrating solar cells which approach the detailed-balance or thermodynamic efficiency limit in order to establish a model system for which mass-produced solar cells can be designed. Polycrystalline CdS/CdTe heterostructures are currently one of many competing solar cell material systems. Despite being polycrystalline, efficiencies up to 21 % have been demonstrated by the company First Solar. However, this efficiency is still far from the detailed-balance limit of 32.1 % for CdTe. This work explores the use of monocrystalline CdTe/MgCdTe and ZnTe/CdTe/MgCdTe double heterostructures (DHs) grown on (001) InSb substrates by molecular beam epitaxy (MBE) for photovoltaic applications.

Undoped CdTe/MgCdTe DHs are first grown in order to determine the material quality of the CdTe epilayer and to optimize the growth conditions. DH samples show strong photoluminescence with over double the intensity as that of a GaAs/AlGaAs DH with an identical layer structure. Time-resolved photoluminescence of the CdTe/MgCdTe DH gives a carrier lifetime of up to 179 ns for a 2 μm thick CdTe layer, which is more than one order of magnitude longer than that of polycrystalline CdTe films. MgCdTe barrier layers are found to be effective at confining photogenerated carriers and have a relatively low interface recombination velocity of 461 cm/s. The optimal growth temperature and Cd/Te flux ratio is determined to be 265 $^{\circ}\text{C}$ and 1.5, respectively.

Monocrystalline ZnTe/CdTe/MgCdTe P-n-N DH solar cells are designed, grown, processed into solar cell devices, and characterized. A maximum efficiency of 6.11 % is demonstrated for samples without an anti-reflection coating. The low efficiency is mainly due to the low open-circuit voltage (V_{oc}), which is attributed to high dark current caused

by interface recombination at the ZnTe/CdTe interface. Low-temperature measurements show a linear increase in V_{oc} with decreasing temperature down to 77 K, which suggests that the room-temperature operation is limited by non-radiative recombination. An open-circuit voltage of 1.22 V and an efficiency of 8.46 % is demonstrated at 77 K. It is expected that a coherently strained MgCdTe/CdTe/MgCdTe DH solar cell design will produce higher efficiency and V_{oc} compared to the ZnTe/CdTe/MgCdTe design with relaxed ZnTe layer.

This work is dedicated to my wife, Nikki DiNezza, whose love and support
have made it possible to pursue my dreams.

ACKNOWLEDGMENTS

First and foremost, I would like to thank my research advisor Dr. Yong-Hang Zhang. He has always challenged and inspired me to think at a much deeper level, both with my technical work and within my personal life. His guidance and intuition has led me to study CdTe solar cells, and I am truly grateful for that. I would also like to thank Dr. Shane Johnson who has also been a mentor to me, particularly relating to the operation of the MBE system. I'm also thankful for my committee members Dr. Meng Tao and Dr. Zachary Holman for their important feedback on this work.

Over the past 6 years there have been many people in our group who have mentored me or contributed to my education and training. I am thankful to have worked with (in roughly chronological order): Dr. Ding Ding, Dr. Shumin Wang, Dr. Songnan Wu, Dr. Robin Scott, Dr. Jin Fan, Dr. Ben Green, Dr. Elizabeth Steenbergen, Dr. Jingjing Li, Dr. Kevin O'Brien, Dr. Swee Hoe Lim, Dr. Charles Allen, Dr. Oray Orkun Cellek, Dr. Qiang Zhang, and Dr. Stuart Farrell. I'm also thankful to have worked with the Master's graduates Junliang Chen and W. H. G. (Hank) Dettlaff.

Special recognition should be given to the many people in our group who worked directly on this project. First to be recognized is Xin-Hao Zhao, who performed photoluminescence measurements, X-ray diffraction measurements, and preliminary modeling. Ying-Shen Kuo and Jacob Becker carried out the processing and testing of solar cell samples. Dr. Alex Kirk and Yuan Zhao provided solar cell modeling. Shi Liu carried out III-V growths, a few of the II-VI growths, and developed the InSb buffer layer growth procedure. Calli Campbell carried out some of the growths as well. Xiao-Meng Shen assisted with XRD. Preston Webster has contributed to my understanding of MBE

growth and characterization through many discussions. From Dr. David Smith's group, I would like to acknowledge Jing Liu who provided TEM cross section measurements. Lastly, I'd like to acknowledge Dr. Xinyu Liu and Dr. Jacek K. Furdyna at Notre Dame University who carried out the ZnTe emitter layer growth. It would not have been possible to demonstrate a working solar cell in such a short period of time without them.

Several ASU and external organizations also contributed to this work. These include the Center for Solid State Electronics Research (CSSER) and the Leroy Eyring Center for Solid State Science (CSSS). Both of these organizations provided the fabrication tools and characterization equipment that have made this work possible. External collaborations include General Electric, First Solar, the National Renewable Energy Laboratory (NREL), and Dr. Tom Myers at Texas State University, all of which have provided important feedback about our samples.

Funding from numerous sources has made this work possible, and I am grateful for their support. These include Fellowships from the Science Foundation Arizona and National Science Foundation (grant number DGE-0802261) which supported me for a total of 5 years. I am also grateful for the fellowship provided by Mr. and Mrs. Kucera through the Achievement Rewards for College Scientists Foundation, the Ford Fellowship, and the Ira. A. Fulton Fellowship. Additional research grants were provided by the Bay Area Photovoltaic Consortium, Department of Energy, First Solar, Science Foundation Arizona, Air Force Office of Scientific Research, Arizona State University, and the National Science Foundation.

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CHAPTER 1

INTRODUCTION

In the quest for low-cost renewable energy, photovoltaic solar cells have emerged as a promising alternative to fossil fuels and other renewable energy sources. What is unique about solar cells is that they *directly* convert photons from the sun into electricity by utilizing the unique properties of semiconductors. Other technologies also derive their energy from the sun, but in indirect and less-efficient ways. For example, bio fuels are derived from plant matter that obtains energy from the sun using photosynthesis, which has a maximum light-to-biomass efficiency of only 8-9 % [1]. In contrast, the maximum theoretical efficiency of a single-junction solar cell is 33.7 % under AM1.5G illumination, as determined by the detailed-balance model and assuming the material has a band gap of 1.34 eV [2]. The relatively high efficiency and the high energy density of sunlight make photovoltaics (PVs) the most promising alternative electricity source.

Polycrystalline CdTe is one of several semiconductor materials that are currently being used in commercially-developed terrestrial PV installations. As a material, CdTe has a nearly ideal direct band gap of 1.51 eV and a large absorption coefficient, which makes it suitable for thin-film solar cells. Other competing technologies include silicon (mono-crystalline, poly-crystalline and amorphous), CIGS (copper indium gallium selenide), and concentrated photovoltaics using multi-junction III-V based junctions on Ge or GaAs substrates [2]. Their efficiencies vary, and all of them have unique device structures, advantages, and disadvantages. One important metric for terrestrial photovoltaics is the price-per-peak-watt output (measured at 1 sun concentration), noted as $\$/W_p$. In 2009, the US-based PV manufacturer First Solar was the first company to

surpass the $\$1/W_p$ threshold using a CdTe/CdS heterojunction device deposited on glass panels [3]. Since then, the company has achieved an impressive $\$0.40/W_p$ for production-quality CdTe modules that operate at 14.2 % efficiency [4], and the record module efficiency is 17.5 % [5]. On the other hand, the record monocrystalline Si module efficiency is 22.9 % [5], and the company Jinko Solar has achieved production-quality modules that operate at 16.5 % efficiency [6] and at a cost of $\$0.47/W_p$ [7]. Clearly, CdTe-based panels have a lot of catching up to do in terms of panel efficiency, which is an important factor for rooftop and space-constrained applications. For these applications, gains in efficiency relate to larger balance-of-system savings compared to utility-scale applications [8]. Also, customers may value the total power output of a rooftop installation over the cost-per-watt metric. For these reasons, it is worthwhile to explore new ways of improving the CdTe cell efficiency and to determine the fundamental limits of this technology.

There has been considerable interest recently in demonstrating solar cells that reach their detailed-balance limit [9]. The motivation for this initiative is to demonstrate very high efficiency cells (albeit at higher cost) which represent the ideal structure for manufacturers to achieve through lower-cost manufacturing processes. Table 1.1 shows a comparison of the efficiencies for CdTe and GaAs solar cells in both polycrystalline and monocrystalline form. Also listed is the detailed balance limit for those materials, which is calculated assuming no non-radiative recombination, one sun concentration (AM1.5G spectrum), 25 °C operation, and a perfect rear reflector [10]. Monocrystalline GaAs shows the highest efficiency at 28.8 %, which is just 4.4 % (absolute) away from its detailed balance limit. Polycrystalline GaAs trails far behind at 18.4 %, which is expected

for materials with a high concentration of crystalline defects. On the other hand, the opposite is observed for CdTe. Most research on CdTe focuses on polycrystalline material due to the relatively low cost deposition and manufacturing process [2]. A record efficiency of 21 % has been achieved by First Solar which is far beyond that of polycrystalline GaAs [11]. Monocrystalline CdTe has not been studied significantly, presumably because the high cost of CdTe substrates are prohibitive for research and commercial applications. The highest efficiency for monocrystalline CdTe is only 13.4 %, which utilizes a CdTe/In₂O₃ PN heterojunction [12]. Given the high efficiency achieved for polycrystalline CdTe, it would be reasonable to expect monocrystalline CdTe cells to achieve efficiencies approaching GaAs or even greater. Advances in materials and growth technology may open up an opportunity to demonstrate high-efficiency monocrystalline CdTe solar cells.

Table 1.1. Demonstrated cell efficiencies and theoretical limits [5], [10].

Material	Polycrystalline Record Efficiency	Monocrystalline Record Efficiency	Detailed Balance Limit
CdTe	21.0 %	13.4 %	32.1 %
GaAs	18.4 %	28.8 %	33.2 %

The relatively poor efficiency of polycrystalline CdTe cells comes from defect recombination losses, which is evidenced by the typically short carrier lifetimes of less than 6 ns [13]. It should be no surprise that defect recombination dominates in these devices considering the small grain size of 1 μm , which provides a large surface area for grain boundary recombination [14]. Recently, our group has grown monocrystalline CdTe/MgCdTe double heterostructures (DHs) on InSb substrates using molecular beam epitaxy (MBE) which have a carrier lifetime of 86 ns for a 1 μm thick CdTe layer [15]. Longer SRH lifetimes of 179 ns have also been demonstrated using a 2 μm thick CdTe

layer, and up to 97 ns has been observed for the 1 μm thick CdTe layer by probing different areas on the wafer [16]. Based on this carrier lifetime and practical assumptions for material parameters (surface recombination, mobility, etc...), our modeling results show that monocrystalline CdS/CdTe solar cells can achieve efficiencies greater than 25 % [10]. Additional improvements are expected by replacing the relaxed CdS emitter layer with a coherently strained MgCdTe emitter. Although such a cell grown by MBE would be too expensive for the PV industry to commercialize, it can be used to investigate the fundamental limits of the material and develop an ideal CdTe structure, which may lead to improvements in commercially-produced polycrystalline CdTe solar cells.

1.1 CdTe-based heterostructures grown on InSb substrates

In order to understand the fundamental physics that limits the record efficiencies of polycrystalline and monocrystalline CdTe solar cells, it is highly desirable to have a model system in which various defect recombination mechanisms can be studied in a controlled manner. A double heterostructure (DH) with type-I band edge alignment provides a model system where the middle CdTe layer can be isolated and studied. Using steady-state photoluminescence (PL) and time-resolved photoluminescence (TRPL) measurements, the recombination mechanisms of bulk CdTe epilayers can be studied without the influence of surface recombination and carrier diffusion to the buffer layers and substrate. These DHs have been used in devices such as LEDs and lasers for many years by the MBE community [17]. It is also the standard structure for MBE calibration samples, of which the PL intensity and peak position give information about the optimal growth conditions and alloy compositions, respectively. However, these structures are not

currently used by the CdTe community. For example, researchers use TRPL to study the properties of poly-CdTe solar cell structures [13]. The measured PL lifetime is related to the material quality but is complicated by the carrier dynamics of the PN junction. It is then necessary to perform simulations in order to analyze the multiple exponential decay characteristics observed in the TRPL. Another example is in the growth quality optimization of MBE-grown CdTe. Previous studies have used plain CdTe epilayers grown on InSb substrates without any carrier confinement [18, 19]. Surface recombination is likely to dominate in those samples, and the density and nature of surface states may be affected by the growth conditions. Therefore, the PL intensity may not be indicative of the bulk material quality but rather the impact of the surface. The aforementioned DH design is ideal for material quality investigation and optimization because of the relative simplicity of the PL analysis. Alternatively, surfaces and interfaces can be studied by growing samples with appropriate layer structures that separate the photogenerated carriers from the surface or interface, respectively. It is then clear that intelligent structure design coupled with PL measurements allows one to gain significant insight into material properties.

MgCdTe is the most practical alloy to form a barrier with CdTe. Figure 1.1 shows the band gap vs. lattice constant of many common semiconductors, where the lines connecting the binary materials represent random alloys containing the common cation or anion. The first consideration in choosing a barrier layer is the lattice constant and band gap. It is generally desirable for a device structure to be made of materials which are all lattice matched so that thick dislocation-free layers can be grown. MgCdTe, although not lattice-matched, provides the largest increase in band gap for the same corresponding

change in lattice constant. Alloys with Zn, Be, and S also increase the band gap but correspond to a large decrease in the lattice constant, making them undesirable for CdTe-based barrier layers. The second consideration is the band alignment and offsets. MgCdTe has a type-I band alignment with CdTe, and the valance band offset is 30 % of the difference between the two band gaps [20]. In a DH used for PL and TRPL measurements, it is desirable to have both electron and hole confinement in the conduction band and valance bands, respectively. MgCdTe can therefore provide the necessary confinement for both electrons and holes, and the dislocation density can be minimized by using thin layers with a moderately small Mg composition.

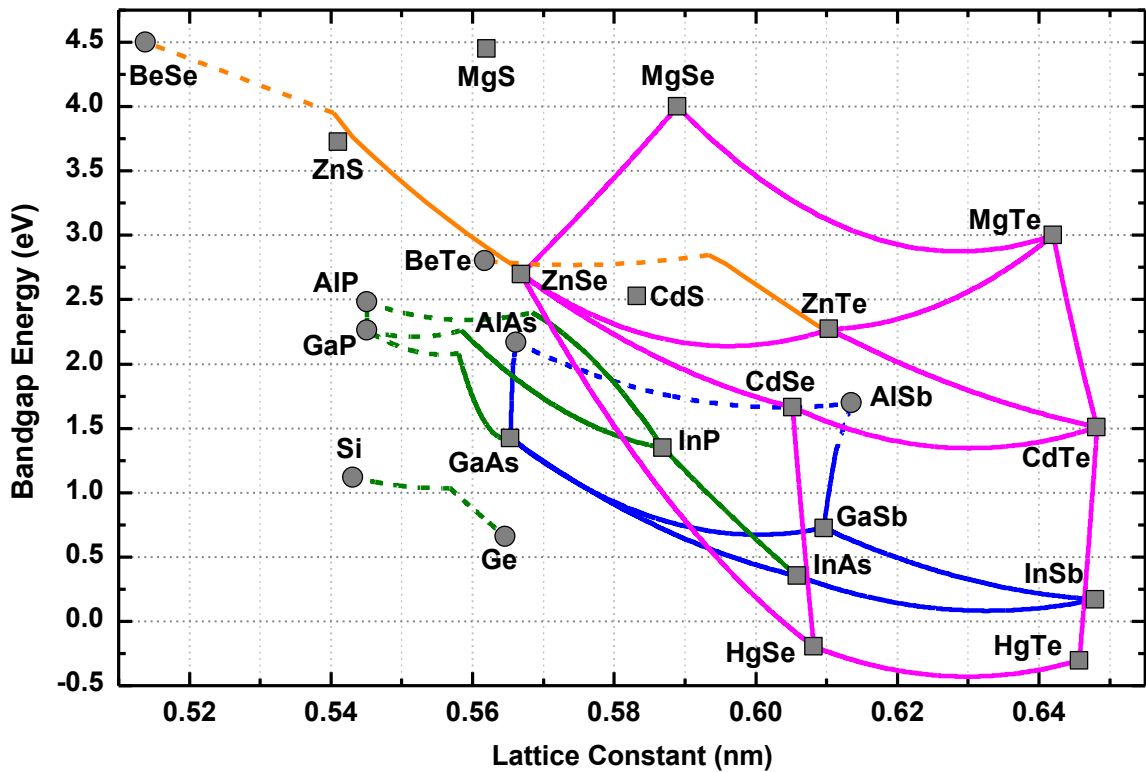


Figure 1.1. A diagram of experimentally measured band gaps vs. lattice constants of common semiconductors. Solid and dashed lines represent direct and indirect band gap alloys, respectively. *Figure provided by Dr. Ding Ding at ASU.

CdTe can be grown on several commercially available substrates, but InSb is the most practical based on lattice mismatch, cost, and pre-existing knowledge of buffer layer growth procedures. The lattice mismatch between CdTe and InSb is incredibly small, only 0.03 %. This is even better than the famous GaAs/AlAs system which has a mismatch of 0.136 %. InSb wafers are commonly used for IR photodetectors and are available in diameters from 2" to 5" with impressive etch pit densities (EPD) of less than 50 cm^{-2} [21]. The cost of an InSb substrate is roughly $\$22 \text{ cm}^{-2}$, which is considerably less than that of CdTe which is about $\$500 \text{ cm}^{-2}$ and is only commonly available in $1 \text{ cm} \times 1 \text{ cm}$ square pieces. Furthermore, the EPD of a CdTe wafer is around 3 orders of magnitude larger than that of InSb [22]. Since the etch pits are indicative of dislocations in the wafer, higher quality CdTe epilayers should be possible using InSb as long as an abrupt interface can be formed and the CdTe critical thickness is not exceeded. CdTe can be grown on GaAs using a ZnTe intermediate layer, but the severe lattice mismatch will result in lower material quality [23]. This structure may be useful for studying the effect of dislocations on CdTe, rather than for demonstrating the highest quality CdTe material or solar cell. Finally, it should also be noted that the growth of CdTe/MgCdTe structures has been previously demonstrated [24], and the growth of CdTe on InSb has also been demonstrated [25]. The novel aspect of this research is the combination of those two ideas for the applications of growth quality optimization, recombination physics investigation, and the exploration of the limits of CdTe solar cell efficiency.

1.2 Organization of the dissertation

Chapter 2 discusses the designs of the CdTe/MgCdTe PL structures used in this study, along with the basics of PL measurements. The choice of composition and

thickness of each layer is determined based on several considerations: critical thickness, barrier heights, and absorption of the PL pump laser. Several different structures are presented in order to determine various physical characteristics of CdTe. These characteristics are the bulk SRH recombination lifetime of CdTe, interface recombination velocity of the CdTe/MgCdTe interface, effect of surface recombination and diffusion of carriers to the buffer layers and substrate, and the effect of the growth temperature and Cd/Te flux ratio on the SRH lifetime of CdTe. An identical GaAs/AlGaAs DH is also grown as a comparison sample, and its sample structure is briefly discussed.

Chapter 3 discusses the MBE growth of the previously mentioned structures. This includes the fundamentals of MBE, *in-situ* characterization techniques, growth rate and Cd/Te flux ratio calibration, and specific details and procedures necessary for obtaining high quality materials. A growth condition optimization experiment is designed based on previous reports in literature. The goal is to increase the carrier lifetime in CdTe by finding the optimal substrate temperature and Cd/Te flux ratio.

Chapter 4 discusses the structural characterization of CdTe/MgCdTe DHs. Atomic force microscopy (AFM) is used to measure the surface roughness as a function of the growth conditions. Transmission electron microscopy (TEM) is used to show the crystalline quality of the InSb/CdTe interface. Finally, X-ray diffraction (XRD) and reciprocal-space maps (RSMs) are used to measure relaxation in the films, the composition of the MgCdTe barrier layers, and the overall crystalline quality of the structure.

Chapter 5 discusses the optical characterization of the samples, which includes PL and TRPL. The PL intensity is correlated with the carrier lifetime, as measured by TRPL.

It is shown through TRPL that the PL measurement conditions are performed under low injection, which is necessary to correlate the PL lifetime with the carrier lifetime. The lifetime is the most important metric used for gauging the material quality because it directly impacts solar cell performance and it is sensitive to both dislocations and point defects.

Chapter 6 discusses PN junction theory and how it relates to solar cells, along with the design of a ZnTe/CdTe/MgCdTe DH solar cell. This structure design is chosen over a MgCdTe/CdTe/MgCdTe DH because of the doping limitations of the II-VI chamber at ASU. This is explained in more detail within the chapter. Numerical simulations using the software PC1D [26] are used to optimize the structure design and to determine which design parameters have the greatest effect on the efficiency.

Lastly, chapter 7 discusses the growth, processing, and testing of the ZnTe/CdTe/MgCdTe DH solar cells. Testing of the solar cells includes current density vs. voltage ($J-V$) measurements both in the dark and under 1 sun concentration, as well as external quantum efficiency (EQE) measurements. These measurements coupled with additional modeling are used to explain the low efficiency measured for these devices. Future recommendations are presented, and the dissertation ends with a conclusion.

CHAPTER 2

PHOTOLUMINESCENCE STRUCTURE DESIGN

CdTe photoluminescence (PL) layer structures are designed for the purpose of material characterization. The choice of barrier material, thickness, and alloy composition is based on the critical thickness and band offsets for that material with respect to CdTe. The basics of PL measurements are discussed, and several structures are presented which are useful for probing various material properties.

2.1 Critical thickness of CdTe and MgCdTe on InSb

One of the first considerations when designing a device structure is the critical thickness of lattice-mismatched epilayers. The critical thickness, denoted as h_c , is defined as the maximum thickness of an elastically strained epilayer in which the substrate and epilayer have the same in-plane lattice constant. Above the critical thickness, strain in the epilayer is relaxed by the formation of misfit dislocations. As more dislocations are generated, the lattice constant of the epilayer approaches its natural bulk value, and the layer becomes fully relaxed. Below the critical thickness, the epilayer is under compressive or tensile strain as it tries to match the in-plane lattice constant of the substrate. When there is no relaxation, the layer is referred to as coherently strained. For the materials considered here, CdTe grown on InSb is under a small compressive strain, while MgCdTe is under moderate tensile strain. It is generally known that dislocations act as non-radiative deep-level recombination centers, so the design must not allow for relaxation.

The critical thickness of CdTe and $\text{Mg}_x\text{Cd}_{1-x}\text{Te}$ on InSb is calculated using two different models, as shown in Fig. 2.1. The first model is one proposed by Matthews and

Blakeslee which involves balancing the line tension of a dislocation and the stress caused by the lattice mismatch [27]. It was originally proposed for the GaAs/GaAsP system. The critical thickness is given by:

$$h_c = \frac{a_s \left(1 - \frac{\nu}{4}\right) \left[\ln \left(\frac{h_c \sqrt{2}}{a_s} \right) + 1 \right]}{k \sqrt{2\pi} |f| (1 + \nu)}, \quad (2.1)$$

$$\nu = \frac{C_{12}}{C_{11} + C_{12}}, \quad (2.2)$$

$$f = \frac{a_s - a_l}{a_l}, \quad (2.3)$$

where a_s and a_l are the substrate and epilayer lattice constants, respectively, ν is Poisson's ratio, C_{11} and C_{12} are the elastic stiffness parameters of the epilayer, and k is a constant equal to 4 for single epilayers (as opposed to quantum wells and superlattices). The material parameters are given in Appendix A. This model gives a critical thickness for CdTe on InSb of only 620 nm. The second model, proposed by Fontaine, *et al.*, is based on empirical XRD measurements of CdTe grown on $\text{Zn}_{0.04}\text{Cd}_{0.96}\text{Te}$ substrates [28]. XRD is used to measure the in-plane lattice constant, which is then used to calculate the stress of the epilayer. They found that above a critical thickness, the product of stress and the thickness remains constant, which indicates that the 2D density of misfit dislocations is increasing as the epilayer thickness increases. The critical thickness is therefore determined by the empirical measurement of the maximum stress-thickness product and is given by:

$$h_c = \frac{\Sigma_{001}}{H_{001} |f|}, \quad (2.4)$$

$$H_{001} = C_{11} + C_{12} - \frac{2C_{12}^2}{C_{11}}, \quad (2.5)$$

where H_{001} is the biaxial modulus, and Σ_{001} is the product of stress and the critical thickness which is equal to $46 \text{ J}\cdot\text{m}^{-2}$ for CdTe according to XRD measurements [28]. Equations (2.4) and (2.5) give a critical thickness of $3.8 \text{ }\mu\text{m}$ for CdTe on InSb, which is nearly an order of magnitude larger than the Matthews-Blakeslee model. The discrepancy could be explained by the differing nature of dislocations in the GaAs/GaAsP and CdTe/InSb systems, which is beyond the scope of this dissertation. For the purpose of designing a PL structure, it appears that the model proposed by Fontaine, *et al.* may be the most relevant to the CdTe/MgCdTe/InSb system.

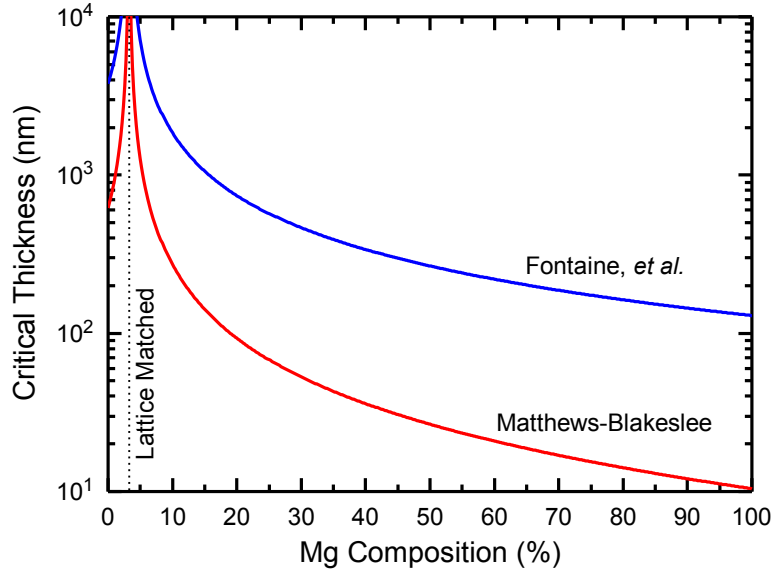


Figure 2.1. Calculated critical thickness of $\text{Mg}_x\text{Cd}_{1-x}\text{Te}$ on InSb using two different models.

2.2 Design of the MgCdTe barrier layer

The MgCdTe barrier layer must meet several criteria in order to be both practical and effective. The composition and thickness must be carefully chosen based on

electronic, optical, and growth (materials) perspectives. From an electronic perspective, the potential energy height of the barrier (known as barrier height) must be large enough to block thermally-excited high-energy carriers. One can set an arbitrary minimum barrier height of $3k_B T$, where k_B is the Boltzmann constant and T is the temperature in kelvin. At room temperature, $3k_B T$ is roughly equal to 76 meV. The barrier height is determined by the Mg composition of the alloy, as shown in Fig. 2.2. The upper limit of the Mg composition is determined by the reactivity of Mg in air (specifically water). Alloys up to 65 % have been shown to be stable [24], while pure MgTe reacts with air. As for the thickness of the barrier, it must be thick enough to prevent quantum tunneling. A minimum barrier thickness of a few tens of nanometers is generally considered to be sufficient to prevent tunneling. The maximum barrier thickness is determined by the critical thickness and absorption losses of the PL pump light. As shown in Fig. 2.2, a Mg composition of 18 % gives a valance band offset of $\Delta E_v = 80$ meV and a conduction band offset of $\Delta E_c = 188$ meV. 30 nm is chosen as the thickness since it is sufficient enough to prevent tunneling and is well below the critical thickness as determined by the Matthews-Blakeslee model. 18 % Mg composition therefore is the lower limit for this structure. It will be shown later through experiments that the barrier is sufficient to block the diffusion of photogenerated carriers.

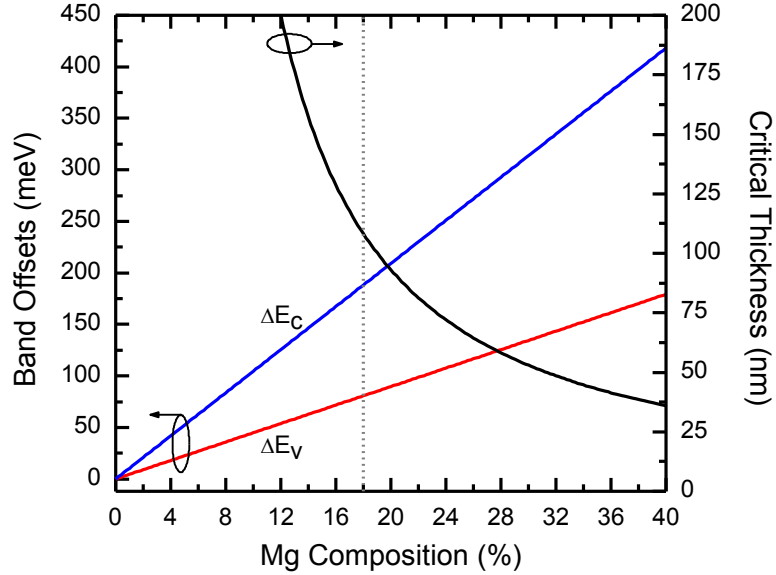


Figure 2.2. Band offsets for CdTe/Mg_xCd_{1-x}Te, assuming that MgTe has a band gap of 3.0 eV, band gap bowing is negligible, and ΔE_V is 30 % of the difference in the band gaps. The critical thickness is calculated using the Matthews-Blakeslee model as a conservative estimate.

The effect of strain on the MgCdTe barrier layer must also be considered. Tensile strain causes the band gap to be reduced, while the heavy- and light-hole bands split. The magnitude of this effect is determined by the amount of strain, the elastic stiffness parameters, and the deformation potentials [17, pp. 136-138]. Some of the deformation potentials are not known accurately for CdTe [29], so the largest value is assumed as a conservative estimate. Based on the equations provided by Chuang [17, pp. 136-138], the maximum band shifting that can be expected is only 9 meV each for the valance and conduction bands. The splitting of the heavy and light hole bands is less than 1 meV. It can therefore be concluded that the effect of strain on the band edges is negligible, since the band offsets are still close to $3k_B T$.

2.3 Basics of PL measurements and PL sample structure designs

A typical PL measurement setup is shown in Fig. 2.3. The sample is mounted on the cold finger of a cryostat in a position perpendicular to the optical input axis of the spectrometer. A 532 nm laser diode is used as the pump source because that wavelength is readily absorbed by CdTe, and the absorption coefficients of CdTe and GaAs are similar at that wavelength [30]. The laser passes through a chopper wheel to modulate the excitation source, which allows for the lock-in technique to be used. The laser is then focused onto the sample with a spot size around 50 μm . Photoluminescence from the sample is collected by a series of lenses and an image of the PL spot is focused onto the entrance slit of the spectrometer. The light then reflects off of two diffraction gratings placed in series, which disperses the PL light across the exit slit. By rotating the gratings, the spectrometer acts as a tunable bandpass filter. The resolution of the spectrometer is determined by the entrance and exit slit widths, which are typically around 1 mm. A photomultiplier tube (PMT) is used to detect the PL light that passes through the exit slit. Lastly, a lock-in amplifier is used to selectively measure the PL signal which is modulated at a frequency around 100 Hz by the chopper wheel. A similar setup is used for TRPL measurements, with some modifications. The laser diode and chopper is replaced with a 530 nm high speed pulsed laser operating at 2 MHz with a peak width of 6 ps. A high speed PMT is used, and the lock-in amplifier is replaced with a time-correlated single-photon counting system. Also, a single grating spectrometer is used for higher throughput and wider spectral bandwidth.

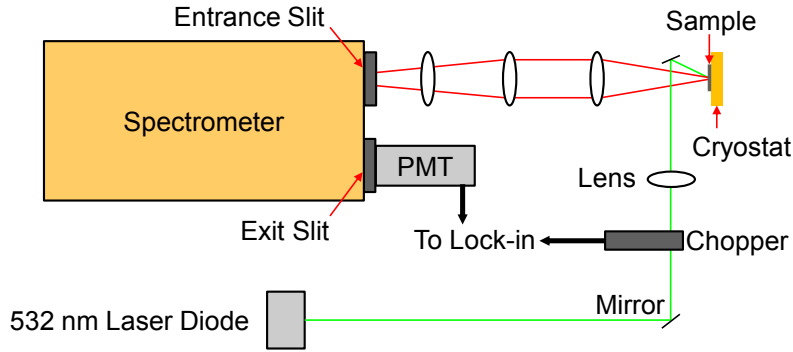


Figure 2.3. Basic setup for steady-state PL measurements.

The layer structure and schematic band edge diagrams for the CdTe/MgCdTe DH are shown in Fig. 2.4. An identical GaAs/AlGaAs DH sample is also grown using the same layer thicknesses and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ barrier layers. The main objective of the design is to generate carriers in the 1 μm thick middle layer using the pump laser, and then capture the luminescence from that layer. The two barriers prevent the carriers from diffusing to the surface and buffer layers. The cap layer is used as a precaution to prevent oxidation of the MgCdTe and AlGaAs barriers, while the buffer layers are used to smooth the surface of the wafer, which improves the material quality of the subsequent layers. The thickness of the middle layer is designed so that very few photons reach the buffer layers. This is done so that PL is not generated in those layers, which would make analysis more difficult. Table 2.1 shows the various loss mechanisms for the pump laser, which is calculated using the Beer-Lambert law for absorption and assuming the laser is at normal incidence to the sample. Since only a small fraction of the pump light reaches the back barrier, it can be assumed that the buffer layer doesn't contribute significant PL.

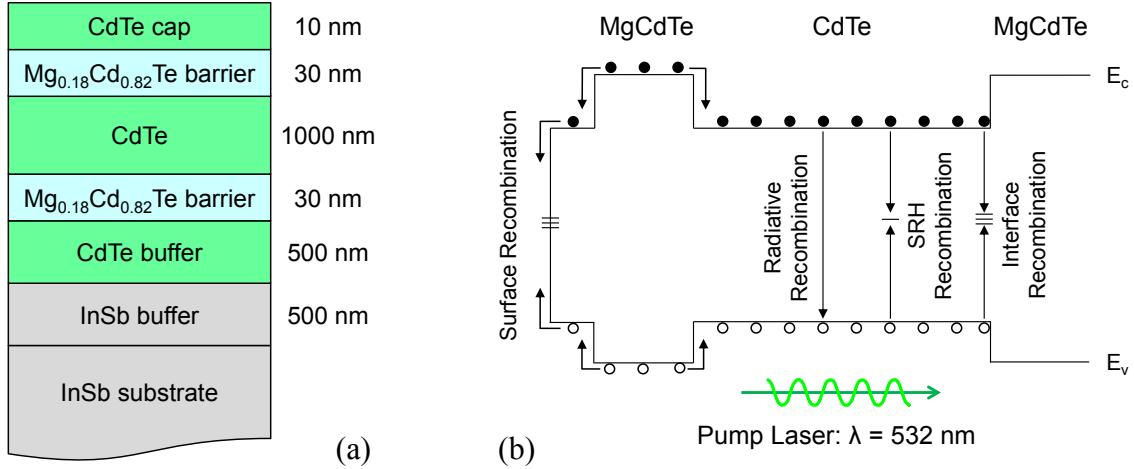


Figure 2.4. (a) Layer structure diagram and (b) schematic band edge diagram for the CdTe/MgCdTe DH PL structure.

Table 2.1. Absorbed pump light in various layers.

	CdTe/Mg _{0.18} Cd _{0.82} Te	GaAs/Al _{0.30} Ga _{0.70} As
Surface reflection	27.1 %	37.4 %
Cap layer absorption	5.30 %	4.25 %
Top barrier absorption	9.90 %	6.25 %
Transmission into back barrier	0.03 %	0.05 %
Total pump light absorbed by middle layer	57.7 %	52.1 %

The schematic band edge diagram in Fig. 2.4b shows the various recombination mechanisms and carrier diffusion, which are expected for the DH. First, electron-hole pairs (EHPs) are generated with a total energy of 2.33 eV, which is equal to the energy of the pump photons. EHPs are mostly generated in the cap, top barrier, and middle layers, as outlined in Table 2.1. The carriers relax to the band edge by emitting phonons, and the carriers can diffuse for a short period of time before recombining. The four significant recombination mechanisms expected for this structure are radiative, Shockley-Read-Hall (SRH), CdTe/MgCdTe interface, and surface recombination. In the cap layer, it is assumed that surface recombination dominates over the other three recombination mechanisms, since the surface is not passivated and there is a high density of surface

states. Carriers generated in the cap layer will be trapped by the MgCdTe barrier and will mostly recombine through surface recombination. Carriers in the barrier layer will quickly diffuse to the lower band gap CdTe layers, and so very little recombination should take place there. Within the middle CdTe layer, only SRH, interface recombination, and radiative recombination are likely to take place. This is because the pump laser is not powerful enough to create the high carrier concentrations which are necessary for Auger recombination. Therefore, the vast majority of PL photons detected should come only from the middle CdTe layer, and the intensity and carrier lifetime observed should be indicative of the bulk and interface properties of the middle CdTe layer.

Two additional layer structures are shown in Figs. 2.5 and 2.6 which are designed to measure the effect of surface and buffer layer recombination, respectively. Both structures are similar to the DH discussed previously, except one of the barriers is omitted from the design. For the structure shown in Fig. 2.5, EHPs are mostly generated in the first few hundred nanometers of the top CdTe layer. Those carriers can diffuse and recombine via surface recombination, in addition to radiative, SRH, and interface recombination. Likewise, for the structure shown in Fig. 2.6, a majority of EHPs are generated in the 1 μm thick CdTe layer. Those carriers can then diffuse to the CdTe/InSb interface and recombine via interface recombination or within the InSb buffer layer. The relative effect of these recombination mechanisms can be determined by comparing the PL intensity of these structures to the DH sample. Furthermore, the comparison also qualitatively indicates the effectiveness of the MgCdTe barrier layers. If the barriers have

relatively low interface recombination velocity, then the PL intensity of the DH sample should be much larger than that of the single barrier samples.

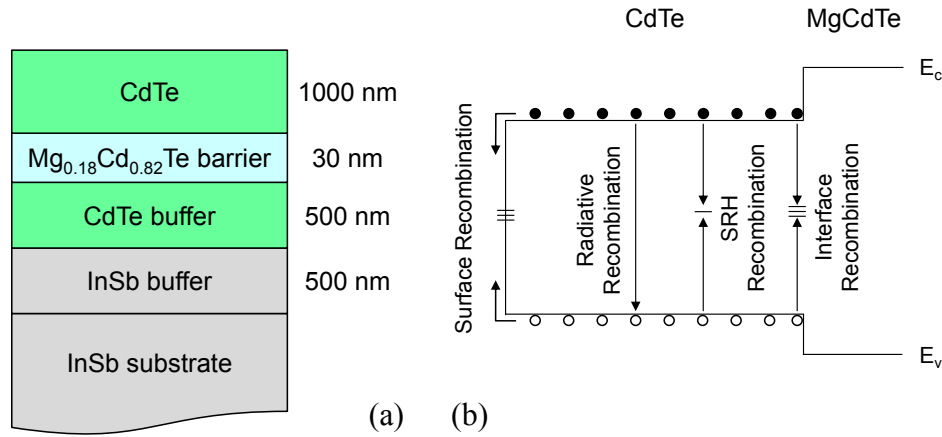


Figure 2.5. (a) Layer structure diagram and (b) schematic band edge diagram for the CdTe/MgCdTe single barrier structure (bottom only).

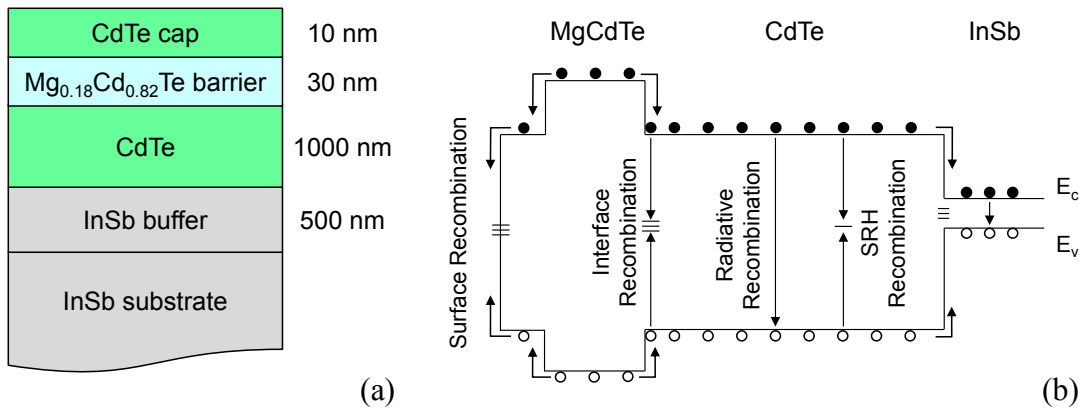


Figure 2.6. (a) Layer structure diagram and (b) schematic band edge diagram for the CdTe/MgCdTe single barrier structure (top only).

In summary, various structures can be used to selectively test the effect of different recombination mechanisms. The double heterostructure (or double barrier) design is used for probing the bulk properties of CdTe, while single heterostructure (or single barrier) designs are used for probing the surface and buffer layers. The following chapter discusses how the material quality of CdTe/MgCdTe DHs are optimized. The single barrier structures are then grown using the optimized growth conditions.

CHAPTER 3

MOLECULAR BEAM EPITAXIAL GROWTH OF CdTe/MgCdTe ON InSb

The fundamentals of MBE are discussed, with emphasis on the concepts that are important for the high-quality growth of monocrystalline layers. A brief literature review of CdTe growth is presented in order to lay the foundation for designing a growth optimization experiment. *In-situ* characterization techniques and basic calibration results are also discussed.

3.1 Fundamentals of MBE and overview of growth

Molecular beam epitaxy (MBE) is a semiconductor deposition technique which offers several unique advantages compared to other techniques. Generally speaking, deposition (henceforth referred to as growth) using MBE involves exposing a heated wafer to atomic or molecular fluxes, which takes place inside an ultra-high vacuum (UHV) chamber. Wafer heating is necessary to improve the surface migration of adsorbed atoms and to sublimate excess flux from the surface, both of which ensure that stoichiometric films can be grown with high structural quality. For example, high-quality stoichiometric GaAs is routinely grown with As/Ga flux ratios of 1.5 when the substrate is heated to around 550 °C. Without substrate heating, which is typical in thermal and electron-beam evaporation, the flux will condense on the wafer without preference for forming a stoichiometric single crystal. Having the ability to heat the substrate also allows for thermal oxide removal and decontamination of the wafer surface prior to deposition. This is essential for forming a good interface and a film with low dislocation density. The UHV condition is also necessary to remove wafer contamination and to reduce the bulk impurity density in the epilayer. Wafers and their holders are typically

decontaminated (outgassed) using a substrate heater in a separate UHV chamber attached to the growth chamber. Without UHV, residual gases such as H₂O, O₂, and CO₂ will condense back on the wafer and re-contaminate the surface. Wafers are outgassed in a separate chamber to prevent contamination of the growth chamber, since the epilayer impurity density is a function of the background pressure in the growth chamber. For example, to obtain a C impurity concentration less than 10¹⁴ cm⁻³ at a growth rate of 1 μm/h, the CO partial pressure in the chamber must be less than 2×10⁻¹² Torr [31, pp. 1-38]. This is easily possible using available pump and chamber technologies, as well as maintaining cleanliness during maintenance periods when the chamber is opened.

MBE also allows for several *in-situ* characterization and process monitoring techniques. Flux monitoring, substrate temperature measurement, and reflection high-energy electron diffraction (RHEED) are the most used in this study. Flux monitoring is used prior to growth to measure the relative flux vs. temperature characteristic of the cell. This is performed by placing an ion gauge in front of the substrate and measuring the resulting ion gauge current from the cell as the temperature is adjusted. This is important for calibrating the flux ratio, as will be discussed later. Substrate temperature measurements are performed during every growth using a pyrometer. The pyrometer is a calibrated InGaAs photodetector which senses the blackbody radiation from the wafer. Based on the intensity of thermal radiation and emissivity of the wafer at the detection wavelength, the temperature is calculated using Planck's law. Detection wavelengths of 950 nm and 1150 nm are used for GaAs and InSb wafers, respectively. It's important to note that the wafers are opaque at those wavelengths (due to optical absorption above the band gap), which is necessary for detecting blackbody radiation from the semiconductor.

The pyrometer used for the InSb wafer allows for temperature measurements down to 250 °C, which is useful for CdTe growth at low temperatures.

RHEED is the most important *in-situ* characterization technique used in this study, simply because of the vast amount of information it provides about the growth. In this technique, a collimated electron beam with a diameter of a few mm strikes the wafer at a glancing angle of only a few degrees from the surface. The electron kinetic energy is 15 keV, and so the electron wavelength is much less than the lattice spacing. Electrons diffract off of the wafer surface and form an image on a phosphor screen, creating what is called a RHEED pattern or image. Because of the glancing angle of the electron beam, only the top few monolayers (MLs) will contribute to the RHEED image, which makes this technique highly sensitive to the atomic configuration of the surface. Several characteristics can be observed. First, surfaces that are oxidized will give hazy RHEED patterns because of the random arrangement of atoms on the surface. This is important for monitoring the oxide removal process. In contrast, smooth surfaces of a monocrystalline wafer will give a pattern of parallel streaks. The brightness and spacing of the streaks is indicative of the atomic periodicity of the surface. Atoms on the surface of a crystal will re-arrange themselves to form the lowest energy state, which is referred to as a surface reconstruction. It is widely known that the reconstruction (and therefore RHEED pattern) is sensitive to the material being deposited, the lattice spacing near the surface, and the growth conditions including substrate temperature (T_s) and flux ratio. RHEED is most useful during growth for monitoring the surface condition, which can drastically change if there's a system problem or error. For example, if a shutter fails to open, the surface can become rough and the RHEED pattern will become spotty. This

technique is also useful for measuring the growth rate. It's commonly observed that the intensity of the zero order diffraction streak oscillates during growth, with each oscillation corresponding to the growth of 1 ML [31, pp. 1-38]. This oscillation is observed for the 2D growth mode, which starts with the formation of 1 ML thick islands followed by a coalescence of those islands. The growth rate can then be used to determine the 1:1 flux ratio, as described in section 3.3.

The MBE system used in this study is a dual-chamber "solid-source" MBE system which was recently upgraded to grow II-VI materials. Two separate chambers are used to grow III-V and II-VI materials in order to prevent cross contamination. Specifically, As is known to be highly mobile in a vacuum chamber, while Cd and Se have similar vapor pressures to As [32]. The chambers are connected by a UHV transfer chamber, which has a heating stage for outgassing wafers. The system is considered to be "solid source" because there are no gas sources (AsH_3 , PH_3 , etc..), although some of the sources are operated above the melting point (notably Ga and Al). For MgCdTe growth, three separate cells are used which consist of graphite crucibles loaded with pieces of Mg, Cd, and Te. The crucibles are heated using tantalum filaments and the temperature is monitored using a thermocouple.

The growth procedure for CdTe samples is briefly outlined in the following. First, a 2" InSb wafer is diced into quarters, and one piece is mounted onto the center of a 3" Si wafer using indium. The Si carrier wafer is mounted on a molybdenum holder and loaded into the system. Note that for the solar cell growths described in chapter 7, whole 2" InSb wafers are loaded in place of the Si carrier wafer, and no indium is used. The wafer and holder is outgassed at 200 °C for 1 hour and then transferred to the III-V chamber for

oxide removal and buffer layer growth. The conditions for oxide removal and InSb growth has been reported elsewhere [33]. After the InSb buffer layer growth, the wafer is transferred to the II-VI chamber and the temperature is raised to the desired growth temperature. At this time, the cells have already been brought up to the operating temperature and stabilized for 30 minutes. At $T_s = 240$ °C, the Cd shutter is opened in order to saturate the surface with Cd. It is known that group VI elements react with group III [34], so a half monolayer of Cd is deposited on the surface before the Te shutter is opened. The Cd shutter can be left open for several minutes, since the substrate temperature is high enough to prevent multiple layers from depositing. When the substrate temperature is stabilized, a computer program is initiated which starts the growth and controls the Mg, Cd, and Te shutters and cell temperatures. An initial Cd/Te flux ratio of 3.5 is used for the first two minutes of growth in order to further prevent the reaction of Te with the substrate [34]. The flux ratio is then ramped down to the desired value within 5 minutes. Figure 3.1 shows typical RHEED patterns for InSb directly after transfer into the II-VI chamber and CdTe after 10 minutes of growth. The streaky patterns indicate that relatively smooth, monocrystalline layers have been grown. When the growth is complete, the shutters are automatically closed and the wafer temperature is ramped down. The wafer holder is then unloaded and the InSb piece is removed from the Si carrier wafer.

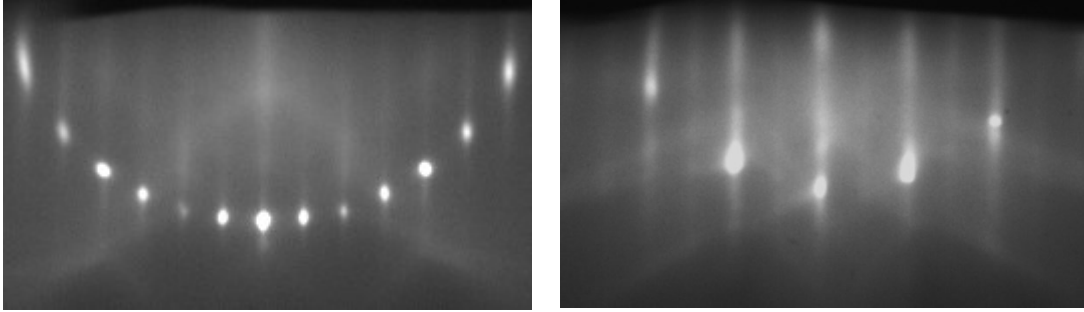


Figure 3.1. RHEED patterns along the (001) direction for InSb at 200 °C (left) and along the (011) direction for CdTe at 265 °C (right).

3.2 Review of CdTe/MgCdTe growth conditions

Several studies have been published on the growth of CdTe and MgCdTe, although none of the studies give a comprehensive overview of the entire parameter space. In order to be considered “comprehensive,” the growth quality must be studied as a function of substrate temperature, flux ratio, growth rate, and preparation procedures. The metric for growth quality will depend on the desired outcome; in this case an improvement in the carrier lifetime is desired. Several factors likely contribute to the relative lack of data in the literature, such as the cost of substrates and source material (particularly CdTe wafers and Mg source material), insufficient “critical mass” of researchers in the II-VI area, and the use of polycrystalline material for low-cost photovoltaics instead of high-quality monocrystalline material. However, there have been some basic studies, particularly in the ‘80’s and early ‘90’s. These studies act as a guide for further exploration of the growth parameter space.

Several material properties must be simultaneously considered when defining the practical limits of the growth window. Table 3.1 shows the equilibrium vapor pressures for various elements at 300 °C, which is a common growth temperature for CdTe. In general, a non-unity flux ratio is typically used, where the material with the larger vapor

pressure has the larger flux. For GaAs, excess As is provided and the growth rate is determined only by the Ga flux. On the other hand, Cd has a higher vapor pressure than Te, so conventional wisdom would say that the material should be grown in Cd-rich conditions.

Table 3.1. Equilibrium vapor pressures [32].

Element	Vapor pressure at 300 °C (Torr)
Mg	2×10^{-5}
Cd	4×10^{-2}
Te	1×10^{-4}
Ga	$\ll 1 \times 10^{-8}$
As	4×10^{-2}
Sb	5×10^{-8}

An experimental study which measured the lower growth temperature limit concluded that Cd-rich growth conditions lead to higher quality CdTe [35]. It is shown that there is a minimum threshold temperature for which monocrystalline CdTe can be formed, below that temperature polycrystalline material is obtained. This threshold is 205 °C for Te-rich growth and only 85 °C for Cd-rich growth. Polycrystalline material is usually formed when the surface migration is too low to form an ordered crystal, so this finding suggests that Cd-rich surfaces have higher migration of adsorbed atoms (adatoms). It is desirable to maximize the adatom migration using flux ratio rather than using a higher growth temperature, since the formation of point defects such as vacancies and interstitials increases with temperature [31, pp. 1-38]. Therefore, the flux ratio is just as important as the growth temperature when optimizing the growth conditions.

The maximum growth temperature is determined by the desorption rate and the tolerance for point defects. RHEED oscillations have been used to measure the desorption rate of CdTe as a function of temperature [24]. A maximum growth

temperature of 340 °C corresponds to a desorption rate of 0.16 Å/s, which is 10 % of the growth rate used in this study (1.6 Å/s). The effect of point defects is more difficult to determine. One study reported the low temperature (2 K) PL spectra of samples grown at different temperatures and concluded that 185 °C is the optimal growth temperature [18]. This optimization is based on maximizing the ratio of free-excitation emission intensity to deep level photoluminescence. Unfortunately, the analysis of the result is complicated by the fact that a compound CdTe source was used for growth, so the surface condition (Cd or Te rich) could not be controlled. Also, this temperature seems unusually low in comparison to the commonly used substrate temperature of 300 °C [31, pp. 311-341].

For the growth of MgCdTe, there are no publications on the optimization of the growth conditions, however MgCdTe/CdTe structures have been demonstrated [36]. The only information available is that MgCdTe can be grown at the same substrate temperature as CdTe, and that the sticking coefficient of Mg is larger than Cd [37]. Since the growths in this study take place in the Cd-rich regime, there is competition between Mg and Cd for the group II lattice positions. Mg will displace Cd due to its larger sticking coefficient, however it is difficult to predict the Mg composition since the sticking coefficients are not accurately known. X-ray diffraction experiments can be performed to determine the composition, as described in the next chapter.

3.3 Growth calibration and optimization

The calibration of the CdTe growth conditions is performed using RHEED oscillations to measure the growth rate. CdTe is grown on an InSb wafer using the procedures outlined previously. After 30 minutes of growth, the CdTe layer is smooth enough to begin calibrations. A camera and computer software is used to select the zero

order (011) diffraction streak, and the average intensity is monitored over time. The oscillations are initiated by shutting the Te shutter for several seconds, then opening it again to resume the growth. Approximately 10 oscillations occur before the intensity dampens. The software is then used to fit the intensity curve to a decaying sinusoidal curve and obtain the growth rate. Figure 3.2 shows the growth rate as a function of Cd flux with fixed Te flux and a substrate temperature of 265 °C. An almost linear increase in the growth rate is observed with increasing Cd flux, followed by a saturation of the growth rate. The saturation indicates that the growth rate is limited by the Te flux. A growth rate of approximately 1.6 Å/s (576 nm/h) is achieved, which is typical for MBE. The linear and constant portions are extrapolated to find the Cd flux which gives a Cd/Te flux ratio of unity. Non-unity values are then determined using the measured flux vs. cell temperature profile for Cd.

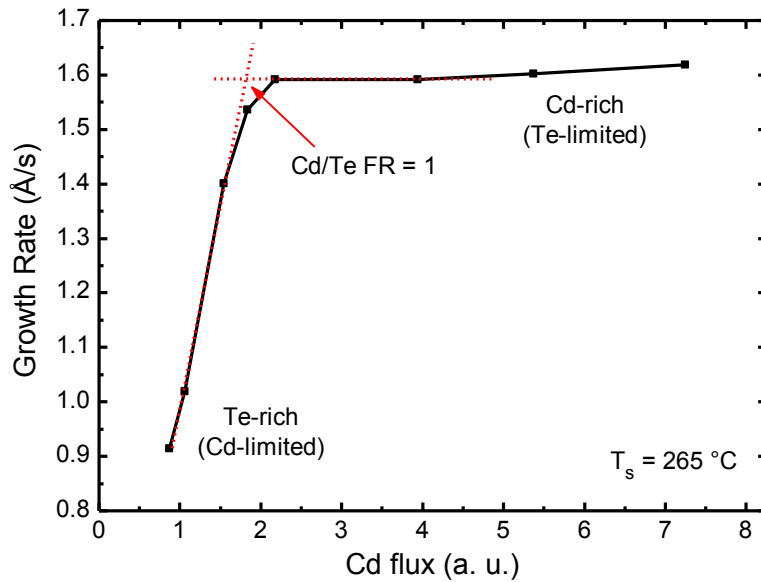


Figure 3.2. CdTe growth rate as a function of Cd flux with the Te flux kept constant. The intersection of the linear region (Cd-limited) and saturation growth rate (Cd-rich) gives the growth conditions where the Cd/Te flux ratio is unity.

A growth optimization experiment is designed to determine the effect of flux ratio and T_s on the carrier lifetime. Table 3.2 shows the “one-factor-at-a-time” design used in this study. The flux ratio is first set to 1.5 and T_s is varied. When the optimal T_s is found, the flux ratio is varied while keeping T_s constant. A flux ratio of 1.5 was chosen as a first guess because that is the flux ratio used for GaAs by our group. Throughout this study, the Mg and Te cell temperatures are fixed at 500 °C and 425 °C, respectively. It should be noted that this design assumes that the growth rate doesn’t change significantly as a function of T_s . Previous studies have shown that the growth rate only varies by 7 % when T_s varies from 235 °C to 295 °C [24].

Table 3.2. Growth conditions and sample numbers for seven samples used in the optimization of the material quality

Cd/Te flux ratio	Substrate temperature (°C)				
	235	250	265	280	295
1.8			A1568		
1.5	A1565	A1564	A1561	A1571	A1566
1.2			A1567		

Lastly, the effectiveness of the MgCdTe barriers are evaluated by growing samples with one of the barriers removed. The growth conditions are similar to that of sample A1561, which is $T_s = 265$ °C and a flux ratio of 1.5. As will be shown in the following chapters, those growth conditions are optimal for CdTe/MgCdTe structures grown on InSb substrates using our MBE system. The sample numbers are A1572 and A1573, which have only the bottom barrier and top barrier, respectively.

CHAPTER 4

STRUCTURAL CHARACTERIZATION OF CdTe/MgCdTe STRUCTURES

Several structural characterization techniques are carried out in order to determine the overall crystalline quality and provide feedback to the grower for calibrating the growth conditions. These measurements are typically carried out when new structures are grown for the first time, or when layer compositions and thicknesses need to be verified. Roughness measurements are carried out on samples used in the growth optimization experiment, the crystalline quality is verified by transmission electron microscopy images, and the Mg composition in the MgCdTe layer is verified by X-ray diffraction measurements.

4.1 Investigation of surface roughness using atomic force microscopy

Surface roughness is one of several metrics which represents the material quality of an epilayer. For ultra-smooth surfaces formed using the 2D growth mode, single step edges with a height of 1 monolayer will be observed. Therefore the surface roughness will be on the order of the monolayer thickness or less. Figure 4.1 shows atomic force microscopy (AFM) images of an InSb buffer layer surface and a CdTe surface after the growth of a CdTe/MgCdTe DH on InSb. The InSb surface has an RMS roughness of 1.86 nm, which is considerably larger than the monolayer thickness. When a smaller region is imaged, each hill is seen to be made of multiple step edges, which indicates a step-flow growth mode for InSb. The CdTe surface shows similar sized features, but the image is blurred and individual step-edges cannot be observed. The reason for the blurred image is not evident, but is repeatable on all CdTe samples.

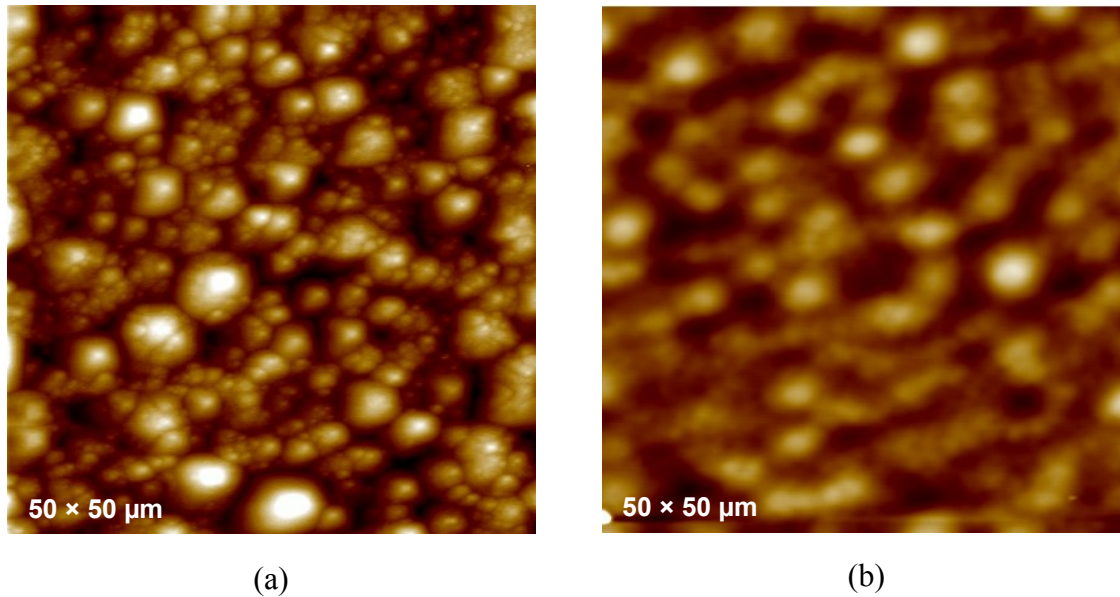


Figure 4.1. Atomic force micrographs of (a) an InSb buffer layer (B2034) and (b) a CdTe/MgCdTe DH grown on InSb with $T_s = 265$ C and a Cd/Te flux ratio of 1.5 (A1579). The z-range for both figures is ± 6 nm.

Figure 4.2 shows the effect of growth conditions on the surface roughness of CdTe/MgCdTe DHs. A clear trend is observed for the effect of growth temperature. Increasing growth temperature leads to smoother CdTe surfaces, which is expected because higher temperature leads to higher adatom migration on the surface during growth. The effect of flux ratio is not obvious since there are not enough data points. However, the lowest surface roughness occurs at the optimal flux ratio (as will be shown in chapter 5). It is important to note that all CdTe surfaces have a smaller RMS roughness compared to the InSb surface, which indicates that smoothing occurs during CdTe growth. Optimization of the InSb growth conditions may lead to smoother surfaces below 1 nm RMS.

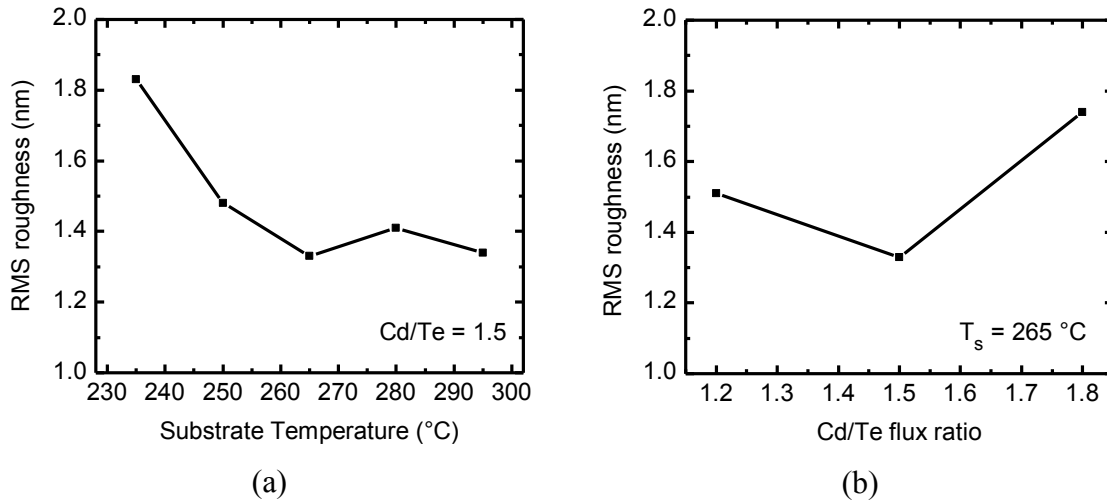


Figure 4.2. RMS surface roughness of CdTe/MgCdTe DHs as a function of (a) substrate temperature T_s and (b) Cd/Te flux ratio.

4.2 Transmission electron microscopy of CdTe/MgCdTe DHs

Transmission electron microscope (TEM) images of the CdTe/MgCdTe DH are taken in order to determine the crystalline quality and thicknesses of all the layers. Figure 4.3 shows a cross sectional TEM image of the lower region of the structure which indicates that all the interfaces are relatively free of defects. Furthermore, the measured thicknesses closely match the design thicknesses for the structure. It should be noted that the speckling of the image is likely due to TEM sample preparation, which is difficult because of the relative softness of both CdTe and InSb.



Figure 4.3. TEM image showing the lower portion of the CdTe/MgCdTe DH. **Image acquired by Jing Lu and Dr. David Smith at ASU.*

4.3 X-ray diffraction measurements of CdTe/MgCdTe DHs on InSb

X-ray diffraction (XRD) is a versatile characterization method which is useful for measuring several properties of a structure, including layer composition, thicknesses, relaxation, and relative dislocation density. The setup consists of a monochromatic, collimated x-ray beam which is directed towards the sample at an angle ω with respect to the wafer surface. X-rays penetrate into the surface up to several microns and diffract off of the atoms back towards the wafer surface, giving rise to intensity variations that can be detected as a function of ω . The measurements used in this study are high resolution ω - 2θ scans, where 2θ is the angle between the x-ray beam and the detector within the plane of incidence. The measurement is high resolution because an x-ray analyzer is used, which limits the acceptance angle of the detector. The angles ω and 2θ are set equal to each

other and scanned within a certain range where diffraction peaks occur. The diffraction is described by Bragg's law:

$$n\lambda = 2d \sin(\omega) , \quad (4.1)$$

where n is the diffraction order, λ is the wavelength of the x-ray beam (1.5406 Å in this case), and d is the spacing between atomic planes. Peaks in the XRD scan correspond to semiconductor layers with a certain periodicity. Since the penetration depth is large, many layers can be detected simultaneously. The geometry of the scan is rather complicated, so the scan is most frequently discussed in terms of reciprocal space. (004) scans take place in the vicinity of the (004) diffraction peak, and likewise for the (115) scan. The former scan gives information about the out of plane (a_{\perp}) lattice constants, while the latter is used to determine in-plane (a_{\parallel}) lattice constants.

Several structural properties can be determined from the scans based on different characteristics. Both a_{\perp} and a_{\parallel} can be measured from the angular position of the diffraction peaks using Bragg's law. If a_{\perp} is the same for all layers in the structure, then the layers are said to be coherently strained. If that condition is not satisfied, then there has been partial or full relaxation of the layer through the formation of misfit dislocations. Assuming the layers are coherently strained, the biaxial strain relationship can be used to determine the Mg composition:

$$\frac{a_{\perp} - a_o}{a_o} = -\frac{2C_{12}}{C_{11}} \times \frac{a_{\parallel} - a_o}{a_o} , \quad (4.2)$$

where a_{\perp} is measured using the (004) ω - 2θ scan, a_o is the lattice constant of unstrained MgCdTe, C_{11} and C_{12} are elastic stiffness coefficients of MgCdTe, and a_{\parallel} is equal to that of bulk InSb. Vegard's law states that the lattice constant of an alloy can be linearly

interpolated between the two constituent binaries, so therefore the composition can be calculated once a_o is known. In addition to composition and relaxation, layer thicknesses can also be determined in some cases. A process similar to thin film optical interference occurs with x-rays, which are known as Pendellösung fringes. The spacing between the fringes is inversely proportional to the layer thickness, and modeling of complex XRD scans can yield certain layer thicknesses. Lastly, the width of the diffraction peak is a function of disorder in the crystal as well as the thickness of the layer. Disorder is often caused by dislocations, which disrupt the periodicity of the crystal. Local variations in the lattice constant which may be caused by relaxation will also broaden the diffraction peak. Therefore it is the goal of the researcher to achieve the narrowest possible diffraction peak for a given layer thickness, and the full-width-at-half-maximum (FWHM) is used to describe the peak width.

Figure 4.4 shows a (004) ω - 2θ scan for a CdTe/MgCdTe DH grown on InSb. The growth conditions are $T_s = 265$ °C with a Cd/Te flux ratio of 1.5. A narrow diffraction peak with a FWHM of 19 arcsec is observed for CdTe (004) diffraction, indicating a relatively low dislocation density. The ω positions of the diffraction peaks are inversely related to a_{\perp} , as the labels indicate. CdTe has the highest intensity because it is close to the surface where less x-ray absorption takes place. MgCdTe has a very broad peak because thin layers in real space appear as broad diffraction peaks in reciprocal space. The intensity is also low because there are fewer atomic planes for diffraction. Narrow Pendellösung fringes of the CdTe layer are clearly observed, indicating smooth DH interfaces. Broad fringes are also observed near the edges of the scan, which are caused by interference from the MgCdTe layers and CdTe cap. Those interference fringes give a

thickness of approximately 30 nm, which is in excellent agreement with the designed thickness.

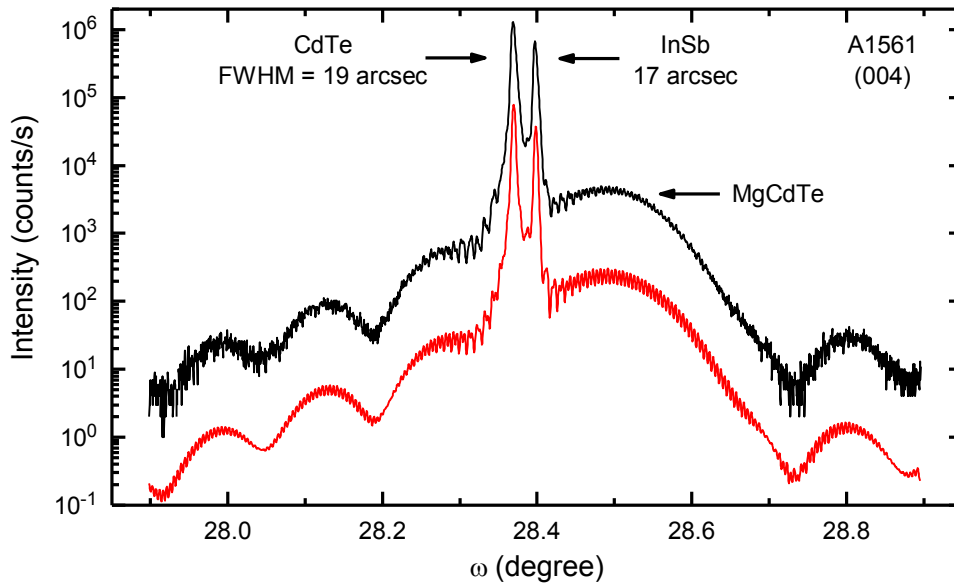


Figure 4.4. X-ray diffraction (XRD) ω - 2θ scan of the CdTe/MgCdTe double-heterostructure sample taken in the vicinity of the (004) diffraction peak. The black curve is the measured diffraction pattern, while the red curve is simulated using the software program X'Pert Epitaxy.

The Mg composition can be found by using the peak position of the MgCdTe diffraction peak and the relations above, however this will lead to substantial error. For the DH samples, the 10 nm thick CdTe cap layer interferes with the MgCdTe layer and forms an intensity envelop which shifts the peak position of the MgCdTe diffraction. Using the relationships above, a Mg composition of 18 % is determined. However, using the XRD simulator program X'Pert Epitaxy version 4.2 with Smoothfit, a composition of 24 % is obtained after using an automatic fitting algorithm. The simulated XRD curve is also shown in Fig. 4.4, which almost perfectly overlaps with the measured curve. Using 18 % Mg composition in the simulation gives a simulated curve that doesn't match the experimental results. Unfortunately, all samples were grown before this issue was

discovered, so all samples have a Mg composition of around 24 % instead of the 18 % target value. Fortunately, the total MgCdTe layer thickness is still below the critical thickness at 24 % composition, and the larger barriers will provide stronger carrier confinement. Therefore, the 24 % Mg composition is satisfactory for the PL sample structures.

Figure 4.5 shows a reciprocal space map (RSM) centered on the (115) diffraction peak for the same structure as discussed previously. The (115) RSM gives two-dimensional information in reciprocal space, which is used to determine whether the layers are coherently strained. As shown in the figure, the diffraction peaks are aligned parallel to the y-axis, which indicates that the in-plane lattice constant of all layers are the same. It can therefore be concluded that all the layers are coherently strained. Likewise, a similar RSM is measured for (004), which indicates that the epilayer crystal structure is not tilted with respect to the substrate [38].

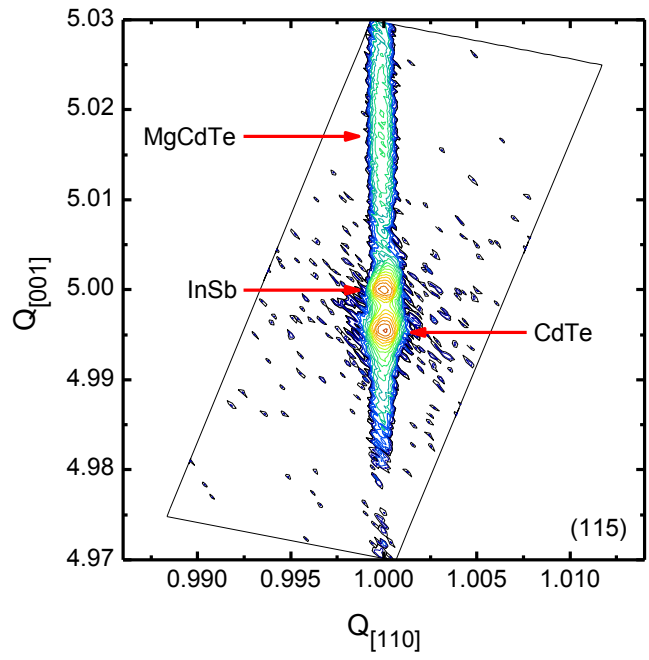


Figure 4.5. Reciprocal space map (RSM) of the CdTe/MgCdTe DH (A1561) in the vicinity of the (115) diffraction peak with contours plotted on a logarithmic scale.

CHAPTER 5

OPTICAL CHARACTERIZATION OF CdTe/MgCdTe STRUCTURES

Photoluminescence measurements are carried out on all of the samples with different structures discussed previously in order to investigate recombination mechanisms that take place. More specifically, the effects of bulk, surface, and interface recombination are quantified. These recombination mechanisms must be understood in order to design working optoelectronic devices. They are also useful for providing feedback to the grower in order to optimize the growth conditions.

5.1 Comparison of steady-state photoluminescence of various structure designs

The photoluminescence intensity of a structure is sensitive to all recombination mechanisms, which includes SRH, radiative, Auger, surface, and interface recombination. All recombination mechanisms act simultaneously to reduce the density of excess electrons (Δn) and excess holes (Δp). In a photoluminescence measurement, electron-hole pairs (EHPs) are generated in equal numbers ($\Delta n = \Delta p$) so that $n = \Delta n + n_o$ and $p = \Delta p + p_o$, where n_o and p_o are the equilibrium electron and hole concentrations, respectively. Under high injection ($\Delta n \gg n_o + p_o$) the recombination rate for the first three mechanisms is given by:

$$R = A\Delta n + B\Delta n^2 + C\Delta n^3, \quad (5.1)$$

where A, B, and C are the SRH, radiative, and Auger recombination coefficients, respectively [17, pp. 40-47]. In this study, low injection conditions are used to determine the properties of SRH recombination, which is necessary to know in order to optimize the growth conditions. To satisfy this condition, it is first assumed that the sample has a background carrier concentration which makes the material slightly n-type. This is a

reasonable assumption because indium, an n-type dopant for CdTe [39, 40], is observed in the CdTe epilayer in concentrations around 10^{15} cm^{-3} using secondary ion mass spectrometry (SIMS) measurements. Under low injection, Auger recombination is negligible and the SRH and radiative recombination rates are given by:

$$R_{SRH} = \frac{\Delta n}{\tau_{SRH}} \quad , \quad (5.2)$$

$$R_{rad} = \frac{\Delta n}{\tau_{rad}} \quad , \quad (5.3)$$

$$\tau_{rad} = \frac{1}{Bn_o} \quad , \quad (5.4)$$

where τ_{SRH} is the SRH lifetime and is assumed to be a constant which is related to the trap density in the material [17, pp. 40-47]. Because of the relatively small value of B, SRH recombination dominates at low injection. Based on these assumptions and Eqs. (5.2) through (5.4), the PL intensity is directly related to the excess carrier concentration. Therefore, the PL intensity can be used to compare the trap density of samples with the same layer structure but grown under different conditions. A similar argument holds true for surface and interface recombination, which are essentially made up of trap states. It will be shown later in chapter 5.2 that interface recombination is quite significant, and that the measured PL intensity is related to both CdTe bulk SRH and CdTe/MgCdTe interface recombination.

Figure 5.1 shows the room temperature PL spectra of three samples: a CdTe/MgCdTe DH grown on InSb using the optimal growth conditions, a 1570 nm thick CdTe layer grown on InSb using similar growth conditions, and a GaAs/AlGaAs DH with identical layer structure design. The power density of the 532 nm laser is 0.1 W/cm^2

for the two DH samples, while the plain CdTe layer needed a larger pump density of 2.1 W/cm^2 in order to reduce the signal-to-noise ratio. The CdTe/MgCdTe DH sample shows over 3 orders of magnitude larger PL intensity compared to the plain CdTe layer on InSb, which indicates that the MgCdTe barrier layers are effective at confining carriers within the CdTe middle layer. The CdTe/MgCdTe DH sample also has much larger PL intensity compared to the GaAs/AlGaAs DH. The GaAs sample was grown using typical growth temperatures and flux ratios, so it is assumed that it represents a sample of “average” quality. It is therefore expected that CdTe has a longer carrier lifetime and higher quantum efficiency compared to GaAs.

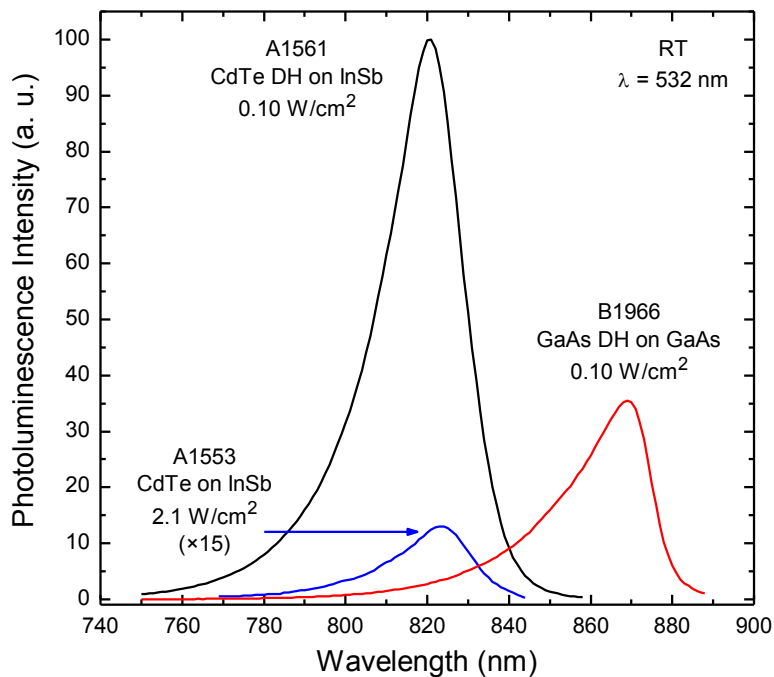


Figure 5.1. Photoluminescence spectra of various CdTe-based structures and a GaAs structure for comparison.

The effect of surface recombination and recombination in the buffer layer is further investigated using PL measurements, as shown in Fig. 5.2. The three samples consist of a CdTe DH on InSb (sample A1561), and single heterostructure samples grown

using the same growth conditions. The results show that removing the bottom barrier reduces the PL intensity by a factor of 5. It is likely that a significant number of carriers diffuse to the InSb buffer layer and recombine non-radiatively. Even more dramatic is the 3 order of magnitude reduction in PL intensity for the sample without the top barrier. It can therefore be concluded that surface recombination is the dominant mechanism when no top barriers are used. These results show the importance and effectiveness of MgCdTe barrier layers to confine carriers.

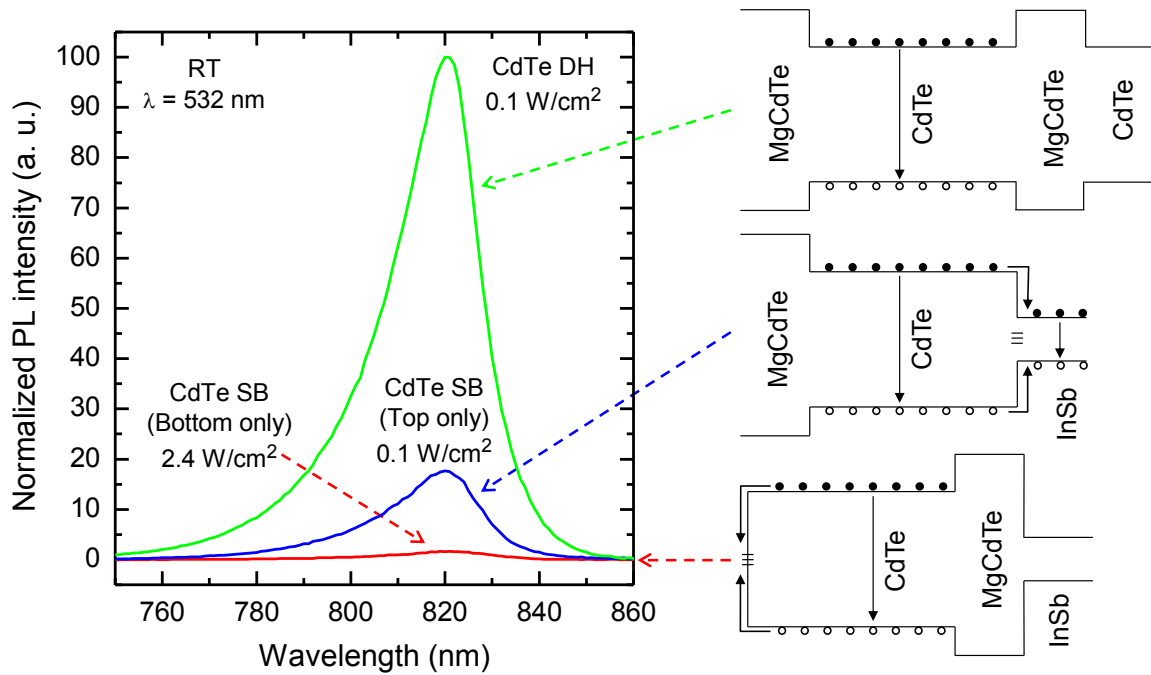


Figure 5.2. Comparison of photoluminescence spectra for the CdTe/MgCdTe double and single heterostructure samples, along with their schematic band edge diagrams showing the various recombination mechanisms.

5.2 Time-resolved photoluminescence of CdTe/MgCdTe DHs

The carrier lifetime of CdTe/MgCdTe DHs are measured using time-resolved photoluminescence (TRPL). As discussed in section 5.1, the PL intensity is directly proportional to the carrier concentration, as long as the low injection condition is

satisfied. Assuming that radiative and Auger recombination mechanisms are negligible, the carrier lifetime is the parallel combination of bulk SRH lifetime and interface recombination, as given by:

$$\frac{1}{\tau} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{interface}} = \frac{1}{\tau_{SRH}} + \frac{2S}{d} \quad (5.5)$$

where τ_{SRH} and $\tau_{interface}$ are the bulk SRH and total interface recombination lifetimes, respectively, S is the interface recombination velocity and d is the thickness of the middle layer in the DH [41]. It is assumed that the diffusion length is much longer than the thickness of the CdTe middle layer so that the carrier density is uniform throughout the layer. According to (5.5), the interface recombination velocity can be determined by measuring the lifetime of samples with different CdTe middle layer thicknesses. Such an experiment is discussed below.

Figure 5.3 shows a TRPL decay curve for the CdTe/MgCdTe DH grown at the optimal growth conditions (sample A1561). The region between 90 ns and 350 ns is fit to a single exponential decay model, and the lifetime obtained is 86 ns. At the time of publication this was the highest reported carrier lifetime for CdTe [15] and represents a breakthrough in the understanding of CdTe/MgCdTe structures. As mentioned in chapter 1, typical carrier lifetimes for polycrystalline material are only 6 ns [13]. The region between 0 ns and 90 ns does not fit well, most likely because the carrier concentration is close to the transition between low and high injection. The initial carrier concentration is estimated based on the pulse energy of the excitation laser and assuming that all of the light (less reflection loss) is absorbed in the middle CdTe layer. The carrier concentration at $t = 0$ ns is $5 \times 10^{14} \text{ cm}^{-3}$, while at $t = 90$ ns it is approximately $1 \times 10^{14} \text{ cm}^{-3}$. Therefore,

the injection condition can be considered “low injection” for carrier concentrations below $1 \times 10^{14} \text{ cm}^{-3}$. The low injection condition is also confirmed for the steady state PL measurements reported in chapter 5.1. A PL pump power density of 0.1 W/cm^2 at a wavelength of 532 nm and with a carrier lifetime of 86 ns gives an excess carrier concentration of around $1 \times 10^{14} \text{ cm}^{-3}$. The PL pump power density gives a photon flux that is comparable to the AM1.5G solar spectrum (within a factor of 2), which makes the PL measurements relevant for solar cell applications.

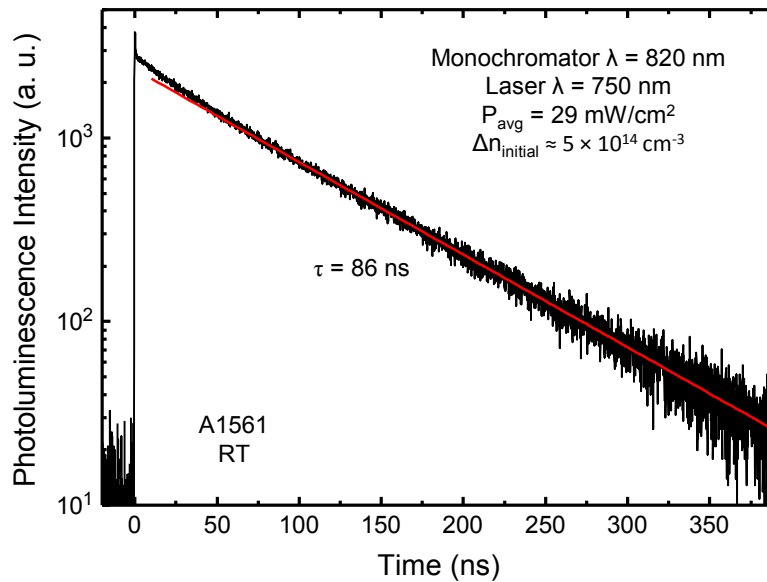


Figure 5.3. Room temperature time-resolved photoluminescence decay of the CdTe/MgCdTe double heterostructure grown on InSb. A carrier lifetime of 86 ns is extracted using a single exponential decay model.

The carrier lifetime is also measured as a function of position on the wafer, and for samples with different CdTe middle layer thicknesses. Table 5.1 lists the average carrier lifetime and the range. Samples are grown using the DH layer design discussed previously but with different CdTe middle layer thicknesses. Whole 2” InSb wafers are used, and samples are mounted without the use of indium. Note that the sample with

86 ns lifetime (A1561) is not included in the table. The non-uniformity of the carrier lifetime is attributed to the non-uniform temperature of the indium-free mounted InSb wafer. Longer lifetimes are observed closer to the edge of the wafer. A further explanation is given in Chapter 7.3. The carrier lifetime also increases with the middle layer thickness, which indicates that interface recombination at the CdTe/MgCdTe interfaces is non-zero. A relatively low interface recombination velocity of 461 cm/s and a long bulk SRH lifetime of 442 ns is determined using Equation (5.5). Interface recombination therefore dominates over bulk SRH recombination for samples grown using the optimal growth conditions, however the interface recombination velocity is still much lower than the free CdTe surface, which is on the order of 10^5 cm/s [42].

Table 5.1. Measured carrier lifetime as a function of CdTe middle layer thickness [16].

Sample	Thickness (μm)	Average carrier lifetime (ns)	Lifetime range (ns)
A1639	0.3	33	31 - 35
A1622	1	86	78 - 97
A1625	2	157	138 - 179

5.3 Optimization of growth conditions using photoluminescence

SSPL and TRPL are both used to determine the quality of DHs grown using different growth conditions. SSPL is the first measurement performed on samples simply because the equipment is readily available within our own lab. SSPL also gives spectral information, while the TRPL signal is integrated over a broad wavelength range. However, TRPL has an advantage in that it is less sensitive to alignment errors. This is because the TRPL decay curve is measured on an arbitrary scale, while the SSPL must be absolute relative to a reference sample. For example, if a PL collection lens is accidentally misaligned between measurements, the SSPL intensity will drop while the TRPL curve

will only shift downward on the y-axis. A lower SSPL intensity is measured, while no change in TRPL decay time is observed. The consequence is that samples measured using SSPL must be measured on the same day in order to ensure a proper comparison.

Figures 5.4 and 5.5 show the correlation between the PL peak intensity and the carrier lifetime as a function of growth temperature and flux ratio. The two measurements track closely to one another, which instills confidence in the measurements. A peak is observed at $T_s = 265$ °C and a Cd/Te flux ratio of 1.5. The curves show a sharp increase in intensity and lifetime as the temperature is raised from 235 °C to 265 °C. The longer carrier lifetime and PL intensity is likely caused by a reduction in the dislocation density, which may be facilitated by an increase in adatom migration. This explanation is supported by Fig. 4.2a which shows a noticeable improvement in the RMS roughness with increasing temperature. For growth temperatures beyond 265 °C, the roughness remains relatively constant while the SSPL intensity and SRH lifetime slightly drop. This is likely due to indium diffusion from the InSb wafer. SIMS measurements show that the indium diffusion from InSb into CdTe increases with temperature. Background concentrations range from mid 10^{14} cm⁻³ to low 10^{18} cm⁻³ for samples grown at 250 °C and 295 °C, respectively. More samples would need to be grown in order to explain the trend for the flux ratio.

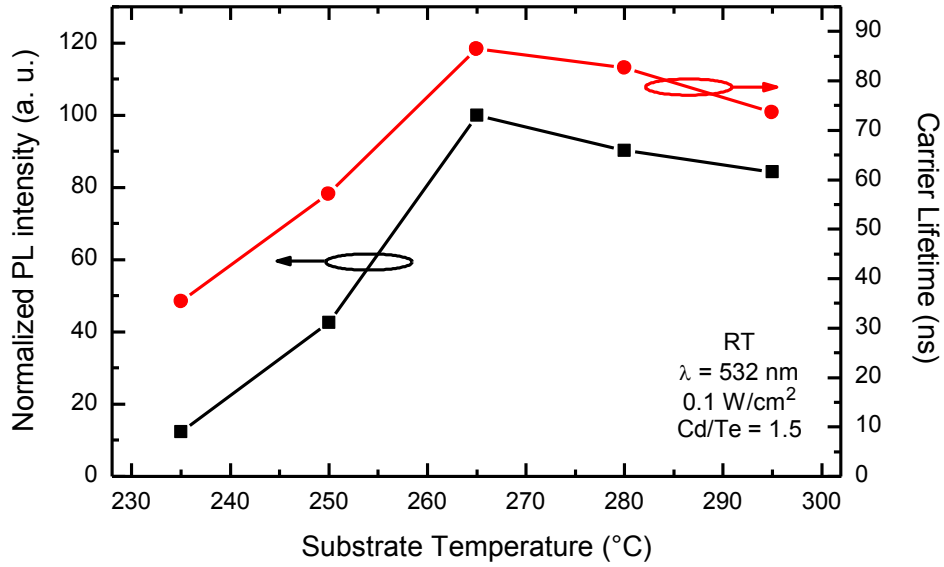


Figure 5.4. Comparison of PL intensity and carrier lifetime as a function of substrate growth temperature.

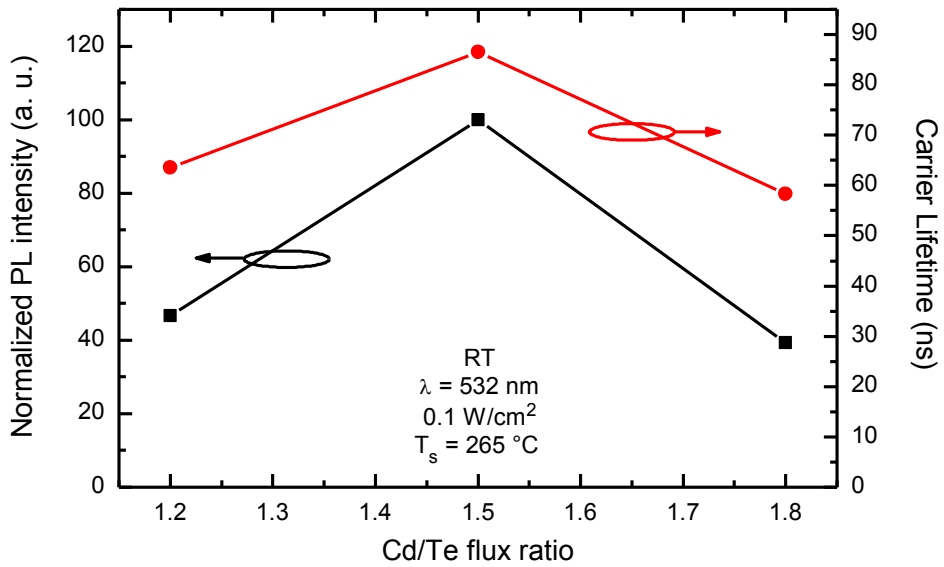


Figure 5.5. Comparison of PL intensity and carrier lifetime as a function of Cd/Te flux ratio.

CHAPTER 6

DESIGN OF ZnTe/CdTe/MgCdTe DOUBLE HETEROSTRUCTURE SOLAR CELLS

The demonstration and characterization of a working device is the next step following the investigation of the material quality. The fundamentals of PN homo- and hetero-junction solar cells are first presented in order to lay the groundwork for designing a more complex ZnTe/CdTe/MgCdTe double heterostructure solar cell. Numerical simulations are carried out using the software PC1D version 5.9 in order to predict the device performance and optimize the layer structure.

6.1 Solar cell operation and design principles

Solar cells can be described from many perspectives. From an electrical engineering perspective, it is simply a two terminal device which delivers electrical power to a connected load when the device absorbs light. The output power of the cell is determined by many factors, most importantly the absorbed photon flux and spectral properties, the efficiency of the cell, the operating temperature, and the load resistance. Solar cells are commonly described by their current density vs. voltage (J - V) characteristics, both in the dark and with the device under illumination. These characteristics are a function of material properties, device structure, temperature, and the wavelength and intensity of the illumination. Significant information about the material quality and device physics can be inferred from these characteristics, and so electrical/optical measurements are incredibly important for troubleshooting problems with the device performance.

6.1.1 Abrupt PN homojunction characteristics

From a semiconductor and quantum physics perspective, solar cells work by converting photons to charge carriers through the process of generation and then separating the carriers to generate a voltage. This process is always working against carrier recombination, which occurs in various places throughout the device (bulk, interface, and surface) and through different recombination mechanisms (SRH, radiative, and Auger). The goal of the device designer is to minimize recombination through appropriate structure design and the use of high-quality materials.

Charge separation is accomplished using the built-in electric field of a PN junction. When a junction is formed between a p- and n-type material, electrons on the n-type side near the junction diffuse to the p-type material, and holes diffuse from the p-type to n-type side. This charge transfer establishes an electric field at the junction. It is this electric field which is used to separate photogenerated carriers, and the separation is best understood under the short-circuit condition using a band edge vs. position diagram, as shown in Fig. 6.1. In this example, a photon is absorbed on the p-type side, and an electron-hole pair (EHP) is generated. Holes on the p-type side see a large potential barrier at the PN junction and therefore mostly remain on the p-type side. However, there are two possibilities for the electron. First, it can diffuse within the p-type region for a period of time and recombine with another hole. No current will be generated in that scenario. The other option is that it diffuses to the edge of the depletion region and is swept to the n-type region by the electric field. As soon as the electron reaches the n-type region, the PN junction is effectively a capacitor with one excess charge on each side. In order to maintain the short-circuit condition depicted in Fig. 6.1, an electron must quickly

move into the n-contact where it will neutralize a hole at the p-contact. By neutralizing the hole, the electron has completed a loop which represents current, and energy has been conserved through the emission of phonons for every step where the electron lost energy. Although diffusion was involved in this process, the photocurrent is analogous to the drift current in a PN junction because the minority carrier was acted upon by the electric field.

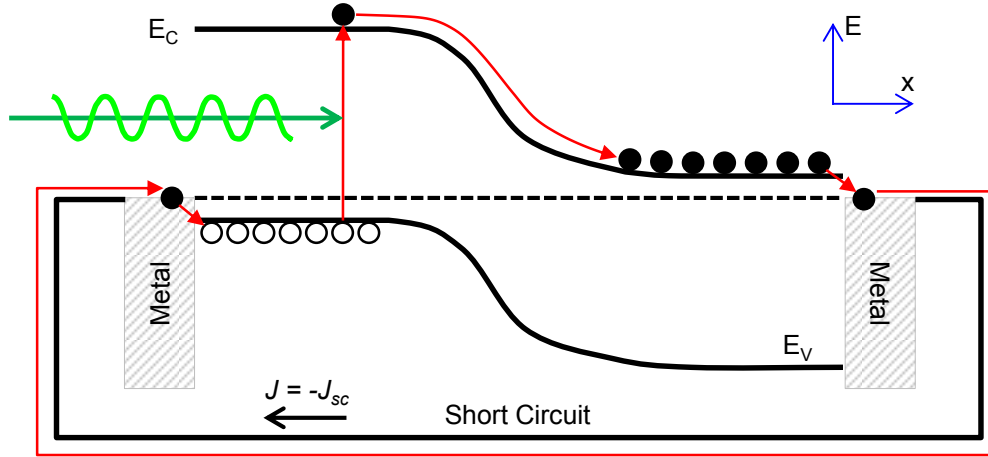


Figure 6.1. Schematic band edge diagram of a PN junction under short circuit conditions and with illumination. Quasi-Fermi levels are omitted for clarity.

It is common to measure solar cell quantum efficiencies under the short-circuit condition. The external quantum efficiency is defined as the ratio of the current density (expressed in charges/cm²/s) to the incident photon flux (expressed in photons/cm²/s). This property is affected by material quality, device structure, and optics structure (front reflectance, grid shadowing loss, and transmission loss). The EQE can be used to determine the internal quantum efficiency (IQE) by removing the front reflectance, grid loss, and transmission loss, as given by:

$$IQE(\lambda) = \frac{EQE(\lambda)}{(1 - R(\lambda))(1 - T(\lambda))(1 - \gamma_{grid})} \quad (6.1)$$

where $R(\lambda)$ is the spectral reflectance, $T(\lambda)$ is the spectral transmittance, γ_{grid} is the grid loss, and λ is the wavelength. The IQE of a solar cell is defined as the ratio of collected charge carriers to photons absorbed in the active layers of the device. It is important to note that the electric field at the junction is greatest under the short-circuit condition. Therefore it is possible to demonstrate near 100 % IQE for photons with certain energies as long as the diffusion length $L_{n,p}$ of minority carriers is much greater than the thickness of the absorbing layer. The IQE characteristics as a function of wavelength give important information about the device. Higher energy photons are absorbed closer to the surface compared to lower energy photons which are absorbed more uniformly. Therefore, one can obtain information about the rate of recombination as a function of depth from the surface. This is useful because solar cell structures typically contain interfaces at various depths, and interface recombination may be significant for certain interfaces.

An external voltage is developed at the contacts when the cell is illuminated and a load with non-zero resistance R_L is applied, as illustrated in Fig. 6.2. Again, using the photogenerated electron on the p-type side as an example, the electron is first swept to the n-type side by the built-in electric field. As more photons are absorbed, electrons build up on the n-type side because R_L does not allow them to neutralize holes on the p-type side without developing an external voltage V_a . A similar situation occurs for holes generated in the n-type material, which are swept to the p-type side and begin to build up. Since the PN junction is essentially a capacitor, the charge build-up causes the external voltage to increase. Working against the charge buildup is the external current J , and the

recombination current. The goal then is to minimize the recombination current so that the maximum voltage can be developed.

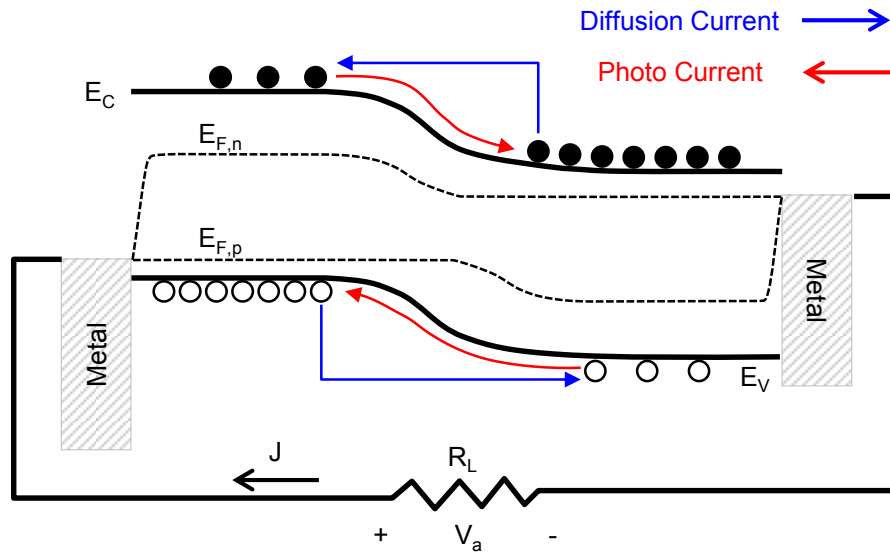


Figure 6.2. Schematic band edge diagram of a PN junction under illumination and with non-zero load resistance.

In the band edge diagram shown in Fig. 6.2, the recombination current which is illustrated is called diffusion current. This is just one of many recombination mechanisms that take place in a PN diode. Diffusion current also occurs in PN heterojunction devices operating with a moderate V_a . Continuing with the previous discussion, the additional charge build-up (in addition to developing an external voltage) also neutralizes some of the charged dopant atoms in the depletion region, therefore reducing the built-in electric field and the depletion region width. As a result, the band edges shift so that the potential barrier is reduced. At a certain V_a , the potential barrier at the PN junction will be sufficiently low and electrons with enough thermal energies can diffuse back to the p-type side and recombine with holes. This diffusion and recombination process is called diffusion current, which is a recombination loss for the cell.

In order to extract the maximum power from the solar cell, R_L is adjusted so that a relatively high voltage is developed while the recombination current is kept relatively small. The operating voltage and current at the maximum power output is labeled V_m and J_m , respectively. As R_L approaches infinity, the cell begins to operate under open-circuit conditions and a voltage V_{oc} is developed at the contacts. Under this condition, the recombination current has increased enough to completely counteract the photocurrent, and no power is delivered to the load.

A closer look at the current density vs. voltage (J - V) relationships can give valuable insight on how various parameters affect the solar cell efficiency. Assuming that the superposition principle holds, the photocurrent and recombination current can be considered to be uncoupled:

$$J(V) = J_D(V) - J_L, \quad (6.2)$$

where J is the output current to the load, J_D is the dark current, and J_L is the photocurrent. J_L appears as a negative term because it is a drift component and is therefore in the opposite direction of the forward bias diode current. Power is delivered to the load when the voltage is positive and the current is negative, as defined by Equation (6.2) and Fig. 6.2. The dark current is the total recombination current in the device. For the present example, J_D is given by:

$$J_D = J_o \left[\exp\left(\frac{qV_a}{nkT}\right) - 1 \right], \quad (6.3)$$

where J_o is the reverse saturation current, V_a is the applied or external voltage, n is the ideality factor, k is the Boltzmann constant, and T is temperature [43]. When n is an integer (1, 2, or 3/2), this equation describes just one recombination mechanism taking

place inside the device, which is characterized by J_o and n . Many recombination mechanisms typically take place simultaneously through different mechanisms (SRH, radiative, and Auger recombination) which can occur at the same location or different locations within the device. The J - V characteristics for a diode with multiple parallel recombination mechanisms can be represented by:

$$J_D = J_{o,1} \left[\exp\left(\frac{qV_a}{n_1 kT}\right) - 1 \right] + J_{o,2} \left[\exp\left(\frac{qV_a}{n_2 kT}\right) - 1 \right] + \dots + J_{o,k} \left[\exp\left(\frac{qV_a}{n_k kT}\right) - 1 \right], \quad (6.4)$$

where k is the total number of recombination mechanisms. For some devices, only one recombination mechanism dominates over a small voltage range, and the J_o term for that mechanism can be extracted from the J - V characteristics. It is often observed however that multiple recombination mechanisms take place within similar voltage ranges, and as a consequence the ideality factor n varies greatly with voltage. Parasitic resistances and high-injection effects further complicate the analysis of the J - V characteristics.

In the present example, the diffusion current is characterized by recombination in the quasi-neutral region, and this mechanism has an ideality factor of 1 [43]. The diffusion current is then characterized by J_o , which is given by:

$$\begin{aligned} J_o &= J_p + J_n = qn_i^2 \left(\sqrt{\frac{D_p}{\tau_p}} \frac{1}{N_D} \right) + qn_i^2 \left(\sqrt{\frac{D_n}{\tau_n}} \frac{1}{N_A} \right) \\ &= qn_i^2 \left(\sqrt{\frac{D_p}{\tau_p}} \frac{1}{N_D} + \sqrt{\frac{D_n}{\tau_n}} \frac{1}{N_A} \right), \end{aligned} \quad (6.5)$$

where J_p and J_n are the currents due to holes and electrons, respectively, n_i is the intrinsic carrier concentration, $D_{p,n}$ is the diffusion coefficient for holes and electrons, respectively, $\tau_{p,n}$ is the minority carrier lifetime for holes (electrons) in n-type (p-type)

material, respectively, N_A is the acceptor concentration and N_D is the donor concentration. One way to decrease J_o is to increase N_D and N_A . The increased doping concentration results in a larger built-in electric field, which can be described in terms of the built-in voltage:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right) . \quad (6.6)$$

Increasing the doping concentration will increase the potential barrier for diffusion current, and so J_o is reduced. However, the carrier lifetime decreases as a result of higher doping concentration, which has the opposite effect on J_o . Other factors such as series resistance and the practical doping limits of semiconductors further complicate the task of determining the optimal doping concentrations, and a combination of numerical simulations and experiments are therefore needed to arrive at the optimal value.

Typical solar cell designs employ an asymmetric dopant profile and layer structure. The structure usually consists of a thin heavily doped n-type layer, called the emitter, on top of a thick lightly doped p-type layer, called the base. There are several advantages to this design. First, it should be mentioned that a moderate total doping is needed to establish a large V_{bi} . It is also known that increased doping concentration decreases the carrier lifetime. Therefore, the semiconductor which absorbs most of the light should be lightly doped so that photogenerated minority carriers have longer lifetime and diffusion length. The heavily doped emitter is then made sufficiently thin in order to minimize absorption, since EHPs generated in that layer are likely to recombine due to the short lifetime. The asymmetric doping also affects the dark current. Considering only the diffusion current described by Equation (6.5), asymmetric doping

causes either the electron or hole currents to be negligible. For example, electron diffusion current dominates in an n^+p structure. Therefore a base material with long carrier lifetime is needed in order to reduce the dark current. Lastly, an N-on-P structure is typically chosen so that photogenerated minority carriers in the base are electrons, which generally have a longer diffusion length compared to holes because of the higher electron mobility.

Although it is desirable to achieve the largest V_{bi} , there are practical limits to the doping. The maximum doping in the emitter is limited by several factors such as dopant solubility, compensation, reduced carrier lifetime, and band gap narrowing. On the other hand, the minimum doping concentration in the base is limited by the background impurities in the system and the contribution to the series resistance. The range of doping concentrations and layer thicknesses are discussed in the following sections.

6.1.2 Abrupt PN heterojunction with asymmetric doping

Heterostructures are useful in solar cell designs because of their ability to form barriers for minority carriers, and the PN heterojunction has advantages over the PN homojunction. Commercially available polycrystalline CdTe solar cells currently utilize an n-type CdS emitter and a p-type CdTe base [2]. The advantages, disadvantages, and design considerations are discussed below.

First, PN heterojunction designs are useful when both n- and p-type doping of the absorber material cannot be achieved with high carrier concentration. This is the case for p-type CdTe, which is difficult to achieve using the available dopants in the growth chamber at ASU. Another advantage is that the device can be designed with a wide band gap emitter. This allows for more light transmission into the base layer. As discussed

previously, it is advantageous to have more light absorbed in the base because of the longer lifetime in that layer. Having a semi-transparent emitter means that fewer EHPs are lost due to non-radiative recombination in the emitter. Lastly, wider band gap materials generally have a smaller refractive index, which results in lower surface reflectance.

The band discontinuities that exist at the PN heterojunction offer a significant design challenge. Figure 6.3a shows the band diagram of a symmetrically doped n-GaAs/p-Al_{0.3}Ga_{0.7}As heterojunction at the maximum power operating point. The doping concentration is $1 \times 10^{17} \text{ cm}^{-3}$ for both the emitter and base. Type-I heterojunctions (such as this one) produce a spike in one of the bands, which impedes the collection of photogenerated carriers. For this example, the $\sim 300 \text{ meV}$ potential spike blocks minority carrier electrons from being swept from the p-type side to the n-type side. It is also undesirable to trap carriers near the interface because of the non-zero interface recombination velocity. Figure 6.3b shows an n⁺p heterojunction with emitter doping of $1 \times 10^{18} \text{ cm}^{-3}$ and a base doping of $1 \times 10^{16} \text{ cm}^{-3}$. With heavier doping, the width of the potential spike is reduced and tunneling is increased. Furthermore, the depletion region extends further into the base which helps with charge separation.

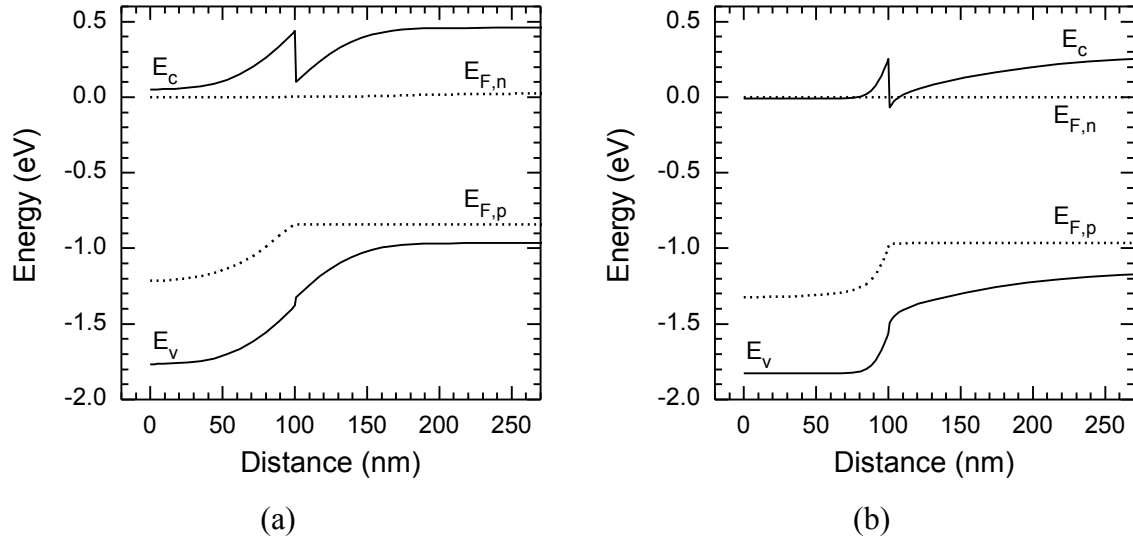


Figure 6.3. Simulated band edge diagrams of symmetric (a, left) and asymmetric (b, right) PN heterojunction at the maximum power operating point.

Simulations are performed on these two structures using PC1D. It is assumed that a large interface recombination velocity of 1×10^5 cm/s exists at the interface of GaAs and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$. The simulated efficiency of the symmetrically doped structure is 23.0 % while the asymmetric structure gives 27.1 %. Note that the built-in potential for these two structures are the same. The reduction in efficiency is due to the increased interface recombination, which causes a reduction in V_m of 122 mV. Without interface recombination in the model, the efficiencies are approximately the same, giving 28.5 % and 27.5 %, respectively. (The symmetrically doped structure shows even higher efficiency than the asymmetric structure because lower doping causes the net lifetime to increase in the PC1D simulator).

Choosing a material with a smaller conduction band offset will reduce the potential spike, but at the same time the built-in potential is also reduced (assuming the band gaps stay the same), as shown by:

$$qV_{bi} = \frac{\Delta E_c - \Delta E_v}{2} + kT \ln \left(\frac{N_d N_a}{n_{i,n} n_{i,p}} \right), \quad (6.7)$$

where ΔE_c and ΔE_v are the conduction and valance band offsets, respectively, $n_{i,n}$ and $n_{i,p}$ are the intrinsic carrier concentrations on the n- and p- side, respectively, and the effective density of states are assumed to be equal for both layers. Both band offsets are defined to be positive for a type-I alignment where the wide band gap material is n-type. The low V_{bi} is problematic when interface recombination is significant, as weak band bending under forward voltage allows carriers to reach the interface. It has been shown that a relatively small (100 meV) potential spike is advantageous for structures with high interface recombination velocity [44].

6.2 Design of the ZnTe/CdTe/MgCdTe layer structure

The design of the solar cell layer structure involves a simultaneous optimization of many aspects related to the junction properties, optical properties, electrical properties, and practicality of the growth and fabrication. The most practical way of designing the structure involves taking an “initial guess” based on a fundamental understanding of the device, then testing how various parameters affect the efficiency using numerical simulations. After optimization of the model, the actual device is created and tested. Results are analyzed to see where the faults are, additional numerical modeling may be performed, and another device is created. This process continues in a loop, as shown in Fig. 6.4 until the device performance has reached the project goals. A total of four solar cell samples are presented here which involves two initial guesses and one refinement in the structure. Since this work is part of an ongoing project within the ASU MBE

Optoelectronics Group, the goal for this dissertation is to demonstrate the first solar cell device and discover what the major problems are.

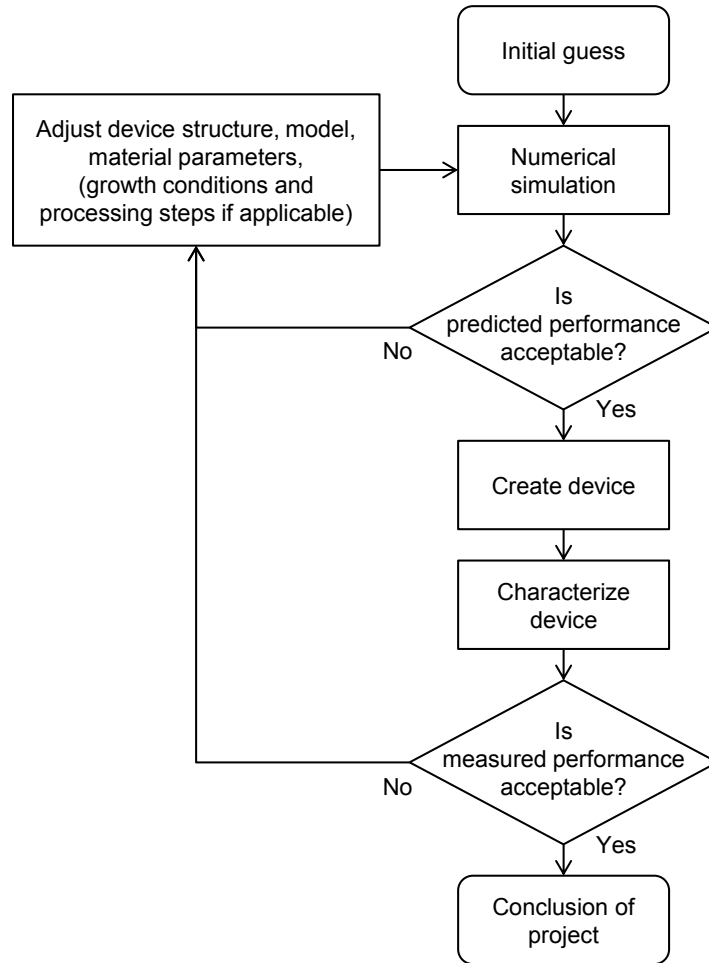


Figure 6.4. Flow chart illustrating the methodology to study and improve the performance of monocrystalline CdTe solar cells.

6.2.1 Initial structure design

In order to make the initial guess, several factors must be examined and some preliminary calculations must be made. First is to define the emitter material and doping type for both the emitter and base. n-type doping of CdTe is easily achieved at ASU using indium [39, 40], whereas p-type doping cannot be easily achieved. The problem for p-type doping is that only phosphorus is available in the II-VI chamber, and it was

discovered through SIMS measurements that the sticking coefficient of P on CdTe surfaces is too small to achieve reasonable doping concentrations. The CdTe base layer must be grown with high material quality using the dual chamber MBE system at ASU, however the emitter layer can be grown by other means. Therefore the base doping must be n-type, and the emitter doping must be p-type. Although the p-on-n structure is not ideal from a mobility standpoint, it will be sufficient for the first demonstration until appropriate dopant cells can be installed on the MBE system. Also, the choice of an n-type CdTe base is acceptable considering that there is significant indium diffusion from the substrate. SIMS measurements show an indium background concentration of around 10^{15} cm^{-3} for CdTe layers grown at $250 \text{ }^\circ\text{C}$. Lastly, only n-type InSb wafers are currently available. The back side of the wafer is typically used as a large-area contact, and so it is straight forward to design a low resistance n-CdTe/n-InSb isotype heterojunction for majority carrier transport which serves as the n-contact for the solar cell.

The emitter material must be able to achieve p-type conductivity while also having a relatively small valance band offset with CdTe in order to avoid the potential spike shown in Fig. 6.3. ZnTe:N is a decent choice considering that hole densities up to $1 \times 10^{20} \text{ cm}^{-3}$ have been demonstrated [45], and it is currently being explored as a back surface field (BSF) and contact layer for polycrystalline n-CdS/p-CdTe solar cells [46, 44]. The valance band offset ΔE_v between ZnTe and CdTe has been reported many times and values range from 0 meV to 180 meV with a type-II alignment [46, 47, 48, 49, 50, 51, 52]. A common practice is to take the average of all the reported values, and so for the purposes of simulation in this study $\Delta E_v \approx 80 \text{ meV}$. It has been previously found through simulations that type-II junctions are not ideal when interface recombination is

significant, and V_{oc} is reduced [44]. The interface recombination velocity at the CdTe/ZnTe interface has been reported to be 4.8×10^5 cm/s [53]. Such a large interface recombination velocity should be expected, considering that ZnTe and CdTe have a lattice mismatch of 6.2 %, and ZnTe films grown on CdTe become fully relaxed after a thickness of 30 nm [46].

Despite these limitations, ZnTe/CdTe PN heterojunction solar cells have been previously demonstrated. An efficiency of 1.3 % has been demonstrated for a device structure deposited on a glass substrate using close space sublimation as the growth technique [54]. MBE has also been used to grow ZnTe/CdTe junctions on GaAs substrates [55], however the device performance is poor and the efficiency is not reported. Lastly, ZnTe/CdTe/CdS and ZnTe/CdTe/GaAs PIN solar cells have been demonstrated using metalorganic vapor phase epitaxy (MOVPE), with the former structure giving up to 13 % efficiency [56]. All of these devices however show poor performance with either V_{oc} , J_{sc} , the fill factor, or a combination of these metrics. Another commonality between these studies is the use of lattice-mismatched substrates for the CdTe absorber, and so a low carrier lifetime is expected for the CdTe base layer. The 13 % efficiency measured for polycrystalline ZnTe/CdTe/GaAs solar cells [56] shows promise for monocrystalline CdTe solar cells on lattice-matched InSb to reach even higher efficiencies.

The overall layer structure shown in Fig. 6.5 is constructed based on material, doping, and processing constraints. First, the device area is defined by etching the II-VI layers to form square mesas. Contacts are made to the emitter layer and the bottom of the substrate. Placing both contacts on the top surface was not feasible because the CdTe

etching recipe is not well developed and the photomasks are not currently available within our group. As a result, the series resistance caused by the potential barrier at the CdTe/InSb isotype heterojunction is of some concern. In addition to the p-ZnTe emitter and n-CdTe base, an n-type MgCdTe BSF layer is used to confine holes to the base layer. The thickness and composition is chosen to be the same as the undoped CdTe/MgCdTe DHs (24 % Mg and 30 nm thick). The doping concentrations of the InSb buffer, CdTe buffer, and MgCdTe BSF layers are chosen to be $5 \times 10^{18} \text{ cm}^{-3}$ in order to reduce the thickness of potential spikes and lower the series resistance.

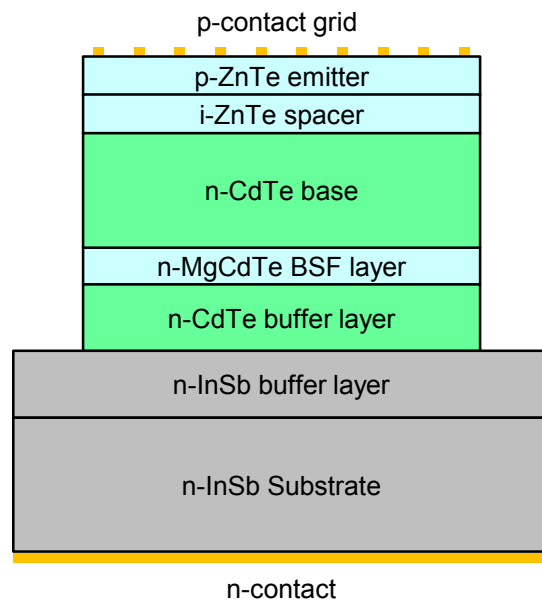


Figure 6.5. Layer structure of a ZnTe/CdTe/MgCdTe double heterostructure mesa-defined solar cell.

The next step is to determine the base layer thicknesses. It is desirable for the base layer to be optically thick in order to minimize transmission loss. The figure of merit is the absorptance, which is the ratio of the absorbed photon flux to the total solar photon flux for energies above the band gap. The absorptance is given by:

$$A_\alpha = \frac{\int_{E_g}^{\infty} [1 - \exp(-\alpha(E) \cdot t)] \cdot \Phi(E) dE}{\int_{E_g}^{\infty} \Phi(E) dE} \quad (6.6)$$

where E is the photon energy, E_g is the band gap of CdTe, t is the thickness of the CdTe layer, $\alpha(E)$ is the absorption coefficient of CdTe as a function of photon energy, and $\Phi(E)$ is the solar photon flux spectrum defined by the AM1.5G standard. A plot of absorptance vs. CdTe thickness is given in Fig. 6.6. At a thickness of 1 μm , the absorptance is 97.5 %, which is considered to sufficiently thick for this initial study. This thickness is also a good choice because the previous study of undoped DHs showed that the 1 μm thick CdTe layer is coherently strained, while thicker films may show undesirable relaxation.

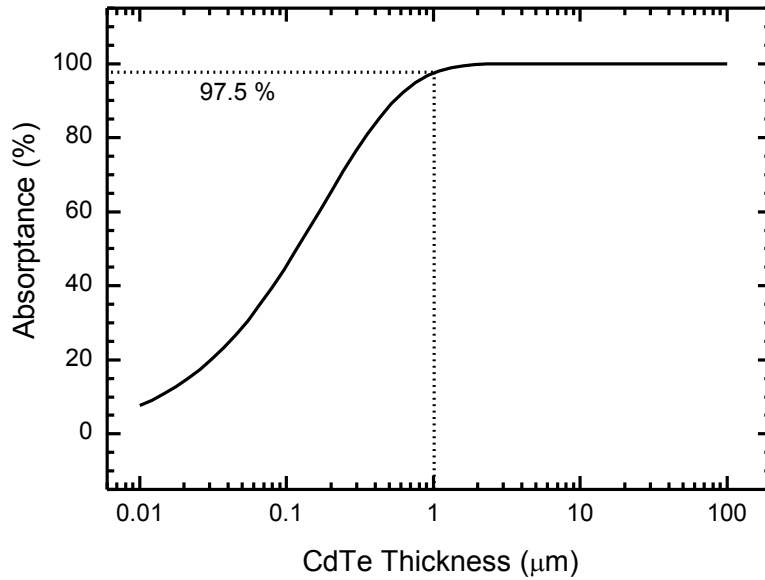


Figure 6.6. Absorptance as a function of CdTe layer thickness for the AM1.5G spectrum.

The base and emitter doping concentration is chosen based on the discussion in section 6.1.2, as well as series resistance considerations. A base doping of $1 \times 10^{16} \text{ cm}^{-3}$ is appropriate considering that it is roughly one order of magnitude larger than the

background In concentration, and so the carrier concentration can be well controlled. The lower limit of the emitter doping is determined by the need to make ohmic contacts to that layer. For ZnTe, any concentration of $1 \times 10^{18} \text{ cm}^{-3}$ or larger is good enough to make low-resistance ohmic contacts after annealing [57]. Series resistance in the emitter layer is also a concern. During operation, current travels vertically through the base and laterally through the emitter to the grid contacts. The fractional power loss for emitter current spreading is given by:

$$P_{\%,em} = \frac{1}{12} \frac{J_m}{V_m} S^2 \rho_{s,em} \quad (6.7)$$

where J_m and V_m are the current density and voltage at the maximum power operation point, S is the finger spacing and $\rho_{s,em}$ is the sheet resistance of the ZnTe layer [58]. Figure 6.7 shows the fractional power loss as a function of thickness for several different doping concentrations. For $N_A = 5 \times 10^{18} \text{ cm}^{-3}$, a thickness of 60 nm gives roughly 0.3 % power loss, and there is a large tolerance for error in the thickness. It is important to have tolerance for error because surface and interface Fermi level pinning can cause depletion which reduces the effective layer thickness. Furthermore, the growth rate and doping concentration can vary between growths.

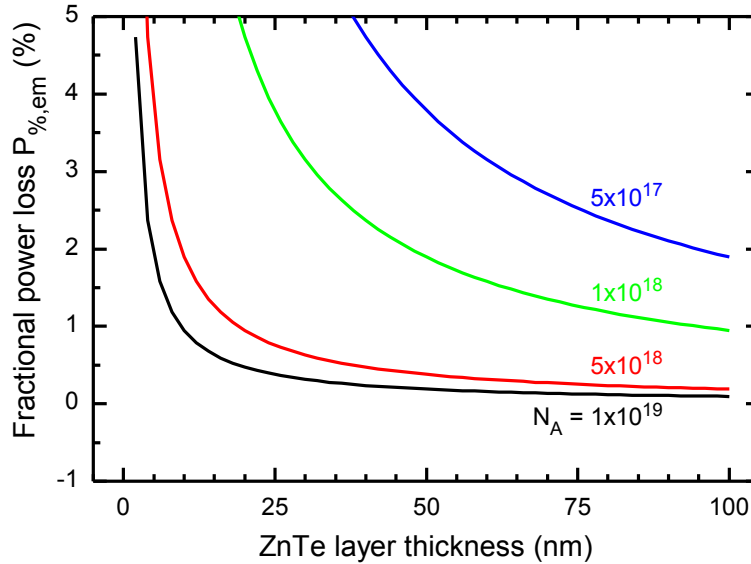


Figure 6.7. Fractional power loss due to emitter current spreading resistance as a function of ZnTe thickness and emitter doping concentration. A mobility of $50 \text{ cm}^2 \text{ v}^{-1} \text{ s}^{-1}$ and a finger spacing of $200 \mu\text{m}$ are assumed.

Lastly, an undoped spacer layer is placed between the p-ZnTe emitter and n-CdTe base. As mentioned previously, the sample needs to be transported in atmosphere to another growth chamber for the deposition of the p-ZnTe emitter. During that transfer, oxygen and carbon from the atmosphere will condense on the surface, causing oxidation and contamination. An arsenic cap is used to protect the II-VI layer, however this process cannot preserve the surface perfectly. Whichever interface is exposed to air will likely have many deep-level trap states caused by impurities. It is more desirable to have the impurities within in the semi-transparent ZnTe emitter instead of at the ZnTe/CdTe interface where minority carriers will recombine. Therefore, including a spacer layer should improve the efficiency by lowering recombination loss. The thickness of the spacer layer is initially set to 15 nm, which should be sufficiently thick to prevent

tunneling of electrons from CdTe into the defective i-ZnTe/p-ZnTe interface where they would recombine.

6.2.2 Numerical simulation and junction analysis

A more detailed analysis is performed on the initial structure design to verify its performance and look for potential problems. The ideal structure is one that gives high performance with a low sensitivity to varying layer thicknesses and doping. Figure 6.8 shows the layer structure used in the numerical simulation. This is chosen to be the default layer structure for which parameters will vary around. The SRH lifetime of the CdTe layer is set to 97 ns, while the other layers are assumed to be 1 ns. Furthermore, interface recombination at the CdTe/ZnTe interface is treated as a variable, with zero recombination being the default. No interface recombination at the CdTe/MgCdTe interface is included in the model. By using the measured 97 ns lifetime as the bulk CdTe lifetime in the model, two CdTe/MgCdTe interfaces are taken into account. Therefore the effective lifetime of a 1 μm thick CdTe layer with only one CdTe/MgCdTe interface will be higher than 97 ns, and so this value represents an underestimate of the effective lifetime. A full list of simulation parameters is given in Appendix B. The simulator program solves the Poisson and continuity equations simultaneously, therefore drift and diffusion is accounted for. Tunneling and thermionic emission currents are not modeled, and so the transport properties across isotype heterojunctions are not accurately represented. As a consequence, the CdTe/InSb junction is omitted from the model.

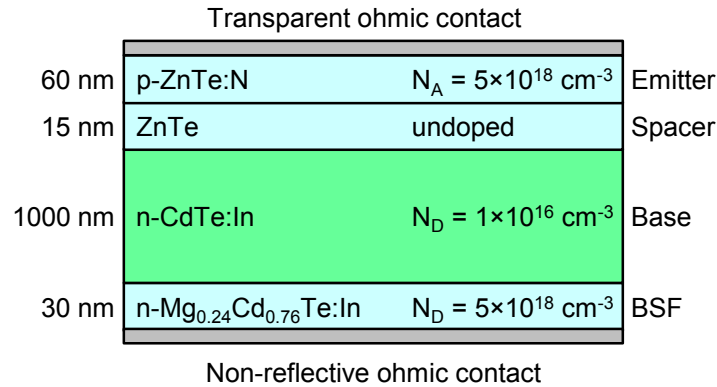


Figure 6.8. Layer structure diagram used as the default structure for the numerical device simulation.

The equilibrium band diagram for the default structure is shown in Fig. 6.9. Because the p-type emitter is more heavily doped, almost all of the band bending occurs in the CdTe base. A built-in potential of 1.29 eV is observed, which occurs mostly in the CdTe base (1.13 eV). Under forward bias and in the dark, the conduction band in the CdTe layer will shift upward, reducing the potential barrier. Holes are injected from the p-ZnTe layer into the n-CdTe layer where they recombine. However, note that electrons cannot be injected into the ZnTe layer because of the very large conduction band offset. As a result, all of the recombination associated with diffusion current takes place in the CdTe base. To reduce the diffusion current, the carrier lifetime in the CdTe layer must be increased so that the recombination rate is reduced, or the potential barrier for holes at the ZnTe/CdTe heterojunction must be made larger.

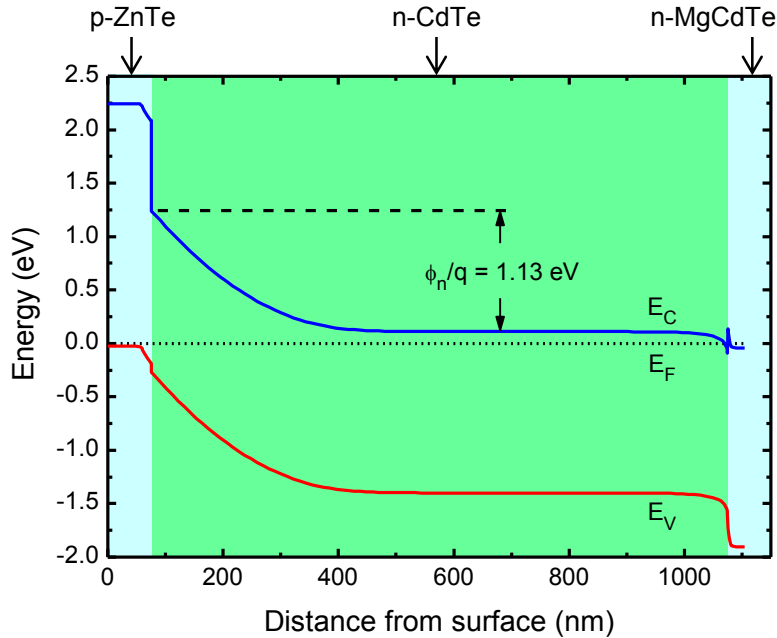


Figure 6.9. Equilibrium band edge diagram of the default structure in Fig. 6.8.

Under photo excitation, photons with energy below 2.26 eV are absorbed in the CdTe layer, while photons above that energy are absorbed in both ZnTe and CdTe layers. EHPs generated in the CdTe layer will be separated by the built-in electric field so that holes travel to the p-ZnTe layer and electrons stay within the n-CdTe layer. A photocurrent and voltage is developed at the contacts as a result.

One major concern for this structure is recombination at the ZnTe/CdTe interface, which is an additional recombination mechanism that increases the dark current. The impact is modeled by varying the emitter doping concentration in order to modulate the built-in potential. Figure 6.10 shows the band edge diagram for two structures with different emitter doping concentrations under one sun concentration and at the maximum power operating point. With low emitter doping, the potential barrier in CdTe at the

interface is reduced and minority carriers experience a smaller electric field. More interface recombination is expected for the sample with the lightly doped emitter.

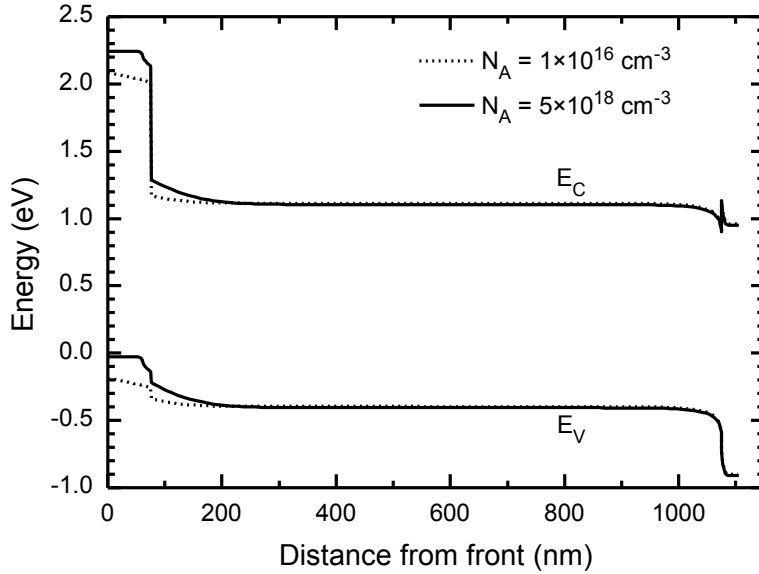


Figure 6.10. Band edge diagrams of two devices with different emitter doping concentration under 1-sun concentration and at the maximum power operating point.

The effect of emitter doping and interface recombination on the efficiency is shown in Fig. 6.11. First consider the case where the interface recombination velocity S is only 10 cm/s. The efficiency is relatively constant until the emitter doping reaches $1 \times 10^{19} \text{ cm}^{-3}$. This is expected, since the dark current will be dominated by recombination in the CdTe layer. The efficiency drop at very high doping concentration is due to a reduction in J_{sc} caused by the low carrier lifetime in ZnTe. The lifetime is low enough that the diffusion length has become shorter than the ZnTe layer thickness. Since the ZnTe layer is not completely transparent to the solar spectrum, many photons above the band gap of ZnTe are lost due to recombination. This conclusion is confirmed by setting the ZnTe layer to be transparent, which causes the efficiency to be independent of N_A . For moderate to high interface recombination velocity, the efficiency is a strong function of

N_A . The efficiency decreases as N_A is reduced because of a reduction in V_{oc} , which is caused by increased dark current. The effect of interface recombination is more dramatic when N_A is low because of the lower built-in electric field at the interface.

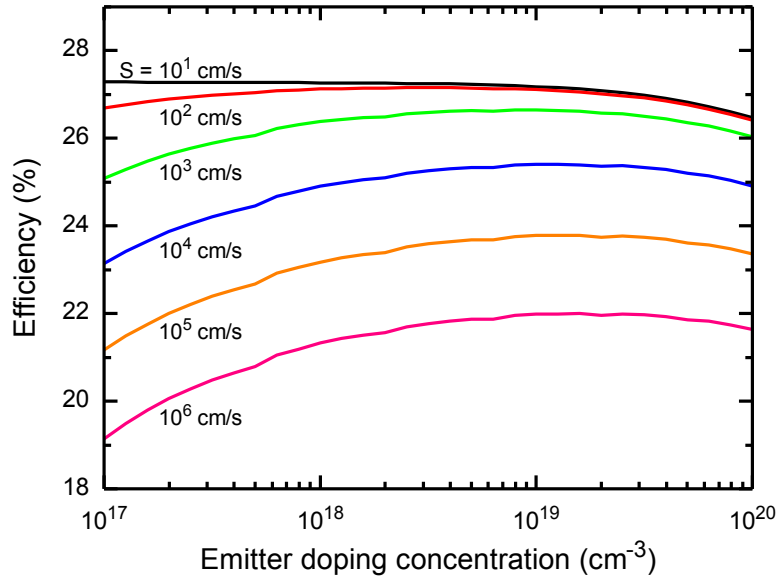


Figure 6.11. Solar cell efficiency as a function of emitter doping concentration and interface recombination velocity at the ZnTe/CdTe interface.

It is expected that the net carrier lifetime in the CdTe base layer will also have a significant impact on the efficiency. The asymmetric doping and large electron barrier at the ZnTe/CdTe interface means that most of the diffusion current is due to hole injection and recombination in the CdTe layer. Therefore, a shorter recombination lifetime in CdTe means faster diffusion and a larger dark current. This is also confirmed by Eq. (6.5) which shows that J_o increases with decreasing τ . For a very short carrier lifetime, photogenerated carriers at the bottom of the absorber will not be able to reach the junction, and J_{sc} will also be reduced. A plot of the efficiency vs. carrier lifetime is shown in Fig. 6.12. An efficiency of 27.2 % is calculated using a carrier lifetime of 97 ns and no interface recombination at the ZnTe/CdTe interface. The simulation also shows a J_{sc} of

28.6 mA/cm² and a V_{oc} of 1.096 V. These metrics become the target for the samples discussed in the next chapter. Interface recombination at the ZnTe/CdTe interface also has a significant impact on the efficiency. When the effective lifetime of the CdTe layer and CdTe/MgCdTe interface is sufficiently high, the efficiency is mainly limited by recombination at the ZnTe/CdTe interface.

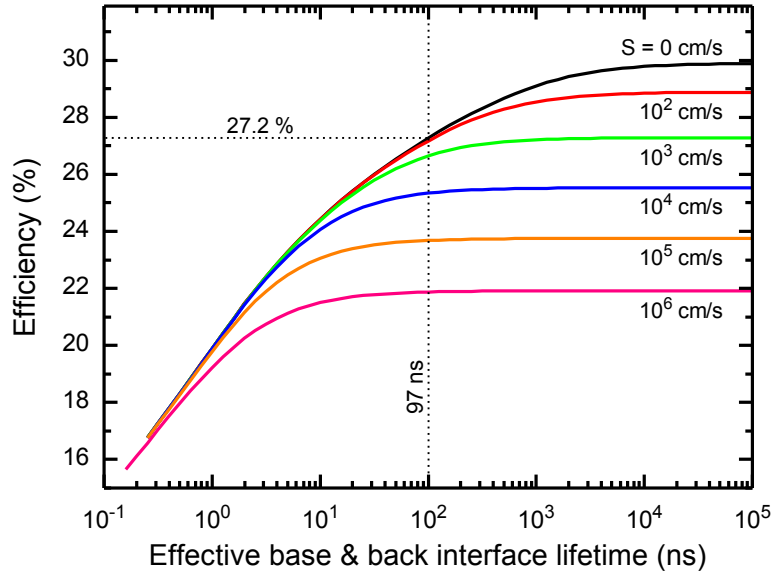


Figure 6.12. Solar cell efficiency as a function of emitter doping concentration and interface recombination velocity at the ZnTe/CdTe interface.

Lastly, it is important to understand the effect of the valance band offset ΔE_v on the efficiency, since that will affect V_{bi} and therefore interface recombination. Figure 6.13 shows the efficiency as a function of interface recombination velocity and ΔE_v . Type-I heterojunctions are preferred in order to increase the V_{oc} and increase band bending at the ZnTe/CdTe interface. An efficiency of 22.4 % can be achieved, assuming $\Delta E_v = 80$ meV and the interface recombination velocity is 4.8×10^5 cm/s, as the previous reports suggest. This efficiency is still greater than the 21.0 % record for CdTe [11]. Furthermore, there is

a chance to improve the interface recombination by optimizing the growth condition, which can be future work at the ASU MBE Optoelectronics Group.

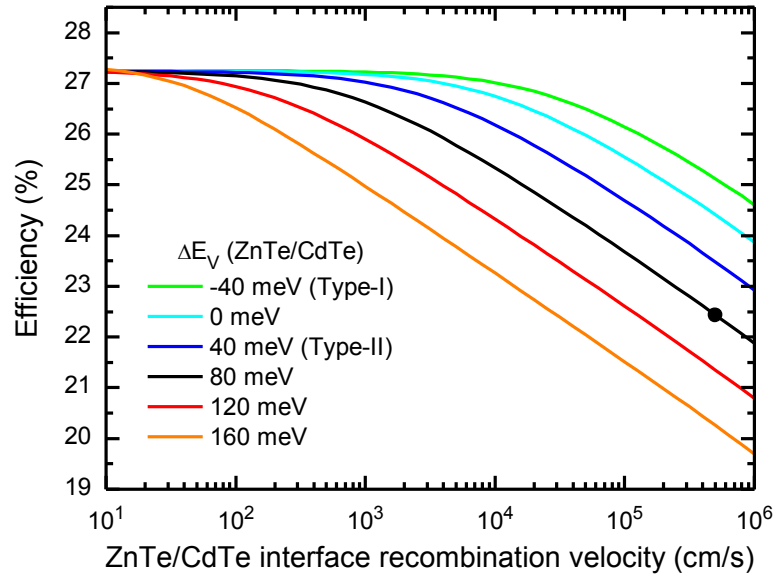


Figure 6.13. Solar cell efficiency as a function of ZnTe/CdTe interface recombination velocity for several band offsets. The black dot represents the efficiency based on the reported values of interface recombination velocity and band offset at the ZnTe/CdTe interface.

CHAPTER 7

GROWTH, PROCESSING, AND DEVICE CHARACTERIZATION OF

ZnTe/CdTe/MgCdTe DH SOLAR CELLS

Following a discussion of the theory and sample design, the next step is to grow, fabricate, and test the solar cell devices. This chapter therefore focuses on the experimental work of demonstrating ZnTe/CdTe/MgCdTe DH solar cells.

7.1 MBE growth of ZnTe/CdTe/MgCdTe DH solar cells

The solar cell structures are grown using a dual-chamber MBE system in the same manner as the undoped CdTe/MgCdTe DHs discussed previously. The growth rate and Mg cell temperature are the same as for the undoped DH, and the optimal growth substrate temperature and Cd/Te flux ratio is used. The two main differences are the use of doping and the growth of a ZnTe emitter at the University of Notre Dame. The indium doping concentration for n-CdTe and n-MgCdTe is calibrated using SIMS. The ZnTe:N doping concentration is calibrated using Hall measurements of a 500 nm thick ZnTe:N layer grown on a semi-insulating GaAs substrate. ZnTe is grown at a growth rate of 2.9 Å/s, a Zn/Te flux ratio of 1, and a substrate temperature of 320 °C as measured by the substrate holder thermocouple. Atomic N is provided by an RF plasma operating at 450 W and the beam flux is roughly $3\text{-}4 \times 10^{-6}$ Torr. These growth conditions have been shown to produce p-type ZnTe films with high conductivity and a mobility of $50\text{ - }60\text{ cm}^2\text{v}^{-1}\text{s}^{-1}$, as determined by Hall measurements.

Figure 7.1 shows a SIMS depth profile of the solar cell structure with a calibrated In trace. The target doping concentration of $1 \times 10^{16}\text{ cm}^{-3}$ is successfully achieved for the top 750 nm, and the buffer layer target doping concentration of $5 \times 10^{18}\text{ cm}^{-3}$ is achieved

as well. However there appears to be significant diffusion of indium from the MgCdTe layer into the CdTe base. Simulations show that the diffusion has negligible effect on the solar cell performance.

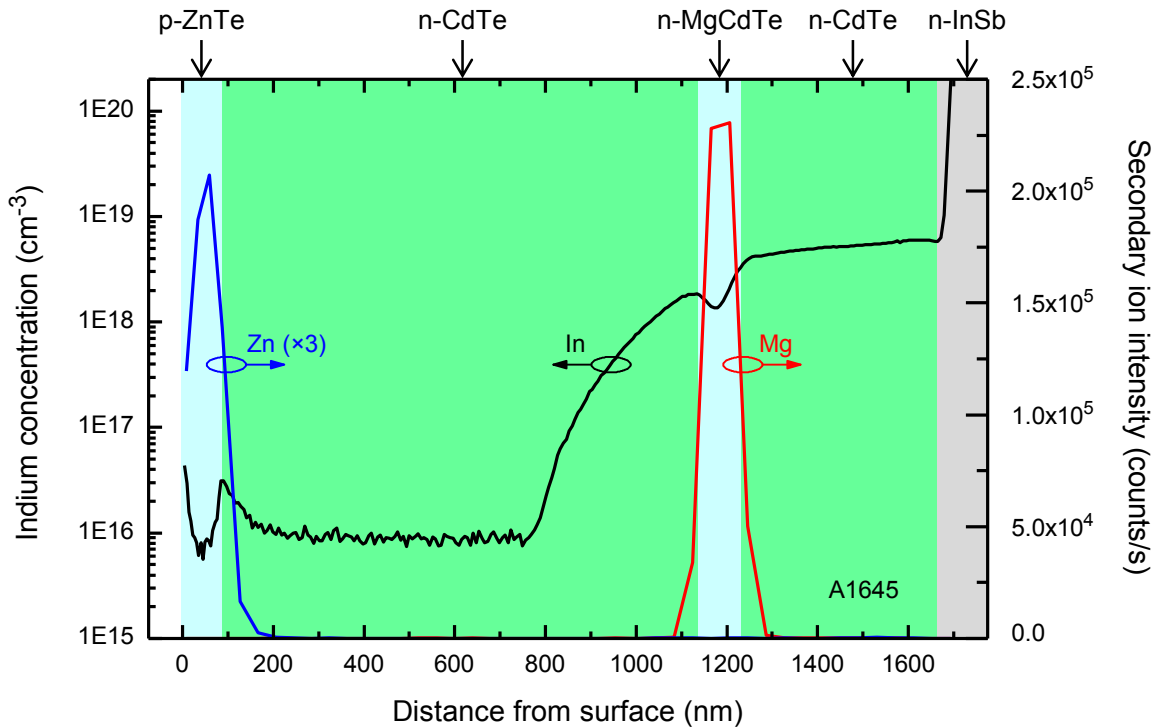


Figure 7.1. SIMS depth profile of the completed solar cell structure with a calibrated In trace.

The use of an As cap layer to protect surfaces from oxidation is known in the MBE community but its effectiveness is not reported frequently, especially for II-VI surfaces. Arsenic is an ideal protective layer because it can be thermally desorbed at temperatures around 300 °C [59]. Furthermore, it has been shown that an As cap can protect the AlGaAs surface for several months in atmosphere [60]. It is not well understood how As reacts with the CdTe surface, however. During the desorption process, the As oxides, contaminants, and bulk As layers are first removed until there is only a single atomic layer of As left on the surface. In this situation, the As-Cd and As-Te

bond strength is important, since that will determine whether the As atoms incorporate, float on the surface as a surfactant, or desorb completely. Little is known about this process for CdTe. From a CdTe standpoint, the CdTe desorption rate is only 1 ML/min at 300 °C [24], so surface damage from thermal desorption of CdTe is not expected to be significant.

To test the effect of an As cap and the possibility to re-grow II-VI layers, an experiment is set up using an undoped CdTe/MgCdTe DH. The idea is to introduce a growth interruption within the CdTe buffer layer and see how that affects the PL of the DH grown on top of it. The normal growth procedure is used to grow the 500 nm thick CdTe buffer layer. Then the sample is transferred back to the III-V chamber and a 100 nm thick As cap is deposited on the CdTe surface at roughly 30 °C. The sample is then exposed to atmosphere for 1 week and reloaded into the II-VI chamber. Thermal desorption of the As cap is performed at around 300 °C and the RHEED pattern recovers from hazy to streaky within 1-2 min. Another 500 nm thick CdTe buffer layer and the DH with 1 μm thick middle layer is grown using the standard procedure.

The PL spectrum of the sample with interrupted buffer layer growth is shown in Fig. 7.2 along with the CdTe/MgCdTe DH and GaAs/AlGaAs reference samples. The sample with growth interruption shows a slight improvement in PL intensity. This demonstrates that a growth interruption does not significantly degrade the crystalline and optical quality of the DH grown above it. The apparent improvement in PL intensity is likely due to degradation of the CdTe reference sample A1561 over the 11 month period between the two growths, since the PL intensity of A1561 was originally twice that of the GaAs sample. The conclusion is that As capping provides sufficient protection for the

CdTe surface which enables the atmospheric transfer and growth of p-type ZnTe at the University of Notre Dame.

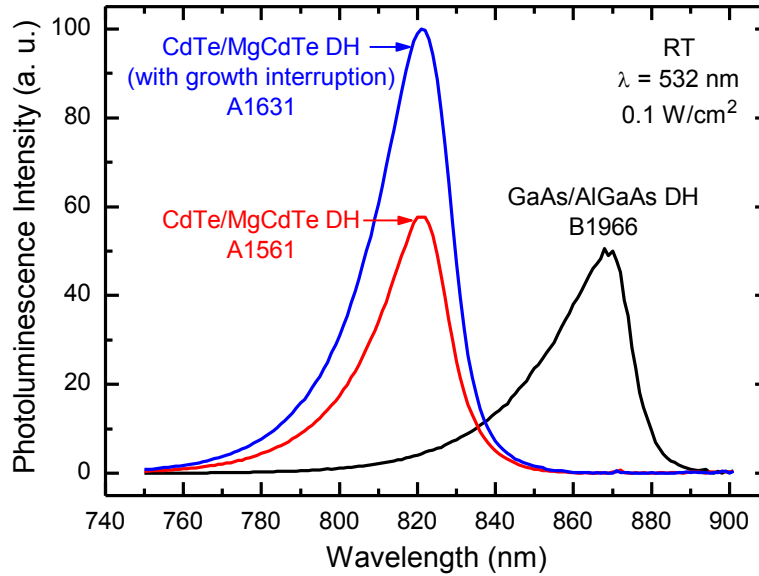


Figure 7.2. Room temperature PL spectra of a CdTe/MgCdTe DH with growth interruption in the buffer layer, the uninterrupted DH sample with 86 ns lifetime, and the GaAs reference sample.

The layer structures for all four solar cell samples discussed in this work are shown in Fig. 7.3. A1643 and A1645 were grown within one day of each other and both were shipped to Notre Dame together. The samples were loaded into the UHV preparation chamber at Notre Dame within 48 hours after being removed from vacuum at ASU. The spacer layer was omitted from sample A1645 to determine the effect of exposure to air, and that sample also has a slightly higher emitter doping concentration. After some initial testing, it was found that A1645 gave better ohmic contacts to the p-ZnTe emitter, so the next two samples A1646 and A1647 were designed with a slightly higher emitter doping concentration. The measured growth rate for ZnTe was significantly larger than expected, so samples A1646 and A1647 have a shorter growth

duration in order to reach the target 60 nm thickness. Lastly, two different kinds of substrates were used: single-side polished (SSP) and double-side polished (DSP). SSP wafers give better temperature uniformity, which is evidenced by significant melting around the edge of the DSP InSb wafers during thermal oxide removal. The better temperature uniformity of the SSP InSb gives a more uniform InSb buffer layer and more uniform CdTe/MgCdTe DH PL intensity across the wafer. Unfortunately, the manufacturer discontinued the production of SSP wafers and so DSP wafers must be used in the future.

		A1643	A1645	A1646	A1647
Emitter	p-ZnTe	90 nm		60 nm	
		3.7×10^{18}	5.4×10^{18}	$N_A = 8 \times 10^{18} \text{ cm}^{-3}$	
Spacer	i-ZnTe	15 nm	-	15 nm	-
Base	n-CdTe	1000 nm $N_D = 1 \times 10^{16} \text{ cm}^{-3}$			
BSF	n-Mg _{0.24} Cd _{0.76} Te	30 nm, $N_D = 5 \times 10^{18} \text{ cm}^{-3}$			
Buffer	n-CdTe	500 nm, $N_D = 5 \times 10^{18} \text{ cm}^{-3}$			
Buffer	n-InSb	500 nm, $N_D = 5 \times 10^{18} \text{ cm}^{-3}$			
Wafer	n-InSb	$n > 1 \times 10^{16} \text{ cm}^{-3}$ Single side polished		$n > 1 \times 10^{17} \text{ cm}^{-3}$ Double side polished	

Figure 7.3. Solar cell layer structure design matrix showing four samples. All values listed are inferred from calibrations.

7.2 Processing of ZnTe/CdTe/MgCdTe DH solar cells

A brief overview of the processing flow is presented along with a discussion about the emitter contact resistivity. Before any processing, samples are cleaved into roughly 2 cm × 2 cm pieces from a 2" diameter wafer with the epitaxial layer structure. Many individual solar cells are made on one wafer piece, and the area of each cell is

defined by a square mesa. The mesa dimensions range from 0.6 mm to 5 mm. Each device is identified by the sample number, size, and device number on the pattern. For example, the sample with highest measured efficiency is designated as A1646 1×1 (212), where A1646 is the wafer growth number, 1×1 is the size (1 mm × 1 mm), and (212) is the device number. The top contact consists of a central busbar and perpendicular finger contacts, with one contact pad on the perimeter for probing.

The sample processing begins by depositing a Ti/Au (50 nm/50 nm) back contact using an electron-beam evaporator. It is found that both SSP and DSP InSb wafers are highly conductive and low resistance contacts can be easily made (the contact resistivity is too low to measure). Following the deposition, processing begins on the top side. Photolithography is used to define the emitter contact grid. Following the photoresist exposure and development, the native oxide is etched for 30 seconds using 1:1 HCl:H₂O and the sample is immediately placed in the electron beam evaporator for the emitter grid deposition. Previous studies have shown that the sequence of Ni/Ti/Pt/Au (10 nm/50 nm/50 nm/100 nm) produces low-resistivity ohmic contacts without annealing [57]. After deposition, excess metal is removed using the lift-off technique. Lastly, square mesa patterns are defined using photoresist and the exposed CdTe is etched using a solution of citric acid (diluted 50 % by weight using DI water)/H₂O₂ (10:1). This etch is found to selectively remove II-VI layers and leave III-V layers intact.

In addition to the solar cell devices, TLM (transfer length method) patterns are also defined on the surface so that the emitter grid contact resistivity can be measured. The TLM patterns consist of several rectangular contact pads placed in a row with

different spacing. By measuring the resistance between contact pads as a function of spacing, the contact resistivity can be determined using:

$$\rho_c = R_c W L_T \quad , \quad (7.1)$$

where ρ_c is the specific contact resistance in $\Omega \cdot \text{cm}^2$, R_c is the contact resistance, W is the width of the contact, and L_T is the transfer length [61]. For lateral current flow, the current density directly under the contact is not uniform and drops off exponentially from the edge of the contact. L_T is the characteristic length where the current density drops off by $1/e$. L_T and R_c are extracted from a plot of resistance vs. contact spacing. Figure 7.4 shows a plot of resistance vs. contact spacing for two of the solar cell samples. The x and y intercepts of the linear fit line equal $2L_T$ and $2R_c$, respectively [61]. Sample A1643 ($N_A = 3.7 \times 10^{18} \text{ cm}^{-3}$) gives a specific contact resistance of $\rho_c = 1.7 \times 10^{-3} \Omega \cdot \text{cm}^2$, while sample A1645 ($N_A = 5.4 \times 10^{18} \text{ cm}^{-3}$) gives a significantly lower value of $2.3 \times 10^{-5} \Omega \cdot \text{cm}^2$. Both values are low enough for the first demonstration of the solar cell at one sun concentration [62]. Sample A1646 shows a ρ_c of $2.4 \times 10^{-4} \Omega \cdot \text{cm}^2$, which is likely due to variations in the contact deposition, surface preparation, or doping concentration.

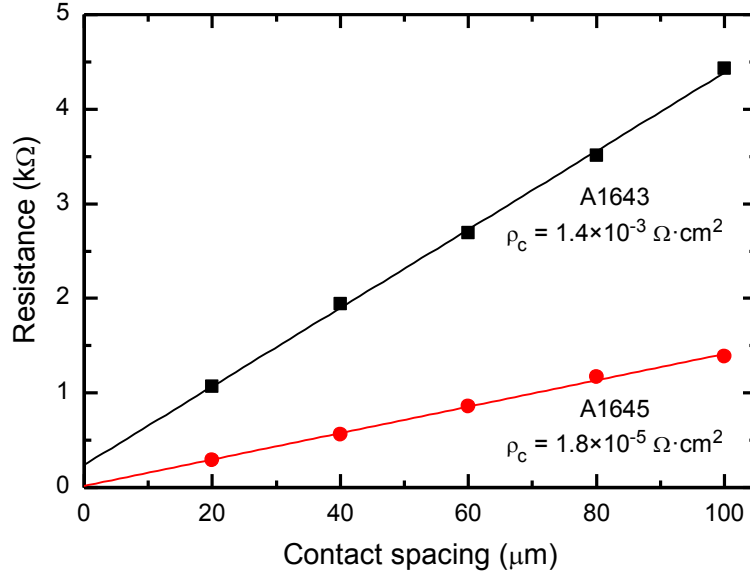


Figure 7.4. Contact resistivity determined by resistance vs. contact spacing for a TLM pattern.

7.3 Characterization of ZnTe/CdTe/MgCdTe DH solar cells

Solar cells are characterized using electrical and optical techniques in order to determine their performance and to discover where improvements can be made. In this study, a majority of the focus is placed on the “hero” sample, which is the solar cell with highest efficiency to date. That sample is A1646 1×1 (212). The first characterization step is the dark current density vs. voltage (J - V) measurement, which is shown in Fig. 7.5. The goal of this measurement is to determine the overall junction quality, and to extract the series resistance. The junction quality in a broad sense is represented by the magnitude of the forward bias dark current, which can be conveniently represented by the turn-on voltage V_T of the diode. V_T is defined in this text as the voltage which produces a current density of 30 mA/cm². This current density roughly corresponds to the maximum J_{sc} for a CdTe solar cell under one sun concentration. It is an important metric because J_{sc} equals the forward bias recombination current at the open circuit condition. Higher V_t is

desirable because a low V_t generally equates to low V_{oc} and efficiency. A high V_t however doesn't necessarily equate to high V_{oc} because series resistance can increase V_t and some devices violate the superposition principle. The turn-on voltage for this cell is 605 mV, which is far below what is expected for a wide band gap material with expected V_{oc} greater than 1 V. It is expected then that this cell will have a low V_{oc} .

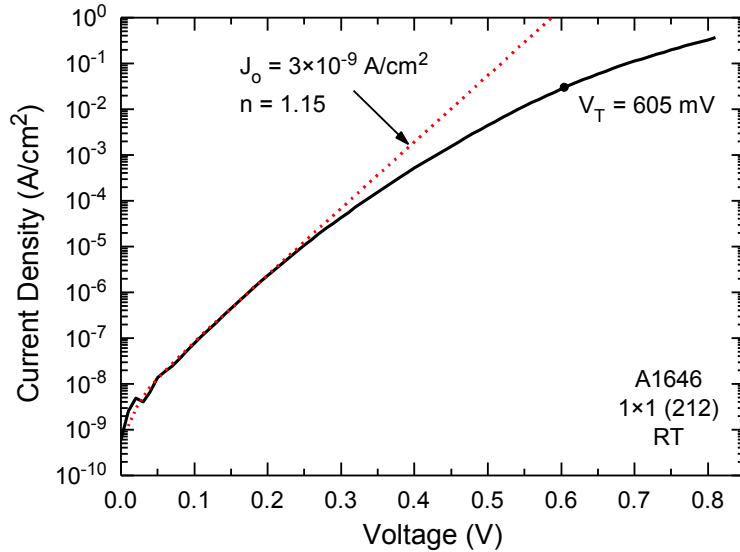


Figure 7.5. Dark J - V curve of the ZnTe/CdTe/MgCdTe DH solar cell at room temperature (solid) plotted with the ideal diode equation (dotted). The turn-on voltage V_T is defined at 30 mA/cm^2 .

Additional analysis of the dark J - V characteristic involves fitting the measured curve to the ideal diode equation (Eq. 6.1). In the ideal case, there will be several linear regions on a J - V curve when plotted on a semi-log plot, each linear region corresponding to a particular recombination mechanism. Figure 7.5 shows that a fit can only be made to the region between 0 V and 0.2 V. The difficulty of analyzing this curve is that the diode ideality factor (i.e. slope) continuously changes as a function of voltage. Nevertheless, some information can still be obtained. A relatively large reverse saturation current of $3 \times 10^{-9} \text{ A/cm}^2$ is observed, which suggests that there is a large forward-bias

recombination loss. Plotting the ideal diode equation with the measured data can be useful for determining the series resistance R_s , however this can only be done when the ideal diode equation can be fit over a larger range.

The next step is to measure the J - V characteristic under illumination. This is performed using a Newport sun simulator, which is calibrated to one sun concentration using a reference Si solar cell. The light J - V characteristic of the hero sample is shown in Fig. 7.6, and the performance metrics are listed in Table 7.1 along with the simulation results for the default structure. The low efficiency of 6.11 % is caused by a combination of low V_{oc} and low J_{sc} . Additional measurements are discussed in the following to explain these low metrics.

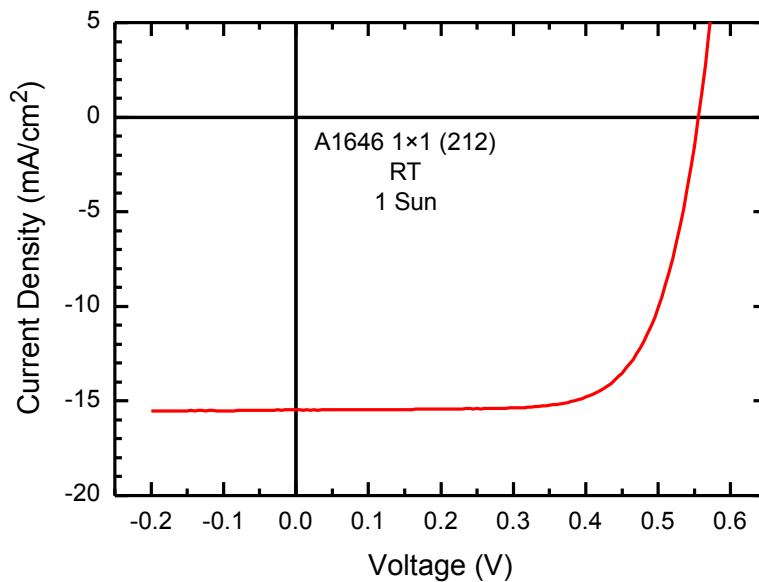


Figure 7.6. Photo J - V curve of the ZnTe/CdTe/MgCdTe DH solar cell at room temperature under one sun concentration.

Table 7.1. Measured and simulated solar cell performance.

Metric	Measured A1646 1×1 (212)	Simulated
Efficiency (%)	6.11	27.2
J_{sc} (A/cm ²)	15.5	28.6
V_{oc} (V)	0.556	1.096
Fill factor (%)	71.2	86.8
R_{sh} (Ω·cm ²)	4.3×10^3	-
R_s (Ω·cm ²)	0.65	-

The shunt and series resistances can be extracted from a combination of the light and dark J - V characteristics. The shunt resistance R_{sh} is an ohmic conduction path which occurs in parallel with the diode, and is mostly caused by macroscopic defects. It lowers the V_{oc} by creating an additional path for photocurrent to be lost. At low voltages, the diode differential resistance is very high, and so R_{sh} can be measured by taking the slope of the photo J - V curve at 0 V. R_{sh} is measured to be $4.3 \times 10^3 \text{ } \Omega \cdot \text{cm}^2$, which is sufficiently large to have a negligible impact on the solar cell performance. The series resistance R_s is caused by ohmic losses from many sources within the device and the metal contacts. R_s is measured using both the dark and light J - V characteristics. First, the photocurrent is assumed to be equal to J_{sc} , and V_{oc} is the junction voltage for which the forward bias current equals the photocurrent. The measurement of V_{oc} represents the actual junction voltage without the effect of R_s because the current is zero. V_{oc} is then compared to the voltage measured in the dark when a current J_{sc} is flowing through the device. The voltage difference divided by the current gives R_s , which is determined to be $0.65 \text{ } \Omega \cdot \text{cm}^2$. This resistance is also sufficiently low [62] and is therefore not the major problem limiting the efficiency. The negligible effect of the parasitic resistances is reflected in the fill factor, which is defined as:

$$FF = \frac{J_m V_m}{J_{sc} V_{oc}}, \quad (7.2)$$

where FF is the fill factor, J_m and V_m are the current density and voltage at the maximum power output condition. It is known that when parasitic resistances are very high, FF suffers considerably. The value of 71.2 % for this device is reasonable, and the shape of the photo J - V curve doesn't suggest that parasitic resistances are the major limiting factor for this device.

The low J_{sc} is investigated next. Figure 7.7 shows the external and internal quantum efficiency (EQE and IQE, respectively) as a function of excitation wavelength, along with the measured reflectance and calculated transmittance. The transmittance is defined as the ratio of photons above the band gap of CdTe that are transmitted into the back MgCdTe barrier layer to the incident AM1.5G spectrum. It is assumed that photogenerated carriers in the MgCdTe and buffer layers don't contribute to the photocurrent. The EQE is measured under the short-circuit condition, so it is used to diagnose problems with J_{sc} . The EQE is measured using a chopped monochromatic light source and lock-in amplifier. The intensity of the monochromatic light is calibrated using a Si reference detector. With the EQE and reflectance accurately measured, the IQE is determined using Equation (6.1). Figure 7.7 shows that the IQE can reach as high as 88 % and is relatively flat over the range of 550 nm to 820 nm. The wavelength 820 nm corresponds to the band gap of CdTe, while 550 nm corresponds to ZnTe. The relatively flat IQE indicates that the CdTe/MgCdTe interface recombination velocity is relatively low, and that the diffusion length is longer than 1 μm . On the other hand, there is a sharp drop in IQE for wavelengths below 550 nm. This is attributed to recombination loss and

short diffusion length in ZnTe. Since the ZnTe layer is not passivated, there will be significant surface recombination where EHPs can recombine. Some photons can transmit through the ZnTe layer, so there is still photocurrent contribution from the short wavelength light. The reflectance loss comes from the fact that there is no anti-reflection (AR) coating. A photocurrent loss of 7.56 mA/cm^2 is calculated based on the reflectance measurement and the AM1.5G spectrum.

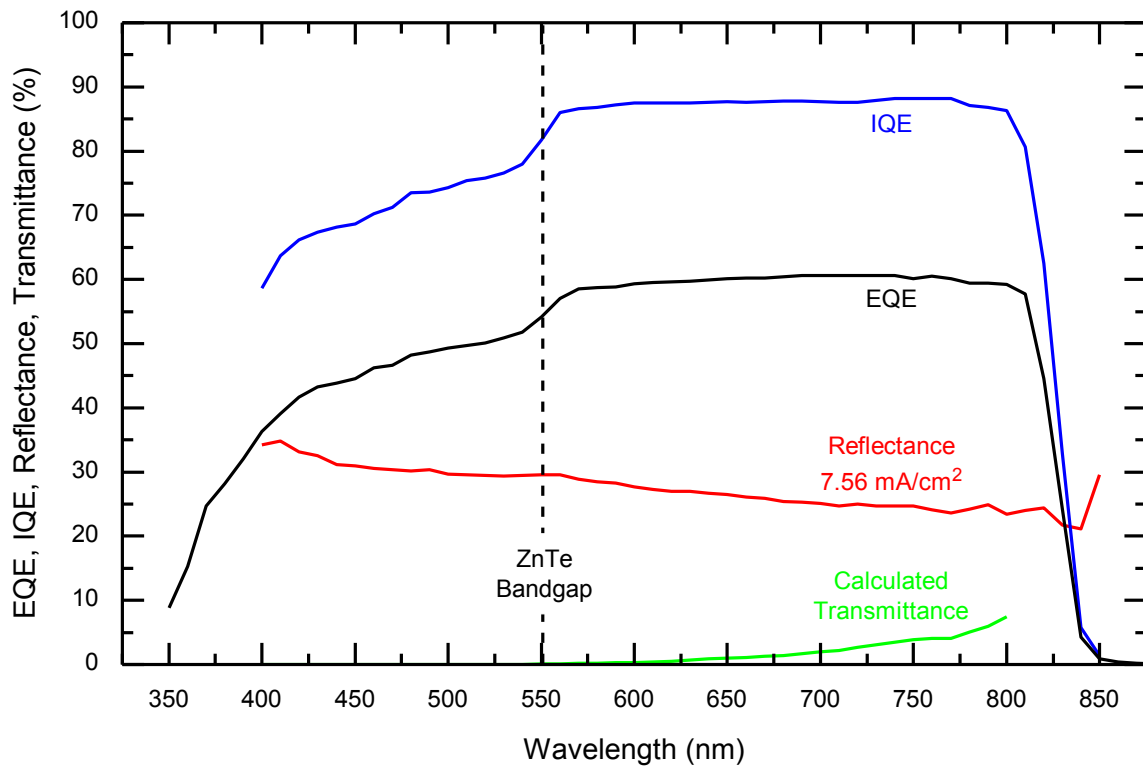


Figure 7.7. Internal and external quantum efficiency, measured reflectance, and calculated transmittance as a function of wavelength for the ZnTe/CdTe/MgCdTe DH solar cell sample. The current loss due to reflectance is calculated for the AM1.5G spectrum.

The current losses are further investigated by calculating the reflectance and absorbance in each layer as a function of wavelength, as shown in Fig. 7.8. The transfer matrix method is used for the calculation, and the published optical constants are used [30]. The photocurrent contribution is calculated for each layer by integrating the

individual layer contribution with the photon flux (AM1.5G) for photon energies above the band gap of CdTe. An EQE of 60 % for CdTe is calculated, which is close to the measured value shown in Fig. 7.7. Also, the measured reflectance loss is almost equal to the calculated value. A comparison of the measured and predicted EQE in the wavelength range of 350 nm to 550 nm shows that ZnTe must contribute photocurrent, otherwise the measured EQE would drop much more sharply like the predicted CdTe absorptance tail.

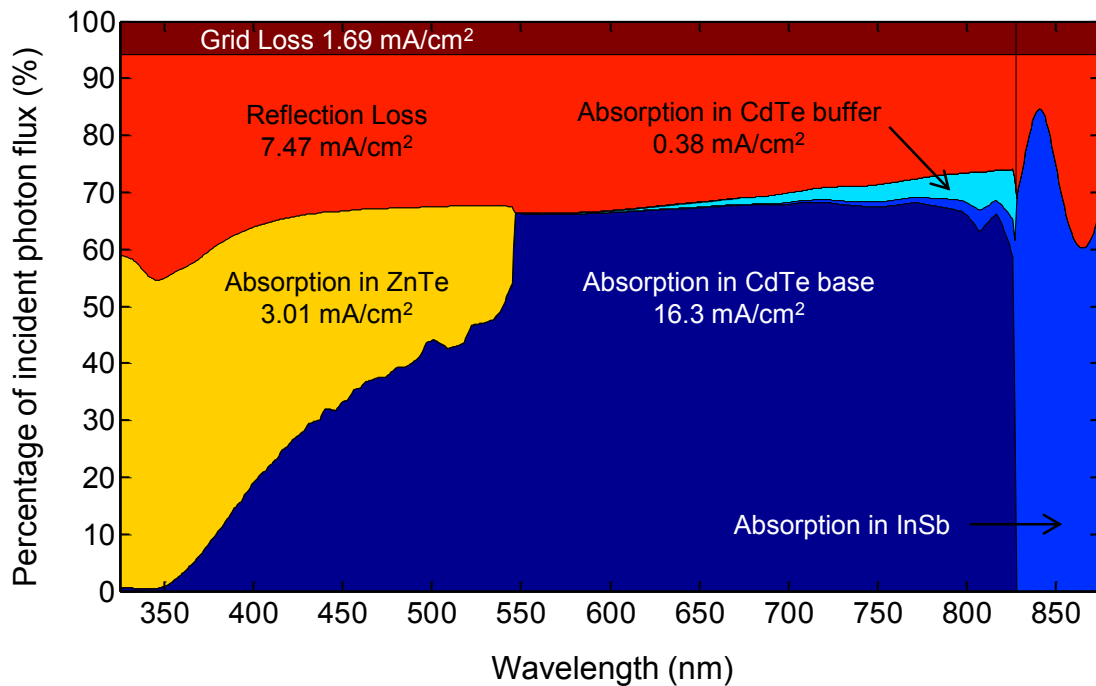


Figure 7.8. Calculated reflectance and absorptance as a function of wavelength for the ZnTe/CdTe/MgCdTe DH with the structure of A1646. *Figure provided by Yuan Zhao at ASU.

A projection of the solar cell performance with AR coating is shown in Fig. 7.9. In order to make the projection, the measured J - V curve is shifted by 90 % of the current loss due to reflectance. The measured reflectance current loss is used, and 90 % represents the IQE of the device. The plot in Fig. 7.9 shows a projected efficiency of 9.15 %. The J_{sc} is still below the simulated value, but that is expected because the

simulation doesn't take into account the grid loss, and the experimental IQE of both ZnTe and CdTe is not 100 %. By shifting the J - V curve to correct for the absence of an AR coating, V_{oc} also increases slightly. However it is still far from the 1.1 V benchmark set by the simulation. Therefore it can be concluded that the low V_{oc} is the major limiting factor for this solar cell, and that the addition of an AR coating cannot solve the problem of low efficiency.

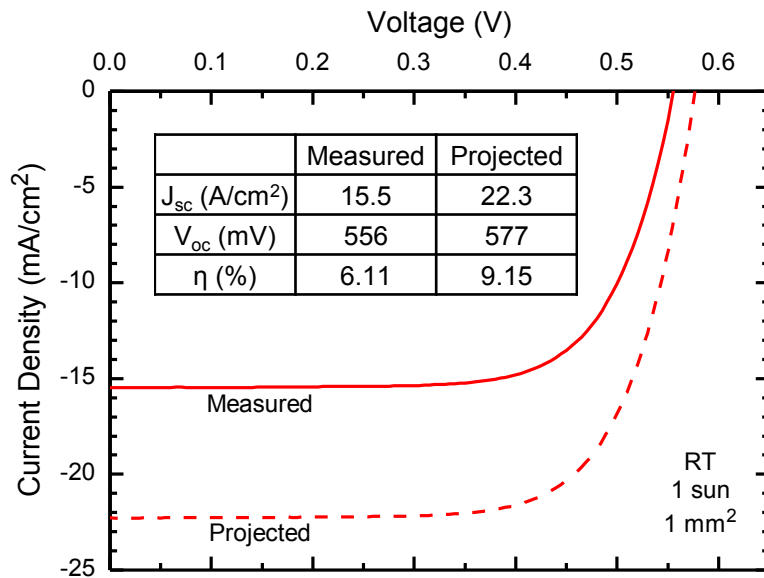


Figure 7.9. Measured J - V curve of the ZnTe/CdTe/MgCdTe solar cell with record high efficiency and projected performance for the same cell with an AR coating.

There are several factors that can reduce V_{oc} and each factor is systematically ruled out until a reasonable explanation is found. The first possibility considered is a low bulk carrier lifetime in the CdTe base. As explained previously, the dark current is dominated by hole injection from p-ZnTe into n-CdTe. A shorter carrier lifetime gives a larger recombination rate and therefore larger dark current and lower V_{oc} . However, the short carrier lifetime that is necessary to reduce V_{oc} by a factor of 2 would also have a

negative effect on J_{sc} . More specifically, the IQE of photons near the CdTe band gap would be poor. Long wavelength photons generate EHPs deep within the base, and those carriers cannot reach the junction if the lifetime and diffusion length is short. The IQE shown in Fig. 7.7 is almost constant up to the CdTe band edge, so it can be concluded that the bulk carrier lifetime in CdTe is not the most significant problem for this cell.

The second consideration is the BSF layer, or more specifically the interface between MgCdTe and the CdTe base. Three problems can occur here: interface recombination and voltage drops caused by series resistance and the photovoltaic effect. The nearly constant IQE for CdTe rules out interface recombination using a similar argument discussed above. Furthermore, lifetime measurements of undoped DHs show an interface recombination velocity of only 461 cm/s [16], which is not large enough to cause the low V_{oc} problem. On the other hand, there is a series resistance introduced by the potential spike in the conduction band which affects majority carrier transport. This however cannot affect V_{oc} because the voltage drop across it is zero under open-circuit (zero current) conditions. Series resistance will affect the fill factor, and if severe enough it can affect J_{sc} , but not V_{oc} . Lastly, the photovoltaic effect is present in isotype heterojunctions because the heterojunction effective force can provide charge separation [63]. However, this voltage is shown to be less than 100 mV [63], which is not large enough to explain the low V_{oc} in this study.

The most likely cause of the low V_{oc} is recombination at or near the ZnTe/CdTe interface, which is enhanced by unfavorable structure properties. From a circuit perspective, interface recombination is a parallel recombination process and is modeled as a diode in parallel with the PN junction. In this circuit, V_{oc} is reduced while J_{sc} remains

the same. J_{sc} is not significantly affected because the internal electric field is highest under the short-circuit condition, and carriers are swept away from the junction before they can recombine. Under open-circuit conditions, the internal electric field is small and electrons with enough thermal energy can overcome the small band bending and reach the interface. At the interface there are many trap states below the band gap, and so electrons can be captured and recombine with holes. It is also conceivable that electrons can tunnel into trap states within the highly defective ZnTe layer (away from the interface) and recombine with holes. Both of these proposed recombination mechanisms can explain the device behavior, however it is beyond the scope of this study to investigate which one dominates.

As shown previously, interface recombination increases as the built-in electric field (and hence V_{bi}) decreases, so any structural properties that lower V_{bi} should be investigated. Low emitter doping is one potential reason for the low V_{bi} . The ZnTe doping was calibrated using a 500 nm thick doped layer grown on GaAs, which is quite different from the 60 nm thick layer grown on CdTe. It is possible that surface depletion and growth on a different substrate material has negatively impacted the emitter carrier concentration. Also, indium seems to act as a surfactant during growth of CdTe, as evidenced by the SIMS depth profile measurement (Fig. 7.1) which shows an indium spike at the CdTe surface. The surface indium may incorporate into ZnTe and cause compensation. However, the ZnTe layer cannot be totally compensated, otherwise the series resistance would be very high.

Table 7.2 compares the measured performance with the simulated performance of the default simulation structure and the same structure with 30 % reflectance and an

interface recombination velocity of 4.8×10^5 cm/s. The simulated V_{oc} is reduced by 200 meV, however it is still far from the measured value. The most probable explanation for the low experimental V_{oc} is still related to the interface, however there must be additional recombination or tunneling mechanisms taking place at the ZnTe/CdTe interface that PC1D is not accounting for.

Table 7.2. Measured and simulated solar cell performance with non-zero surface reflectance and ZnTe/CdTe interface recombination.

	Measured	Simulated	
	A1646 1×1 (212)	$R = 0\%$ $S = 0$ cm/s	$R = 30\%$ $S = 4.8 \times 10^5$ cm/s
Efficiency (%)	6.11	27.2	15.5
J_{sc} (mA/cm ²)	15.5	28.6	20.0
V_{oc} (V)	0.556	1.096	0.901

The efficiency and V_{oc} as a function of temperature is shown in Fig. 7.10. Lowering the temperature of the device lowers the non-radiative recombination rate, so V_{oc} and therefore efficiency is expected to increase as the temperature is lowered. V_{oc} shows a linear dependence with temperature while the efficiency shows saturation below 150 K. The reason for the saturation is a decrease in the fill factor, which is likely due to an increase in series resistance caused by carrier freeze-out. No saturation is seen in V_{oc} since it is not affected by series resistance. Saturation of V_{oc} would likely indicate a transition from non-radiative recombination dominated to radiative recombination dominated operation, since the carrier lifetime reaches a maximum at that transition. The absence of V_{oc} saturation then indicates that the device is dominated by non-radiative recombination at room temperature.

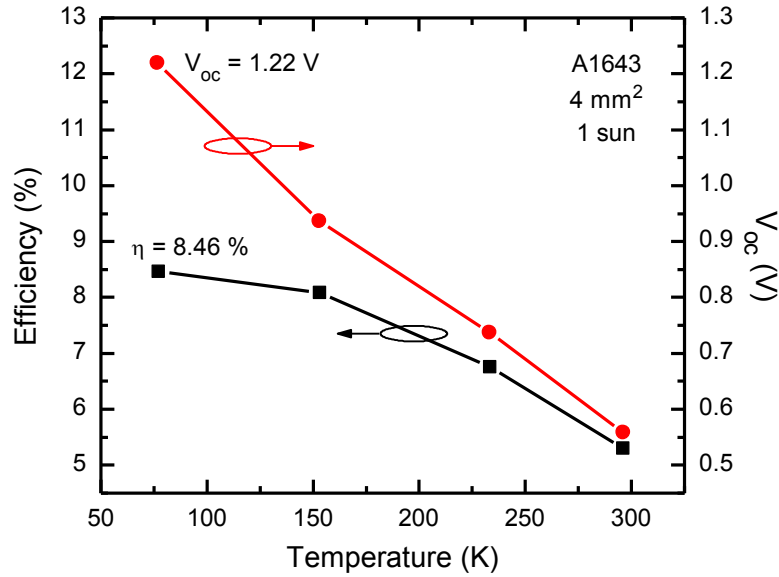


Figure 7.10. Efficiency and V_{oc} as a function of temperature for sample A1643 2×2 (211) under one sun concentration.

The properties of the remaining samples are investigated in order to determine the effect of the emitter thickness, the use of an undoped ZnTe spacer layer, and the use of single-side polished (SSP) or double-side polished (DSP) wafers. Many devices on each wafer piece are characterized in order to obtain a statistical representation of the sample structure quality. Figure 7.11 shows a scatter plot of the efficiency vs. sample number. Unfortunately only five devices were characterized on sample A1645 before it was accidentally broken, and so a statistical analysis will be more difficult for that sample. Samples A1646 and A1647 show a much wider scatter in the efficiencies, and they show several devices with almost zero efficiency. The highest efficiency is observed for sample A1646.

oxide desorption is more complete in the center. It is therefore recommended that SSP wafers be used in the future, or DSP wafers should be used with an alternate wafer holder design which improves the uniformity.

A comparison of V_{oc} for the samples is shown in Fig. 7.12. Again, samples that use DSP wafers show a larger scatter in V_{oc} . The devices with low V_{oc} show very low J_{sc} below 1 mA/cm² and near zero efficiency. The reason for the low J_{sc} is currently unknown. A second observation is that samples with the undoped ZnTe spacer layer (A1643 and A1646) show approximately 30 mV higher V_{oc} in comparison to those without the spacer layer (A1645 and A1647). It is expected that capping the CdTe layer with As and exposing the sample to atmosphere will introduce contamination to the CdTe surface after the As cap is desorbed. That contamination introduces interface states when ZnTe is grown on top at Notre Dame. Therefore, moving the atmosphere-exposed interface into the wider band gap ZnTe should lower the recombination rate at the ZnTe/CdTe interface. Although the observed 30 mV improvement is still a step in the right direction, it is not significant enough to reach the expected 1.1 V V_{oc} .

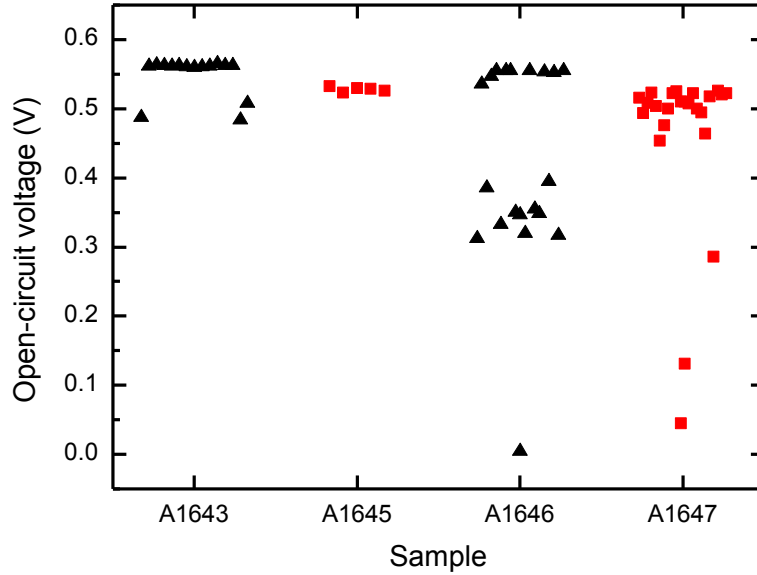


Figure 7.12. Scatter plot of V_{oc} vs. sample number for samples with i-ZnTe spacer layer (black triangles) and without spacer layer (red squares) at room temperature and under one sun concentration.

Lastly, a comparison of J_{sc} for the various samples is shown in Fig. 7.13. The maximum J_{sc} is held by sample A1647 which has the thinnest ZnTe layer (60 nm). An improvement of J_{sc} with a thinner ZnTe layer is expected because the IQE of the ZnTe layer is relatively poor. The difference between A1647 (ZnTe thickness = 60 nm) and A1643 (105 nm) is only 0.6 mA/cm², however. It is apparent that the uniformity of devices across the wafer needs to be improved significantly in order to improve the statistical analysis.

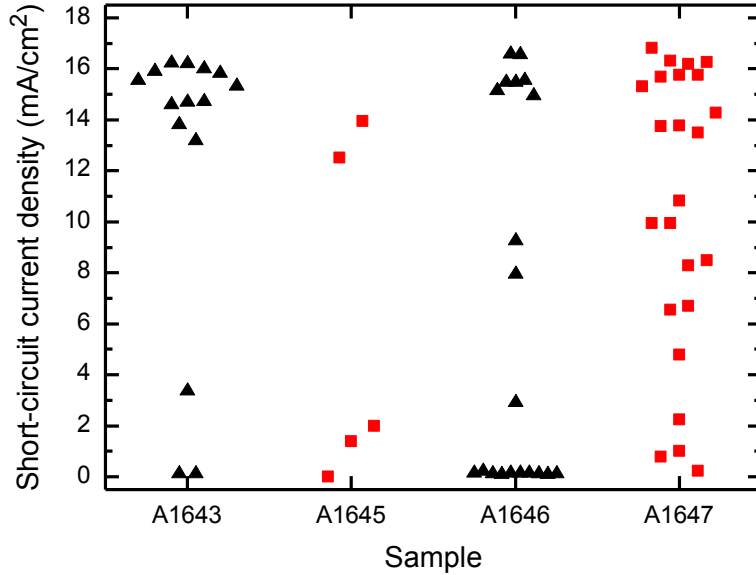


Figure 7.13. Scatter plot of J_{sc} vs. sample number for samples with i-ZnTe spacer layer (black triangles) and without spacer layer (red squares) at room temperature and under one sun concentration.

The experimental results discussed above show promise for the use of monocrystalline CdTe grown on InSb for demonstrating solar cells which approach the detailed-balance limit, however much work needs to be done to improve the material and interface quality. It is apparent that recombination at the ZnTe/CdTe interface must be minimized in order to obtain devices with high V_{oc} . A p-MgCdTe emitter layer grown directly on CdTe without atmospheric transfer is the most promising route to high V_{oc} devices, and this can be achieved by installing more suitable dopant sources such as arsenic into the II-VI chamber at ASU.

CHAPTER 8

CONCLUSIONS

Monocrystalline ZnTe/CdTe/MgCdTe P-n-N heterostructure solar cells grown on InSb substrates are designed and demonstrated for the first time. This achievement was preceded by the demonstration of undoped CdTe/MgCdTe double heterostructures (DHs) with long carrier lifetimes up to 179 ns for a 2 μm thick CdTe layer and 97 ns for a 1 μm layer. Both of these demonstrations are enabled by the use of a dual-chamber molecular beam epitaxy (MBE) system employing separate III-V and II-VI growth chambers. Furthermore, MgCdTe barrier layers are found to be effective at confining photogenerated carriers and are useful for photoluminescence (PL) test structures.

CdTe/MgCdTe single heterostructures (SHs) and DHs are grown in order to investigate recombination mechanisms within CdTe and at interfaces and surfaces. Surface recombination is shown to dominate for CdTe samples without barrier layers near the surface. This is evidenced by a three order of magnitude improvement in the PL intensity for DHs in comparison to a structure without a top barrier. Recombination within the buffer layers also dominates when the back barrier is omitted, as evidenced by a fivefold improvement in the PL intensity for the DH sample.

The crystalline and optical quality of CdTe/MgCdTe DHs are systematically investigated using various techniques, and the growth conditions are optimized. X-ray diffraction (XRD) mapping shows that all of the epilayers are coherently strained to the substrate. High-resolution transmission electron microscopy (TEM) measurements show that CdTe/InSb and CdTe/MgCdTe interfaces are abrupt and have low dislocation density. The carrier lifetime of CdTe/MgCdTe DHs grown under different conditions is

measured using time-resolved photoluminescence (TRPL) measurements. An optimal growth substrate temperature of 265 °C and Cd/Te flux ratio of 1.5 is determined for the CdTe/MgCdTe DH, which has a carrier lifetime ranging from 78 ns to 97 ns depending on the position on the wafer. The PL intensity of the CdTe/MgCdTe DH is comparable to a GaAs/AlGaAs DH sample with identical layer structure design, which further shows the potential for CdTe as a photovoltaic material for high efficiency solar cells.

ZnTe/CdTe/MgCdTe double heterostructure solar cells are designed, grown, fabricated, and tested. Modeling is performed in order to predict the efficiency and determine which parameters have the largest effect on the efficiency. It is found that any parameter which lowers the built-in electric field at the ZnTe/CdTe interface has a strong negative effect on the efficiency when recombination at that interface is included in the model. These parameters include the emitter doping concentration and the valance band offset between ZnTe and CdTe. The highest efficiency experimentally achieved so far is 6.11 %, with a projected efficiency of 9.15 % if a perfect AR coating is employed. The low efficiency is due to the low open-circuit voltage (V_{oc}), which is likely caused by recombination at the ZnTe/CdTe interface. Although the demonstrated efficiency is far below the detailed balance limit for CdTe, this work represents the first step in achieving high-efficiency devices. One possible way to achieve higher efficiency is to replace the relaxed ZnTe emitter layer with a coherently strained MgCdTe emitter layer, which should have much lower interface recombination and therefore higher V_{oc} and efficiency.

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APPENDIX A

MATERIAL PARAMETERS USED FOR PHOTOLUMINESCENCE STRUCTURE

DESIGN

	CdTe	MgTe	Mg_{0.18}Cd_{0.82}Te	InSb	GaAs	Al_{0.3}Ga_{0.7}As
A ₀ (Å)	6.481	6.420	6.470*	6.479	5.6533	5.6556 [17, p. 804]
E _g (eV)	1.506	3.0 [20]	1.77*	0.17	1.424	1.798*
C ₁₁ (10 ¹¹ dyne/cm ²)	5.35	5.28	5.34*	-	-	-
C ₁₂ (10 ¹¹ dyne/cm ²)	3.69	3.66	3.68*	-	-	-
α (at 532 nm) (cm ⁻¹)	7.54×10 ⁴	-	5.27×10 ⁴	-	7.03×10 ⁴	3.75×10 ⁴
Reflectivity (at 532 nm)	0.271	-	-	-	0.374	-

*Linearly interpolated from the values of binary compounds

**Binary parameters from references [29] and [30]

APPENDIX B

MATERIAL PARAMETERS USED IN PC1D SIMULATIONS

Parameter	CdTe	MgTe	Mg _{0.24} Cd _{0.76} Te	ZnTe	Refs
E _g (eV)	1.51	3.0 [20]	1.86	2.27	[29]
m _e *	0.09	0.17	0.11	0.117	[29]
m _{HH} *	0.76	0.71	0.75	0.62	[29]
m _{LH} *	0.144	0.20	0.16	0.158	[29]
N _c /N _v	0.0376	-	0.0511	0.0726	Calc.
n _i (cm ⁻³)	7.59×10 ⁵	-	1.02×10 ³	3.43×10 ⁻¹	Calc.
μ _n (cm ² /v/s)	1050	-	50***	600	[29]
μ _p (cm ² /v/s)	104	-	50***	50*	[29]
ε _r	10.4	6.95	9.57	9.4	[29]
τ _p , τ _n (ns)	97	-	1***	1***	-
ΔE _v (meV)	0	447 [20]	107	80**	-
Electron Affinity (eV)	4.28 [29]	-	4.037	3.44	-

*Measured

**Averaged from many sources [46, 47, 48, 49, 51, 50, 52]

***Assumed value