Self-Calibration And Digital-Trimming Of Successive Approximation Analog-To-Digital Converters

by

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ABSTRACT

Several state of the art, monitoring and control systems, such as DC motor controllers, power line monitoring and protection systems, instrumentation systems and battery monitors require direct digitization of a high voltage input signals. Analog-to-Digital Converters (ADCs) that can digitize high voltage signals require high linearity and low voltage coefficient capacitors. A built in self-calibration and digital-trim algorithm correcting static mismatches in Capacitive Digital-to-Analog Converter (CDAC) used in Successive Approximation Register Analog to Digital Converters (SAR-ADCs) is proposed. The algorithm uses a dynamic error correction (DEC) capacitor to cancel the static errors occurring in each capacitor of the array as the first step upon power-up and eliminates the need for an extra calibration DAC. Self-trimming is performed digitally during normal ADC operation. The algorithm is implemented on a 14-bit high-voltage input range SAR ADC with integrated dynamic error correction capacitors. The IC is fabricated in 0.6-um high voltage compliant CMOS process, accepting up to 24Vpp differential input signal. The proposed approach achieves 73.32 dB Signal to Noise and Distortion Ratio (SNDR) which is an improvement of 12.03 dB after self-calibration at 400 kS/s sampling rate, consuming 90-mW from a +/-15V supply. The calibration circuitry occupies 28% of the capacitor DAC, and consumes less than 15mW during operation. Measurement results shows that this algorithm reduces INL from as high as 7 LSBs down to 1 LSB and it works even in the presence of larger mismatches exceeding 260 LSBs. Similarly, it reduces DNL errors from 10 LSBs down to 1 LSB. The ADC occupies an active area of 9.76 mm^2.

Dedicated to my Parents

Dr. D. Thirunakkarasu and Mrs. J. Selvalatha

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LIST OF ABBREVIATIONS

A/D	Analog/Digital Converter
ADC	Analog-to-Digital Converter
D/A	Digital/Analog Converter
DAC	Digital-to-Analog Converter
DNL	Differential Non Linearity
DRC	Design Rule Check
ESD	Electro Static Discharge
INL	Integral Non Linearity
IOS	Input Offset Storage
LSB	Least Significant Bit
LVS	Layout versus Schematic
MSB	Most Significant Bit
NMOS	N-type mosfet
OOS	Output Offset Storage
PMOS	P-type mosfet
S/H	Sample and Hold
SAR	Successive Approximation Register
SOC	System On Chip
SOS	Silicon On Sapphire
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio

T/H	Track and Hold
THD	Total Harmonic Distortion
VHDL	Very-high-speed-integrated-circuit Hardware Description Language

PREFACE

Successive Approximation Register Analog-to-Digital Converter (SAR ADC) uses binary search algorithm for converting an analog input value into a digital equivalent output code. In a high precision SAR ADC, the binary matching between the capacitors determine the linearity of the converter. Usually trimming is done at final test to improve the linearity. So there is a huge amount of trim time getting wasted at final test, in order to physically correct the mismatches in binary weighted capacitors. This study explains the architecture for Built-in Self-Calibration and Digital-Trimming of SAR ADCs which could be automatically performed on power-up. This architecture is designed and fabricated using 0.6 um HV-CMOS technology. The improvement in performance is proved in silicon. This work is divided into six chapters. A brief introduction to the contents of each chapter is outlined below.

Chapter 1 covers an overview of the existing analog to digital (A/D) converters. It also briefly touches upon the types of A/D converters with its performance metrics. It gives a very brief introduction to SAR A/D converters with a detailed literature survey on this type of Nyquist A/D converter.

Chapter 2 discusses the principle of conventional SAR A/D converter using binary search algorithm. It explains the different types of SAR A/D circuit blocks such as sample and hold (S/H), Digital-to-Analog (D/A) converter and comparator with different ways of implementing it. It also explains the performance metrics associated with each type of circuit block.

Chapter 3 discusses the conventional procedure for high precision SAR ADC calibration and trimming.

Chapter 4 explains in detail, the architecture of the proposed SAR ADC self-calibration and digital-trimming algorithm. All the implementation details involved in this type of algorithm is discussed.

Chapter 5 discusses in detail all the simulation and measurement results obtained during this work.

Chapter 6 concludes this dissertation with a recap of the work conducted and also with a possible list of future works that could be carried out in this field.

1 INTRODUCTION

1.1 OVERVIEW OF ANALOG TO DIGITAL CONVERTERS

The past few years will be remembered as the start of the "system on chip (SOC)"-style of design and manufacturing: the semiconductor companies are keen to cut costs and therefore gain a competitive edge by integrating all system functions onto a single substrate with as few external components as possible. This task is made much easier if analog signals, which are how any real-world quantity must inevitably be represented, are converted to digital form for on-chip processing. This helps in two main ways: digital signals are less susceptible to corruption by circuit noise and process variations. Also, more digital signal processing circuitry can be integrated into the same die area than analog circuitry. Thus, it is clear that analog-to-digital converter (ADC) circuits play an important role in modern integrated systems.

There are conceptually three distinct operations that are performed sequentially by an A/D converter [1],[2]: (1) It samples a continuous-valued, continuous-time analog signal; (2) it quantizes the sampled signal to a finite number of levels; (3) it assigns a digital code to the related quantized level. With this sequence of operations, any physical signal, no matter if it is mechanical, thermal, optical, acoustical, or magnetic, once it has been transformed into electrical signal by a proper sensor, it can be converted into digital signal by an A/D converter and processed conveniently with powerful digital signal processing components, out of which various useful information can be extracted.

A number of different approaches exist for the realization of Analog to Digital

Converters. Some of these approaches include Flash, Multi-Step, Pipelined, Algorithmic, Successive Approximation Register (SAR) and Sigma Delta Converters. All of the above are Nyquist rate converter except Sigma Delta converter which is an oversampling converter. Nyquist rate converters are those converters in which the sampling rate could be as low as twice that of the highest signal frequency component. This condition is required in order to reconstruct the original analog signal reliably in digital domain. On the other hand, oversampling sigma delta A/D converters require its sampling rate to be much larger than the highest signal frequency component. Different types of data converters are used for different applications. For applications like data acquisition, motor control, system interfaces, instrumentation applications, transducers etc where it is required to produce conversion with moderate accuracy and at moderate speed, SAR ADCs are generally preferred.

In a conventional SAR ADC, the number of clock cycles required to make one complete conversion process is equal to the number of bits of the A/D converter. This number of clock cycles poses a fundamental limit on the speed at which a complete conversion from analog domain to digital domain takes place. Also, in a conventional SAR converter, the fundamental bottleneck for high-precision comes from the matching requirements in a Capacitive Digital to Analog Converter. Typically in a high precision SAR ADC, the mismatch in the capacitors that occur during fabrication is trimmed at final test using in-package trimming mechanism. This is a time intensive process and increases test cost enormously. To reduce the time that it takes to test a single chip during final test and to reduce its associated cost, there is an urgent need to build a self-

calibration routine within the chip at design stage. A built in self-calibration and digital-trimming algorithm is proposed in this research to cancel the effect of mismatches occurring in Capacitive Digital-to-Analog Converter (CDAC) of Successive Approximation Register Analog to Digital Converter (SAR-ADC). This research work involved the fabrication of this built-in self calibration and digital trimming architecture in 50HPA07HV 0.6 um High Voltage Texas Instruments (TI) process and its hardware results are presented in Chapter 5.

There are many different performance metrics that are used to characterize a designed A/D converter. Some of the important parameters that are usually used to characterize an A/D converter include its resolution (number of bits), its speed (how many conversions it does per second), power consumption, Differential Non-Linearity (DNL) versus Codes, Integral Non-Linearity (INL) versus Codes, Signal to Noise and Distortion ratio (SNDR) versus Input frequency (fin), SNDR versus Sampling frequency (fs), SNDR versus Amplitude, Total Harmonic Distortion (THD), figure of merit etc. It is customary to design an A/D converter in order to maximize its resolution, speed, SNDR and figure of merit while the other characteristics such as power consumption, DNL, INL THD are minimized.

1.2 THESIS STRUCTURE

Chapter 2 describes the principles of a conventional successive approximation A/D converter. Chapter 3 discusses some of the prior architectures on calibration and trimming mechanism done in SAR A/D converters. Chapter 4 explains the proposed

research. Chapter 5 shows the simulation results and silicon measurements. Finally this dissertation is concluded in Chapter 6.

1.3 Literature Survey And Specifications of ADC

A lot of work has been done in the field of SAR ADCs. There are many different types of SAR A/D converters designed in the past for different applications. However in terms of architecture, there is not a major improvement that had taken place. Since the introduction of the first MOS implementation of a SAR ADC [3],[4] its architecture has remained relatively unchanged [5],[6],[7],[8],[9]. As shown in Fig. 1, the basic architecture of a conventional MOS charge redistribution SAR A/D converter consists of a charge-scaling DAC, a comparator, and digital control logic to implement the successive approximation algorithm. The only noticeable change found in some recent implementations has been the separation of the sample and hold function inherently present in the DAC [10],[11],[12],[13],[14]. When a charge-scaling DAC is employed in the ADC, using a separate sample and hold unit makes the input capacitance independent from the capacitor array. As a result, the ADC contributes less loading to the input circuitry or preceding stage. Modifications in architectures were also made to account for the on-chip self calibration circuits and in certain other non-conventional circuits [15],[16],[17],[18],[20],[21],[22],[23],[24],[25],[26],[27],[28],[29]. Other than these major architectural changes, all the other basic circuit blocks in SAR A/D converter remained more or less constant.

Table 1 summarizes the performance specifications of some of the recently

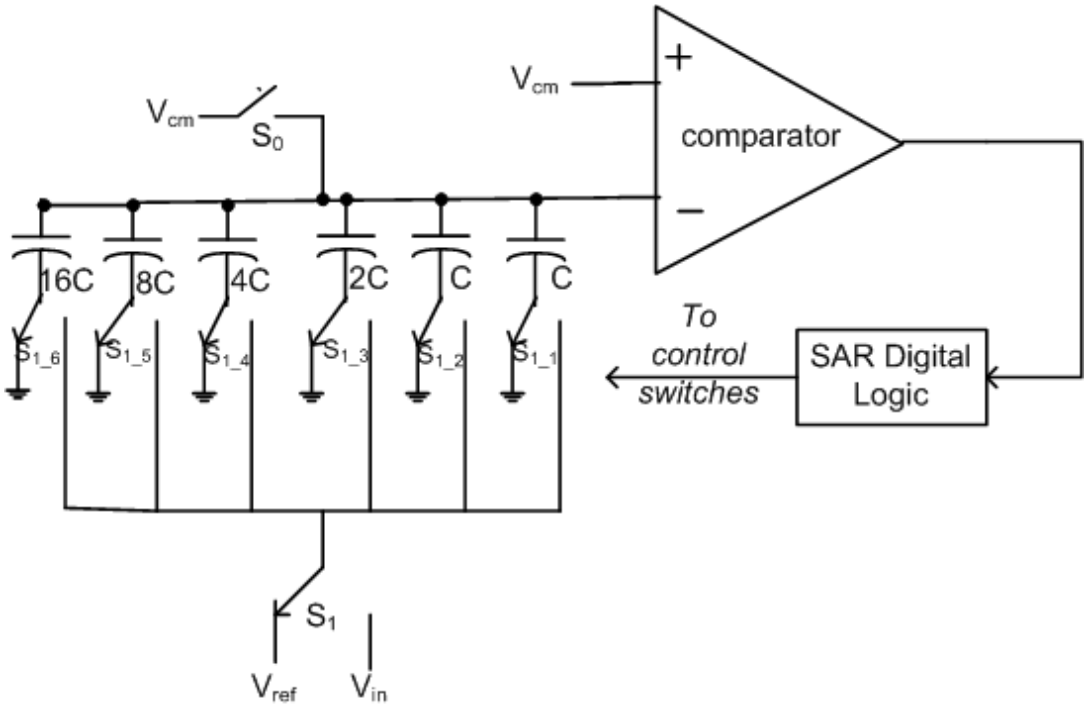

Fig. 1 MOS Charge Redistribution SAR A/D Converter

fabricated SAR A/D converters found in the literature.

In reference [5], an ultra-low power ADC for distributed sensor networks had been presented. The resolution achieved was 8-bits with 3.1 uW of power consumption.

In [6], a differential switched capacitor ADC producing a resolution of 12 bits at 1 MS/s is presented.

In [7], a SAR A/D converter implemented on a 0.5 um Silicon on Sapphire (SOS) technology producing a resolution of 8 bits at 1.23 MS/s is presented. The lack of parasitics in the Silicon on Sapphire is advantageously used in this paper.

A non-binary radix less than 2 SAR A/D converter is implemented in [8] having a resolution of 10 bit at 20 MS/s.

In [9], a high accuracy comparator is proposed with open loop and closed loop offset compensation techniques producing a resolution of 10 bit at 500 kS/s is presented.

[12] shows a method in which the op-amp input common mode voltages can be biased near ground to minimize the supply voltage. This paper produces a resolution of 8 bits at 50 kS/s.

In [30], a resolution-rate scalable ADC with 12 bit mode and 10 bit mode operating at 100 kS/s and at 200 kS/s respectively is presented.

Table 1 Comparison on Previous Works of SAR A/D Converters

Reference	**Supply**	**Resolution**	**Speed**	**Power**	**Technology**
M. D. Scott [5]	1 V	8-bit	100 kS/s	3.1 uW	0.25 um
N. Verma [30]	1 V	12-bit	200 kS/s	25 uW	0.18 um
G. Promitzer [6]	5 V	12-bit	1 MS/s	15 mW	0.6 um
E. Culurciello [7]	3.3 V	8-bit	1.23MS/s	1.5 mW	0.5 um (SOS)
J. Park [9]	1.5 V	10-bit	500kS/s	1 mW	0.25 um
F. Kuttner [8]	1.2 V	10-bit	20 MS/s	12 mW	0.13 um
S. Mortezapour[12]	1 V	8-bit	50 kS/s	0.34mW	1.2 um

After going through a number of previous works, it was decided to implement a built-in auto self-calibration and digital-trimming in SAR A/D converter with a high voltage 0.6 um CMOS technology for motor control applications using supply voltages of +/-15V. The SAR ADC is designed for high precision producing a resolution of 14 bits at the output. Table 2 shows the target specification goal set before the implementation of the SAR A/D converter.

This project was started with building up of a matlab model for a high precision 14-bit SAR A/D Converter. Then, capacitors are mismatched intentionally followed by the

Table 2 Specifications of the Target SAR A/D Converter

Parameter	**Target Specification**
Resolution	14 bits
Sampling Frequency	500 kS/s
Power Consumption	100 mW
Supply Voltage	5 V, +/-15V
Technology	0.6 um HVCMOS
INL	within +/- 1 LSB

application of this algorithm using matlab models. Integral and Differential Non-Linearities (INL/DNL) were seen to be less than +/-1-LSB. This algorithm was applied on a 14-bit high precision, high voltage SAR A/D converter operating between +/-15V accepting +/-10V input designed in 0.6um HV CMOS technology for motor control applications. Spectre/Virtuoso tools from Cadence were used for analog design. Digital RTL Design was done using HDL Designer from Mentor Graphics. Synthesis was done in Design Compiler from Synopsys and all the back-end work for digital place and route was done using Encounter from Cadence. The results are provided in Chapter 5.

2 CONVENTIONAL SAR A/D CONVERTERS

2.1. PRINCIPLE OF SAR A/D CONVERTER WORKING

An analog to digital converter converts an original input analog signal into an N-bit equivalent output digital codes. A conventional N-bit SAR A/D converter in particular takes N clock cycles for one full complete conversion process. This A/D converter consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC) and a digital logic. The ADC employs a binary-search algorithm that uses the digital logic circuitry to determine the value of each bit in a sequential or successive manner based on the outcome of a comparison between the outputs of the S/H circuit and DAC. Fig. 2 illustrates a basic block diagram of a conventional binary search SAR A/D converter [3],[4].

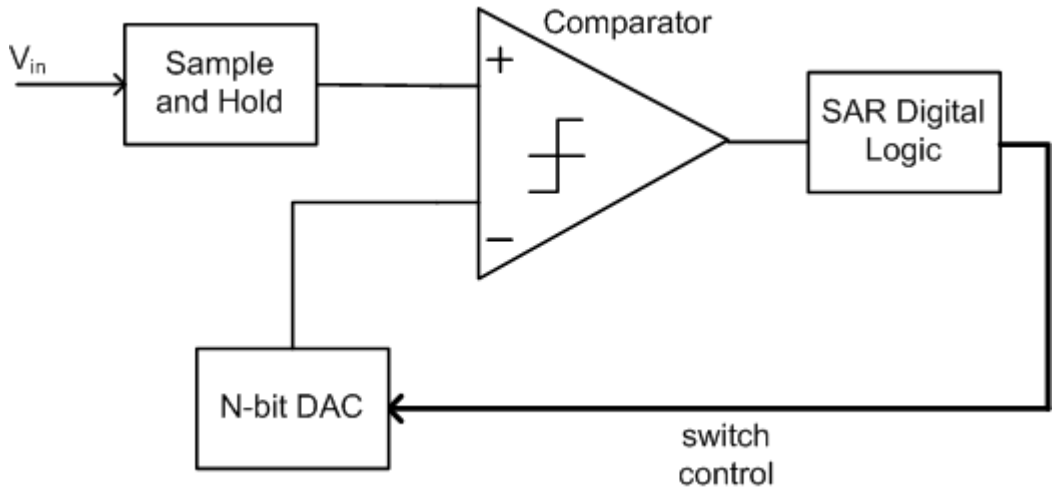

Fig. 2 Block Diagram of Conventional SAR A/D Converter

The conversion sequence starts by sampling an input analog signal through S/H circuit, where the input signal is converted from the continuous-time domain into the

discrete-time domain. The digital logic then sets the Most-Significant-Bit (MSB) to ’1’. With the remaining bits set to ’0’, the analog equivalent of the digital word produced will be equal to the mid-scale of the reference voltage, V_{ref}. The digital word is then applied to the DAC in order to produce an analog output voltage that, once settled within 0.5 LSB of accuracy, is compared with the sampled voltage by the comparator. A comparator output of ’1’ means that the sampled signal is larger than the DAC’s output. If this is the case the MSB remains as ’1’, otherwise, it is set to ’0’. The process is repeated by setting the next bit of the digital word to ’1’ and applying the digital word to the DAC for comparison of its output signal with that of the S/H circuit. Just as before, depending on the outcome of the comparison the bit either remains as ’1’ or is set to ’0’. The comparison cycle will continue until all bits have been successively determined. For an N-bit SAR A/D converter, it takes N cycles to determine the digital value corresponding to that of the sampled signal. Moreover, the precision required by the comparator increases as the converter goes from the MSB to the LSB in the approximation algorithm of the output code.

The main advantage of the SAR A/D converter is that the circuit complexity and power dissipation are far lesser than those found in most other types of ADCs [1], [5]. Its main disadvantage is the restriction towards achieving higher resolution and higher speed. As it takes N clock cycles for the A/D converter to do one complete conversion, the speed of the converter is limited by the output settling time of the DAC and the time needed by the comparator to resolve small input differences of the order of 1 LSBs’.

Moreover the resolution of the converter is restricted by the matching of the capacitors within each other in the capacitor array which is shown in Fig. 1.

2.2. ADC CIRCUIT BLOCKS

As previously seen, S/H circuit, DAC and comparator form the basic building blocks in all SAR A/D converters. Now a detailed description of the implementation of these circuit blocks based on Fig. 1 and how it affects the performance of the A/D converter will be given. The main performance metrics of each circuit block are described along with the different techniques available for the implementation of these circuits.

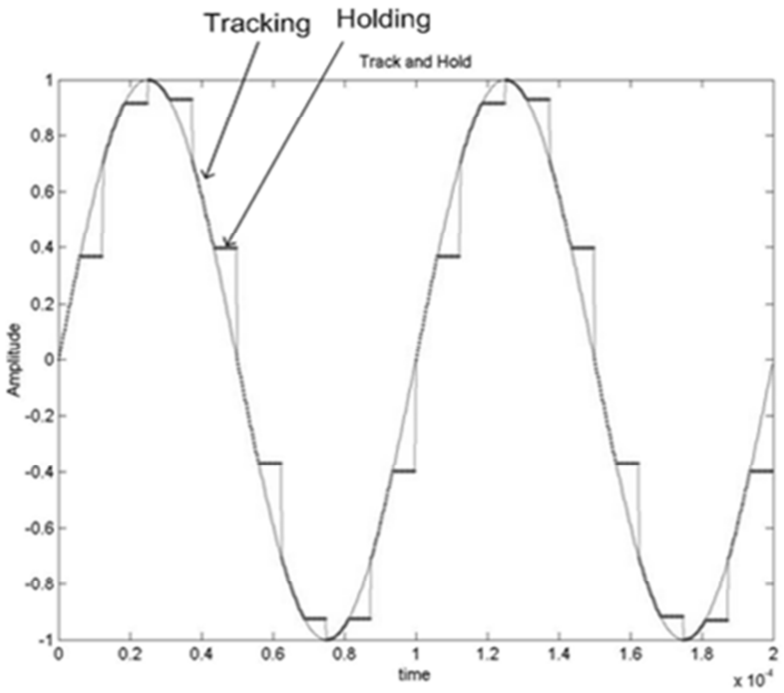

Fig. 3 Track and Hold

2.2.1. SAMPLE AND HOLD CIRCUIT

A sample-and-hold (S/H) circuit takes samples of its analog input signal and holds these samples in a memory element. These held samples are used by the A/D converter in each and every clock cycle and converts them into an equivalent digital output codes. The operation of S/H circuit is divided into two modes, sample and hold. During the sample-mode the output of the circuit can either track the input or reset to some fixed value. In

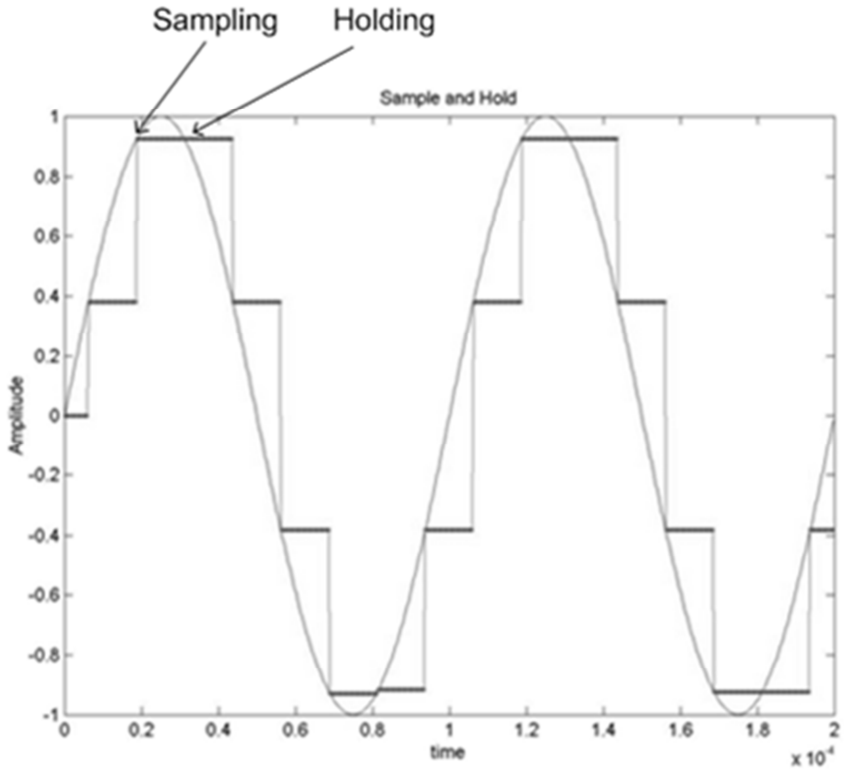

Fig. 4 Sample and Hold

the hold-mode, the output of the S/H circuit is equal to the input value obtained (sampled) at the end of the sample mode. Fig. 3 and Fig. 4 illustrate the example waveforms of a sample and hold (S/H) and track and hold (T/H) circuits respectively. Although there is

an obvious difference between the sampling and tracking, the majority of the circuits used today with the name sample and hold are all track and hold circuits.

Some of the important performance metrics of S/H circuit are explained in [1] and is shown in Fig. 5.

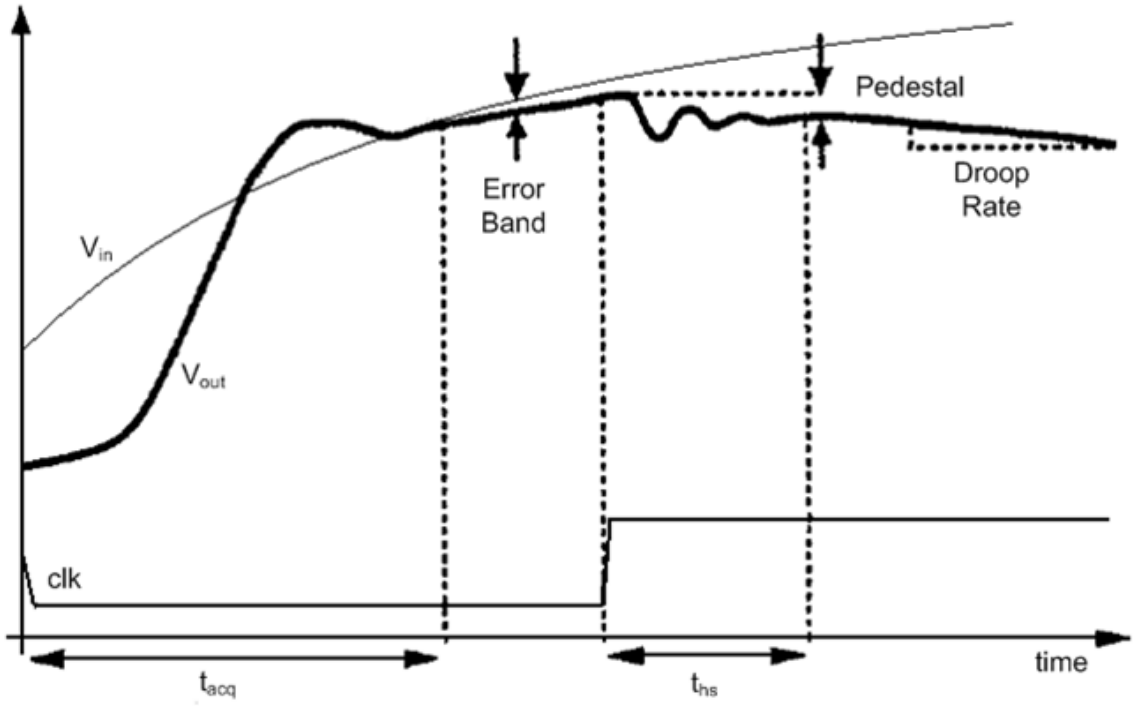

Fig. 5 Sample and Hold Performance Metrics from [1]

• Acquisition time, t_{acq}, is the time required, after the sampling command, for the S/H circuit to take a new sample, so that its output during the hold mode is within a specified error band.

• Hold settling time, t_{hs}, is the time required after the hold command is asserted for the S/H circuit's output to settle within a specified error band of its steady state value. This is usually the limiting factor on the sampling rate of the circuit.

- Dynamic range is the ratio of the maximum allowable input signal and the minimum input signal that can be sampled within a specified degree of accuracy.
- Signal-to-noise ratio (SNR) is the ratio of signal power to noise power present at the output in the hold mode.
- Signal-to-(noise + distortion) ratio (SNDR) is the ratio of the signal power to the total noise and harmonic power present at the output in the hold mode.
- Aperture jitter is the random variation in the time required for the sampling switch to turn off after the hold command is asserted. Also called "aperture uncertainty," this error is a measure of the deviation of sampling instants from equally spaced points in time and arises from the noise that affects the hold command assertion.
- Pedestal error is the error introduced at the output of the S/H circuit between the time when the sample mode ends and the time the hold mode is active.
- Droop rate is the rate of change of the output, due to signal leakage during the hold mode. It is the rate of discharge of capacitor during hold mode.
- Hold-mode feedthrough is the percentage of the input signal appearing at the output during hold mode. It is due to the signal coupling created by the parasitic elements surrounding the internal nodes of the S/H circuit.

Referring to Fig. 1, MOS based charge re-distribution SAR A/D converter has an inherent sample and hold function in which the analog input signal is connected to all the capacitors in the binary array during the first clock cycle of a N-bit conversion process. Although there are several different ways by which sampling could be carried out, it was decided to go in for inherent sampling with a charge scaling DAC as shown in Fig. 1 to

avoid any extra sampling circuits. The DAC architecture was chosen based upon this reason of inherent sampling and for layout efficiency. More detailed explanation towards DAC will be provided in 2.2.2. Sampling will take place during the first clock cycle. The type of the switching circuits, its resistances and absolute values of the capacitors in the binary array along with the parasitic capacitors determine the above mentioned performance metrics in this type of A/D converter.

2.2.2. DIGITAL TO ANALOG CONVERTERS

A digital-to-analog converter (DAC) receives a digital code at the input and generates an analog output signals equivalent to the digital code. The analog voltage generated could be anywhere from 0 to V_{ref} where V_{ref} is the reference voltage. The reference could also be current or charge as well depending upon the architecture. The output voltage of the DAC can be expressed as

$$V_{out} = V_{ref} * (\sum_{b=0}^{N-1} D_b * 2^{-b}) \quad (1)$$

where V_{ref} is the reference voltage, N is the number of bits in this DAC which is also equal to the number of bits of the A/D converter, D_b is the b_{th} bit of the digital code. The summing term in the equation represents the binaryweighting produced by the division of the reference voltage. The accuracy with which the DAC works determine the linearity of this A/D converter [1].

Some of the important performance metrics of a DAC are described below.

- Differential Non-Linearity (DNL) is the maximum deviation in the output, step size from the ideal value of one least significant bit (LSB).

From Fig. 6, it is difference between the obtained and expected quantization levels divided by the expected quantization level.

$$DNL = \frac{Obtained\ Quantization\ Level - Expected\ Quantization\ Level}{Expected\ Quantization\ Level} \quad (2)$$

- Integral Non-Linearity (INL) is the maximum deviation of the input/output characteristic from a straight line passed through its end points. The summation of DNL also gives INL profile.

$$INL = \sum_{0}^{N-1} DNL \quad (3)$$

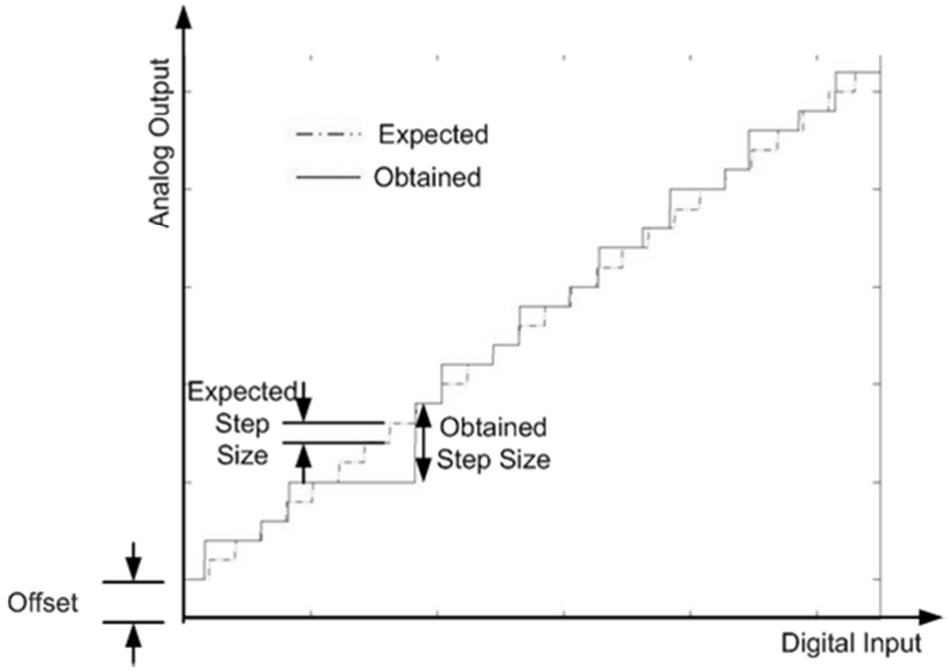

Fig. 6 Static Parameters of D/A Converters

- Offset is the vertical intercept of the straight line passed through the end points.

- Gain error is the deviation of the slope of the line passed throught the end points from its ideal value (usually unity).
- Settling time is the time required for the output to experience full-scale transition and settle within a specified error band around its final value.
- Signal to noise and distortion ratio (SNDR) is the ratio of the signal power to the total noise and harmonic distortion at the output when the input is a (digital) sinusoid.

There are many different types of DAC architectures such as voltage scaling, current scaling, charge scaling etc. All these parallel DAC architectures which produce the output analog voltage in a single clock cycle. There are also many configurations of a serial DAC which takes N clock cycles for a N-bit DAC. But in SAR ADCs where the binary search is carried out, usually parallel DACs are used in order to finish one complete conversion process within N clock cycles.

Fig. 7 illustrates a current-scaling architecture, also called binary-weighted resistor DAC [31]. For an N-bit converter, it requires N switches and N resistors sized in binary array. The binary-weighted currents generated by the resistors are directed to the op amp according to the state of the switches. Those bits asserted with a "1", will have their corresponding switch set to the reference voltage V_{ref} and the current through it will flow through the feedback resistor R_f. The bits containing a "0" will have their corresponding switch set to ground potential, preventing any flow of current through them.

The main advantage of the current-scaling architecture is that it is insensitive to parasitic capacitors and, hence, can provide faster conversion rates [31]. Disadvantages

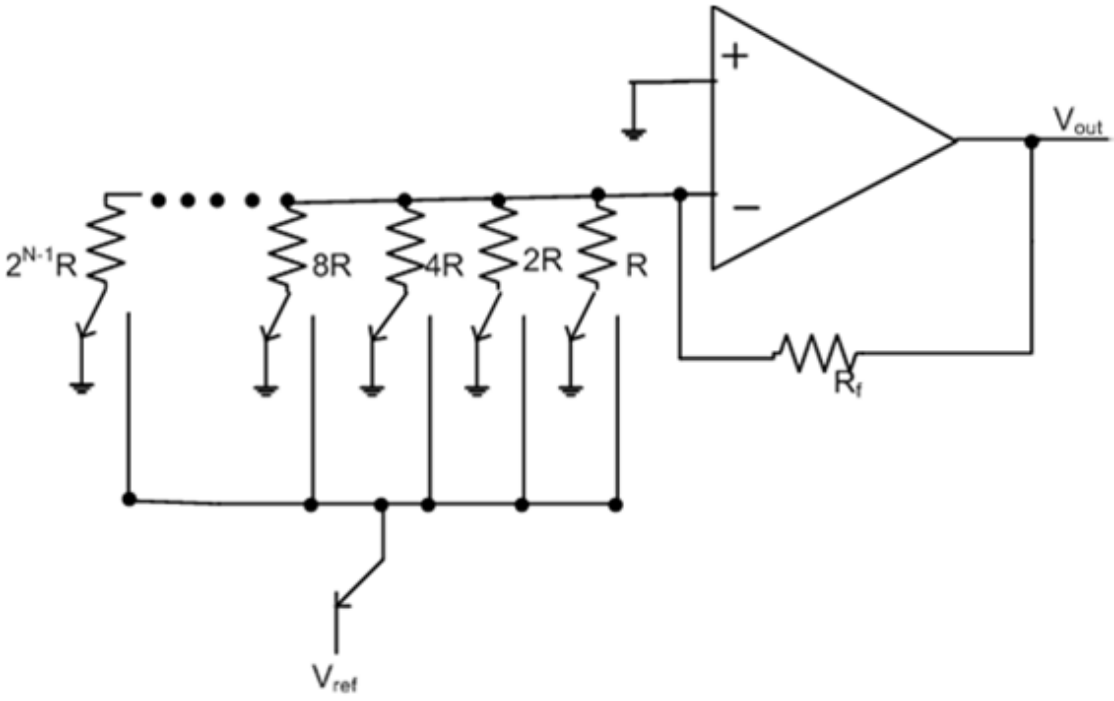

Fig. 7 Current Scaling D/A Converter

include the required area and poor matching of resistors that limit the resolution below 10 bits. When higher resolution is needed, an alternative R-2R circuit solution requiring less area is shown in Fig. 8.

The voltage-scaling DAC converts the digital input code into an analog output by scaling the reference voltage into a set of N node voltages. The basic configuration is shown in Fig. 9, consists of a resistor string and a series of switches. These switches are controlled by the digital input and the output represents the analog estimate of the input code. The main advantage of this architecture is the guaranteed monotonicity. Its main disadvantage is the large number of resistors and switches required, limiting the resolution to about 6-bits and the speed will also be much lower in this architecture.

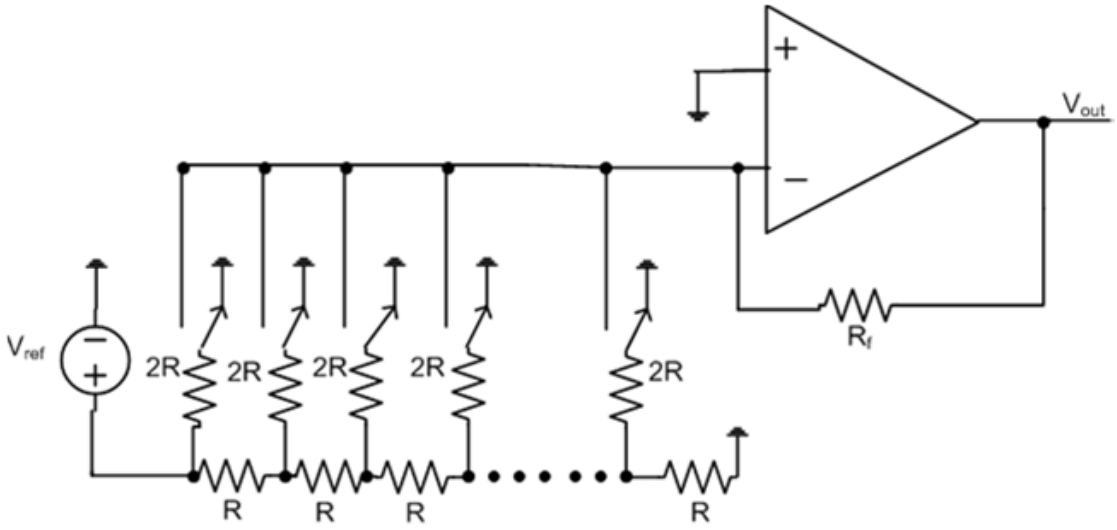

Fig. 8 R-2R Resistor Ladder D/A Converter

The charge-scaling method consists of a capacitor array with a combination of switches that distributes the circuit's total charge among the capacitors. The basic architecture used with this method is shown in Fig. 10. The operation of the circuit is controlled by a clock. During the positive phase the bottom-plate of the capacitors are connected to ground through the switches, allowing them to discharge.

During the negative phase, the digital input code will control to what potential the switches will be connected. For a bit containing a "1" the switch's terminal will be connected to the reference voltage V_{ref} and for a bit containing a "0" the switch's terminal will remain connected to ground. The equivalent of the digital code will be the sum of the charge distributed through those capacitors connected to V_{ref}. When used as a standalone unit, the DAC requires an output buffer to prevent the discharge of the unit capacitor due to resistive loads. Similar to the binary-weighted resistor DAC, the accuracy of this DAC is limited by the precision of the passive components. A careful design must be followed

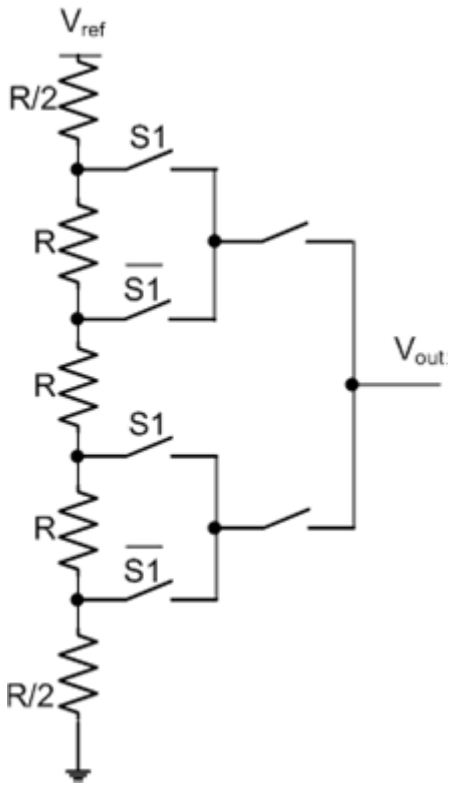

Fig. 9 2-Bit Voltage Scaling D/A Converter

so that the capacitors are correctly sized with respect to the parasitic capacitances.

This kind of charge scaling DAC architecture is chosen to implement self-calibration/digital trimming SAR A/D converter in this dissertation for the above mentioned reason in 2.2.1. For the architectures described thus far, the primary factor limiting their resolution is the precision of its passive components. For current CMOS technologies, the maximum resolution is around 10 bits. Since the accuracy of these DACs depends on the ratio of the largest to smallest component, a means to increase the resolution without a significant increase in area must be followed.

One of the techniques available to reduce the required area of these passive

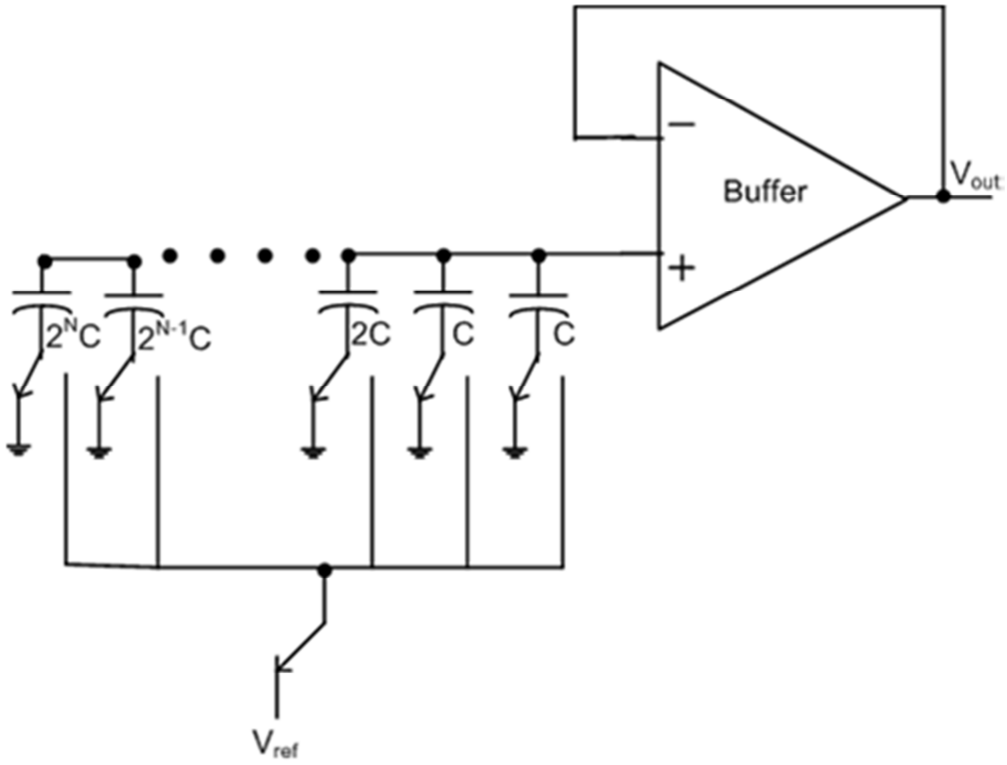

Fig. 10 Charge Scaling D/A Converter

components is to go in for segmented DAC approach. In this approach, there will be two DACs operation in parallel, one of them would be A-bit DAC and the other would be B-bit DAC. In combination, they would act as though there is an (A+B)-bit DAC. One of the subDACs would be used to process the A most significant bits (MSBs) and the other subDAC would be used to operate the B least significant bits (LSBs). They would operate simulataneously to provide a single analog equivalent output corresponding to the input digital code. A block diagram illustrating this technique is shown in Fig. 11. First, the output of the LSB subDAC is scaled by a factor of $1/2^A$. Then, the scaled output is added to that of the MSB sub-DAC.

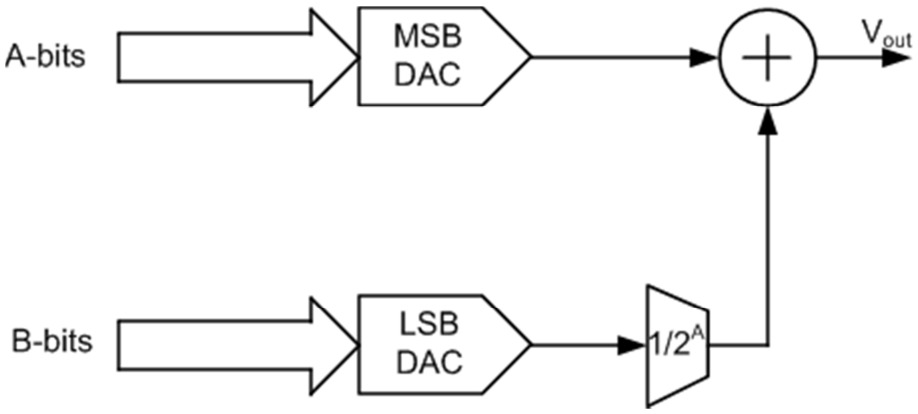

Fig. 11 Segmented DAC Approach

A similar technique used for increasing DAC resolution consists on scaling the voltage reference of the LSB subDAC instead of scaling its output voltage by 2^A. Again, the output of an A-bit subDAC is combined with the output of a B-bit subDAC to represent the converted analog output of the complete DAC.

An example of a DAC implemented using scaled output voltages is shown in Fig. 12. Here, an 4-bit charge scaling DAC was formed from the combination of two 2-bit subDACs. This is done through capacitor C_S, which scales the output voltage of the LSB subDAC and produce the least-significant-bit for the MSB subDAC. The series addition of the scaling capacitor, C_S and the effective capacitance of the LSB subDAC, must terminate the MSB subDAC and, hence, be almost equal to the unit capacitor C. It should be noted that C_s affects both the LSB and MSB subDACs because it acts as a termination capacitor for the MSB DAC [31]. An approach similar to the one described above can be followed using current scaling or voltage-scaling methods.

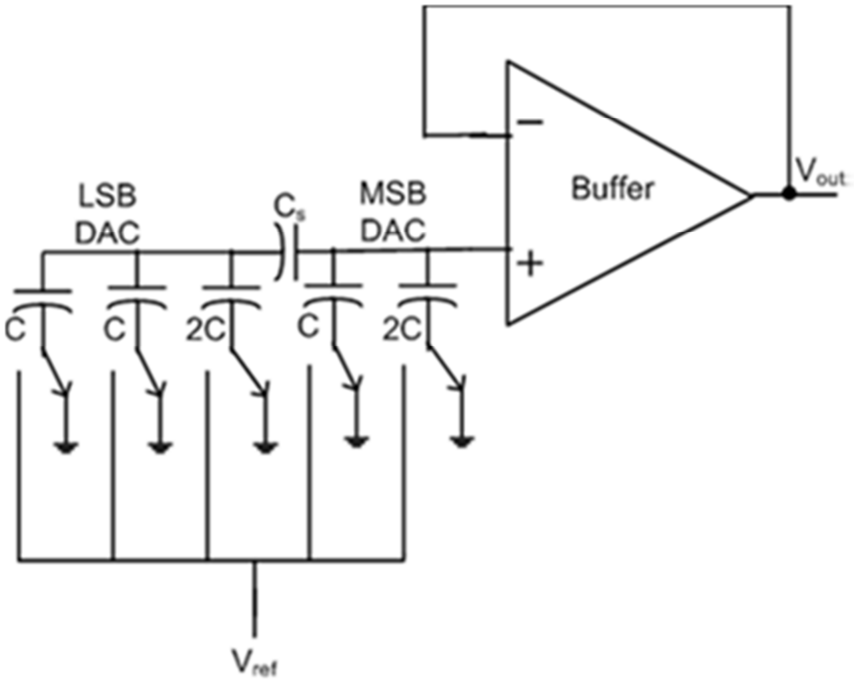

Fig. 12 4-Bit Charge Scaling DAC Composed of Two 2-Bit DACs

2.2.3. COMPARATORS

A comparator is a module whose function is to compare the analog signals present in the inputs. Depending on the polarity of the differential input, the logic output would be produced. As it is the case with several types of ADCs, usually one of the comparator's input is connected to a constant potential or reference. When the analog voltage present in the positive input terminal (V_A) of the comparator is greater than the analog voltage present in the negative input terminal (V_B), a logic high (V_{OH}) output would be produced. When the voltage present in the negative input terminal (V_B) is greater, then logic low (V_{OL}) output would be produced.

The transfer function of the ideal non-inverting comparator is shown in Fig. 13.

Some of the important performance metrics of a comparator are described below.

- Resolution is the minimum input difference that yields a correct digital output. It is limited by the input-referred offset and noise of both the preamplifier and the latch.
- Comparison rate is the maximum clock frequency at which the comparator can recover from a full-scale overdrive and correctly respond to the next subsequent 1-LSB input. This rate is limited by the recovery time of the preamplifier as well as the regeneration time constant of the latch.

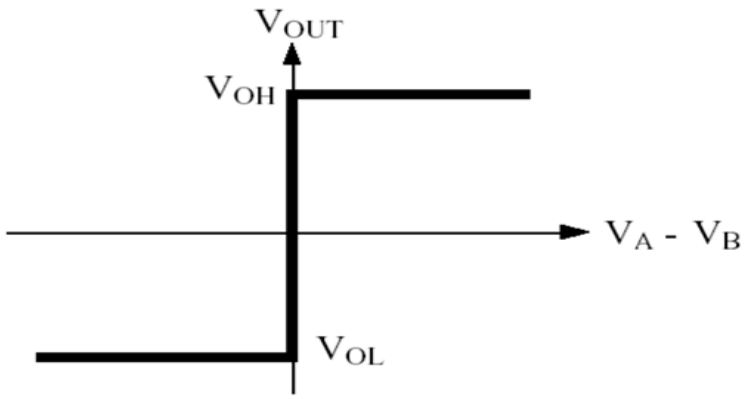

Fig. 13 Ideal Comparator Transfer Function

- Dynamic range is the ratio of the maximum input swing to the minimum resolvable input.
- Kickback noise is the power of the transient noise observed at the comparator input due to switching of the amplifier and the latch.
- Input referred offset is the V_{OUT} reflected back to the input when V_A is physically connected to V_B.

- Gain of the comparator in the open loop mode is the ratio of the difference between the logic high (V_{OH}) and logic low (V_{OL}) to the smallest resolution of the comparator.
- Slew Rate is a large-signal behavior that sets the maximum rate of the output voltage change. It is limited by the output driving capability of the comparator. The propagation delay is inversely proportional to the difference in the input voltage applied. This means that applying a larger input voltage will improve the propagation delay, up to the limits set by the slew rate.

Comparators can be classified as open-loop comparators and regenerative (positive feedback) comparators. The main difference resides on whether or not feedback is applied to the op amp used. To obtain the benefits offered by both types of comparators, many configurations have been developed that employ a combination of open-loop stages with regenerative stages that uses positive-feedback.

An open-loop comparator is an operational amplifier designed to operate with its output saturated, close to the supply rails, based on the polarity of the applied differential input. The op-amp does not employ the use of feedback and hence no compensation is required to achieve stability in the system. This doesn't pose a serious problem since the linear operation is of no interest in comparator design. The main advantage of not compensating the op amp is that it can be designed to obtain the largest possible bandwidth, thereby improving its time response.

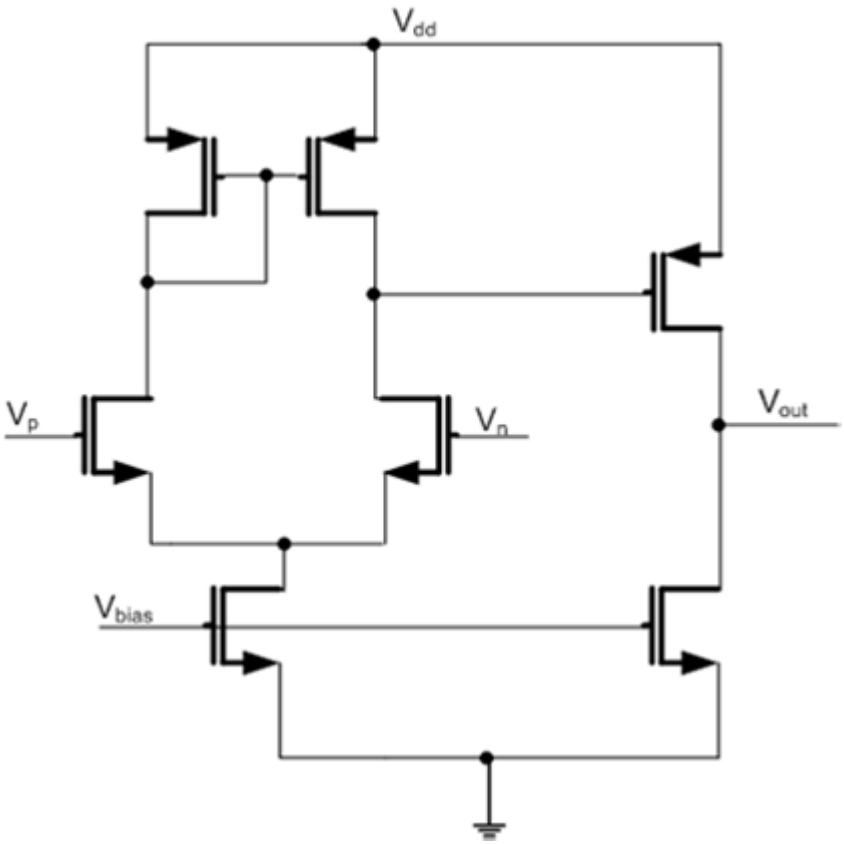

Fig. 14 Two Stage Open Loop Comparator

Fig. 14 illustrates a circuit example of an open-loop comparator. It is based on the commonly used two-stage op amp. The first stage is a NMOS input differential-pair with PMOS transistors M4 and M5 acting as a diode-connected active load. The NMOS tail transistor present in the first stage acts as a current sink and is used to bias the input pair. The output stage is a current sink inverter.

The main advantage of open-loop comparators is that, if enough gain is provided, the minimum detectable differential input can be very small. It would be reasonable to think that by simply designing the comparator with the largest possible gain, an almost infinite resolution can be achieved. However, increasing the gain also reduces the bandwidth of

op amps. This means that although the resolution will improve, the time response of the comparator will degrade. Thus, a trade off between speed and resolution must be made. The absolute maximum resolution of open-loop comparators is limited by input-referred noise and the offset voltage present in the op amp used.

Unlike open-loop comparators, regenerative comparators make use of positive feedback to realize the comparison between the two signals.They operate with a clock that divides the operation of the circuit into two phases. During the first phase the comparator tracks the input and during the second phase the positive feedback is enabled. Depending on the polarity of the input, one of the latch's output will go high and the other will go down.

The basic principle of regeneration consists in employing a latch circuit. Shown in Fig. 15, the latch employs a positive feedback through the cross-coupled connection of the PMOS transistors. One of the advantages of using positive feedback is that the time response can be very fast thanks to the positive exponential transfer characteristic of the latch. However, due to mismatches present in the transistors, the resulting offset voltage limits the maximum resolution achievable with this circuit. In order for the latch to operate in the exponential region of its transfer characteristic, the minimum resolvable input must be large enough to overcome the large offset voltage, typically in the range from 30 to 100 mV.

It was described above that the gain required to achieve a high resolution resulted in a comparator with a large delay. The use of a latch comparator would provide a very fast

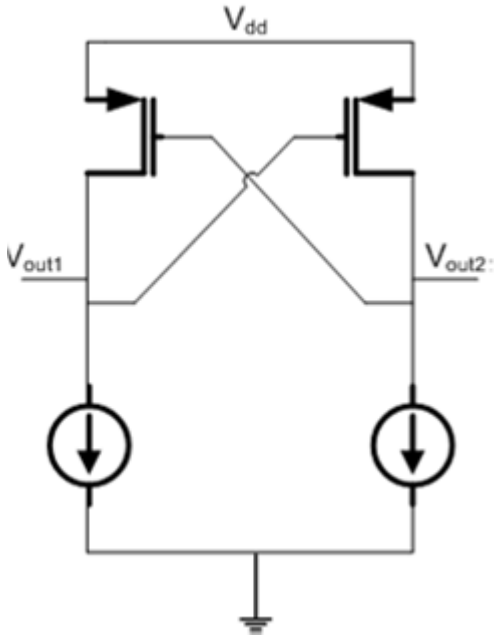

Fig. 15 Basic Latch Using PMOS Transistors

time response, but only for large input differences due to its input offset voltage. The optimal solution that allows to reach a trade-off between resolution and speed consists of combining a pre-amplifier and a latch. The gain needed by the preamplifier will depend on how large is the offset voltage produced by the latch circuit. The idea is to provide enough linear amplification so that the difference seen at the latch input is large enough for the latter to work in the exponential region of its input/output characteristic. Since the combination of a pre-amplifier and a latch provides both speed and resolution, only these types of comparators will be discussed from here on.

The offset voltage present in the comparators limits their resolution. Although the offsets resulting from matching errors can be reduced through the use of layout techniques such as common-centroid, those errors produced by random process variations

needed different techniques. One way to partially eliminate such type of offset errors is by using offset cancellation techniques [32].

There are two offset cancellation techniques, namely Input Offset Storage (IOS) cancellation technique and Output Offset Storage (OOS) cancellation technique. Each has its own advantages and disadvantages and they are discussed below.

The input offset storage scheme is illustrated in Fig. 16. The comparator makes use of switches and capacitors to store the offset voltage present at its input. Circuit operation is divided into two phases. During the first phase, φ1, the offset present in the preamplifier and latch is stored in capacitors C_1 and C_2. This is done by configuring the preamplifier in unity feedback mode with switches S_1 through S_4. In the second phase, φ2, the above mentioned switches are opened while switches S_5 and S_6 are closed. The input signal is connected to the comparator's input, allowing the latter to perform the comparison. This last phase must also allow the latch to be strobed in order to sense the amplified output provided by the preamplifier. Under this scheme, the preamplifier must be stable when configured in the unity-feedback configuration. As a result, it becomes necessary to employ compensation techniques for pre-amplifiers.

In the input offset storage technique, there will be three types of offset components. They are preamplifier's offset reflected to its input (V_{OFF}), the charge injected by switches S_3 and S_4, and the latch's input offset as seen at the comparator's input ($V_{OFF(latch)}$) [33]. Of these offset components, only the one introduced by charge injection is not reduced. An expression for the final offset after cancellation is given by

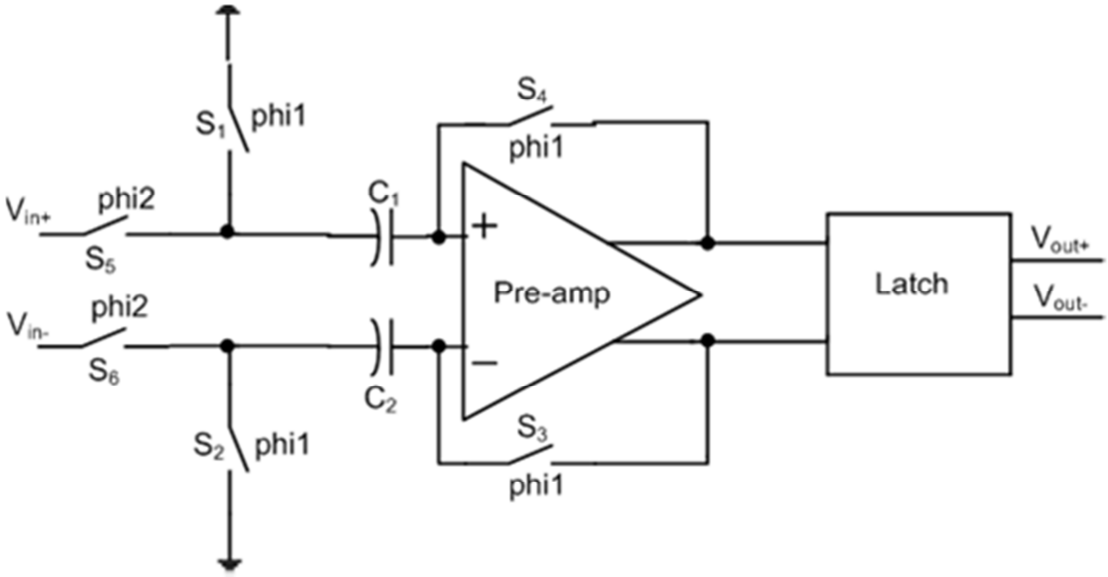

Fig. 16 Input Offset Storage Technique

$$V_{OFF(final)} = \frac{V_{OFF}}{1+A_O} + \frac{\Delta q}{C} + \frac{V_{OFF(latch)}}{A_O} \qquad (4)$$

Attractive features of the Input offset storage cancellation technique are rail-to-rail input common-mode range and the improved overdrive recovery provided by the unity-gain feedback. The most important disadvantage is the kT/C noise, produced by the input sampling capacitors, that will disturb the input signal during the preamplification mode. Increasing the size of these capacitors to minimize the noise will lead to a slower circuit time response. Another disadvantage is the need for compensation in the preamplifier; needed for stable operation under the unity-feedback configuration.

The output offset storage cancellation technique is shown in Fig. 17. It works in a similar fashion to the input offset cancellation technique. The main difference is that in neither of the two clock phases the preamplifier operates in unity-feedback mode. During

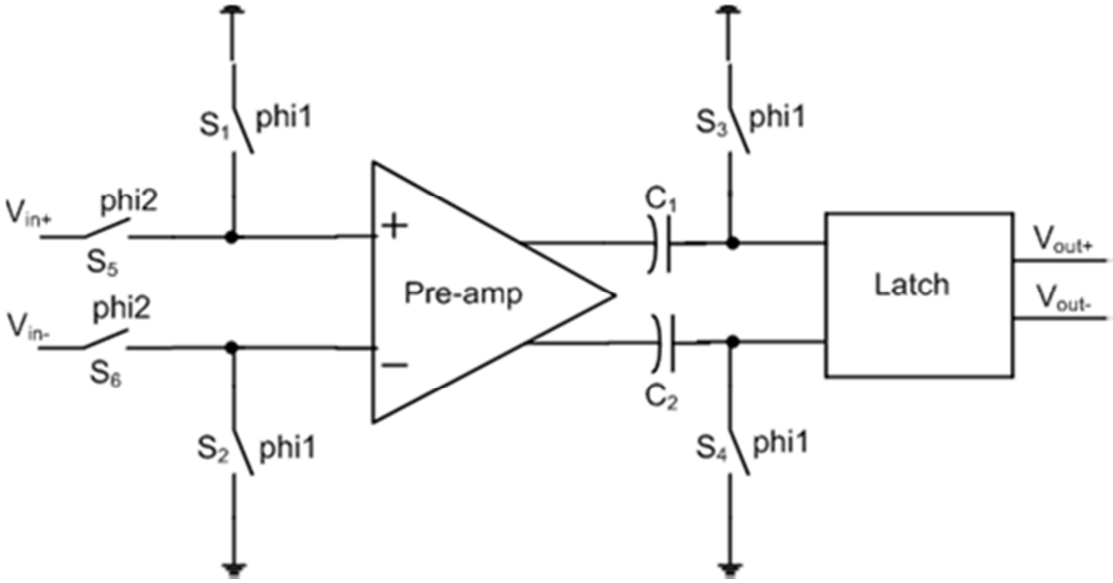

Fig. 17 Output Offset Storage Technique

phase φ1, the MOS switches connected to ground are "on" and the offset is stored in the capacitors. During phase φ2 these switches are "off" and input is connected to the comparator allowing comparisons to be made. As in the previous scheme, this last phase must allow the comparator to fully resolve the input difference.

For the Output Offset Storage cancellation technique, there will be two types of offsets that are produced. They are charge injection of switches S_3 and S_4 and the latch offset [32]. As the sampling capacitors are located at the preamplifier's output, the offset voltage of the latter is completely canceled when reflected to the input. The final expression for the total offset remaining after cancellation can be written as

$$V_{OFF(final)} = \frac{\Delta q}{A_O C} + \frac{V_{OFF(latch)}}{A_O} \qquad (5)$$

The main advantages of the Output Offset Storage cancellation technique over Input Offset Storage cancellation technique are the complete cancellation of the preamplifier's offset, the reduction in offset due to charge injection, and the lower input capacitance due to the placement of the sampling capacitors at the preamplifier's output. A disadvantage of OOS is the limited input common-mode range due to the DC coupling that need to be present for biasing the input transistor of the pre-amplifier. Moreover, the open-loop configuration in the preamplifier requires a lower gain to avoid saturating the preamplifier if a large offset voltage is present.

3 CONVENTIONAL SAR-ADC CALIBRATION AND TRIMMING

3.1 INTRODUCTION

There are various methods that were used previously to implement calibration and trimming procedure within a Successive Approximation Analog to Digital Converter. This is done to eliminate the mismatches between the binarily weighted capacitor array to get a highly linear transfer function.

3.2 CONVENTIONAL METHODS:

The architecture of a conventional on-board self-calibration procedure using a memory for storing the errors occurring in each capacitor of the main array and correcting it through an extra error correction sub-CDAC is shown in Fig. 18 [23]. The error in each capacitor is measured as follows. In the case of finding the mismatch of capacitor 16C, a set of lower capacitors 8C, 4C, 2C, C and C are sampled to V_{ref} while the top plate switch S_0 is grounded. This will store a known charge on the top plate node. Then the bottom plate of capacitor 16C is tied to V_{ref} while the top plate switch S_0 is open and other capacitors are grounded. The exact point at which the comparator output changes sign is found by connecting bottom plates of the capacitors in the sub-CDAC array one by one to V_{ref}. This is the point at which the charge stored on the lower set of capacitors 8C, 4C, 2C, C and C gets neutralized by the charge stored on mismatched capacitor 16C together with the sub-CDAC achieving binary relationship. Once the error corresponding to capacitor 16C is stored in the memory, the errors of other higher

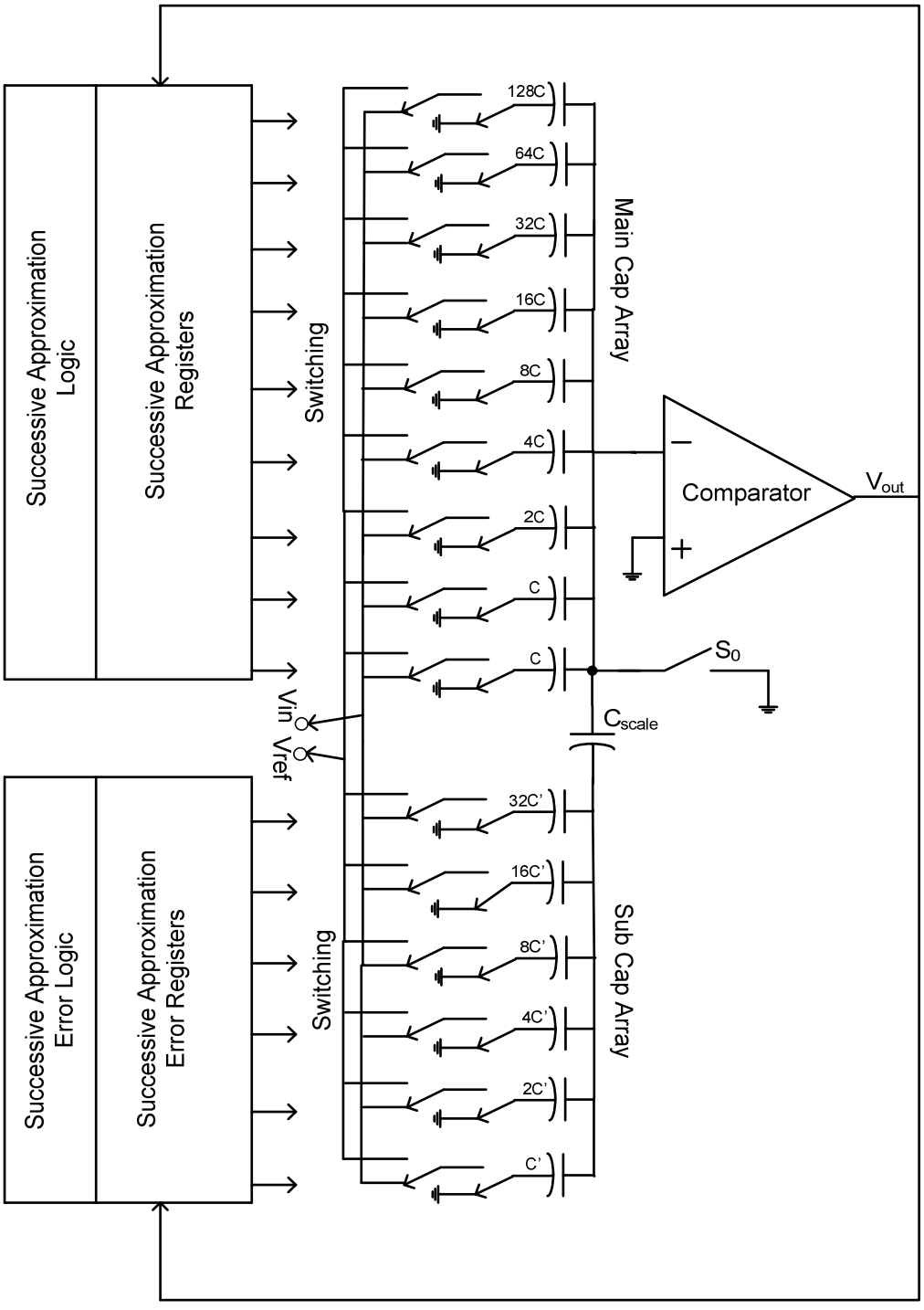

Fig. 18 Self-Calibration Using Memory and Extra Sub-CDAC

capacitances 32C, 64C and 128C are similarly found and stored accordingly. After this calibration mode, during normal ADC conversion process, whenever these MSB capacitors 16C, 32C, 64C and 128C are made to toggle from *Gnd* to V_{ref}, the trim capacitors associated with each of these capacitors, which are calculated as described above are also toggled from *Gnd* to V_{ref} using sub-CDAC array to maintain the binary relationship between the capacitors. In this way, the calibration and trimming is done using physical trim capacitors. Another work [27] explains a way of correcting mismatches through physical trim capacitors. In this work, multiple trim capacitors were used for each individual primary capacitor in the main array. The errors associated with each primary capacitor could be found during the final test and the errors are stored to program the trim capacitors as the way in which it is required for binary matching.

The programmed trim capacitors toggle in the same manner as the primary capacitor in the main CDAC array. This method is shown intuitively in Fig. 19.

Yet another work [35] describes one way of digital trimming algorithm in which the exact value of the errors associated with each and every capacitor are stored with exact decimal accuracy in the memory. During normal conversion, whenever a capacitor is decided to be connected to V_{ref}, its exact absolute value gets added in the accumulator and the decimal part of the accumulated value is made to adjust the residual capacitors throughout the conversion process. At the end of the conversion process, the integer part of the digitally accumulated value is given out as the final result. This is shown in Fig. 20.

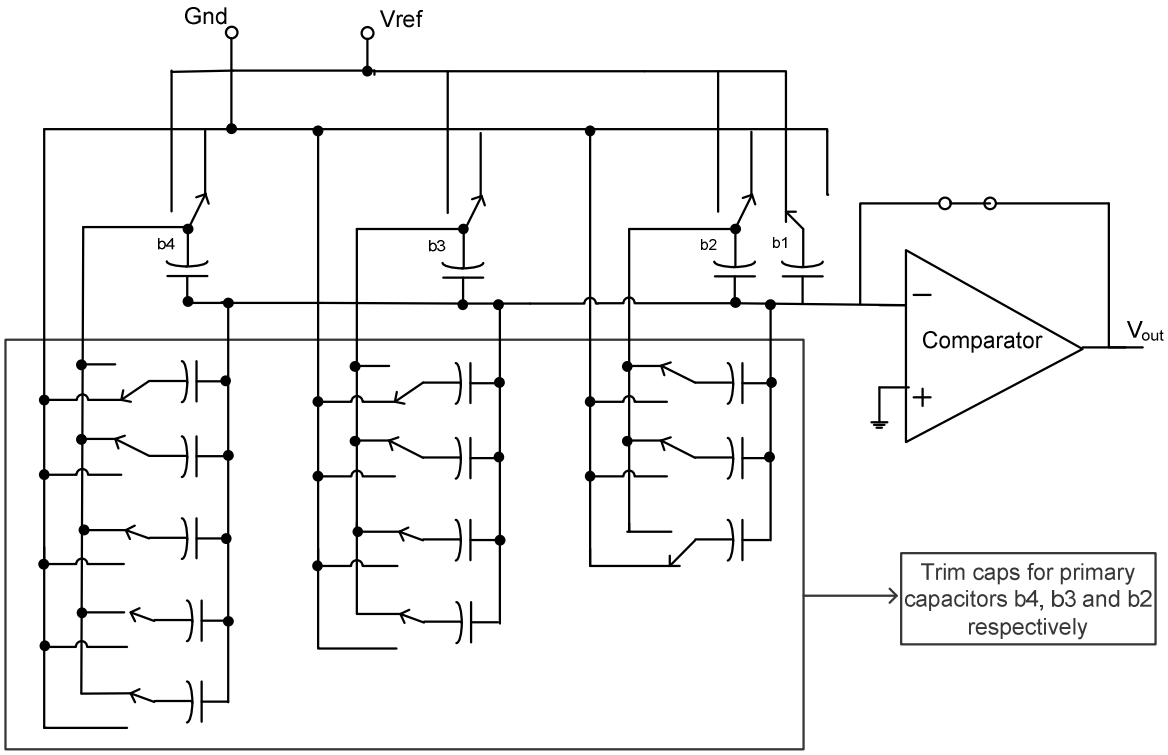

Fig. 19 Physical Trim Capacitors for Separate Primary Capacitors in the Array

In [24], each capacitor in the main array requires an individual calibration capacitor and calibration voltages are generated by resistive DACs which again increases area. Implementation in [28] involves extra switching sequences for cancelling the errors in the capacitors, reducing throughput. Another technique proposed in [36] collects 200,000 samples using two independent half-sized ADCs driving a least mean square feedback loop in order to calibrate the CDAC, thereby trying to achieve convergence in the calibration algorithm. This takes a lot of time in calibrating the mismatches. There are also a number of other derived techniques [17],[25],[26],[37] to calibrate the mismatches in the capacitors, which either occupies extra area or extra time. In this paper, an efficient

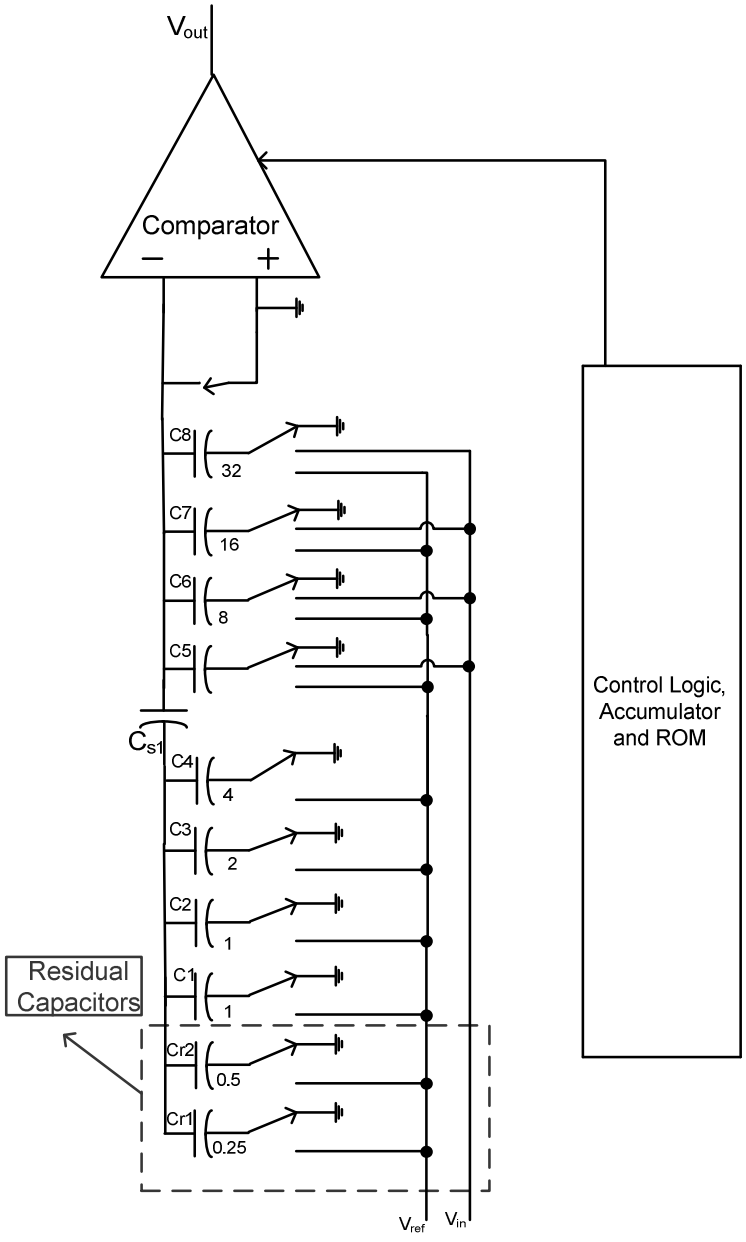

Fig. 20 Digitally Corrected SAR Converter Including a Correction DAC

self-calibration and digital trimming algorithm is proposed which does not take any area for implementing trim capacitors, does not reduce throughput and takes almost negligible in calibrating the mismatches.

4 PROPOSED SELF-CALIBRATION AND DIGITAL-TRIMMING ALGORITHM

The algorithm is implemented with the help of dynamic error correction capacitors explained in 4.1. Section 4.2 introduces the actual self-calibration. A novel method to cancel out the charge injection based offset error due to hold switch, is explained in 4.3. Section 4.4 introduces two different methods of digital trimming algorithm.

4.1 DYNAMIC ERROR CORRECTION

Dynamic error correction helps in achieving redundancy during SAR ADC operation. There are different techniques to achieve redundancy as explained in [8],[18],[21],[29]. Among them, [8],[29] uses non-binary capacitor array implementation which is not effective in a monolithic implementation with different capacitor dimensions which is difficult to implement and will not match properly. A general architecture for the proposed 14-bit CDAC with Dynamic Error Correction is shown in Fig. 21. There are two extra capacitor next to normal bit-6 capacitors which are called $b_{6down\text{-}p}$ and $b_{6up\text{-}p}$ on the P-side and $b_{6down\text{-}n}$ and $b_{6up\text{-}n}$ on the N-side. These two capacitors on both P-side and N-side are employed for differential dynamic error correction purpose and it has the same value as normal bit-6 capacitor (256 LSBs).

Similarly, there are two extra capacitors next to normal bit-12 capacitor which are called $b_{12down\text{-}p}$ and $b_{12up\text{-}p}$ on the P-side and $b_{12down\text{-}n}$ and $b_{12up\text{-}n}$ on the N-side. These two capacitors on both P-side and N-side are employed for differential dynamic error correction purposes and it has the same value as normal bit-12 capacitor (4 LSBs).

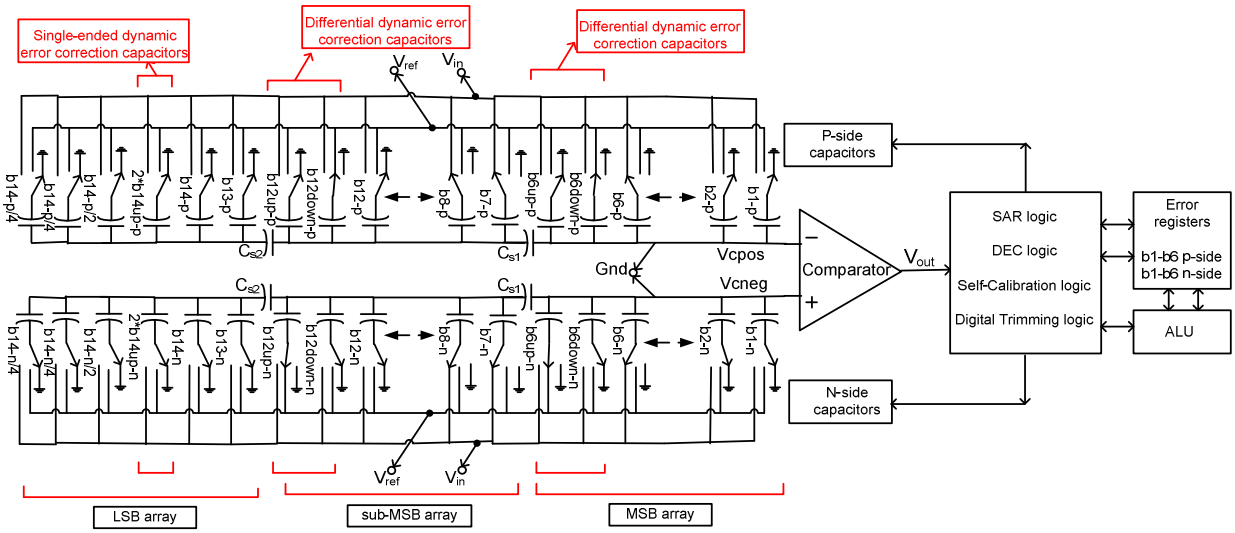

Fig. 21 14-Bit CDAC Architecture with Dynamic Error Correction

On the same lines, there is one extra capacitor next to normal bit-14 capacitor which is called b_{14up}. This capacitor on both P-side and N-side are employed for single-ended dynamic error correction purpose and it has twice the value as normal bit-14 capacitor (2 LSBs). This error correction procedure is explained in [18],[19].

The ideal values of the capacitors for a 14-bit converter configuration are shown below. Differential dynamic error correction at bit-6, bit-12 and a single-ended dynamic error correction at bit-14 capacitor values are underlined.

pcaps=[8192 4096 2048 1024 512 256 <u>256</u> <u>256</u> 128 64 32 16 8 4 <u>4</u> <u>4</u> 2 1 <u>2</u> 0.5 0.25 0.25];

ncaps=[8192 4096 2048 1024 512 256 <u>256</u> <u>256</u> 128 64 32 16 8 4 <u>4</u> <u>4</u> 2 1 <u>2</u> 0.5 0.25 0.25];

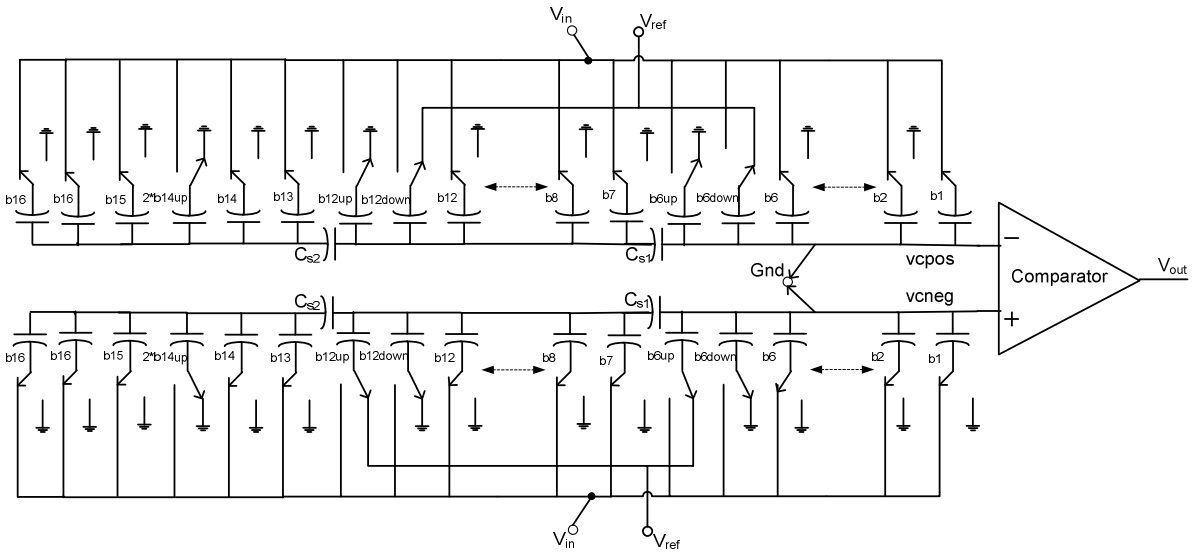

Fig. 22 Sampling Phase Configuration

Fig. 22 exactly shows the position of switches during sampling phase. In the sampling phase, the top plates of all the capacitors in the MSB array on both CDACs are grounded. Bottom plates of certain capacitors on both P-side CDAC and N-side CDAC sample V_{inp} and V_{inn} respectively. The number of capacitors used for sampling is dependent on the following gain equation stated in (6)38. This also decides the gain of the ADC [38]. Typically, the inputs are sampled on

$$C_{samp} = \frac{V_{ref} \cdot C_T}{V_{inp} - V_{inn}} \qquad (6)$$

where Csamp is the total sampling capacitance and CT in the sum of all capacitances on either P-side or N-side.

Zero power sampling technique shown in Fig. 23 is adopted where phi1 represents the conversion phase of ADC and phi2 represents the sampling phase. The bulk of high-voltage boosted sampling NMOS is switched to avoid back-gate effect during sampling

and in low-voltage top plate hold switch to avoid leakage when the top plate node goes below *Gnd* during conversion cycles.

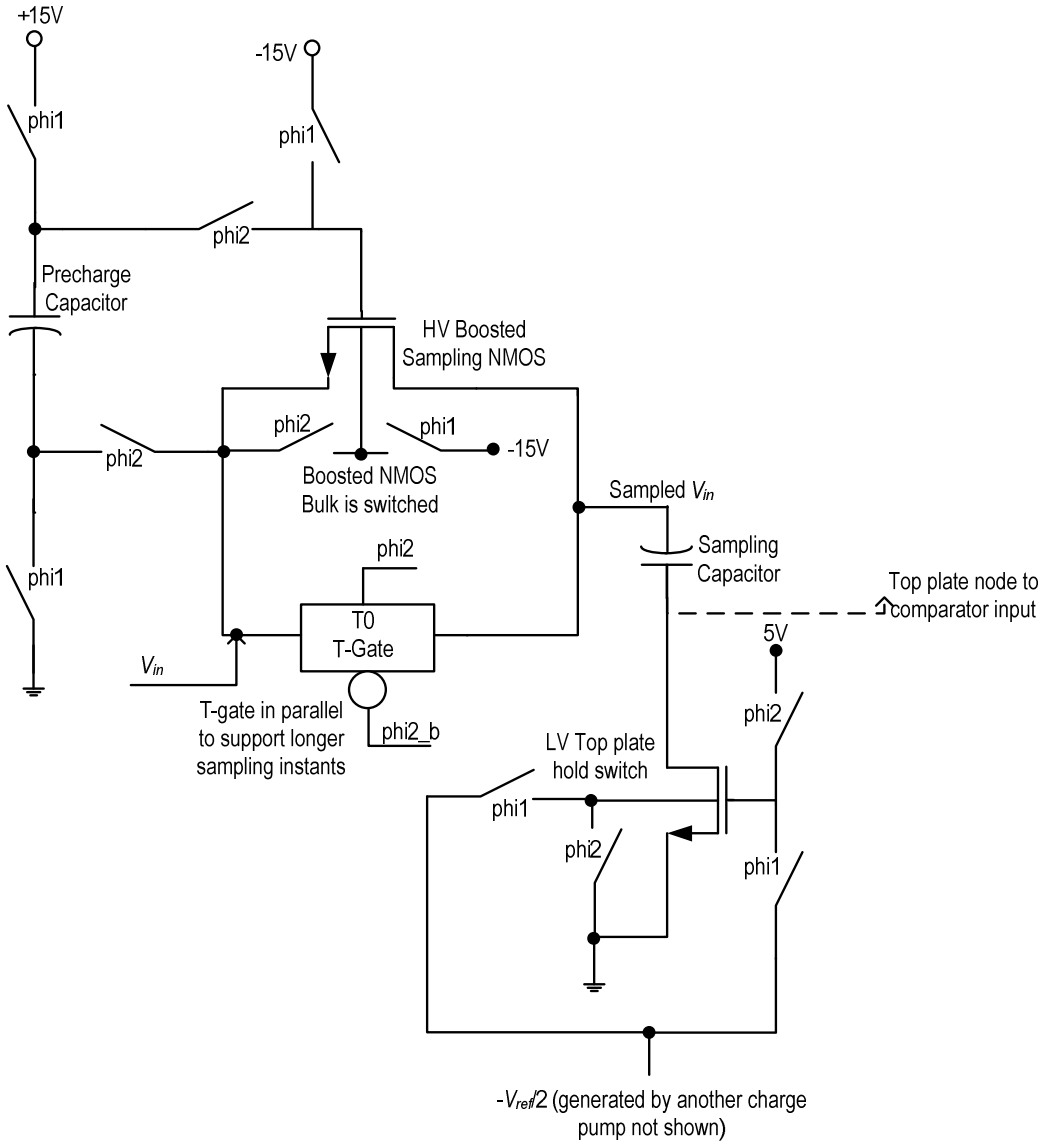

Fig. 23 Zero Power Sampling Technique Adopted in High Voltage Input SAR-ADC for All Sampling Capacitors

In the case of differential error correction on bit-6 and bit-12, one of the error correction capacitors is sampling *Gnd* and the other one sampling V_{ref}. Here in this Fig.

22, $b_{6down\text{-}p}$ and $b_{6up\text{-}n}$ are sampling V_{ref} and $b_{6up\text{-}p}$ and $b_{6down\text{-}n}$ are sampling *Gnd* respectively. Similarly, in the bit-12 error correction capacitors, $b_{12down\text{-}p}$ and $b_{12up\text{-}n}$ are sampling V_{ref} and $b_{12up\text{-}p}$ and $b_{12down\text{-}n}$ are sampling *Gnd* respectively. In the case of single-ended error correction on bit-14, the bottom plate of this error correction capacitor $2*b_{14up}$ is sampling the *Gnd*. During conversion, the main aim is to achieve convergence between V_{cpos} and V_{cneg} which are the two inputs of the comparator.

Once the input is sampled, the top plates of the capacitors in the MSB array is disconnected from *Gnd*. The inputs are then disconnected from the bottom plates and a typical SAR conversion is done from b_1 to b_6.

The V_{cpos}, V_{cneg} could vary anywhere depending upon the input voltage V_{in} sampled. At any point during the conversion process, the difference or the residue between V_{cpos} and V_{cneg} should be equal to or less than 2 times of its corresponding test weight. The main aim is to make V_{cpos} and V_{cneg} converging to less than 1-LSB at the end of conversion. If there is a dynamic settling error during switching of a particular bit weight in the middle of a conversion process, then it wouldn't converge to less than 2 times of its corresponding test weight, because of which dynamic error correction is done.

During multiple clock cycles in a conversion phase, V_{cpos} and V_{cneg} could attain any voltage value depending on the input voltage V_{in} equivalent to sampled $V_{inp} - V_{inn}$. At any given clock cycle of a conversion process, the maximum difference between V_{cpos} and V_{cneg} should be less than or equal to two times of its corresponding bit-test weight, i.e assume at the end of 6^{th} clock cycle in which bit-6 capacitor is tested, the difference of

voltages between V_{cpos} and V_{cneg} should be less than or equal to two times b_6 weight as stated in (7) as long as the input is within the specified range

$$V_{cpos} - V_{cneg} <= 2.\frac{b_6}{C_T}.V_{ref} \quad (7)$$

This condition is checked using either differential or single-ended dynamic error correction capacitors and it ensures that, at the end of conversion process, V_{cpos} and V_{cneg} would converge to less than 1-LSB. If this condition is met, dynamic error did not occur and all the MSB capacitors are completely settled during the conversion process. And if this condition is not met, it means that dynamic error exists and the MSB capacitors are not settled. Dynamic error correction capacitors add or subtract voltages to V_{cpos} and V_{cneg} to achieve convergence within 1-LSB. This is later accounted digitally in a dynamic error correction process.

Fig. 24, Fig. 25 and Fig. 26 explains the differential dynamic error correction in detail. In this explanation, it is assumed that the differential dynamic error correction capacitors are placed between the b_6 and b_7 capacitors and above the scale-down capacitor. The value of the differential dynamic error correction capacitor is equal to normal b_6 capacitor. In Fig. 24 on the top side, it is assumed that V_{cneg} is greater than V_{cpos} during b_5 testing. During b_6 testing, $b_{6\text{-}p}$ capacitor on the p-side is brought up from *Gnd* to V_{ref} while the $b_{5\text{-}n}$ capacitor on n-side is brought down from V_{ref} to *Gnd* and $b_{6\text{-}n}$ capacitor is brought up from *Gnd* to V_{ref}. Equivalently, there is an addition of b_6 weight on the p-side in V_{cpos} node while there is a subtraction of b_6 weight on the n-side in V_{cneg} node.

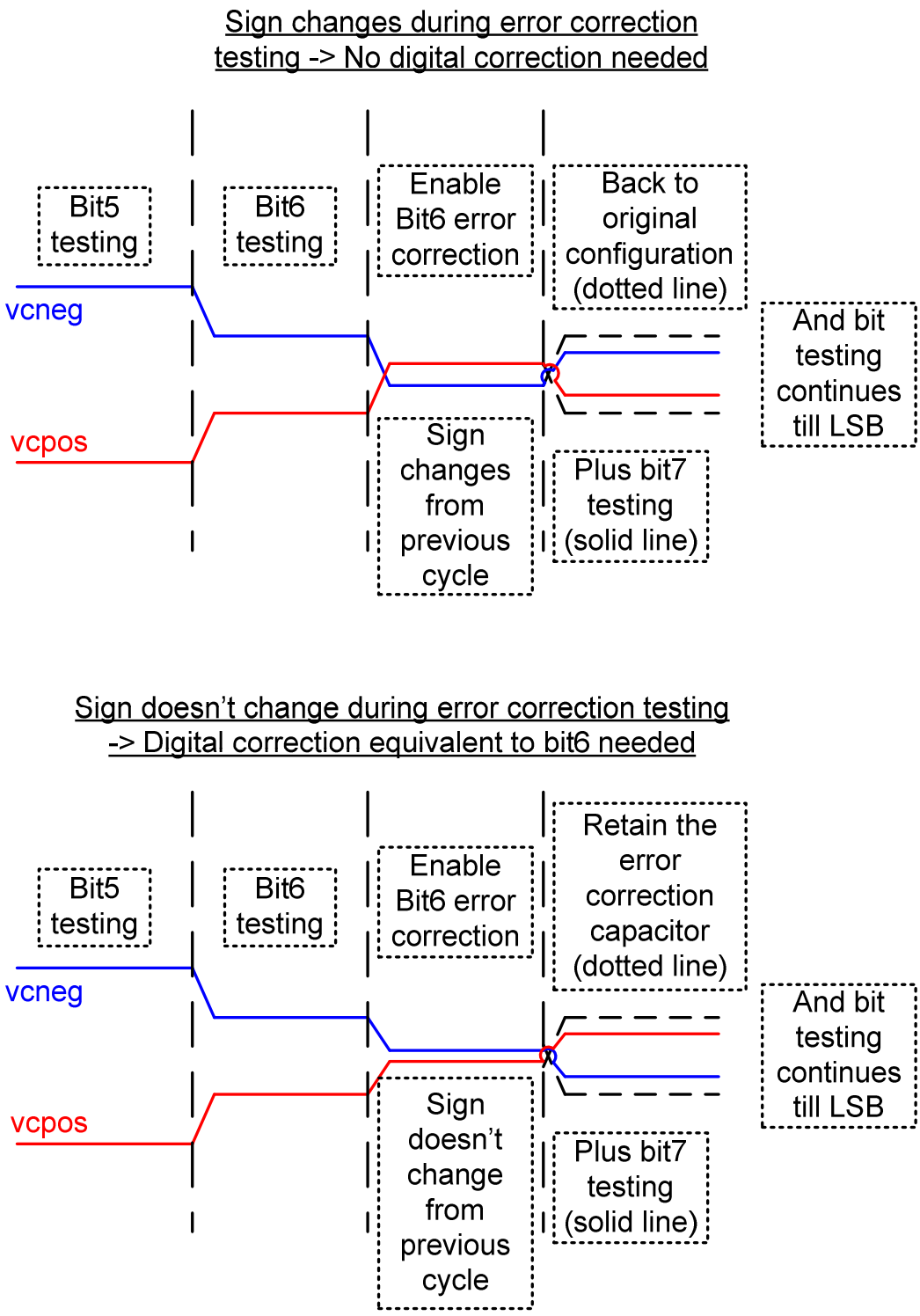

Fig. 24 Conceptual Diagram - Differential DEC Up-Transition

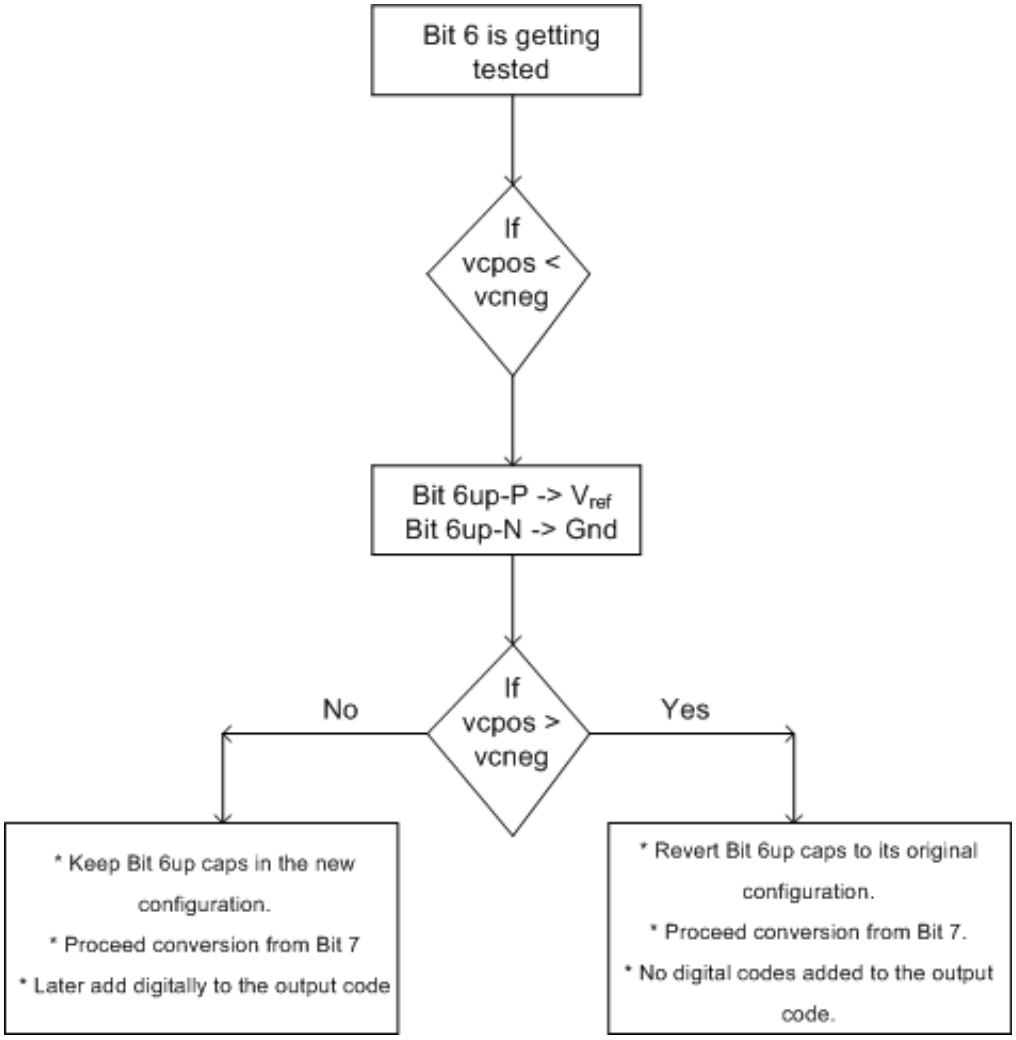

Fig. 25 Flow Chart for Checking Up-Transition in DEC

Since V_{cneg} is greater V_{cpos} during b_6 testing, dynamic error correction need to be performed by increasing the weight of V_{cpos} to another b_6 weight by switching the bottom plate of $b_{6up\text{-}p}$ on p-side from *Gnd* to V_{ref} and decreasing the weight of V_{cneg} to the same amount by switching the bottom plate of $b_{6up\text{-}n}$ from V_{ref} to *Gnd*. If the signs changes, then it means that V_{cpos} was closer to V_{cneg} by less than 2 times the corresponding b_6 weight at the end of normal b_6 testing. So we can be sure that V_{cpos} and V_{cneg} would converge to less

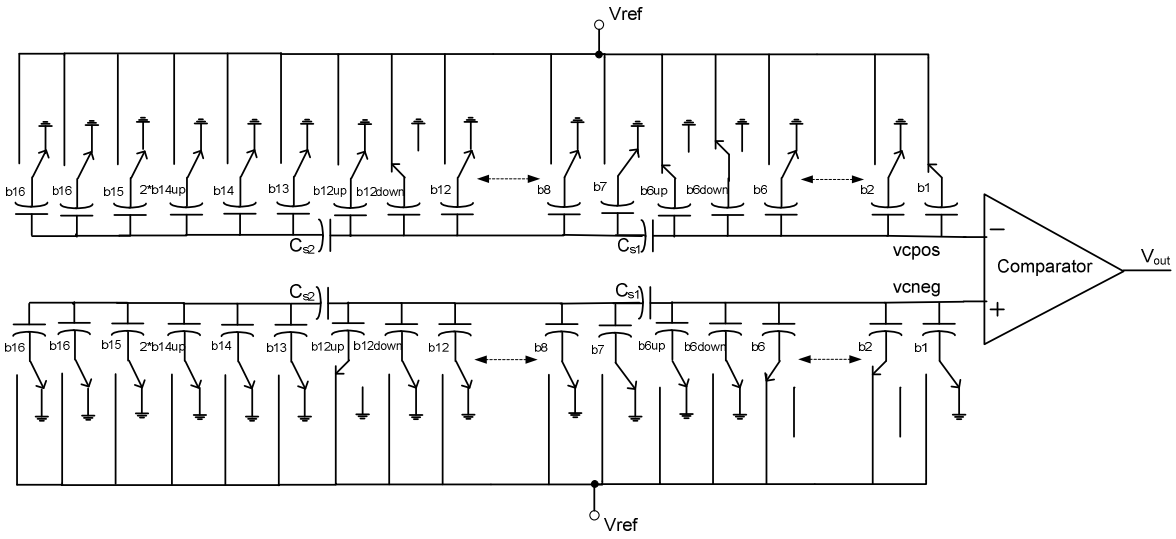

Fig. 26 Up-Transition Checking

than 1-LSB at the end of conversion. The differential dynamic error correction capacitors could be switched to its original default position before going ahead with b_7 testing and so on as shown on the top side of Fig. 24.

Else, as shown on the bottom side of Fig. 24, if the sign does not change during b_6 error correction cycle, then it means that V_{cpos} was away from V_{cneg} by more than 2 times the corresponding b_6 weight at the end of normal b_6 testing. This shows that the MSB capacitors have not settled causing dynamic errors. So there is a possibility that V_{cpos} and V_{cneg} would not converge to less than 1-LSB at the end of SAR conversion. So the differential dynamic error correction capacitors are retained in the same way as it was switched during error correction cycle till the end of SAR Conversion. The amount of charge added by the differentail dynamic error correction capacitors in analog domain is equivalently subtracted in digital domain. This helps in achieving convergence between

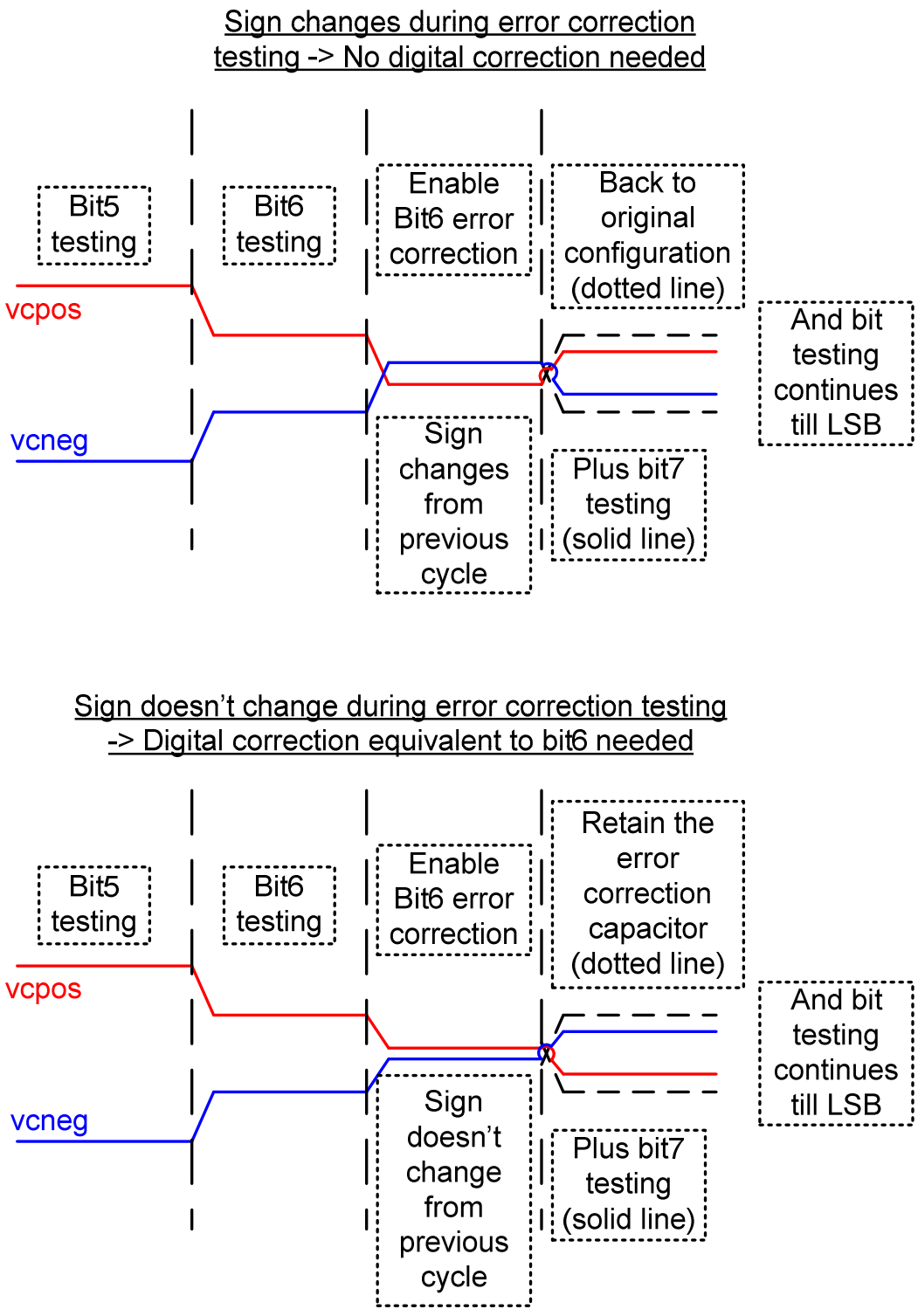

Fig. 27 Conceptual Diagram - Differential DEC Down-Transition

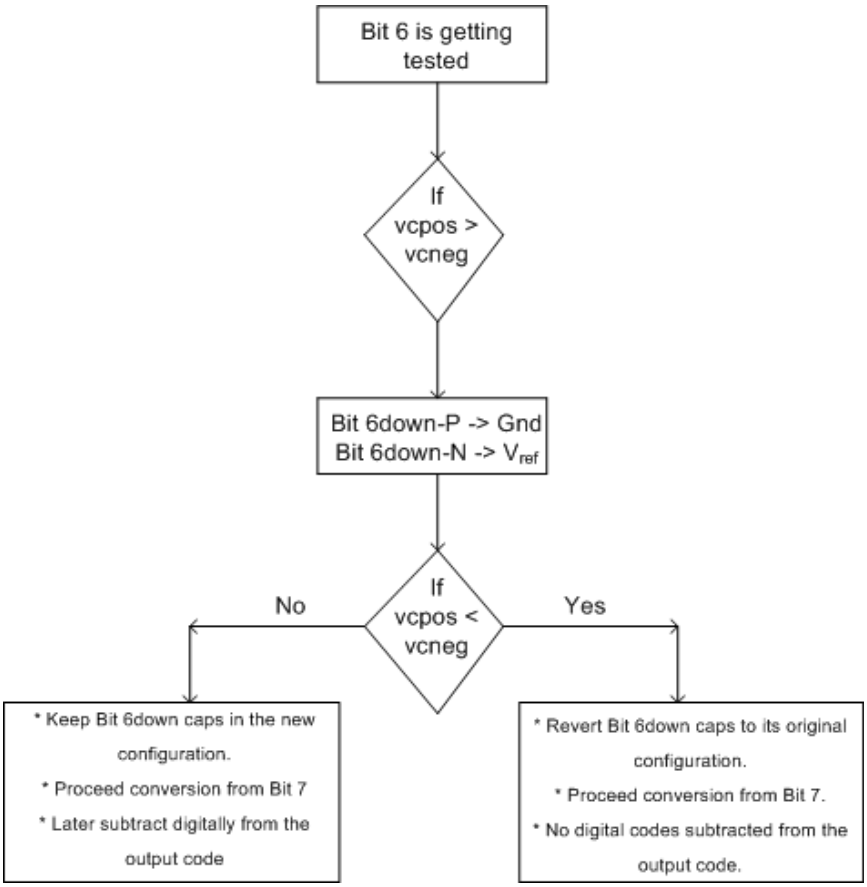

Fig. 28 Flow Chart for Checking Down-Transition in DEC

V_{cpos} and V_{cneg} easily. This also helps in bit-cycling the SAR capacitors at the pretty fast rate achieving higher speed in high precision converters.

Fig. 25 shows the block diagram of the above mentioned procedure in the case of up-transition where the V_{cpos} is less than V_{cneg} during the start of b_6 error correction cycle. Fig. 26 shows the location to which the bottom plates of the capacitors need to be connected during b_6 error correction cycle if V_{cpos} is less than V_{cneg} at the end of b_6 testing.

Similarly, Fig. 27 shows the node voltages of V_{cpos} and V_{cneg} during b_5, b_6 and b_6 error correction cycle for the case in which V_{cpos} is greater than V_{cneg} at the end of b_6 testing.

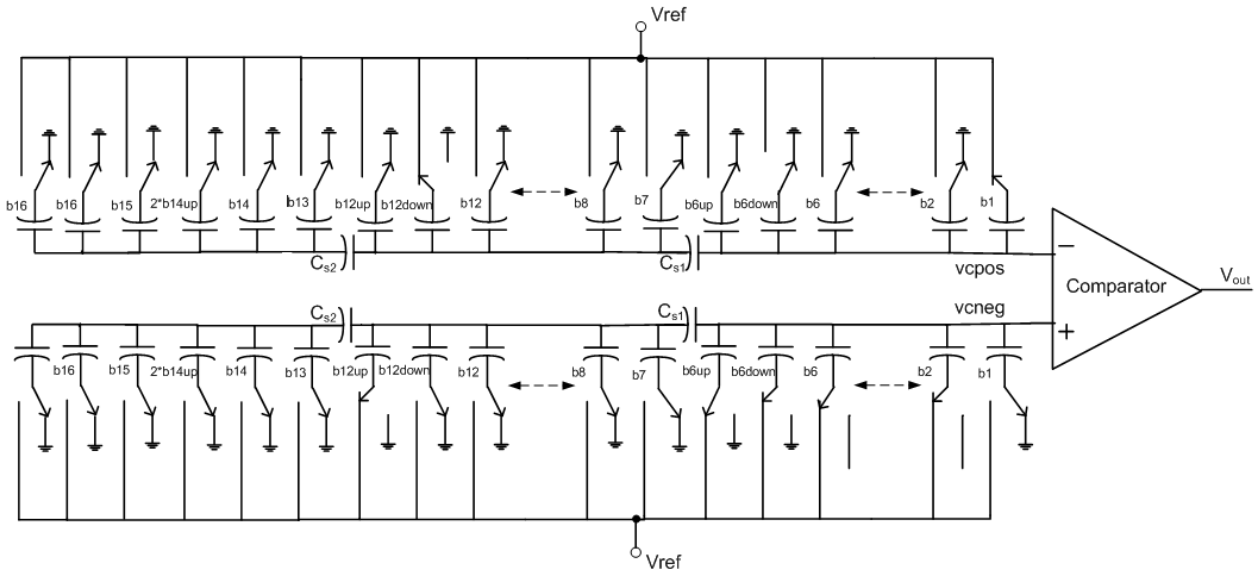

Fig. 29 Down-Transition Checking

So we need to check dynamic errors for down-transition in this case. Also Fig. 28 shows the block diagram of the procedure to check for dynamic error correction and Fig. 29 shows the location to which the bottom plates of the capacitors need to be connected during b_6 error correction cycle if V_{cpos} is greater than V_{cneg} at the end of b_6 testing.

Fig. 30 summarizes the DEC operation for both up and down transition at bit-6.

4.2 Built-In Self Calibration Algorithm

The architecture for the proposed built-in self-calibration algorithm is shown in Fig. 31. In this segmented, differential CDAC architecture, it is assumed that the first scale-down capacitor is placed between b_6 and b_7 capacitors and the second scale-down capacitor is placed between b_{12} and b_{13} capacitors. The first and second scale down capacitors separates the MSB array from the sub-MSB array and LSB array respectively. The scale down capacitor provides the capacitive division between the MSB array and sub-MSB

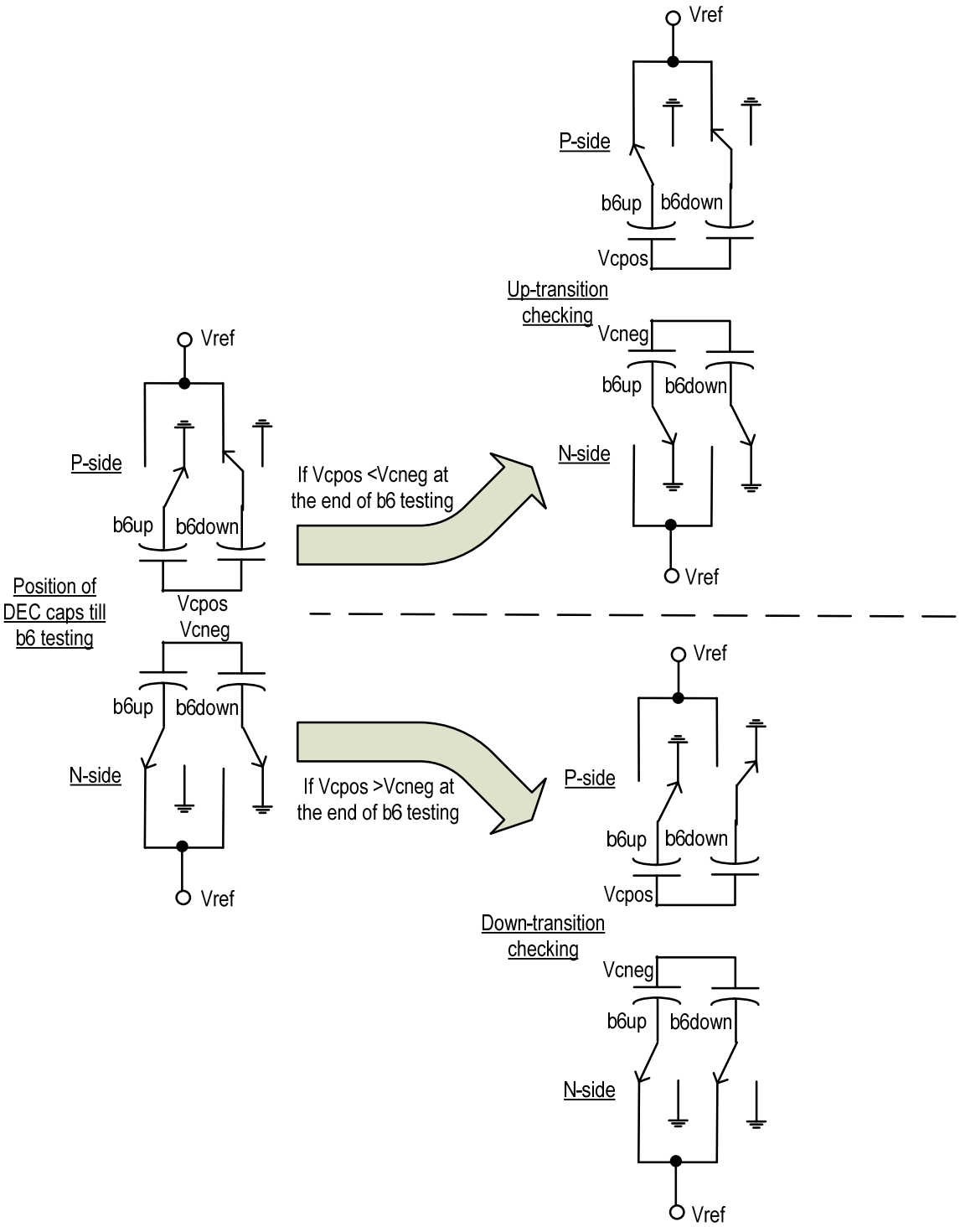

Fig. 30 DEC Operation at Bit-6 Position

array. Because of this capacitive division, the scale down capacitor decreases the sensitivity of the sub-MSB array and the LSB array. So the effect of mismatch between the capacitors in sub-MSB and LSB array would be lesser than the mismatch of the capacitors in the MSB array or between the mismatch of MSB-array capacitors with respect to sub-MSB array capacitors. Also the variation in the parasitic capacitor on the bottom plate of the first scale down capacitor causes an intrinsic mismatch between the MSB array and the sub-MSB array. This needs to be corrected either by trimming the first scale down capacitor or equivalently each of the capacitors from b_1 to b_6. Trimming of the scale down capacitor C_{s1} involves laser trimming techniques or more analog switches tied to the floating nodes which may lead to poor performance. Also trimming b_1-b_6 individual capacitors may be conventionally done by additional analog circuits as already discussed. As we see here, only the MSB array is trimmed.

In the proposed technique, a purely digital trimming approach completely eliminating the trim capacitors, is followed without using input voltage Vin, where the errors in each capacitor from b1-b6 can be found using self-calibration technique. The proposed method can correct for mismatches within an array and also between the P-side and N-side arrays in a fully differential CDAC since the errors will be found independently on both sides.

In this built-in self-calibration approach, the capacitor errors are found by first sampling bdown capacitor on the P-side (b6down-p) to Vref and the performing differential conversion from b7. The error of b6down-p is obtained by subtracting the ideal expected value from this conversion result.

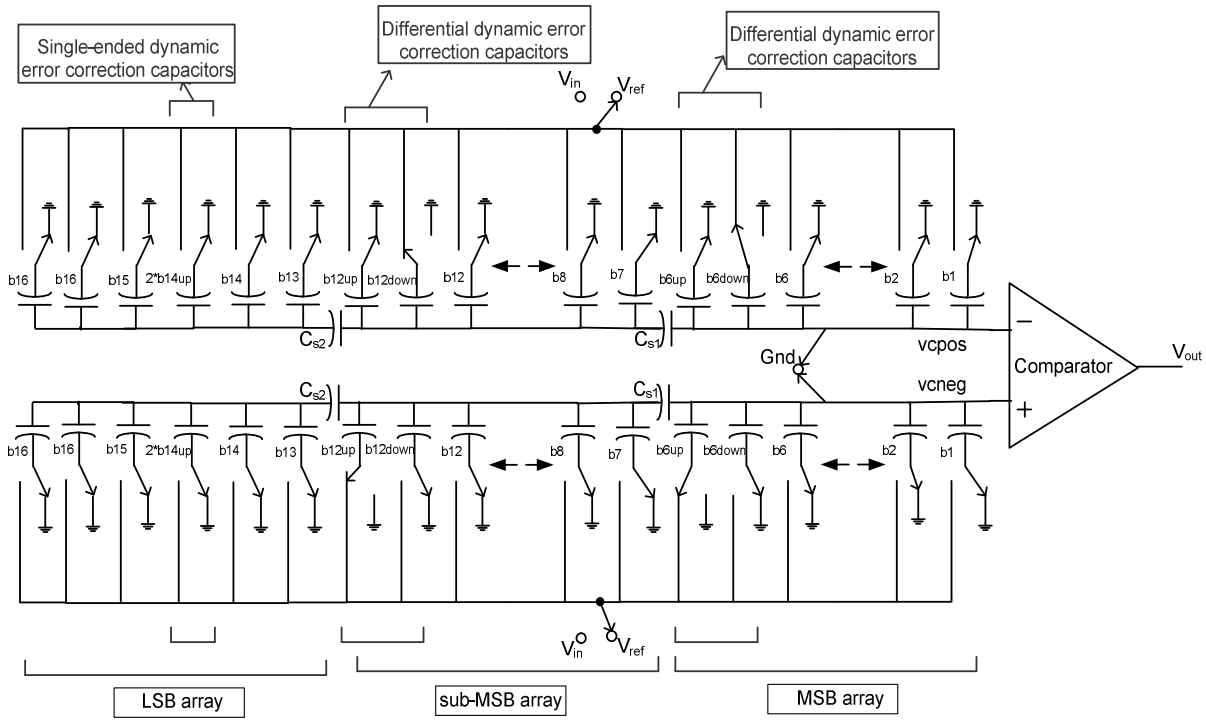

Fig. 31 Differential CDAC SAR A/D Architecture

The error obtained on $b_{6down\text{-}p}$ will be half the value of the original error because of the single-ended sampling (P-side alone) on a single capacitor but then doing a differential conversion. In contrast to the traditional easier techniques using physical trim capacitors in which single-ended sampling and single-ended conversion is performed [23],[27] or differential sampling and differential conversion is performed [23],[27] this technique eliminates physical trim capacitors and adopts the single-ended sampling independently on both P-side and N-side with differential conversion to account for the mismatches occurring in the bit capacitances between the P-side and N-side arrays. In addition, this technique also corrects the mismatches found between the binarily weighted capacitors within any array.

Similarly the errors of $b_{6up\text{-}p}$ and $b_{6\text{-}p}$ capacitors are found by sampling the respective capacitors followed by performing differential conversion from b_7 and then subtracting from its ideal value. Similarly the errors on $b_{5\text{-}p}$, $b_{4\text{-}p}$….$b_{1\text{-}p}$ capacitors are found by sampling each one of them separately and then performing differential conversion from b_6, b_5….b_2 respectively with dynamic correction employed at b_6, b_{12} and b_{14} positions followed by subtraction from its ideal expected values.

Dynamic error correction is employed in [18],[19] to reduce the settling errors during MSB cycles while the ADC is converting at full speed. In the proposed architecture, dynamic error correction is employed during self-calibration at positions b_6, b_{12} and b_{14} while measuring the errors of b_5, b_4….b_1 so that even if these capacitors are mismatched by a large margin, up to the order of +/-261 LSBs (summation of b_6, b_{12} and b_{14} LSB values), the transfer function of DNL/INL vs Codes would result in less than 1-LSB. In a way, the DEC capacitors are also correcting static mismatches in this algorithm. In this way, the errors are calculated on P-side and N-side capacitors independently. Let the errors of capacitors $b_{1\text{-}p}$, $b_{2\text{-}p}$….$b_{6\text{-}p}$,$b_{6up\text{-}p}$, $b_{6down\text{-}p}$, $b_{1\text{-}n}$, $b_{2\text{-}n}$....$b_{6\text{-}n}$, $b_{6up\text{-}n}$ and $b_{6down\text{-}n}$ obtained in this step be $\varepsilon_{1\text{-}p}$, $\varepsilon_{2\text{-}p}$…. $\varepsilon_{6\text{-}p}$, $\varepsilon_{6up\text{-}p}$, $\varepsilon_{6down\text{-}p}$, $\varepsilon_{1\text{-}n}$, $\varepsilon_{2\text{-}n}$…. $\varepsilon_{6\text{-}n}$, $\varepsilon_{6up\text{-}n}$ and $\varepsilon_{6down\text{-}n}$.

The values of the $\varepsilon_{6\text{-}p}$, $\varepsilon_{6up\text{-}p}$, $\varepsilon_{6down\text{-}p}$, $\varepsilon_{6\text{-}n}$, $\varepsilon_{6up\text{-}n}$ and $\varepsilon_{6down\text{-}n}$ obtained in the previous self-calibration step are not modified. But the errors associated with other capacitors are modified when they come across dynamic error correction capacitors depending upon how these correction capacitors are used while doing conversion in the self-calibration

phase. The modifications that the capacitors on the P-side goes through while calculating

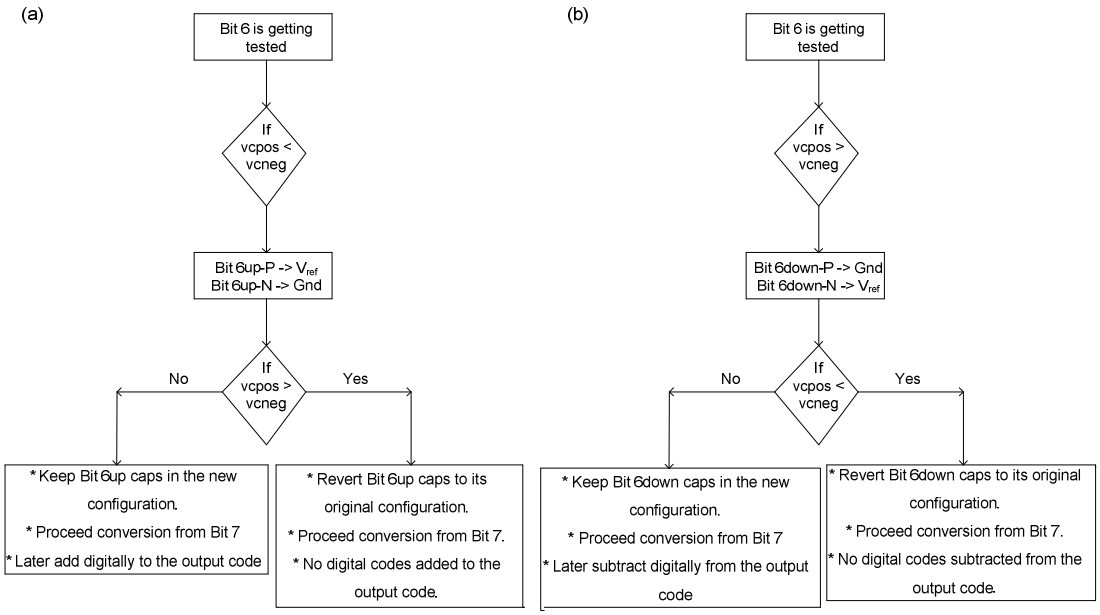

Fig. 32 (a) Differential DEC Flow-Chart for Up-Transition; (b) Differential DEC Flow-Chart for Down-Transition

$\varepsilon_{5\text{-}p}$ to $\varepsilon_{1\text{-}p}$ and the modifications that the capacitors on the N-side goes through while calculating $\varepsilon_{5\text{-}n}$ to $\varepsilon_{1\text{-}n}$ are respectively shown in Fig. 32 (a) and Fig. 32 (b). For example, during self-calibration, while finding the error associated with $b_{5\text{-}p}$, after initially sampling $b_{5\text{-}p}$ alone to V_{ref}, V_{cpos} in Fig. 31 would be less than V_{cneg}. Therefore dynamic error correction needs to be performed by switching $b_{6up\text{-}p}$ to V_{ref} and $b_{6up\text{-}n}$ to *Gnd* as shown in Fig. 32 (a) . Suppose if the sign changes, then add $\varepsilon_{6up\text{-}n}$ to the error of $b_{5\text{-}p}$ while calculating $\varepsilon_{5\text{-}p}$. Also retain $b_{6down\text{-}p}$ capacitor to *Gnd* and $b_{6down\text{-}n}$ to V_{ref}. Incase if the sign doesn't change, then add ideal value of b_6 and subtract $\varepsilon_{6up\text{-}p}$ from the error of $b_{5\text{-}p}$ while calculating $\varepsilon_{5\text{-}p}$. Similarly, the errors associated with $b_{4\text{-}p}$, $b_{3\text{-}p}$….$b_{1\text{-}p}$ are calculated based upon the flow chart shown in Fig. 32 (a). In the same way, the errors associated with $b_{5\text{-}n}$,

$b_{4\text{-}n}\ldots b_{1\text{-}n}$ are calculated based upon the flow chart shown in Fig. 32 (a). In the same way, when V_{cpos} in Fig. 31 would be greater than V_{cneg} during b_6 dynamic error correction, then flow chart in Fig. 32 (b) is followed.

In the previous step, it could be seen that the errors calculated on the $b_{5\text{-}p}$ is correct only based upon the assumption that b_6 capacitors are all perfect. But there could be a mismatch on the b_6 capacitors which needs to be considered. Similarly while calculating the errors associated with $b_{4\text{-}p}$, $b_{3\text{-}p}\ldots b_{1\text{-}p}$, it is assumed that all the lower capacitors are all accurate. But then in real scenario, the lower capacitors would also be mismatched. In order to compensate for this, a compensation factor needs to be added as follows. The final value of err5-p is obtained by adding the previous $\varepsilon_{5\text{-}p}$ with the $\varepsilon_{6\text{-}p}$ and $\varepsilon_{6down\text{-}p}$ as shown in equation (8) assuming that $\varepsilon_{6down\text{-}p}$ is always connected to V_{ref} during sampling and during initial conversion.

$$\varepsilon_{5-p}(final) = \varepsilon_{5-p}(previous) + \varepsilon_{6-p} + \varepsilon_{6down-p} \quad (8)$$

Similarly, final value of $\varepsilon_{4\text{-}p}$ is obtained by adding the previous $\varepsilon_{4\text{-}p}$ with $\varepsilon_{5\text{-}p}$, $\varepsilon_{6\text{-}p}$ and $\varepsilon_{6down\text{-}p}$ as shown in (9). The final value of $\varepsilon_{3\text{-}p}$ to $\varepsilon_{1\text{-}p}$ is computed in the same manner.

$$\varepsilon_{4-p}(final) = \varepsilon_{4-p}(previous) + \varepsilon_{5-p}(previous) + \varepsilon_{6-p} + \varepsilon_{6down-p} \quad (9)$$

For the case of $\varepsilon_{5\text{-}n}$, its final value is computed by adding the previous value of $\varepsilon_{5\text{-}n}$ with $\varepsilon_{6\text{-}n}$ and $\varepsilon_{6up\text{-}n}$ assuming $\varepsilon_{6up\text{-}n}$ is initially connected to V_{ref} during sampling and during initial conversion.

$$\varepsilon_{5-n}(final) = \varepsilon_{5-n}(previous) + \varepsilon_{6-n} + \varepsilon_{6up-n} \quad (10)$$

The final value of $\varepsilon_{4\text{-}n}$ to $\varepsilon_{1\text{-}n}$ is found using the same method.

$$\varepsilon_{4-n}(final) = \varepsilon_{4-n}(previous) + \varepsilon_{5-n}(previous) + \varepsilon_{6-n} + \varepsilon_{6up-n} \quad (11)$$

By doing so, an estimate of the errors occurring on the capacitors of both P-side and N-side from b_1 to b_6 is known during this self-calibration step. Once the estimate of errors is known for each capacitor above the scale-down during self-calibration step, it is stored in local registers.

4.3 Charge Injection Based Offset Error in Self-Calibration

During Self-Calibration, when each capacitor is individually calibrated from $b_{6down\text{-}p}$, $b_{6up\text{-}p}$, $b_{6\text{-}p}$….$b_{1\text{-}p}$ on the P-side and from $b_{6down\text{-}n}$, $b_{6up\text{-}n}$, $b_{6\text{-}n}$….$b_{1\text{-}n}$ on the N-side, errors occur due to charge injection of the hold switch. The amount of charge injection will be based on the impedance looking into the top plate of the calibrating capacitor which is different for different calibrating capacitor. For example as shown in Fig. 21, at the end of sampling phase in a self-calibration algorithm, when the hold switch opens, charge injection from the hold switch is different when $b_{6down\text{-}p}$ is sampled to V_{ref} than when $b_{1\text{-}p}$ is sampled. This creates offset error between different capacitors and may provide false correction value during calibration. So there should be a charge injection based offset cancellation that need to be performed for different capacitors while it is being calibrated.

This is usually done after self-calibration algorithm is completed. To cancel the offset provided by the charge injection of the hold switch during $b_{6down\text{-}p}$ sampling phase, $b_{6down\text{-}p}$ is sampled to V_{ref} on the bottom plate while the top plate is grounded. In the hold phase, top plate hold switch is opened while the bottom of $b_{6down\text{-}p}$ is still connected to V_{ref}. Next differential conversion is performed from b_7 to calculate the offset due to charge injection

of hold switch during $b_{6down\text{-}p}$ calibration. Similarly, offset due to charge injection of hold switch for different capacitors are found independently and stored. These values are subtracted from the errors of different capacitors found in self-calibration algorithm to calculate the exact mismatches in each capacitor.

4.4 DIGITAL TRIMMING

Once the estimate of errors is known for each capacitor above the scale-down during the self-calibration up-on power up, it is stored in local registers. During normal conversion, whenever a $b_{1\text{-}p}$ to $b_{6\text{-}p}$ is connected to V_{ref} on the positive side, the sum of the final errors computed for those bits on both positive and negative sides need to be added to the digital output got with incorrect physical capacitance. Also whenever a bit6 weight is subtracted, the $\varepsilon_{6down\text{-}p}$ and $\varepsilon_{6down\text{-}n}$ is also subtracted. In the same way, whenever a bit6 weight is added, the $\varepsilon_{6up\text{-}p}$ and $\varepsilon_{6up\text{-}n}$ is also added. Implementing all the four steps as stated above would ensure that the final error plot to be within +/-1 LSB.

Again, during normal conversion, the sum of the errors found on the positive and negative side could be added when a $b_{1\text{-}p}$ to $b_{6\text{-}p}$ is connected to V_{ref} on the positive side or the other option would be to add the errors found on the positive side alone whenever the decision is taken for those bits to be connected to V_{ref} and the errors found on the negative side could be subtracted when the corresponding capacitor on the positive side is decided to be connected to *Gnd*. Both the options work out to be fine and it could be proved mathematically as follows.

Let the reference voltage used in the circuit be V_{ref} and let $\Sigma C_{high,P}$ denotes the summation of all capacitors tied high on the P-side at the end of conversion, $\Sigma C_{high,N}$ denotes the summation of capacitors tied high on the N-side. If $C_{total,P}$ and $C_{total,N}$ denote the sum of all capacitors tied both high and low, then equation (10) is valid at the end of conversion.

If we assume that ΣdN_{high}, ΣdN_{low}, ΣdP_{high} and ΣdP_{low} denotes the delta errors due to mismatches occurred on the capacitors of N-side tied high, low and on P-side tied high, low at the end of conversion, then equation (12) is valid.

$$\frac{Vref * \sum ChighN}{CtotalN} = \frac{Vref * \sum ChighP - CtotalP * Vin}{CtotalP} \quad (12)$$

$$\frac{Vref * (\sum ChighN + \sum dNhigh)}{CtotalN} = \frac{Vref * (\sum ChighP + \sum dPhigh) - CtotalP * Vin}{CtotalP} \quad (13)$$

The relationship that describes the complimentary nature of $\Sigma C_{high,P}$ and $\Sigma C_{high,N}$ is

$$\frac{\sum ChighN}{CtotalN} = 1 - \frac{\sum ChighP}{CtotalP} \quad (14)$$

Since the two DACs are independent in terms of their actual capacitor values, it is possible to write it in terms of ratios.

$$\frac{\sum Chigh}{Ctotal} = \frac{Code}{FSCode} \quad (15)$$

where Code represents the equivalent digital output code for the capacitors tied high and *FSCode* represents the full scale output code. Also since both DACs have the same resolution, *FSCode* is same for both and the compliment between the digital equivalent of capacitors tied high on the positive side $Code_{,P}$ and the one on the negative side $Code_{,N}$ is described as

$$CodeN = FSCode - CodeP \tag{16}$$

$$\frac{Vref * \sum dNhigh}{CtotalN} + \frac{Vref * \sum ChighN}{CtotalN} = \frac{Vref * \sum dPhigh}{CtotalP} - Vin + \frac{Vref * \sum ChighP}{CtotalP} \tag{17}$$

Assuming that DP_{code_h} and DN_{code_h} represents the summation of digital equivalent of errors occurred in the capacitors tied high on the positive and negative side respectively, then

$$\frac{DNcode\_h}{FSCode} * Vref + (1 - \frac{CodeP}{FSCode}) * Vref = \frac{DPcode\_h}{FSCode} * Vref - Vin + \frac{CodeP}{FSCode} * Vref \tag{18}$$

$$\frac{Vin}{Vref} = \frac{2 * CodeP - DNcode\_h + DPcode\_h}{FSCode} - 1 \tag{19}$$

$$CodeP = \frac{FSCode * (\frac{Vin}{Vref} + \frac{DNcode\_h - DPcode\_h}{FSCode} + 1)}{2} \tag{20}$$

$$CodeP = \frac{DNcode\_h}{2} - \frac{DPcode\_h}{2} + \frac{FSCode*(Vref+Vin)}{2*Vref} \quad (21)$$

$$CodeP - \frac{DNcode\_h}{2} + \frac{DPcode\_h}{2} = \frac{FSCode*(Vref+Vin)}{2*Vref} \quad (22)$$

$$CodeP - \frac{DNcode\_h}{2} + \frac{DPcode\_h}{2} = \frac{FSCode}{2} + Vin \quad (23)$$

Here if it is assumed that the input range V_{in} or equivalently *FSCode* range from $-V_{ref}$ to $+V_{ref}$, then *FSCode*/2 indicates bipolar zero. Therefore V_{in} is equal to the summation of decisions taken on the positive side minus the summation of half of the errors occurred in the capacitors tied high on the negative side plus the summation of half of the errors occurred in the capacitors tied high on the positive side.

Similarly, re-working the derivation substituting,

$$\frac{Vref*\sum ChighN}{CtotalN} = Vref - \frac{Vref*\sum ClowN}{CtotalN} \quad (24)$$

$$Vref - \frac{Vref*(\sum ClowN + \sum dNlow)}{CtotalN} = Vref*\frac{(\sum ChighP + \sum dPhigh) - CtotalP*Vin}{CtotalP} \quad (25)$$

Proceeding ahead in the same way as shown above for the first case, it will turn out to be

$$CodeP + \frac{DNcode\_l}{2} + \frac{DPcode\_h}{2} = \frac{FSCode}{2} + Vin \quad (26)$$

In this case, DN_{code_l} denotes the summation of digital equivalent of errors occurred in the capacitors tied low on the negative side. This equation (26) states that it is possible to add the sum of the errors found on the positive and negative side of the capacitors that are decided to be connected to V_{ref} on the P-side. This sum could be added with the intermediate digital output got with mismatched physical capacitances to get the final digital output value.

Equations (23) and (26) show different ways of doing digital trimming process both of which are valid. Fig. 33 captures the proposed algorithm in a single flow chart.

4.5 Comparator Design

The comparator is made up of six gain stages and a separate differential to single ended converter amplifier. It also has a buffer at the end. The comparator is designed to work with a common mode voltage varying from 0 to 4.096V with an accuracy of 14-bits. It is made to deliver the outputs within 50 ns. Since the comparator should also work with a common mode of 0V, it is made with PMOS input stages with autozeroing done at the end of 2^{nd} and 4^{th} gain stages. The block level schematic of the comparator is shown in Fig. 34.

4.6 Layout Details

The layout of this self-calibrating SAR A/D converter is shown in Fig. 35. The size of this die is 3757.6 um x 3470 um. The placement of different blocks such as comparator, reference, reference buffer, capacitors on the positive side of the CDAC (P-CDAC), capacitors on the negative side of the CDAC (N-CDAC), high voltage positive switches,

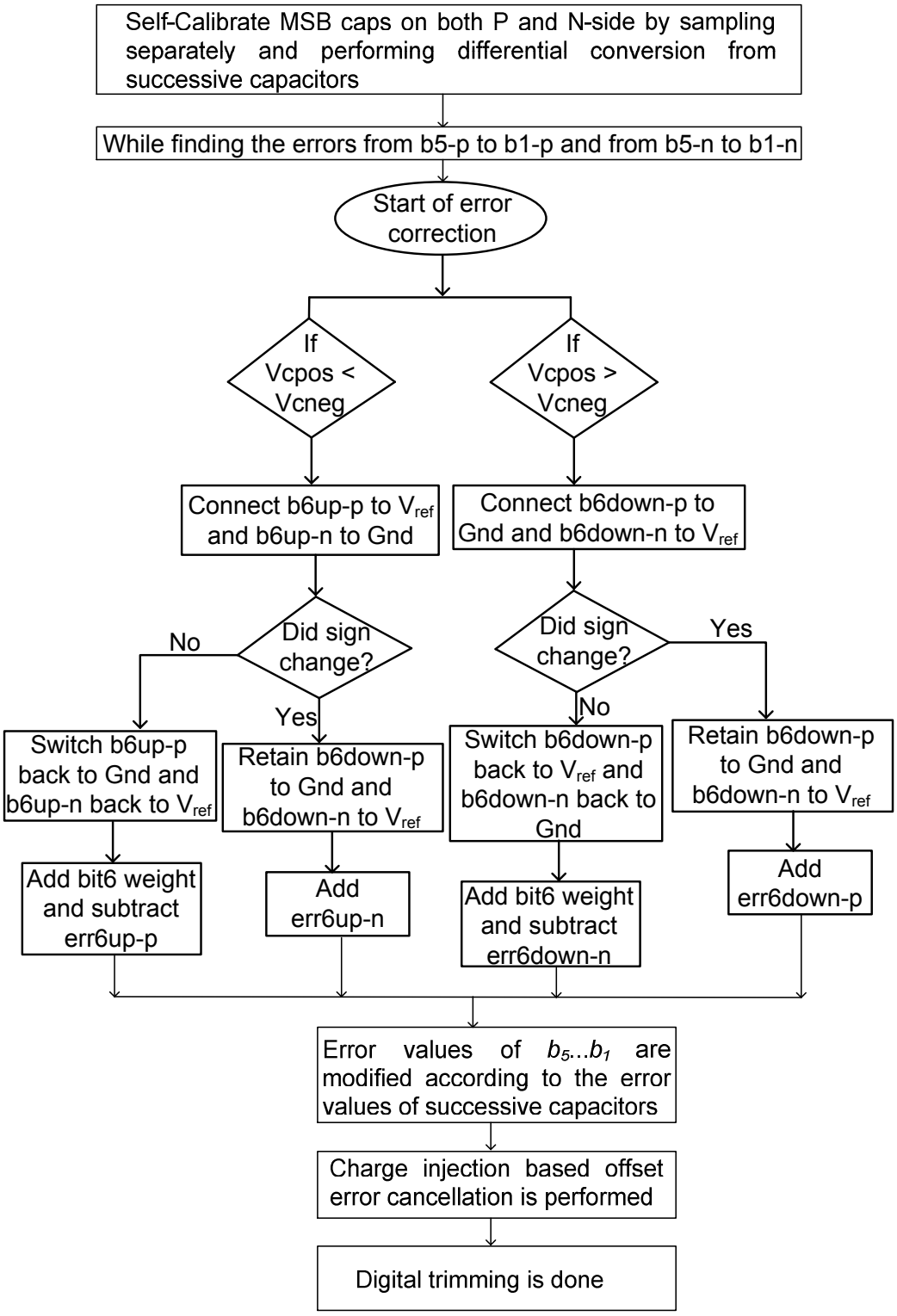

Fig. 33 Summary of the Proposed Algorithm

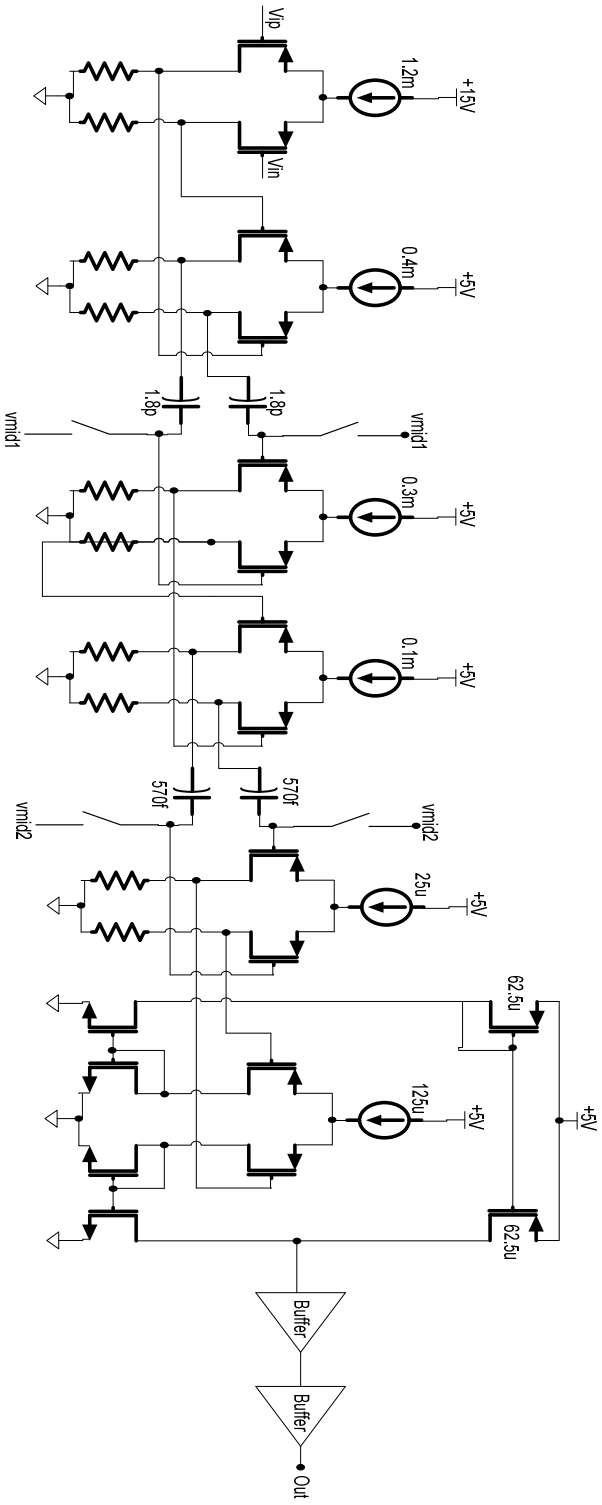

Fig. 34 Comparator Design

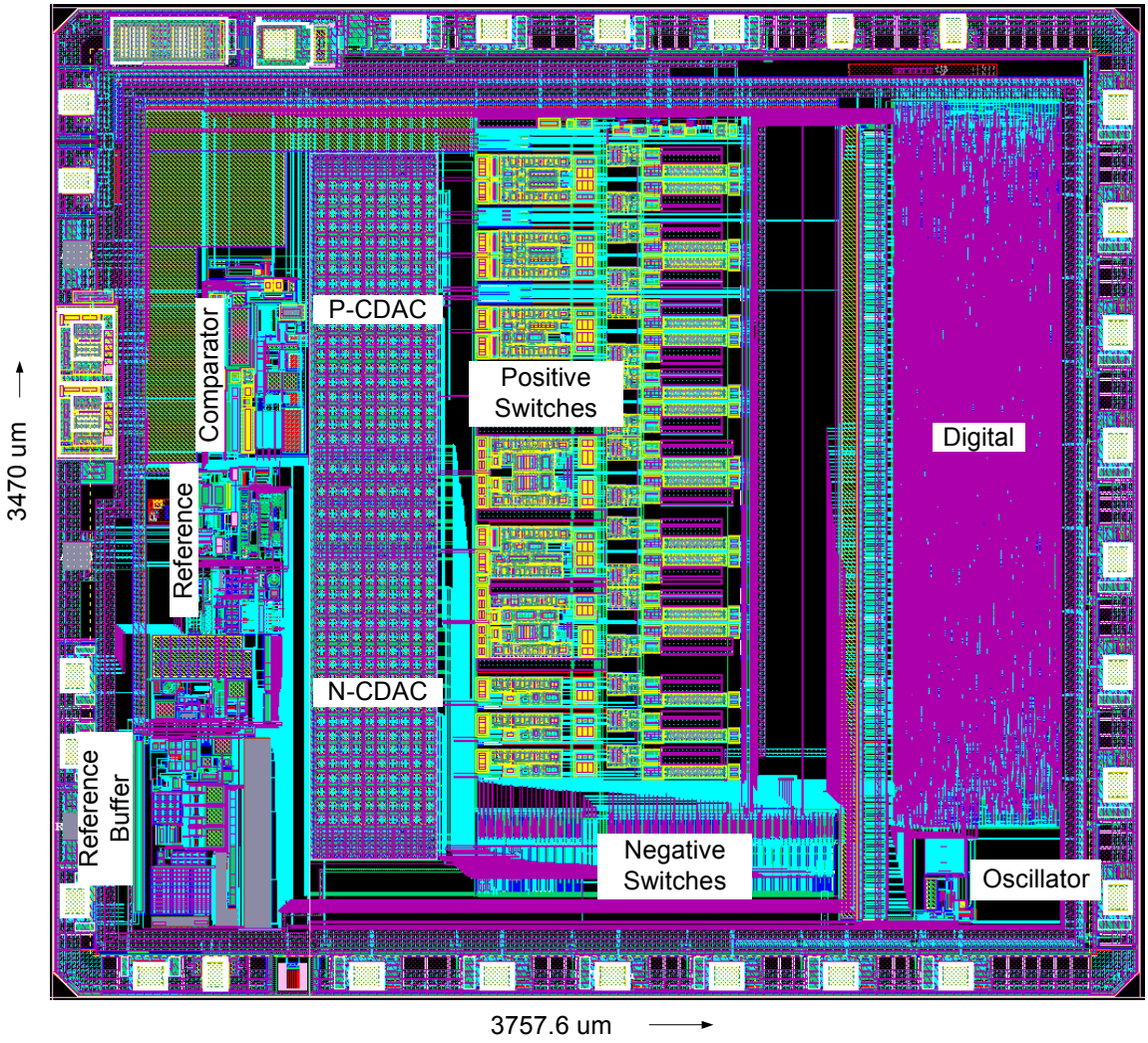

Fig. 35 Layout of Self-Calibrating SAR A/D Converter

low voltage negative switches, digital block and oscillator block are all shown in the Fig. 35.

Design Rule Check (DRC) and Layout versus Schematic (LVS) was run on this layout. The reults were seen to be clean except for a minute parametric errors on the resistors and capacitors due to pdk version and we do not typically care about it. The LVS result is shown in Fig. 36.

4.7 DIGITAL DESIGN

The implementation of the digital block is made by RTL design using VHDL and Verilog codes. The digital block contains several sub-blocks including SAR engine, digital calibration, asynchronous sampling, fuse controls, register mapping and SPI interface. The RTL design is done using HDL Designer from Mentor Graphics. Synthesis is done using Design Compiler from Synopsys, Place and Route is done using Encounter from Cadence. During Place and Route, all the steps were taken care of including Floorplanning, Power Planning, Placement of Standard Cells, Clock Tree Synthesis,

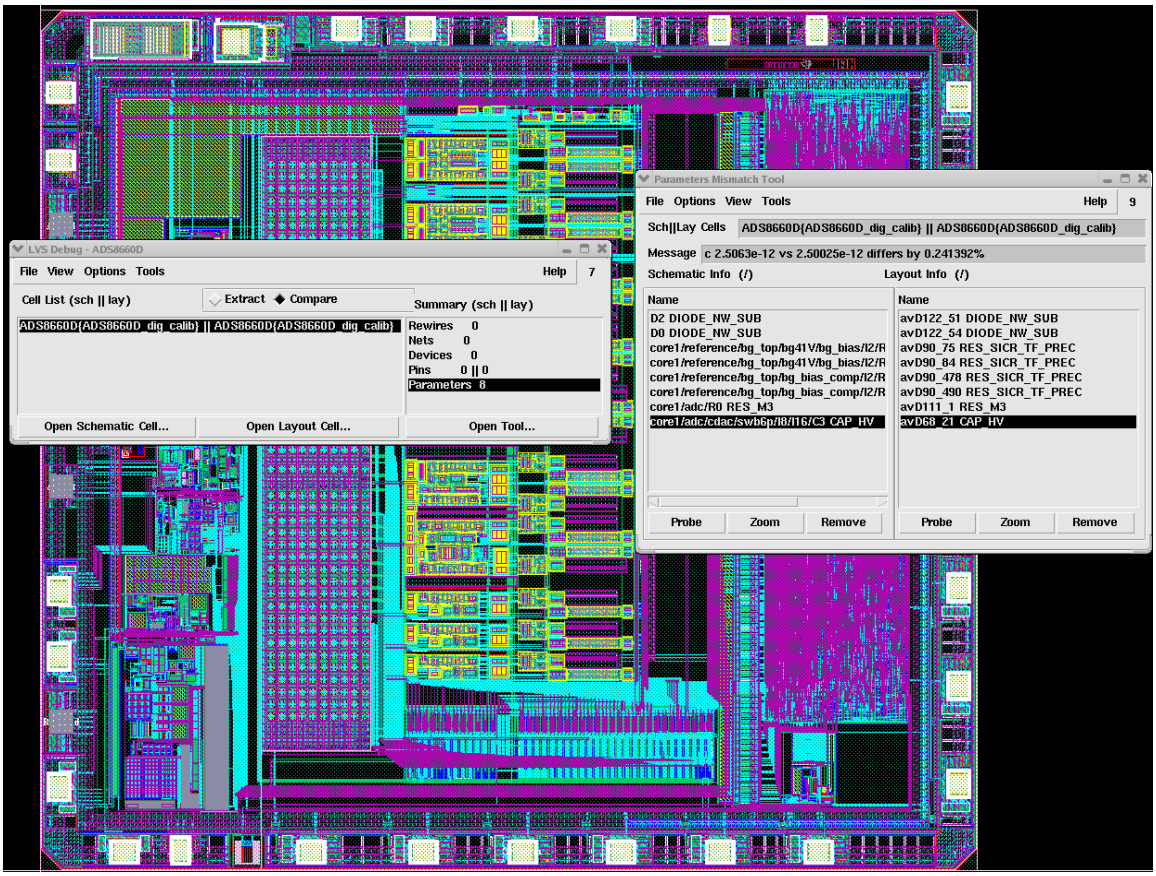

Fig. 36 LVS Result

Timing Analysis and Placement of Spare Capacitors and Spare MOS etc.

The digital die area alone occupies 2534.8 um x 575.8 um. The designed digital block have 13967 cells equivalent to a 2-input NAND gate cell in which the digital calibration unit alone occupies 2802 cells. So the increase in digital die area due to self-calibration and digital-trimming is only 20%.

5 SIMULATION AND MEASUREMENT RESULTS

5.1 SIMULATION RESULTS

The Self-Calibration and Digital-Trimming algorithm is simulated both using both Matlab and in Cadence Design Environment using 0.6 um High Voltage CMOS TI process. The ideal value of the capacitors for a 14-bit converter with differential dynamic error correction at bit-6, bit-12 and a single-ended dynamic error correction at bit-14 would be

P-side caps = [*8192 4096 2048 1024 512 256 256 256 128 64 32 16 8 4 4 4 2 1 2 0.5 0.25 0.25*];

N-side caps = [*8192 4096 2048 1024 512 256 256 256 128 64 32 16 8 4 4 4 2 1 2 0.5 0.25 0.25*];

During Matlab simulation, to check the validity of this algorithm, intentionally capacitors were mismatched as follows in Example – I below.

Suppose if the capacitor values are

P-side caps = [*8192 4096 2048 1055 512 256 256 256 128 64 32 16 8 4 4 4 2 1 2 0.5 0.25 0.25*];

N-side caps = [*8342 4096 2048 1024 512 256 256 256 128 64 32 16 8 4 4 4 2 1 2 0.5 0.25 0.25*];

Now with this erroneous capacitor values, linearity curves were plotted with and without this algorithm. Without this algorithm, the errors were ranging from -750 LSBs to +300 LSBs. But after using this algorithm, we see that this linearity error is getting

restricted within +/-1 LSB. Here we plotted all the 16384 codes interleaved by just 512 codes for faster matlab simulation. The Matlab plots for this Example – I with and without this algorithm is shown in Fig. 37. The red curve is linearity plot without using this algorithm and the blue curve shows the plot after using this algorithm. The inscribed plot is the zoomed in version after applying this algorithm showing that the linearity error is within +/-1 LSB.

Similarly again, capacitors were mismatched in the other way in Example – II. Suppose if the capacitor values are

P-side caps = [8152 4056 2048 1044 512 256 256 256 128 64 32 16 8 4 4 4 2 1 2 0.5 0.25 0.25];

N-side caps = [8172 4096 2048 1024 512 256 256 256 128 64 32 16 8 4 4 4 2 1 2 0.5 0.25 0.25];

The plot for this case is shown in Fig. 38. Here it shows that without applying this algorithm, the linearity error varies from -200 LSBs to +800 LSBs. But after applying this algorithm, the linearity error is restricted to less than +/-1 LSB which is zoomed and shown in the inscribed picture within Fig. 38.

Then this algorithm is implemented on a SAR ADC meant for usage in industrial applications, particularly motor control applications. For this application, the ADC should be capable enough to accept +/-12V with a power supply of +/-15V generating 14-bit at a speed of 400 kSps. This ADC is designed in Cadence Design Environment using transistors from 0.6 um High Voltage CMOS process from TI. With the self-

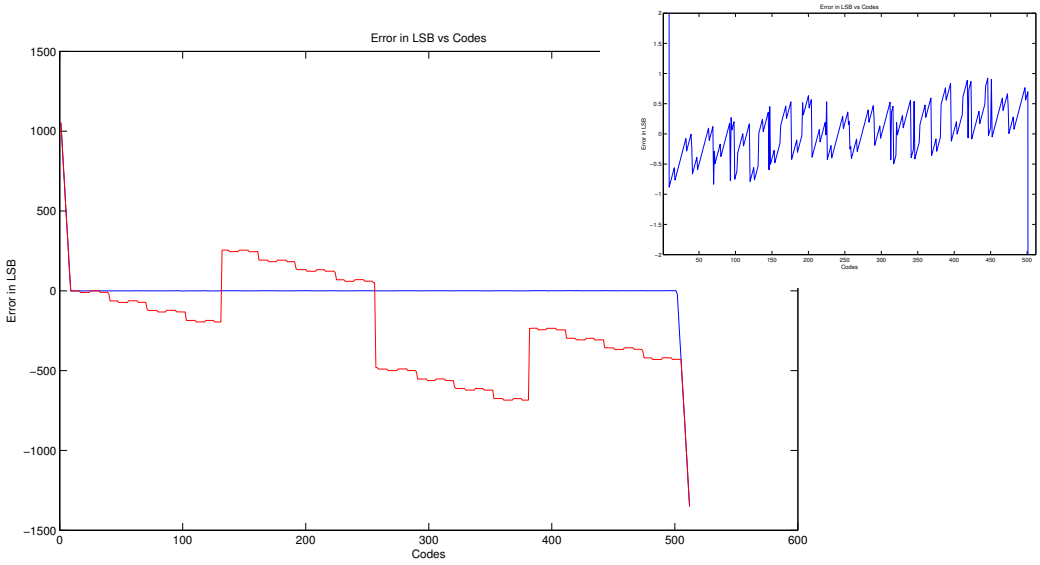

Fig. 37 Matlab Simulation Result for Example – I

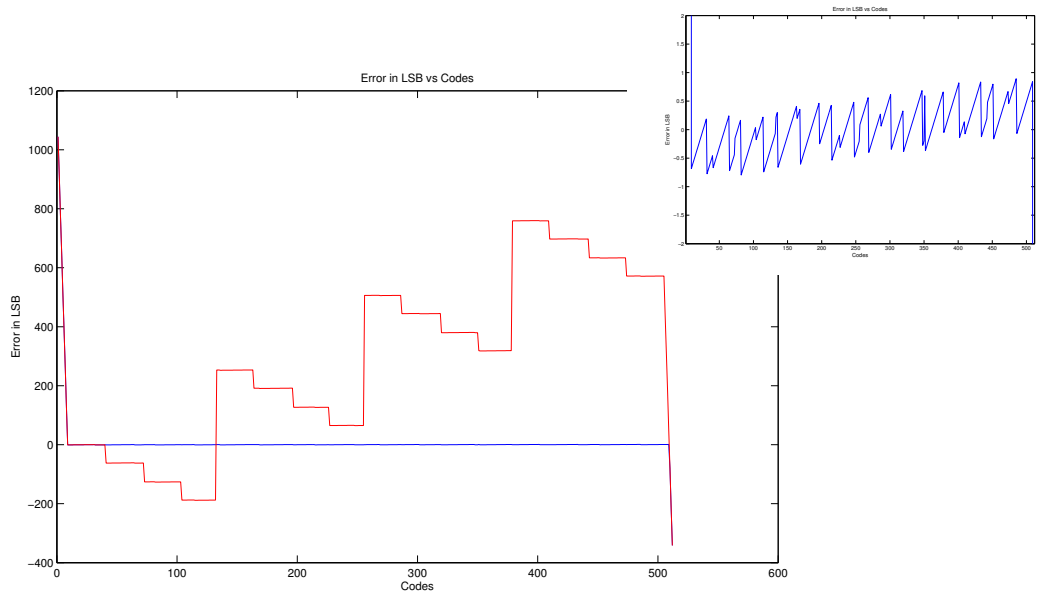

Fig. 38 Matlab Simulation Result for Example - II

calibration feature switched on in Spectre simulation, different parts of the input voltage is ramped up at steps of LSB/4 and the output digital codes are monitored to see for any long codes or any missing codes. No discrepancies were observed in Cadence Simulation. The output digital codes are seen to have errors less than +/-1 LSB. This confirms the working of this algorithm in Cadence Design Environment. One such plot containing input ramp in steps of LSB/4 versus output digital codes is shown in Fig. 39. Here is the output digital codes is shown in terms of analog voltage for verification convenience. Also the analog voltage difference between the input ramp and output digital code is because of the intentional offset and gain error setup in the simulation.

5.2 MEASUREMENT RESULTS

The proposed on-chip, self-calibrated and digitally-trimmed high-voltage compliant SAR ADC core occupies an area of 9.76 mm^2. This area includes high-voltage compliant bootstrapped input switches, internal reference, reference buffer, internal oscillator, fuses and digital logic. A die micrograph is shown in Fig. 40. This SAR-ADC consumes about 90-mW during normal operation from +/-15V supply. Input capacitance of 40 pF is used in each CDAC and an internal reference of 4.096V is used in this design. The SAR uses a master clock of 20 MHz, and a differential dynamic error correction is performed at bit-6 and bit-12 positions using 256 and 4-LSB capacitors respectively. Moreover, single-ended dynamic error correction is also performed at bit-14 position using 2-LSB capacitor. The density of the poly1-trinitride capacitors used in CDAC array is 0.63 fF/um^2.

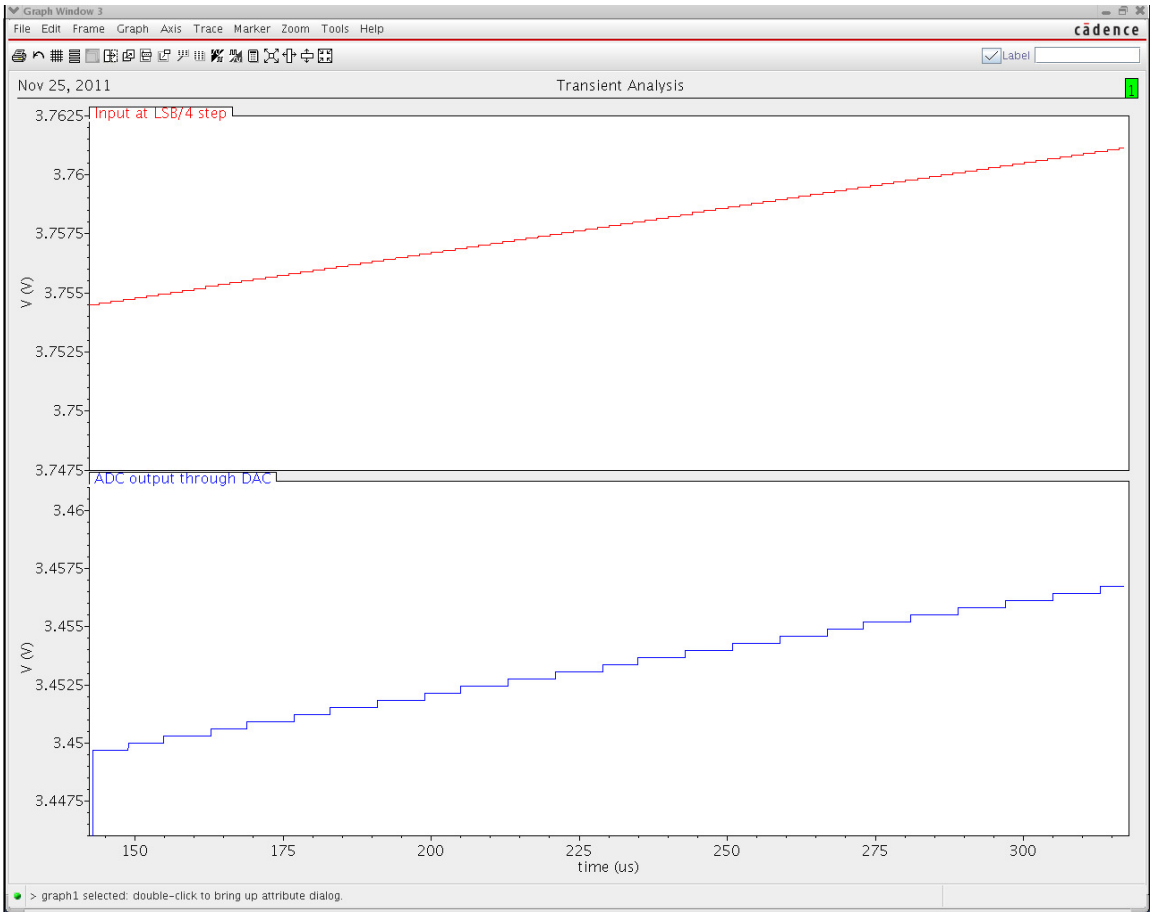

Fig. 39 Input Ramp vs Ouput Steps in Cadence Simulation

The analog and digital circuitry for the proposed technique occupies less than 4% of the total area and consumes less than 3 mA during calibration. The proposed calibration technique has minimum impact on power consumption during normal operation. Self-calibrating the differential array takes just 515 µs on power-up and digital trimming process does not take any additional time.

Fig. 41 compares the differential non-linearity before self-calibration and after self-calibration. Similarly, Fig. 42 compares the integral non-linearity. It was seen that the INL errors of the order of 7 LSBs are reduced to less than 1 LSB after self-calibration at

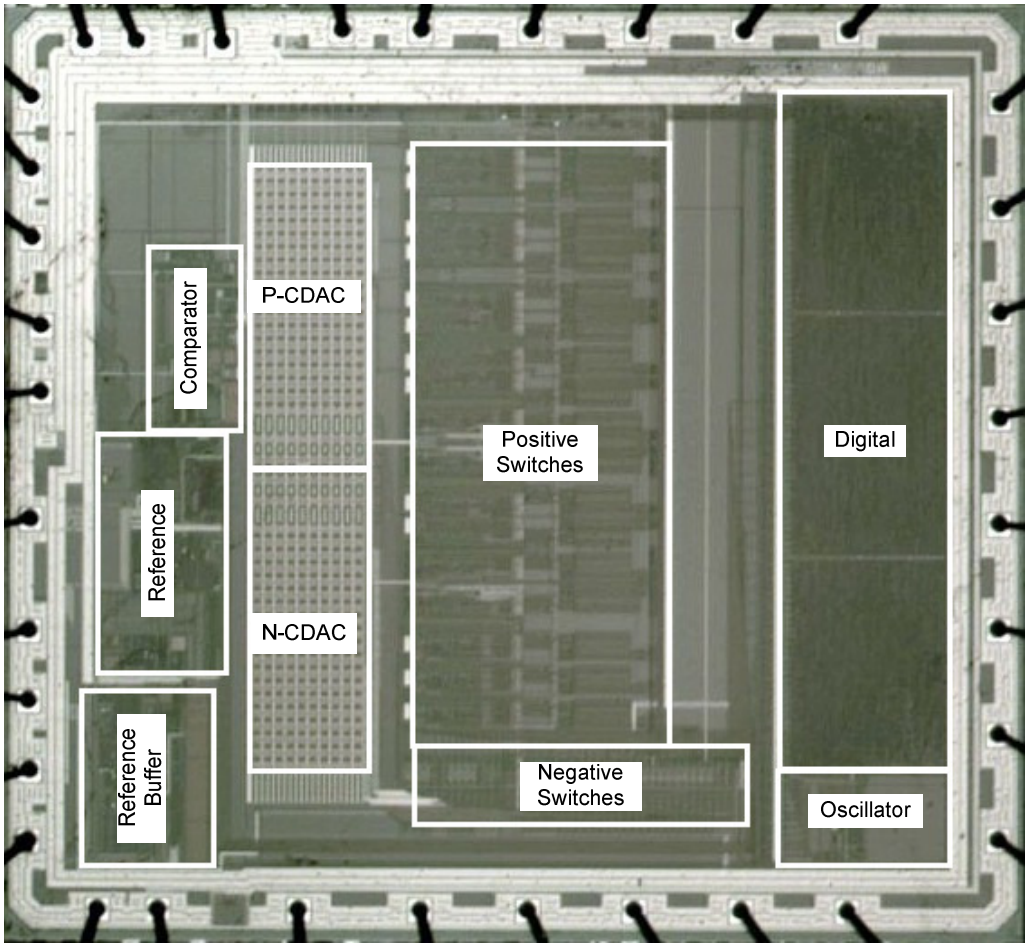

Fig. 40 Die Micrograph

at 14-bit level. Fig. 43 and Fig. 44 compare the FFT plot of the samples collected at the output of ADC before and after self-calibration. For this case, the ADC is converting an input sine wave of 5.053 kHz while running at a sampling rate of 400 kSPS. As shown in Fig. 43, before self-calibration, the ADC has less than 65-dB total harmonic distortion (THD) due to capacitive mismatch. This THD improves by 24-dB after self-calibration is performed. The SNDR value before self-calibration is 61.29 dB and after self-calibration, it is 73.32 dB. Fig. 45 shows the SNDR and SFDR values across different input

frequencies. Dynamic Error Correction (DEC) is used both during normal operation as well as during intial calibration. DEC improves the INL performance of the order of 0.5 LSB at 400kS/s. While running at 500 kS/s, it makes a difference of 1 LSB with and without DEC. The overhead being the three extra clock cycles for each conversion but the clocks are now run faster with DEC in order to compensate for it. Even after accounting for three extra clocks for DEC, the effective conversion speed is much higher

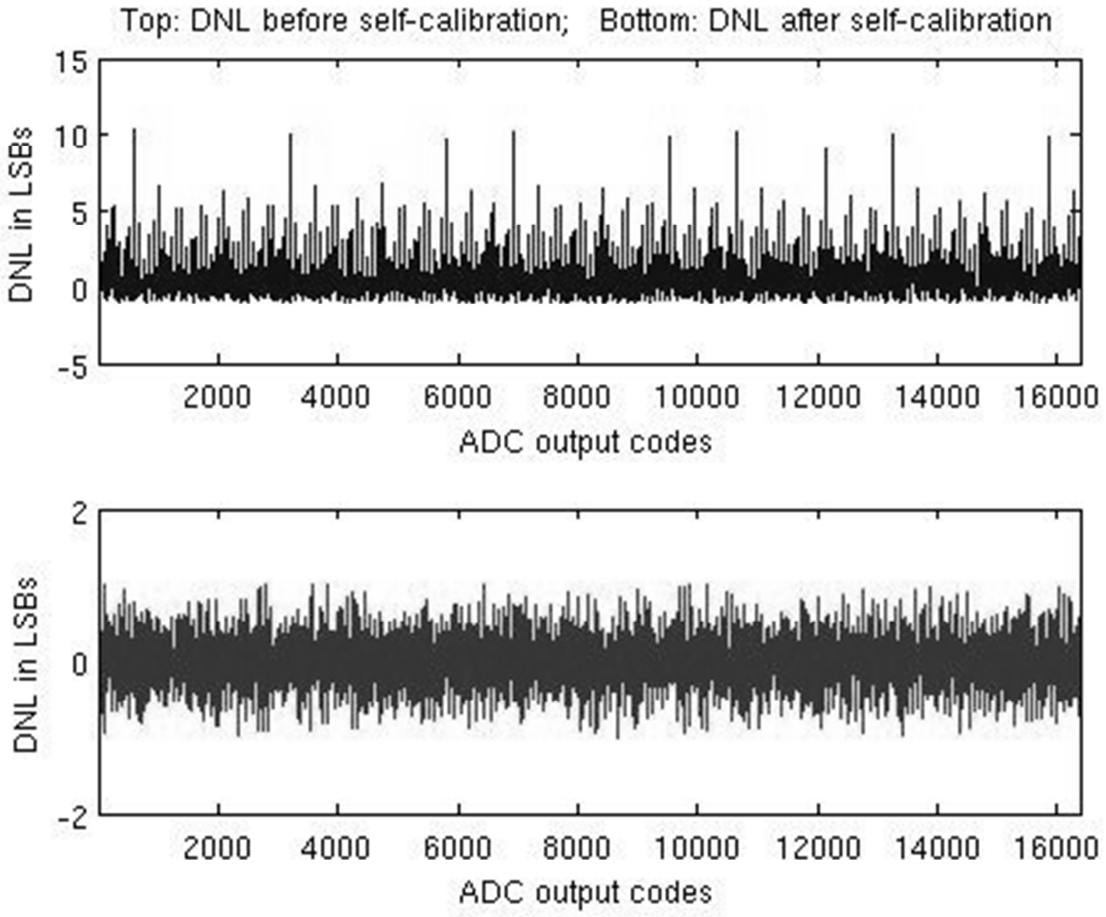

Fig. 41 Differential Non Linearity Before and After Self-Calibration

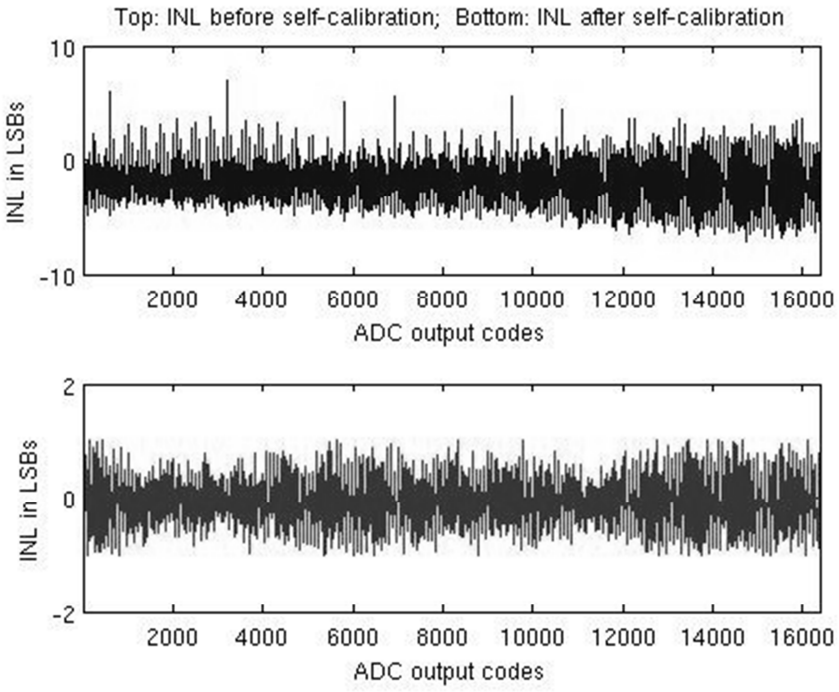

Fig. 42 Integral Non Linearity Before and After Self-Calibration

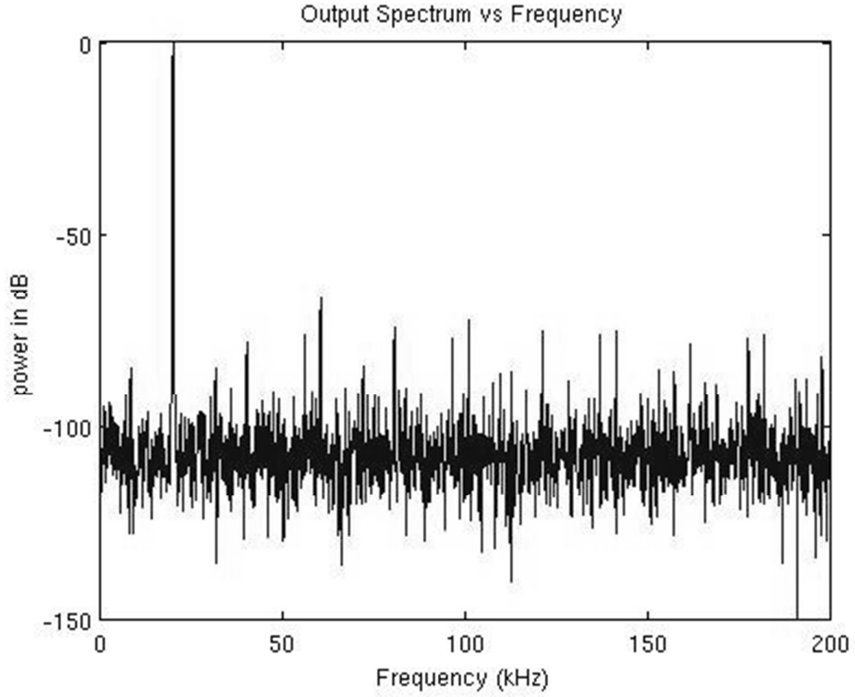

Fig. 43 FFT Plot Before Self-Calibration

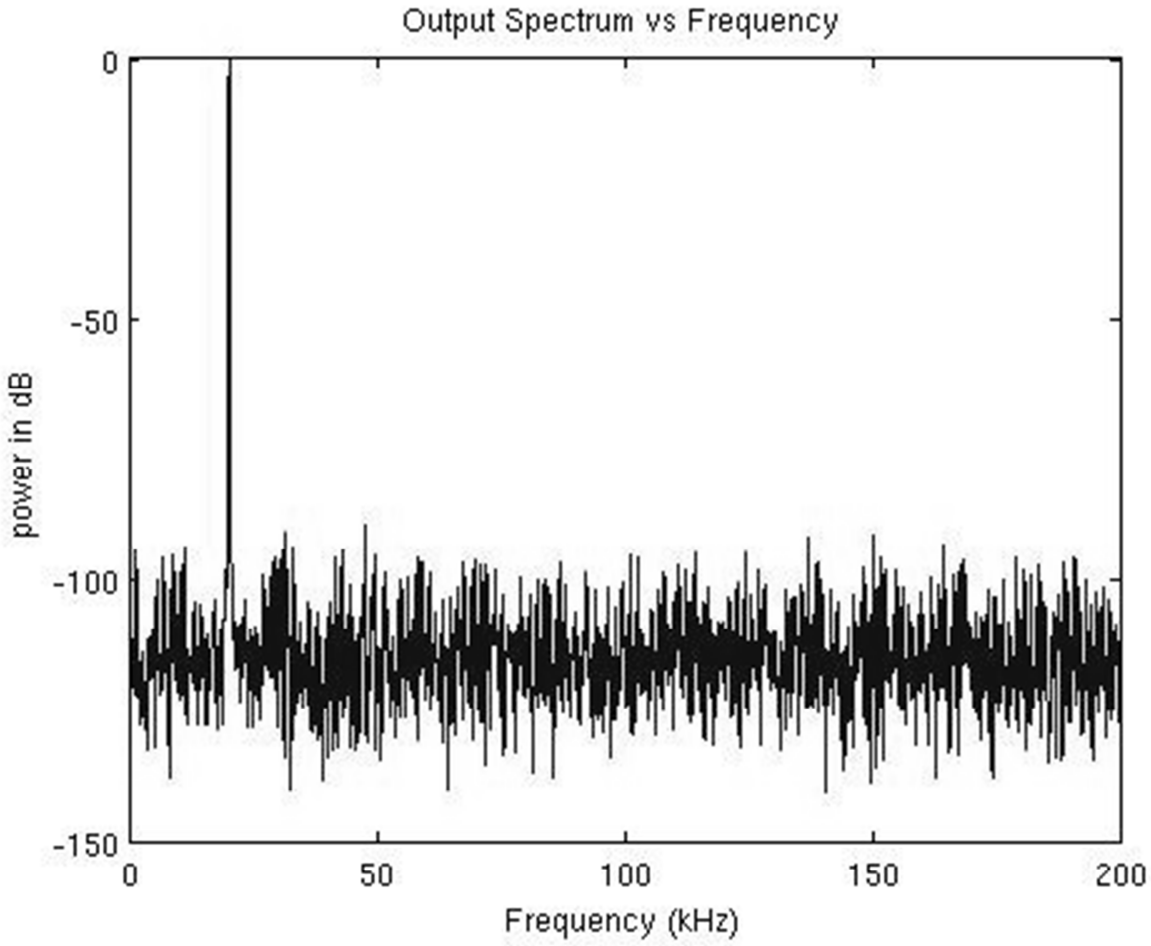

Fig. 44 FFT Plot After Self-Calibration

for the required INL performance. Table 3 tabulates the achieved performance with this implementation and Table 4 compares this work with respect to other state of the art ADCs.

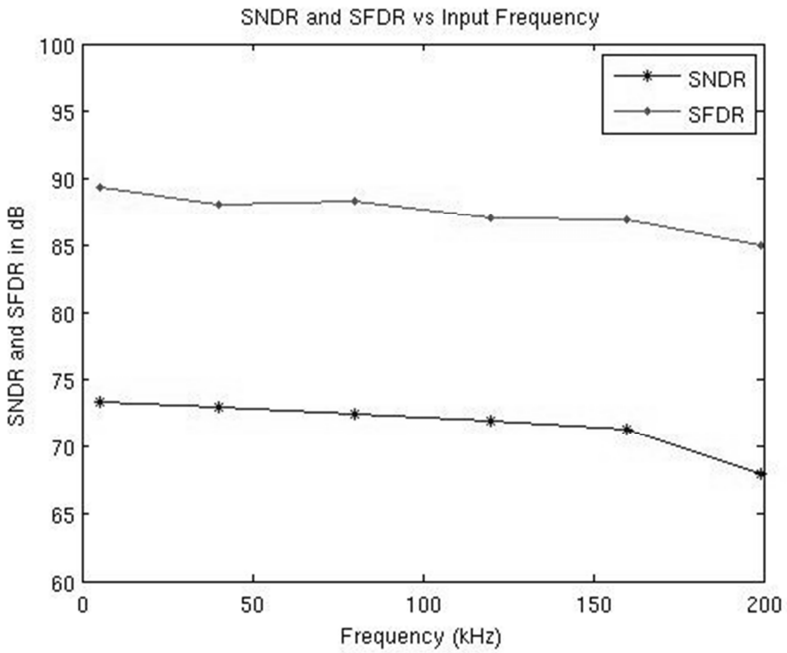

Fig. 45 SNDR and SFDR Plot Versus Input Frequency

Table 3 Silicon Performance

Technology	**0.6 um HV CMOS Process**
Resolution	14-bit
Conversion Rate	400 KHz
Area	9.76 mm^2
Input Voltage	+/-12 V
Supply Voltage	+/-15 V
SNDR	73.32 dB
THD	89 dB
Total Power Consumption	90 mW
INL	0.95 LSB
DNL	0.92 LSB
Input Capacitance	40pF

Table 4 Comparison to the State of the Art Works and Specification Summary

	Verma, JSSC 2007, [1]	**AD7610**	**ADS8504**	**This Work**
Process	0.18u	NA	0.6u	0.6u
ENOB (bit)	10.5 @ 50kHz	15.2 @ 2kHz	11.8 @ 45kHz	11.9 @ 5kHz
Sampling Frequency (kS/s)	100	250	250	400
Power (mW)	0.025	90	70	90
Area (mm2)	0.63	NA	NA	9.76
Input Range	1-V	+/-10-V	+/-10-V	+/-12-V
Resolution	12	16	12	14

6 CONCLUSION

6.1 CONCLUSION

A power-on self-calibration and digital-trimming algorithm for a 14-bit high-voltage SAR ADC converter is presented. By using the proposed approach, even a larger mismatch of around 261-LSBs can be corrected to improve yield. The algorithm can be adopted for SAR ADCs with both differential CDACs and single-ended ones. This is the only calibration algorithm known in literature to correct for mismatches occurring on any bit capacitance between the P-side and N-side arrays in addition to correcting for mismatches within the binary weighted capacitors inside any array. Also this algorithm is unique to detect and correct for charge injection based offset error in self-calibration and at the same time, it eliminates mismatches occurring between the dynamic error correction capacitors and normal capacitors. This algorithm is also more robust since it finds the errors on capacitors of both P-side and N-side arrays individually and so it could correct a wide range of errors including the mismatch between the arrays. Also this self-calibration routine could be run on SAR ADCs during each power-on so that the capacitive mismatches that could occur due to environmental conditions such as temperature and process variations affecting the linearity of the ADCs could be totally eliminated.

6.2 FUTURE WORKS

A possible list of future works is listed below.

- An alternate and effective implementation of the self-calibration/digital-trimming algorithm could be thought of without relying too much on the dynamic error correction capacitors.
- A similar self-calibration/digital-trimming algorithm could be thought of, to be generalized in all the ADCs and not specifically with respect to SAR ADCs alone.

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BIOGRAPHICAL SKETCH

Shankar Thirunakkarasu was born in Chennnai, India. He received the B.E. degree in Electronics and Communication Engineering from College of Engineering, Guindy, Anna University, India in 2006 and the M.S degree in Electrical Engineering from Arizona State University in 2008. He received the Best Teaching Assitant Award from ASU in 2008. In Summer 2007, he worked as a design intern in On-Semiconductor, Phoenix, AZ. From October 2008 to May 2013 he was with Nyquist Converter group and Advanced Development for Precision Data Converters group in Texas Instruments, Tucson, AZ designing high resolution A/D converters. Since June 2013, he has been working at Broadcom, Austin, TX, on the design of communication receivers for satellite and TV applications. His research interests are in the area of high performance and high frequency analog/mixed signal circuit designs. He is currently finishing his Ph.D. in Arizona State University.