Static Behavior of Chalcogenide Based Programmable Metallization Cells

by

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ABSTRACT

Nonvolatile memory (NVM) technologies have been an integral part of electronic systems for the past 30 years. The ideal non-volatile memory have minimal physical size, energy usage, and cost while having maximal speed, capacity, retention time, and radiation hardness. A promising candidate for next-generation memory is ion-conducting bridging RAM which is referred to as programmable metallization cell (PMC), conductive bridge RAM (CBRAM), or electrochemical metallization memory (ECM), which is likely to surpass flash memory in all the ideal memory characteristics. A comprehensive physics-based model is needed to completely understand PMC operation and assist in design optimization.

To advance the PMC modeling effort, this thesis presents a precise physical model parameterizing materials associated with both ion-rich and ion-poor layers of the PMC's solid electrolyte, so that captures the static electrical behavior of the PMC in both its low-resistance on-state (LRS) and high resistance off-state (HRS). The experimental data is measured from a chalcogenide glass PMC designed and manufactured at ASU. The static on- and off-state resistance of a PMC device composed of a layered (Ag-rich/Ag-poor) Ge30Se70 ChG film is characterized and modeled using three dimensional simulation code written in Silvaco Atlas finite element analysis software. Calibrating the model to experimental data enables the extraction of device parameters such as material bandgaps, workfunctions, density of states, carrier mobilities, dielectric constants, and affinities.

The sensitivity of our modeled PMC to the variation of its prominent achieved material parameters is examined on the HRS and LRS impedance behavior.

The obtained accurate set of material parameters for both Ag-rich and Ag-poor ChG systems and process variation verification on electrical characteristics enables greater fidelity in PMC device simulation, which significantly enhances our ability to understand the underlying physics of ChG-based resistive switching memory.

Dedicated to my parents

Mr. Manouchehr Rajabi and Mrs. Nasrin Sarabadani

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NOMENCLATURE

CBRAM	conductive-bridging random-access memory
ChG	chalcogenide glass
DFT	density function theory
DRAM	dynamic random-access memory
ECM	electrochemical metallization
FEA	finite element analysis
FEM	finite element method
MOS	metal-oxide-semiconductor
NVM	non-volatile memory
PMC	programmable metallization cell
Redox	reduction-oxidation (chemical reactions)
ReRAM /RRAM	resistive random-access memory
TCAD	technology computer aided design

1. INTRODUCTION

1.1. Motivation

The ideal memory is non-volatile one which has the ability of maintaining stored information even when the power to the system has been turned off. NVM has maximal capacity, speed, retention time, endurance, and radiation hardness while also having minimal physical size, energy usage, and cost. Discrete and embedded NVM technologies have therefore been an essential part of electronic systems for the past 30 years. The most popular type of NVM is flash memory. Flash memory is a division of electrically erasable and programmable read only memory (EEPROM) devices with exclusive architecture compromises granularity of write operation to achieve cost and scalability advantage.

Today's nonvolatile memory technologies based on charge storage mechanism are facing serious scaling challenges [1], [2], [3]. Many new main technologies are being assumed for future generation of nonvolatile memory. The key driver is reducing the cost that has considerably increased the bit density 10^4 times for flash memory over the previous two decades [4]. However there are other minimal requirements that must be covered by an emerged technology before it can be set up as the next generation NVM for code storage applications. Some of these merits are mentioned in Table1 where a typical 65nm NOR flash memory specifications are summarized as a reference [4]. In this table, F is the minimum lithographic feature size. Different manufacturers have different definitions for word, block and sector concepts but usually 16 bits represent 1 word and 64000 words represent one block or sector. SLC and MLC refer to single level and multilevel cell, respectively. The ratio of total chip area devoted to storage cells to the overall chip area is defined as array efficiency. In an SLC only one bit can be stored per physical cell location, but in a MLC, 2 or more bits can be stored per cell. At last, the exact requirements for "high temperature" retention specifications depend on the end market and the memory device usage field. The minimum requirements indicated in this table for future NVM technologies are somewhat arbitrary but are based on the rational assumptions and estimations. Whatever technology that becomes the replacement of today's code storage technologies will have to satisfy the performance metrics and cost minimum limits and also match with today's reliability parameters of different solutions.

Besides, for future scaling and cost reduction, the emerged technology has to solve the difficulties that exist for NVM scaling or provide the MLC storage capability at the same F^2 footprint [3], [4].

Energy and power consumptions are important parameters but the main driver for almost all of today's markets is cost. The core cell operation requirements are essential in assessing any new memory technology for being matched to ultralow-energy applications and they derive from the physics governing data storage mechanism [4].

Table I: Requirements for NVM Devices for Code Storage **[4]**

Requirements for NVM Devices for Code Storage		
	Today's Typical NOR Flash Specifications for Code Storage Applications	**Next Generation NVM Technologies' minimal requirements**
Cell Size (for SLC)	$9F^2$ to $15F^2$	<$9F^2$
Array Efficiency	>60%	>70%
Program Time	100µs to 500µs per WORD	<10µs per WORD
Erase Time	500ms to 5s per BLOCK	<5ms per BLOCK
Write Cycles Allowed	100000	100000
Read Access Time	<100ns	<50ns
Retention	10 years at high temp	10 years at high temp
MLC Capability Requiremetn	YES	YES

The storage mechanisms in most of the emerging technologies are common and they are struggling for victory as the next NVM technology [5]-[7], [8]. Four technologies that currently have reached a level of maturity that is beyond simple demonstration of single cell functionality in a laboratory are: magnetoresistive memory (MRAM), phase change memory (PCM), ferroelectric memory (FeRAM), and conductive bridging memory (CBRAM) [4].

- Magnetresistive Memory:

Magnetoresistive random access memories (MRAM) data storage is through modulating the resistance of magnetic tunnel junctions whose resistivity is due to magnetic polarization of thin ferromagnetic layers [9]-[11].

- Phase Change Memory:

Phase change memory (PCM or PRAM) devices store the data as the dielectric resistance change, that can switch between crystalline or amorphous states due to applying voltage or current [14]-[16].

- Ferroelectric Memory:

Ferroelectric random access memories (FeRAM) save information by modulating ferroelectric capacitor polarization and sensing the charge_voltage response [12], [13].

- Conductive Bridging Memory:

Conductive bridging RAM (CBRAM), also known as programmable metallization cell (PMC), solid electrolyte memory, or nano-ionic resistive memory is another family of resistive memory cells saving data by modulating the resistance of a dielectric through transport and reduction of metallic ions [17]-[20].

Table II compares four new memory technologies mentioned above from two points of view. The first is their compatibility to substitute today's NVM technologies regarding improvements in performance, scalability and cost. The second is the operational characteristic of mentioned technologies from integration in subthreshold CMOS point of view. Among these four types of memories, PMC technology is the only technology that has the capability to satisfy more concerns facing flash memory as well as cover the requirements for subthreshold CMOS and ultralow-energy applications. PMC is less mature than the other introduced technologies [4].

The other advantage of CBRAM (ionic memory) is that the cell write energy is much less than other resistive memories [21]. Device switching speed versus write energy is graphed for different memory technologies in Fig. 1 [21]. The size of the circles shows relative voltage of operation. CBRAM can work at lower voltages than some emerged technologies [4].

Table II: Comparison of four emerging memory technologies over today's floating gate based NVM technologies used for code storage [4].

	MRAM	FeRAM	PRAM	CBRAM
Cost(sell size, array, efficiency)	NO	NO	YES	YES
Cost(MLC Capability)	NO	NO	Unknown	YES
Performance (write speed, read speed)	YES	YES	YES	YES
Reliability (endurance, retention)	YES	YES	YES	YES
Compatibility with subthreshold CMOS	NO	NO	NO	YES
Maturity Level	16Mb Production. Niche Markets	2Mb Production. Niche Markets	512Mb Testchips	2Mb Testchips

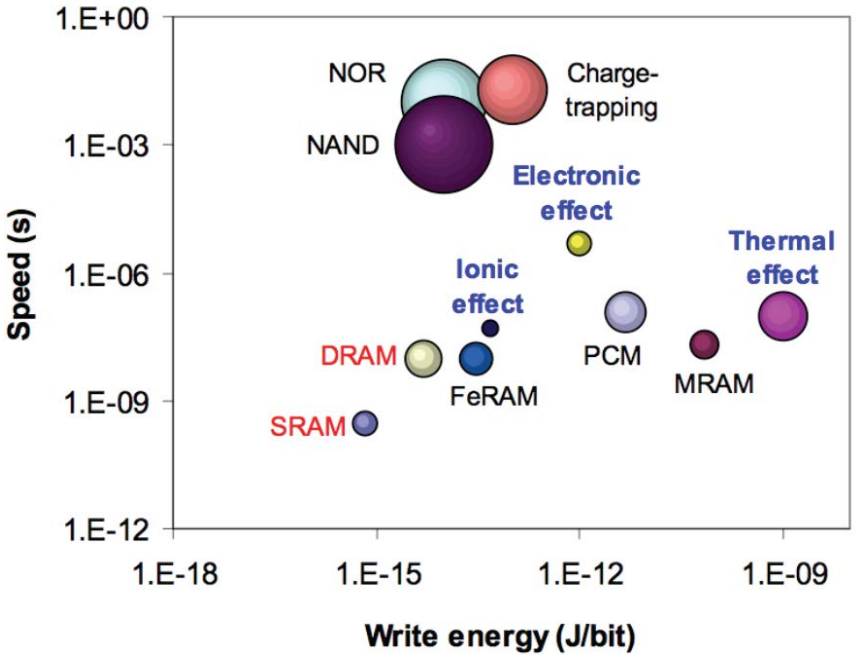


Fig. 1: Write energy and switching speed of some emerged memory technologies [21]

1.2. AgGeSe Glasses

The chalcogenide glasses are favorite semiconductors for many applications. They have used in optical recording [23], fiber optics [24], phase change memory [25], and some other technologies. GeSe glasses have been studied due to their good chemical stability, ready glass formation, and easy synthesis requirements. Se chains and GeSe tetrahedral are the basic structure units that can combine in many ways [22].

The Ge-Se system was the first one in which an intermediate phase formation was shown experimentally by Boolchand et al. [26] and developed more theoretically by Thorpe et al. [27]. In binary Ge_xSe_{1-x}glasses, when x is between 0.2 and 0.254, the phase is self organized, while glasses with x less than 0.2 are assumed as floppy and those with x higher than 0.26 are stressed rigid. Dynamic calorimetry measurements on the intermediate phase have shown that such materials do not age [28]. This property is important in their applications.

Adding silver to chalcogenide glasses has attracted extensive attention to the soft condensed matter science [29], [30]. The interest is partly due to the high glass formation tendency in the Ge-Se-Ag ternary, the eight orders of magnitude increase in glass electrical conductivity, and some light-induced effects such as photodeposition, photodiffusion, and photodoping. One of the problems of solid state ionics is still the detailed dynamics of mobile ions in amorphous materials [31], [32]. The Ge-Se-Ag structure has been studied using different methods (extended x-ray-absorption fine structure (EXAFS), differential anomalous x-ray scattering (DAS), x-ray diffraction, neutron diffraction with isotopic substitution, modeled differential scanning calorimetry (MDSC), and Raman spectroscopy). The ternary structure of the Ge-Se-Ag glasses has not yet been totally known. Main properties of the glass structure particularly for Se rich glasses with Se of more than 67% are being studied [32].

1.3. PMC Details

The PMC has many names due to its application including conductive-bridging random-access memory (CBRAM), resistive random-access memory (RRAM/ReRAM), electrochemical metallization memory (ECM), memristor, nano-ionic memory, redox memory, solid-electrolyte memory, and

Nanobridge. The cells switch by formation and dissolution of conductive filaments within a solid-state electrolyte between two electrodes through electrochemical reduction-oxidation reactions and ionic transport. The PMC device is a simple two-terminal structure, comprising a bottom inert electrode, the solid electrolyte, and an oxidizable metal layer, which can also be the top electrode. It can be at high-resistance in the non-bridge off-state or low-resistance in the bridged on-state. The bridge continually can form and dissolve and is effectively stable in high and low resistance states without wasting the static power [43]. PMC covers main features of flash and DRAM including small size, non-volatility, high endurance, multilevel programmability [39], fast random access speed [40], and very low energy usage in comparison with Flash [41], [43]. PMC has been used in memory applications like optics [38], micro-electromechanical systems [36], neuromorphic computing [35], and microfluidics [37].

To fully understand PMC operation and help in getting optimized design, a comprehensive physics-based model is needed. The other benefit of this model is creating an insight letting the development of a precise compact model for circuit simulation, which is required for efficient circuit design using PMC memories [43].

PMC technology is using in ultralow-energy and subthreshold CMOS applications, but there are many challenges need to be overcome yet. Some of these challenges are: accurate end-of-life reliability models, noise immunity perspectives, proper circuit techniques, operational algorithms to ensure reliable operation, and manufacturing initial volume runner products [43].

This thesis, with the intent of advancing the PMC modeling effort, presents a precise physical model parameterizing PMC's electrolyte materials and checks the process variation effects on those. Chapter 2 provides material and device theory applicable to the PMC as well as some electrical data and imagery of various filament types. Chapter 3 is dedicated to the PMC fabrication process and characterization. Chapter 4 presents a novel precise physical model parameterizing materials associated with both ion-rich and ion-poor layers of the PMC's solid electrolyte, so that captures the static electrical behavior of the PMC in both its low-resistance on-state (LRS) and high resistance off-state (HRS). Chapter 5 shows the effects of process variation on the impedance behavior of the PMC devices through changing the prominent achieved material parameters in both HRS and LRS.

2. THEORY

2.1. PMC Structure and Operation

The PMC device is a simple two-terminal structure, comprising a bottom inert electrode, the solid electrolyte, and an oxidizable metal layer, which can also be the top electrode. The solid electrolyte is an ion-conducting resistive material, often comprising a chalcogen-rich germanium-selenide (or -sulfide) chalcogenide glass (ChG) or sometimes oxides. The anode is made of a readily oxidizable metal such as Ag or Cu. The cathode is made of a non-oxidizable metal such as Ni, W or Pt. The memory effect of these materials was first reported in 1976 by Hirose and Hirose [44]. Designs with more layers do also exist [45, 46]. Many chemical compounds have been used as the solid-electrolyte, although they are mostly oxides or chalcogenides. Through a thermal, chemical, or photochemical doping process during fabrication or through an electrical forming process after fabrication, some materials which are being used in electrolyte, such as Ge_xS_y and Ge_xSe_y, start as insulators without mobile ions and become ionic or mixed conductors containing mobile ions [47]. Silver density functional calculations in Ge_2Se_3 have shown that silver will auto-ionize via giving an electron to the conduction band, which makes the ionized Ag atom to transport in the presence of an electric field. This behavior happens in insulators with large numbers of acceptor defect states in the bandgap and narrow-bandgap materials [48].

By applying an electrical field, an electrochemical reaction happens at the anode side that generates silver ions. The ions migrate across the chalcogenide layer and are deposited at the cathode. A metal conductive filament forms that bridges the gap between cathode and anode, and shunts the high resistance electrolyte. So the device goes from high resistance to low resistance (LRS) [49]. Fig 2 is showing a bridged device from the Hirose and Hirose paper [44].

After applying reverse bias, at the beginning of the reset process under reverse electrical bias, because of the enhanced lateral electric field at the top of the filaments, firstly the cations tend to dissolve laterally. At some point the diameter of the filament goes to zero at the top and the reset occurs. So the device returns to its high resistance state (HRS) as the filament breaks and the Ag is deposited back to the top electrode [44].

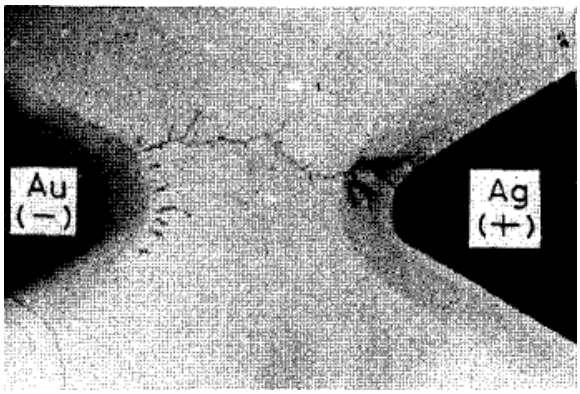


Fig. 2: Silver dendrite bridging of the gap [44]

Fig. 3 is showing how the PMC memory works [49]. When the voltage increases silver oxidizes at the anode and migrates under the electric field to reduce on the cathode ((A) write operation). A silver conductive filament starts to form on the cathode. By increasing the applied voltage, gap will be bridged and. current flow instantly increases, due to a much lower resistance path between the two electrodes which is provided by the conductive fillament. ((B) written device).

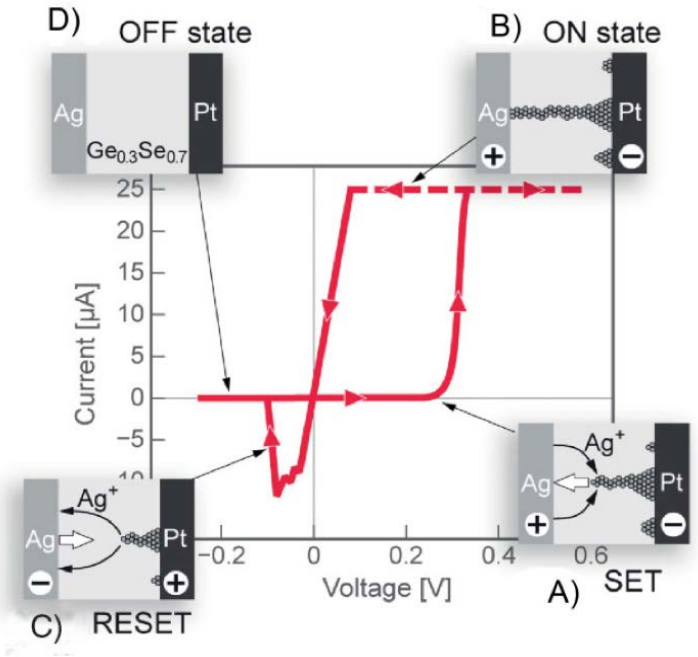


Fig. 3: PMC device operation [49].

In Fig. 3, as it can be seen the compliance current is set to 25μA. Then by reducing the applied voltage, the filament acts like a resistor and the current-voltage response would be linear at lower voltages. When the applied voltage gets more negative, the silver oxidizes from the filament and migrates back toward the Ag anode until a gap opens in the filament, and silver no longer bridges the electrodes. So the current instantly drops ((C) reset operation). Applying more negative voltages causes most silver returns to the anode ((D) erased device). The resistance of the written state is usually many orders of magnitude lower than that of the erased state, allowing the device to behave as memory [49].

By changing the compliance current, multiple resistance states have been demonstrated [50]. Higher current results in more radial growth of the filament. The filament formation and the redial growth is shown in Fig. 4 [50]. Multiple resistance states mean that we can have multibit storage per cell.

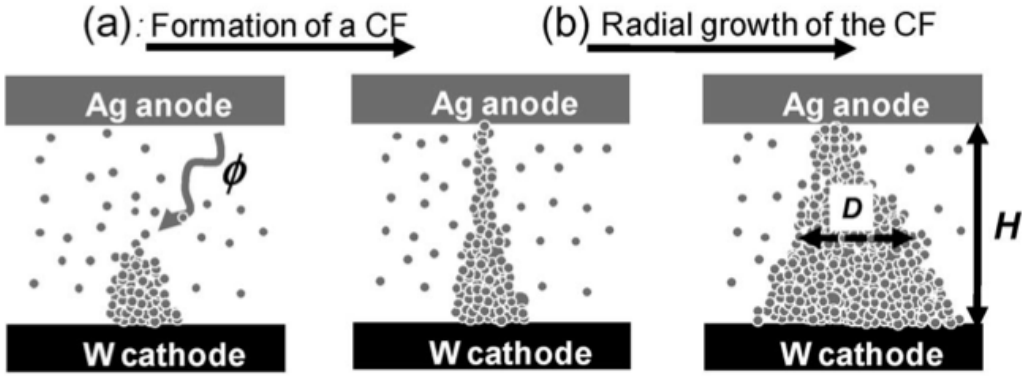


Fig. 4: Filament formation and subsequent radial growth [50].

Possibility of multiple resistance states, means having quantized conductance [51]. The fundamental conductance is $G_0 = 2e^2/h$ and Conductive values may be in multiples of that [51], and it means conductive filaments can be as small as one atom wide. Figs. 5 and 6 are showing the possibility of radial growth of the filament for very low written resistances. It may take more time or voltage to erase for devices with large filament and with large amount of silver. The required time for erasing the cell is depended both on the written resistance and erase voltage of the device [52]. It can be seen from Figs. 5 and 6 that lower erase voltages result in longer erase times [52].

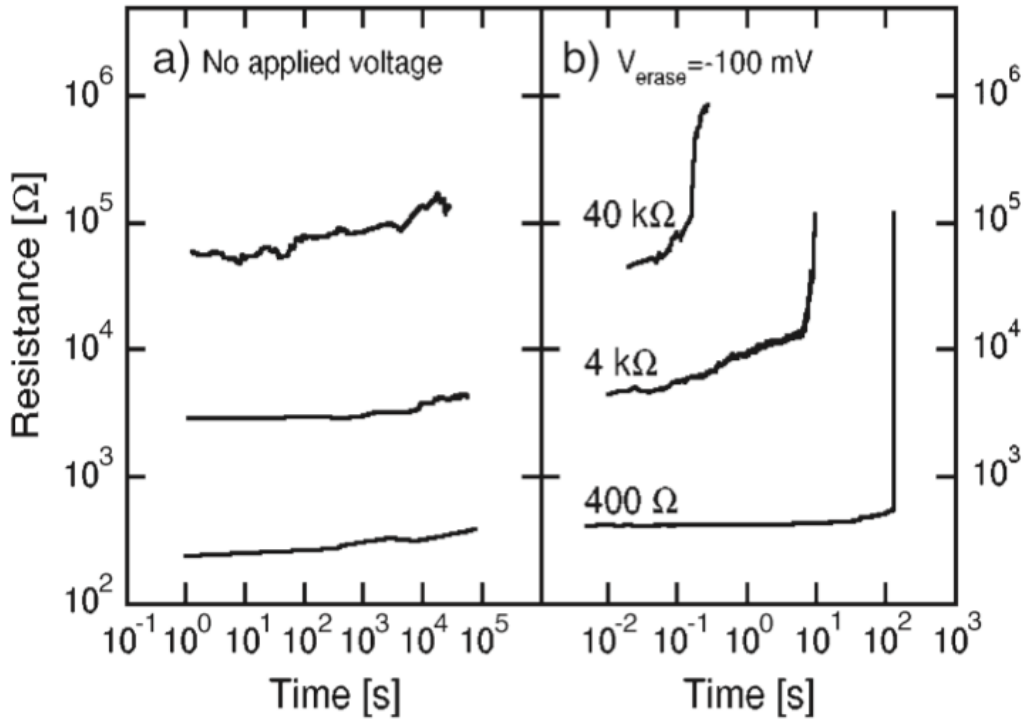


Fig. 5: Erase time required based on written resistance [52].

In many cases, chalcogenide memory is fabricated as a binary chalcogenide, such as Ge_xSe_y. At first write, since Ag migrate the entire gap, it may take more time. For next write operations, since the path has already been formed, it may be faster. Higher silver incorporation into the memory layer speeds up the first write operation [53].

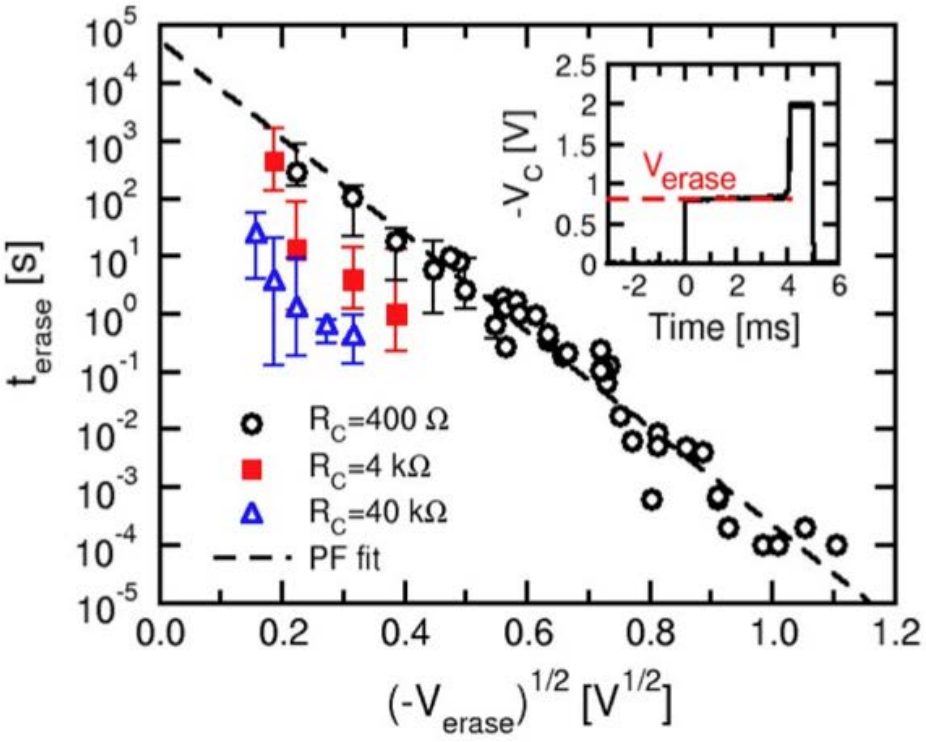


Fig. 6: Time required to erase based on erase voltage [52].

When the device's gap has been bridged, the resistance characteristics are metallic; while in the erased state, the resistance characteristic acts as a semiconductor [44]. The conduction characteristic is important because it strengthens the idea that there is a metallic filament acting as the semiconductor when the device is written. In the erased state, there is no metal conductor.

2.2. Theories of Conduction

Writing process is three steps. The first step is the oxidation at the anode Eq. (1).

$$Ag \rightarrow Ag^{+} + e^{-} \quad (1)$$

Next, ions migrate toward the cathode under an electric field. Finally, the ions reduce at the cathode Eq. (2).

$$Ag^{+} + e^{-} \rightarrow Ag \quad (2)$$

So the kinetics of silver ions motion are devided into two parts: the migration of ions through the chalcogenide memory layer modeled by the Mott and Gurney thermally activated ion hopping mechanism[53], and the Butler-Volmer equation modeling the anode and cathode reaction [54].

There is also electron flow in the chalcogenide layer during the write and erase operations. The electron flow mechanisms are [49]:

- Band conduction in the extended states
- Mott's $T^{\frac{1}{4}}$ variable range hopping
- Schottky emission
- Poole-Frenkel emission
- Fowler-Nordheim tunneling

2. 2.1. Metal ions: Butler-Volmer Equation for Electrode Redox[49]

Eq. (3) is the Buttler-Volmer equation, which describes the current when there is oxidation at anode and reduction at cathode [15].

$$I = I_0[\frac{C_0(0,t)}{C_0^*}\exp\left(\frac{a\eta}{kT/q}\right) - \frac{C_r(0,t)}{C_r^*}\exp\left(-\frac{(1+a)\eta}{kT/q}\right)] \quad (3)$$

where I_0 is the exchange current, defined as the equilibrium current from either electrode (the net current flow is zero), and the transfer coefficient α is a 0-1.0 fitting parameter η is the overpotential defined as the potential difference between the applied voltage and zero current equilibrium potential. The PMC device has no current at zero applied potential, so the overpotential is equal to the applied potential to the device. Q is the ion charge. For Ag^{+}, it is the elementary charge multiplied by one. $\frac{C_0(0,t)}{C_0^*}$, while $\frac{C_r(0,t)}{C_r^*}$ are the relative surface to bulk concentrations at electrodes. The other exponential term is the anode current. In Fig. 7 the individual cathode and anode current are shown in the typical Butler-Volmer current-overpotential plot [54].

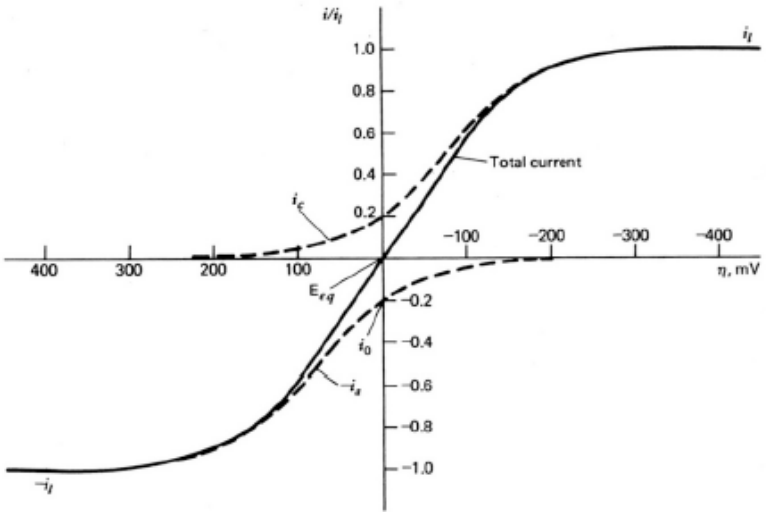


Fig. 7: Butler-Volmer current-overpotential curve showing cathode and anode and total current (i_c and i_a) [54].

2.2.2. Metal Ions: Mott-Gurney Hopping [49]

The ion-transfer process is based on Mott-Gurney hopping [55]. The ion current density-electric field equation for ion hopping is shown in Eq. (4).

$$J = 2qCav.\exp\left(-\frac{w_a^0}{kT/q}\right).\sinh\left(\frac{aE}{2kT/q}\right) \quad (4)$$

The equation consists of the concentration of mobile cations C, the hopping rate v, the hopping distance a, and the energy barrier w_a^0. The hyperbolic sine tends to an exponential at high electric fields, as shown in Eq. (5) [53].

$$J = 2qCav.\exp\left(-\frac{w_a^0}{kT/q}\right).\exp\left(\frac{aE}{2kT/q}\right) \quad (5)$$

For low electric fields, the equation will have a linear dependence on the electric field, as shown in Eq. (6) [53].

$$J = \frac{qa^2Cv}{kT/q}.E.\exp\left(-\frac{w_a^0}{kT/q}\right) \quad (6)$$

3. EXPERIMENT

3.1. Fabrication

The PMC devices studied in this work are integrated onto a test chip, designed and fabricated at Arizona State University's Center for Applied Nano Ionics. The fabrication procedure is as follows:

PMC devices are fabricated on a 100mm (diameter) 0.5mm (thick) p-type Silicon wafer. First, the wafer goes through standard cleaning processes (Acetone and IPA rinse followed by dehydration bake at 120C for 5 minutes). Then, it is loaded into an e-beam evaporator tool (Lesker PVD75 E-beam Evaporator) for deposition of oxide and metal stack (100nm of SiO_2, 100nm of Ni and again 100nm of SiO_2).

The intermediate Ni layer acts as device cathode and the top SiO_2 layer is used for isolation. Then, a photolithography step is performed to pattern the substrate for forming device via(s) on the top SiO2 isolation layer. It then goes through a wet etch step to expose the Ni layer in the via regions. The vias are used either as contact holes to the Ni electrode, i.e., cathode vias, or as "device" vias which define the active area of the PMC. After etching, a second photolithography step is performed to pattern the substrate for deposition of 60 nm $Ge_{30}Se_{70}$ and 30 nm Ag films. These films are deposited on the vias using a thermal evaporator (Cressington). The wafer is then exposed to UV light (λ = 324 nm, E = 3.82 eV) for 1 hour at a power density of 10 mW/cm^2 in order to allow Ag photo-doping of the chalcogenide film. Photodiffusion of silver is one of the most interesting effects that occur in chalcogenide glass films as it dramatically changes the properties of the starting material [20, 21]. Exposing PMCs to UV light causes Ag incorporation from the anode into the chalcogenide glass. This photo-induced doping changes the electric properties of the glass from dielectric to solid-state electrolyte and ensures repeatable switching behavior [22-24]. An additional 35 nm of Ag is then deposited on top of the silver-doped $Ge_{30}Se_{70}$ layer to create the device anode. A lift off and the third photolithography step follows by to pattern the substrate for final metal pad depositions. For the current devices, a stack of 800nm Al, 10nm of Cr and 150nm of Au is used to form the metal pads. The metal pad formation step completes with a final lift off step which prepares the device ready for a post processing annealing step at 120° C for 60 minutes.

As we know, bias-dependent transport of Ag (or Cu) ions, via the application of a voltage or current across the electrodes, and electrochemical reduction-oxidation (redox) reactions allow Ag- or Cu-rich

filaments to be grown or dissolved in the active film where ions conduct [63-70, 71-74]. In order to reduce the energy needed for filament growth or dissolution, electrochemically active metal is typically introduced into the film during fabrication when a metal/glass bilayer is exposed to light in a process known as photo-doping. Exposure to photons of ultra-violet (UV) light causes metal to diffuse into the film and form ternary phases that extend into the film from the active metal side. Within this photo-doped, metal-rich region, the film resistivity is many orders of magnitude less than undoped glass [75]. However, even with metal concentrations as high as tens of atomic percent, these metal doped chalcogenide films have resistivities that are still many orders of magnitude higher than the metallic filaments [76].

After a typical photo-doping process involving Ag and a ChG, the resulting structure comprises an Ag-rich ternary layer extending from the active Ag anode and a region of relatively undoped (high resistivity) glass, as illustrated in Fig. 8. Photo-doping can be used in PMC processing to produce such a layered structure and thereby reduce the span of undoped material over which a filament must be grown. Reducing the thickness of material to be bridged decreases the switching voltage and filament formation time.

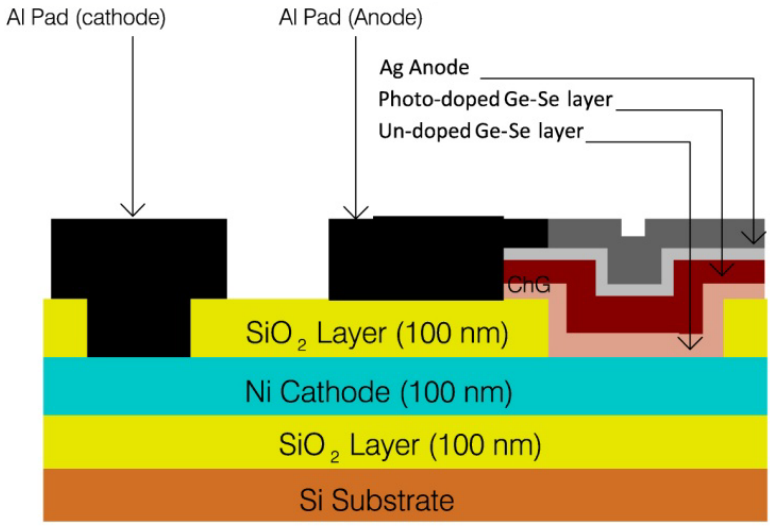


Fig. 8: Illustration of PMC device cross-section with Ag anode, Ni cathode and chalcogenide (ChG) layer showing the two layer photo- and unphoto-doped ChG structure.

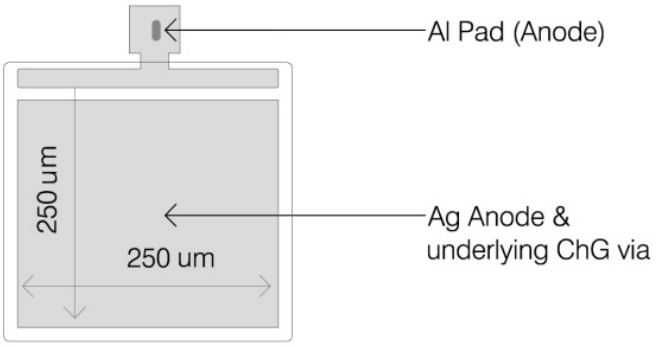


Fig. 9: Top (planar) view of a PMC device with via dimension 250 µm by 250 µm.

Fig. 8 illustrates a cross section of the PMC device. Fig. 9 shows the top-view of a PMC test device with via dimension of 250 µm by 250 µm. Such relatively large devices were used to reduce the effects of parasitics in the probe pads and metallization.

Photo-doping of silver into the ChG film dramatically changes the properties of the material [77, 78]. Fig. 10 shows the Ag atomic profile along the cross section of the PMC device after the photo-doping process, where the solid line represents the actual data obtained from energy dispersive spectroscopy (EDS) measurements, and the dashed line represents the trend line. The inclusion of Ag into the ChG film changes its electrical properties from dielectric to solid-state electrolyte. This improves the material stability and repeatability of resistive switching [79-81]. Capturing the impact of Ag incorporated into the glass is critical to accurate parameterization of the PMC device.

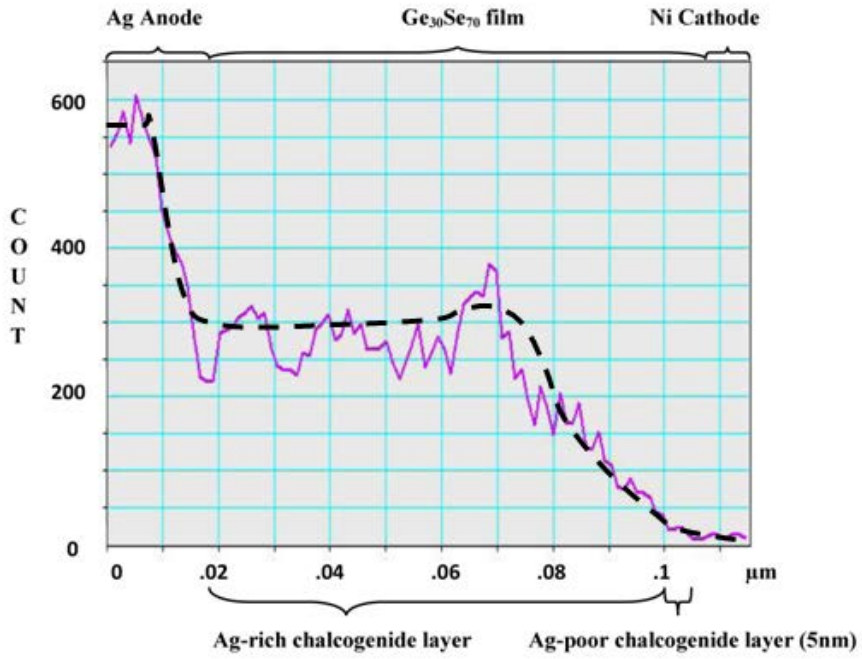


Fig. 10. Atomic profile of Ag along the PMC device obtained from EDS measurements, showing low Ag count near the cathode side.

3.2. Characterization

The data shown in Figs. 11 and 12 were obtained from measurements on a PMC device integrated onto a test chip, designed and fabricated at Arizona State University's Center for Applied Nano ionics. Current versus voltage (I-V) data (Fig. 11) is recorded by an Agilent 4156C Precision Semiconductor Parameter Analyzer. The test performed is a double DC voltage sweep from -0.5V to 0.5V and back to -0.5V with 5 mV steps at a rate of 1 V/s and a compliance current limit of 50 µA. The PMC is initially OFF, switched to ON and then returned to OFF. The write and erase threshold voltages for this device are approximately 150 mV and -60 mV, respectively. The OFF resistance is 36.6 MΩ at 10 mV. The ON resistance is 26.2 kΩ at 10 mV. The OFF/ON resistance ratio is 1.40E3. Note that when the current is at the 50 µA limit the displayed voltage continues along the set DC sweep, but the actual voltage is reduced. The R-V data in Fig. is calculated with the displayed voltage and is therefore erroneous where the current is limited.

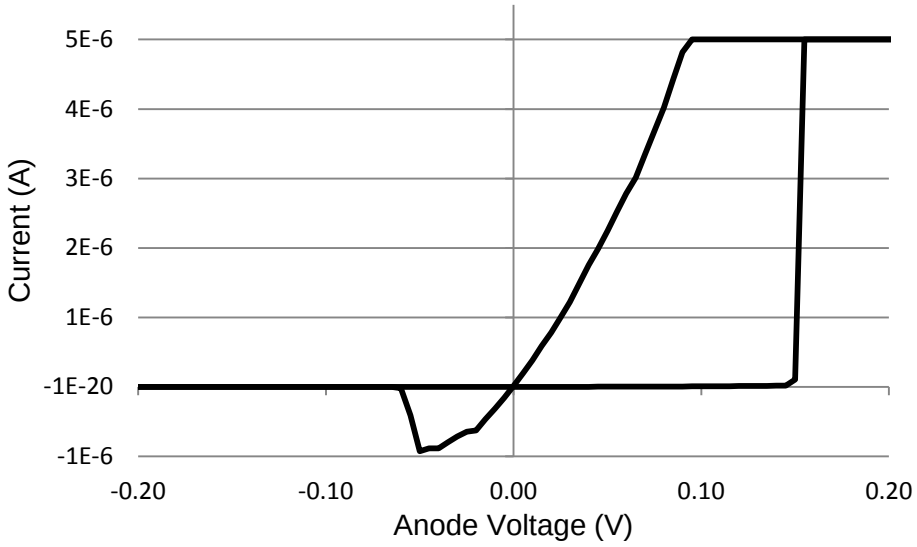


Fig. 11: PMC I-V characteristic

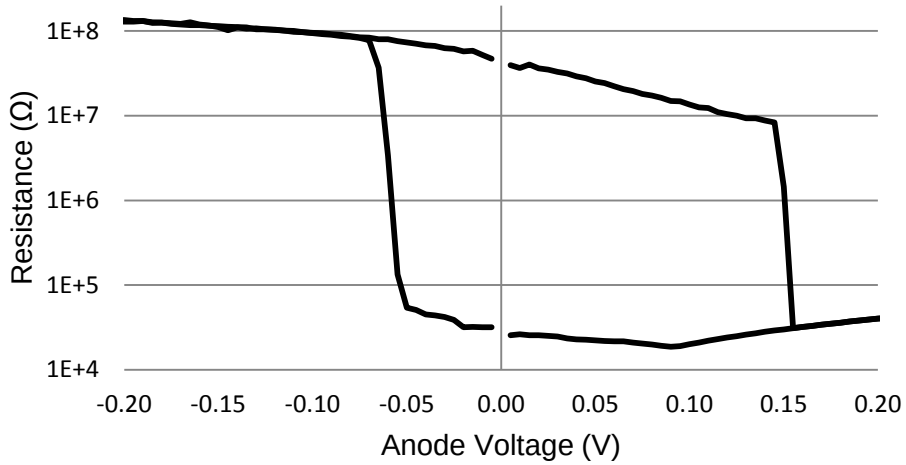


Fig. 12: PMC R-V characteristic

The impedance spectra data on PMC devices with three different via diameters (250 µm, 400 µm and 500 µm) are obtained using an Agilent 4284A LCR meter for the frequency range of 20 Hz to 1 MHz with an AC small signal voltage of 10 mV_{RMS} applied across the device in both HRS and LRS.

Electrochemical impedance spectroscopy (EIS or IS) has been previously used to characterize different nano-devices and thin films [82-85]. Here the impedance spectra data are plotted as Cole-Cole plots for PMC devices in both HRS and LRS.

In Cole-Cole plots [86-88], the negative of the imaginary part of the impedance is represented as a function of the real part of the impedance. Figs. 13 and 14 show the Cole-Cole plots obtained for devices with three different via diameters in both HRS and LRS, respectively.

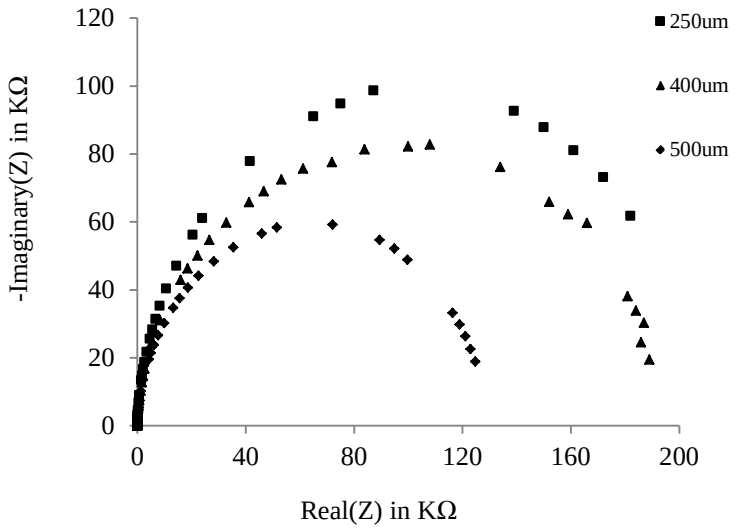


Fig. 13: Measured HRS impedance spectra of PMC devices for three different via diameters (250 µm, 400 µm, 500 µm)

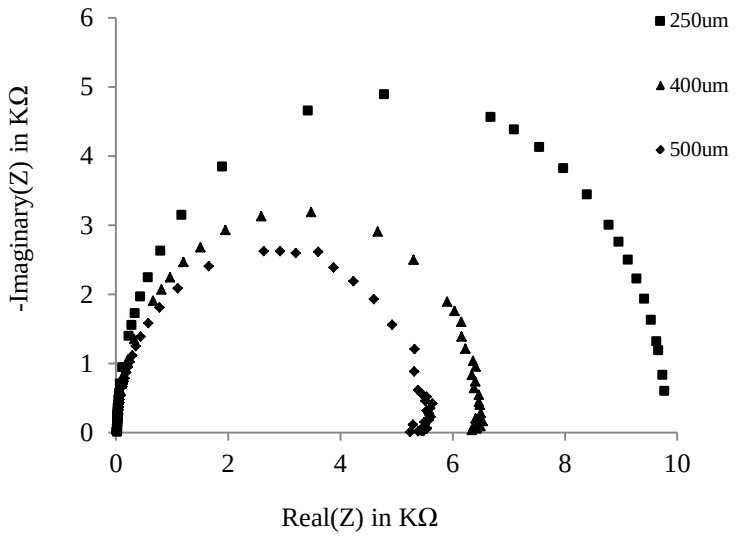


Fig. 14: Measured LRS impedance spectra of PMC devices for three different via diameters (250 µm, 400 µm, 500 µm)

4. SIMULATION AND MODELING

Material parameters associated with both the Ag-rich (photo-doped) and Ag-poor (unphoto-doped) layers in the ChG film are not well known. A precise physical model that captures the electrical behavior of the PMC in both its low-resistance on-state (LRS) and high resistance off-state (HRS) has therefore yet to be developed.

The primary objective of this work is to model the PMC with a device simulator and extract material parameters associated with the ChG film when the device is in its HRS and LRS.

Extraction is performed by adjusting these parameters, which include material bandgaps, affinities, dielectric constants, carrier mobilities and effective state densities, in order to fit simulation results to electrical data on actual PMC devices. These extracted values are compared to first principles calculations on GeSe films, as well as results reported in literature. Obtaining an accurate set of material parameters for both Ag-rich and Ag-poor ChG systems enables greater fidelity in PMC device simulation, which significantly enhances our ability to understand the underlying physics of ChG-based resistive switching memory.

4.1. Parameter Extraction Approach

After processing, the PMC structure may be described as a non-uniformly doped electrolyte with a significantly reduced Ag doping concentration close to the bottom Ni electrode. As can be seen from the Ag atomic profile shown in Fig. 12, the Ag concentration in the $Ge_{30}Se_{70}$ is relatively low up to 5 nm from the cathode contact. This low Ag concentration will result in a high resistivity layer which will dominate the off state resistance of the PMC. During the write process (HRS to LRS switching), Ag^{+} ions from the anode and from the Ag-rich photo-doped layer contribute to the formation of the metal filament along the length of the device, included in the lightly-doped region.

In order to extract parameters for the film in both its HRS and LRS, the ATLAS device simulator from the Silvaco suite of simulation tools is used to perform three-dimensional finite difference modeling on the structures. For the HRS case, two layers are defined, one Ag-rich region (Ag-$Ge_{30}Se_{70}$) with 55 nm thickness and one Ag-poor (un-photodoped $Ge_{30}Se_{70}$) with a thickness of 5 nm. For the LRS model, the

structure must be modified to include another region as a grown conductive Ag filament across both layers in the electrolyte. The diameter of this filament in the model is estimated at 5 nm from the on-state resistance data and conductivity values obtained for Ag filaments at room temperature from previous works [89, 90].

The cylindrical TCAD structures used for the HRS and LRS models are shown in Figs. 15 and 16.

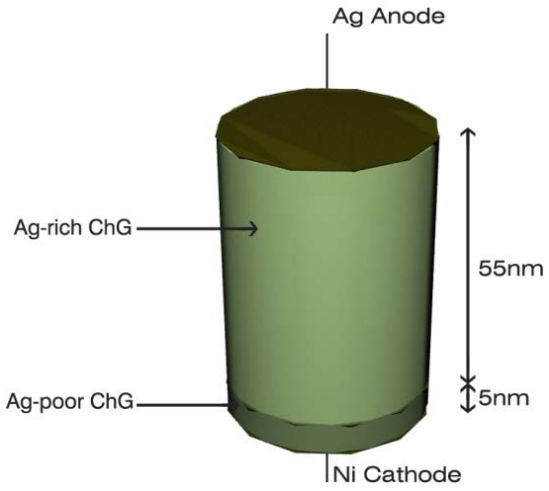


Fig. 15: The PMC off-state (HRS) model

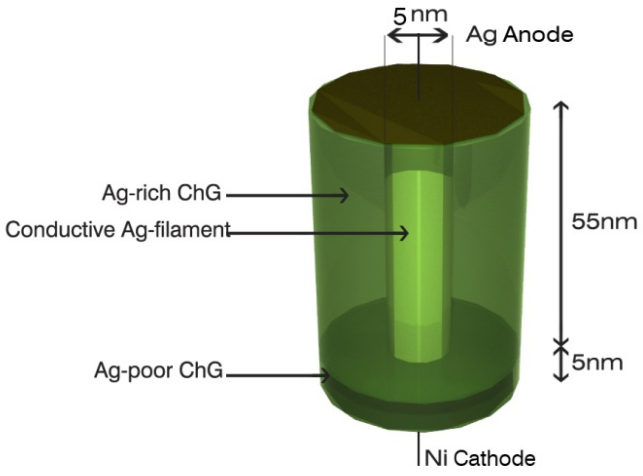


Fig. 16: The PMC on-state (LRS) model

Finally, in order to complete parameterization, both HRS and LRS device conditions are modeled with the RC networks (Fig. 17). Fig. 17(a) shows that when the PMC is in the HRS, it can be modeled as a passive RC network composed of two parallel RC configurations. The HRS RC configuration composed of R1 and C1 determines the impedance of the photo-doped layer of the chalcogenide film. The R2 and C2 configuration is related to the un-photodoped chalcogenide layer.

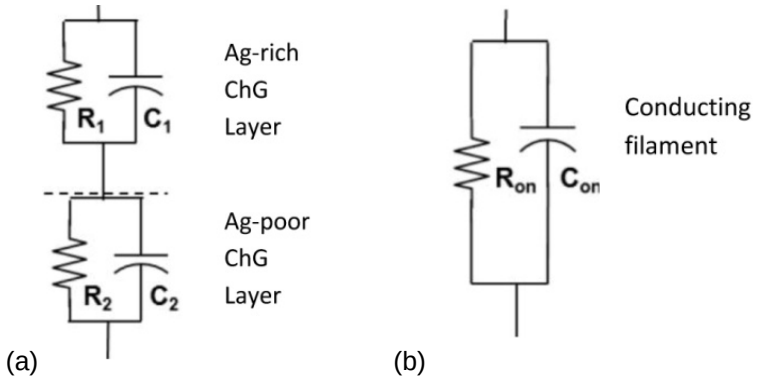


Fig. 17: Equivalent RC circuits of : (a) HRS PMC with R_1, C_1 associated with the Ag-doped ChG layer and R_2, C_2 associated with the undoped ChG layer, (b) LRS PMC with R_{on}, C_{on} associated with the conductive filament.

In the LRS, the resistance across the chalcogenide film can be assumed to be dominated by the resistance of the conductive filament and thus the LRS PMC can be modeled as one parallel RC circuit as it is shown in Fig. 17(b).

By fitting the HRS and LRS equivalent circuit impedance formulas to the experimental data, all resistance and capacitance values related to the Ag-poor, Ag-rich and conducting filament regions can be extracted. After extraction of the equivalent RC network parameters in both HRS and LRS, parameters for doped and un-doped ChG films are determined by adjusting material constants used by the simulator in order to fit the extracted resistance and capacitance values. These constants include bandgap, density of states in conduction and valence bands, affinity, intrinsic carrier concentration, electron and hole mobility and dielectric constant for the Ag-rich and Ag-poor regions as well as the filament parameters in the LRS case.

4.2. Results

All the resistance and capacitance values related to the Ag-poor chalcogenide, Ag-rich chalcogenide, and conducting filament layer for PMCs with via diameters of 250 µm, 400 µm and 500 µm are obtained from the data and reported in Table IV.

Table IV: The HRS and LRS passive elements of the PMC equivalent RC circuit model for different via sizes

Via Diamater Size	250µm	400µm	500µm
$R_1(\Omega)$	5×10^3	4.8×10^3	2.1×10^3
$R_2(\Omega)$	2×10^5	1.8×10^5	1.2×10^5
$C_1\ (F)$	2×10^{-8}	3.5×10^{-8}	7.7×10^{-8}
$C_2(F)$	3.6×10^{-9}	9.1×10^{-9}	1.3×10^{-8}
$R_{on}(\Omega)$	9.8×10^3	6.4×10^3	5.3×10^3
$C_{on}(F)$	2.9×10^{-9}	7.2×10^{-9}	1.1×10^{-8}

From capacitance values, the dielectric constant of each photo-doped (Ag-rich) ChG layer and unphotodoped (Ag-poor) ChG layer can be obtained using the Eq. (7)

$$C = \frac{k\varepsilon_0 A}{t_l} \tag{7}$$

Where, A is the via/device area, t_l is the thickness of that layer, and k is the semiconductor dielectric constant used in that layer.

The on-state resistance for all the PMCs with three different via sizes does not seem to be strongly dependent on via size. This non-scalability can be attributed to the fact that R_{on} is determined by the

resistance of the conductive Ag-filament formed across the film, which is likely independent of the device area. So in our simulation an Ag metallic filament with 5 nm diameter and conductivity of 5×10^3 $\Omega^{-1}cm^{-1}$ [89, 90] is used to model the LRS resistance across the chalcogenide film. The filament diameter is calculated from Eq. (8)

$$d = 2\sqrt{\frac{\rho.l}{\pi.\mathrm{R_{on}}}} \tag{8}$$

Where, ρ is the filament resistivity, *l* is length of the filament, and $\mathrm{R_{on}}$ is the on-state resistance.

By adjusting the material parameters used by the ATLAS simulator to fit the experimental data, parameters for the Ag-rich and Ag-poor regions have been extracted and reported in Table V. These values are in good agreement with those from previous works [89-95]. For example, the bandgap and affinity difference between Ag-poor $Ge_{30}Se_{70}$ and Ag-rich $Ge_{30}Se_{70}$ regions is 0.3 eV which is similar to values reported in [92].

Effective densities of states were obtained from density functional theory (DFT) calculations, in the generalized gradient approximation, applied to crystalline $GeSe_2$. We used QUEST, a local orbital code that uses double-zeta-quality basis functions plus polarization basis elements. We also used the Perdew-Burke-Ernzerhoff (PBE) exchange-correlation functional [96], Hamann pseudopotentials [97], and Monkhorst-Pack k-space gridding [98].

The effective density of states was obtained from equations in standard semiconductor theory (see, for example, Ref. [99]), starting from Eq. (9) which is valid in the conduction band.

$$n = \int_{E_c}^{\infty} n(E).f(E)d(E) \tag{9}$$

Here $n(E)$ is the density of states in the conduction band, $f(E)$ is the probability of occupation, i. e. the Fermi-Dirac distribution function, and E_C is the energy at the conduction band edge. The standard analysis then assumes parabolic band structure, so that Eq. (10) can be written

$$n = \frac{2\,N_c}{\sqrt{\pi}} F_{\frac{1}{2}}(\eta_c) \tag{10}$$

Where N_c is an effective density of states, $F_{\frac{1}{2}}(\eta_c)$ is the order ½ of Fermi-Dirac integral, η_c is $(\varepsilon_F - E_c)/k_BT$, ε_F is the Fermi level, E_c is the energy at the conduction band edge, k_B is Boltzmann's constant, and T is the absolute temperature.

For non-degenerate semiconductors, Eq. (11) reduces to

$$n = N_c \exp(\frac{\varepsilon_F - E_c}{KT}) \quad (11)$$

There is an analogous expression for N_V, the effective density of states in the valence band. Because the band structure in Ge-Se compounds can be non-parabolic, we evaluated Eq. (9) using the calculated, DFT density of states (DOS), and then took advantage of Eq. (11) to evaluate N_C. Reliable values of N_C and N_V required a dense Monkhorst-Pack grid (2034 k-points in a 48-atom unit cell). The calculated DOS in the valence and conduction bands are shown in Fig. 19. The values used for N_C and N_V in the simulations reflect the slopes of each DOS function, which, in turn, reflect the curvatures at the respective band edges, shown in Fig. 18. As expected, the effective density of states in the valence band is much larger (~10X), reflecting the nearly flat valence band edge.

The intrinsic electron concentration reported in Table V is calculated using the obtained values for N_c and N_v as

$$n_i = \sqrt{N_c N_v} \exp(\frac{-E_G}{2KT}) \quad (12)$$

The charge carrier drift mobility values in low conductivity materials of disordered structure are independent of technology. In our model we assumed very low mobility for the electrons and a hole mobility of 100 cm^2/Vs at room temperature, which is similar to values reported in [95].

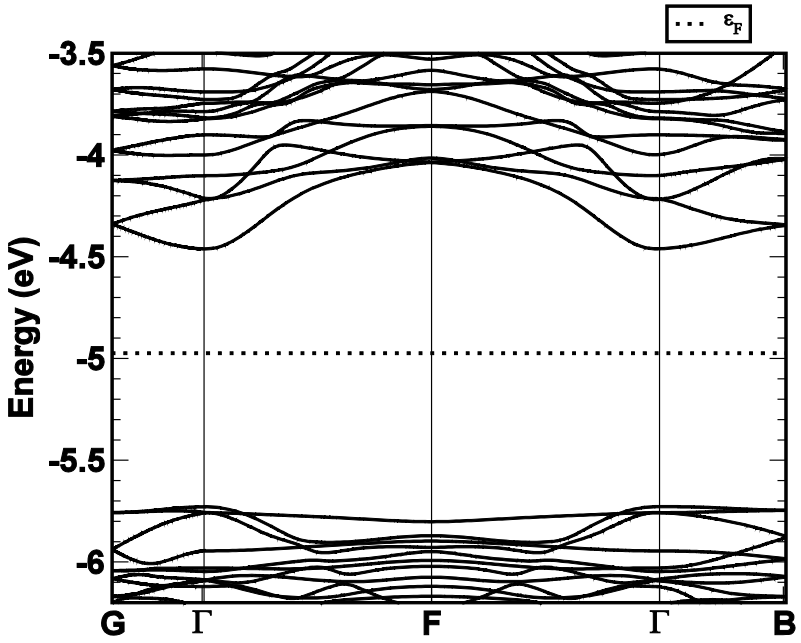
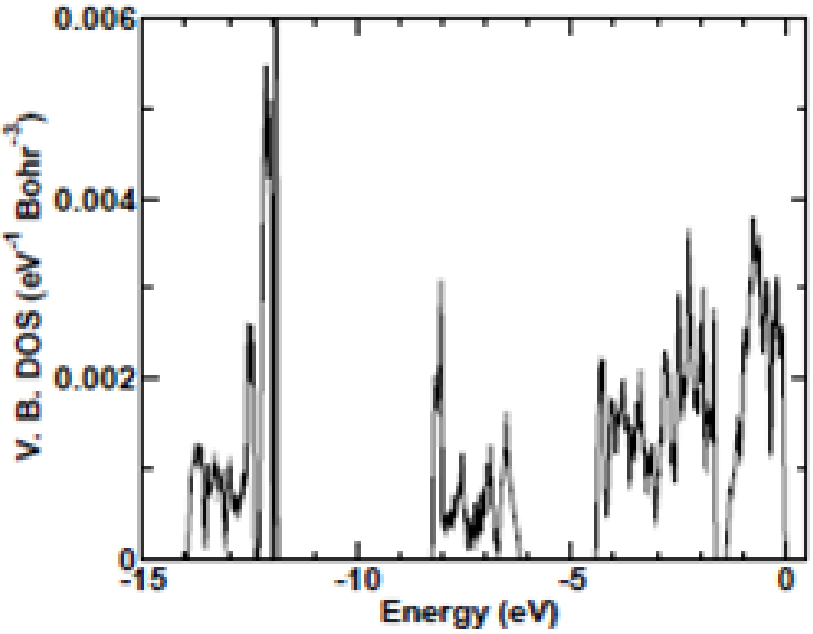
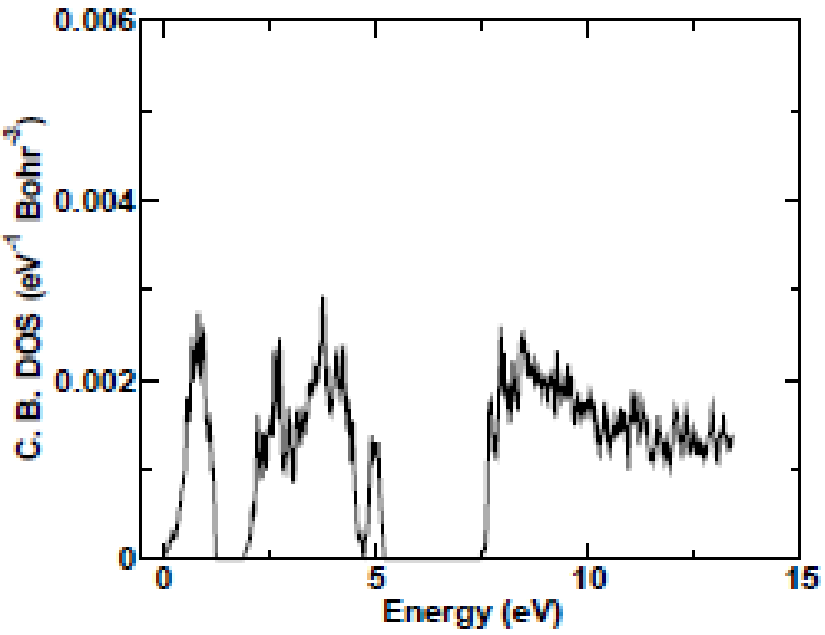


Fig. 18: DFT band structure for crystalline $GeSe_2$.



(a)



(b)

Fig. 19: Calculated DOS for crystalline GeSe2 in the valence band (a) and in the conduction band (b). In both cases the zero of energy is at the appropriate band edge.

Table V: The static device level parametric model for photodoped and undoped Ge30Se70

	Ag-poor $Ge_{30}Se_{70}$	Ag-rich $Ge_{30}Se_{70}$	Ag metallic filament
Bandgap (eV) [a]	1.86	1.56	_
Affinity (eV) [b]	3.05	3.35	_
Density of States in Conduction Band (per cc)	1×10^{19}	1×10^{19}	_
Density of States in Valence Band (per cc)	1×10^{20}	1×10^{20}	_
Intrinsic Carrier Concentration (per cc)	2.52×10^{6}	7.61×10^{3}	_
Electron Mobility (cm^2/Vs) [c]	1×10^{-5}	1×10^{-5}	_

Hole Mobility (cm^2/Vs) [d]	10	10	–
Dielectric Constant	40.9	1.7×10^3	–
Conductivity ($\Omega^{-1}. cm^{-1}$) [f]	–	–	5×10^3

The parameter values achieved in this work's model are in good agreement with those from below mentioned works:

a Ref. [91, 92]

b Ref. [93]

c, d Ref. [95]

f Ref. [89, 90]

Figs. 20-25 show the real and imaginary parts of the impedances versus frequency (from 10Hz to 1MHz) for both HRS and LRS of the simulated PMC devices with via diameters of 250 µm, 400 µm and 500 µm.

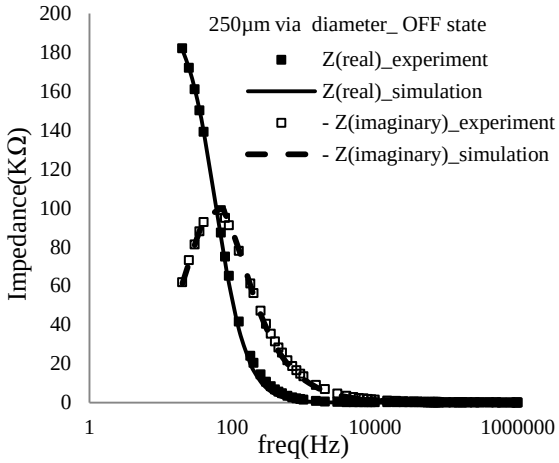


Fig. 20: The PMC simulated impedance

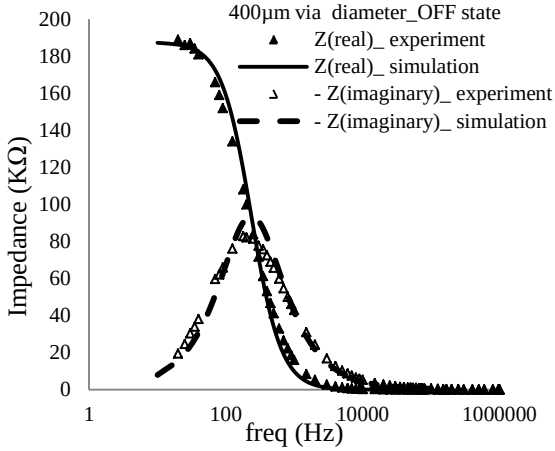


Fig. 21: The PMC simulated impedance

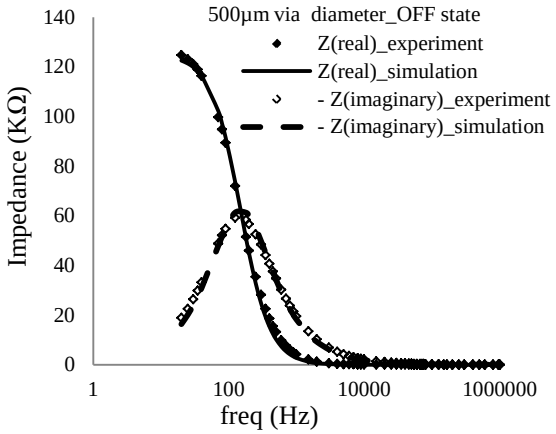


Fig. 22: The PMC simulated impedance

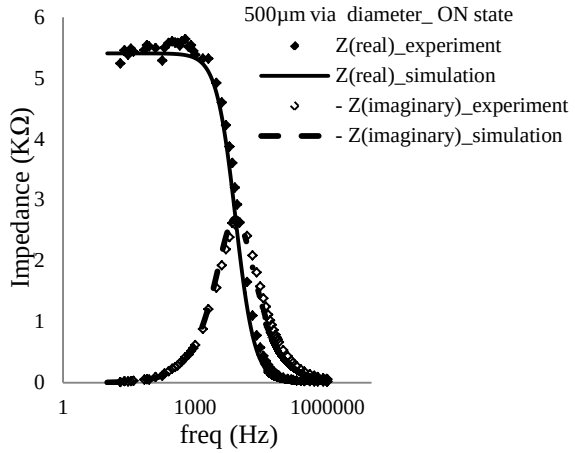


Fig. 25: The PMC simulated impedance

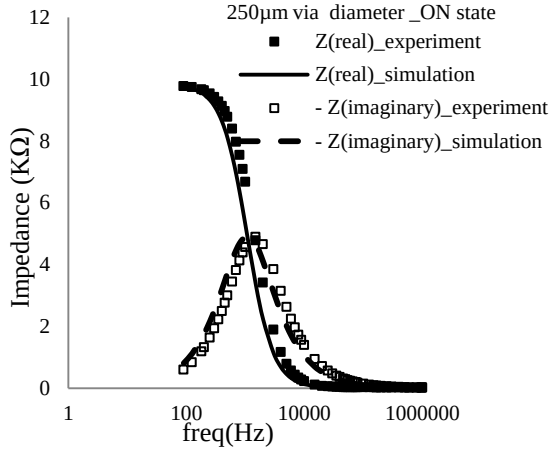


Fig. 23: The PMC simulated impedance

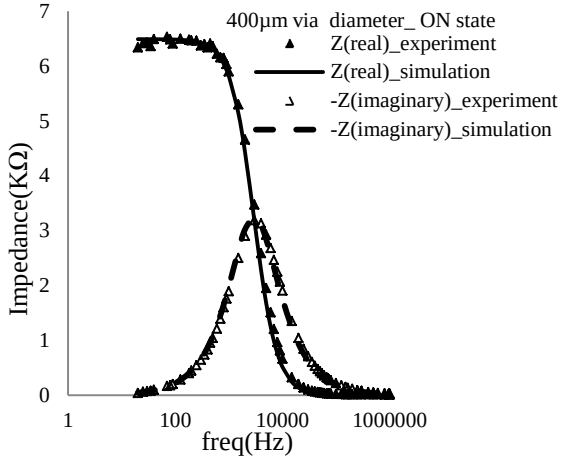


Fig. 24: The PMC simulated impedance

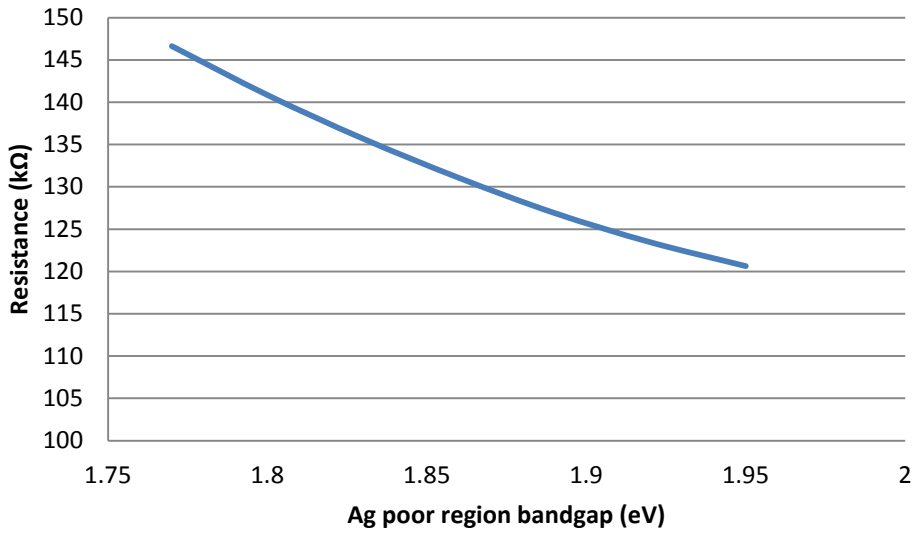
To see how well the simulation results are correlated with the impedance spectra data, the measured data are also shown on the same figures. At low frequencies from real part $R_1 + R_2$ for the off state and R_{on} for the on state can be extracted.

Since we know in a parallel RC circuit the maximum for the imaginary part happens at $\omega = \frac{1}{\sqrt{R\,C}}$, from figs. 27-32, C_1 , C_2 and also C_{on} can be estimated. The excellent fit between simulation and impedance experiment data shows the accuracy of our model in parametrizing the Ag-rich and Ag-poor $Ge_{30}Se_{70}$ material for next PMC static behavior studies.

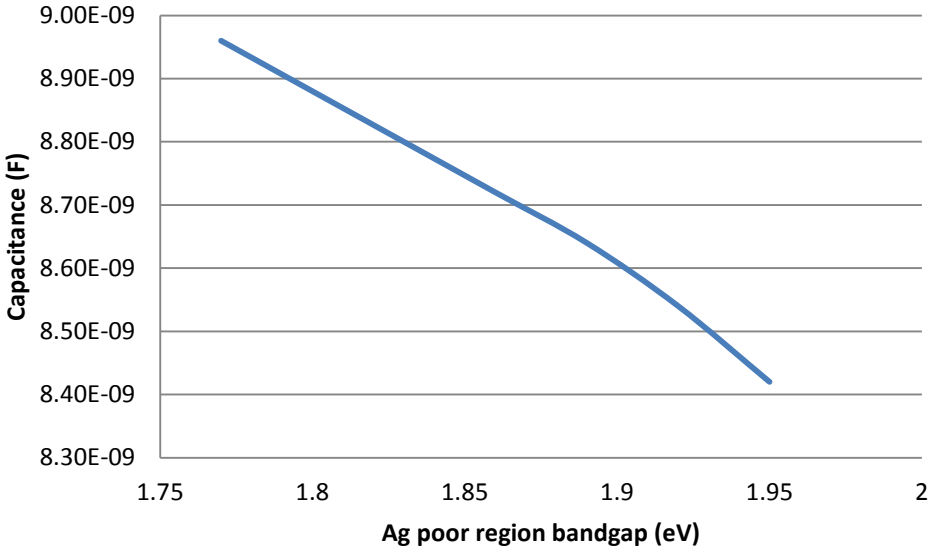
5. PROCESS VARIATION

The effects of process variation on the impedance behavior of the PMC devices through changing the prominent achieved material parameters of our model in this chapter have been studied. For the ON state, based on our simulations, the conductive filament resistance is dominant compared to Ag-poor and Ag-rich regions' resistances. Besides, the added filament does not change the capacitance values in comparison with the OFF state. Here we just see the effects of fluctuation of some of our presented model parameters on the impedance behavior of the PMC device.

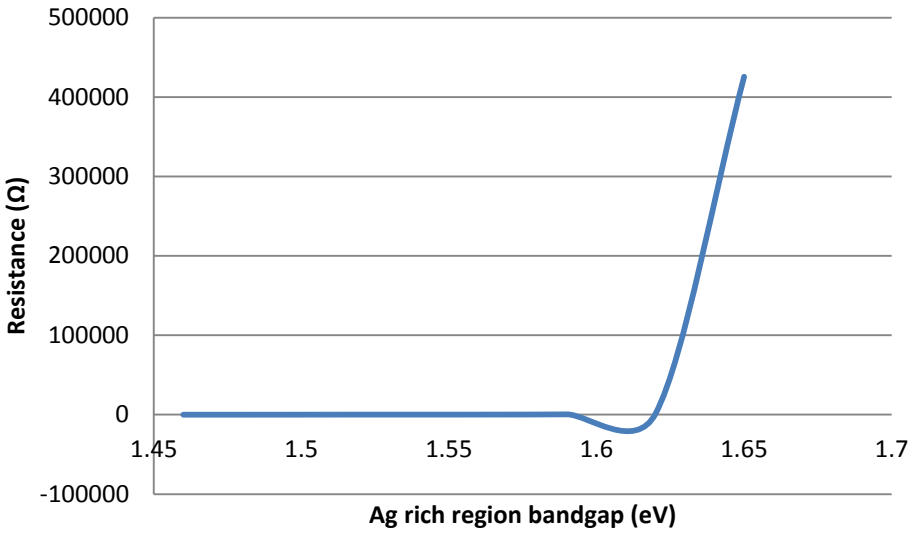
At first, the effect of bandgap fluctuation of each region is studied. By comparing Fig. 26(a) and Fig. 26(c), it can be concluded that the resistance dependency on the fluctuation of Ag-rich bandgap is dominant. This is because the thickness of Ag-rich region (55 nm) is much larger than that of Ag-poor region (5 nm). The bandgap fluctuation dependency of the capacitance for each region is shown in Fig. 26(b) and Fig. 26(d). The effect of fluctuation of affinity of each region on the resistance and capacitance is shown in Fig. 27. Based on Table V, the affinity of Ag-poor region (3.05 eV) is higher than that of Ag-rich region (3.35 eV). Therefore, by increasing the affinity of Ag-poor region, the conduction band of Ag-poor region approaches to that of Ag-rich region and consequently, the barrier height at the interface decreases. This is the reason of why the resistance reduces by increasing the Ag-poor affinity based on Fig. 27(a). On the opposite side, when the affinity of Ag-rich region increases, the barrier height at the interface of two regions increases, therefore; the resistance changes based on Fig. 27(c). In comparison with the affinity of Ag-poor region, the effect of Ag-rich affinity is dominant and significantly changes the resistance with several orders of magnitudes. Fig. 28 shows the effect of fluctuation for the permittivity of each region on the resistance and capacitance.


150
145
140
135
130
125
120
115
110
105
100
Resistance (kΩ)
1.75
1.8
1.85
1.9
1.95
2
Ag poor region bandgap (eV)

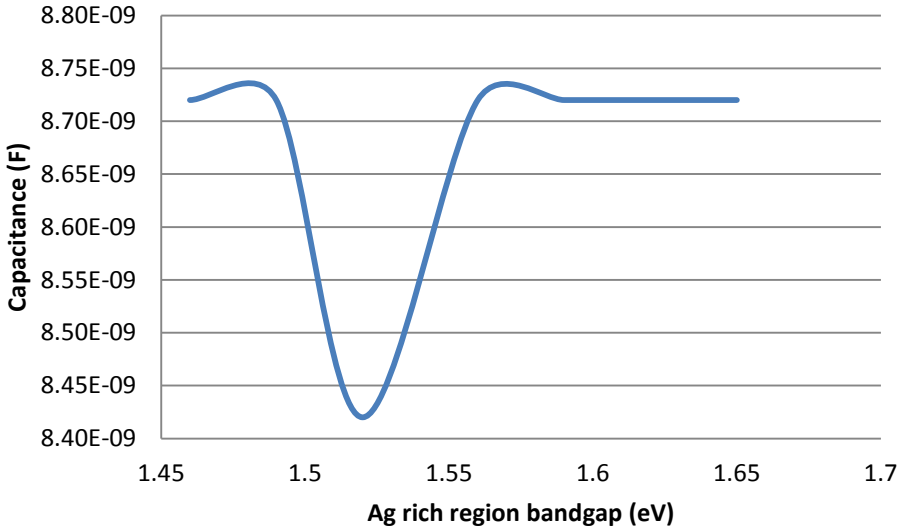
(a)


9.00E-09
8.90E-09
8.80E-09
8.70E-09
8.60E-09
8.50E-09
8.40E-09
8.30E-09
Capacitance (F)
1.75
1.8
1.85
1.9
1.95
2
Ag poor region bandgap (eV)

(b)

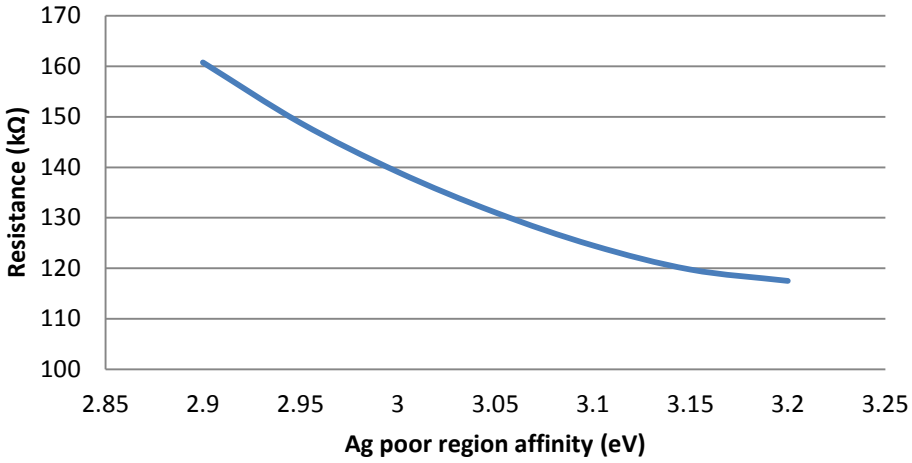


(c)

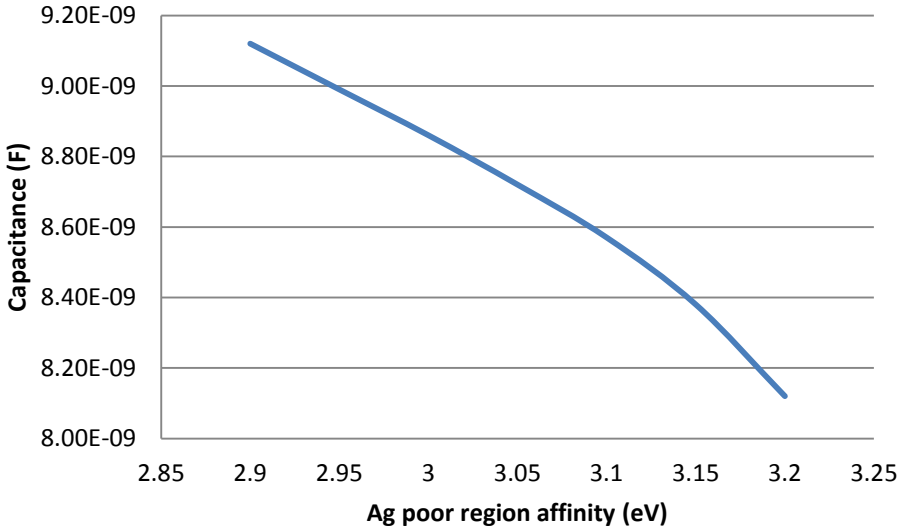


(d)

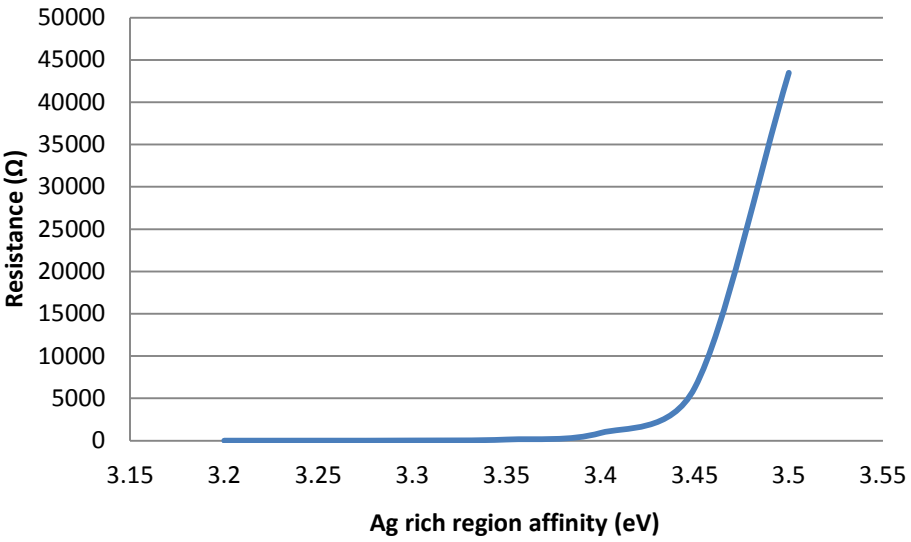
Fig. 26: Resistance and capacitance vs. bandgap of Ag-poor region in the OFF state (a, b), resistance and capacitance vs. bandgap of Ag-rich region in the OFF state (c, d).


170
160
150
140
130
120
110
100
Resistance (kΩ)
2.85
2.9
2.95
3
3.05
3.1
3.15
3.2
3.25
Ag poor region affinity (eV)

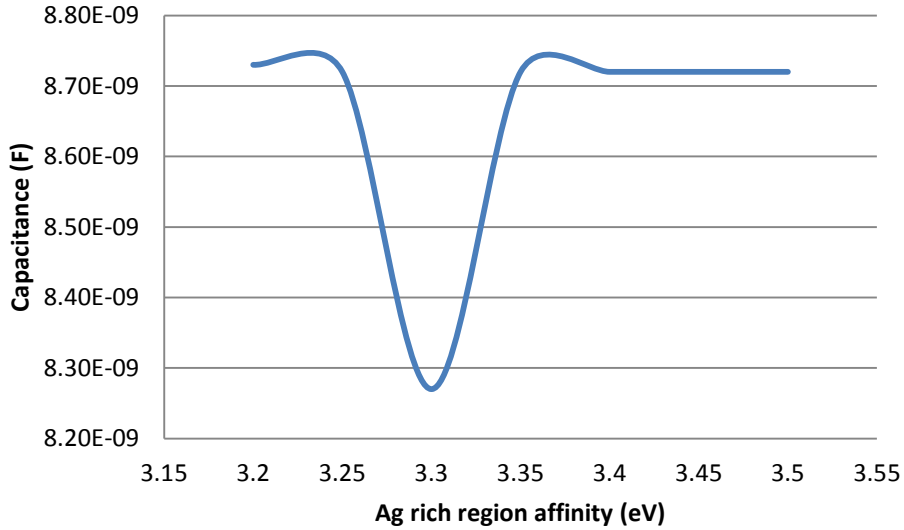
(a)


9.20E-09
9.00E-09
8.80E-09
8.60E-09
8.40E-09
8.20E-09
8.00E-09
Capacitance (F)
2.85
2.9
2.95
3
3.05
3.1
3.15
3.2
3.25
Ag poor region affinity (eV)

(b)

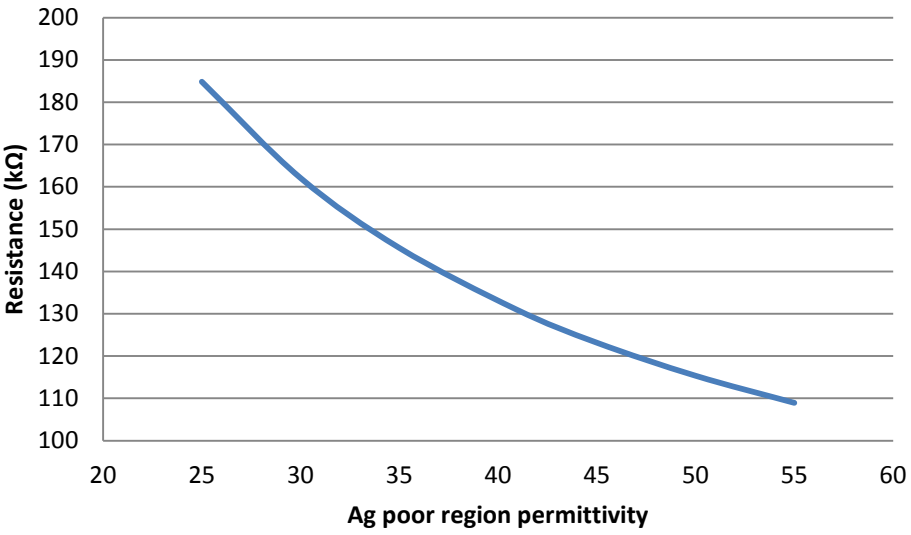


(c)

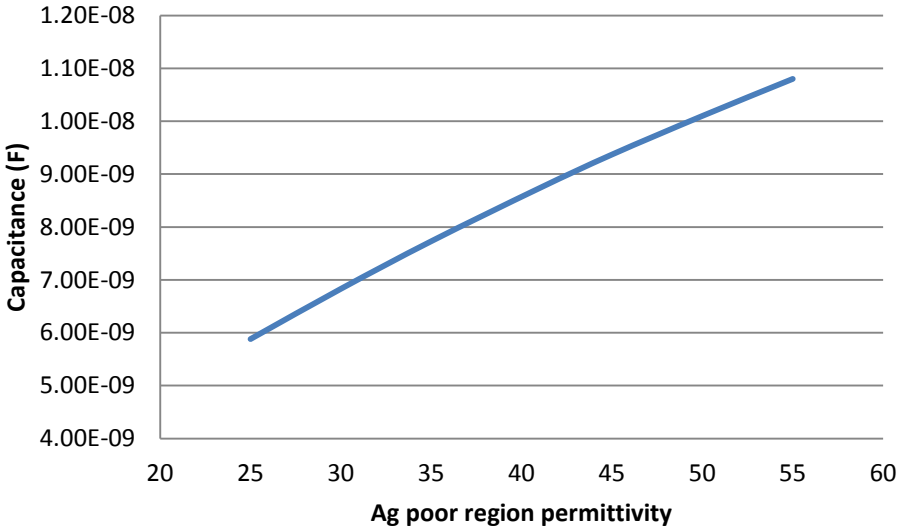


(d)

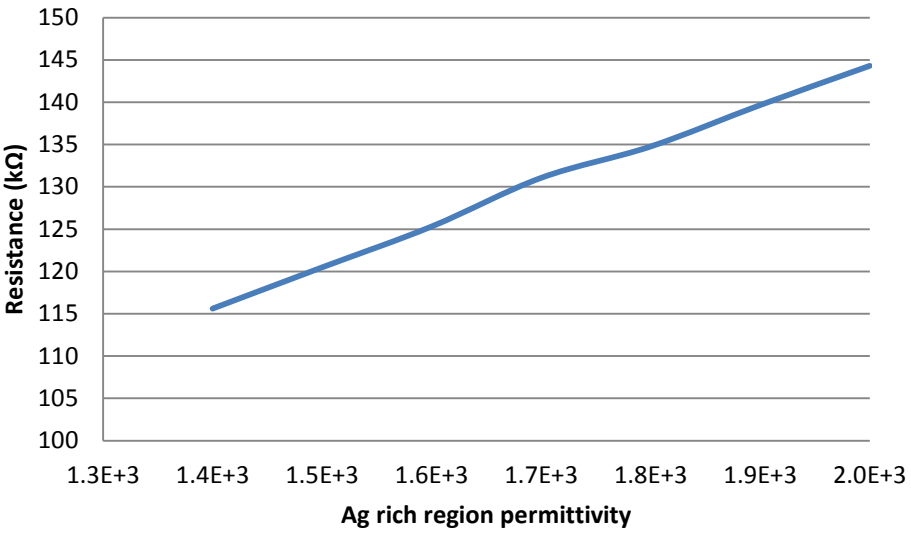
Fig. 27: Resistance and capacitance vs. affinity of Ag-poor region in the OFF state (a, b), resistance and capacitance vs. affinity of Ag-rich region in the OFF state (c, d)


200
190
180
170
160
150
140
130
120
110
100
Resistance (kΩ)
20
25
30
35
40
45
50
55
60
Ag poor region permittivity

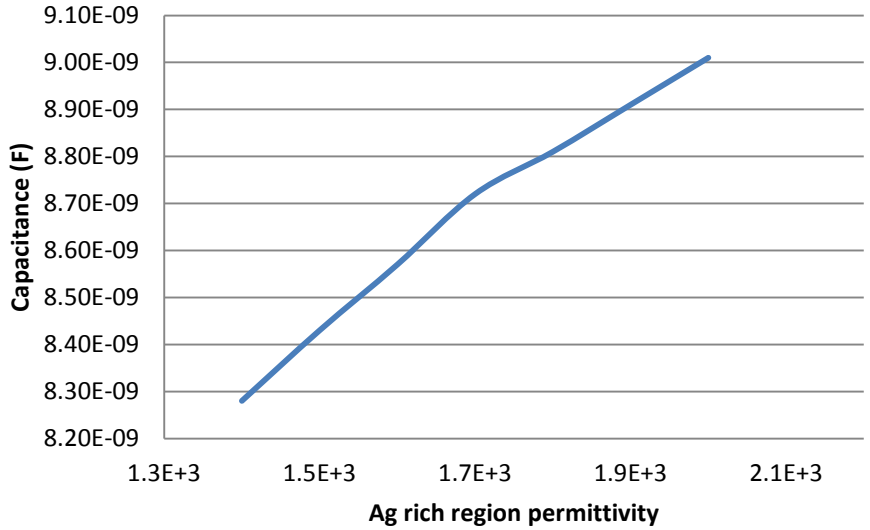
(a)


1.20E-08
1.10E-08
1.00E-08
9.00E-09
8.00E-09
7.00E-09
6.00E-09
5.00E-09
4.00E-09
Capacitance (F)
20
25
30
35
40
45
50
55
60
Ag poor region permittivity

(b)



(c)



(d)

Fig. 28: Resistance and capacitance vs. permittivity of Ag-poor region in the OFF state (a, b), resistance and capacitance vs. permittivity of Ag-rich region in the OFF state (c, d)

6. SUMMARY

In this work, we have developed and verified a precise physical model that captures the electrical behavior of programmable metallization cell devices in both their low resistance on-state and high resistance off-state. The parameter extraction has been performed by adjusting material parameters used for numerical device simulations to calibrate the model to the results of electrical measurements on actual PMC devices with different via areas.

The effects of process variation, which is an important consideration especially in nano-scaled memory devices, on the obtained parametric model for the static impedance behavior of the PMC memory for three different via sizes have been investigated. Among the parameters, the fluctuations of the Ag-rich ChG bandgap and affinity change the OFF-state resistance fundamentally.

Obtaining an accurate set of material parameters for both Ag-rich and Ag-poor ChG systems and investigating the process variation of the achieved model enables greater fidelity in PMC device simulation, which significantly enhances our ability to understand the underlying physics of ChG-based resistive switching memory.

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