Design Techniques For Ultra-Low Noise And Low Power Low Dropout (LDO) Regulators

by

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ABSTRACT

Modern day deep sub-micron SOC architectures often demand very low supply noise levels. As supply voltage decreases with decreasing deep sub-micron gate length, noise on the power supply starts playing a dominant role in noise-sensitive analog blocks, especially high precision ADC, PLL, and RF SOC's. Most handheld and portable applications and highly sensitive medical instrumentation circuits tend to use low noise regulators as on-chip or on board power supply. Nonlinearities associated with LNA's, mixers and oscillators up-convert low frequency noise with the signal band. Specifically, synthesizer and TCXO phase noise, LNA and mixer noise figure, and adjacent channel power ratios of the PA are heavily influenced by the supply noise and ripple. This poses a stringent requirement on a very low noise power supply with high accuracy and fast transient response. Low Dropout (LDO) regulators are preferred over switching regulators for these applications due to their attractive low noise and low ripple features. LDO's shield sensitive blocks from high frequency fluctuations on the power supply while providing high accuracy, fast response supply regulation.

This research focuses on developing innovative techniques to reduce the noise of any generic wideband LDO, stable with or without load capacitor. The proposed techniques include Switched RC Filtering to reduce the Bandgap Reference noise, Current Mode Chopping to reduce the Error Amplifier noise & MOS-R based RC filter to reduce the noise due to bias current. The residual chopping ripple was reduced using a Switched Capacitor notch filter. Using these techniques, the integrated noise of a wideband LDO was brought down to 15μV in the integration band of 10Hz to 100kHz. These techniques can be integrated into any generic LDO without any significant area overhead.

DEDICATION

Dedicated to my wonderful parents, my sweet sister and my dear friends..!!

ACKNOWLEDGMENTS

Firstly, my heartfelt and sincere thanks to my humble and charming advisor Dr. Bertan Bakkaloglu for providing me an opportunity to work on this valuable research project. His guidance and support during my Master's and this project, both technically and emotionally has been amazing. I am deeply grateful to him.

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CHAPTER 1
INTRODUCTION

1.1. Importance of Low Supply Noise

Modern era of communication is dominated by compact, portable and low cost smart phones and tablets. With technology scaling leading to deep sub-micron processes, large scale integration of analog, digital and RF blocks on to a single System-on-chip (SOC) has been the trend. While it benefits the digital design methodologies and allows adding extensive features on chip, helps in bringing down the area and cost, it has its own disadvantages towards Analog and RF blocks. Matching accuracy, lower overdrive, channel length modulation, higher parasitic and noise are a few to name.

As supply voltage decreases with decreasing deep submicron gate lengths, noise on the power supply starts playing a dominant role in noise-sensitive analog blocks, especially high precision ADC, PLL, and RF SOC's [1][10][11]. Most handheld and portable applications alongside highly sensitive medical instrumentation circuits tend to use low noise regulators as on-chip or on board power supply. Nonlinearities associated with LNA's, mixers and oscillators up-convert or intermodulate low frequency noise with the signal band. Specifically, synthesizer and TCXO phase noise, LNA and mixer noise figure, and adjacent channel power ratios of the PA are heavily influenced by the supply noise and ripple. This poses a stringent requirement on a very low noise power supply with high accuracy and fast transient response.

1.2. Basic Structure of an LDO

Low dropout (LDO) regulator is a circuit that provides a well specified stable DC output voltage whose input to output voltage difference is very low and is independent of load current, input voltage variations, temperature and time. The *drop-out voltage* is defined as the value of the input/output differential voltage where the control loop stops regulating. In general sense, LDO acts as a *variable resistor* that is placed in between the input power source and the load in order to control the voltage applied to the load [13] [14].

An LDO works on the principles of feedback theory. The variations in the output voltage is monitored and compared with the reference voltage to generate an error signal which in turn regulates the output voltage. The block diagram of a typical LDO is shown in the Fig. 1.2.1.

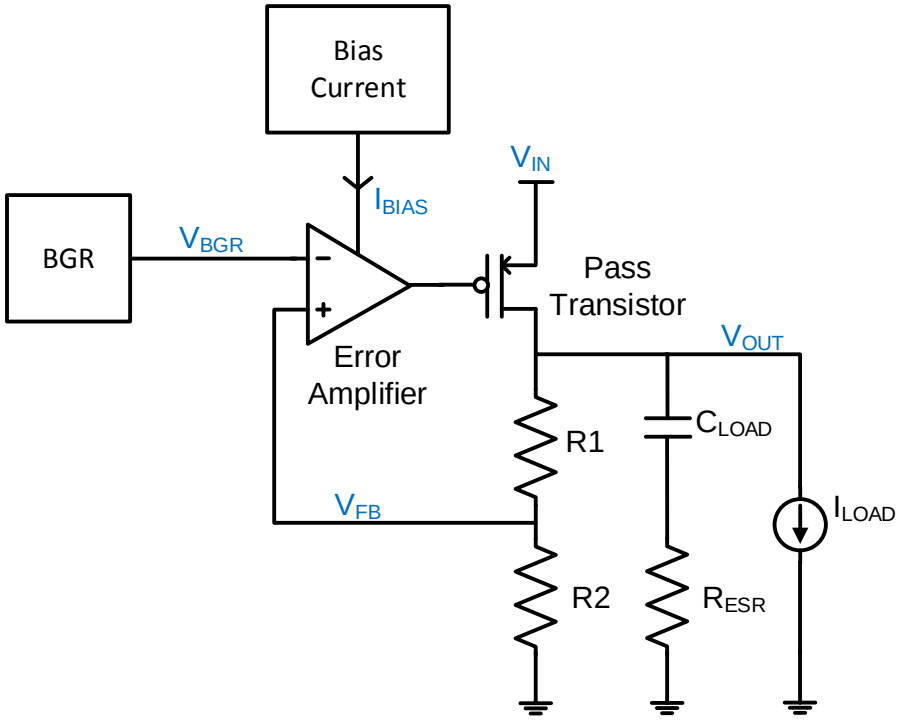

Figure 1.2.1 Block Diagram of a generic LDO

Major blocks of the LDO are a PVT independent constant voltage reference which is called the Bandgap reference (BGR), a high gain differential amplifier to compare the output voltage to the reference voltage, a constant current reference to bias the error amplifier, a PMOS/NMOS pass transistor and 2 series resistors deriving the feedback voltage (V_{FB}). The regulation action of an LDO can be understood with a case study. Let us consider that the load current (I_{LOAD}) increases, this results in a drop in the output voltage (V_{OUT}). Due to this, the difference between V_{FB} & V_{BGR} reduces and the error amplifier's output voltage reduces increasing the PMOS pass transistor V_{GS}. This brings back the output voltage to its nominal value.

1.3. Typical applications of a Low Noise LDO

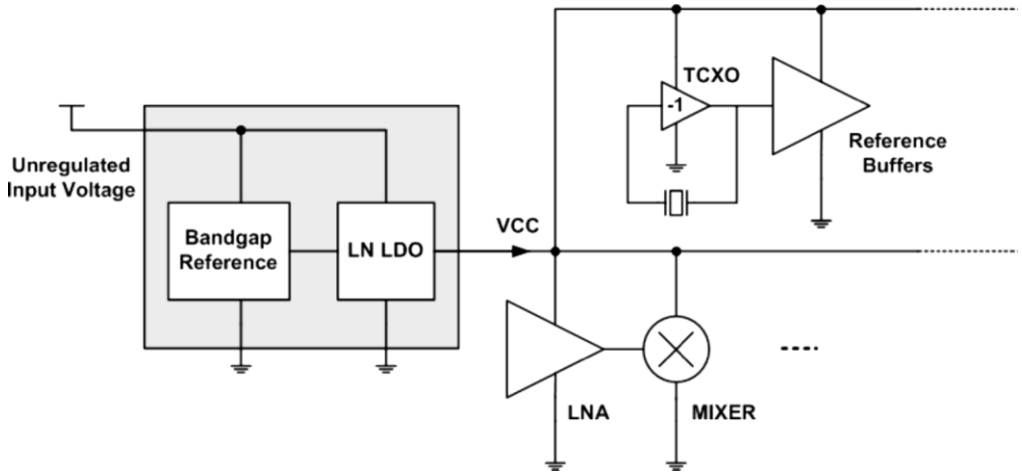

Figure 1.3.1 Typical application of a Low Noise LDO in RF circuits

As discussed earlier, it is critical for the power supply used in RF and high precision applications to be very accurate, low noise and low ripple in the baseband range of up to 100 kHz. With recent advances in communication when there is a densely packed spectrum, any noise in the baseband can be modulated to a higher frequency and interfere with the signal. Fig. 1.3.1 shows a typical RF application that requires a low noise LDO [1]. In addition to RF sections, baseband and analog sections of RF transceivers, especially the transmitter power control DACs and the receive

channel ADCs have finite PSR; therefore, at lower supply rails, they require low noise power supplies. Low noise LDO is also critical in very sensitive medical instrumentation applications where the signals of interest are low power as well as low frequency.

1.4. Previous research on Low Noise LDO

As seen in the above 2 sections, low noise LDO design is critical for high precision and high speed RF applications. Some of the previous research work has been towards designing low noise LDO's using techniques like filtering, feedback, increasing bias current, chopping, etc.

[10] uses an RC low pass filter at the output of the BGR to reduce the overall noise of the BGR. An R=100MΩ & C=100pF is used in this RC filter. A 2 stage design with power drivers is used to drive the pass transistor. This LDO posts an Integrated Noise of 21.2μV_{RMS} within the integration band of 1kHz – 100kHz. In [11], LDO consists of a 4-stage error amplifier with 1st stage noise playing the critical role in the overall LDO noise. Higher sizes and larger current is used to reduce noise. The LDO has an Integrated Noise of 40μV_{RMS} within the integration band of 100Hz – 100kHz. [12] uses a MOS-R based RC filter to reduce the noise due to BGR. The MOS resistor is of the order of 1 – 10GΩ & a MOS capacitor of 100pF is used in this filter to obtain a pole location of about 0.1Hz. It has an Integrated Noise of 10μV_{RMS} in the integration band of 10Hz – 100kHz. In [1], a chopper stabilized error amplifier is used to achieve low 1/f noise. It uses a noise shaped clock generator as clock source and posts an integrated output noise of 14μVrms in the bandwidth of 1kHz to 100kHz.

All 4 techniques mentioned above target reduction of only one of the major noise contributors in an LDO. Publications that discussed about the reduction of noise of all the constituent blocks in a generic LDO was not found, which determines the focus of this research thesis.

1.5. Research Objective

This research aims at developing innovative techniques to reduce the overall noise of any generic wideband LDO stable with or without a load capacitor. The research focusses on reducing the noise of TLV713XX family of LDOs from Texas Instruments which is a standalone LDO IC available in the market. This family of LDO is a load capacitor free, high PSRR, compact, 150mA output load current, programmable output voltage LDO with very low dropout [15]. The overall integrated noise of the original LDO at tested conditions in the integration band of 10Hz – 100kHz is 78μV_{RMS}. The objective was to integrate this existing LDO with noise reduction techniques so that the overall integrated noise reduces to about 10uV_{RMS} without affecting any other performance parameters of the LDO. Thus the project assumes an available LDO design based on structural design methodology and takes it as a starting point. The details of the original LDO circuit design are kept confidential to abide by the NDA with Texas Instruments and details provided as a part of the report are generic representations of the underlying circuit.

The deliverables of the project includes circuit design to integrate the various noise reduction techniques, layout design and post layout simulations and exporting GDSII as a part of the pre-tape-out phase. Board design, soldering and Low noise LDO characterization as the post-tape-out phase. Thus it covers the complete VLSI IC design cycle.

1.6. Thesis outline and organization

This research thesis report is organized into 6 chapters. Chapter 1 establishes the need for low noise power supply and introduces a generic LDO structure. It also gives the details on the research objective and background.

Chapter 2 introduces the types of noise found in deep sub-micron CMOS processes. It discusses the various sources of noise in a generic LDO and talks about how it is measured and compared in the industry.

Chapter 3 gives the details of the proposed noise reduction techniques and gives details about the core part of the research. It discusses all the noise reduction techniques along with the chopping ripple reduction technique. It gives the details of the circuit implementation of these techniques and key points related to the layout design are also highlighted.

Chapter 4 captures all the chip characterization results and compares it with original LDO simulation results alongside giving details about the measurement setup and board design details.

Chapter 5 discusses the future work and improvements.

CHAPTER 2
NOISE OF AN LDO

2.1. Noise in CMOS circuits

Signal power in the modern day wireless communication is usually very less due to imposed constraints like low-power design, long range communication, channel attenuation, etc. For an electronic circuit to be able to process this feeble signal, it is very critical to ensure that its noise levels are much lower than the signal amplitude levels. This also puts a limit on the minimum required signal amplitude determined by the noise floor of the electronic circuit. Thus, it is crucial to understand the modeling and behavior of noise in CMOS circuits so as to be able to develop low noise mixed signal design techniques.

Based on the source and frequency spectrum, noise in CMOS circuits can be classified into 3 major categories: Thermal noise, Flicker (1/f) noise and Shot noise. Among these the thermal and 1/f noise components are dominant contributors in the deep sub-micron CMOS processes and this research aims at suppressing these 2 types of noises [7] [17].

2.1.1. Thermal Noise

Thermal noise is generated when thermal energy causes free electrons to move randomly in a resistive material. This phenomenon was first measured and evaluated by Johnson in 1928 and is also called as Johnson noise. Nyquist later used thermodynamic argument to show that the thermal noise power in a resistor can be characterized in terms of power spectral density (PSD) with the units of V^2/Hz as

$$V_R^2(f) = 4kTR$$

Where *k* is the Boltzmann's constant, *T* is the absolute temperature in ^oK and *R* is the resistance in Ω [7] [16] [18].

In current domain, thermal noise of the resistor is given with the units of A^2/Hz by

$$I_R^2(f) = \frac{4kT}{R}$$

Where *k* is the Boltzmann's constant, *T* is the absolute temperature in ^oK and *R* is the resistance in Ω.

The Thevenin's and the Norton's equivalent of resistor noise are shown in the Fig. 3 [7]. As we can see in the above equations, the power spectrum for thermal noise is independent of the frequency for a given bandwidth. Thus, the power spectrum of thermal noise is *uniform* or *flat* and it is also called as *white noise*.

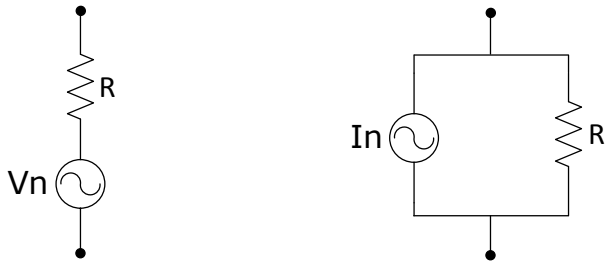

Figure 2.1.1 Thevenin's and Norton's Equivalent of Thermal Noise Model

In a circuit containing R, L & C, only the resistor generates noise. The equivalent series resistance (ESR) for inductor/capacitor should be modelled as a separate resistor and also results in thermal noise. Thus the overall integrated noise power of an impedance Z, over a bandwidth ($\Delta f = f_2 - f_1$) is given by:

$$V_{NR}^2 = \int_{f1}^{f2} 4kTRe(Z)\Delta \mathrm{f}$$

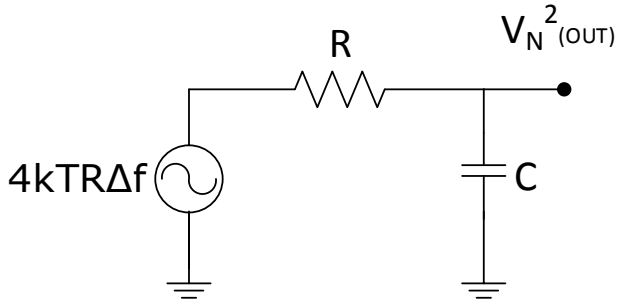

Figure 2.1.2 RC filter output Noise analysis

For e.g. in an RC circuit as shown in Fig. 2.1.2, the PSD of thermal noise (in V^2/Hz) can be calculated as:

$$V_{N(OUT)}^2(f) = 4kTR * \left|\frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}\right| = \frac{4kTR}{\left|1 + j\frac{f}{f_{3dB}}\right|}$$

$$V_{N(OUT)}^2(f) = \frac{4kTR}{1 + \left(\frac{f}{f_{3dB}}\right)^2}$$

Using the concept of Noise equivalent bandwidth (NEB) [17] for this circuit since it has a single pole response, we can derive the output integrated noise power to be

$$V_{N(OUT)}^2 = V_{N,low-freq}^2 * NEB = V_{N,low-freq}^2 * f_{3dB} * \frac{\pi}{2}$$

where

$$f_{3dB} = \frac{1}{2 * \pi * R * C}$$

Using this we have

$$V_{N(OUT)}^2 = \frac{kT}{C}$$

This shows that the value of the integrated thermal noise for an RC circuit is entirely dependent on the value of the capacitor, though the source of noise is the resistor.

2.1.2. Flicker (1/f) Noise

Flicker noise or 1/f *(one over f)* noise or *pink noise (due to pink appearance of visible light in this power spectrum)* is observed in the low frequency noise spectrum of MOSFET noise measurement. This is roughly inversely proportional to frequency and hence is called *1/f noise*. A typical spectrum of low frequency noise for a MOSFET is shown in Fig. 2.1.3 [18]. Although there are probably several different physical mechanisms resulting in noise in MOSFET's, there are strong indications that traps at the Si–SiO interface play the most important role. Electron trapping and de-trapping can lead to conductance variations.

Although the exact mechanism has been, and still is, subject to discussion, two frequently encountered modeling approaches exist: 1) the carrier-density fluctuation model (number fluctuations), predicting an input referred noise density independent of the gate bias voltage and proportional to the square of oxide thickness; 2) the mobility fluctuation model, predicting an input referred noise voltage increasing with gate bias voltage, and proportional to oxide thickness [7] [9] [16]-[18].

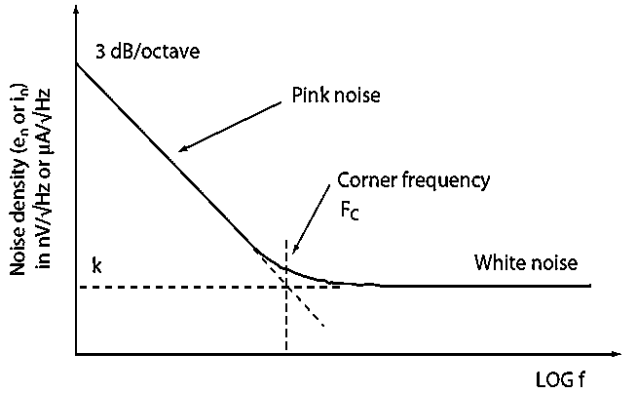

Figure 2.1.3 Low frequency Noise Spectrum for a MOSFET

2.1.3. Shot Noise

Shot Noise is generated in semiconductors by the random diffusion of electrons and holes through p-n junction and by random generation and recombination of electron-hole pairs [17]. The shot noise generated by a device is modeled by a parallel noise current source. The RMS shot-noise current in the frequency band Δf is given by

$$I_{sh} = \sqrt{2 * q * I * \Delta f}$$

where q is the electronic charge and I is the dc current flowing through the device. For a fixed bandwidth, the noise current is independent of frequency so that shot noise has a flat power distribution, i.e., it is *white noise*.

2.1.4. Other Noise sources

Apart from these major noise sources, there are other less significant noise sources like Burst noise and Avalanche Noise. Burst noise is seen in time domain. Burst noise is often called as popcorn noise. When a signal containing burst noise is played on a speaker the burst noise components sound like popping corn. The generation of popcorn noise in a broad sense is thought to be related to how generation-recombination centers affect the diffusion of carriers in pn-junction. On the other hand Avalanche noise is due to the breakdown of diode due to large electric field in reverse biased pn-junction [17] [18].

2.2. Sources of Noise in a generic LDO

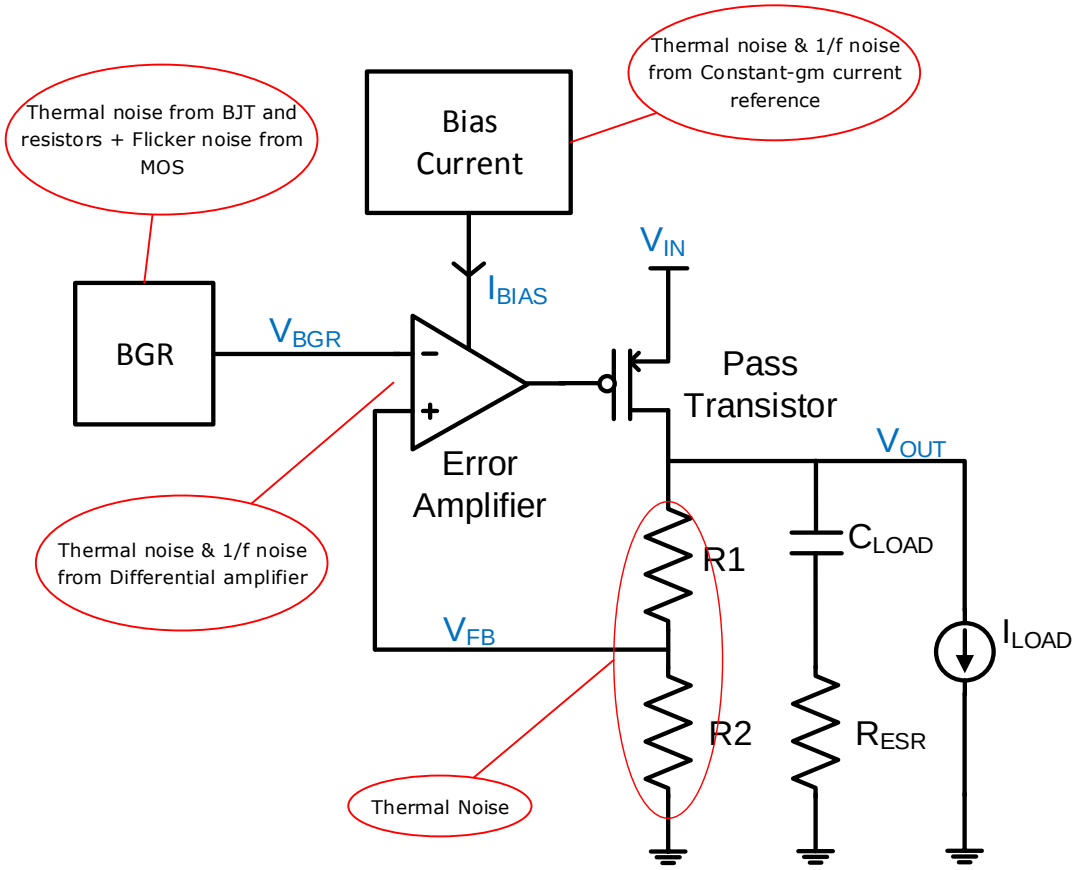

Figure 2.2.1 Major Noise sources in a typical LDO

Fig. 2.2.1 shows the major noise contributors in a typical LDO. Overall LDO noise is dominated by the noise from Bandgap Reference (BGR) and the error amplifier. Thermal noise can be pre-dominantly observed due to the BJT and the resistors present in the BGR along with the feedback resistors. 1/f noise is due to the transistors in the differential amplifier. The input pair and the folding transistors add both thermal and 1/f noise. On the other hand, if an on-chip current reference like constant-gm current reference is used, it also adds to the thermal and flicker noise of the overall LDO [1].

2.3. Quantifying LDO Noise

Typically noise of an LDO is specified in datasheets in 2 fashions [16]. One is "Total (Integrated) output noise – in μVrms", which is RMS value of the spectral noise density integrated over finite frequency range. The second method is to show the "Spectral Noise density curve – in μV/√Hz", which is a plot of Noise density vs Frequency. Since the output noise voltage is specified by a single number, the integrated noise specification is very useful for comparison purposes. When noise specifications of different LDOs are compared, it is imperative that the two regulators' noise measurements be taken over the same frequency range and at the same output voltage and current values.

It is important to pick one of either of these specifications depending upon the application of interest. This can be explained as per the following 2 examples:

1. Consider an RF system in which an LDO powers a Voltage Controlled Oscillator (VCO). If we assume that the VCO is working at a frequency of 2.4GHz, then LDO noise contributes to the VCO noise spectrum both above and below 2.4GHz with up to bandwidth of LDO. The LDO noise (shown in Fig. 2.3.1) adds to the original VCO noise plot which increases the VCO noise floor level around the center frequency. So in this RF application the user should use Spectral Noise Density curve since the single noise number loses the frequency dependence and would not be an accurate representation of the final output.
2. Consider a system in which LDO is powering an ADC or DAC. Any sampled system causes the high frequency noise to fold to lower frequencies due to aliasing. For example, if the sampling frequency is 100kHz and the noise due to LDO is at 90kHz and 110kHz, 190kHz and 210kHz, etc., then all the noise will fold back to 10kHz which is the beat frequency. This will occur for any frequency of the output noise so that all of LDO noise folds back to within the bandwidth of the sampling system.

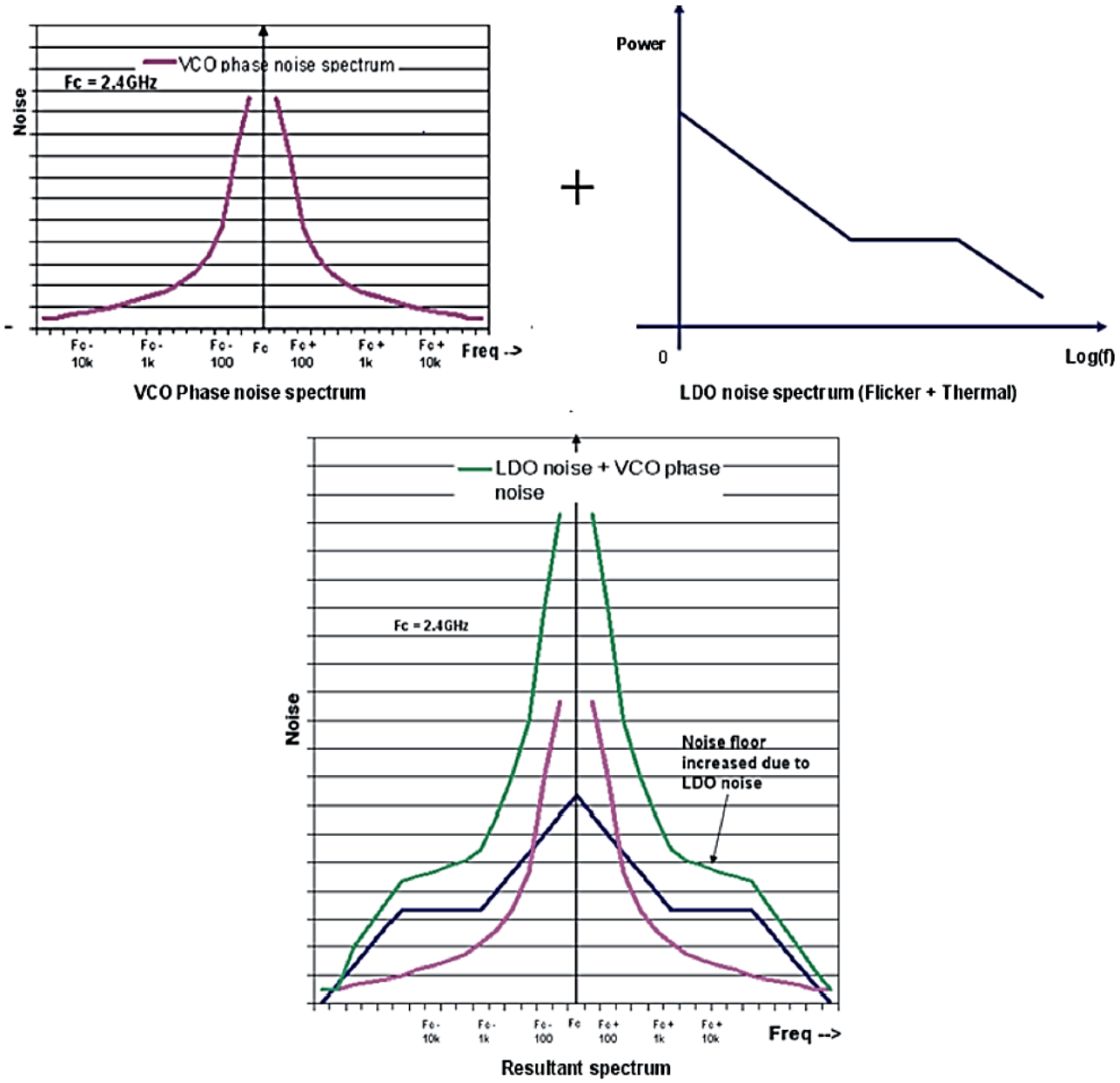

Figure 2.3.1 Effect of LDO Noise on VCO Phase Noise Spectrum

This is same as integrating all the noise from DC to bandwidth of the system and computing the total noise. This way, the performance of ADC/DAC suffers if the LDO total (integrated) noise is high.

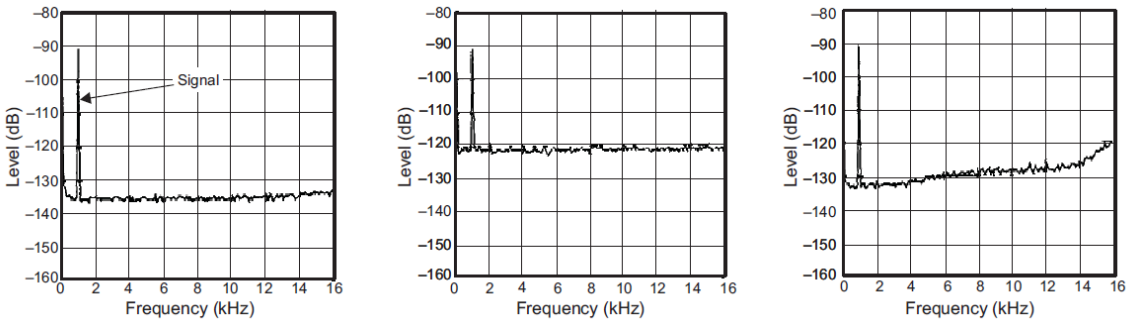

Figure 2.3.2 Effect of LDO Noise over an ADC's performance

Fig. 2.3.2 shows how LDO noise aliasing takes place. The first graph is for a system powered by ideal LDO, the second is for a system powered by LDO with thermal noise that increases noise floor and the third is for a system powered by LDO with noise at high frequency that aliases to lower frequency.

CHAPTER 3
TECHNIQUES FOR LDO NOISE REDUCTION

In chapter 2 we saw that the LDO's overall noise is dominated by thermal and 1/f noise of its constituent blocks. Mainly the BGR and the Error amplifier noise dominates the noise profile of the overall LDO. In this research, we propose different techniques to reduce the noise of each individual noise contributor. These are the Switched RC based BGR, Chopping for the Error amplifier & MOS-R based filter for the bias current noise. Chopping introduces ripple which is reduced using a Switched Capacitor based Notch Filter. In this chapter we discuss the details of all these proposed techniques.

3.1. Switched RC Bandgap Reference

Bandgap Reference (BGR) is responsible for providing a PVT independent reference voltage in an LDO. Since this voltage is directly driving one of the inputs of the error amplifier, the noise in the reference voltage (V_{REF}) appears at the output of the LDO. Thus, it is important to isolate the V_{REF} fed to the error amplifier from the noise introduced by the BGR. Most techniques till now focused on reducing the BGR noise internally using low noise circuit design approaches. In this research we propose a new technique using the concepts of Sample-and-hold and Switched RC filter. This approach not only brings down drastically, the noise of the BGR but also reduces the power consumption. Before we proceed with the overall approach, it is important to present the details of the concept of Sample-and-hold Bandgap and Switched RC filter.

3.1.1. Sample and Hold BGR

Ultra low energy consumption of the BGR can be achieved in two ways [2]:

1. By decreasing currents running in the core with use of the prohibitively large resistors in 100's of MΩ range. Even if these resistors were realistic they would increase the BGR noise. According to simulations the peak-to-peak noise in the BGR with 100–200 nA consumption becomes a dominant error source.
2. By activating BGR for short periods of time and sampling reference voltage on the capacitor. Low charge leakage from this capacitor during long hold periods is critical for accuracy of such a reference.

Since the objective of a BGR is to generate a reference voltage (V_{REF}) which is fed to the gate of the input pair of the error amplifier, it is convenient and effective to use a Sample & Hold circuit at the output of the BGR so that we can conveniently turn BGR off during the hold period (provided the hold time is significantly long). For e.g. in the current design we have a sample time of T_S = 10μs & hold time of T_H = 1s. If the startup time for BGR is 50μs, then the ON time for BGR is only about 60μs for every second. This results in a significant reduction in the power consumption of the BGR without affecting the LDO performance. Fig. 3.1.1 shows the block level implementation of a Sample-and-hold BGR.

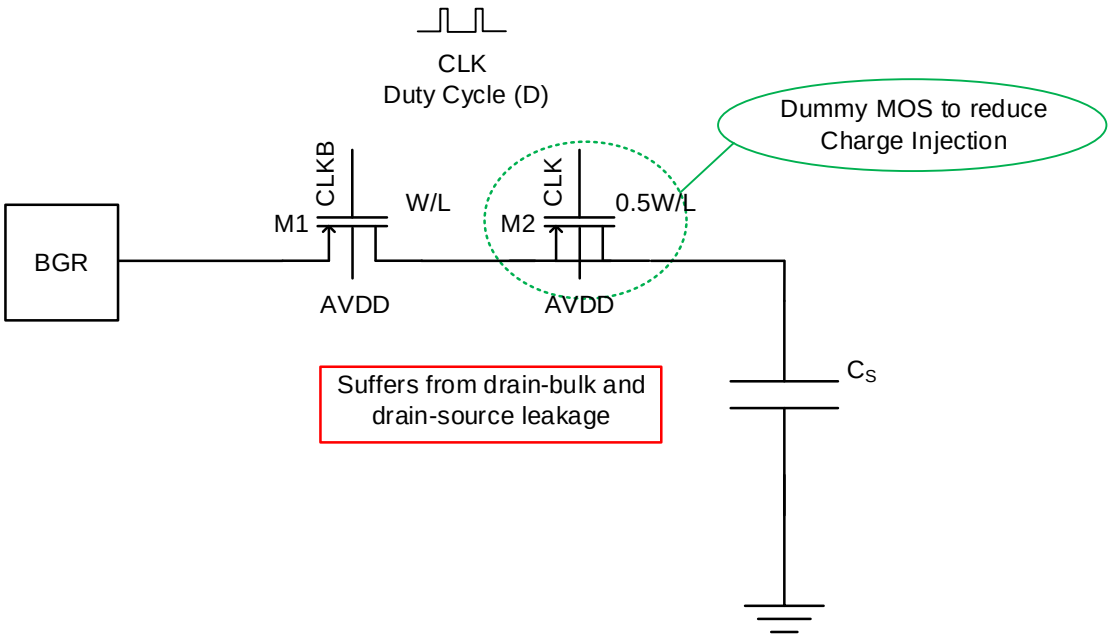

Figure 3.1.1 Block diagram for Sample-and-Hold BGR

It consists of a PMOS switch controlled using a short sample time and long hold time clock and a storage Capacitor (C_S). A dummy PMOS is used to reduce the effect of charge injection in series with the actual switch towards C_S. The disadvantage of this setup is the charge leakage of the storage capacitor (C_S) dominated by the junction leakage of the PMOS switch (Drain to Bulk & Drain to Source) during the hold mode. Junction leakage is roughly proportional to the voltage drop across junction. Therefore low leakage and long hold time S/H can be realized by keeping zero voltage across drain-source and drain-body of the switch.

3.1.2. Low leakage Sample-and-Hold BGR

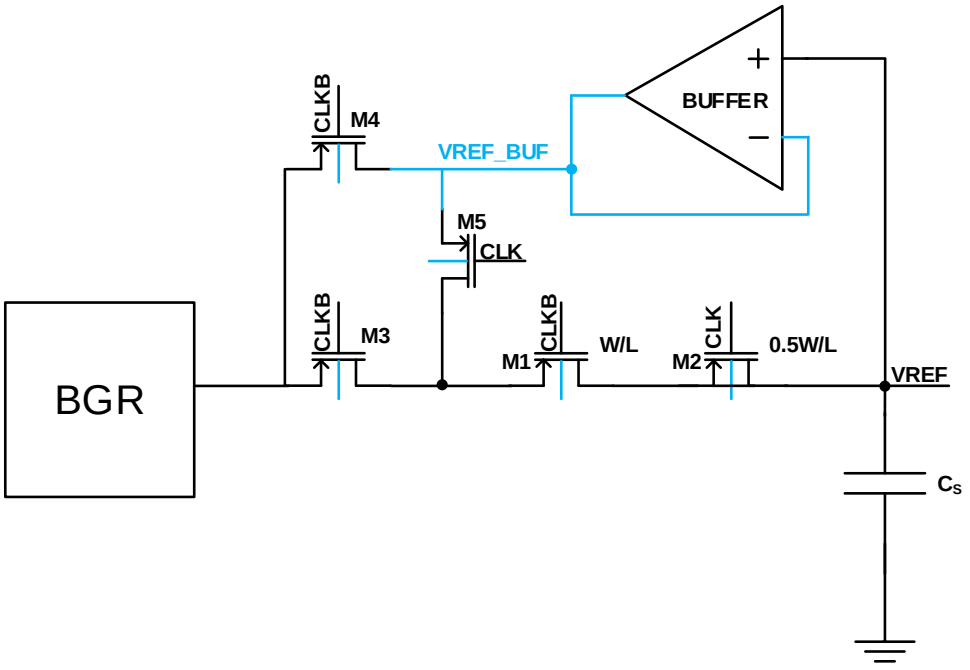

Figure 3.1.2 Leakage compensated Sample-and-Hold BGR

The circuit shown in Fig. 3.1.2 keeps the drain-bulk and drain-source voltage equal to the offset (V_S) of the buffer amplifier [2]. This very low power (300nA) buffer ensures that the junction leakages are kept to few pA even at high temperature. The simulations confirm the same. The PMOS switches M1 & M2 are the sampling and the dummy switches. M3 & M4 isolate the rest of the circuitry from BGR when it is turned off and pulled high in the hold phase. M5 ensures that the buffered reference voltage (VREF_BUF) is connected to the source of M1 during hold phase to reduce drain-source leakage. The bulk terminal of all the PMOS switches is connected to VREF_BUF to ensure that the drain-bulk leakage is minimal.

3.1.3. Switched RC filter

Typical noise integration bandwidth for an LDO starts from frequencies very close to DC. For this TLV713 family of LDO's, we are interested in a Bandwidth of 10Hz

to 100kHz. As an initial effort, let us consider implementing a simple RC low-pass filter to reduce the noise of BGR. For our application, we need the pole location of this low pass filter at a frequency lower than 10Hz. Let us consider a decade lower frequency of 1Hz as the pole location. Assuming, an on-chip capacitance of 100pF (very large in area but realizable worst case value), we can estimate the value of resistance using the low pass filter pole equation:

$$f_{3dB} = \frac{1}{2 * \pi * R * C}$$

$$\rightarrow R = \frac{1}{2 * \pi * f_{3dB} * C}$$

$$\rightarrow R \cong 1.5G\Omega$$

Implementing both R and C of this value would result in a huge area overhead and is not implementable in the modern day VLSI design due to high cost.

To realize very low cutoff frequencies for the low pass filter, we can use the concept of switched RC filter [4]. The circuit for a switched RC filter for the BGR shown in Fig. 3.1.2 is a modified version of Sample-and-hold BGR discusses in previous section. Along with the hold/storage capacitor (C_S) it consists of a filter resistance 'R_F' and a switch in series with the BGR. The switch is controlled using a clock with a very small duty cycle (D) i.e. very short Sample time (T_S) and long Hold time (T_H).

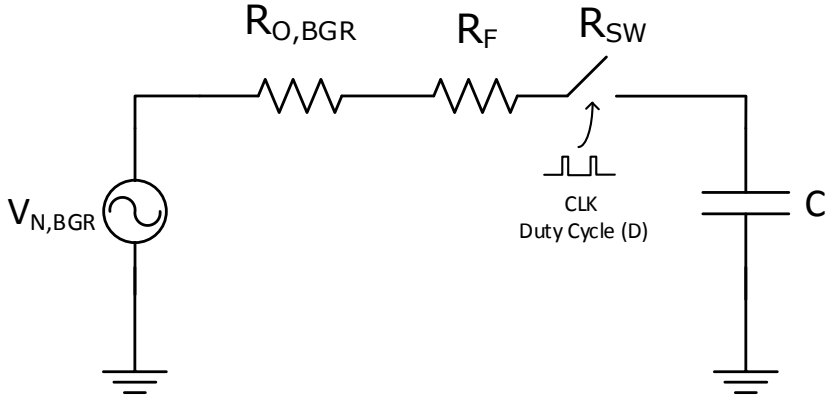

Figure 3.1.3 Switched RC filter circuit

The equivalent resistance (R_{eq}) is a combination of 3 resistances: BGR's output resistance ($R_{O,BGR}$), filter resistance (R_F) & the on resistance of the switch (R_{SW}).

$$R_{eq} = R_{O,BGR} + R_F + R_{SW}$$

With the switch operating at clock with duty cycle 'D', the average resistance of the switched RC filter can be given as

$$R_{avg} = R_{eq}/D$$

Thus the effective filter pole location is at

$$f_{3dB} = \frac{D}{2 * \pi * Req * C}$$

NOISE ANALYSIS

With the switched RC filter at the output of the BGR, the overall noise after the switched RC filter can be given as

$$V_{NO(RMS)}^2 = \int_0^\infty \frac{V_{PSD,LF(RMS)}^2}{\left(\sqrt{(1 + \left(\frac{f}{f_{3dB}}\right)^2}\right)^2} df$$

where $V_{PSD,LF(RMS)}^2 = V_{PSD,BGR(RMS)}^2 + 4 * k * T * R_{eq}$

If we use,

$$\int \frac{du}{a^2 + u^2} = \frac{1}{a}\tan^{-1}\frac{u}{a} + C$$

$$\rightarrow V_{NO(RMS)}^2 = V_{PSD,LF(RMS)}^2 * f_{3dB} * \frac{\pi}{2}$$

In the above term we define the Noise equivalent bandwidth (NEB) as

$$NEB = f_{3dB} * \frac{\pi}{2}$$

Using the value of cutoff frequency obtained from the switched RC filter equation we get the overall output noise as

$$V_{NO(RMS)}^2 = \left(V_{PSD,BGR(RMS)}^2 + 4 * k * T * R_{eq}\right) * \frac{D}{2 * \pi * Req * C} * \frac{\pi}{2}$$

$$V_{NO(RMS)}^2 = \frac{V_{PSD,BGR(RMS)}^2 * D}{4 * Req * C} + \frac{k * T * D}{C}$$

From the above equation we can see that both the BGR noise and the kT/C noise are scaled down by a factor of the duty cycle of the switching clock. For e.g. if we choose T_S = 10µs & T_H = 100ms, the D = 0.01% which results in a significantly lower cutoff frequency very much close to DC. Thus by using this technique of Switched RC filter along with Sample-and-hold, both noise and power consumption of the BGR can be reduced significantly.

3.1.4. MOS based Resistor

To obtain a switched RC pole close to DC, in our case assuming 0.1Hz (2 decades before 10Hz) with a capacitance of 10pF and a duty cycle D=0.01%, we can estimate the required resistance using the filter equation as

$$f_{3dB} = \frac{D}{4 * Req * C} = 0.1Hz$$

$$R_{eq} \cong R_F = \frac{10^{-4}}{4 * 0.1 * 10p}$$

$$R_F = 25M\Omega$$

This value of R_F results in a large area resistor if implemented using a POLY resistor. Since the required accuracy is not lesser than 1%, we can substitute this resistor with a sub-threshold region MOS resistor [12]. Fig 3.1.5 shows the implementation of a sub-threshold MOS resistor.

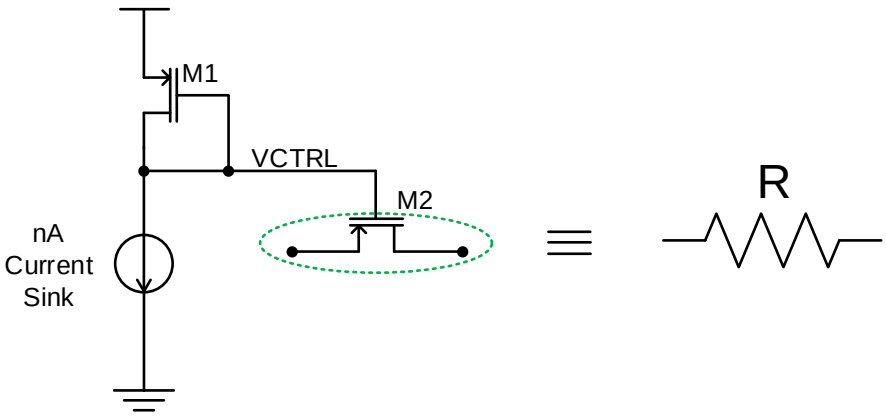

Figure 3.1.4 Sub-threshold region biased MOS based Resistor

A diode connected PMOS (M1) is biased using a very low current to ensure that the V_{GS} of the PMOS is less than its V_{TH} and the MOS is biased in sub-threshold region. This V_{GS} acts as a control voltage (VCTRL) to another PMOS gate which acts as a high value resistor. The size of M1 is varied to change VCTRL and thus the resistance offered by M2.

3.1.5. Overall Switched RC BGR Structure

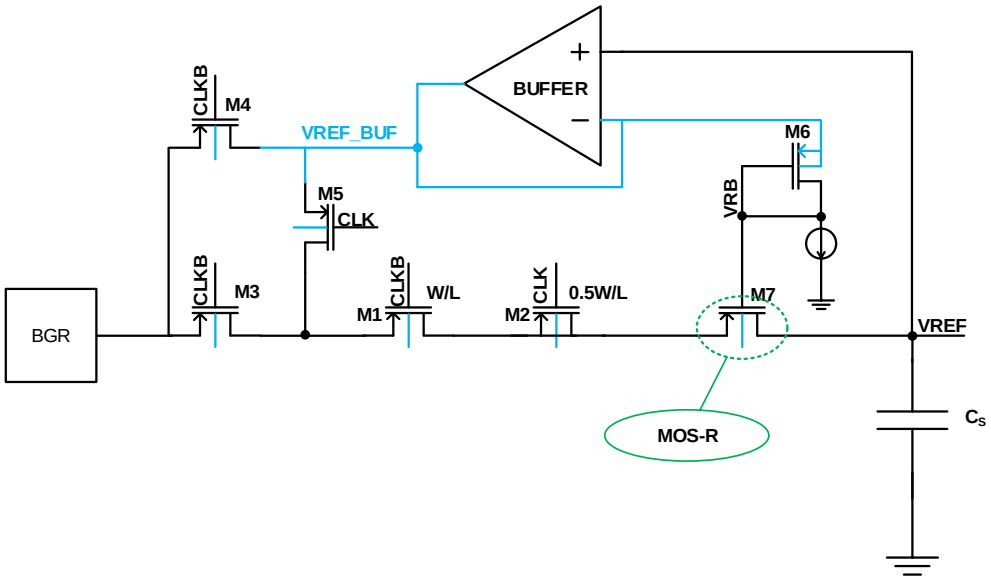

Figure 3.1.5 Switched RC BGR with Noise and Leakage reduction techniques

3.2. Feedback Resistor Noise Reduction

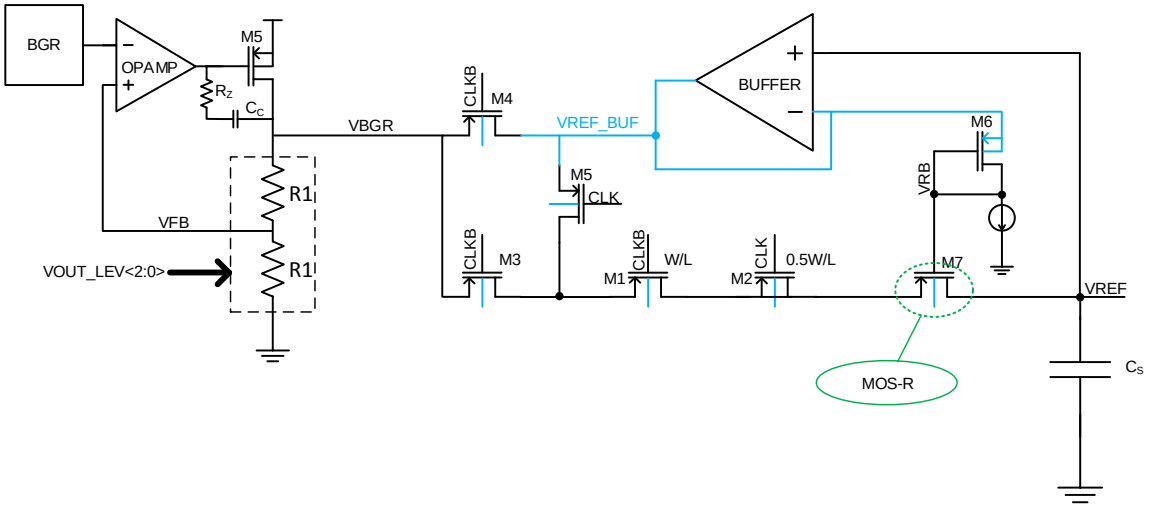

Figure 3.2.1 Switched RC BGR with Scaling Amplifier

As seen in section 2.2, the feedback resistors at the output of the error amplifier is also a major noise contributor in the overall LDO noise. In order to reduce this noise, it was placed before the Switched RC filter by using the setup shown in Fig. 3.2.1 [10]. The error amplifier is used in Unity feedback configuration and a high gain scaling amplifier is used to scale the actual BGR output to the required output voltage. In general, an output voltage programmable LDO uses the feedback resistors to program the output voltage. Here the same programmability is used to program the output of the BGR + Scaling amplifier so that the required output voltage is generated and fed to the error amplifier.

Since the switched RC filter is placed beyond the scaling amplifier, the noise due to both scaling amplifier and the feedback resistors along with the BGR is filtered out. Thus Switched RC BGR technique reduces noise due to both BGR and Feedback resistors.

3.3. Chopping for Error Amplifier

At low frequencies 1/f noise of the Error amplifier is the dominant contributor to the overall LDO noise. There are many techniques available to reduce the 1/f noise of operational amplifiers, especially instrumentation amplifiers. Auto-zeroing, chopping, etc. are well known techniques for reducing offset and low frequency 1/f noise. In our case, since the signal is at DC and auto-zeroing places a null at DC, this technique cannot be used. Chopping on the other hand can be used to reduce the 1/f noise seen in the error amplifier.

3.3.1. Details of Chopping technique

Chopping is continuous time modulation technique that modulates offset and low frequency 1/f noise to a higher frequency [5]. Fig. 3.3.1 gives the details about the implementation and frequency response of chopping technique [6]. The input voltage V_{IN} first passes through a chopper driven by a clock at chopping frequency f_{ch}, thus it is up-converted to a frequency f_{ch}. Next, the modulated signal is amplified together with its own input offset. The second chopper then demodulates the amplified input signal back to DC, and at the same time modulates the offset and the 1/f noise to the odd harmonics of f_{ch}, where they are filtered out by a low-pass filter (LPF). This results in an amplified input signal without offset and 1/f noise.

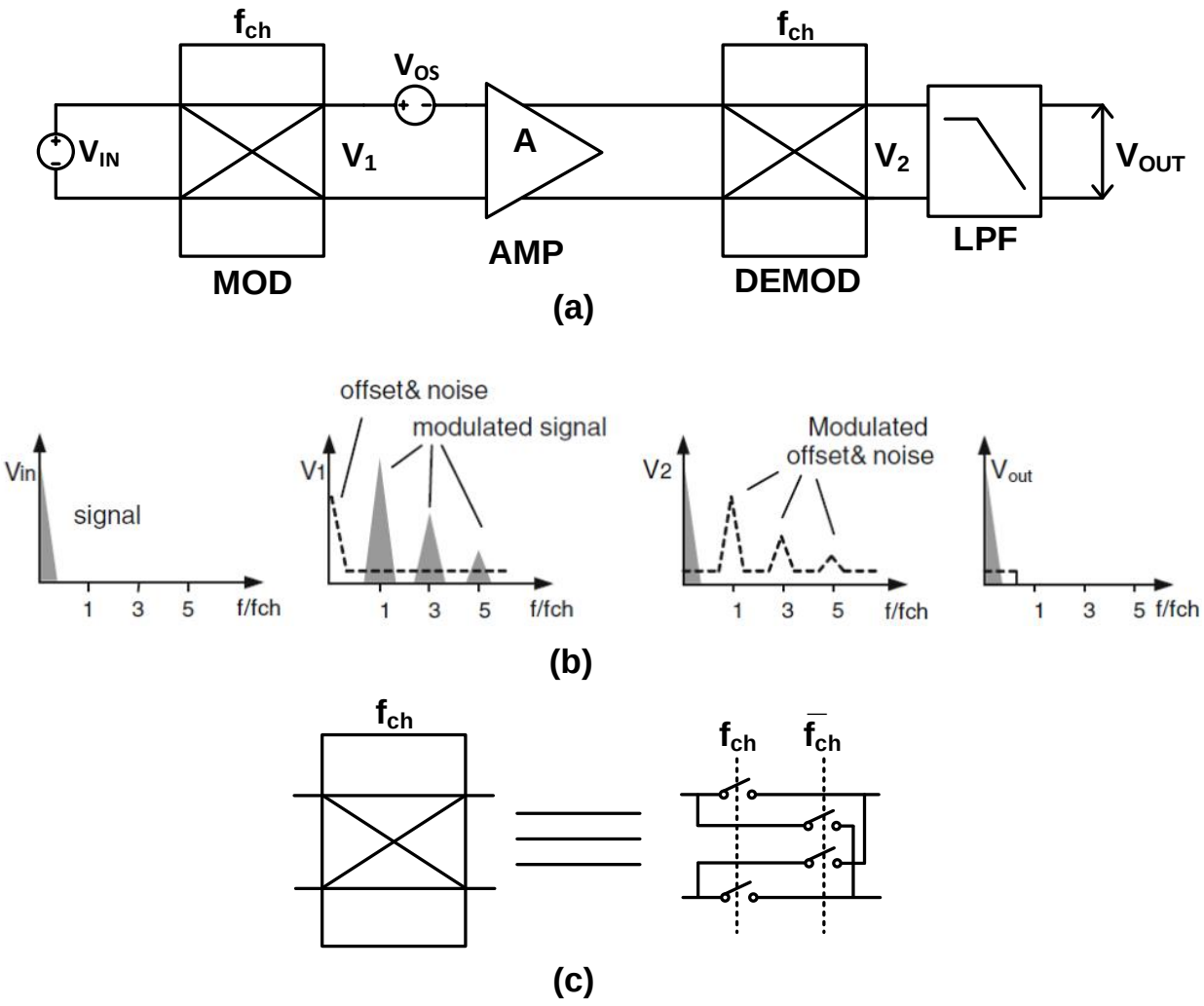

Figure 3.3.1 (A) Block diagram description of Chopping technique;

(B) Frequency domain depiction of Chopping technique;

(C) Implementation of Chopper

The implementation shown here is chopping done in voltage domain. Thus it is important for the amplifier bandwidth to be at least twice the chopping frequency for maximum gain of this stage. This limited bandwidth of the amplifier results in even harmonics and lower DC gain for the amplifier and chopper stage. The modulated low frequency noise and offset appear as chopping ripple at the output of the amplifier which are at harmonics of the chopping frequency in the frequency spectrum.

3.3.2. Limitations of this approach

There are 2 major limitations of the approach discussed in Section 3.3.1 due to which it cannot be used for this LDO under consideration:

1. The reference input V_{REF} is derived from the Switched RC BGR's storage capacitor (C_S). If the 1st stage chopper is placed before the error amplifier (gate end chopping), then due to continuous switching there will be a significant leakage in the stored charge at C_S resulting in an erroneous reference voltage being fed to the error amplifier.
2. The bandwidth of the error amplifier is limited to a few tens of kHz, thus if voltage mode chopping is used, then the effective DC gain of this stage drops down to a very low value resulting in inaccurate LDO output [5] [6].

3.3.3. Modified current mode Chopping technique

To overcome the limitations mentioned above, a modified chopping technique with drain-end chopping is proposed. Fig. 3.3.2 shows the circuit implementation of this modified chopping technique. Current mode modulation chopper is placed just after the input pair transistors MN1 & MN2. The signal is modulated to the chopping frequency (f_{CH}) at this chopper. At the demodulating choppers the signal is converted back to DC and the low frequency noise of transistors MP1 & MP2 along with MN5 & MN6 are modulated to f_{CH}. This technique has the following features:

1. Since it is current mode chopping, the bandwidth of the amplifier is not limiting the performance of the overall amplifier with chopping integrated. Thus this gives the freedom to increase the chopping frequency up to a few MHz as long as the circuit is fully functional.
2. Charge leakage from the Switched RC BGR's storage capacitor C_S due to chopping is eliminated. Since the chopping is done at the drain-end of the input pair there is no question of charge leakage at the gate terminal.

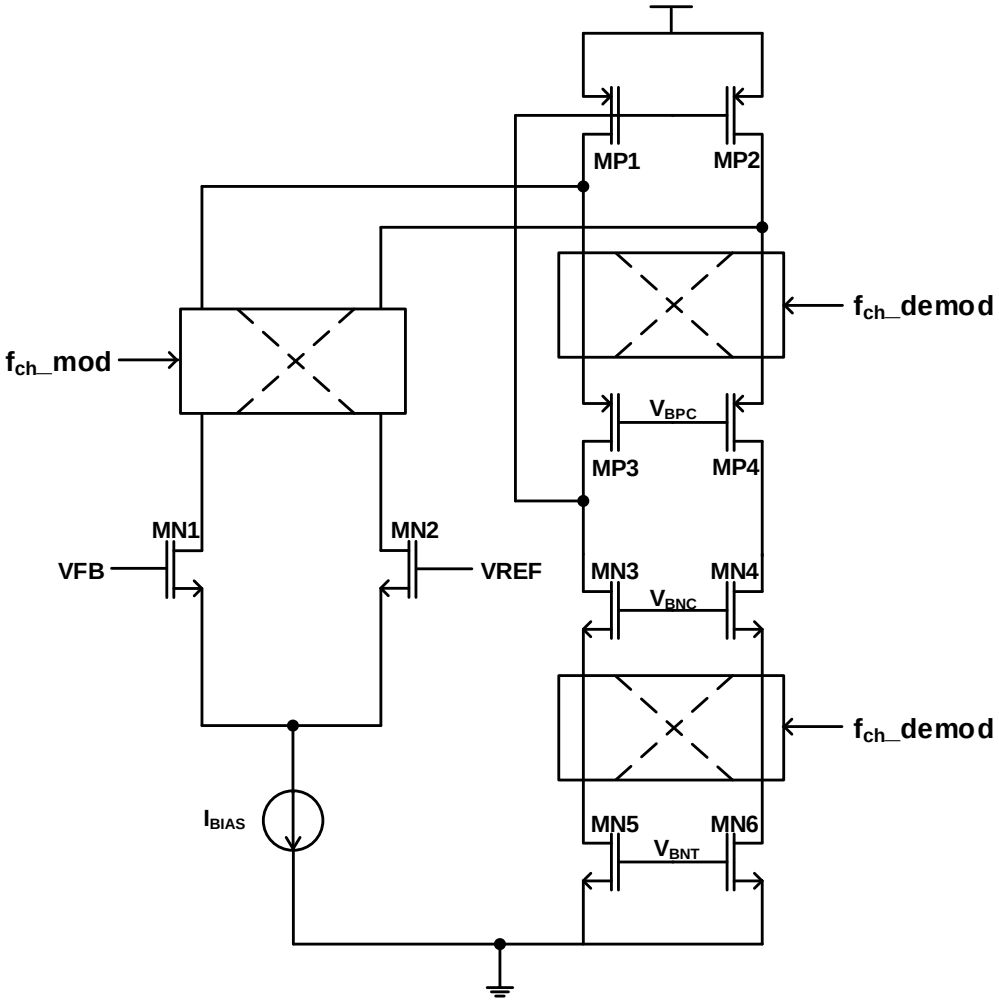

Figure 3.3.2 Modified Drain-end Chopping for Error Amplifier Noise reduction

This technique eliminates the use of degeneration resistors for the PMOS load to reduce its 1/f noise. However the major disadvantage of this technique is that the 1/f noise of the input pair which is one of the major contributor in the error amplifier noise is not modulated. The modulation happens after the input pair converts the applied gate voltage to current. Thus the input pair is not in between the modulation-demodulation choppers and its noise is not modulated.

3.4. Chopping Ripple reduction

Chopping technique introduces chopping ripple at the output of the amplifier. This shows up as spikes in the LDO output at the rate of chopping frequency. Since a typical application of an LDO demands low noise and low ripple supply, it is important to reduce this chopping ripple. Multiple techniques have been proposed to reduce the chopping ripple at the output of the amplifier. Broadly, they can be classified into continuous time and discrete time ripple reduction techniques. Since we have a clock in the circuit, discrete time ripple reduction using Switched Capacitor techniques turns out to be a good option.

Fig. 3.4.1 shows a Switched Capacitor (SC) based Notch Filter structure [3]. The reduction of ripple is achieved by integrating the output of the error amplifier synchronous to chopping. Consider a positive offset voltage, at the output of the error amplifier during $f_{ch} = 1$ & an equal and opposite negative offset voltage when $\overline{f_{ch}} = 1$ as a result of chopping of its offset and 1/f noise. This offset is nulled by integrating half of the positive offset voltage and half of the negative offset voltage during $f_{nch} = 1$, and this is passed onto the output when $\overline{f_{nch}} = 1$. In other words, the sampling of the output of the error amplifier happens when the initial switching ripple has settled and this stable value is passed onto the output. The frequency response of this SC

notch filter is shown in Fig. 3.4.3. By keeping the ratio of C1/C2 to about 1:6, a largely flat response is obtained for the notch filter till the chopping frequency.

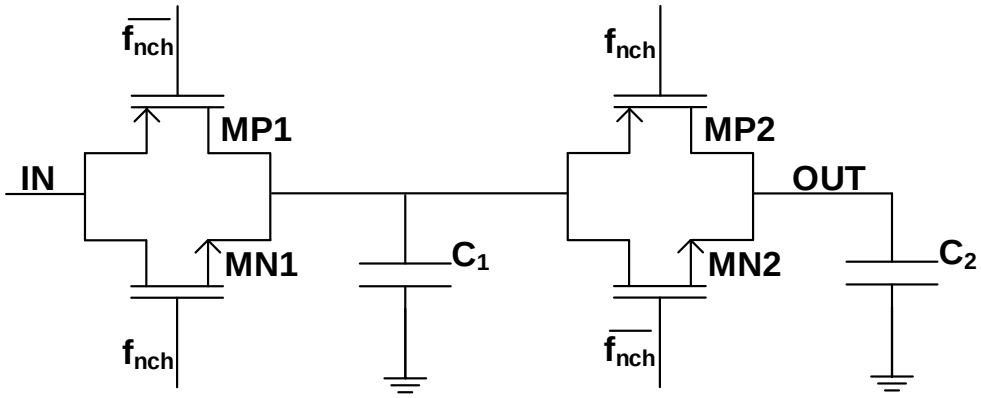

Figure 3.4.1 Switched Capacitor (SC) Notch filter

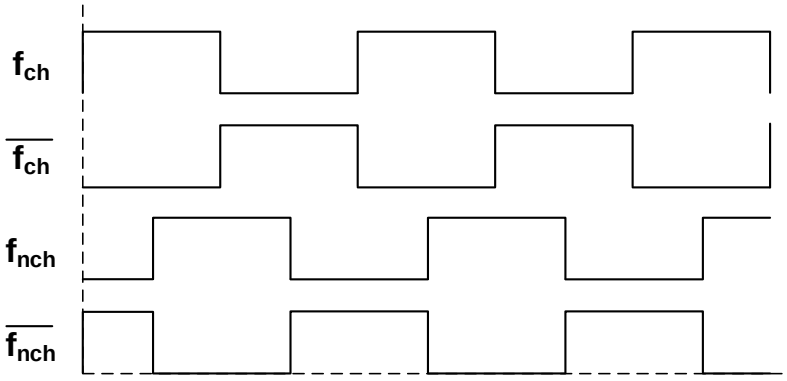

Figure 3.4.2 Chopping and Notch filter clock phases

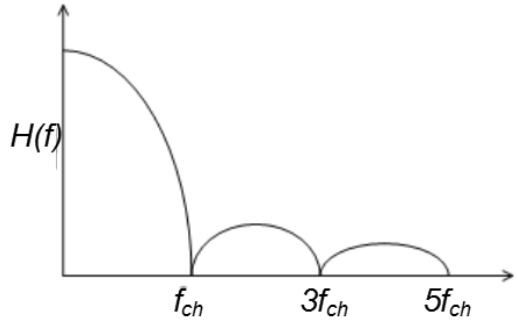

Figure 3.4.3 Frequency response of SC Notch filter

3.5. Bias Current Noise filtering

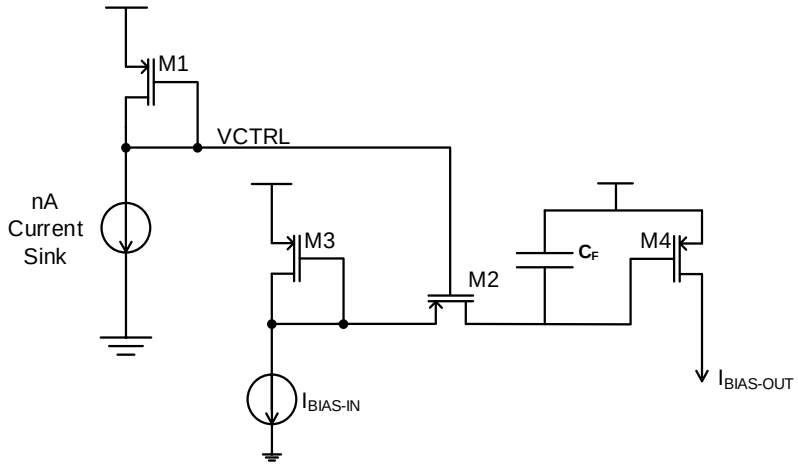

Figure 3.5.1 MOS-R based RC filter for Bias Current Noise filtering

MOS resistor based RC filter is used to filter the bias current noise. It is placed in between the last V-I convertor current mirror closer to the error amplifier. The noise due to transistors in the constant-gm current reference are filtered out and this voltage is fed to the final V-I converter.

3.6. Overall Low Noise LDO structure

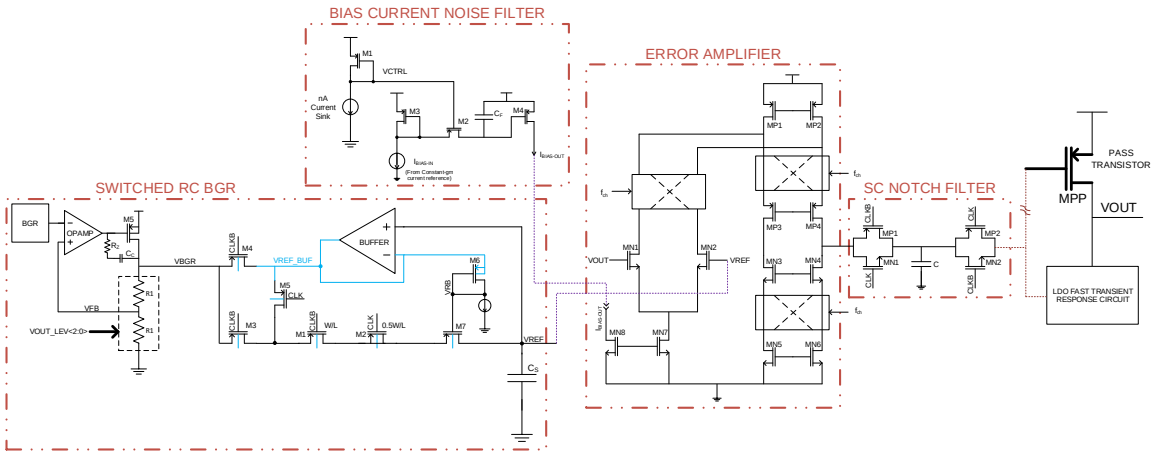

Figure 3.6.1 Low Noise LDO with Noise, Power and Ripple reduction techniques

3.7. Layout design

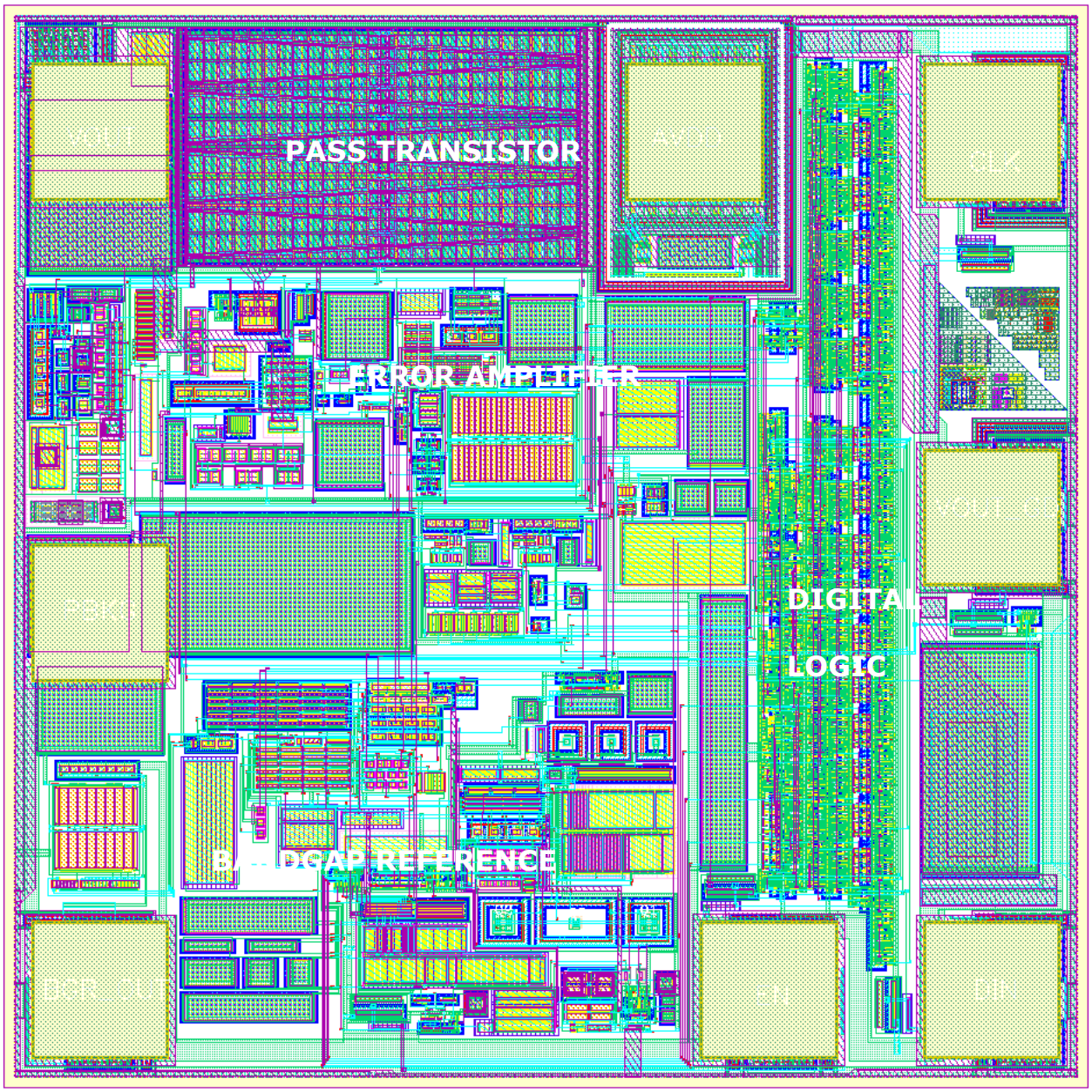

Figure 3.7.1 Low Noise LDO layout

3.7.1. Key points of Low Noise LDO layout

1. The full chip layout consists of 8 I/O pads: VDD, OUT, EN & VSS (the default original LDO pins); CLK, DIN, VOUT_GD & BGR_OUT (the additional pins added for testing).
2. Layouts for Bandgap Reference and pass transistor used from original LDO unchanged. Layout for Error amplifier, scaling amplifier and filter blocks done. Top level and Pad ring layouts done.
3. Required matching constraints followed while doing layout of error amplifier e.g. Common centroid for input pair, interdigitated for PMOS load & cascode devices, etc. Symmetric Routing followed for critical blocks and routing width chosen according to EM constraints.
4. Chopper switches layout made symmetric with devices matched and symmetric routing.
5. Overall layout area is 580µm x 580µm.
6. The area overhead incurred by the added techniques excluding the extra pads and the digital mode setting logic is about 200µm x 200µm out of which the added capacitances occupy an area of 120µm x 120µm

CHAPTER 4
SIMULATION AND MEASUREMENT RESULTS

4.1. Board design

Board design for this low noise LDO was done using Multisim and Ultiboard software. A 2 layer PCB was designed and SMA connectors were used to tap the outputs and also to provide the clock input. An SPI interface MCP2210 was used to program the internal modes. Decoupling capacitor chain for power supply was placed with the lowest Capacitor near to the LNLDO chip. Fig. 4.1.1 shows the Low Noise LDO board used for measurement.

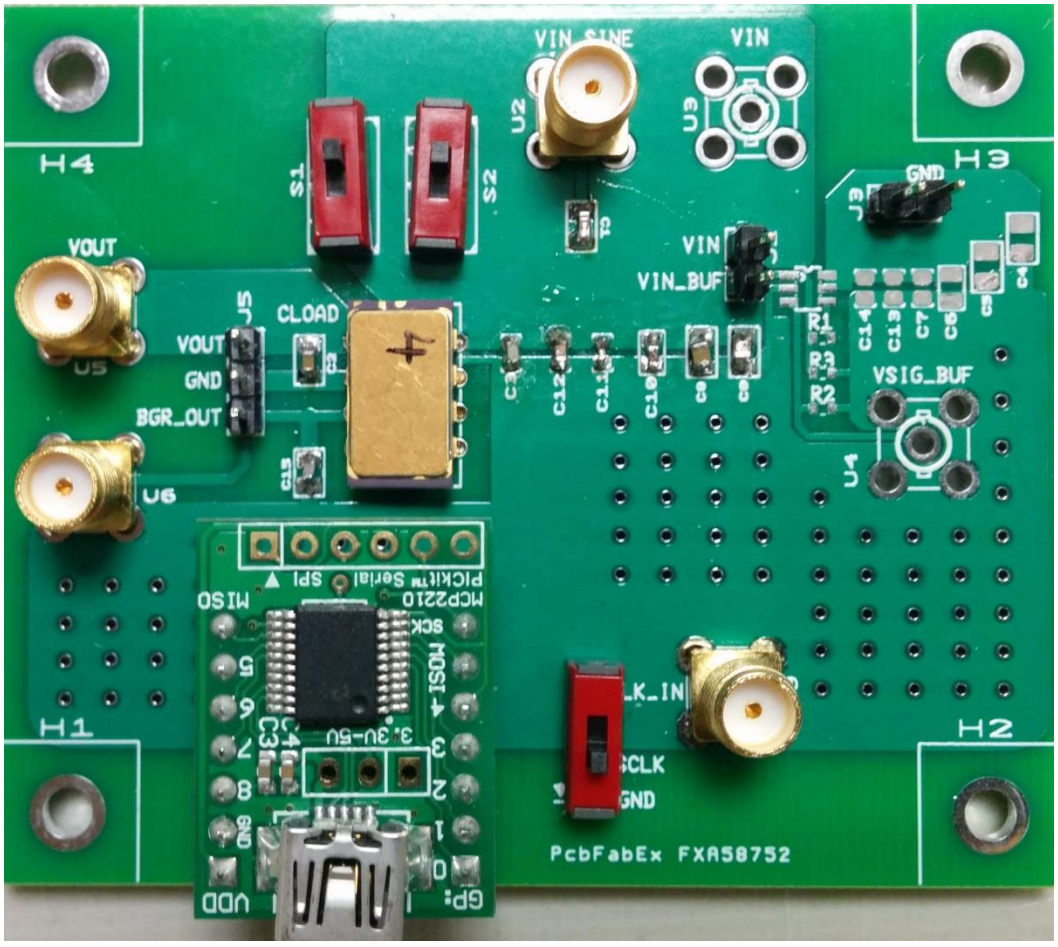

Figure 4.1.1 Low Noise LDO Measurement Board

4.2. Measurement setup

Fig. 4.2.1 shows the measurement setup with all the major instruments used to characterize this low noise LDO. Noise was measured using Agilent 35670A Dynamic Signal analyzer capable of computing FFT from DC–100kHz which includes our bandwidth of interest. Agilent Spectrum analyzer was used to measure the ripple content at the output of the LDO. For both noise and ripple a Low Noise Preamplifier from Stanford Research Systems was used at the output of the LDO for accurate measurement. An accurate discrete resistor was used to set the required load current for noise and ripple measurements. An electronic load was used for Dynamic regulation test. Microchip MCP2210 SPI interface was used to program the Serial shift register to program the different modes of the LDO. A 4.5V DC battery was used to power-up LDO for noise and ripple measurements to avoid a noisy power supply. Agilent 33250A waveform generator was used to provide the required clock input.

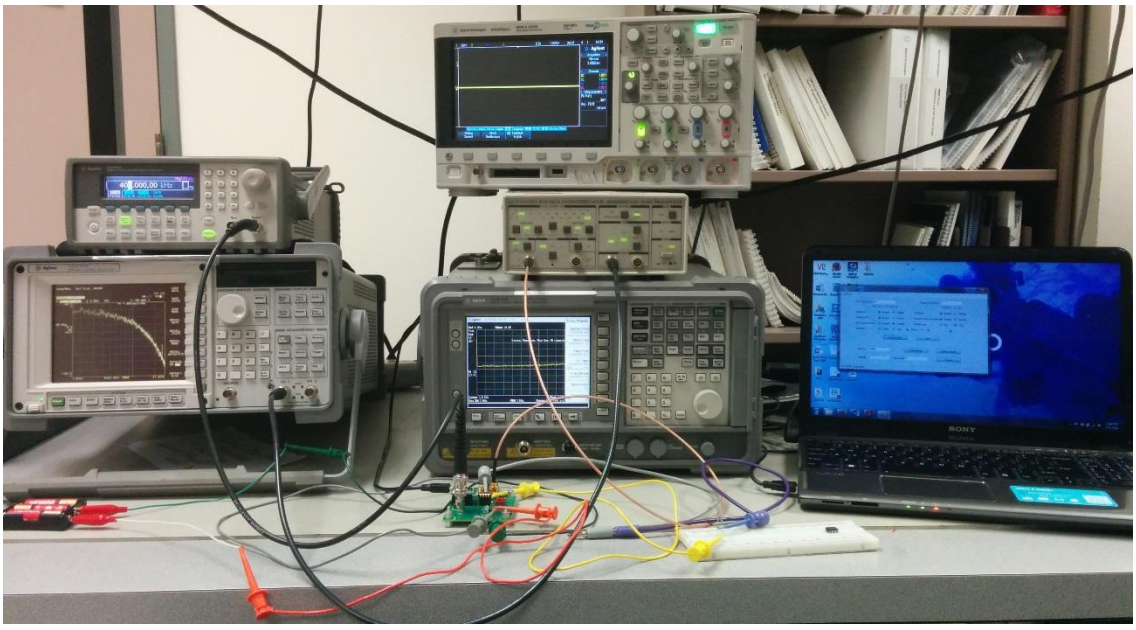

Figure 4.2.1 Low Noise LDO Measurement setup

4.3. Noise

4.3.1. Noise of overall LDO

Measurement conditions: VDD=4.5V, VOUT=1.8V, I_{LOAD}=10mA, C_{LOAD}=470nF & Temp =300K. Noise integration bandwidth 10Hz – 100kHz.

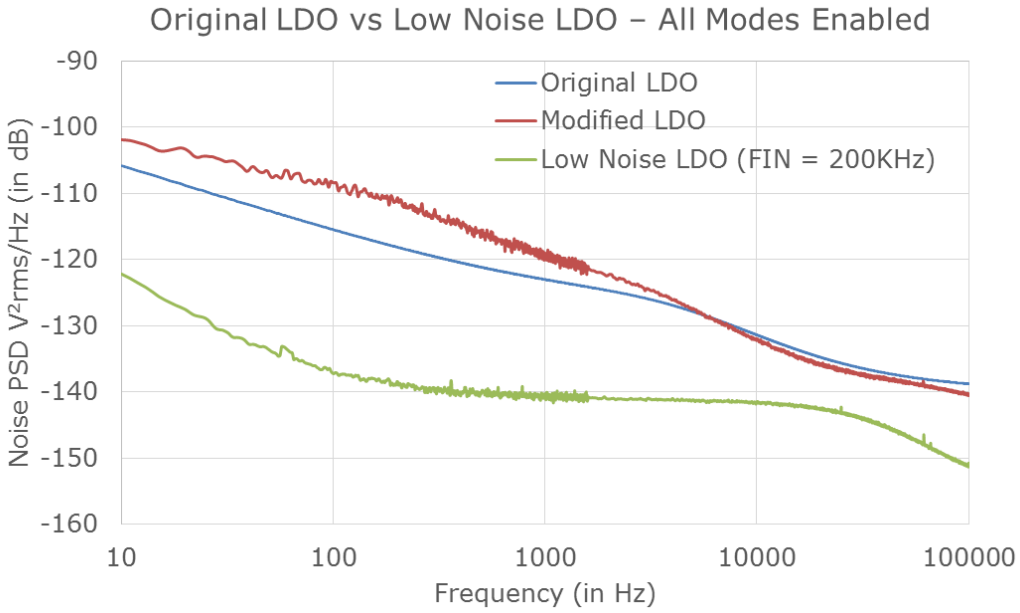

Figure 4.3.1 Noise comparison between Original LDO and Low Noise LDO

Mode of LDO	**Integrated Noise**	
	nV^2_{RMS}	**μV_{RMS}**
Original TLV713 LDO	5.33	73
Modified LDO without any noise reduction techniques enabled	9.08	95.3
Low noise LDO with all techniques enabled and a with F_{CHOP} = 200kHz	0.32	17.9

Table 4.3.1 Integrated Noise summary for different LDO modes

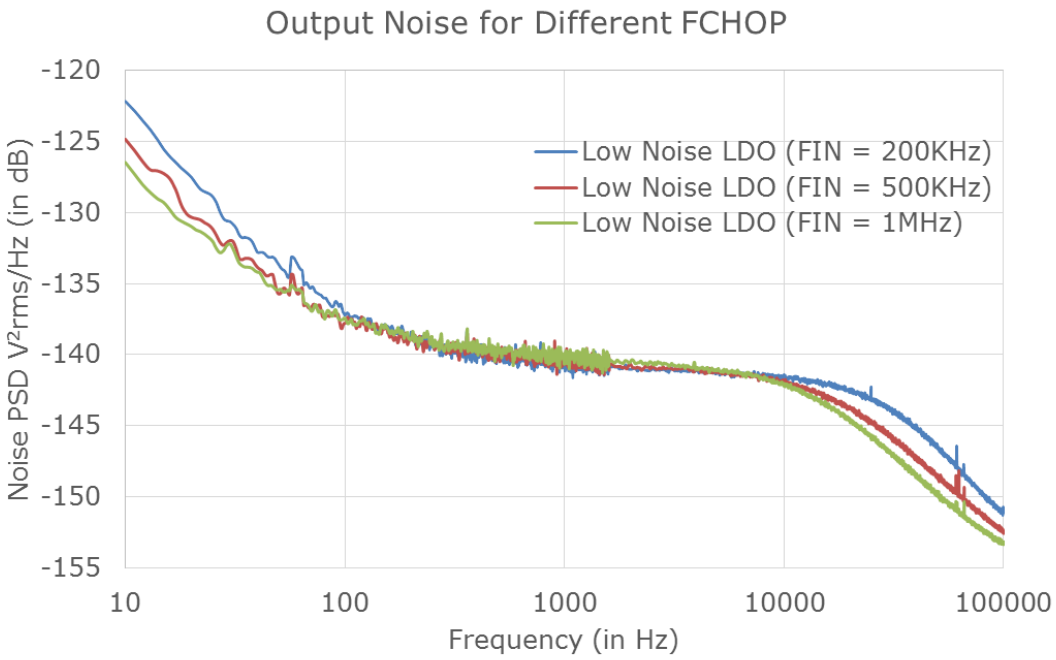

Figure 4.3.2 Low Noise LDO for different Chopping frequency

Mode of LDO	**Integrated Noise**	
	nV^2_{RMS}	**μV_{RMS}**
Low noise LDO with F_{CHOP}= 200kHz	0.322	17.9
Low noise LDO with F_{CHOP}= 500kHz	0.25	15.8
Low noise LDO with F_{CHOP}= 1MHz	0.148	14.8

Table 4.3.2 Low Noise LDO Integrated Noise summary for different F_{CHOP}

4.3.2. Switched RC BGR Noise

Noise measured at the output of the LDO with only Switched RC noise reduction technique enabled. Noise captured with Switched RC clock of duty cycle = 6.67m% with sample time T_S = 10µs & hold time T_H = 150ms

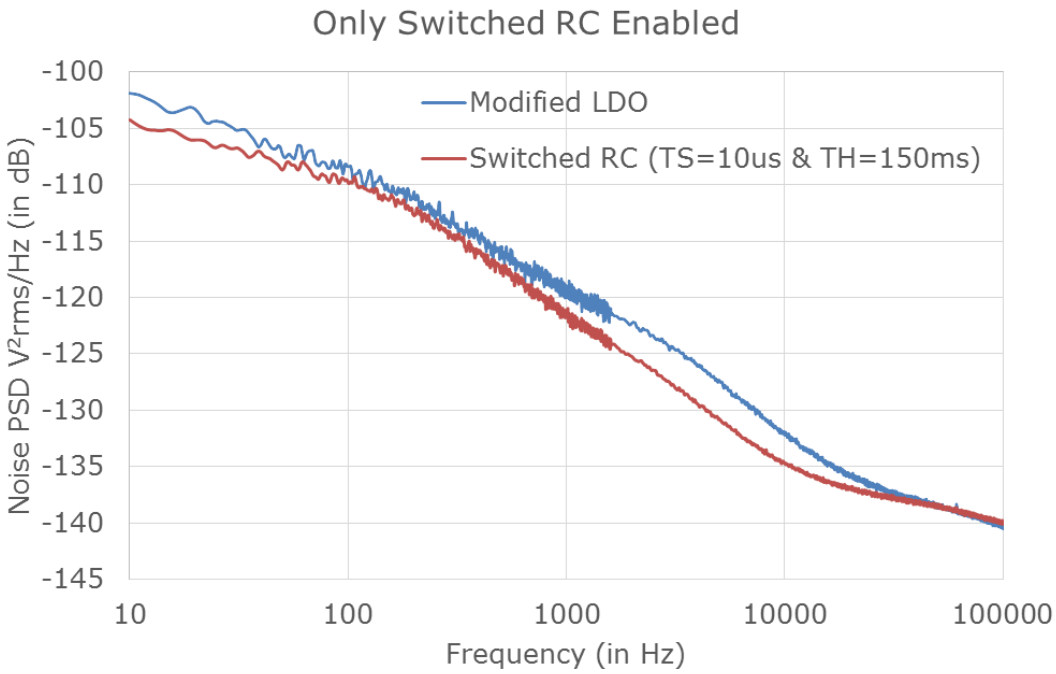

Figure 4.3.3 Switched RC BGR Noise reduction

Mode of LDO	**Integrated Noise**	
	nV^2_{RMS}	**μV_{RMS}**
Modified LDO without any noise reduction techniques enabled	9.08	95.3
Only Switched RC technique for BGR enabled	6.35	79.7
Reduction achieved	**2.72**	**52.2**

Table 4.3.3 Integrated Noise summary for Switched RC technique

4.3.3. Noise of Error Amplifier with Chopping

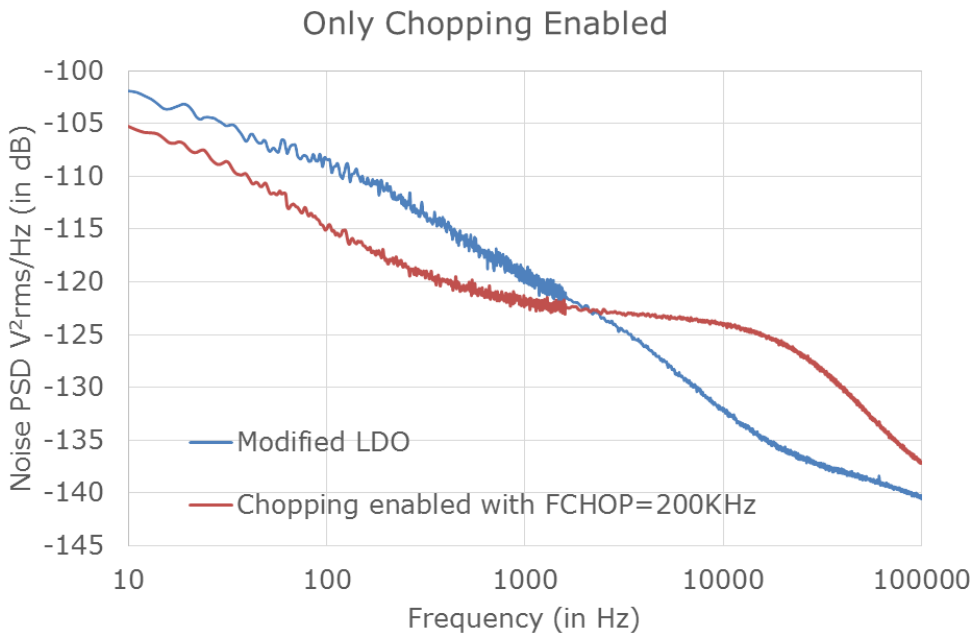

Figure 4.3.4 Noise reduction due to Chopping at 200kHz

NOTE: Even the overall noise after chopping only increases due to increase in the noise floor beyond 1kHz, it is the low frequency reduction which is critical. The high frequency increased noise floor will still be buried within the overall noise floor of the LDO and would not affect much of its noise performance.

Mode of LDO	**Integrated Noise**	
	nV^2_{RMS}	**μV_{RMS}**
Modified LDO without any noise reduction techniques enabled	9.08	95.3
Only Chopping enabled at F_{CHOP}=200kHz	15.1	123
Reduction achieved in the bands <2kHz	**3.67**	**60.63**

Table 4.3.4 Integrated Noise summary with Chopping

4.3.4. Bias Current Noise filtering

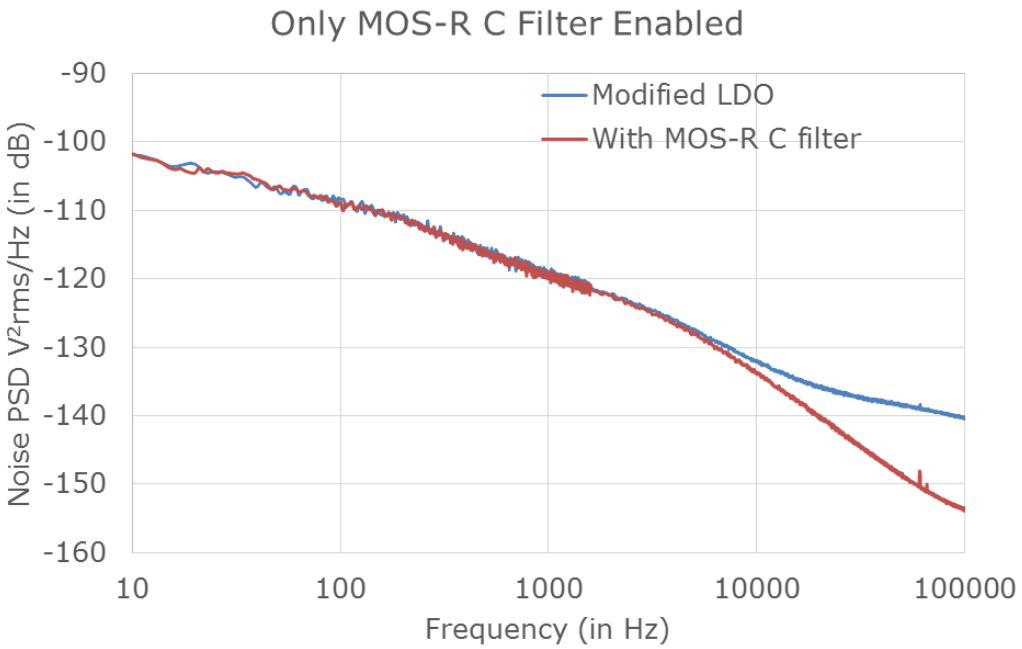

Figure 4.3.5 Noise reduction by MOS-R C filter

Mode of LDO	**Integrated Noise**	
	nV^2_{RMS}	**μV_{RMS}**
Modified LDO without any noise reduction techniques enabled	9.08	95.3
Only MOS-R C filter enabled	7.71	87.8
Reduction achieved	**1.37**	**37**

Table 4.3.5 Integrated Noise summary with MOS-R C filter

4.4. Output Ripple

Measurement conditions: VDD=4.5V, VOUT=1.8V, I_{LOAD}=10mA & C_{LOAD}=470nF

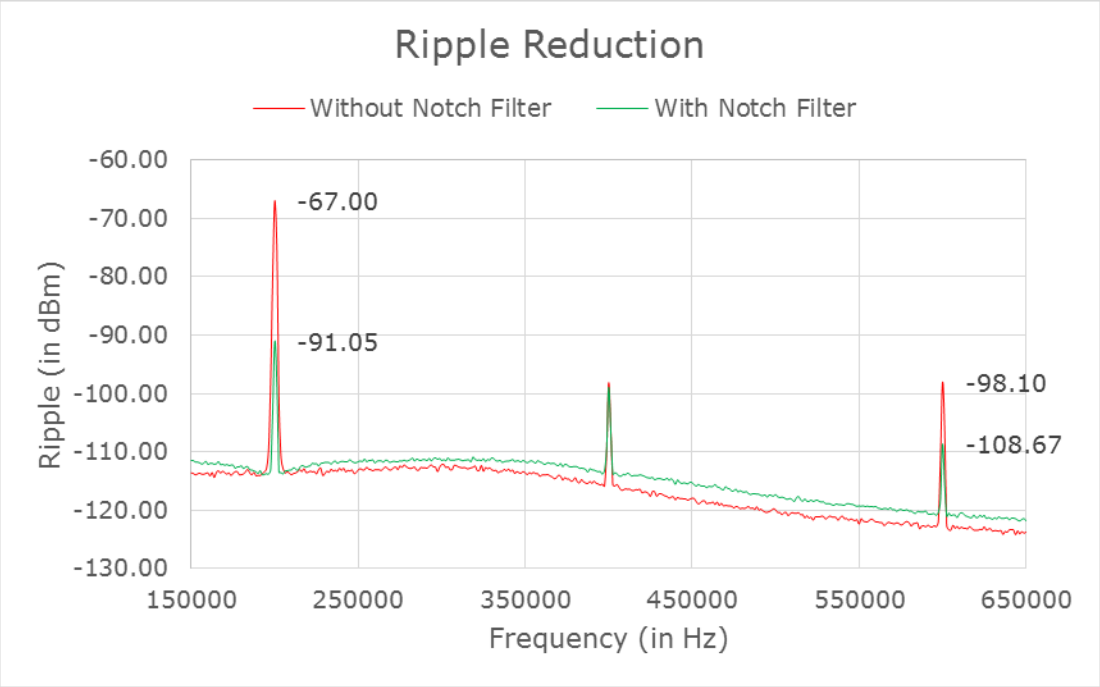

Figure 4.4.1 Ripple reduction using SC Notch filter

Mode of LDO		**Ripple**	
		dBm	**μV_{RMS}**
Ripple without SC notch filter at F_{CHOP} = 200kHz	1st harmonic	-66.14	110.21
	3rd harmonic	-97.27	3.06
Ripple with SC Notch at F_{CHOP} = 200kHz	1st harmonic	-90.11	6.98
	3rd harmonic	-107.48	0.94
Reduction achieved	**1st harmonic**	**-66.16**	**109.99**
	3rd harmonic	**-97.70**	**2.91**

Table 4.4.1 Ripple reduction summary

4.5. Power reduction in BGR

The quiescent current used in the BGR for this LDO is 8µA. With Sample and hold switched RC BGR, the on time of the BGR in each cycle is = Start up time of BGR (100µs) + sample time with buffer (100µs) = 200µs. The following table gives the summary of the noise reduction achieved due to this technique:

Mode of BGR	**I_Q (avg.)**	**Power (avg.)**	**Reduction (%)**
Original BGR	8µA	40µW	NA
T_s=10µs & T_H=10ms	$\frac{8 * 200\mu}{10m} = 0.16\mu A$	0.8µW	98%
T_s=10µs & T_H=150ms	$\frac{8 * 200\mu}{150m} = 0.01\mu A$	50nW	99.87%
T_s=10µs & T_H=1.5s	$\frac{8 * 200\mu}{1.5s} = 1nA$	5nW	99.99%

Table 4.5.1 Switched RC Sample-and-Hold BGR Power reduction summary

NOTE: If a Switched RC based Sample and hold method is used instead of MOS-R filter for bias current noise reduction as well, the overall reduction in power can be higher. In this case out of 52uA overall bias current of the LDO, with switched RC filter for both BGR and bias current noise filtering the overall reduction in I_Q = 10µA.

4.6. Power Supply Rejection Ratio

Measurement conditions: VDD=4.5V, VOUT=1.8V, I_{LOAD}=30mA & C_{LOAD}=470nF

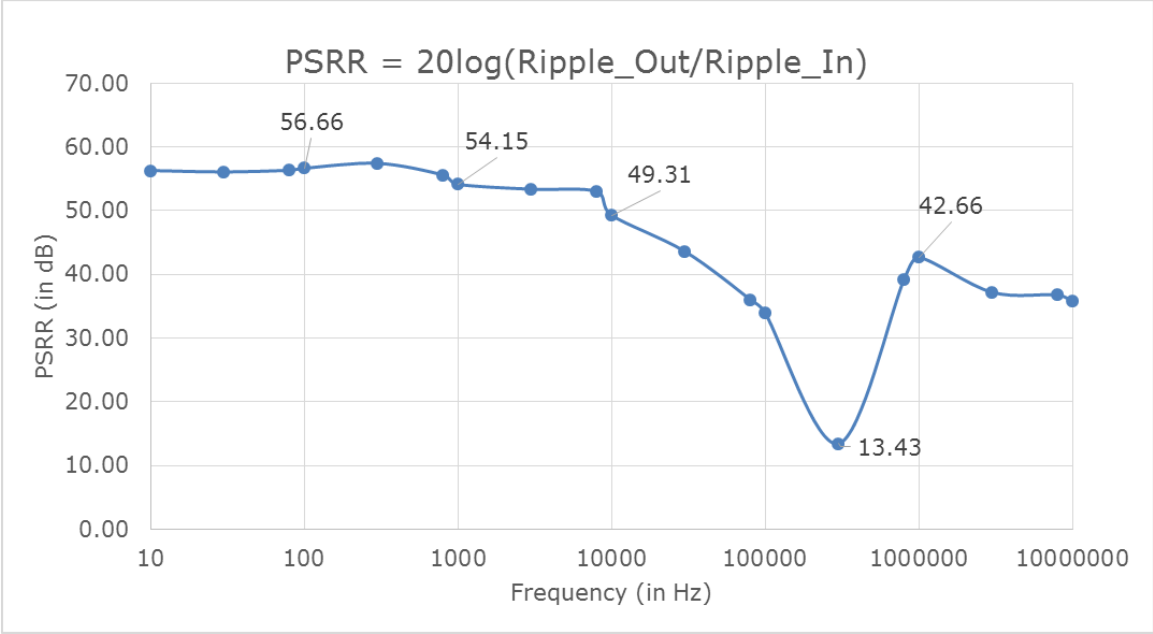

Figure 4.6.1 Low Noise LDO Power Supply Rejection Ratio

4.7. Static Load and Line Regulation

Measurement Conditions: VDD=4.5V, VOUT=1.8V & Temp=300K

4.7.1. DC Load Regulation

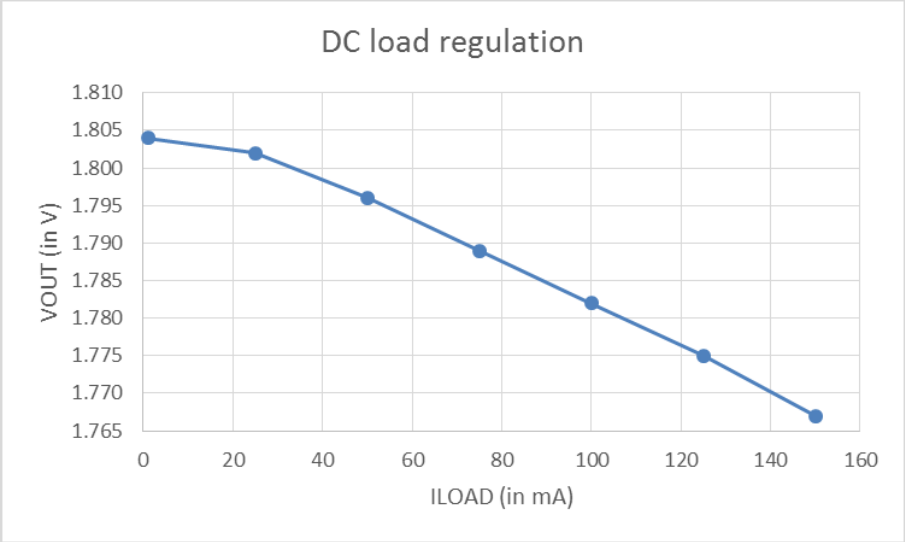

Figure 4.7.1 DC Load Regulation

4.7.2. Dc Line Regulation

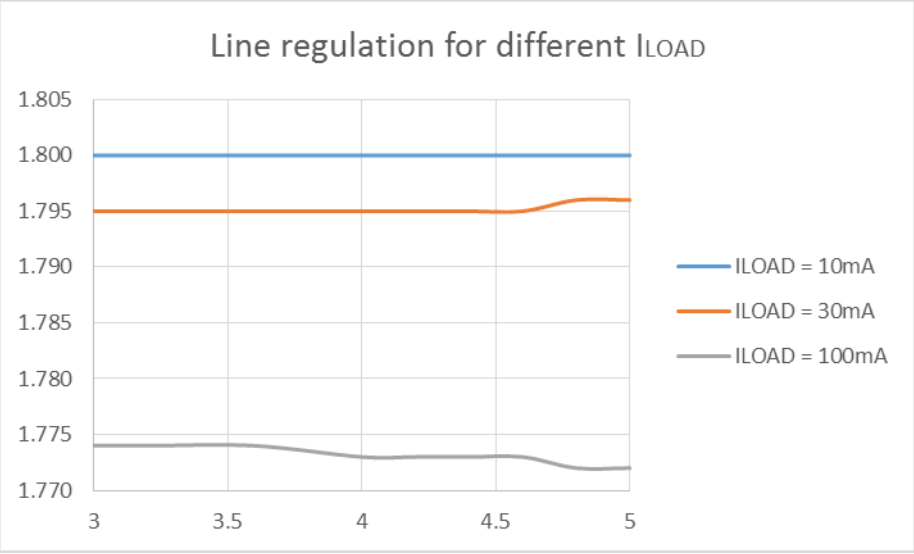

Figure 4.7.2 DC Line Regulation for different Load currents

4.8. Transient Load and Line response

Measurement Conditions: VDD=4.5V, VOUT=1.8V, C_{IN}=10uF, C_{OUT}=470nF & Temp=300K

4.8.1. Transient Load response

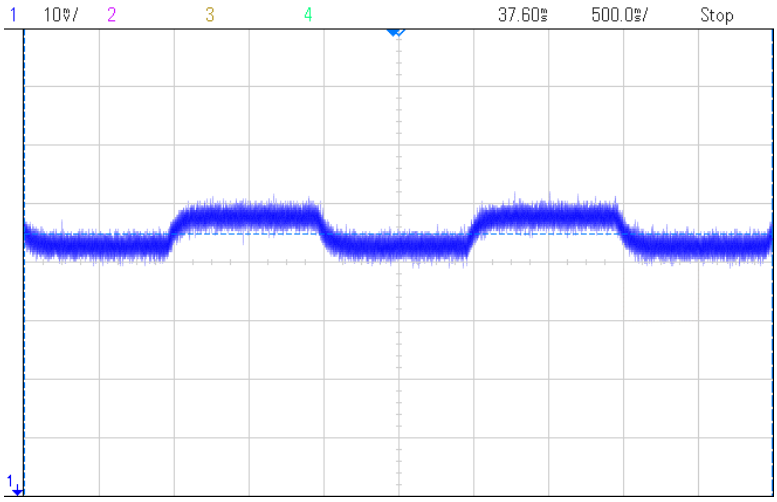

Figure 4.8.1 Transient response for I_{LOAD} 0 → 30mA

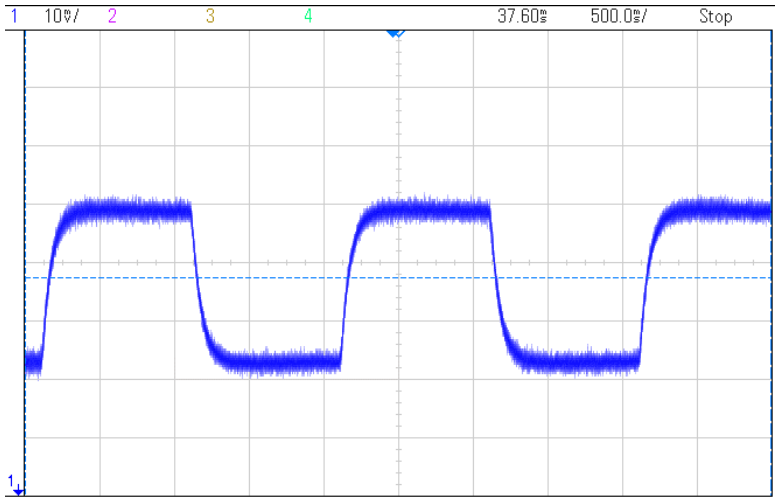

Figure 4.8.2 Transient response for I_{LOAD} 0 → 100mA

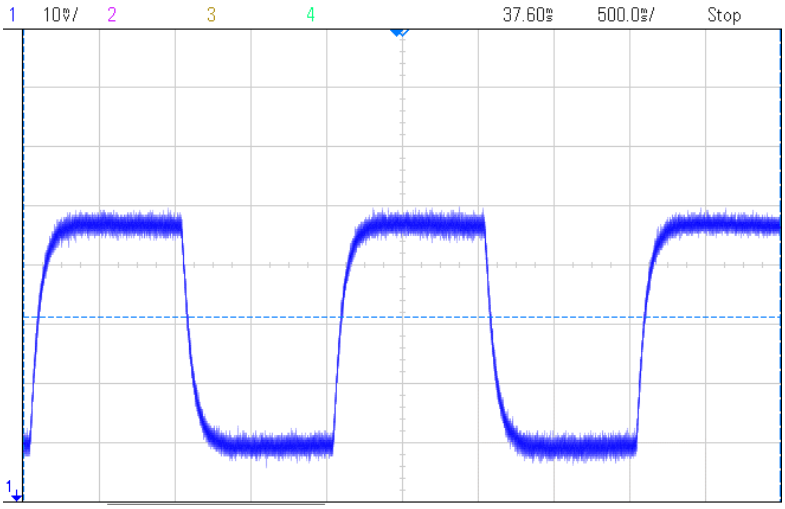

Figure 4.8.3 Transient response for I_{LOAD} 0 → 150mA

4.8.2. Transient Line response

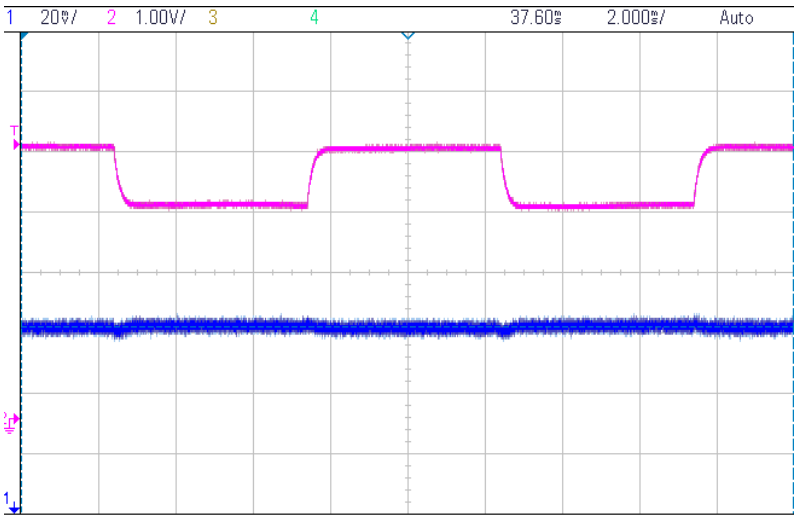

Figure 4.8.4 Transient response for VDD 4V → 5V Step

CHAPTER 5
THESIS SUMMARY AND FUTURE WORK

5.1. Summary

Ultra-low noise and low power design techniques for any generic wideband Low Drop-out (LDO) Regulator are proposed as a part of this research. Switched RC Bandgap, Drain-ended Chopping and bias current MOS-R based filtering techniques are used to reduce the noise of different blocks of any LDO. A switched capacitor based notch filter is used to reduce the chopping ripple. Sample-and-hold approach for the BGR results in a very low power architecture.

These techniques are implemented on TLV713XX family of LDO's from Texas Instruments Inc. available in the market. Design, layout, verification, board design and measurement were done as a part of the process. The layout area for the entire chip is 580µm x 580µm. The overall noise of the original LDO was reduced from 73µVrms to 15µVrms in the integration band of 10Hz to 100kHz. The area overhead incurred due to added techniques is 200µm x 200µm. The overall increase in the value of quiescent current due to these techniques is ~1µA.

The Low Noise LDO chip is characterized for the results using Dynamic Signal Analyzer & Spectrum analyzer and the measured results are in good agreement with the simulation results.

5.2. Future Work/Improvements

There are 2 major points which need to be worked on as a part of future work/improvements: 1. Reduction of input pair noise & 2. Integration of on chip oscillator for clock generation.

5.2.1. Reduction of Input pair Noise

As we saw in section 3.3.3, one of the major disadvantages of drain-end chopping is the fact that the input pair 1/f noise is not modulated. This is one of the major contributors of noise as is seen in the noise summary from simulation results. If we can reduce the input pair noise then we can achieve integrated noise numbers of <10μVrms.

One of the major techniques which was explored in order to reduce the input pair 1/f noise was the Switched Biasing technique [9]. In this technique, a cycling of MOS transistor between cutoff and saturation is used to reduce its intrinsic 1/f noise. The limitations of usage of this technique for our input pair was mainly due to integrating it in such a way that it does not affect the chopping process and choosing a proper frequency for turn on and turnoff in current domain without affecting the performance of the overall LDO. Thus if an innovative solution is found out to this problem and if switched biasing can be used, then that would reduce the input pair noise bringing down this LDO noise to <10μVrms.

5.2.2. Integration of on-chip Oscillator

In order to provide more flexibility for characterization an external clock was used for the test chip. This can be replaced by an on-chip low power and low area oscillator generating a clock of about 1MHz which can be used by different noise reduction techniques internally.

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