

VerilogA Modelling of Programmable  
Metallization Cells

by

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## ABSTRACT

There is an ever growing need for larger memories which are reliable and fast. New technologies to implement non-volatile memories which are large, fast, compact and cost-efficient are being studied extensively. One of the most promising technologies being developed is the resistive RAM (ReRAM). In ReRAM the resistance of the device varies with the voltage applied across it. Programmable metallization cells (PMC) is one of the devices belonging to this category of non-volatile memories.

In order to advance the development of these devices, there is a need to develop simulation models which replicate the behavior of these devices in circuits. In this thesis, a verilogA model for the PMC has been developed. The behavior of the model has been tested using DC and transient simulations. Experimental data obtained from testing PMC devices fabricated at Arizona State University have been compared to results obtained from simulation.

A basic memory cell known as the 1T 1R cell built using the PMC has also been simulated and verified. These memory cells have the potential to be building blocks of large scale memories. I believe that the verilogA model developed in this thesis will prove to be a powerful tool for researchers and circuit developers looking to develop non-volatile memories using alternative technologies.

## DEDICATION

*Dedicated to my parents*

*Narasimha Prasad BK and Rekha N Prasad*

## ACKNOWLEDGMENTS

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## CHAPTER 1

### INTRODUCTION

#### **1.1.Motivation**

Data storage has become a core component of all the electronics we use today. Ideally, data storage devices are required to be capable of storing large amounts of data and have short read and write times. A short read and write time implies that the time required to write data onto the device or the time required to read data from the device need to be minimized. In order to meet both of these requirements a two-tier memory system is used. The term computer storage is used to refer to a permanent high capacity memory like the hard disk of the computer. The data written on this type of memory is unaltered even on power down. This is typically implemented using non-volatile memory (NVM) such as Flash Memory. On the other hand the term computer memory is used to refer to the RAM of the computer. This is the instant storage that programs and applications running on the computer utilize to run at high speeds. The rate of development of these RAM memories in terms of speed and endurance has been far greater than that of NVM. Hence, there is a strong need to look into alternative memory technologies to bridge this gap between NVM and RAM.

Another reason for the ever growing need for alternative memory technologies is scaling [9]. In accordance with Moore's law the semiconductor industry is looking to double the number of ICs in a unit area of the chip every two years (Figure 1). This implies that we are now working with smaller transistors with gate lengths approaching 10nm. Figure 2 demonstrates that number of charges stored in these devices is getting smaller as well. Retention and detection of charges gets more difficult as the total charge

gets smaller. Also, the programming voltages need to be lower in these technology nodes.

[3]

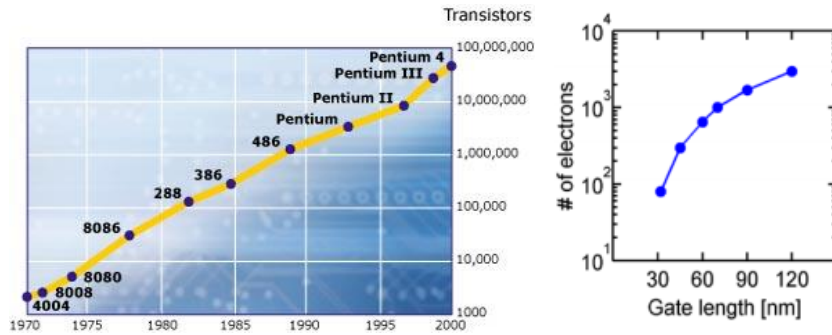


Figure 1 Moore's law

Figure 2 Number of electrons vs gate length

## 1.2. Introduction to resistive memories

The need for alternative memory technologies has led to the development of several new device types. Of these devices, the ones in which the resistance of a two-electrode element is changed by varying the applied potential across the electrodes are known as resistive memory devices. Typically, they are implemented using a metal-insulator-metal (MIM) structure [9]. Resistive memories can further be classified into several major sub-technologies. Some of the existing ReRAM memories are phase-change memory (PCRAM)[1], valence-change memory and ion-conducting bridging memory.

This thesis deals with ion-conducting bridging memory. These devices are also referred to as programmable metallization cells (PMC). They are based on formation of a conducting bridge between the two metal electrodes of the device. When a suitable voltage ( $V_{fwd}$ ) is applied across these elements, a conducting bridge is formed between the electrodes making the device operate in low resistance state. When a voltage of

opposite polarity is applied, the conducting bridge is dissolved and the device now operates in high resistance state.

Due to the proven stability and reliability of ion-conducting bridging memory this thesis deals with this class of resistive memory [2]. Figure 3 plots the endurance of these devices for both the high resistance ( $R_{off}$ ) and low resistance ( $R_{on}$ ) states. In Figure 3 it is observed that over a significant number of cycles the  $R_{on}$ ,  $R_{off}$ , and  $V_{th}$  remain consistent.

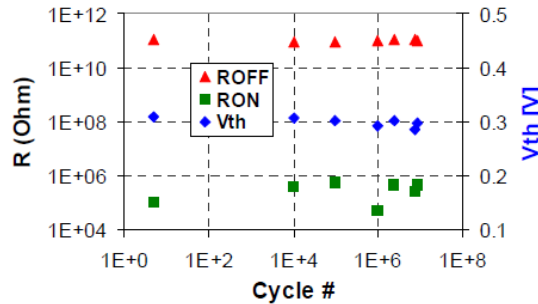


Figure 3  $R_{on}$  and  $V_{th}$  of a PMC over a large number of cycles [2]

Figure 4 demonstrates the retention capacity of these devices. Here, the ON and OFF resistance of the device were measured for 50 days. The devices were also exposed to various temperatures. Though the ON resistance of the device does increase slightly over time, the ratio of ON to OFF resistance is always more than  $10^5$ . [2]

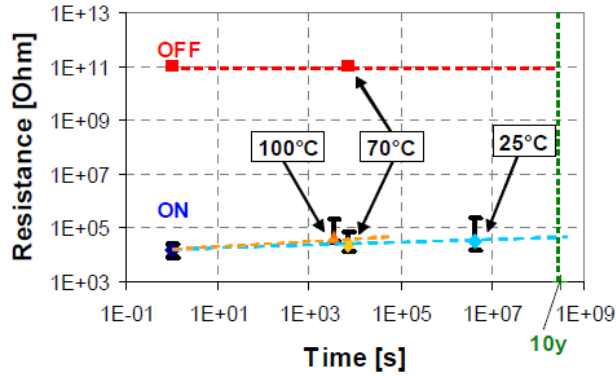


Figure 4 Ron and Roff of a PMC over a long period of time [2]

The density of memory i.e. the number of bits stored per unit area on chip is critical in order to reduce the overall size of the memory block. It can be seen from Figure 5 that these devices have multi-level programming capability which enables the storage of more than one bit on a single device.

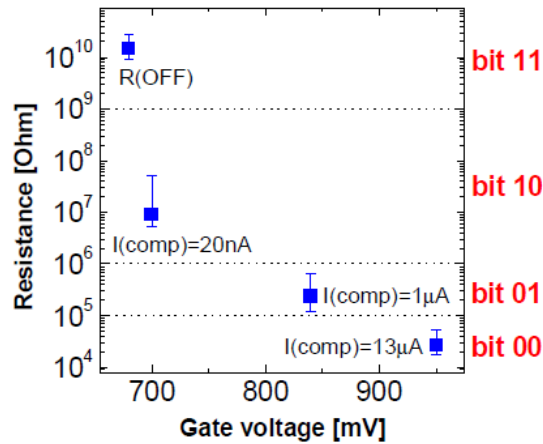


Figure 5 Multi-level programming ability of a PMC [2]

Figure 6 demonstrates the retention of multi-level programming of these devices.

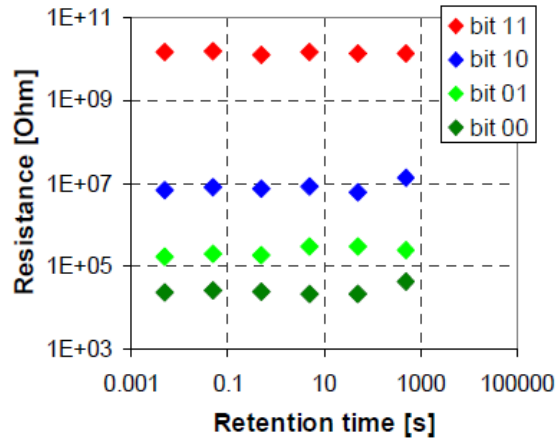


Figure 6 Different resistance levels of a PMC observed over a long period of time [2]

Given the proven stability, reliability and endurance of these devices it is fair to assert that these devices are capable of replacing traditional flash memories in the non-volatile memory sector. In order to develop memory arrays using these devices, there is a need for a model which replicates the behavior of these devices accurately in the circuit design environment. In this thesis a verilogA model has been developed for the PMC. DC simulations, pulsed transient simulations have been performed using this model. A memory cell has also been designed using this model. The data from a PMC device fabricated at Arizona State University has been matched to simulation results in order to prove the accuracy of the developed model.

## CHAPTER 2

### PROGRAMMABLE METALLIZATION CELLS

#### 2.1. Device Structure

The PMC is a two terminal device made up of an active electrode, an inert electrode and an electrolyte. The device primarily operates in either the low resistance state or high resistance state. This depends on presence or absence of a bridge between the two electrodes. One of the electrodes is called an active electrode and is made up of an electrochemically active metal such as Ag or Cu. The other electrode is made up of an inert material such as Ni or W. The usages of various combinations of these materials have been reported [4]. Table 1 indicates a few of these combinations

Table 1

Commonly used materials in the PMC [4]

Anode metal	Ag	Cu
Electrolyte	Cathode metal	
GexSy	W	W
GexSey	W, Pt, Ni	W
Ge-Te	TiW	TaN
GST	Mo	
As-S	Au	
ZnxCd1-xS	Pt	
Cu2S		Pt, Ti
Ta2O5		Pt, Ru
SiO2	Co	W, Pt, Ir
WO3	W	W
TiO2	Pt	
ZrO2	Au	
GdOx		W

Experimental results presented later in this thesis are from a device fabricated at Arizona State University which has Ag as the active electrode, Ni as the inert electrode and  $\text{Ge}_{30}\text{Se}_{70}$  as the electrolyte.

Figure 7 is a cross-section image of the device taken using a scanning electron microscope (SEM). The  $\text{SiO}_2$  layer is added to act as an insulator separating the device from the Si substrate.

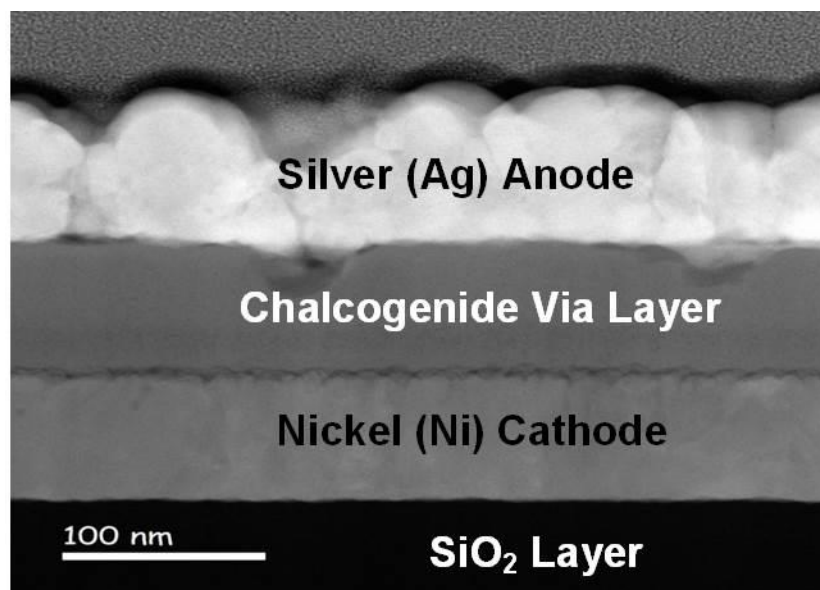


Figure 7 SEM image of PMC fabricated at ASU

## 2.2. Basic operation

The eventual goal is to use the device as a building block for memory. This is achieved by operating the device in primarily two operating states the low resistance state (LRS) and high resistance state (HRS). In the low resistance state (LRS), the device can be considered to be ON and it allows current to flow through it. In the high resistance



state (HRS), the device can be considered to be OFF and ideally, no current can flow through it. [8, 13]

For our analysis, one can assume that initially the device is in high resistance state (HRS) (section a in Figure 8) or OFF state. There is no conducting bridge between the electrodes. As a positive voltage greater than the forward threshold voltage ( $V_{\text{fwd}}$ ) is applied on the active electrode of the device, a bridge is formed between the two electrodes. The device can now conduct current through it (section b in Figure 8). The device is now in the low resistance state (LRS) or ON state. As the voltage is further increased, the effective radius of the bridge increases, reducing the resistance of the device. The device hence, allows more current to flow through it. If one allows the current in the device to increase to a very high value it is possible to damage the device. Hence, there is a need to set the maximum current that can flow through it, referred to as the compliance or programming current. While testing the device, this can be done by setting the maximum current delivered by the voltage source. While using this element as a memory element one can use a transistor to limit the current (section c in Figure 8). The device can be reset (or switched OFF) by reducing the voltage applied. When a voltage of reverse polarity with magnitude greater than the reverse threshold voltage of the device ( $V_{\text{rev}}$ ) is applied the conducting bridge in the electrolyte dissolves and the device enters a high resistance state (HRS) (section d in Figure 8) or OFF state. It now allows only small amounts of current to flow through it.

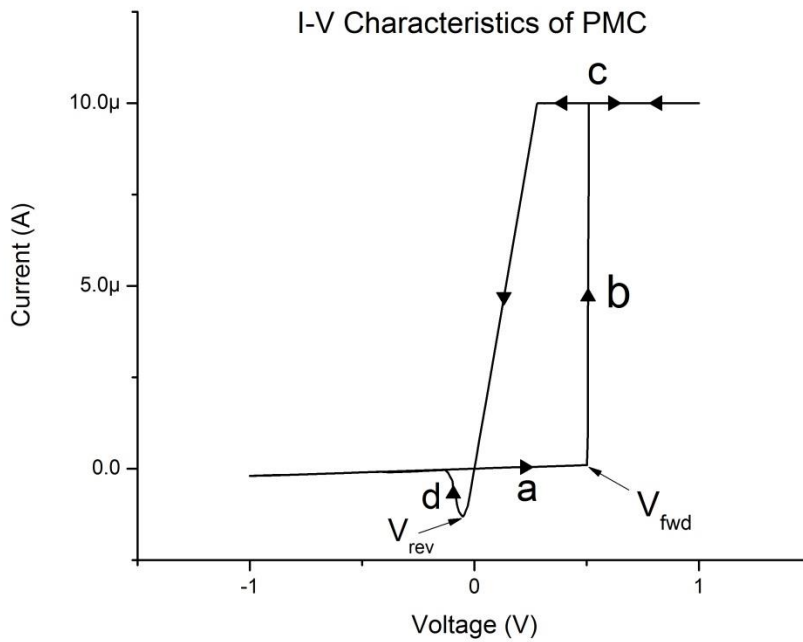


Figure 8 I-V characteristics of a PMC

This I-V characteristic of the device gives an indication of the input voltage required for testing the device. If a simple increasing (or decreasing) DC sweep is done then the hysteresis behavior of the device cannot be observed. Hence a slow positive ramp is used to initially increase the voltage until the current reaches compliance current and then a slow negative ramp is used to decrease the voltage and cause the device to reset.

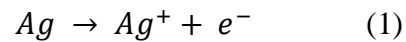
### 2.3. Physical description of the operation

The formation of the conducting bridge through the application of a positive voltage can be attributed to a set of oxidation and reduction reactions along with ion-

transport in the electrolyte [4]. The formation of the conducting bridge can be broken down into three steps.

### Step 1 - Oxidation

When positive potential is applied to the active electrode (anode), there is an oxidation reaction which results in the formation of cation. This explains the need for an electrochemically active material for the anode. When Ag is used as the anode, the oxidation reaction is as follows >



### Step 2 – Ion – transport

Under the influence of the electric field, these  $Ag^+$  cations travel through the electrode to the inert electrode (cathode).

### Step 3 – Reduction

Once the cation reaches the inert electrode, it recombines with an electron and gets deposited on the cathode surface. This process of electro-crystallization is enhanced by the electric field and as a result a metal filament starts growing from the cathode towards the anode.

When the metal filament grows back towards and eventually touches the anode, a conducting bridge is formed between the two electrodes and the device can conduct current. Figure 9 indicates the formation and dissolution of the conducting bridge in various regions of the I-V plot.

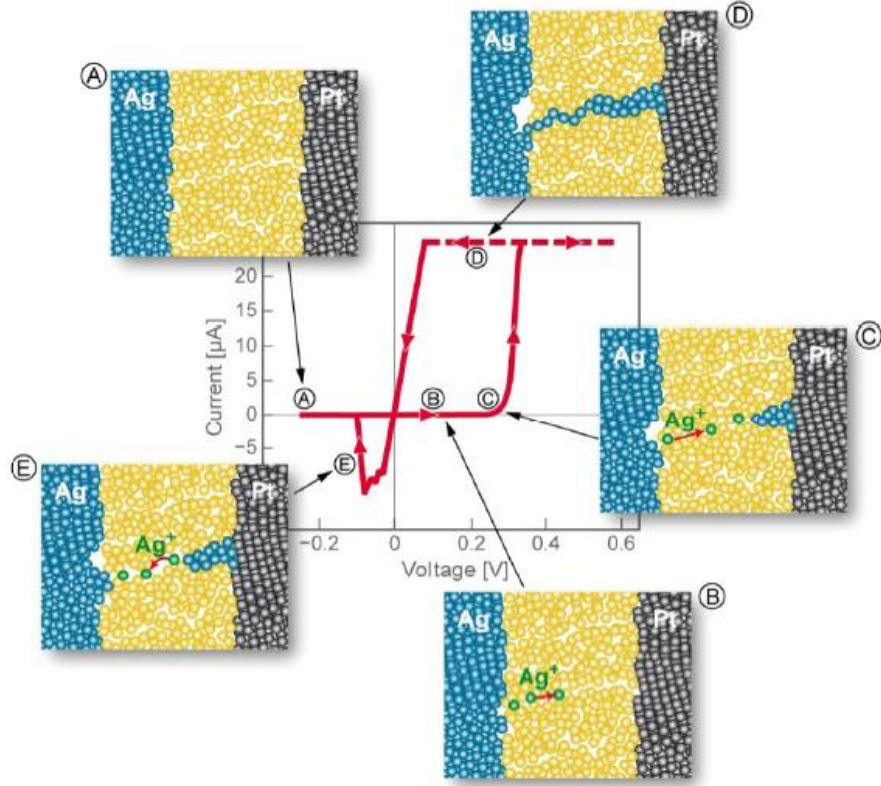


Figure 9 Conducting bridge during various section of I-V characteristics of PMC [4]

## 2.4. Current Equations

The currents generated during the formation and dissolution of the conductive bridge can be divided into two parts.

### 2.4.1. Electrode current

During the write operation, before the conductive bridge is formed there is oxidation and reduction occurring at the electrodes. Ag from the anode is oxidized and the  $\text{Ag}^+$  ions are reduced at the cathode. The current associated with these electrochemical reactions can be described mathematically using the Butler-Volmer equation [5]

$$I = I_o \left[ \frac{C_o(0, t)}{C_o^*} e^{\frac{\alpha\eta}{kT/q}} - \frac{C_r(0, t)}{C_r^*} e^{-\frac{(1-\alpha)\eta}{kT/q}} \right] \quad (2)$$

In equation 2,  $I_o$  is the equilibrium current which refers to the current when the rate of reaction at anode is equal to the rate of reaction at the cathode. The first term inside the bracket refers to cathodic current and the second term refers to anodic current.  $C_o^*$  and  $C_r^*$  are bulk concentrations,  $\alpha$  is the transfer co-efficient and  $\eta$  is the current-overpotential.

The exponential terms in this equation indicates the change in energy barrier for oxidation and reduction when an external potential is applied to the system. Figure 10 is a plot of electrode current vs  $\eta$ . The curve,  $i_a$ , represents the anodic current and  $i_c$  represents cathodic current. The total current indicated by the solid line is the sum of anodic and cathodic currents.

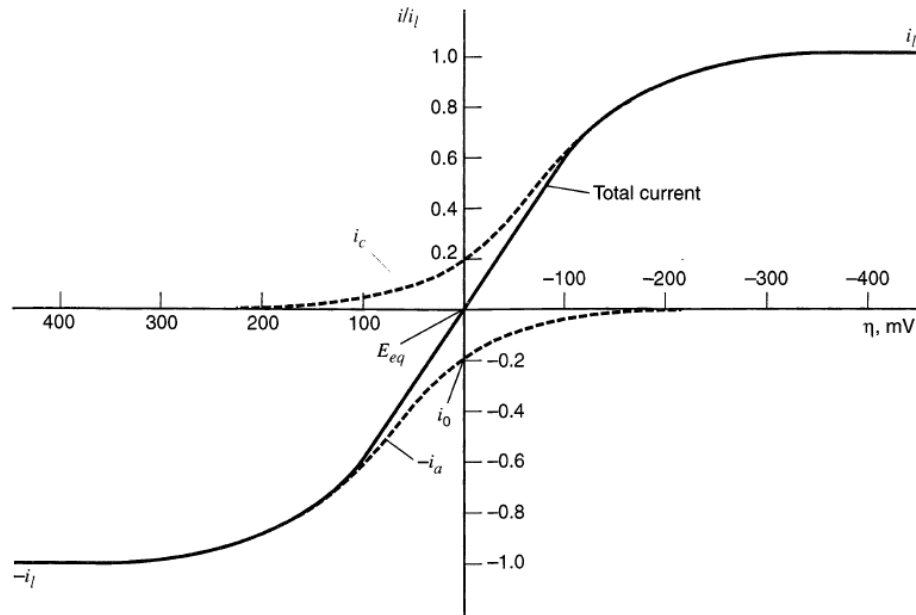


Figure 10 Electrode current vs over-potential [5]

#### 2.4.2. Ion-transport current (Mott-Gurney ion hopping current)

This is the current due to transport of the cation formed at the anode through the electrolyte until it reaches the cathode. The ion moves from one position in the electrolyte to another position in the electrolyte by overcoming a potential barrier. The probability of an ion hopping from one position to the other in unit time is expressed as

$$w = v_o e^{(-W_a/kT)} \quad (3)$$

where  $v_o$  is the vibration frequency of the ions and  $W_a$  is the activation energy. [6] Upon the application of a potential, the probability of a hop in the direction of the electric field,  $E$ , decreases while the probability of the jump against the electric field increases. Hence the mean drift velocity can be calculated as

$$v_d = 2av_o e^{(-W_a/kT)} \sinh(eEa/2kT) \quad (4)$$

where  $a$  is hopping distance. The mobility of these carriers is then defined as

$$\mu = \frac{v_d}{E} \quad (5)$$

where  $E$  is the applied electric field. The drift current density resulting from the movement of the ions can then be estimated as

$$J = qn\mu E \quad (6)$$

where  $n$  is the number of free carriers per cubic centimeter. Hence the drift current density due to the transport of ions from anode to the cathode is expressible as

$$J = 2ZeN_i av_o e^{(-W_a/kT)} \sinh(eEa/2kT) \quad (7)$$

where  $Z$  is the total number of charged ions and  $N_i$  is the density of ions in the electrolyte. This is known as the Mott-Gurney equation [15].

## CHAPTER 3

### MODELLING THE PMC CONDUCTING BRIDGE

The ability to simulate a circuit before fabrication is one of the most valuable tools available to an engineer today. It allows one to predict and analyze the behavior of the circuit designed. Circuit simulation helps predict the behavior of the various circuit elements when they are connected together. Often, this task is mathematically intensive and too rigorous to do manually.

Hence, for any new emerging device there is a great need to develop models for devices which can be used in circuit simulations. Previously, a TCAD model [19] and a mathematical model for PMC have been developed [17]. There have also been attempts to develop verilogA models for the PMC[18,19,20]; but they have been limited to the I-V characteristics or transient pulse simulations. The model developed here is a comprehensive verilogA model which can be used to replicate both the I-V characteristics and transient pulsed behavior of the PMC and also its behavior when used in a 1T 1R memory cell. In this thesis the multi-level programming ability of the PMC using the verilogA model will be demonstrated.

#### **3.1. Equations used for modelling**

In the previous chapter it was stated that the change in the state of the device from LRS to HRS and vice-versa occurs due to the formation of a conducting bridge between the two electrodes. The device is modelled by replicating the formation of the conducting bridge. The rate of formation of this conductive bridge depends on the rate at which the cations are reduced at the cathode. This in turn depends on the rate at which the cations

are able to move through the electrolyte to the cathode. This is given by the Mott-Gurney equation (Equation 7). The current density from the Mott-Gurney equation can be related to the rate of change of height of the conducting bridge as follows

$$N_m dh = \frac{J}{Ze} dt \quad (8)$$

where  $N_m$  is the density of the metal [7].

By substituting the Mott-Gurney equation into Equation. 7, the rate of change of height of the conducting bridge can be described as

$$\frac{dh}{dt} = 2 \frac{N_i}{N_m} a v_o e^{(-W_a/kT)} \sinh\left(\frac{qEa}{2kT}\right) \quad (9)$$

This can be further reduced as

$$\frac{dh}{dt} = v_h e^{(-W_a/kT)} \sinh\left(\frac{\alpha qV}{kT}\right) \quad (10)$$

where

$$v_h = 2 \frac{N_i}{N_m} a v_o \quad (11)$$

and

$$\alpha = \frac{Za}{2d} \quad (12)$$

where V is the voltage applied across the device

When there is a reset of the device, we can think of the dissolution to be occurring laterally. Hence, there is a change in the effective radius. The rate of change of the effective radius can be modelled as

$$\frac{dr}{dt} = v_r e^{(-W_a/kT)} \sinh\left(\frac{\beta qV}{kT}\right) \quad (13)$$



where  $v_r$  and  $\beta$  are fitting parameters. The equations 10 and 13 give us the rate of change of height and effective radius of the conducting bridge. Both of these are used to obtain the dimensions of the conducting bridge. The dimensions of the conducting bridge can then be used to model the resistance across the device.

There are two components which act together to give the overall resistance of the device. The first one is the resistance through the electrolyte. This can be evaluated as

$$R_e = \frac{\rho_e L}{\pi(r_{cell}^2 - r^2)} \quad (14)$$

The second component is the resistance of the conductive bridge. This is given as

$$R_f = \frac{\rho_f h + \rho_e(L - h)}{\pi r^2} \quad (15)$$

Both of these resistances are in parallel with each other. Therefore, the overall resistance can be calculated as

$$\frac{1}{\left(\frac{1}{R_e} + \frac{1}{R_f}\right)} \quad (16)$$

Figure 11 shows what  $R_{cell}$ ,  $r$ ,  $L$  and  $h$  used in the above equations refer to.

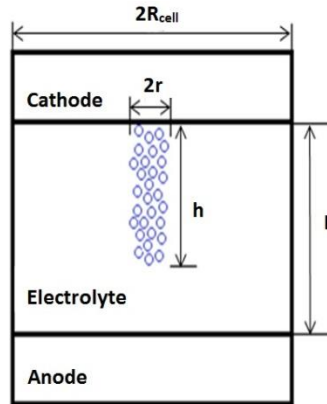


Figure 11 Various parameters used in verilogA code

The following table indicates all the values used during simulation

Table 2  
Parameters used in the verilogA code

Symbol	Quantity	Value
K	Boltzmann's constant	8.617e-5 eV/K
T	Room temperature	300.15K
$v_h, v_r$	Velocity co-efficient	5m/s
$W_a$	Activation energy	0.4eV
L	Distance between the electrodes	60nm
$R_{cell}$	Radius of PMC device	2.5 $\mu$ m
$r_{min}$	Minimum radius of the filament	0.1nm
$h_{min}$	Minimum height of the filament	0.1nm
A	Hopping distance	48nm
A	Fitting constant	0.4
B	Electric field fitting constant	0.086 (V>0) 0.164 (V<0)
Q	Charge of an electron	1.602e-19 C
$N_A$	Avogadro's constant	6.0221413e23 mol <sup>-1</sup>
$\rho_{Ag_2Se}$	Molar mass of Ag <sub>2</sub> Se	294.7 g/mol
$N_{Ag_2Se}$	Density of Ag <sub>2</sub> Se	8.22 g/cm <sup>3</sup>
Pe	Electrolyte resistivity	8e3 $\Omega$ cm
Pf	Filament resistivity	2.3e-6 $\Omega$ cm

### 3.2. Flow diagram of bridge formation and dissolution

The device is modelled as shown in Figure 12. It is first determined whether the voltage across the device is greater than the forward threshold voltage,  $V_{\text{fwd}}$ . If it is then the height of the conducting bridge is first increased using the Equation 10. Once the height is equal to the distance between the two electrodes i.e.  $L$ , the effective radius of the conducting bridge is increased. This is done using Equation 13. The variable “state” which is shown in the diagram will be discussed later in Sec. 3.3. At any point if the current through the device is equal to compliance current  $I_{\text{comp}}$ , then the effective radius and height of the device is set to zero.

If the voltage across the device is determined to be less than reverse threshold voltage  $V_{\text{rev}}$ , then the dissolution of the conducting bridge is simulated by decreasing the effective radius of the filament and then reducing the height of the filament.

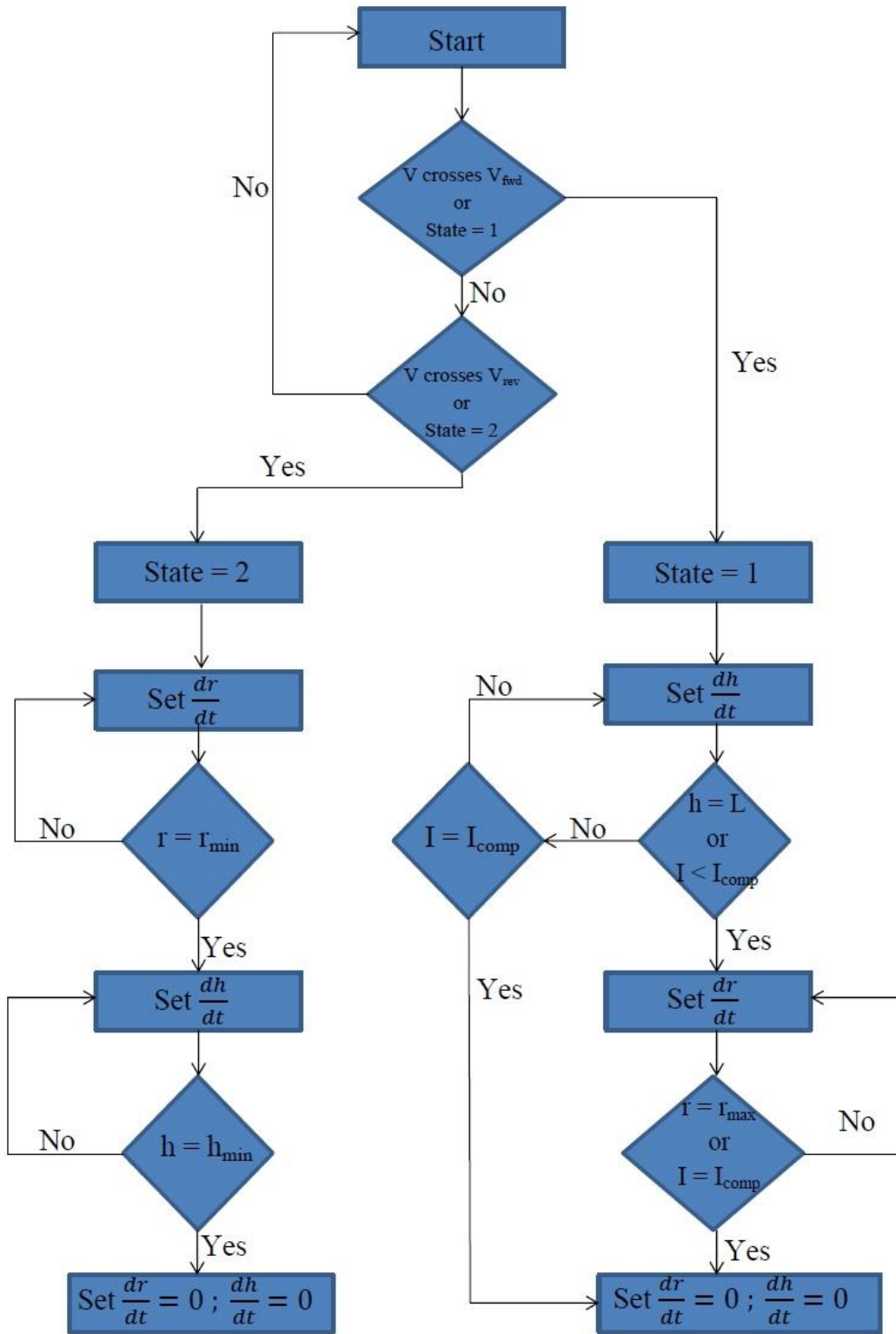


Figure 12 Flow diagram of verilogA code

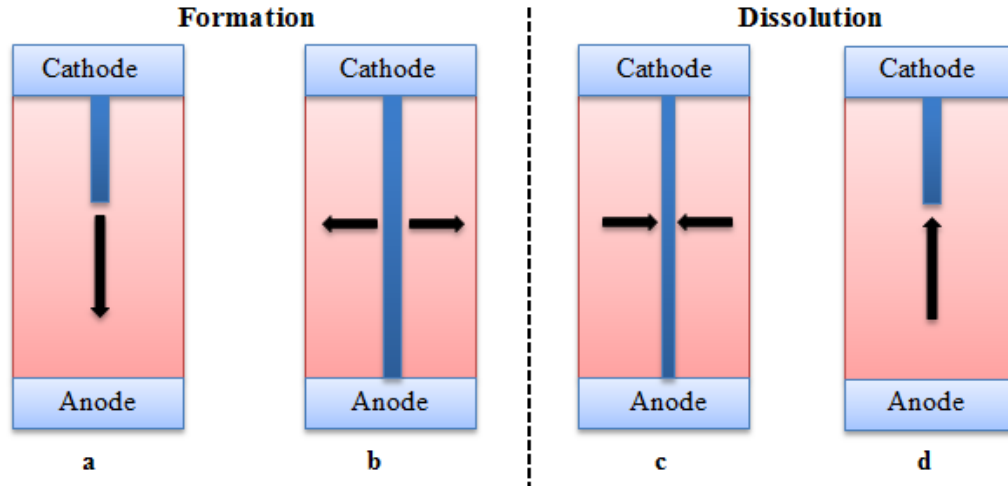


Figure 13 Order of occurrence of events during bridge formation and dissolution

Figure 13 shows the formation and dissolution of the conducting bridge. Figure 13a and 13b show the formation of the conducting bridge while Figure 13c and 13d show the dissolution of the conducting bridge. First the bridge starts forming at the cathode. The height of the conducting bridge continues to grow until it reaches the anode. After the maximum height has been reached, the conducting bridge starts growing laterally. When there is a reset voltage applied across the device, the conducting bridge starts shrinking laterally until its effective radius is  $R_{\min}$ . Then, the height of the conducting filament is reduced to  $H_{\min}$ .

### 3.3. Implementation of the filament growth and dissolution

The implementation of the model uses various flags whose status is determined by the voltage level across the PMC device. The “state” flag is defined as follows :

- a. State = 0 ; if  $V$  crosses  $V_{\text{fwd}}$  while decreasing or  $V$  crosses  $V_{\text{rev}}$  while increasing
- b. State = 1 ; if  $V$  crosses  $V_{\text{fwd}}$  while increasing

c. State = 2 ; if  $V < V_{rev}$  while decreasing

Initially the “state” flag is set to zero. When the voltage increase above  $V_{fwd}$  then state changes to one. Changing the state to one starts the change in dimensions of the filament at the rate of  $dh/dt$  and  $dr/dt$  as explained earlier, but the dimensions are limited by the physical dimensions of the device and the compliance current of the device. As the voltage starts decreasing and crosses  $V_{fwd}$  the state is set to zero. When the voltage falls below  $V_{rev}$ , then the state is set to two and the effective radius is reduced at the rate  $dr/dt$  until it reaches  $R_{min}$ . Then, the height is reduced until it reaches  $H_{min}$ .

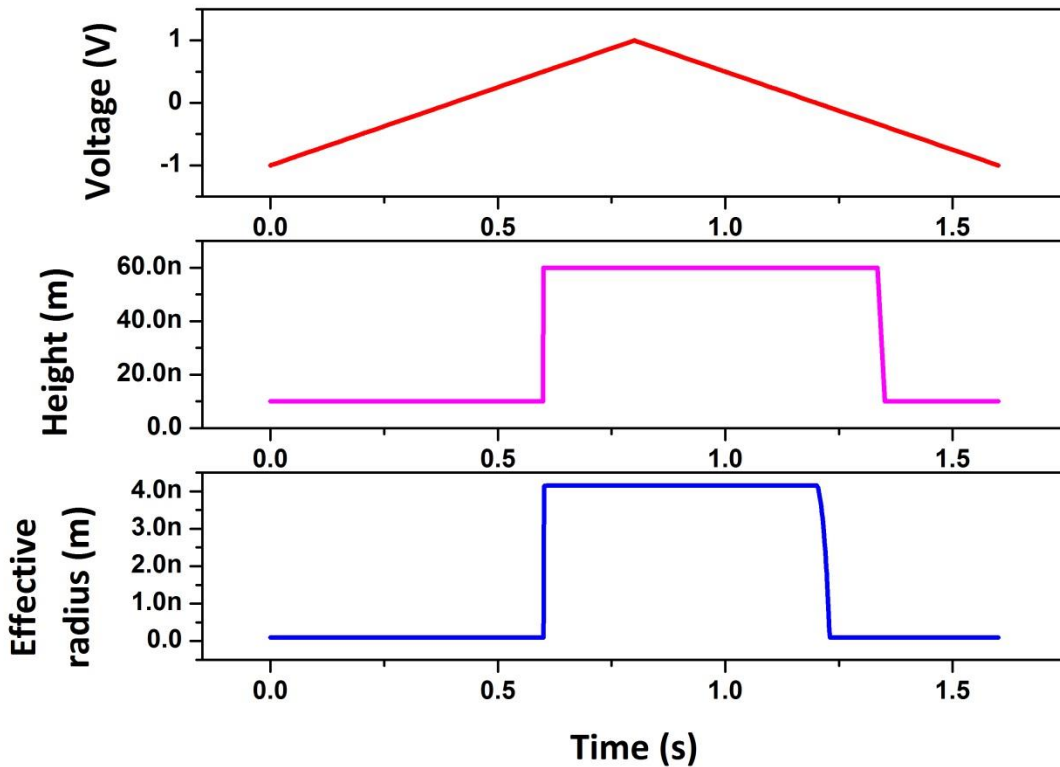


Figure 14 Formation of the conducting bridge on application of voltage across PMC model

Figure 14 plots the effective radius and height of the conducting bridge as a function of time. These are results from the verilogA model with compliance current  $I_{\text{comp}}$  equal to  $100\mu\text{A}$ . The first plot shows the voltage across the device. It can be seen that as soon as the voltage crosses the  $V_{\text{fwd}}$  threshold voltage, the height starts to increase. Once it reaches the maximum possible height, the conducting bridge starts growing laterally. Also, it can be seen that when the voltage crosses  $V_{\text{rev}}$  threshold voltage, the effective radius first decreases to the minimum possible value and then the height starts decreasing. It should be noted that the minimum height and effective radius are non-zero. This is because physically the atoms forming the conducting bridge can never be completely eliminated. There will be some Ag atoms of the conducting bridge always present in the device. The second graph shows the current flowing across the device. It can be observed that the compliance current is set to  $100\mu\text{A}$ .

### **3.4.Calculation of resistance of the PMC**

The flag “store” is used to determine the point at which change in dimensions of the filament start affecting the resistance of the device. The resistance of the PMC is defined using store flag as follows –

- a. Store = 0 ;  $R = R_{\text{off}}$
- b. Store = 1 ; R is defined by Equation 16

For the sake of simplicity, it is assumed that the resistance of the device is equal to  $R_{\text{off}}$  until the bridge reaches the anode. What this means is that initially, the resistance of the device is  $R_{\text{off}}$  and even when the voltage applied across the device is greater than  $V_{\text{fwd}}$ , the resistance remains equal to  $R_{\text{off}}$  until the height of the conducting bridge is equal

to the distance between the two electrodes. As the soon as height of the conducting bridge is equal to distance between the electrodes the store flag is set to one and resistance is calculated according to Equation 16.

When the voltage drops below  $V_{rev}$  the store flag already set to one. This implies that the resistance is calculated according to Equation 16. Once the effective radius and height of the PMC have been reduced to  $R_{min}$  and  $H_{min}$  respectively then the store flag is set to zero. This implies that the resistance of the device is set to  $R_{off}$  ( $5M\Omega$ ).

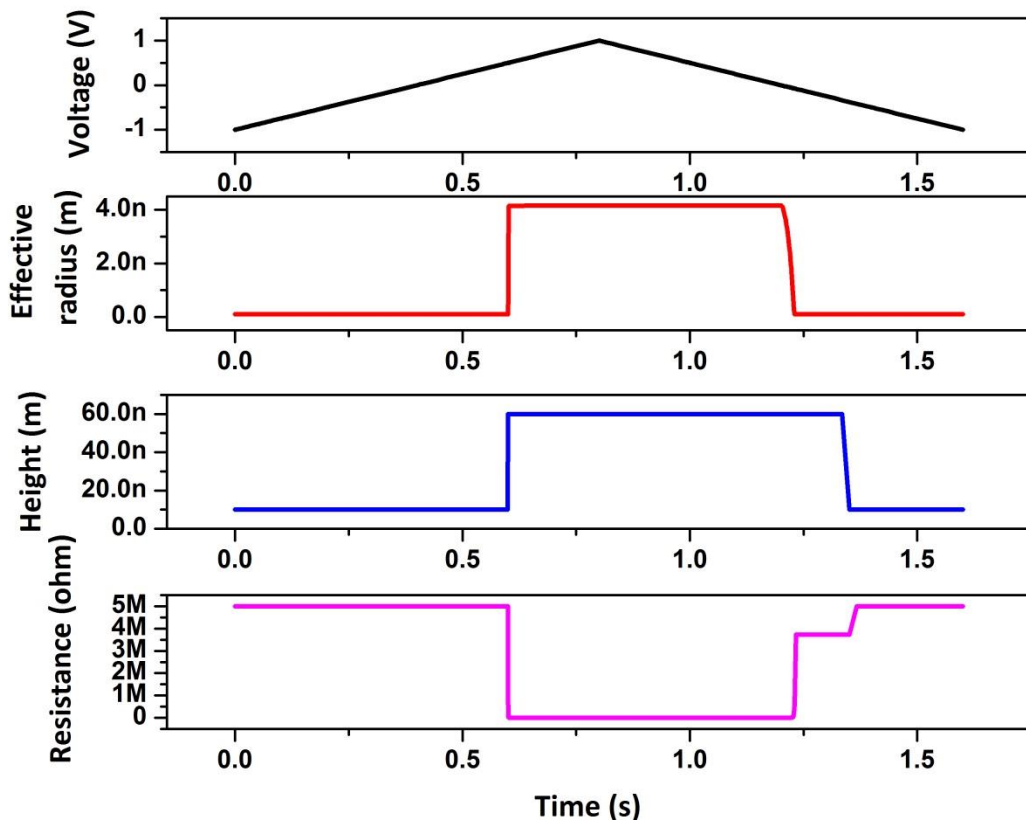


Figure 15 Change in resistance of PMC

Figure 15 shows how the effective radius and height of the conducting bridge control the resistance of the device. It can be seen that when the effective radius and height of the conducting bridge are at their minimum values, then the resistance of the



device is set to  $R_{off}$  ( $5M\Omega$ ). When the height of the conducting bridge becomes equal to the distance between the two electrodes the resistance of the PMC decreases. This results in increase in the current flowing through the device. Similarly when the effective radius and height return to their minimum values the resistance of the PMC increases to  $R_{off}$  which is  $5M\Omega$ .

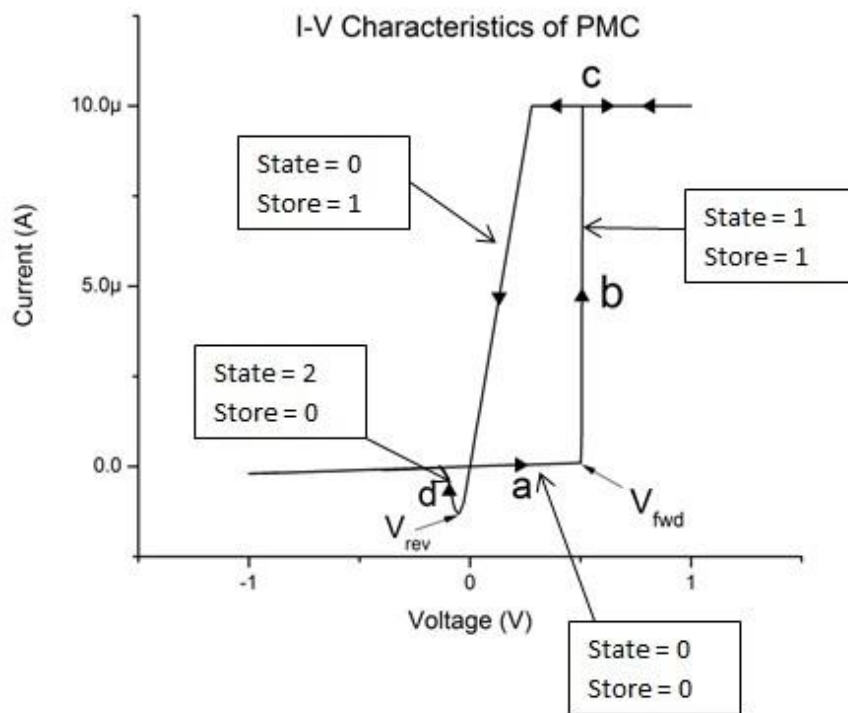


Figure 16 Value of flags used in verilogA code during different stages of PMC operation

Figure 16 indicates the value of the “state” and “store” flags in various regions of the I-V characteristics of the PMC.

## CHAPTER 4

### DC AND TRANSIENT MODELLING

In this chapter, we will discuss the DC and transient testing methodology for a PMC, the various results obtained from the PMC verilogA model and also compare these results with the experimental data obtained from testing the PMC fabricated at Arizona State University.

#### **4.1.DC modelling**

In order to test the DC characteristics of the PMC, a slow increasing ramp followed by a slow decreasing ramp was used. This is done since it is known that the value of current for a given voltage depends on whether the conducting bridge has been formed or not. For example let us assume that  $V_{fwd}$  threshold is 0.5V and  $V_{rev}$  threshold is -0.1V. If the voltage is applied across the device is 0.2V, then there are two possibilities. First, if the device has not crossed the  $V_{fwd}$  threshold previously. Then there is no conducting bridge and hence no current will flow through the device. In the second scenario the device has crossed the  $V_{fwd}$  threshold previously and there will be some current due to the presence of a conducting bridge. Hence, a simple DC sweep of voltages which does not take into account the previous input voltage applied across the device cannot be used. Figure 17 shows a typical voltage applied across a PMC when measuring its DC characteristics.

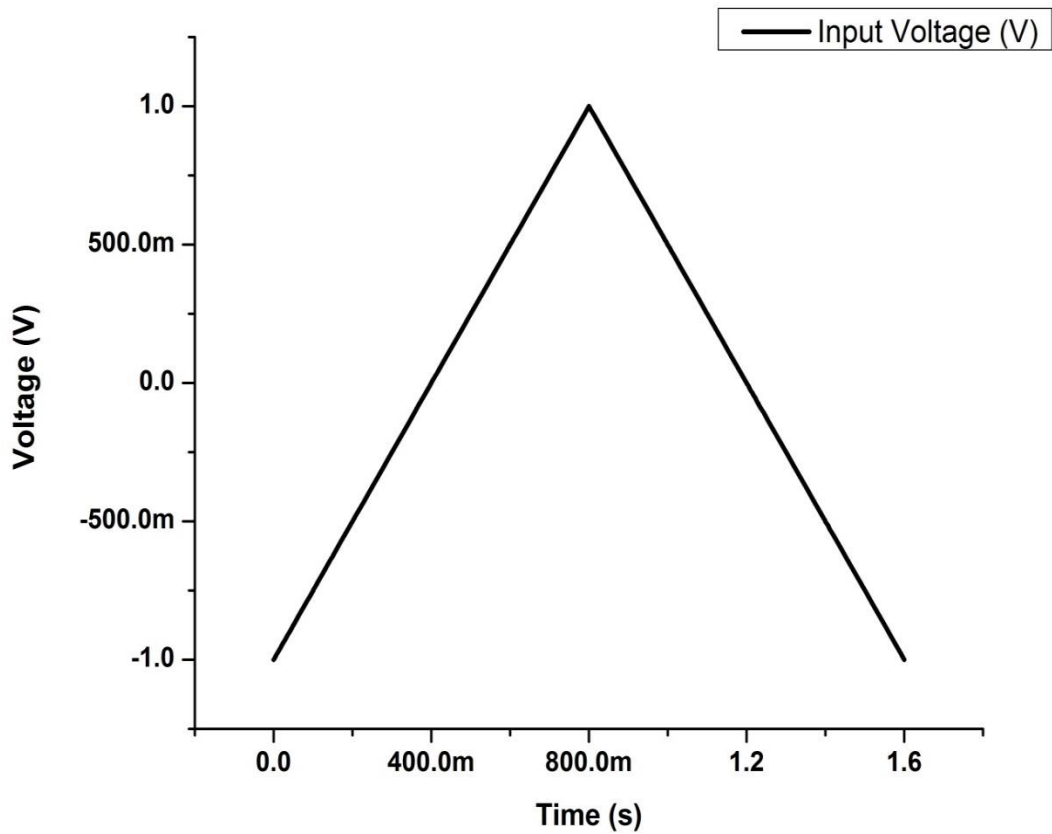


Figure 17 Input voltage applied across PMC to study its DC behavior

#### 4.1.1. I-V characteristics

For the purpose of obtaining the I-V characteristics of the device a transient analysis was carried out with the voltage waveform shown in Figure 17. In the verilogA code, there is an option for setting the compliance current through the device in the code. The model was tested with various compliance currents. Figure 18 shows the I-V characteristics from the verilogA model with compliance current varying from  $10\mu\text{A}$  to  $1\text{mA}$ .

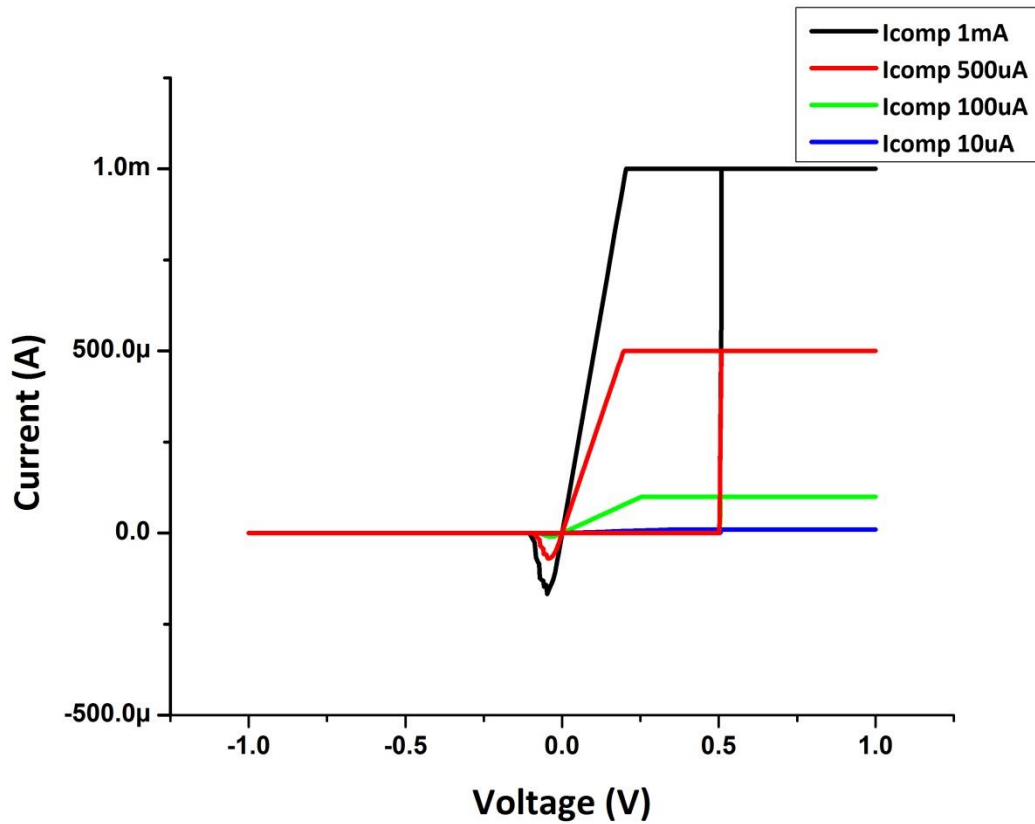


Figure 18 I-V characteristics of PMC with different compliance currents

The different values of compliance currents were realized by using different radii of the conducting filament. The variation of effective radius of the filament for different compliance currents is shown in Figure 19

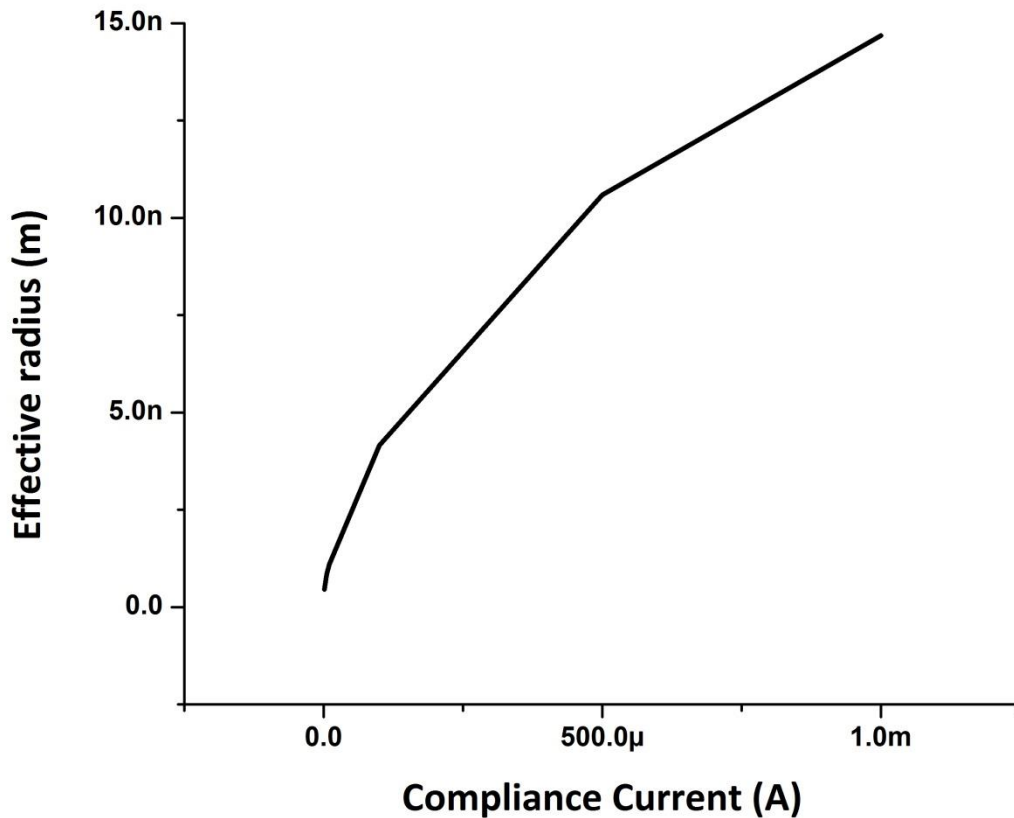


Figure 19 Effective radius of the conducting bridge formed vs compliance current

The I-V characteristics obtained from the verilogA model were matched with data obtained from testing the fabricated PMC device. The equipment used for testing are the Semi Probe PSM 1000 Probe Station and Agilent 4156C Precision Semiconductor Parameter Analyzer. The parameter analyzer was used to apply the input voltage ramp across the device and monitor the current through it. The signals were applied to the device on the probe station using the XYZ500 TIS micropositioners. Figure 20 shows the results obtained from the verilogA overlapped with experimental data obtained for a compliance current of 100μA.

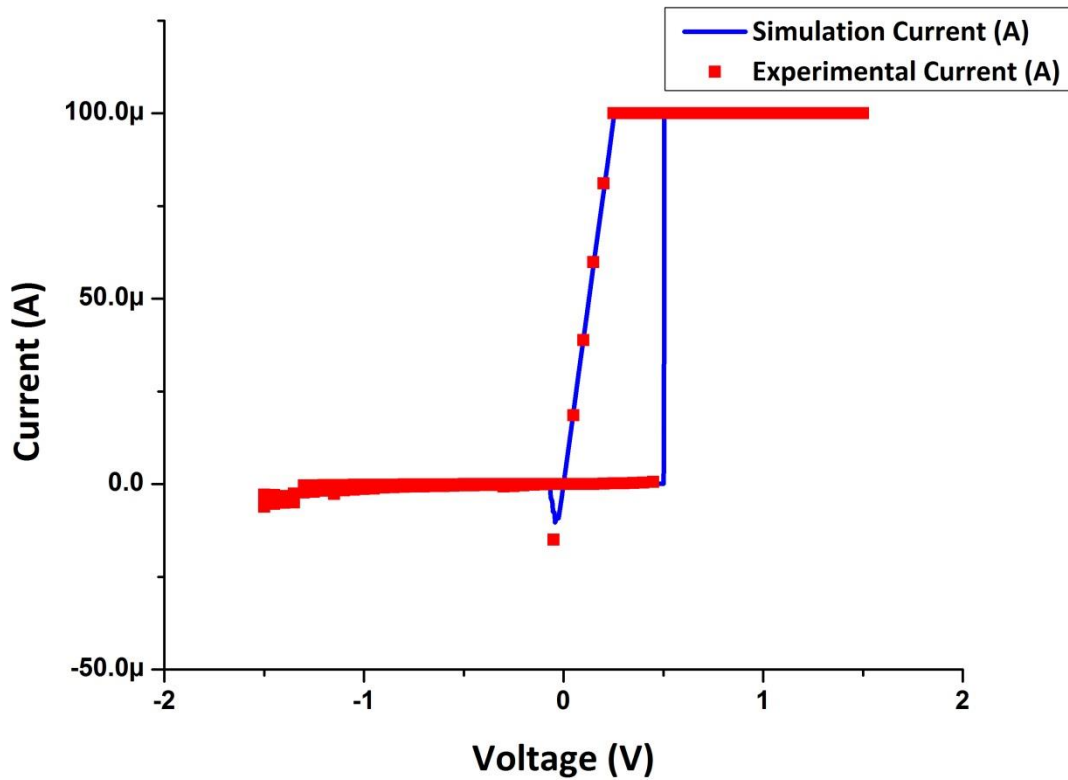


Figure 20 Comparison of I-V characteristics obtained from simulation and experimental data for compliance current of 100uA

The device and models were tested for a wide range of compliance currents. The highest compliance current used was 1mA. Figure 21 and Figure 22 show the I-V characteristics of the verilogA model overlapped with those obtained from experiments. It is observed that both the I-V characteristics resemble each other very closely in determining when the PMC operates in the Low Resistance State (LRS) and when it operates in the High Resistance State (HRS).

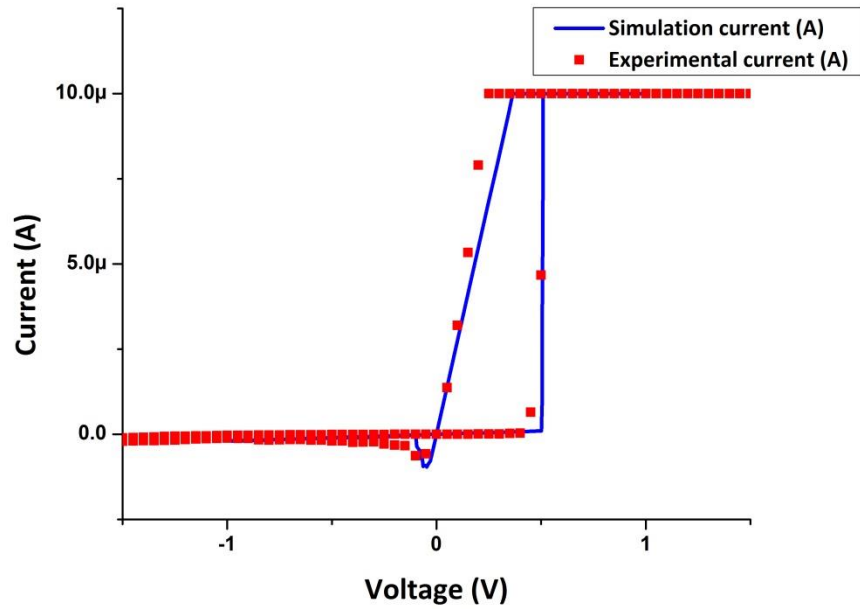


Figure 21 Comparison of I-V characteristics obtained from simulation and experimental data for compliance current of 10uA

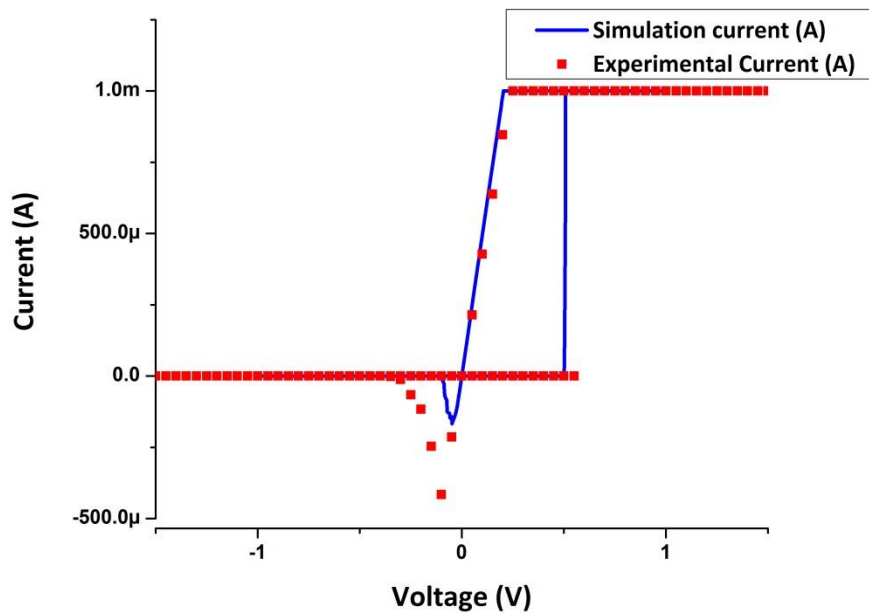


Figure 22 Comparison of I-V characteristics obtained from simulation and experimental data for compliance current of 1mA

#### 4.1.2. Low State Resistance $R_{on}$

An important parameter that needs to be compared is the On-Resistance  $R_{on}$ . This is the resistance of the device when it operates in Low Resistance State (LRS). It can be computed as the slope of the I-V curve in the region when the current starts dropping from the compliance current value towards 0. Figure 23 indicates how the  $R_{on}$  of the device can be computed from the I-V characteristics.

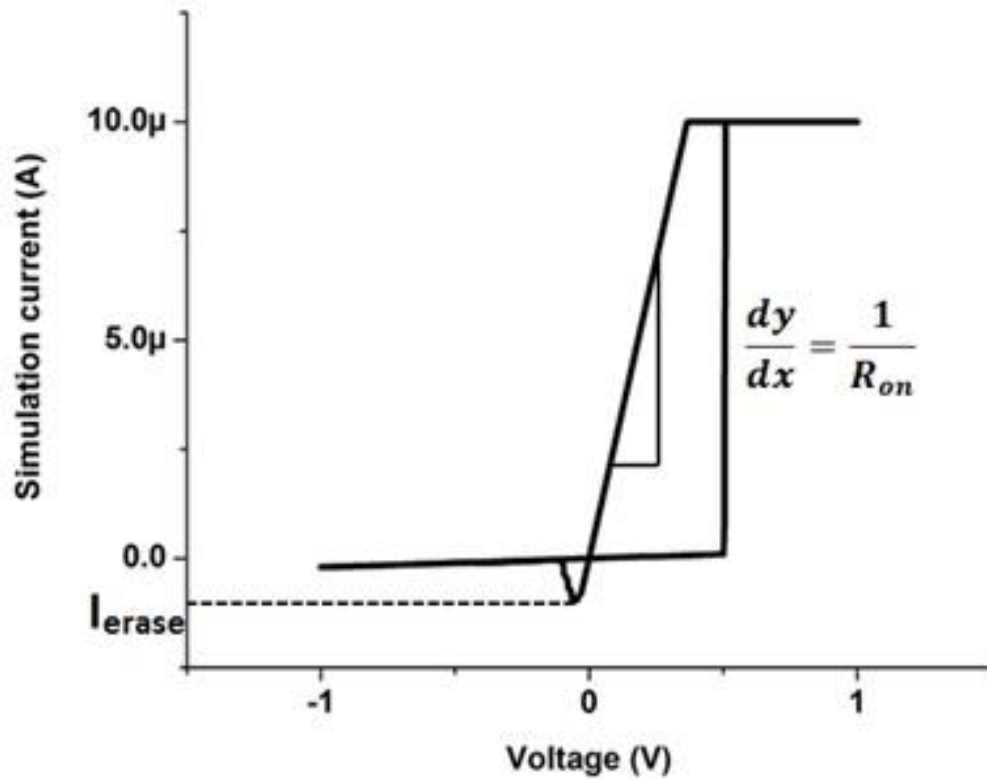


Figure 23 Determination of  $R_{on}$  and erase current from I-V characteristics

Figure 24 shows the scatter plot of  $R_{on}$  obtained from experimental data and from the verilogA model. The experimental data were obtained from a large number of cycles. The points indicate the average while the error bars indicate the standard deviation of the  $R_{on}$  values across cycles.



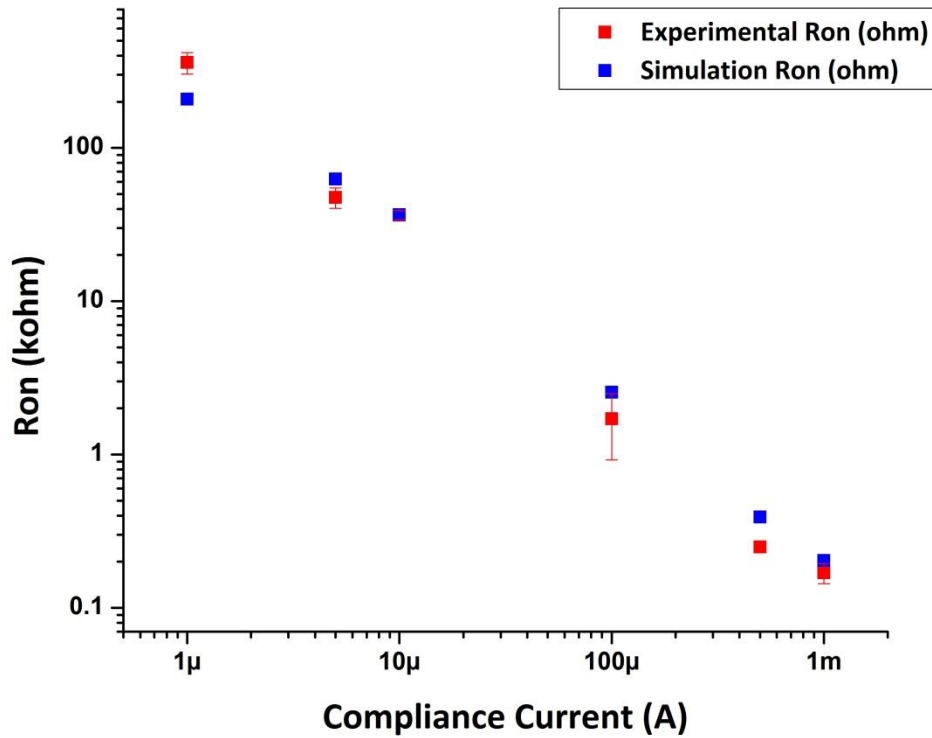


Figure 24 Comparison of Ron obtained from simulation and experimental data

#### 4.1.3. Erase Current

The other parameter illustrated in Figure 23 is the erase current  $I_{\text{erase}}$ . It is defined to be the minimum value of current through the device before it switches back to High Resistance State (HRS). Figure 25 shows a scatter plot of erase current obtained from the verilogA and experimental data.

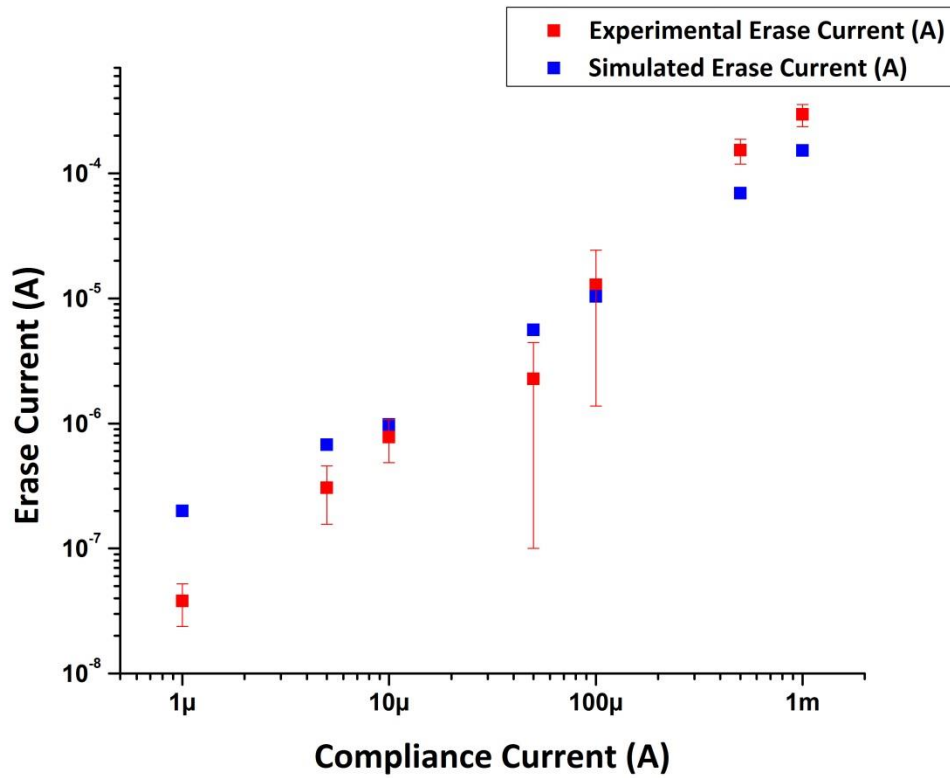


Figure 25 Comparison of erase current from simulation and experimental data

#### 4.1.4. Temperature Behavior

Since the device is intended to be used to create large memories and store large amount of valuable information, the reliability of the device becomes extremely critical. Hence, to determine the reliability of the device, its behavior under various temperatures was studied. The temperature behavior of the device is accounted for in the verilogA model using Equation 10 and Equation 13. Figure 26 shows the  $R_{on}$  of the device at temperatures ranging from 27°C (room temperature) to 120°C.

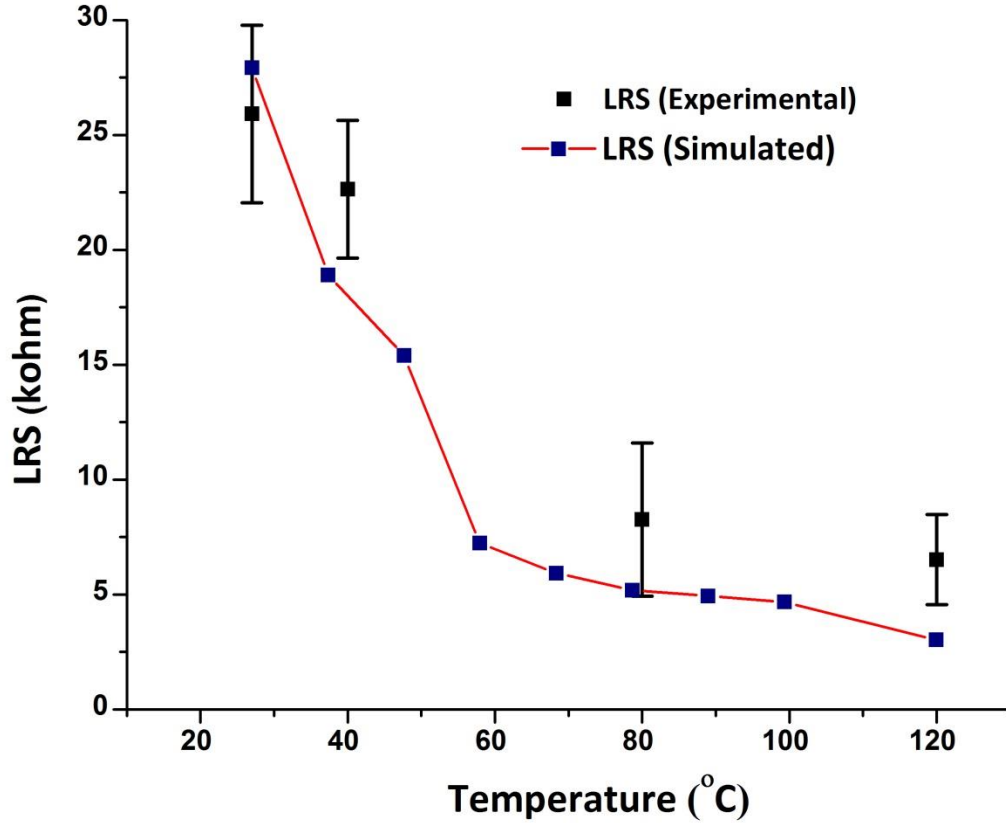


Figure 26 Ron behavior with change in temperature [16]

#### 4.2. Transient Simulations

The transient response results obtained from the verilogA model are presented in this section. A comparison of the results from simulation and experimental data is also presented.

In order to study the transient behavior, voltage pulses of different magnitudes were applied across the device. The following are the three different types of pulses applied:

1. A large positive pulse represents a write pulse
2. A small positive pulse represents a read pulse

3. A negative pulse represents an erase pulse

The resistance level of the device represents the bit stored in the device. In this section the use of the device to store one bit is demonstrated. Later the ability of the device to store multiple bits will be demonstrated.

The bits stored are associated with the resistance of the device as follows –

1. Bit 1 - Low Resistance State
2. Bit 0 – High Resistance State

In the test setup a large positive pulse which represents a write pulse was first applied. This implies that a bit 1 is written onto the device. The write pulse is followed by a read pulse to verify whether the device has stored the previously written bit 1. Then a negative pulse is applied to erase the bit 1 stored in the device. The device is now expected to hold a bit 0. To verify the erase operation a read pulse is applied once again.

Figure 27 shows the simulation results obtained after applying the test pulse.

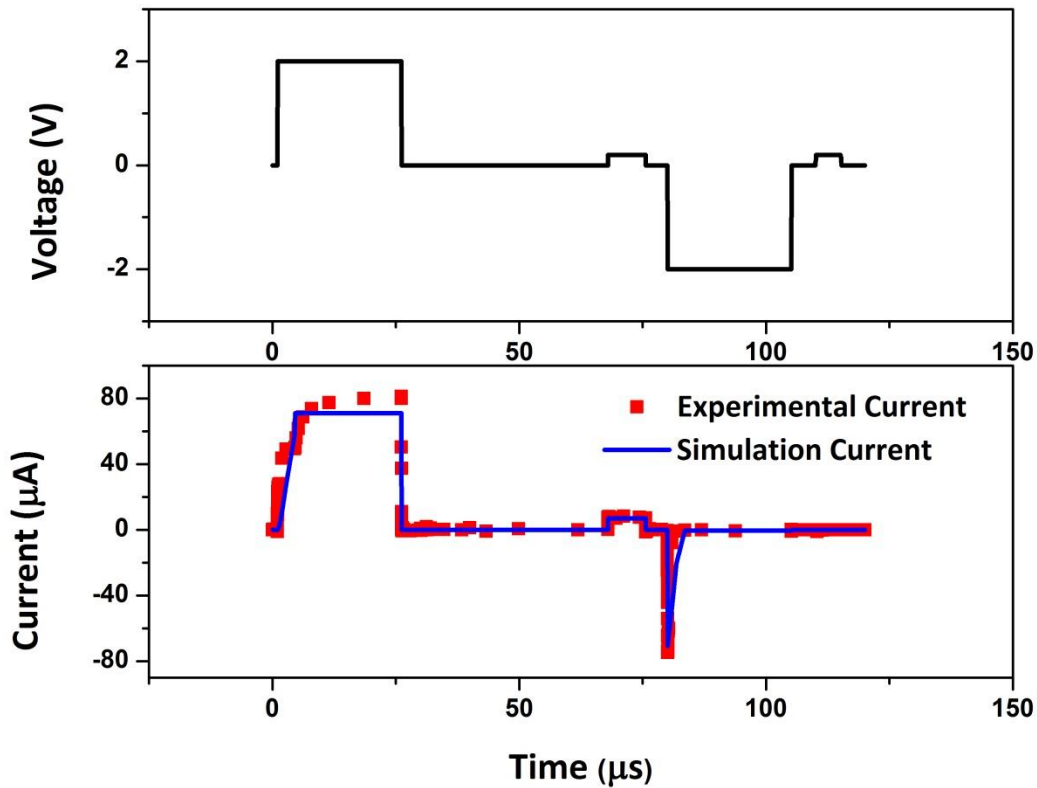


Figure 27 Current through the PMC on application of write-read-erase-read pulse sequence [16]

Figure 27 shows the voltage applied across the device. The current simulated is also shown in Figure 27. A high level of current implies that device is operating in its low resistance state. Initially when a write pulse is applied, the conducting filament is formed in the device and it is operating in the low resistance state. As a result when the read pulse is applied the device allows some current to flow through it. This indicates that a bit 1 is stored in the device. When a negative pulse is applied during the erase operation, the conducting filament is dissolved. This results in the device getting switched to a high resistance state. Hence, the bit 1 is now erased and the device stores a bit 0. The read

pulse subsequently applied results in no current flow through the device implying that the bit stored in the device is a 0.

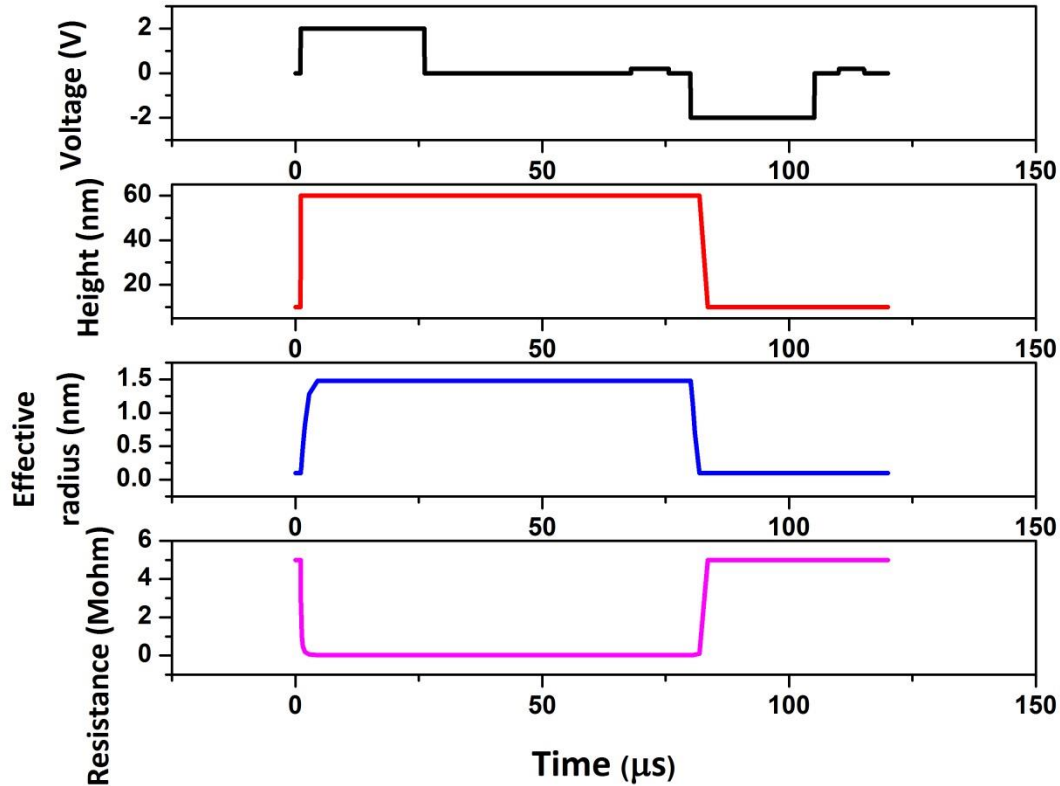


Figure 28 Conducting bridge dimensions and resistance of PMC on application of write-read-erase-read pulse sequence

Figure 28 indicates the formation and dissolution of the conducting bridge during the write and erase operation. Figure 28 also indicates the resistance of the device. It can be seen that upon the application of a write pulse the device is in Low Resistance State (ON State) whereas on the application of the erase pulse the device is in High Resistance State (OFF State).

### **4.3.Multi-Level Programming**

There is an every growing need for electronic components to shrink in size. Often times, memory blocks occupy the largest share of space on chip. Hence, the potential for growth of condensed memory is immense. In this section, the multi-level programming capability of the PMC device will be demonstrated. This will help in using this as a building block for condensed memory [8].

In order to store multiple bits in one PMC device, we need to be able to program the device resistance to multiple values depending on the voltage applied across it. For example, to be able to store 2 bits we need to be able to achieve four distinct resistance levels in the device.

To demonstrate the multi bit storing capacity of the PMC, the device was used along with a current limiting resistor. The write-read-erase-read pulse operation was performed on the device multiple times. Different values were chosen for the magnitude of the write pulse. Figure 29 shows the cumulative distribution of the Low State Resistance (LRS) of the device when voltage pulses of magnitude 1.4V, 1.6V, 1.8V and 2V were applied.

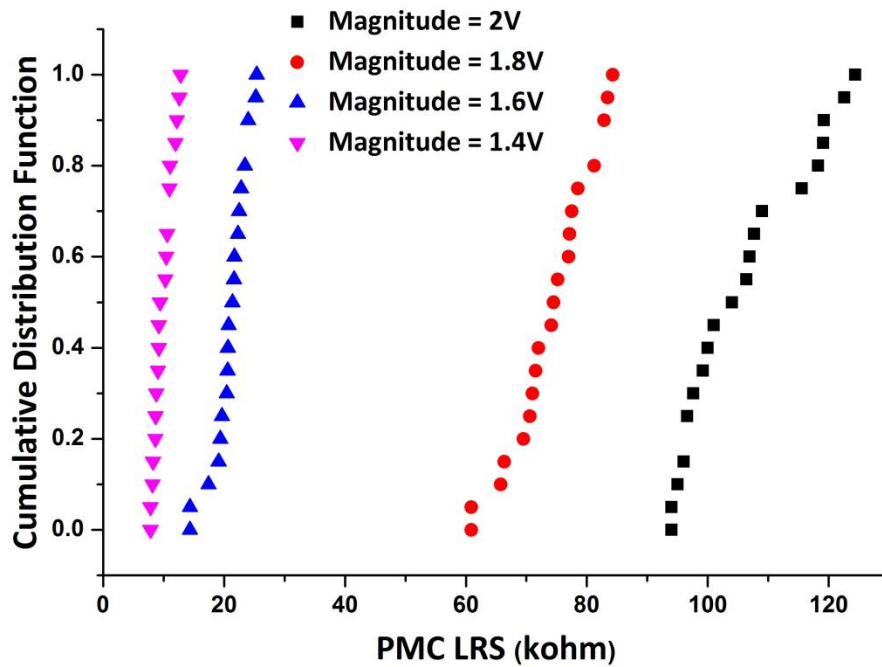


Figure 29 Cumulative distribution function of PMC LRS for different voltage pulse magnitudes [16]

A comparison of the ON State Resistance obtained from the verilogA model and experimental data is shown in Figure 30. The ON State Resistance is compared for various write pulse magnitudes. The figure also shows the behavior of the effective radius of the conducting filament with respect to the write pulse magnitude. As is expected higher magnitude write pulses result in conducting filaments of lower effective radius and as a result the device exhibits lower resistance or higher current can flow through the device.



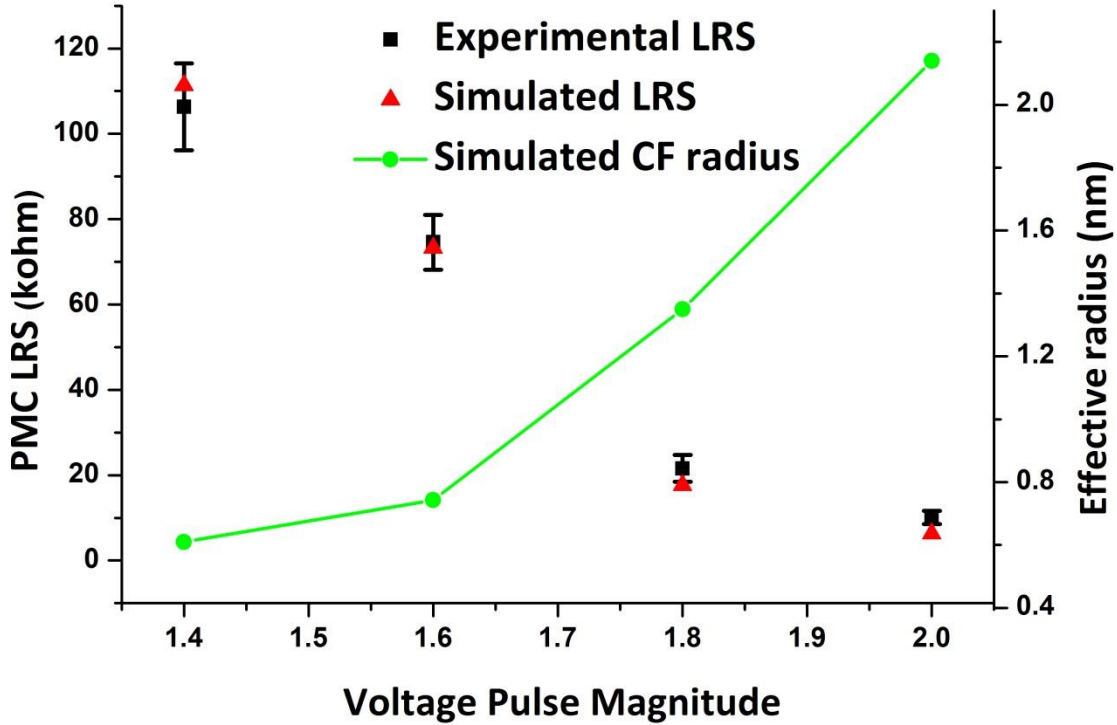


Figure 30 PMC LRS and effective radius for different voltage pulse magnitudes [16]

The number of bits that can be stored in one PMC device is related to the number of resistance levels exhibited by the PMC as follows by the equation

$$N_r = 2^n \quad (17)$$

where  $N_r$  is number of distinct resistance levels exhibited by the PMC and  $n$  is the number of bits that can be stored in the PMC.

#### 4.4. Neuromorphic circuit application of PMC

The multi-level resistance programming ability of the PMC device was also illustrated using multiple pulses of the same magnitude. Here, on the application of

successive positive pulses of short duration a gradual increase in the effective radius is observed. This is followed up with multiple negative pulses of short duration. Figure 31 shows the gradual change in the effective radius of the conducting filament when a series of short voltage pulses are applied.

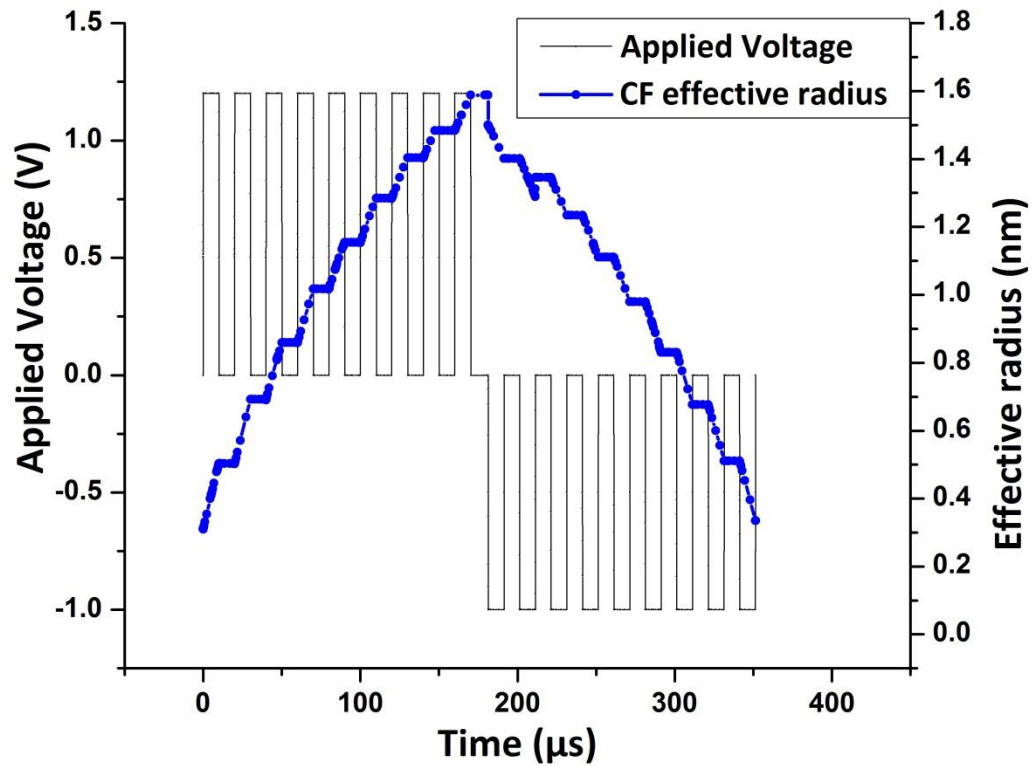


Figure 31 Gradual change in effective radius on application of successive pulses [16]

Each distinct effective radius value leads to the device exhibiting a distinct resistance level. Figure 32 shows the gradual change in resistance.

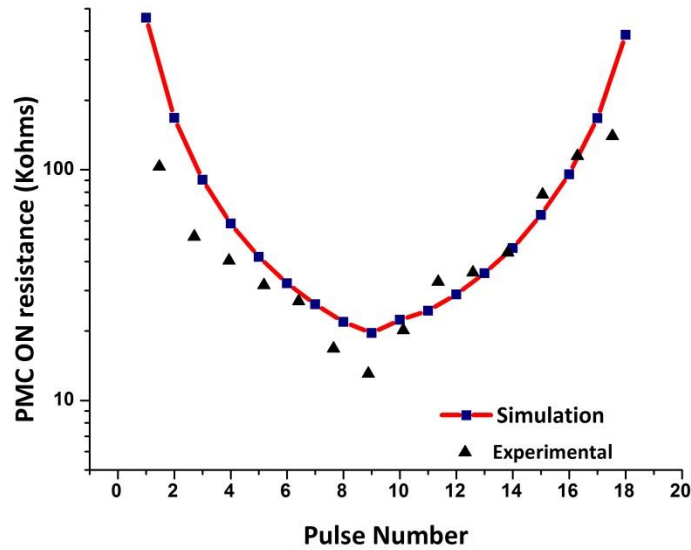


Figure 32 PMC on resistance on application of multiple pulses [16]

Figure 32 also shows a comparison between the simulation resistance levels and the experimentally observed resistance values. It is observed that the experimental data closely resembles the simulation data. This behavior of the PMC to exhibit gradual change in the resistance levels means that the device can be used in Neuromorphic modelling.[10,11,12] The PMC device can be used as a synapse with CMOS neurons. The PMC can be used as connectors between neurons and their gradual change in resistance models the biological behavior of a synapse better than digital circuitry.

## CHAPTER 5

### PMC MEMORY CELL

It has been stated earlier that there is a limit to the amount of current that can flow through the PMC before the PMC breaks. The maximum current that is allowed to flow through the PMC is referred to as the compliance current  $I_{comp}$ . It has also been seen that varying the compliance current helps in achieving multi-level programmability.

In the DC and transient results presented in the earlier chapters, the maximum current flowing through the device is controlled using the voltage supply used. This cannot be done in a large memory array. For this purpose, in this section the 1T 1R model is introduced.

#### **5.1.1T 1R model**

The 1T 1R model has a PMC with NMOS transistor in series connected to it. The transistor is connected to the cathode of the PMC. The gate and source voltage of the transistor and the anode voltage of the PMC can be altered. Figure 33 shows a single 1T 1R memory cell.

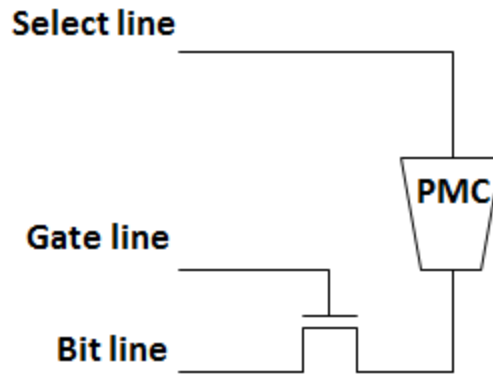


Figure 33 1T 1R memory cell setup using PMT

The transistor performs the role of a current limiter in this setup. The maximum current that can flow through the PMT is set by the transistor. The current limiting behavior of the transistor can be explained by looking at the  $I_D - V_{DS}$  curves of a transistor. As we know initially the current increases with an increase in  $V_{DS}$ , but once the transistor enters saturation the current attains a constant level.

The 1T 1R model can be used as a memory cell by setting the bit line to 0V, the gate voltage greater than the threshold voltage of the NMOS transistor and varying the anode voltage.

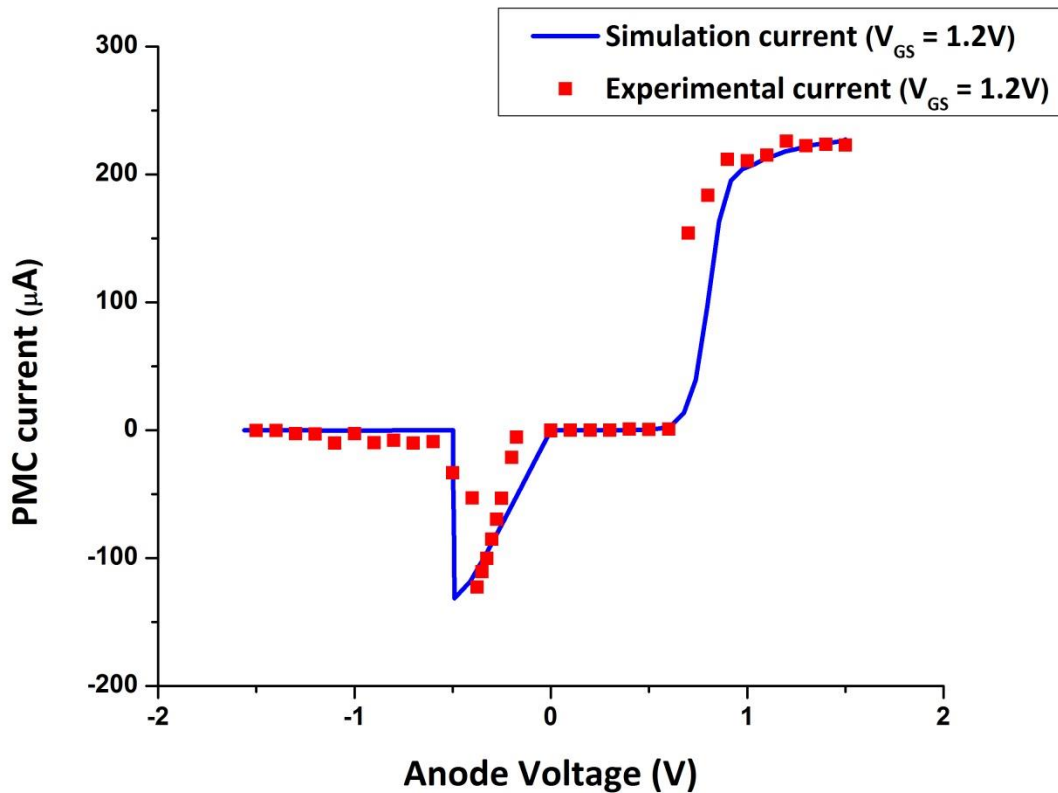


Figure 34 PMC current vs anode voltage [16]

In Figure 34 the current through the PMC has been plotted versus the anode voltage. Here the gate voltage has been set to 1.2V. The anode voltage is then varied. It can be seen that for positive anode voltages, once the voltage drop across the PMC ( $V_{an} - V_{ca}$ ) crosses the positive threshold voltage of the PMC the current increases until it reaches compliance current. This indicates that the PMC shifts from HRS to LRS. For negative anode voltages, the transistor terminal connected to the PMC is at a lower potential than the bit line voltage. Hence, it starts acting as the source and the terminal connected to the bit line is acting as the drain. This results in current flowing in the opposite direction or negative values of PMC current. Once the anode voltage is negative

enough such that  $V_{an} - V_{ca}$  is lesser than the reverse threshold voltage of the PMC, the current snaps back to zero since the PMC transitions from LRS to HRS.

## 5.2. Multiprogramming of 1T 1R cell

One of the main advantages of using the PMC as a memory building block is its ability to store multiple bits. In the 1T 1R model this can be done by varying the gate voltage applied. A change in the gate voltage causes the  $V_{GS}$  of the transistor to change. This results in a different saturation current of the transistor.

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{GS} - V_T)^2 \quad (18)$$

The saturation current of the transistor is nothing but the compliance current of the PMC in the 1T 1R cell. As we have seen, different compliance currents correspond to different LRS resistances of the PMC. This can be used to store multiple bits in the PMC as demonstrated in Figure 5. Figure 35 indicates the variation in compliance current with change in gate voltage while Figure 36 shows variation in  $R_{on}$  with change in gate voltage.

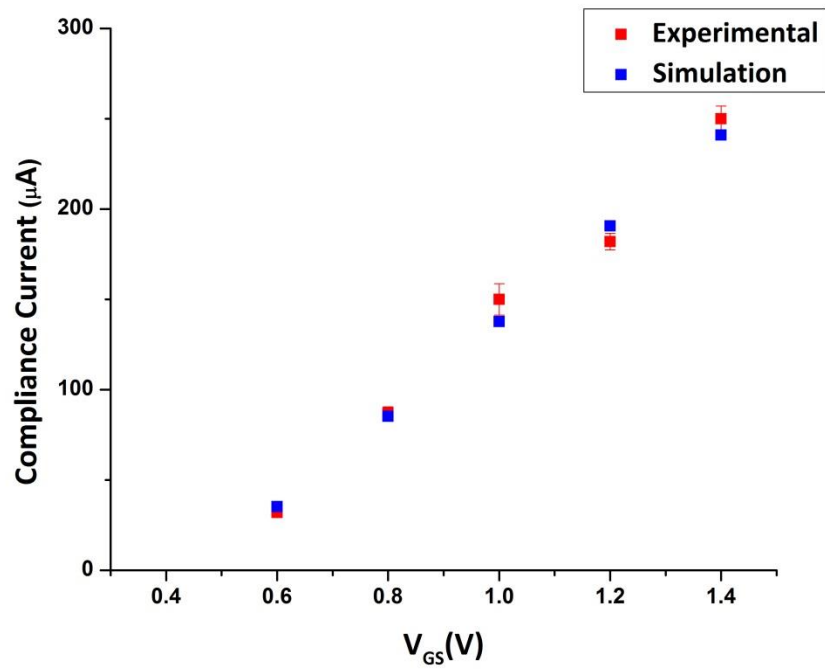


Figure 35 Change in compliance current of PMC with change in gate voltage

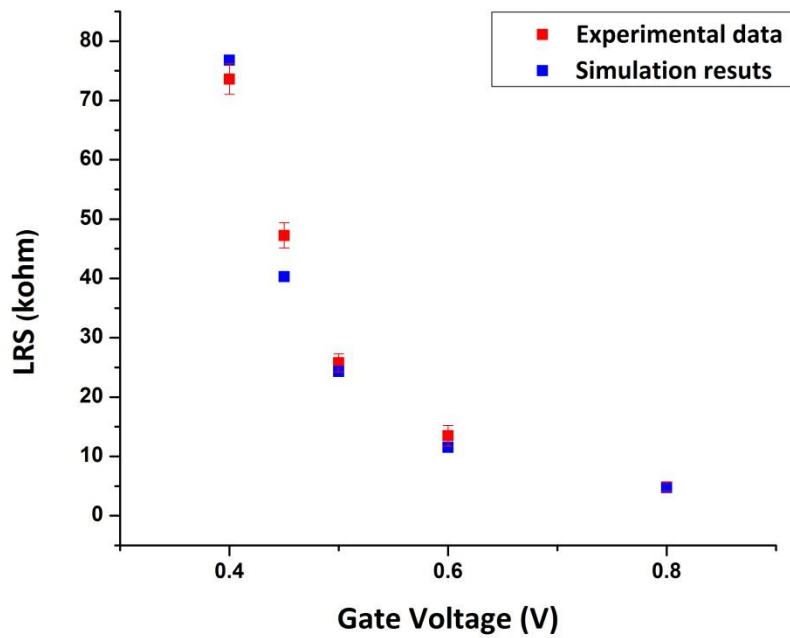


Figure 36 Change in LRS resistance of PMC with change in gate voltage



Both Figure 35 and Figure 36 show simulation results from the verilogA model and the experimental data obtained from testing the 1T 1R memory cell provided by Adesto Technologies. It can be seen that both the simulation results and experimental data follow each other closely.

## CHAPTER 6

### CONCLUSION

A verilogA model for a type of resistive memory, Programmable Metallization Cells (PMC), has been presented in this thesis. The working of the PMC has been modelled by replicating the formation and dissolution of the conducting bridge. The I-V characteristics of the PMC was simulated using the verilogA model. The simulation results were verified against experimental data for a wide range of compliance currents.

The transient response of the PMC was simulated using the verilogA model. This was done using the write-read-erase-read pulse sequence. The ability of PMC to switch from HRS to LRS upon the application of a write pulse and remain in LRS until an erase pulse is applied has been demonstrated. Multi-programming of the PMC has been shown by applying write pulses of different magnitudes.

The possibility of the PMC being used to replicate a synapse in neuromorphic circuits has been discussed. The other major application area for the PMC discussed in this thesis is large scale memories. A 1T-1R memory cell which can act as the building block for large scale memories has been simulated using the verilogA model. The I-V characteristics of the 1T-1R has been matched with experimental data. Multi-programming property of 1T-1R cell which can be used to create high density memory has been demonstrated.

Though the simulation results are a very good match to experimental data, the model can be further improved by modelling the conducting bridge as a frustum instead of a cylinder. Also, including the Butler-Volmer current can further improve the model. But the present model can be used to simulate the behavior of the PMC in a circuit

environment very accurately. The model offers circuit designers an opportunity to design circuits using the PMC, which can greatly aid in the development of programmable metallization cells.

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APPENDIX A  
VERILOGA CODE

```

//VERILOGA for PMC, DC_version2, veriloga

`include "constants.vams"
`include "disciplines.vams"

module DC_version2(an,ca,t);
inout an,ca,t;
electrical an, ca,t;

//structure parameters
parameter real rho_f = 2.3e-6;
parameter real rho_e = 8e3;
parameter real rcell = 2.5e-6;
parameter real Kb = 1.38e-23;
parameter real Kb1 = 8.617e-5;
parameter real T0 = 300.15;

//filament growth parameters

parameter real q = 1.602e-19;
parameter real h0 = 10e-9;
parameter real rmin = 0.1e-9;
parameter real vh = 5;//0.07
parameter real vr = 5;//0.05
parameter real beta = 0.086;
parameter real beta1 = 0.164;
parameter real Ea = 0.4;
parameter real L = 60e-9;
parameter real Icomp = 500e-6;
parameter real Roff = 5e6;
parameter real mAg2Se = 294.7;
parameter real Na = 6.022e23;
parameter real rho_Ag2Se = 8.216;
parameter real alpha1 = 0.4;
real
h,Vol,r,store,r_limit,Wa,Jhop,Jhop_on,E,dhdt,drdt,Rsf,Rse,Re,Rf,R,m,
n,sgn,state,dh,th,dr,r_dummy,Rd,alpha,T;

analog begin@(initial_step)
begin
m = h0;
n = rmin;
r = rmin;
h= h0;
store =0;
r_limit =0;
dhdt = 0;
drdt=0;
state = 0;
alpha = 0.4;
T = T0;

```

```

end

@(cross(V(an,ca) - 0.5, +1))
begin
state = 1;
m = h0;
end

@(cross(V(an,ca) - 0.52, -1))
begin
state = 0;
end

@(cross(-0.01-V(an,ca), +1))
begin
state = 2;
end

@(cross(-0.05-V(an,ca), -1))
begin
n = rmin;
state = 0;
end

@(cross(h - 49.9e-9, +1))
begin
th = V(t);
end

if (state == 1)
begin
if (V(an,ca)/R < Icomp) begin
dhdt = vh*exp(-
Ea/(Kb1*T))*sinh((alpha*q*(V(an,ca)))/(Kb*T));
if (h == L) begin
drdt = vr*exp(-
Ea/(Kb1*T))*sinh((beta*q*(V(an,ca)))/(Kb*T));
dr = drdt;
store = 1;
end
else begin
store = 0;
dh = dhdt;
end
end
if (I(an,ca) >= Icomp) begin
dr = 0;
dh = 0;
end
end
end

```



```

if (state == 2)
    begin
        drdt = vr*exp(-
Ea/(Kb1*T))*sinh((beta1*q*(V(an,ca)))/(Kb*T));
        if (r > rmin) begin
            dr = drdt;
        end
        else begin
            dr = 0;
            dhdt = vh*exp(-Ea/(Kb1*T))*sinh((alpha1*q*(V(an,ca)))/(Kb*T));
            if (h>h0) begin
                dh = dhdt;
            end
            else begin
                store = 0;
            end
        end
    end
end

if (state == 0)
    begin
        dh = 0;
        dr = 0;
    end

n = idt(dr,rmin);
m = idt(dh,h0);

Rse = ((rho_e*L)/(3.14*((rcell*rcell)- (r*r)))));
Rsf = ((rho_f*h + rho_e*(L-h))/(3.14*r*r));

Rd = 1/((1/Rsf)+(1/Rse));

if (store == 1) begin
    R = Rd;
end
else begin
    R = Roff;
end

if (V(an,ca) >= 0) begin
    sgn = 1;
end
else begin
    sgn = -1;
end

if (m >= L) begin
    h=L;
end
if (L > m > h0) begin
    h=m;
end
end

```

```
if (m <= h0)begin
h = h0;
end

if (rmin < n) begin
r = n;
end

if (n <= rmin)begin
r = rmin;
end

if (V(an,ca)/R >= Icomp)
begin
I(an,ca) <+ Icomp;
end

else
begin
I(an,ca) <+ V(an,ca)/R;
end

end
endmodule
```