Analog Fault Modeling, Simulation and Diagnosis

by

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A Thesis Presented in Partial Fulfillment of the Requirements for the Degree Master of Science

Approved April 2014 by the Graduate Supervisory Committee:

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April 2014

ABSTRACT

Chip test has become increasingly important than before when the process technology changes from um to nm. Although the scaling down size of fabrication brings low power and high speed, the fault becomes complex and easy to happen. Each chip company has no choice to recruit more testing engineers to solve thousands of tricky faults after fabrication.For digital integrated circuit testing, Automatic Test Pattern Generation (ATPG), Leakage Current method and Scan method are widely used as highly efficient testing tools. But for analog integrated circuit testing, there is no automotive testing tool to improve test cost. Therefore, my thesis focuses on establishing the relationship between specific analog defect and obscure defect performance, thus developing an automotive testing tool in real practice.

The research objective is fully differential op-amp with common mode feedback, which are applied in filter, band gap, Analog Digital Converter (ADC) and so on as a fundamental component in analog circuit. Having modeled various defect and analyzed corresponding probability, defect library could be built after reduced defect simulation.Based on the resolution of microscope scan tool, all these defects are categorized into four groups of defects by both function and location, bias circuit defect, first stage amplifier defect, output stage defect and common mode feedback defect, separately. Each fault result is attributed to one of these four region defects.Therefore, analog testing algorithmand automotive tool could be generated to assist testing engineers to meet the demand of large numbers of chips.

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DEDICATION

To my parents for their love and support

ACKNOWLEDGMENTS

I would like to show my sincere gratitude to my master's degree advisor, Dr. SuleOzev, especially for her continuous guidance and patience during the past year and a half. It is my great honor to have the opportunity to work for her and officially start my research life. I am also grateful to Dr. UmitOgras and Dr. SayfeKiaei for their time and effort in reviewing my work.

I would like to thank my mentor AliasgarPresswala and my director Michael Laisne at Qualcomm for all their help. I could not have accomplished this research without their ideas and assistance from the industrial area. I am also grateful to the other members of the Testing Group supervised by Dr. SuleOzev for their encouragement and their patience in answering my questions. Finally I would like to thank my friends and my family for their continuous support and all those who have helped me on my way toward this moment.

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CHAPTER 1

INTRODUCTION

System-on-chip (SOC) has shown the increasing importance in analogcircuit. It is common that Integrated circuits (ICs) composed of digital and analogcircuits are on the same substrate [1].Advancednano technologies in IC fabrication have triggered the massive IC complexity. Therefore, the more complexfunctionand smaller size of IC chips bringsa challengingtesting.Meanwhile, high quality and low price are two main goals of testing.

IC tests are classified intothree types such as digital, analogand mixed-signal. Currentdigital circuits testing are well developed and has been put into use for years. As industrial company like Qualcomm shown, testing methods contain Automatic Test Pattern Generation (ATPG), Leakage Current method, Scan method, IEEE Standard 1149.1 [2]and so on. Butanalogcircuits testing remainsin academic research because of the various analog situations.For the relationship between digital circuit and analog circuit, "when digital clock rates get reallyhigh, the 0's and 1's don't have real meaning anymore. The behavior is essentially analog" [3].

With wide applications, Analog and Mixed Signal Integrated Circuits become the fundamental component in solid state industry nowadays. In comparison todigital testing, analog testing seems far behind in both tools and methodologies. It needs a continuous effort in both academic and industrial area. Theaim of this thesis is to studyanalog fault modeling, defect simulation and testing diagnosis on basic analog device, fully differential operational amplifier with common mode feedback (CMFB) and multiple feedback (MFB) third order band pass filter.

1.1 History

Analog and mixed-signal testing always acts as key role in analog circuit design, chip manufacture, and reliability of integrated circuits. Back to discrete electronic components in early years, testing and fault diagnosis are not challenging. It just depends on testing engineers'own experience and this custom has not changed since then. At that time, the testing research seemed to be unessential. But with the boost of integration circuits in the 1970s, research on analog and mixed-signal testingturns to be increasingly important.Asone of IC branches, testinghave been developed into fault modeling, defect simulation, diagnosis methodology and so on.

1.2 Problems

Within my intern in Product Test Group of Qualcomm, San Diego, I collected some problems of Analog Testing from the industry in summer 2013.

Firstly, Electrostatic discharge(ESD) could not simulated in Cadence, which brings the potential threat to analog fault. It can be only characterized with simulation.

Secondly, the impact of parasitic parameters becomes another key to analog fault. For example, there are more than a thousand transistors in power management integrated circuit (PMIC) with millions of parasitic parameters. It is seldom to simulate all the parasitic parameters in Cadence.

Thirdly, the corner simulation of Process-Voltage-Temperature (PVT)sometimes is not the worst case. Analog fault would happen even if the corner was simulated. Fourthly, equivalent defects contain positive defect and negative defect, which results in normal performance. Therefore, it is hard to distinguish whether there are equivalent or not.

Fifthly, there is a distortion in the transform from the time domain to the frequency domain. For example, both saturation distortion and cutoff distortion show the similar frequency response.

In overall, all these practical problems above show that analog fault testing is a challenging task, attracting more and more researchers to study and develop effective and efficient testing tools and methodologies.

CHAPTER 2

OPAMP AND FILTER DESIGN

2.1 Fully Differential Operational Amplifier with Common Mode Feedback

To reduce the effects of charge injection and clock feed through in the circuits, fully differential op-amp are widely used in Analog Circuit Design. But the fully differential op-amp needs a common-mode feedback(CMFB). The CMFB circuit keeps the op-amp's outputs around a known voltage.Usually,the common mode voltage is half of supply voltage.

2.1.1 Design Schematic

Because this fully differential op-amp with common mode feedback is used in multiple feedback third order band-pass filter, the design specification are shown below. VDD: 1.8V, DC gain: at least 55 dB, Cutoff frequency: 1MHz, Phase Margin: at least 40 degree. What's more, a standard 0.35 um process technology is applied in this research.

Due to the long channel process, Beta-multiplier reference[4] is as the bias circuit, shown in Figure2.1. For bias circuit, when the gates of M3/M4are too high around VDD and the gates of M1/M2are too low near ground, MSU3 is on because its gate is connected to the diode MSU2. Afterwards, the leakage current flows from M3/M4 to M1/M2, during which the gate voltage of M3/M4 decreases and the gate voltage of M1/M2 increases. When the difference between these is not big enough, MSU3 turns off and the bias circuit has started up.



Figure 2.1 The Schematic of Bias Circuit (Vbiasp=2V, Vbiasn=0.9V, Vcm=1.5V)

The prototype of fully differential operational amplifier with common mode feedback [4] is shown in Figure 2.2. The first stage is a cascode amplifier. The second stage is fully swing output buffer. Common mode feedback loop keeps these two opamp's outputs balanced at half of supply voltage. What's more, between these two stages there are two compensation capacitances to adjust the bandwidth of frequency response and avoid oscillating.



Figure 2.2The Schematic of Fully differential op-amp with CMFB

2.1.2 DC Analysis

There are two tables below to show DC Analysis. Table 2.1is to show sizes of all the transistors used for the differential op-amp as well as bias circuit. Table 2.2 is to show DC parameters of each transistor such as drain current, threshold voltage and so on.

Name	Length (m)	Multiplier	Width (m)	M*W(m)
N1	4.00E-07	2	8.00E-06	1.60E-05
N2	4.00E-07	1	8.00E-06	8.00E-06
N3	4.00E-07	1	1.00E-05	1.00E-05
N4	4.00E-07	1	1.00E-05	1.00E-05
N5	4.00E-07	2	1.00E-06	2.00E-06
N6	4.00E-07	2	1.00E-06	2.00E-06
N7	4.00E-07	1	4.00E-06	4.00E-06
N8	4.00E-07	1	4.00E-06	4.00E-06
N9	4.00E-07	1	4.00E-06	4.00E-06

N10	4.00E-07	1	4.00E-06	4.00E-06
N11	4.00E-07	2	1.00E-06	2.00E-06
N12	4.00E-07	2	1.00E-06	2.00E-06
N13	4.00E-07	1	1.00E-05	1.00E-05
N16	4.00E-07	1	8.00E-06	8.00E-06
N17	4.00E-07	2	8.00E-06	1.60E-05
N19	4.00E-07	4	2.00E-06	8.00E-06
N20	4.00E-07	1	4.00E-06	4.00E-06
N21	4.00E-07	1	4.00E-06	4.00E-06
N22	4.00E-07	1	2.00E-06	2.00E-06
N23	4.00E-07	1	4.00E-06	4.00E-06
N24	4.00E-07	1	2.00E-06	2.00E-06
N26	4.00E-07	1	6.00E-06	6.00E-06
N27	4.00E-07	1	6.00E-06	6.00E-06
N28	4.00E-07	2	6.00E-06	1.20E-05
N29	4.00E-07	2	6.00E-06	1.20E-05
PO	4.00E-07	2	8.00E-06	1.60E-05
P2	4.00E-07	1	8.00E-06	8.00E-06
P3	4.00E-07	1	1.00E-05	1.00E-05
P4	4.00E-07	1	8.00E-06	8.00E-06
P5	4.00E-07	1	1.00E-05	1.00E-05
P6	1.20E-06	1	5.00E-06	5.00E-06
P7	4.00E-07	1	1.00E-05	1.00E-05
P8	4.00E-07	1	8.00E-06	8.00E-06
P9	4.00E-07	1	8.00E-06	8.00E-06
P10	4.00E-07	1	8.00E-06	8.00E-06
P12	4.00E-07	2	8.00E-06	1.60E-05
P13	4.00E-07	1	1.20E-05	1.20E-05
P14	4.00E-07	1	1.20E-05	1.20E-05
P15	4.00E-07	1	1.20E-05	1.20E-05
P17	4.00E-07	1	5.00E-06	5.00E-06
P18	4.00E-07	1	5.00E-06	5.00E-06
P19	8.00E-06	1	8.00E-07	8.00E-07

Table 2.1Transistors Sizes

Name	Id (A)	Vgs (V)	Vth (V)	Vds (V)	Vdsat (V)
N1	1.61E-04	0.9062	0.7166	1.2	0.1922
N2	8.47E-05	0.9175	0.7152	0.9175	0.2009
N3	6.03E-05	0.998	0.865	0.998	0.1618

N4	6.03E-05	0.998	0.865	0.998	0.1618
N5	6.03E-05	1.101	0.6694	0.5284	0.358
N6	6.03E-05	1.101	0.6694	0.5284	0.358
N7	6.03E-05	0.9028	0.6274	0.3988	0.2423
N8	6.03E-05	0.9028	0.6274	0.3988	0.2423
N9	6.03E-05	0.9028	0.6274	0.3988	0.2423
N10	6.06E-05	0.9028	0.6273	0.4166	0.2424
N11	6.06E-05	1.083	0.6706	1.098	0.3462
N12	6.03E-05	1.101	0.6694	0.5284	0.358
N13	6.03E-05	0.998	0.865	0.998	0.1618
N16	8.47E-05	0.9175	0.7152	0.9175	0.2009
N17	1.61E-04	0.9062	0.7166	1.2	0.1922
N20	3.36E-05	0.8032	0.6248	0.8933	0.1766
N21	3.29E-05	0.8032	0.6253	0.8032	0.1763
N26	8.47E-05	0.9028	0.6339	0.2931	0.2384
N27	8.47E-05	0.9028	0.6339	0.2931	0.2384
N28	1.61E-04	0.8933	0.6338	0.3043	0.232
N29	1.61E-04	0.8933	0.6338	0.3043	0.232
P0	-1.61E-04	-1.075	-0.7306	-1.495	-0.318
P2	-6.03E-05	-1.075	-0.749	-0.3969	-0.3038
P3	-6.03E-05	-1.089	-0.8188	-0.678	-0.2688
P4	-6.03E-05	-1.075	-0.749	-0.3969	-0.3038
P5	-6.03E-05	-1.089	-0.8188	-0.678	-0.2688
P6	-6.06E-05	-1.486	-0.7205	-1.486	-0.6567
P7	-6.03E-05	-1.089	-0.8188	-0.678	-0.2688
P8	-6.03E-05	-1.075	-0.749	-0.3969	-0.3038
P9	-8.47E-05	-1.075	-0.7256	-1.789	-0.3218
P10	-8.47E-05	-1.075	-0.7256	-1.789	-0.3218
P12	-1.61E-04	-1.075	-0.7306	-1.495	-0.318
P13	-6.65E-05	-1.004	-0.7411	-0.5249	-0.2555
P14	-3.29E-05	-0.9705	-0.8213	-1.672	-0.1757
P15	-3.36E-05	-0.9751	-0.8228	-1.582	-0.1781

Table 2.2DC Parameters

2.1.3 Frequency Response

In analog circuits, DC analysis emphasizes on low frequency characteristics. High frequency characteristics is related to the effect of device and load capacitances. The

speed of analog circuit is the tradeoff of other parameters such as power, gain and bandwidth. Therefore, it is essential to understand the frequency response [5] of analog circuit.

It is to plot gain and phase margins for Vcm=1.5V and VDD=3V.From Figure 2.3, we can getPhase Margin=68.4degree, Gain Margin=12.44dB and DC Gain=62.77dB.



Figure 2.3Phase and gain margins

Power Supply Rejection(PSRR)shows how the noise on the supply exerts an impact on the output of an op-amp. It is defined as the gain from the input to the output divided by the gain from the supply to the output. Common mode rejection ratio(CMRR)is defined as the rejection by the device of unwanted input signals common to both inputs, relative to the wanted difference signal.

It is to plot PSRR, CMRR vs. Frequency for Vcm=1.5V and VDD=3V.From Figure 2.4, we can get PSRR=313dB at low frequency. From Figure 2.5, we can get CMRR=302dB at low frequency.



Figure 2.4 PSRR

Expressions



Figure 2.5 CMRR

2.2 Multiple Feedback Third Order Band Pass Filter

As a popular configuration, the multiple feedback(MFB) filter, uses op-amps asintegrators. Therefore, the dependence of the transfer function on the op-amp parameters is greater than in the Sallen-Key [6] realization. For the design of MFB third order filter, 'Filter Pro' developed by Texas Instrument is used.

2.2.1 Design and Derivation

The MFB third order filter is composed of low pass filter and high pass filter in series, separativelyin Figure 2.6 and Figure 2.7. Design specifications are shown below: Starting frequency= 1KHz, Stopping frequency= 1MHz, Q factor=1. Name: Lowpass, Multiple Feedback Fully Differential, Butterworth Part: Ideal Opamp Order: 3 Number Of Stages: 2

Gain: 1 V/V (0 dB) Allowable PassBand Ripple: 1 dB Passband Frequency: 1 MHz Corner Frequency Attenuation: -3 dB



Figure 2.6 MFB Low Pass Filter Schematic

First part pole, $f0 = \frac{1}{2\pi R^2 C1}$. Second part pole, for R3=R1/2 and R2=R1, then $f1 = f2 = \frac{1}{2\pi\sqrt{C1C2R1}}$ which are conjugate poles.

Define the node Vx between R1 and the first op-amp, C1, R2 in parallel; the node Vo1 between the first op-amp, C1, R2 in parallel and R1; the node Vy between R1 and R3.

First part pole:

For small signal analysis Vx=0,

$$\frac{Vin1 - Vx}{R1} + (Vo1 - Vx)(\frac{1}{R2} + SC1) = 0$$

$$Vx = 0$$

$$\Rightarrow \frac{Vin1}{R1} + Vo1(\frac{1}{R2} + SC1) = 0$$

$$\Rightarrow \frac{Vo1}{Vin1} = \frac{-\frac{1}{R1}}{\frac{1}{R2} + SC1}$$

$$\Rightarrow \frac{Vo1}{Vin1} = \frac{-\frac{R2}{R1}}{1 + \frac{S}{\frac{1}{R2}C1}}$$

$$w0 = \frac{1}{R2C1} = 2\pi f 0$$

$$f 0 = \frac{1}{2\pi R2C1}$$

Second part poles:

Simply the circuit from two inputs and two outputs to single input and single output, in which the equivalent capacitance between two inputs is 2C2 while R1/2 is in place of R3 and R1 is in place of R2.

$$\frac{Vo1 - Vy}{R1} + \frac{Vo2 - Vy}{R1} = \frac{Vy}{\frac{1}{2}SC2} + \frac{Vy}{R2}$$
$$\frac{Vy}{R2} = \frac{-Vo2}{\frac{1}{5}SC1} \Rightarrow Vy = -Vo2SC1R2$$

Then combine those equations,

$$\frac{Vout2}{Vo1} = \frac{-1}{S^2 C 1C2R 1^2 + 2SC1R 1 + 1}$$

$$\Rightarrow w1 = \frac{1}{C2R 1} \pm \frac{\sqrt{C1C2 - C1^2}}{C1C2R 1} j$$

$$|w1| = \frac{\sqrt{C1C2}}{C1C2R 1} = 2\pi f \Rightarrow f = \frac{1}{2\pi R 1 \sqrt{C1C2}}$$

$$Q^2 = \frac{C1C2R 1^2}{(2C1R 1)^2} = 1 \Rightarrow C2 = 4C1$$



Figure 2.7 MFB High Pass Filter Schematic

First part pole,
$$f0 = \frac{1}{2\pi R 1C1}$$
. Second part pole, for C2=C1, then $f1 = f2 =$

20nF

 $\frac{1}{2\pi\sqrt{R1R2C3C1/2}}$ which are conjugate poles.

Put the node Vo1 between the first op-amp and C1,

First part pole:

$$\frac{V_{01}}{R2} + \frac{V_{1n1}}{\frac{1}{SC1} + R1} = 0$$

$$\Rightarrow \frac{V_{01}}{V_{1n1}} = \frac{-SC1R2}{1 + SC1R1}$$

$$\Rightarrow \frac{V_{01}}{V_{1n1}} = -\frac{SC1R2}{1 + \frac{S}{\frac{1}{C1R1}}}$$

$$\Rightarrow f 0 = \frac{1}{2\pi C1R1}$$

Second part poles:

Simply the circuit from two inputs and two outputs to single input and single output, in which the equivalent capacitance between two inputs is 0.5R2.Use KVL and KCL as shown in low pass filter.

$$\frac{Vout2}{Vo1} = \frac{-S^2 \frac{C1}{C2}}{S^2 + \frac{C1 + C2 + C3}{R1C3C2}S + \frac{2}{R1R2C2C3}}$$
$$fc = \frac{1}{2\pi\sqrt{R2R1C3C1/2}}$$
$$Q^2 = \frac{(R1C1/2)^2}{R1R2C1^2} = 1 \Longrightarrow R2 = \frac{R1/4}{4}$$

2.2.2 Frequency Response of MFB filter

Figure 2.8 shows Low pass filter's frequency response. Figure 2.9 shows High pass filter's frequency response. Figure 2.10 shows MFB band pass filter composed of high pass filter and low pass filter in series. Figure 2.11 shows Band pass filter's frequency response in dB20 and magnitude.



Figure 2.8 Low pass filter's frequency response



Figure 2.9 High pass filter's frequency response



Figure 2.10The block graph of band pass filter



Figure 2.11The output frequency response in dB20 and Magnitude

CHAPTER 3

DEFECT MODELING

A fault model is a hypothesis of how a circuit may cause incorrect behavior due to a manufacturing defect. It is a means of specifying the characteristics of a physical defect, so that the representation of the digital defect is easily understood by tools. The following are the common fault models [7] [8] [9] [10]used in the industry today.

3.1 Bridge Fault

Bridge fault, also named as short fault, is caused primarily by dust particles on the mask or wafer, or in processing chemicals. It can be modeled as a small resistance on the conducting layer, described in Figure 3.1.



Figure 3.1 Bridge Fault

There are four types in Bridge Faults: Metal1 Layer Short, Metal2 Layer Short,

Diffusion Layer Short, Poly Layer Short. And this resistance of bridge fault is derived as

follows.Furthermore, Table 3.1 shows various modeling resistances of bridge fault.

$$R_{bridge} = R_{sheet} \times \frac{W}{L} = R_{sheet} \times \frac{\pi}{2}$$

Туре	Sheet Resistance(Ω /sq)	Bridge Resistance(Ω)
M1 Layer Short	0.07	0.11
M2 Layer Short	0.07	0.11
N+ Diffusion Short	78.2	122.8
P+ Diffusion Short	150.7	236.7
Ploy Layer Short	8.9	13.98

Table 3.1 Modeling Resistance of Bridge Fault

3.2 Pinhole Fault

Because of oxygen deficiencies at the $Si-SiO_2$ interface, tensile stress, surface imperfections, chemical contamination, etc, pinhole fault becomes another part of analog fault. It can cause a high impedance defect to short different layers, described in Figure 3.2.





There are four types of pinhole faults, such as Metal1 Poly1 Pinhole, Metal1 Poly2 Pinhole, Metal1 Metal2 Pinhole, Poly1 Active Pinhole. And this resistance of pinhole fault is derived as follows. What's more, it is equivalent to contact or via between adjacent layers but the size is different. Table 3.2 shows various modeling resistance of pinhole fault.

Туре	Contact Resistance(Ω)	Size Ratio	Pinhole Resistance(Ω)
Metal1 Poly1 Pinhole	7.2	16	115.2
Metal1 Poly2 Pinhole	38.9	16	622.4
Metal1 Metal2 Pinhole	1.37	16	21.92
Poly Active Pinhole			100

 $R_{pinhole} = R_{contact} \times \frac{Area_{pinhole}}{Area_{contact}}$

Table 3.2 Modeling Resistance of Pinhole Fault

3.3 Break Fault

Break Fault forms an electrically insulating region that can cause open circuits. It may result from dust particles on the mask or oxygen deficiencies at interface, described in Figure 3.3.



Faults: OPENS, OPENVIA

Figure 3.3 Break Fault

There are four types, such as Metal1 and Diffusion Contact Open, Metal1 and Poly1 Contact Open, Metal1 and Poly2 Contact Open and Metal1 and Metal2 Via Open. It is modeled as a large resistance between interconnection.

 $R_{break}\approx 10 M\Omega$

CHAPTER 4

DEFECT PROBABILITY

Defect probability is employed by the set of random number generator and then place local defects on the layout of a chip. We assume that the defects in one process are treated independently. Therefore, the discussion of defect probability is only on the standard 0.35 um process technology. What's more, the defect size distribution method is applied in the statistics of defect probability.

4.1 Defect Size Distribution

The models of defects are based on extra or missing materials as circles. Therefore, the size of defects is proportional to the diameter of these circles. There is a peak frequency X0 when the diameter is increasing. The frequency peaks at the smallest diameter that can resolved by the lithography process. We utilize a defect size distribution from the reference [11], shown in Figure 4.1.



Figure 4.1 Defect size distribution

$$S(x) = \begin{cases} D\frac{x}{x_0^2} & , 0 \le x \le x_0 \\ D\frac{x_0^2}{x^3} & , x_0 \le x \le \infty \end{cases}$$

D: density defect

x: diameter of a defect (random variable)

x₀: the defect diameter observed most often (experimental parameter)

All the metal lines have the minimum spacing S. In the real practice, S is larger than X0. Therefore, the shaded area of the distribution in Figure 4.2 shows the defect probability [12].



Figure 4.2Truncated defect size distribution

$$F = \frac{X_0^2}{16r^2} for \frac{X_0}{2} < r < \infty$$

4.2 Bridge Defect Probability

General probability of bridge defect can be calculated by this equation below:

$$Defect_i Probability = W_{eff} \times L \times Density(defect_i) for W_{min} > X_0$$

where L, W and Density(defect i) are length, width, and density of ith defect separately.Figure 4.3 shows the typical scenario of bridge defect, where yellow circles indicates the critical region for the bridge defect.



Figure 4.3 Bridge Defect Probability

4.3 Pinhole Defect Probability

Figure 4.4 shows the typical scenario of pinhole defect, where the overlap area indicates the critical region for the pinhole defect. The correlated probability can be calculated by this equation below.



Figure 4.4 Pinhole Defect Probability

4.4 Break Defect Probability

Figure 4.5 shows the typical scenario of break defect, where the yellow circle indicates the break defect to block vias and contacts. The occurred probability is calculated by these equations below.



Figure 4.5 Break Defect Probability

4.5 Defect Probability Statistics

In overall, all the defects cenarios are applied to the layout of fully differential opamp with CMFB. Defect probability statistics is shown in Table 4.2 with the defect density [13] [14] shown in Table 4.1.

Туре	Density
M1 short	1
M2 short	1.5
Diff short	1
Poly short	1.25
M1 P1 pinhole	0.05
M1 M2 pinhole	0.05
M1 P2 pinhole	0.05
M1 diff contacts open	0.66
M1 P1 contacts open	0.67
M1 P2 contacts open	0.67
M2 M1 vias open	0.8
P1 Active pinhole	0.05

Table 4.1 Defect Density Table

Туре	Density	Relative	total	Percentage	
		Probability			
M1 short	1	2.725431	15.57064	0.175037	
M2 short	1.5	0.758526	15.57064	0.048715	
Diff shrot	1	0.411342	15.57064	0.026418	

Poly short	1.25	0.216969	15.57064	0.013935
M1 P1 pinhole	0.05	0.356	15.57064	0.022864
M1 M2 pinhole	0.05	2.955	15.57064	0.18978
M1 P2 pinhole	0.05	0.048	15.57064	0.003083
M1 diff contacts open	0.66	0.144375	15.57064	0.009272
M1 P1 contacts open	0.67	0.25125	15.57064	0.016136
M1 P2 contacts open	0.67	0.08375	15.57064	0.005379
M2 M1 vias open	0.8	0.8	15.57064	0.051379
P1 Active pinhole	0.05	6.82	15.57064	0.438004

Table 4.2 Defect Probability Statistics

CHAPTER 5

DEFECT REDUCTION

In order to reduce the simulation burden to an affordable level, the defect reduction must be considered into this research. We can select a subset of most likely faults to simulate while limiting the DPPM impact of upgraded faults. In assumption [10], if the relative probability of selected faults up to 99.9%, and the overall yield of the circuit is 90%, then the DPPM impact of the faults will be upper bounded by 100.

5.1 Defect Coverage

Based on the assumption above, it is reasonable to set defect coverage to 90 percent taken the test time into account. For example, in industry, the typical defect coverage for PMIC is around 60%.

There are originally 552 analog defects in the layout of op-amp. After the 90 percent defect coverage reduction, the total number of defects be simulated decreases to 343.

5.2 Improved Layout Rules

Improved layout rules can also lead to defect reduction.

For break faults, if we double the contacts or vias instead of only one contact or via, its probability decreases by 50% at least.

For pinhole faults, if we try the best to eliminate the overlap of two adjacent different layers, its defects number can decreases a lot.

Therefore, the number of defect situation in this op-amp layout decreases to 95. The reduced defects are mainly bridge defects.

CHAPTER 6

DEFECT SIMULATION

6.1 Defect Location

Figure 6.1, 6.2, 6.3, 6.4 show the defect locations to be simulated. Based on the specific layout location and defect modeling as discussed above, each defect can be simulated by Hspice tool in Cadence.



Figure 6.1 Defects Located in Bias Layout



Figure 6.2 Defects Located in CMFB layout



Figure 6.3 Defect located in PMOS of Op-amp



Figure 6.4 Defect located in NMOS of Op-amp

6.2 One Fault Simulation

We inject all the defects to the layout of op-amp, thensimulate only one defect each time by Hspice of Cadence to establish the defect library shown in Flow Chart below, described in Figure 6.4.



Figure 6.4 Simulation Flow

Because the fault scan tool in real practice can check approximately 10 transistors layout in one micro picture, therefore, this op-amp is categorized into four parts by the function and layout location such as bias circuit, first stage, output stage and CMFB. The defect simulation for each part is shown in Table 6.5, Table 6.6, Table 6.7, Table 6.8 respectively. The specifications for each defect simulation involve offset voltage, supply current, DC gain, cutoff frequency, phase margin, PSRR, CMRR.

No.	Offset	Id	DC gain	Cutoff	Phase Margin	PSRR	CMRR	Description
	(V)	(A)	(dB)	Frequency(Hz)	(degree)			
1	-1.80E-16	2.36E-03	42.7	4.36E+08	7.08E+01	3.37E+02	3.00E+02	
3	5.55E-17	5.27E-05	20.21	1.59E+06	1.00E+02	unstable	unstable	
5	5.55E-17	5.27E-05	20.21	1.59E+06	1.00E+02	unstable	unstable	
6	5.55E-17	5.27E-05	20.21	1.59E+06	1.00E+02	unstable	unstable	
9	2.22E-16	8.74E-04	62.77	4.65E+08	4.52E+01	3.40E+02	2.92E+02	soft
10	2.22E-16	8.74E-04	62.77	4.65E+08	4.52E+01	3.40E+02	2.92E+02	soft
11	-4.44E-16	3.65E-03	40.43	4.18E+08	7.27E+01	unstable	unstable	

12	2.22E-16	2.19E-03	42.4	4.34E+08	7.11E+01	3.56E+02	2.88E+02	
21	-4.44E-16	3.65E-03	40.43	4.18E+08	7.27E+01	unstable	unstable	

Table 6.1 Bias Defect Simulation

No.	Offset	Id	DC gain	Cutoff	Phase	PSRR	CMRR	Description
	(V)	(A)	(dB)	Frequency	Margin			
				(Hz)	(degree)			
23	3.00E-14	8.74E-04	62.77	4.65E+08	4.52E+01	3.37E+02	3.00E+02	soft
24	-9.77E-15	1.83E-03	62.94	4.68E+08	4.53E+01	unstable	unstable	
25	7.30E-02	8.68E-04	63.47	4.92E+08	4.00E+01	1.00E+02	7.00E+01	
29	-4.00E-15	7.58E-04	32.14	7.12E+07	8.76E+01	unstable	unstable	
30	2.25E-01	8.80E-04	41.65	1.69E+08	8.38E+01	1.65E+02	1.80E+01	
34	-6.11E-16	9.69E-04	45.24	1.74E+08	5.62E+01	unstable	unstable	
35	-4.44E-15	7.28E-04	32.14	7.12E+07	8.76E+01	unstable	unstable	
36	-9.77E-15	1.83E-03	62.84	4.68E+08	4.53E+01	unstable	unstable	
37	1.58E-15	9.67E-04	33.27	8.36E+07	8.90E+01	unstable	unstable	
38	-4.44E-15	7.28E-06	32.14	7.12E+07	8.76E+01	unstable	unstable	
39	-7.30E-02	8.68E-04	63.47	4.88E+08	4.06E+01	1.00E+02	7.00E+01	
40	7.30E-02	8.68E-04	63.46	4.92E+08	4.00E+01	1.00E+02	7.00E+01	
41	-8.80E-13	8.74E-04	62.77	4.65E+08	4.52E+01	3.37E+02	3.00E+02	soft
42	-8.80E-13	8.74E-04	57.1	3.50E+08	4.47E+01	2.70E+02	2.20E+02	
43	1.28E-12	8.74E-04	57.1	3.51E+08	4.46E+01	2.70E+02	2.20E+02	
44	1.11E-16	9.39E-04	63.39	4.75E+08	4.63E+01	unstable	unstable	
45	1.11E-16	9.39E-04	63.39	4.75E+08	4.63E+01	unstable	unstable	
46	-4.44E-15	7.28E-04	32.14	7.12E+07	8.76E+01	unstable	unstable	
47	-4.44E-15	7.28E-04	32.14	7.12E+07	8.76E+01	unstable	unstable	

Table 6.2CMFB Defect Simulation

No.	Offset	Id	DC gain	Cutoff	Phase Margin	PSRR	CMRR	Description
	(V)	(A)	(dB)	Frequency(Hz)	(degree)			
55	0.00E+00	5.49E-03	negative		unstable	unstable	3.00E+02	
56	0.00E+00	5.49E-03	negative		unstable	unstable	3.01E+02	
56	0.00E+00	4.86E-03	negative		unstable	unstable	unstable	
57	-9.79E-02	5.44E-04	39.07	1.40E+08	unstable	8.40E+01	1.82E+01	

57	2.05E-02	5.39E-03	negative		unstable	unstable	unstable	
58	-9.79E-02	5.44E-04	39.07	1.40E+08	unstable	8.40E+01	1.82E+01	
58	-1.30E-01	5.60E-04	40.04	1.70E+08	6.68E+01	8.60E+01	1.80E+01	peak
59	9.79E-02	5.35E-04	40.08	1.50E+08	unstable	8.50E+01	1.92E+01	
59	1.89E+00	1.51E-03	negative		unstable	-7.00E+00	-1.40E+01	
60	9.79E-02	5.35E-04	40.08	1.50E+08	unstable	8.50E+01	1.92E+01	
60	1.30E-01	5.60E-04	41.06	2.02E+08	6.56E+01	8.80E+01	1.90E+01	peak
61	-9.19E-01	1.33E-03	50.04	1.97E+08	6.15E+01	1.15E+02	1.90E+01	peak
62	0.00E+00	5.23E-03	negative		unstable	1.50E+02	unstable	
63	0.00E+00	5.23E-03	negative		unstable	1.51E+02	unstable	
80	3.14E-02	5.49E-03	negative		unstable	-2.62E+00	3.01E+01	
81	0.00E+00	4.31E-04	23.5	5.62E+07	8.86E+01	unstable	unstable	
82	-6.55E-08	4.04E-04	negative		unstable	9.59E+00	1.63E+01	
83	1.65E+00	1.39E-03	24.17	8.06E+07	8.99E+01	5.09E+01	1.78E+01	peak
84	0.00E+00	8.74E-04	negative		unstable	2.23E+02	unstable	
85	-1.65E+00	1.39E-03	22.97	7.13E+07	8.93E+01	4.97E+01	1.66E+01	peak
86	2.49E-02	4.37E-04	10.36	1.79E+07	1.13E+02	4.59E+01	1.96E+01	
87	-3.33E-02	5.11E-03	negative		unstable	unstable	2.74E+01	
94	3.14E-02	5.49E-03	negative		unstable	-2.83E+00	2.96E+01	
110	0.00E+00	5.00E-04	negative		unstable	unstable	unstable	
111	0.00E+00	5.00E-04	negative		unstable	unstable	unstable	
112	0.00E+00	5.33E-03	negative		unstable	285.6	unstable	
113	0.00E+00	5.33E-03	negative		unstable	286.6	unstable	
114	-4.89E-15	9.49E-04	36.89	3.38E+08	5.66E+01	3.40E+02	3.39E+02	
115	-4.89E-15	9.49E-04	36.89	3.38E+08	5.66E+01	3.40E+02	3.39E+02	
142	0.00E+00	8.74E-04	negative		unstable	3.02E+02	unstable	

Table 6.3First Stage Defect Simulation (Note: Peak in description means unstable)

No.	offset(V)	Id(A)	DC	Cutoff	Phase	PSRR	CMRR	Description
			gain(dB)	Frequecny(Hz)	Margin(degree)			
49	3.00E-14	8.74E-04	62.77	4.65E+08	4.52E+01	3.37E+02	3.00E+02	soft
50	-9.95E-02	9.73E-04	33.56	8.00E+07	7.59E+01	1.60E+02	1.80E+01	
51	-9.95E-02	9.73E-04	33.56	8.00E+07	7.59E+01	1.60E+02	1.80E+01	
52	-2.15E-01	9.02E-04	40.68	1.77E+08	7.73E+01	9.00E+01	1.60E+01	

53	-2.15E-01	9.02E-04	40.68	1.77E+08	7.73E+01	9.00E+01	1.60E+01	
64	2.15E-01	9.02E-04	41.95	2.03E+08	7.86E+01	9.20E+01	1.70E+01	
65	3.00E-14	8.74E-04	62.77	4.65E+08	4.52E+01	3.37E+02	3.00E+02	soft
67	2.15E-01	9.02E-04	41.95	2.03E+08	7.86E+01	9.20E+01	1.70E+01	
68	1.03E+00	1.91E-03	66.92	5.34E+08	8.30E+00	6.80E+01	2.12E+01	
69	1.03E+00	1.91E-03	66.92	5.34E+08	8.30E+00	6.80E+01	2.12E+01	
70	3.00E-14	8.74E-04	62.77	4.65E+08	4.52E+01	3.37E+02	3.00E+02	soft
75	-9.95E-02	9.73E-04	33.56	8.00E+07	7.59E+01	1.62E+02	1.81E+01	
76	-2.15E-01	8.74E-04	40.68	1.71E+08	8.13E+01	1.05E+02	1.61E+01	
77	-2.15E-01	8.74E-04	40.68	1.71E+08	8.13E+01	1.05E+02	1.61E+01	
78	-1.74E-01	8.71E-04	51.26	2.85E+08	5.42E+01	1.98E+02	1.91E+01	
79	2.15E-01	8.82E-04	41.98	2.08E+08	8.89E+01	1.18E+02	1.74E+01	
88	-2.15E-01	8.82E-04	40.71	1.76E+08	8.79E+01	1.17E+02	1.62E+01	
89	2.15E-01	8.52E-04	41.94	2.08E+08	7.57E+01	1.69E+02	1.73E+01	
90	2.15E-01	8.74E-04	41.95	1.98E+08	8.23E+01	1.06E+02	1.73E+01	
91	2.15E-01	8.74E-04	41.95	1.98E+08	8.23E+01	1.06E+02	1.73E+01	
92	9.95E-02	9.73E-04	32.43	7.69E+07	8.23E+01	1.61E+02	1.69E+01	
105	-3.75E-16	9.72E-04	42.57	1.47E+08	6.00E+01	unstable	3.24E+02	
106	-3.75E-16	9.72E-04	42.57	1.47E+08	6.00E+01	unstable	3.25E+02	
108	-1.07E-01	8.72E-04	49.27	3.57E+08	6.97E+01	3.34E+02	3.06E+01	
109	2.12E-01	8.79E-04	44.49	2.28E+08	8.15E+01	1.27E+02	1.85E+01	
116	-2.12E-01	8.79E-04	43.31	2.00E+08	8.02E+01	1.26E+02	1.74E+01	
117	1.07E-01	8.72E-04	49.01	3.34E+08	7.09E+01	3.33E+02	3.03E+01	
119	3.75E-16	9.72E-04	42.57	1.47E+08	6.00E+01	unstable	3.20E+02	
120	3.75E-16	9.72E-04	42.57	1.47E+08	6.00E+01	unstable	3.21E+02	
130	-8.33E-02	4.91E-04	24.59	9.72E+07	7.72E+01	1.21E+02	1.86E+01	
131	8.34E-02	4.91E-04	25.58	1.07E+08	7.86E+01	1.23E+02	1.95E+01	
140	9.95E-02	9.73E-04	32.43	7.69E+07	8.23E+01	1.60E+02	1.69E+01	
141	-9.95E-02	9.73E-04	33.56	8.00E+07	7.59E+01	1.61E+02	1.81E+01	

 Table 6.4 Output Stage Defect Simulation

CHAPTER 7

DIAGNOSIS METHODOLOGY



7.1 Fault Free Monte Carlo Simulation

Figure 7.1 Bandwidth Monte Carlo Simulation (1000 sets)



Figure 7.2 DC Monte Carlo Simulation (1000 sets)



Figure 7.3 Gain Margin Monte Carlo Simulation (1000 sets)



Figure 7.4 Ids Monte Carlo Simulation (1000 sets)



Figure 7.5 Offset Monte Carlo Simulation (1000 sets)



Figure 7.6 Phase Margin Monte Carlo Simulation (1000 sets)

7.2 One Fault Monte Carlo Simulation

No	BWσ(MHz)	$BW\delta(MHz)$	$\text{Gain}\sigma(dB)$	$\text{Gain}\delta(dB)$	$GM\sigma(dB)$	$GM\delta(dB)$	$Ids\sigma(uA)$	$\text{Ids}\delta(uA)$	$\text{Offset}\sigma(mV)$	$\text{Offset}\delta(mV)$	PMo(°)	PM	δ(°)
0	59.53	6.21	44.51	7.09	19.25	0.67	531.92	84.01	-23.92	695.59	86.53		1.25
1	97.64	5.57	37.43	3.47	18.14	0.35	1356.31	84.02	52.51	251.57	89.16		1.48
2	1.61	1.12	44.77	11.28	36.67	0.58	9.32	6.37	159.77	955.15	88.31		2.95
3	62.02	5.21	44.61	7.02	19.05	0.55	563.64	71.76	134.14	650	86.73		1.27
4	51.46	16.38	44.38	8.63	20.81	4.62	444.89	153.52	146.47	708.55	86.94		2.79
5	35.53	21.78	42.11	11.17	24.31	7.16	288.07	187.12	168.09	736.9	87.94		4.4
6	66.26	4.84	44.28	6.58	18.84	0.5	626.67	70.25	125.8	607.75	86.92		1.29
7	0.475	0.479	42.56	10.62	36.89	0.39	2.91	2.82	121.44	817.36	88.7		3.67
8	87.19	4.73	41.05	4.2	18.41	0.4	1056.43	74.62	77.09	372.41	88.28		1.45
9	28.38	15.63	-22.25	4.76	40.29	0.75	29.67	4.47	0.45	2.36	na	na	
10	66.07	5.75	44.27	6.63	18.86	0.54	619.96	83.39	125.71	610.95	86.92		1.3
11	81.8	8.33	-4.9	4.79	22.64	0.76	2160.71	138.85	1.8	17.25	na	na	
12	54.05	5.62	26.4	0.34	19.98	0.31	671.06	82.55	12.14	73.75	90.88		0.86
13	0.14	0.07	-9.25	5.88	na	na	367.4	53.4	0.19	1.31	na	na	
14	37.76	3.64	-6.62	0.41	23.52	0.3	342.81	49.6	0.04	0.38	na	na	
15	56.79	5.96	42.82	2.04	19.73	0.59	537.24	78.04	78.77	425.86	86.59		1.04
16	11.82	1.54	-5.61	5.47	32.42	0.63	2885.97	323.89	1	19.28	na	na	
17	0	0	-89.72	0.65	na	na	49.97	7.53	-0.003	0.127	na	na	
18	0	0	-89.81	0.65	na	na	651.75	91.81	0.008	142.43	na	na	
19	na	na	-36.59	0.45	36.7	0.47	481.75	73.02	1606.2	23.34	na	na	
20	na	na	-32.83	0.61	33.08	0.68	482.14	72.92	-1605.14	22.48	na	na	
21	51.34	5.9	-1.83	0.59	21.5	0.45	507.36	76.57	1603.73	15.6	na	na	
22	48.54	5.29	-1.86	0.6	21.14	0.53	507.59	76.49	-1603.04	15.2	na	na	
23	37.38	3.98	40.51	4.16	21.32	0.49	524.45	79.61	705.11	382.25	94.73		1
24	37.77	4.17	41.92	3.98	22.93	0.55	524.52	79.58	-563.19	408.53	93.27		1.11
25	39.74	4.13	20.62	1.75	22.96	0.54	530.84	80.54	-1145.96	57.54	96.24		1.19
26	39.63	4.13	20.08	1.41	28.12	0.68	530.6	80.61	1157.04	63.07	95.86		1.03
27	32.58	3.39	-0.38	0.43	23.24	0.53	569.42	85.79	-1543.08	26.05	na	na	
28	32.42	3.01	-0.71	0.31	28.34	0.59	568.95	85.93	1543.85	26.85	na	na	
29	37.72	3.64	-6.62	0.41	23.54	0.3	341.12	49.43	0.04	0.38	na	na	
30	59.03	6.16	44.88	7.39	19.24	0.62	524.46	79.6	140.98	690.05	86.61		1.26
31	54.39	5.53	4.88	0.8	20.3	0.57	555.54	82.85	0.63	5.29	122.69		4.04
32	37.72	3.64	-6.62	0.41	23.54	0.3	371.28	52.57	43.17	381.66	na	na	
33	53.95	5.45	-1.65	0.82	20.38	0.58	2338.77	128.12	0.28	2.45	na	na	
34	49.15	5.36	38.19	10.75	21.98	0.65	523.95	79.64	151.38	451.61	81.8		2.44
35	48.81	5.29	38.08	10.31	23.69	0.68	524.28	79.55	32.14	447.77	80.84		2.43
36	59.04	6.16	44.77	7.33	19.24	0.62	1.73E+07	2.75E+06	138.83	679.31	86.61		1.25

Table 7.1 One Fault Monte Carlo Simulation (100 sets)

7.3 Ambiguity Groups

Based on MC simulation results in Table 7.1, defects can be coarsely divided into 5 groups [15] [16] [17].

Group Name	Defect Number
Soft Defect(8 green)	3,4,6,10,15,30,34,35
BW&PM not estimated Defect(2 blue)	19,20
GM&PM not estimated Defect(3 red)	13,17,18
Only PM not estimated Defect(11 orange)	9,11,14,16,21,22,27,28,29,32,33
Other Defect(12 white)	1,2,5,7,8,12,23,24,25,26,31,36

Table 7.2 Ambiguity Coarse Groups

With Matlab programming, defects can be identified accurately in each group.

Defect	Ambiguity Group
19	19
20	20

Table 7.3 BW&PM not estimated Defect

Defect	Ambiguity Group
13	13
17	17
18	18

Table 7.4 GM&PM not estimated Defect

Defect	Ambiguity Group
9	9
11	11,33
14	14,29,32
16	16
21	21,28
22	22,27
27	22,27
28	21,28
29	14,29,32
32	14,29,32
33	11,33

Table7.5 Only PM not estimated Defect

Defect	Ambiguity Group
1	1,8
2	2,5,7
5	2,5,7,12,23,24
7	2,5,7
8	1,8
12	5,12
23	5,23,24
24	5,23,24
25	25
26	26
31	31
36	36

Table 7.6 Other Defect

CHAPTER 8

CONCLUSION

In this paper, we present Analog Fault Modeling, Simulation and Diagnosis that spans from the process and layout level to the circuit level. Analog defect are modeled and the corresponding probability are analyzed. In addition, we construct fault library using an efficient hierarchical process variation analysis after defect reduction.

Monte Carlo Simulation and Bayesian Theory are also introduced in this paper. Our objective is a fully differential operational amplifier with common mode feedback. It shows that more than 50% of process and layout level fault can be diagnosed by ambiguity groups.

In the future, we will developed an automotive analog testing tool to help industrial establish an effective and efficient testing system.

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