Nanowire Specialty Diodes for Integrated Applications

by

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ABSTRACT

Semiconductor nanowires are important candidates for highly scaled three dimensional electronic devices. It is very advantageous to combine their scaling capability with the high yield of planar CMOS technology by integrating nanowire devices into planar circuits. The purpose of this research is to identify the challenges associated with the fabrication of vertically oriented Si and Ge nanowire diodes and modeling their electrical behavior so that they can be utilized to create unique three dimensional architectures that can boost the scaling of electronic devices into the next generation.

In this study, vertical Ge and Si nanowire Schottky diodes have been fabricated using bottom-up vapor-liquid-solid (VLS) and top-down reactive ion etching (RIE) approaches respectively. VLS growth yields nanowires with atomically smooth sidewalls at sub-50 nm diameters but suffers from the problem that the doping increases radially outwards from the core of the devices. RIE is much faster than VLS and does not suffer from the problem of non-uniform doping. However, it yields nanowires with rougher sidewalls and gets exceedingly inefficient in yielding vertical nanowires for diameters below 50 nm. The I-V characteristics of both Ge and Si nanowire diodes cannot be adequately fit by the thermionic emission model. Annealing in forming gas which passivates dangling bonds on the nanowire surface is shown to have a considerable impact on the current through the Si nanowire diodes indicating that fixed charges and traps on the surface of the devices play a major role in determining their electrical behavior. Also, due to the vertical geometry of the nanowire diodes, electric field lines originating from the metal and terminating on their sidewalls can directly modulate their conductivity. Both these effects have to be included in the model aimed at predicting the current through vertical nanowire diodes.

This study shows that the current through vertical nanowire diodes cannot be predicted accurately using the thermionic emission model which is suitable for planar devices and identifies the factors needed to build a comprehensive analytical model for predicting the current through vertically oriented nanowire diodes.

DEDICATION

To my mother whose love has lit up my life like the rays of the morning sun.

"*No language can express the power, and beauty, and heroism, and majesty of a mother's love. It shrinks not where man cowers, and grows stronger where man faints, and over wastes of worldly fortunes sends the radiance of its quenchless fidelity like a star.*" *--- Edwin Hubbell Chaplin*

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Prof. Trevor Thornton, the Director of CSSER at ASU was generous enough to share some of his experience in fabricating metal Schottky contacts, which proved very helpful for us. He also made special arrangements for getting me trained on a wide variety of fabrication equipment in a relatively small amount of time. This would not have been possible of course, without the dedication of the members of the CSSER staff who have made themselves available for providing assistance and guidance to me. Thanks to Jon Martin, Art Handugan, Carrie Sinclair, Paul Boland and Jerry Eller for providing me the tools I needed to conduct my experiments but sometimes, did not have. Art Handugan is a very patient and dedicated instructor who conducted my training on the electron beam lithography system. His detailed explanations and considerable experience with the tool helped me get a firm grip on what turned out to be the most important step in the entire fabrication process I developed during this research. Stefan Myhajlenko, the

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My deepest regards are reserved for my mother whose love, encouragement and guidance are the reasons behind all that I have achieved. She has a constant source of inspiration for me during tough times and her teachings have had a profound effect on my personality. Without her love and support it would have been nearly impossible for me to overcome all the challenges I have faced till this day.

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LIST OF SYMBOLS

q: Elementary charge (1.6×10^{-19}C)

n_i: Intrinsic concentration of charge carriers (cm^{-3})

Dn, Dp: Diffusion coefficient of electrons and holes respectively (cm^2s^{-1})

Ln, Lp: Diffusion length of electrons and holes (cm)

N_A, N_D: Acceptor and donor concentration (cm^{-3})

V: Voltage applied externally to the diode (Volt)

n: Ideality factor of a diode

k: Boltzmann constant ($1.38 \times 10^{-23}JK^{-1}$)

T: Absolute temperature (K)

A: Area of cross section of the diode (cm^2)

W: Width of the depletion region (cm)

τ_{SCR}: Minority carrier recombination lifetime inside the space charge region (sec)

A^*: Richardson constant ($A\ cm^{-2}K^{-2}$)

ϕ_B: Schottky barrier height (eV)

r_S: Series resistance of the diode (Ω)

ϕ_{Bn}: Schottky barrier height for electrons (eV)

J_n: Electron current density ($A\ cm^{-2}$)

F: Image force on the electron (N)

ε_0: Permittivity of free space ($F\ cm^{-1}$)

$PE(x)$: Potential energy of the electron at x cm from the surface of the semiconductor (Joule)

E: Electric field ($V\ cm^{-1}$)

$\Delta\phi$: Lowering in Schottky barrier height (eV)

x_m: Distance from the semiconductor at which the $PE(x)$ is the maximum

γ: Surface energy (Joule)

Ω: Molar volume (cm^3/mol)

p: Partial pressure of a gas (Torr)

p^{∞}: Partial pressure of the gas in equilibrium with a planar surface

r: Radius of a droplet of a liquid phase in equilibrium with the vapor phase of any solute species

σ: Interfacial energy between the molten metal droplet and the nucleation site (Joule)

ΔG_V: Decrease in volume free energy (Joule)

C: Solute concentration within the molten metal catalyst droplet (cm^{-3})

C^*: Equilibrium concentration of the solute species in the molten metal (cm^{-3})

φ: Contact angle of the metal catalyst droplet with the tip of the tip of the nanowire (radian)

α_S, αL: Solid-vapor and liquid-vapor interface tensions respectively (J cm^{-2})

δ: Conical angle of the nanowire (radian)

σ_i: Surface energy of a facet (Joule)

α_i: Area of the facet (cm^2)

Δz: Thickness of the interface of the metal catalyst droplet with the Si substrate (cm)

σ_S: Surface energy of the substrate (Joule)

L: Circumference of the interface of the metal catalyst droplet with the substrate (cm)

σ_{LS}: Liquid-solid interface tension (J cm^{-2})

A: is the area of the interface (cm^2)

γ: Contrast

D_0: Minimum dose at which the resist is cleared all the way down to the substrate (C cm^{-2})

D_1: Maximum dose below which the full thickness of the resist is retained (C cm^{-2})

d: Diameter of the electron beam spot (cm)

I: Beam current (Ampere)

NA: Numerical aperture of the electron lens

I_S: Reverse saturation current of a Schottky diode (Ampere)

V_{FB}: Flat band voltage (Volt)

ϕ_{MS}: Difference in work function between the metal and semiconductor in a MOS device (eV)

Q_f: Sheet density of fixed charge at the oxide-semiconductor interface (C cm^{-2})

C_{OX}: Capacitance per unit area of the oxide in a MOS structure (F cm^{-2})

t_{OX}: Thickness of the oxide in a MOS structure (cm)

$\rho_{OX}(x)$: Volume charge density trapped in the oxide of a MOS structure as a function of distance (x) from the oxide-semiconductor interface.

Q_{IT}: Sheet charge density due to traps at the oxide-semiconductor interface (C cm^{-2})

ϕ_S: Surface potential of the semiconductor (Volt)

C_{SFB}: Capacitance per unit area due to dielectric relaxation in a semiconductor under flat band condition (F cm^{-2})

L_D: Debye length (cm)

C_{FB}: Capacitance of the MOS structure at flat band condition (F)

C_{SCR}: Capacitance of the space charge region under the Schottky contact inside the nanowire diode (F)

CM_{OS}: Capacitance due to the metal/SOG/Si substrate MOS structure (F)

R_{Si}: Resistance of the Si substrate under the nanowire (Ω)

R_{NW}: Resistance of the quasi-neutral region inside the nanowire (Ω)

Z_{DUT}: AC Impedance of the device under test (Ω)

Z_1, Z_2 and Z_3: Known AC impedances in the bridge circuit of a LCR meter (Ω)

C_{COU}: Coupling capacitance between the surface of the nanowire and the metal contact at its tip (F)

C_{Si}: Capacitance of the depletion region formed on the surface of the Si substrate (F)

G_{Si}: AC conductance of the Si substrate (S)

G_{NW}: AC conductance of the nanowire (S)

ω: Frequency of capacitance vs. voltage measurement performed on the nanowire diode (radian)

PREFACE

The work presented in this report is original. All the experiments presented henceforth, were conducted in the Center of Solid State Electronics Research (CSSER), at Arizona State University in collaboration with the Center for Integrated Nanotechnologies (CINT) at Los Alamos National Laboratory (LANL). This research was directed by Prof. Stephen M. Goodnick and Dr. Clarence J. Tracy in collaboration with Dr. S. Tom Picraux who worked in CINT at LANL until December 2012. I was responsible for the design and execution of all experiments performed at CSSER under the direction of my academic advisor Prof. Stephen M. Goodnick and in consultation with my committee members Dr. Clarence J. Tracy, Prof. David K. Ferry and Prof. Hongbin Yu.

The growth of n-type Ge nanowires presented in chapter 4 was conducted using the recipe developed by Dr. Jeong-Hyun Cho under the supervision of Dr. S. Tom Picraux who worked as the Chief Scientist in CINT at LANL until December 2012. A part of chapter 3 has been published [Chandra, N.; Overvig, A.C.; Tracy, C.J.; Goodnick, S.M., "Fabrication and characterization of vertical Si nanopillar Schottky diodes," *Nanotechnology Materials and Devices Conference (NMDC), 2012 IEEE* , vol., no., pp.58,62, 16-19 Oct. 2012 doi: 10.1109/NMDC.2012.6527591]. I was responsible for supervising and / or conducting the experiments whose results are published in this report and all the work related to this publication was done using the facilities provided by CSSER. Adam C. Overvig, who is one of the co-authors of this publication, was an undergraduate student working with our research group through the Research Experience for Undergraduates (REU) initiative of the National Nanotechnology Infrastructure Network (NNIN). He worked directly under my supervision helping with the analysis of electrical data and conducting some of the experiments.

The study presented in chapter 6 is an original, independent and unpublished work which I have performed under the direction of Prof. Stephen M. Goodnick and Dr. Clarence J. Tracy. I am solely responsible for all the experiments conducted and the results presented in that chapter.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Scaling of semiconductor devices has driven the industry for over half a century. It has provided more functionality per unit area of the semiconductor at the same or lesser cost with every generation. Scaling is economical and provides circuits with better performance. However, the smaller a device gets, the more complicated it becomes to fabricate and understand the physics behind its working. Currently, the 22 nm technology node is in production and has been designed using tri-gate transistors also called FINFETs. This has been the first time that the basic structure of the MOSFET has changed from planar towards three-dimensional. Increased "off" current and reduced control of the gate over the channel current have forced the industry to take this step. Smaller transistors also tend to have lower reliability because they suffer a greater impact of gate oxide leakage, impact ionization, drain induced barrier lowering (DIBL), and gate induced drain leakage (GIDL) among other short channel effects. Alleviating short-channel effects and improving reliability raises the cost of an IC. Thus, it is becoming increasingly difficult to reduce the cost per function on an IC while staying on the aggressive scaling trend followed by the industry to date.

There is a strong motivation to look for alternative ways of building electronic devices out of which the semiconductor nanowire is an attractive option. Having a diameter of few tens of nanometers and lengths on the order of micrometers, nanowires can be made to work as vertically standing devices which occupy a substantially smaller area compared to planar devices. Moreover, if semiconductor nanowires can be integrated with planar technology, it will boost the scalability of the well-established process of fabricating planar integrated circuits. The main motivation behind this research is to fabricate and understand the electrical behavior of vertically oriented nanowire diodes. This process will serve as a platform for integration of any type of vertical nanowire device with planar CMOS circuits.

1.2 Statement and objectives of the current research

This research seeks to answer the following questions:

- Is it possible to integrate nanowire diodes into pre-determined locations on planar ICs?

- Once created, how can we probe them to measure their electrical characteristics?
- What mathematical models can explain the measured electrical behavior?
- How are the current conduction phenomena in nanowire diodes different from planar diodes?

The search for finding answers to these questions starts with choosing the material of the nanowire and the substrate. Since there is abundance of research on Si and Ge nanowires on Si and Ge substrates, we started with creating Si and Ge nanowires. After creating nanowires, they were encapsulated in a dielectric and metal contacts were fabricated on their tips. Then the electrical behavior of the nanowire diodes was characterized using current vs. voltage and capacitance vs. voltage measurements. Using small signal equivalent circuit models of the nanowire diode, we have made an attempt to explain their electrical behavior.

1.3 The importance of diodes

Studying the electrical behavior of nanowire diodes can be extremely beneficial for scaling down the size of a large variety of integrated circuits. A diode is a two-terminal device composed of two regions of semiconductors with different doping type and/or concentration. The purpose of a diode is to act as an electronic switch. An ideal diode provides a low resistance path for current in one direction (forward biased) and acts as an open circuit in the opposite direction (reverse biased). The simplest type of diode is the Schottky diode which is formed by the junction between a metal and a semiconductor. Schottky diodes have a very high switching speed between forward and reverse bias and low voltage drop during forward bias. Since only majority carriers are involved in current conduction the diode can respond very quickly to reversals in the applied voltage and it can be used at high frequencies. Due to low forward-biased voltage drop, Schottky diodes are used for clamping electrical signals.

The diode is a very versatile semiconductor device. Some of its other main uses are as a rectifier, photodetector, solar cell, light emitter, microwave generator and LASER. A p-n junction diode can detect temperature changes, light, solar energy and other types of electromagnetic radiation depending on the properties of the semiconductor used. The generation of charge carriers due to solar energy is used to generate electrical power in solar cells. Diodes are also used as switches in memory circuits where they are

used for addressing specific cells for storing and retrieving information. Light emitting diodes are used in electronic displays from something as simple as an eight-segment display to the screen of a high-definition flat panel television. Thus, diodes occupy a fundamental place among all the different types of electronic devices used in today's world.

1.4 Nanowire diode

A nanowire is a high aspect ratio cylindrical structure whose diameter is ~10-100 nm and its length can be on the order of several microns. If nanowires are fabricated vertically, they will occupy a very small planar area and have all the electrical functionality along their length. The fact that their length can be on the order of microns relaxes the tolerance on fabrication of different regions along the vertical dimension. In planar devices lithography becomes extremely critical in defining the device in two dimensions as their size is reduced. The tolerance for defining the dimensions of different regions on the device becomes extremely low. Planar devices also need a substrate whose thickness depends on the application. In photon capturing devices, the substrate has to be thick enough to absorb all the energy corresponding to the longest wavelength present in the incident radiation. In the case of nanowires, the substrate can be made as thin as possible based on the limits of the fabrication process because they can absorb the radiation all along their length and since their areal density can be very high, the net reflectance of a surface covered with vertically standing nanowires can be considerably lower compared to a planar surface even after texturing and application of anti-reflection (AR) coatings. Thus, vertically standing nanowire devices can provide integrated circuits which are not only extremely compact but also extremely thin compared to planar circuits. Diodes can be of several types but we plan to concentrate on Schottky diodes in this study because they are the simplest vertical nanowire devices and should serve as a foundation for developing the understanding of more complex nanowire structures. Today, nanowires can be grown in a controlled and reproducible way using the Vapor-Liquid-Solid (VLS) (bottom-up) approach. Another approach to form nanowires is top-down, by means of vertical reactive ion etching (RIE). Theoretically it is possible to form abrupt p-n junctions by switching the process gases containing dopant atoms during nanowire growth (Le, Jannaty, Zaslavsky, Dayeh, & Picraux, 2010). So, in principle both the VLS and vertical RIE approach are capable of fabricating almost all types of nanowire diodes.

1.5 State of the art in nanowire research

Most of the research performed till date on nanowires has been aimed at studying their properties (electrical, optical, mechanical etc.). A relatively fewer amount of studies have been reported about the fabrication of vertical nanowire devices so that they can work along with planar devices in the form of an integrated circuit. The studies regarding fabrication of vertical nanowire diodes are of special interest to us. We will make a brief mention about them in this section and describe them in detail later in the second chapter.

Electroluminescence and photoluminescence of ZnO nanowires has been reported (Lai, Kim, & Yang, 2008). A more recent study of vertically standing AlGaN nanowire LEDs on n-type (111) Si substrates has also been reported (Carnevale et al., 2013). The nanowires were grown using MBE and contacted individually using AFM tip. Aluminum Schottky contacts to a single GaN nanowire laid horizontally on thermally grown SiO_2 on a Si substrate have been reported (Kim et al., 2002). Although rectifying behavior was observed yet, the ideality factor was 17.8 indicating a very poor fit with the thermionic emission model. Vertically oriented Si nanowire p-n junction diodes with Ti/Au top contacts have been reported (Tang, Kamins, Liu, Grupp, & Harris, 2005). These nanowires were grown by CVD using Ti as catalyst. A vertical MOSFET type of structure has been reported using p-type Si nanowires on a p-type Si substrate (Goldberger, Hochbaum, Fan, & Yang, 2006). The length of the gate was controlled by the thickness of the dielectric deposited along the length of the nanowire and the voltage applied at the gate contact was used to modulate the current through it. Vertically oriented p-n junction tunnel diodes have been reported by growing n-type Si nanowires on degenerately doped p-type Si substrates (Schmid, Bessire, Björk, Schenk, & Riel, 2012). A peak to valley current ratio (PVCR) of 4.29 was reported in this study. Vertical Si p-n junction nanowire diodes by growing p-type Si substrates using Vapor-Liquid-Solid (VLS) technique on n-type Si substrates have also been reported (Jackson, Kapoor, Jun, & Miller, 2007).

Fermi level pinning is a phenomenon which is caused by electrically active defects at the interface of the metal and the semiconductor in Schottky diodes. It tends to fix the barrier height of the diode making it independent of the work function of the metal. It has been reported that in Ge Schottky diodes, S atoms implanted at the Ni/Ge interface can alleviate Fermi level pinning (Ikeda, Yamashita, Sugiyama, Taoka, &

Takagi, 2006). The cause of Fermi level pinning has been cited as the presence of defects on the Ge surface (Zhou et al., 2010). De-pinning of the Fermi level by laser annealing of the Ni/Ge interface to form $NiGe_2$ has also been reported (Lim, Chi, Wang, & Yeo, 2012). The effect of annealing temperature on the Schottky barrier height of diodes formed by depositing Ti, Pt and Ni on n-type Ge has been studied in detail (Chawanda et al., 2010). Schottky barrier diodes formed by monolayer graphene (MLG) on Ge have been shown to work as photodetectors under reverse bias (Zeng et al., 2013).

1.6 Contribution of this work

This research extends the current knowledge about the factors affecting the conduction of current in vertically oriented nanowire Schottky diodes. It starts with the development of fabrication processes for n-type Ge and Si nanowires on Ge and Si substrates respectively. Bottom-up Vapor-Liquid-Solid (VLS) and top-down Reactive-Ion-Etching (RIE) approaches have been followed here to create vertically oriented nanowires. Once the nanowires are created and electrical contacts are made to them at their tips, it is shown that their DC current vs. voltage behavior cannot be explained purely on the basis of thermionic emission as their ideality factors are higher than 1. In order to investigate the main factors affecting current conduction in nanowire diodes, we have investigated the effect of passivation on the surface of these devices. N-type Si nanowires were created on n-type Si substrates using vertical RIE. Three types of surface passivations, namely thermal oxide, amorphous Si and un-passivated nanowires were compared in terms of their DC current vs. voltage and AC capacitance and conductance vs. voltage measurements. Analytical models have been proposed for the nanowire Schottky diode working under accumulation (forward bias), depletion and inversion (reverse bias). The net admittance for the different bias conditions has been derived to yield analytical expressions for capacitance and conductance of the device. These quantities are compared and shown to be in agreement with the measured values from actual arrays of nanowires proving the validity of the proposed model.

Hence, this research extends the understanding about the working of nanowire diodes by simplifying it into easily understandable small signal equivalent circuit models. It provides experimental evidence that the condition of charges on the nanowire surface governs the overall current as a function of voltage applied to the device. The main conclusion from this research is that for having a stable and high

yield process of fabrication of vertical nanowire devices, the energy distribution of electrically active defects on their surfaces must be undertaken.

1.7 Outline

This remaining part of this study is divided into seven chapters. Chapter 2 presents in detail, the background behind research on nanowires, the kinetics of their fabrication using the VLS technique, the rate of growth, shape, direction and quality of the nanowires, different materials used for making nanowires along with their uses and a discussion about imperfections commonly observed during nanowire growth. Prior research on nanowire diodes and Schottky barrier diodes is also discussed in the second chapter. The third chapter presents a discussion about understanding the working of nanowire diodes through simulations. The simulation results in this chapter act as a reference for the electrical behavior of real nanowire diodes presented later in this work. Bottom-up and top-down processes for fabrication of vertical Ge and Si nanowire Schottky diodes have been demonstrated in chapter 4. Chapter 5 presents I-V measurements performed on Ge nanowire diodes and their analysis using the thermionic emission model. Chapter 6 describes the effect of surface passivation on the electrical characteristics of Si nanowire diodes. DC current vs. voltage and AC capacitance vs. voltage measurements performed on the diodes are used to explain the reasons behind the observed electrical behavior of the devices. Chapter 7 summarizes the achievements of this research and in light of the results obtained here it lists the topics of further investigation which are critical for modeling the electrical behavior of nanowire diodes.

CHAPTER 2

NANOWIRES: BACKGROUND, FABRICATION AND USES

2.1 Introduction

This chapter provides a background on nanowires in a general way. It starts with a brief introduction to nanotechnology followed by a discussion about the invention of nanowires. Different types of nanowires along with their main applications are presented in this chapter. For the most part, the chapter focuses on the VLS process of growing semiconductor nanowires. The discussion presents how nanowire growth is initiated by the diffusion of source gases into catalysts on the substrate. It explains that the size of the metal catalyst cluster determines whether or not, it is possible to grow a single nanowire under it. Also, the phase diagram of the metal-semiconductor system sets the pressure and temperature conditions in which VLS growth can occur. The choice of metal impurity has to be made depending on the material of the nanowire. The shape and stability of the nanowires depends on the surface tension between the molten metal impurity and the semiconductor of the nanowire. Finally, the chapter discusses some imperfections that have been reported in nanowires grown using the VLS technique and possible explanations that have been offered. In this way, this chapter provides a theoretical background to the growth of nanowires, a general overview of different types of nanowires, their uses and the kinetics of the VLS technique used for growing semiconductor nanowires.

2.2 Nanotechnology

The capability of producing electronic devices smaller than 100 nm has been available for approximately three decades, but it was not until the last decade that researchers started looking carefully into the properties of materials at the nanoscale. Research on nanostructures systems has studied how the properties of nanoscale materials are different from their bulk counterparts and how they can give rise to systems with novel physical and chemical properties. (Klabunde & Richards, 2009) discusses that the delocalization of valence electrons in a material is inversely proportional to its dimension. As we move towards smaller dimensions, quantization of motion results in discrete energy levels just like in a molecule. This transition occurs gradually as the structure size is reduced. For example, it has been observed that the melting point of bulk Au is 1064 C however a 5 nm Au particle melts approximately 200 C below that

temperature. A 6 nm Pd particle has a specific heat 48% higher than that of bulk Pd at constant volume at 250K (Klabunde & Richards, 2009). Also, the ratio of the percentage of the number of atoms on the surface to that in the bulk increases rapidly with decrease in size of a particle. Therefore, the effects of surface phenomena like adsorption, surface conduction, solubility, etc. begin to dominate as dimensions are reduced. Scaling devices down to the nanometer scale has led us into a domain where materials are likely to show widely different behavior than they do at micro or millimeter scales.

The change in electrical properties of materials as a result of size scaling is of great interest to the semiconductor community. In a bulk material, electrical behavior can be modeled accurately by considering charge carriers as particles. However, as the dimensions of the conductor are reduced and become comparable to the inelastic mean free path of its charge carriers, we begin to observe ballistic transport and the behavior of charge carriers starts being dominated by their wave nature. Since the total number of particles in a nanoscale device is less, their phase interaction also becomes important. Quantization of electrical conductivity has been observed in split-gate Schottky contacts, quantum point contacts (QPC's) and Aharonov-Bohm (AB) rings (Ferry & Goodnick, 2009) which highlights the formation of discrete energy levels in 1-D semiconductor structures. Since nanoscale devices already have the obvious potential of creating very high density integrated circuits, it has become essential to study their properties and determine how they can outperform their bulk counterparts. Towards this end, numerous nano-structures have been fabricated and tested in laboratories around the world.

2.3 Nanowires

A nanowire is usually a cylindrical structure having a diameter of a few nanometers and a height up to a few microns. The earliest research on nanowires was on the growth of thin whiskers of silver from surfaces of silver sulfide around the 1940's, because they were found to be the cause of short circuits and the mechanism of their formation was not understood at that time (Levitt, 1970). Further, in 1952, Herring and Galt of Bell Telephone laboratories determined that the tensile strength of tin whiskers was much higher than bulk tin and in fact it approached the theoretical limit (Herring & Galt, 1952). Similar studies suggested that solids in whisker form had tensile strengths approaching theoretical limits. This was probably, the first indication that materials of reduced dimensionality have widely different physical

properties than their bulk properties. This difference was explained by the fact that whiskers had nearly perfect crystal structure with very few defects compared to bulk material. This discovery led to the development of methods for growing whiskers using single elements as well as compounds, including but not limited to metals and semiconductors. It was believed that screw dislocations which terminate on the surface of the substrate provide energetically favorable sites for atoms in vapor-phase to accumulate, and caused the anisotropic crystal formation of whiskers. The defect believed to permeate along the axis of the whisker causing growth to proceed in the preferred direction (Burton, Cabrera, & Frank, 1951). Therefore, many vapor-phase reactions were developed for growing whiskers of different materials. Analysis of Si whiskers grown by these methods however, showed the following important facts (Levitt, 1970):

a) The whiskers were perfect crystals and their growth was not initiated by a screw dislocation.
b) An impurity was important for growth of whiskers
c) The presence of liquid phase on the tip of the whiskers was noted during growth.

All these observations led to development of the Vapor-Liquid-Solid (VLS) mechanism proposed by Wagner and Ellis from Bell Telephone Laboratories in 1964 (Wagner & Ellis, 1964) which is discussed in detail in the later section 2.5.1. In 1975, Givargizov and Sheftal experimented with the growth of Si whiskers using 50-100 nm films of catalysts (Au, Ga, In). They concluded that the critical step which governs the rate of growth is the incorporation of Si atoms into the lattice at the tip of the whisker and the stability as well as the growth direction had a strong dependence on temperature (Meyyappan & Sunkara, 2010).

The whiskers discussed above were a few hundred microns in diameter. The transition from micron-scale whiskers to nanowires came around 1995 when they were first grown by Westwater et al. (Westwater, Gosain, Yamauchi, & Usui, 1995). They grew Si nanowires approximately 10 nm in diameter from 5 nm thick Au films and used silane as the source gas instead of Si tetrachloride used in earlier experiments with whisker growth. A couple of years later, this group studied the stability of Si nanowires as a function of silane concentration, temperature and nanowire diameter (Westwater, Gosain, Tomiya, Usui, & Ruda, 1997). Ozaki et al. also reported growth of Si nanowires with 6-30 nm diameter using thin Au films in 1998 (Ozaki, Ohno, & Takeda, 1998). At the same time, nanotechnology had gained significant

interest as the technology of the next generation of electronic devices. Hence, research activities in the area of inorganic nanowires in general and semiconductor nanowires in particular, started around the beginning of the 21st century.

2.4 The importance of nanowires

Vertical nanowires are ideal for fabricating high density integrated circuits because of their small planar footprint. The charge carriers are free to move in the axial direction only. If the diameter of the nanowire is on the order of a few nanometers, it can be a useful tool in studying the wave-like nature of electrons. Low-defect semiconductor nanowires with small diameters show the presence of discrete energy levels by exhibiting quantization of conductance. (Tilke, Simmel, Lorenz, Blick, & Kotthaus, 2003). Further confinement of electrons along the axis of the nanowire is possible with heterojunctions created within them (Björk et al., 2004; Thelander C. et al., 2003). Such nanowires may have quantum dot like structure sandwiched between two successive heterojunctions along their length which exhibit periodicity in conductance with variation in the confining potential.

Apart from providing evidence of quantum mechanical properties, semiconductor nanowires may be used as the channel region of MOSFET's (Cui, Zhong, Wang, Wang, & Lieber, 2003; Koo et al., 2004; Nguyen et al., 2004), concentrator photovoltaic cells (Pala, White, Barnard, Liu, & Brongersma, 2009; Tian et al., 2007), light-emitters (Hersee et al., 2009; Könenkamp, Word, & Schlegel, 2004), field-emission electron guns (Gangloff et al., 2004), lasers (Johnson et al., 2002), thin-film transistors (TFT's) (Duan et al., 2003), crossbar address decoders (Zhong, Wang, Cui, Bockrath, & Lieber, 2003) and diodes (Agarwal, Vijayaraghavan, Neuilly, Hijzen, & Hurkx, 2007; Jackson, Jun, Kapoor, & Miller, 2006). In all the above applications, semiconductor nanowires grown by a variety of techniques have been employed. The results from the above experiments indicate that although nanowires show the correct type of I-V behavior, considerable improvement is needed in their fabrication if they are to compete with their planar counterparts. This includes control over growth, defect density, stability orientation and position of nanowires. At the same time, the process has to be such that it is possible to be integrated into a standard planar CMOS process. When these challenges are overcome, it will push the current limits of scaling, down

to a few nanometers and result in highly integrated electronic systems with better performance than the existing ones.

2.5 Different types of nanowires

2.5.1 Semiconductor Nanowires

Si nanowires have received a lot of attention because of the huge amount of investment in Si technology around the world. Si growth technology has matured more than any other semiconductor partly because of the demand and partly because of the abundant availability of raw materials which are processed to make semiconductor grade Si. Today, defect-free Si wafers as large as 450 mm in diameter can be manufactured in large quantities. The depth of theoretical knowledge and the practical experience of manufacturing devices in Si is more than any other semiconductor. There are other materials like III-V compound semiconductors e.g. GaAs and wide bandgap materials like SiC, which are more suited to specific uses like light emission and high temperature operation but, it is not yet possible to make complex integrated circuits like microprocessors, using these materials. Germanium is another semiconductor which has properties similar to Si but, is more expensive a therefore, not so widely used. Thus, the most sought after semiconductor for making integrated nanowire devices in the future is Si. That being said, one should keep in mind that at nanoscale dimensions, the properties of a material can be very different from that observed in bulk. This makes it all the more interesting to make Si nanowire devices and see if some of the undesirable properties of Si can be engineered so as to make it even more versatile at the nanoscale. A great example of this is emission of light across the entire visible spectrum from Si nanowires (D. P. Yu et al., 1999). The wavelength of the emitted light was found to undergo a blue shift on reducing the diameter of the core using oxidation to form SiO_2 on the surface of the nanowires.

Apart from Si, Ge, has been fabricated into nanowires because of its lower bandgap (0.67eV indirect and 0.88eV direct), higher mobility and better light-emission efficiency. Germanium also has a larger exciton Bohr radius than Si hence, can exhibit quantum confinement effects at larger nanowire diameters as compared to Si. Nanowires of III-V materials like GaAs, $Al_xGa_{1-x}As$, InP, etc. have also been fabricated. These compound semiconductors have been engineered to produce a wide range of energy bandgaps. They have larger mobility and better response to high-frequency operation than Si. They have

been used to study quantum wells and superlattices which can be fabricated by growing thin layers of compound semiconductors over each other using Molecular Beam Epitaxy (MBE). Vertical Cavity Surface Emitting Lasers (VCSEL's) are a particularly attractive avenue for the use of nanowires because of the extreme confinement of charge carriers which a nanowire can provide by virtue of its structure.

2.5.2 Chalocogenide Nanowires

Phase change materials have the property of switching between amorphous and crystalline states based on the Joule heating produced by a current flowing through them. The amorphous and crystalline states have widely different electrical and optical properties because of which it can be used as a memory. The difference in optical properties is already being used commercially in storage media like compact disks (CD's) and Digital Versatile Disk (DVD's). With flash memory likely to reach its scaling limits, there is a huge demand for an alternative way of storing digital information in an ultra-high density solid-state memory. Phase-change RAM (PRAM) consists of a chalocogenide (phase-change) material sandwiched between two metal electrodes. It works by changing the resistivity of the chalocogenide by virtue of Joule heating produced due to current flow between the electrodes. The low and high resistance states are designated as logic "0" or "1". It is being thoroughly investigated for replacing flash memories because of its ease of fabrication, scalability, faster read/write speeds and simplicity of operation. The only major limitations of this memory are the large programming current required to change the state of the chalocogenide material and thermal interference between adjacent cells i.e. programming one bit might affect the state of the adjacent one because of proximity.

The idea of fabricating such memories from chalocogenide cells in the form of nanowires provides many interesting implications. It is a fact that the melting point of a material decreases on reducing the dimensions (Sun, Yu, Ng, & Meyyappan, 2007). Even at high levels of integration, nanowires can be written such that adjacent cells do not affect each other adversely (Sun, Yu, & Meyyappan, 2007). Also, because of the reduced size, lower overall currents can translate to sufficient current densities inside the cell which will help operate the memory at lower programming currents (B. Yu, Sun, Ju, Janes, & Meyyappan, 2008). Like other phase-change memories, the operation of nanowire PRAMs will not be affected by

radiation. GeTe, $Ge_2Sb_2Te_5$ (GST), In_2Se_3 and GeSb nanowires have already been fabricated (Meyyappan & Sunkara, 2010).

2.5.3 Metallic Nanowires

Metals in general, are used as conductors in electrical circuits. It is therefore a matter of great interest to investigate the changes in properties of metals at nanoscale dimensions. Nanowires have been fabricated using metals like Bismuth, Silver, Copper, Nickel and Zinc (Meyyappan & Sunkara, 2010). Bismuth nanowires have been shown to have a melting point proportional to their diameter but independent of the crystal orientation. Silver nanowires have high thermal and electrical conductivity. Copper is currently being used in interconnect metal lines on integrated circuits because of its high conductivity and resistance to electromigration. Thus, Cu nanowires have attracted a lot of attention. It has been found that copper nanowires are susceptible to changes in conductivity due to oxide formation on the surface. Also if Cu nanowires are transferred onto pre-patterned contacts, they show a very high resistance (Meyyappan & Sunkara, 2010). Copper nanowires placed in 230 nm deep SiO_2 trenches show reduced effect of oxidation but resistivity is still more than bulk because of scattering at the interface of Cu and SiO_2 and grain boundaries inside the nanowire. Overall, the current progress of research on Cu nanowires shows that their electrical properties are not better than bulk copper.

Nickel, because of its magnetic behavior has been fabricated into nanowires for potential applications in magnetic memories. Nickel nanowires exhibit either a stable face-centered cubic (FCC) or a metastable hexagonal close-packed (HCP) phase (Meyyappan & Sunkara, 2010). The hcp phase exhibits non-magnetic behavior. However, hcp changes to face centered cubic (FCC) under heat treatment and the nanowires exhibit a diameter dependent coercive field. The coercive field increases from 600 to 1200 Oe as the diameter is reduced from 55 to 30 nm (Nielsch et al., 2001).

Zinc nanowires have superconducting and light-emitting properties (Tong, Shao, Qian, & Ni, 2005; Wang, Tian, Kumar, & Mallouk, 2005). As with other materials, Zn nanowires show a “blue shift” of the emitted electromagnetic radiation providing evidence of increase in the energy bandgap at nanoscale dimensions. Zinc nanowires can be easily oxidized to form ZnO nanowires which have good light-emitting properties. Thus, Zn nanowires can be used to make light-emitting diodes and lasers.

2.5.4 Nanowires of other materials

Besides metals, chalocogenides and semiconductors compound nanowires have also been fabricated. Nanowires made out of oxides, sulfides and tellurides of metals have been grown by various methods (Meyyappan & Sunkara, 2010). The inspiration behind these experiments has been the quest for engineering the properties of these compounds for extending their utility beyond the limitations observed in their bulk state. These compounds in bulk state are light emitters, energy conversion/storage elements, catalysts, etc. which show interesting properties at the nanoscale.

2.6 Fabrication of semiconductor nanowires

As mentioned in the previous sections, nanowires of semiconductors, metals, chalocogenides and compounds like oxides, sulfides, antimonides and tellurides have been synthesized from their constituent elements by a number of methods. In this work, the main emphasis is on semiconductor nanowires made of Si and Ge. The methods of synthesizing them bottom-up using the Vapor-Liquid-Solid (VLS) technique and top-down using the Bosch process will be discussed here in detail. All other methods are used for growing nanowires of other materials, which although very important from a material viewpoint, are not directly related to the purpose of our research.

2.6.1 VLS Technique

The VLS method was first described by Wagner and Ellis from Bell Laboratories Inc. in 1964 (Wagner & Ellis, 1964) when they demonstrated that vertical single-crystal Si whiskers could be grown on a (111) Si substrate using SiI_2 and $SiCl_4$ as source gases. The diameter of these whiskers varies from a few hundred nanometers to a few hundred microns. A schematic representation of the growth of a whisker is shown in *Figure 1*.

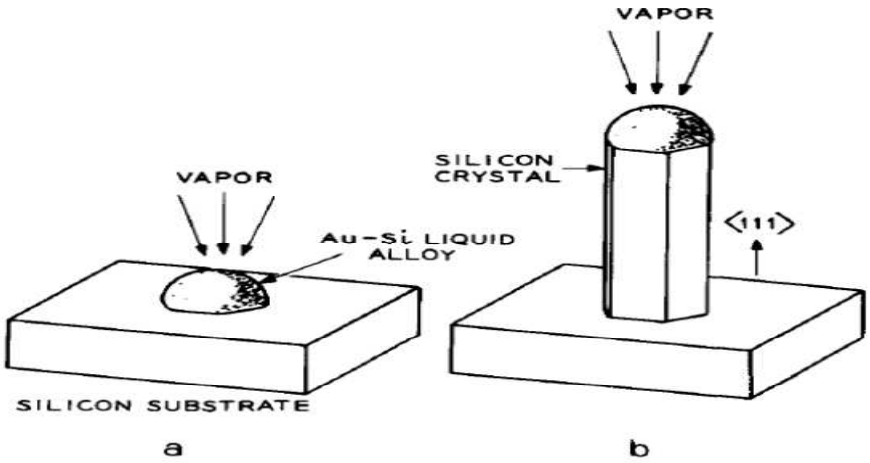


Figure 1. **(a) Impurity droplet on the Si surface; (b) Growth of a single crystal whisker with the impurity droplet at the tip. (Reproduced from (Wagner & Ellis, 1964)).**

A few decades later, it was found that the same basic technique, with a thinner coating of the impurity produced whiskers of nanoscale diameters which came to be known as nanowires (Ozaki et al., 1998; Westwater et al., 1995; Westwater et al., 1997). The role of the impurity (in this case, Au) is very important as it causes preferential reaction of the gaseous source species on the substrate and causes anisotropic growth in the form of whiskers. First, the substrate is heated to a temperature at which the impurity melts and forms a molten alloy cluster with the substrate. Then the gas containing the source species in vapor phase is introduced which reacts preferentially with the melted cluster as compared to the rest of the substrate and forms a supersaturated solution of the source material into the molten alloy. Eventually, this leads to precipitation of the growth species at the molten cluster-substrate interface in the form of a single crystal. As the reaction proceeds, the molten cluster sits on the tip of the whisker leading to a 1-D growth.

For impurities like Au whose solubility in the molten cluster is high, the diameter of the nanowire is limited by the size of the impurity cluster (Meyyappan & Sunkara, 2010). In this work, the growth of nanowires has been achieved using Au as the impurity on top of (111) Si substrates. The diameter of the Au cluster is critical to the diameter of the resulting nanowire.

2.6.2 Dynamics of the VLS Technique

In order to understand how the source gas transfers the nanowire material anisotropically, we need to split the technique into its constituent phenomena and consider them separately as a single crystal on the substrate. The processes occurring during VLS nanowire growth using the VLS technique can be broadly classified into the following (Meyyappan & Sunkara, 2010):

a) Selective absorption of source gases at the vapor-liquid interface

b) Adatom diffusion from the substrate to the liquid-solid interface

c) Precipitation at the liquid-solid interface

Apart from the above processes there are some thermodynamic principles which govern the formation and growth of nanowires under the liquid droplets of their molten impurities. It is possible that multiple nanowires might grow out of a single molten impurity cluster. It is therefore necessary to choose the right combination of impurity and source gas for growing individual nanowires and controlling their diameters. It has been experimentally determined that the growth kinetics and surface structure depends mainly on the rate of absorption of the vapor phase into the liquid and also on the rate of diffusion of adatoms along the surface of the nanowire towards the liquid-solid interface. Some impurities increase the dissociative adsorption of the source gases on the surface of the liquid droplet, which in turn, increases the rate of dissolution of the source atoms into the liquid. The following discussion provides an introduction to the concepts which help decide what materials and conditions one must choose in order to grow nanowires in a controlled manner using the VLS growth technique.

2.6.3 Nanowire growth initiation

First we discuss the initiation of nanowire growth. The catalyst which promotes nanowire growth in the VLS technique is a metal. This metal melts and forms a eutectic with the Si substrate at the growth temperature. The source material of the nanowire is introduced in gaseous form into the system. As the gas comes into contact with the molten metal cluster, it is absorbed into the liquid and reacts to give the source material in elemental form. At this point, the source material can either diffuse through the liquid to reach the substrate and form a single crystal nanowire whose characteristics are well-controlled, or it can form multiple nucleation sites on the surface of the liquid droplet giving rise to a bunch of nanowires whose

growth direction cannot be controlled. What actually happens depends upon the combination of metal and source material. In order to understand the thermodynamic concepts underlying growth, we start with the formation of a droplet of molten metal on the substrate.

Using the Gibbs-Thompson equation, the partial pressure of a gas in equilibrium with a liquid droplet of radius (r) is given as (Meyyappan & Sunkara, 2010)

$$kTln\left[\frac{p}{p^{\infty}}\right] = \frac{2\gamma\Omega}{r} \tag{2.1}$$

Where, γ is the surface energy of the droplet, Ω is the molar volume of the species within the droplet, p is the partial pressure of the gas in equilibrium with the droplet, p^{∞} is the partial pressure of the gas in equilibrium with a planar surface (radius = ∞), k is the Boltzmann constant and T is the absolute temperature. The ratio p/p^{∞} signifies the degree of vapor-phase supersaturation of the source material in the gas phase. Equation (2.1) shows the need for supersaturation of the solute species in the vapor phase in order to form a liquid droplet. The radius of one such droplet is given as

$$r = \frac{2\gamma\Omega}{kTln\left[\frac{p}{p^{\infty}}\right]} \tag{2.2}$$

The above expression gives the radius of a droplet in liquid phase in equilibrium with the vapor phase of any solute species. Considering the possibility of nanowire growth via multiple nucleation sites on the surface of a droplet of molten metal, the concept of minimization of Gibbs free energy gives the radius of a nucleation site for which there is the maximum possible decrease in free energy. The critical radius is generally (Meyyappan & Sunkara, 2010):

$$r_C = \frac{-2\sigma}{\Delta G_V} \tag{2.3}$$

Where, σ is the interfacial energy between the molten metal droplet and the nucleation site and ΔG_V is the volume free energy given by (Meyyappan & Sunkara, 2010):

$$\Delta G_V = \frac{kT}{\Omega} ln\left(\frac{C}{C^*}\right) \tag{2.4}$$

Where, C represents the solute concentration within the molten metal cluster and C^* is the equilibrium concentration of the solute species in the molten metal which can be obtained as a function of temperature

from the liquidus line in the binary phase diagram. Therefore, the radius of the nucleation site formed on the surface of the molten metal cluster is

$$r_C = \frac{2\sigma\Omega}{kT \ln\left(\frac{C}{C^*}\right)} \tag{2.5}$$

The above equation tells us that at a certain concentration of the solute species in the molten metal cluster, the minimum radius of a nucleation site formed on the surface of the metal droplet is given by the term r_c. This has an important role to play in choosing the combination of catalyst metal and the material of the nanowire. Consider the example of an Au-Si eutectic at approximately 650K in which the atomic % of Si is close to 19%. At this concentration and temperature, the minimum radius of a nucleation site is of the order of several microns. Thus, if we have Au clusters of sub-micrometer dimensions, there will not be any nucleation site on the surface of the molten Au-Si eutectic. Instead, the Si will diffuse through the liquid and form a single crystal nanowire at the liquid-solid interface. On the other hand if we have a different metal like Ga, the solubility of Si in liquid phase of Ga is much less as compared to that in Au. So, at 1000K with a Si concentration of say 3 atomic %, the minimum radius of a nucleation site can be approximately 10 nm. This means that if we have a sub-micrometer sized cluster of Ga on the substrate and we expose it to a vapor phase containing Si, multiple nucleation sites may develop on the surface of a single liquid Ga eutectic phase giving rise to a bunch of disordered nanowires. Thus, we have to choose a suitable catalyst metal by looking at the binary phase diagram of that metal with the growth species dissolved in it as shown in *Figure 2*.

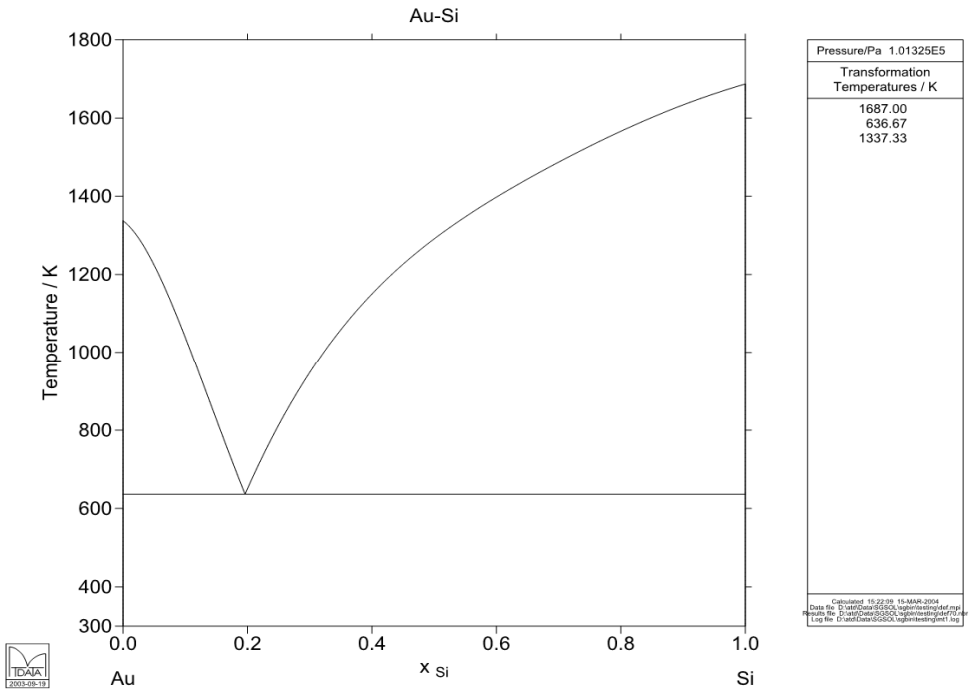


Figure 2. **Phase diagram of the Au-Si system.**
(Reproduced from http://mtdatasoftware.tech.officelive.com/phdiagrams/ausi.htm)

For the VLS process we hold the temperature at 363 C which is the eutectic temperature for Au-Si system. At this temperature the atomic % of Si in the melt is approximately 19%. From this state, a single crystal of Si starts forming by saturating the eutectic with Si atoms obtained by the decomposition of silane. The Au-Si phase diagram in *Figure 2* shows that if the system is held at 363 C or 636K (the eutectic temperature) and the concentration of Si in the eutectic is increased, Si in solid form will segregate from the solution and the Au will be retained in liquid form without being consumed. The creation of multiple nucleation sites on the surface of the eutectic melt is prevented by the size of the Au-Si droplet and the concentration of Si in the supersaturated melt. In this case, the 19% atomic concentration of Si ensures that the minimum size of a nucleation site is of the order of a few microns. In the present work, we have taken care to pattern our substrates with Au particles of sub-micrometer dimensions thereby ensuring that tip-led growth of a single nanowire will occur from each Au cluster on the substrate.

It is a standard approach to check the phase diagram of a system to find a eutectic point where concentration of the growth species inside the melt is such that the creation of multiple nucleation sites is impossible and by saturating the melt at constant temperature, catalytic growth of nanowires can be obtained. A good example is the formation of Ga and In nanowires using Sb as catalyst metal (Meyyappan & Sunkara, 2010).

2.6.4 Effect of the liquid-solid interface on nanowire growth stability

The shape of the catalyst metal droplet is the result of the balance of forces resulting from interface tensions present at the liquid-solid interface of the nanowire. It has been observed that nanowires grown using the VLS technique can have different shapes depending on the combination of the metal and the growth species. This difference is because the metal droplet controls the interfacial energy at the liquid-nanowire interface (Nebol'sin & Shchetinin, 2003). Different metals form alloys having different compositions with the source material at the eutectic temperature. These molten alloys have interface tensions different from the pure metal and hence a fair amount of experimentation is required to determine the suitable catalyst-nanowire combination for a certain application.

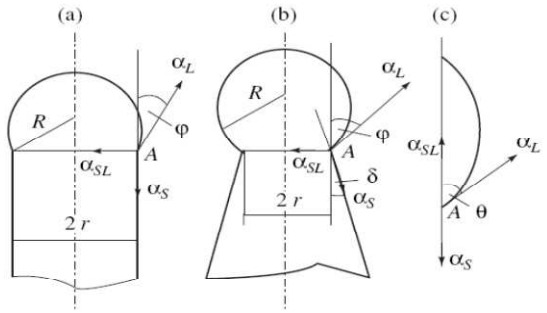


Figure 3. **Nanowire geometry and balance of surface tension in case of (a) Cylindrical wire, (b) Conical wire and (c) droplet wetting the lateral face of the nanowire. (Reproduced from (Nebol'sin & Shchetinin, 2003))**

The shape of the nanowire surface is determined by the minimization of Gibbs free energy, and for growth in a particular direction it is necessary for the droplet to cover the surface. There is a range of angles, φ shown in *Figure 3*, for which the growth of the nanowire is thermodynamically possible (Meyyappan & Sunkara, 2010)

$$\frac{\alpha_S}{\alpha_L} < \frac{\sin\varphi + \cos\varphi}{\cos\delta - \sin\delta}, \tag{2.6}$$

Where, α_S and α_L are the solid-vapor and liquid-vapor interface tensions respectively and δ is the conical angle of the nanowire. For understanding the condition of stable growth of the nanowire, the plot shown in *Figure 4* is helpful. It shows two cases: (1) is when the shape of the nanowire is cylindrical and (2) is when it is a cone inclined at an angle of δ from the vertical. In case (1) and case (2) the areas under the curve bounded by (sin φ + cos φ) / (cos δ-sin δ) = 1.33 are the ranges of δ for stable nanowire growth in the case of cylindrical and conical nanowires respectively. These areas fall under the region numbered II on the plot. In regions I and III on the plot, nanowire growth is not possible. One can easily infer that the range of δ for stable growth is more for conical than for cylindrical nanowires. That is why the formation of conical nanowires is more favorable than cylindrical ones. Also, equation (2.6) implies that stable growth is more likely if α_L is larger compared to α_S. Hence, proper choice of the metal-nanowire source material combination is extremely necessary for obtaining a desired shape of nanowires.

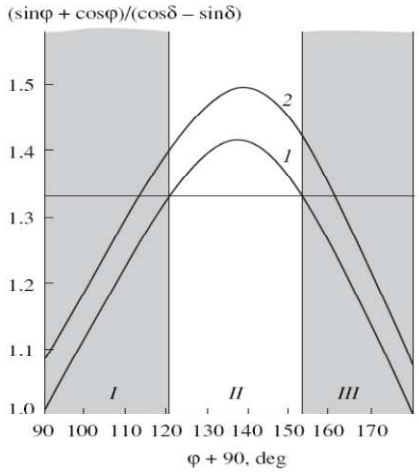


Figure 4. **Plot of (sin φ + cos φ) / (cos δ-sin δ) versus the angle of contact (φ) of the metal droplet with the nanowire surface. (Reproduced from (Nebol'sin & Shchetinin, 2003))**

2.6.5 Imperfections observed in nanowire structures

Sometimes, spiral geometries have also been reported in literature (McIlroy et al., 2004). It is believed that asymmetry in the contact angle of the metal droplet to the nanowire surface leads to differences in the rate of growth of material across the diameter of the wire. The system grows in the

direction which supports minimum interfacial energy and a periodic asymmetry results which forms a spiral because of the height of the wire.

Another observation in Si nanowires growing in the <111> direction is that their lateral surfaces have a "sawtooth" faceting on them. This faceting has been explained based on the Gibbs theorem of minimization of free energy (Meyyappan & Sunkara, 2010):

$$Free\ energy = \Sigma\sigma_i\alpha_i = minimum \tag{2.7}$$

In this expression, σ_i is the surface energy of a facet and α_i is its area. The surface energy of a facet to is related to its distance (h) from the crystal center as (Meyyappan & Sunkara, 2010)

$$\frac{\sigma_a}{h_a} = \frac{\sigma_b}{h_b} = \frac{\sigma_c}{h_c} \tag{2.8}$$

Sunkara (Sunkara, 1993) proposed an explanation of this phenomenon applying the above theorem in a Kinetic Monte Carlo simulation for creating a 3-D octahedral crystal of diamond. They conclude that the rate of growth of the nanowire also has a role to play in determining the growth direction. The formation of crystal facets was preferentially <111> because of lower surface energy than other orientations. However, due to interactions with the second and third nearest neighbors in a crystal, the <111> surface develops kinks and steps which roughens up the surface and increases its energy above that of other orientations. This results in a change in growth direction towards other orientations which have lower surface energy.

Gösele et. al. (Schmidt, Senz, & Gösele, 2005) reported that Si nanowires with diameters larger than 20 nm grew in the <111> directions but, for smaller nanowires, <110> growth was possible. They proposed a model which states that the minimization of free energy of the surface of the nanowire determines the growth direction and the free energy is a function of the nanowire diameter. The expression for the free energy is

$$Free\ energy = \Delta z\sigma_s L + \sigma_{ls} A, \tag{2.9}$$

Where, Δz is the interfacial thickness on the Si surface, σ_S is the surface energy of the Si, L is the circumference of the interface, σ_{LS} is the liquid-solid interface tension and A is the area of the interface. As the diameter of the nanowire changes, it changes the contributions from the solid-liquid interfacial tension and the Si surface tension from the edge of the interface, towards the free energy of the nanowire surface.

This explanation suggests that the nanowire growth direction changes with its diameter because of the free energy of the interface. The only weakness in the previous argument is the question whether it can be applied to the growth of a nanowire where the surface is actually a liquid-solid interface and whose dimensions are a few nanometers.

2.6.6 Vertical etching

The outcome of the VLS growth is strongly dependent on the material of the nanowire and also the surface chemistry between the catalyst and the substrate. A more straightforward approach is to use reactive ion etching to vertically etch nanowires using the Bosch process. This approach is simpler as it does not involve a catalyst. There is no question about non-uniform doping as one can use a uniformly doped substrate. The only requirement for this process is having particles on the substrate which act as hard masks to etch down the nanowires. The interface between the hard mask and the substrate does not have to be atomically clean; all that matters is the position of the hard mask making the process robust to the cleanliness of the substrate. The other main advantage of vertical etching is low temperature processing. The only annealing that has to be performed is to form a silicide or germanide of the metal at the tips of the nanowires after contacts are fabricated. This makes the process fit for integration into a pre-established flow without worrying about the effects of high temperature on doping profiles of other devices.

2.7 Nanowire diodes: prior research

Considerable research has been reported on methods of fabrication and understanding of the electrical behavior of nanowire diodes. In most studies, nanowires have been dispersed horizontally on a dielectric (SiO_2), and electrodes have been lithographically deposited on top. Since this work concerns fabrication of vertically oriented nanowire diodes, we review below, some of the work which has been directed towards this cause.

ZnO nanowires (n-type) on p-GaN films deposited on Al_2O_3 substrates have been reported (Lai et al., 2008). GaN films were grown using MOCVD up to 1 µm in thickness and doped with Mg to yield hole concentration of ~ 4.5 x 10^{17} cm^{-3}. Solution growth method was used to grow ZnO nanowires on the film. The substrate was suspended in an aqueous solution of a Zn salt for a specific amount of time which governed the length of the ZnO nanowires. This yielded 100-600 nm thick vertical ZnO nanowires. The

nanowires were then spin-coated with PMMA for electrical insulation between the substrate and top electrical contacts made of Ti/Au deposited by thermal evaporation. *Figure 5* shows the results of this study.

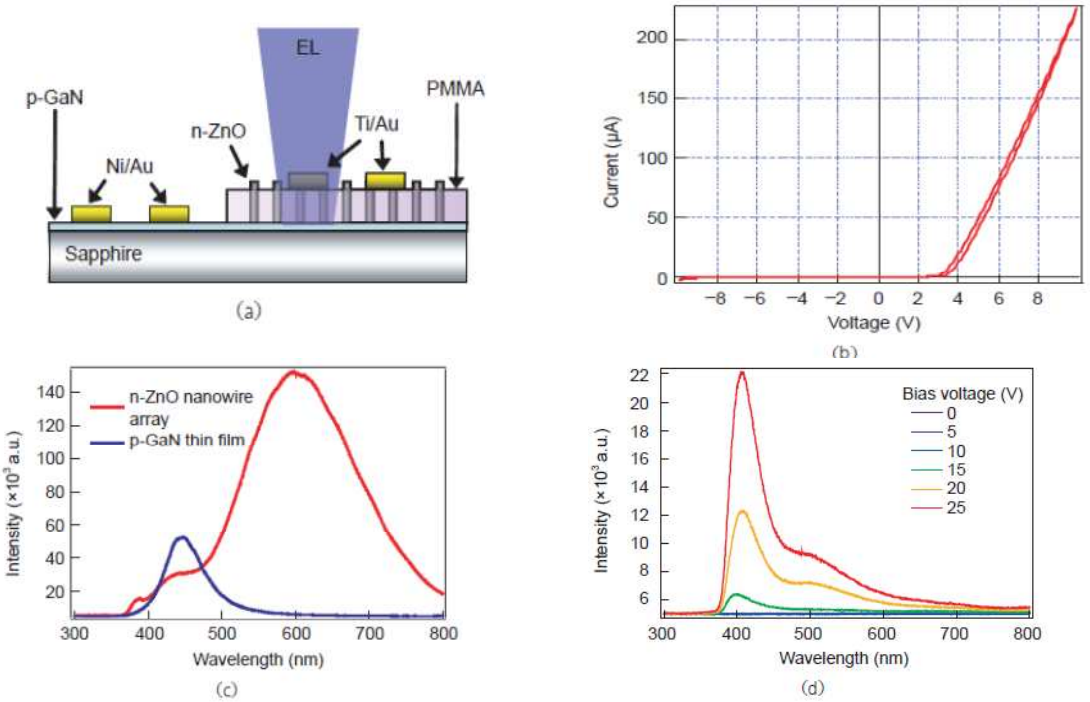


Figure 5. **(a) Schematic of the device cross-section , (b) I-V characteristics, (c) Photoluminescence spectra and (d) Electrluminescence spectra of ZnO-GaN nanowire LEDs (Lai et al., 2008).**

In another study, Schottky and Ohmic contacts were fabricated on to a single GaN nanowire laid horizontally on thermally grown SiO_2 on a Si substrate. Ti/Au and Al were deposited using thermal evaporation to form Ohmic and Schottky contacts respectively (Kim et al., 2002). Although rectifying behavior was observed with the Al contacts, the fit with the thermionic emission model was poor yielding an ideality factor of 17.8 which the authors justify by hypothesizing the formation of AlN at the interface of the GaN with Al.

Ti has been reported to have been used as a catalyst in growing Si nanowires on Si substrates. In this study by Tang et al. (Tang et al., 2005), Si nanowires were grown by MBE using Si_2H_6 as the precursor and Arsenic and Boron from effusion cells as dopant gases. A layer of SiO_2 was thermally grown on the Si substrate and a patterned with 1.5 μm diameter opening using optical lithography. Then the SiO_2 was selectively etched through those openings in the photoresist, and the wafer was loaded in an MBE chamber.

Ti was deposited and the wafer was annealed to form islands of $TiSi_x$, which acted as nucleation sites for Si nanowires on introduction of the precursors. After growing the nanowires, they were encapsulated in SiO_2 using CVD and mechanically polished to reveal the tips of the nanowires which were ~ 300 nm in length after polishing. Top electrodes were fabricated by patterning and depositing 300 nm Ti covered with 30 nm Au. The I-V characteristics of p-n junction formed within nanowires and between nanowire and substrate in case of an n-type nanowire on a p-type substrate are shown in *Figure 6*.

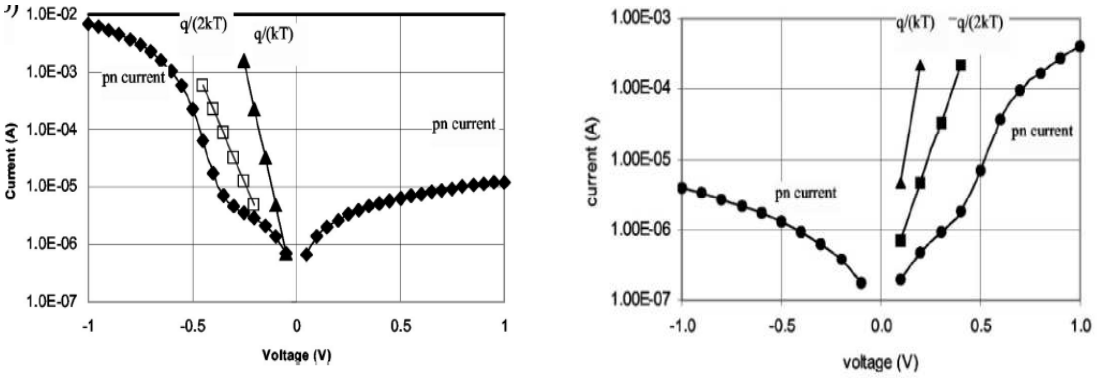


Figure 6. **I-V characteristics reported for (left) p-n junction made between the nanowire and the substrate and (right), p-n junction within the nanowire (Tang et al., 2005).**

Using a gate to control the conductivity of vertically grown p-type Si nanowires on p-type (111) Si substrates has also been reported (Goldberger et al., 2006). In this case the gate dielectric was thermally grown oxide which can be used to control the thickness of the channel as it consumes the nanowire material to grow. The channel length is along the nanowire and can be controlled by the thickness of the metal deposited on the thermally grown gate oxide to act the gate electrode. A schematic of the structure and modulation of the conductivity of the nanowire by application of a gate voltage are shown in *Figure 7*.

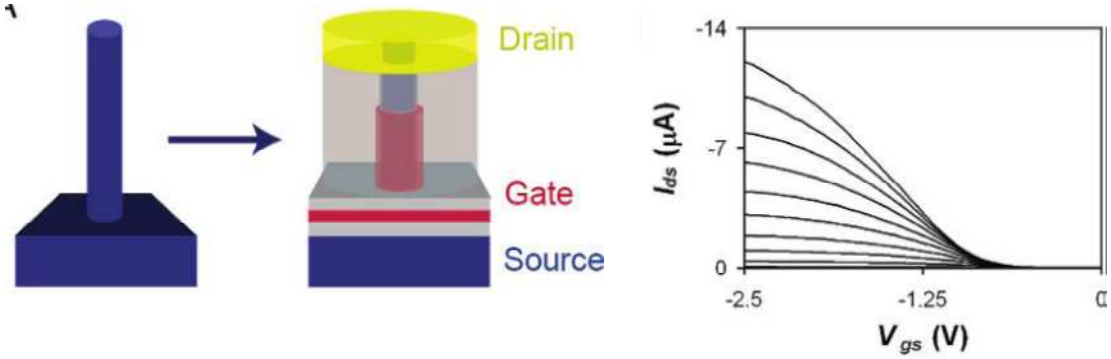


Figure 7. **Vertical nanowire FET schematic (left) and I-V characteristics (right) (Goldberger et al., 2006).**

Tunnel (Esaki) diodes have also been reported by growing n-type Si nanowires on degenerately doped p-type Si substrates (Schmid et al., 2012). Since it is difficult to get heavy p-type doping inside a Si nanowire during VLS process due to solid solubility limit of Boron at the growth temperature, the authors grew n-type (P doped) nanowires doped ~ 10^{19} cm^{-3}. The p-n junction was reported to be at the base of the nanowire. Ti/Au contacts were made to the top of the nanowire and negative differential resistance behavior was observed as shown below.

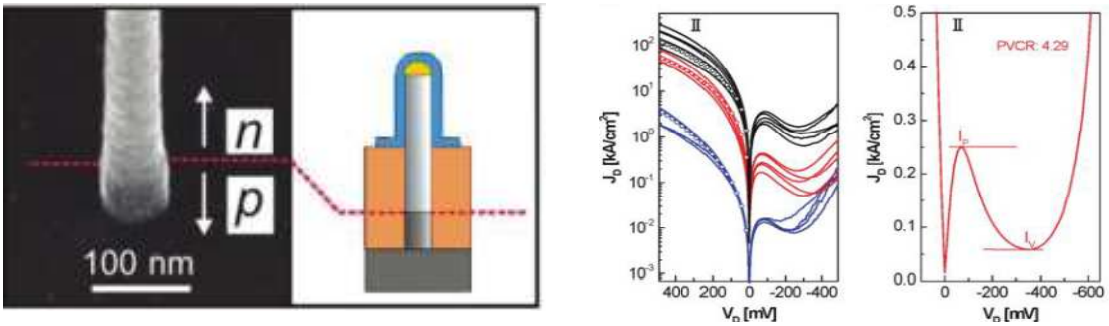


Figure 8. **Si nanowire Esaki diodes. (Left) Schematic of the device structure and (right) I-V characteristics showing negative differential resistance (Schmid et al., 2012).**

Another investigation into vertical Si p-n junction nanowire diodes on Si substrates has been reported by Jackson et al. (Jackson et al., 2007). SiO_2 was thermally grown on a Si substrate and openings having diameters from 750 nm to 2.25μm were opened up using optical lithography and selective HF etching. Au catalyst particles were then, deposited through the openings in SiO_2 and nanowires were grown using atmospheric CVD at 900 C in a H_2 + $SiCl_4$ ambient. Once grown, the nanowires were encapsulated in spin-on-glass up to a length of ~ 700 nm. Top contacts to the nanowire tips and a bottom contact to the back of the Si substrate were fabricated by depositing Al. The nanowires were not doped at all during

growth and the substrate was n-type doped to have a resistivity of 4 Ωcm. VLS grown nanowires develop p-type nature electrically when not doped intentionally. The exact cause of this is currently an open discussion but it is believed to be due to diffusion of Au into the nanowire from the tip. Au acts as a mid-level acceptor trap giving rise to a p-type behavior. The structure of the device and its I-V characteristics are shown in *Figure 9*.

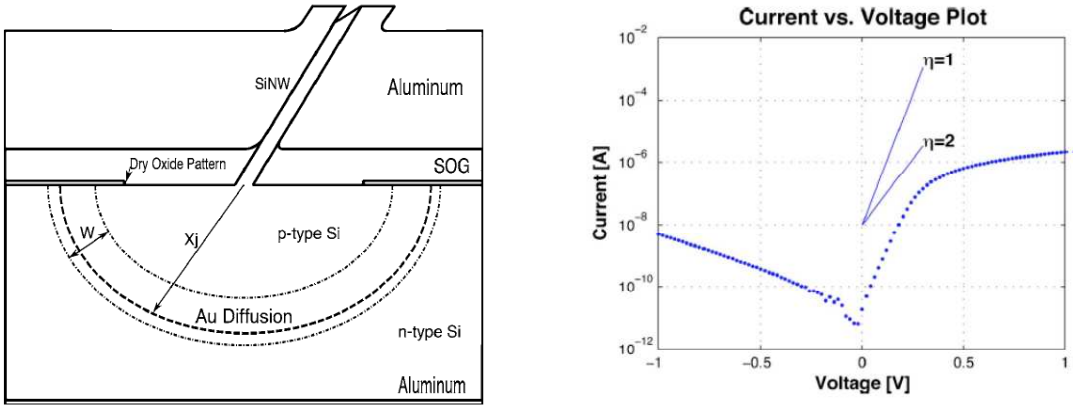


Figure 9. **(Left) Schematic of the p-n junction diode between the p-type nanowire and the n-type Si substrate and (right), I-V characteristics of the nanowire diodes (Jackson et al., 2007).**

The p-type doping concentration of the nanowire inferred from series resistance is ~ 3 x 10^{17} to 10^{18} cm^{-3}. The ideality factor of these diodes was between 1.5 and 2 which indicates that both space-charge region and quasi-neutral region recombination are at work. Further, the reverse bias leakage current is greater than what one would expect to leak from an area equivalent to the cross-section of the nanowire itself. The authors hypothesize that the leakage current can be explained if a hemispherical depletion region of diameter ~ 20 to 50 µm is assumed which would be the case if the Au from the catalyst particles diffused into the Si substrate when the nanowires nucleated during growth.

Now we briefly review some current research that has been published on Ge Schottky diodes. Fermi level pinning is a well-known phenomenon in the case of the interface of a metal with Ge. Due to this phenomenon the Schottky barrier height becomes independent of the work function of the metal and stays around 0.5 eV. The Fermi level is pinned at ~ 0.18 eV above the valence band in Ge. Thus, all metal contacts to n-type Ge are rectifying and those with p-type Ge are Ohmic independent of the work function of the metal. There have been studies for investigating the de-pinning of the Fermi level by modification of the Ge surface. Sulfur atoms implanted at the Ge surface can alleviate the Fermi level pinning at Ni/Ge

interfaces (Ikeda et al., 2006). In this study, Ni contacts were fabricated on top of Ge implanted with different doses of S and NiGe was formed by annealing the Schottky contacts. The barrier height decreased from 0.61 to 0.15eV at a dose of 10^{15} cm^{-2} of the S ions implanted at an accelerating voltage of 10 keV. Zhou et al. (Zhou et al., 2010) have tried to explain the cause of this effect. The motivation for this study was the uncertainty between the presence of defects at the Ge surface or metal-induced interface states as the cause of Fermi level pinning. A metal/MgO/n-Ge structure was fabricated with 0.5-3 nm thick MgO layer. Sulfur implanted Ge Schottky diode were also prepared in this study. It was found that the barrier height did not depend on the thickness of the MgO layer but was strongly affected by the presence of a Sulfur passivation layer on the Ge. Thus, their conclusion was that the Fermi level pinning was mainly due to defects on the Ge surface and not because of interface states induced by the metal.

Fermi level de-pinning at the Ni/Ge interface on n-type Ge wafers using laser annealing has been demonstrated by Lim et al. (Lim et al., 2012). They have shown that with laser pulses with a fluence of 300 mJ cm^{-2} can raise the temperature of the Ni/Ge interface to ~ 600 C forming $NiGe_2$ which shows an effective barrier height of 0.37 eV compared to that of 0.6 eV shown by NiGe contacts annealed at 350 C using RTA. The authors explain this reduction in barrier height as Fermi level de-pinning caused by satisfying more dangling bonds by the formation of $NiGe_2$ at the interface. Chemically altering the Ge surface using hydrazine has also been reported to increase the effective Schottky barrier height on a Ti/p-type Ge junction by Jung et al. (Jung, Jung, & Park, 2013). They have demonstrated that hydrazine first reduces the native oxide of Ge within ~ 10 min and then forms GeO_xN_y which satisfies the dangling bonds at the Ge surface and un-pins the Fermi level making the p-type Ge behave increasing the effective barrier height for holes. The authors have performed XPS and AFM analyses to prove that there is a GeO_xN_y phase present on the surface and the native oxide is completely removed by hydrazine.

In yet another interesting study (Koleśnik-Gray et al., 2013), Fermi level de-pinning has been demonstrated on side-contacted Ge nanowires with Ag, Pd, Au and Pt. Metal contacts were fabricated on Ge nanowires laid horizontally on a SiO_2 substrate and it was ensured that there was no native oxide between the metal and the nanowire. The nanowires were doped 10^{14} cm^{-3} to 10^{18} cm^{-3} n-type. Contact resistivity measurements showed that the Ag behaved as Ohmic and the Pt, Pd and Au behaved as Schottky

contacts. The effective barrier heights from Au, Pd and Pt contacts were 0.4, 0.5 and 0.6 eV respectively. This showed that the Fermi level was not pinned in case of these nanowires contacted from the side.

The effect of annealing conditions on the Schottky barrier heights of Ti, Pt and Ni contacts formed on n-type Ge have been reported in literature (Chawanda et al., 2010). It was found that the barrier height in case of Ni contacts remained almost constant under annealing temperatures of 100 C to 500 C whereas, in case of Ti it changed from 0.56 eV to 0.5 eV when annealed at 100 C and 300 C respectively. For Pt contacts the barrier height decreased from 0.58 eV to 0.56 eV when annealed at 100 C and 500 C respectively. The ideality factor in the range of annealing temperatures from 100 C to 500 C remained almost constant at 1.0 in case of Pt and stayed in the range of 1.3 to 1.45 in case of Ni but increased from 1.3 to 3.0 in case of Ti. The authors have concluded that in case of Ni and Ti an increase in temperature causes deviation from ideal thermionic emission even though the overall behavior remains rectifying.

Photodetectors have been demonstrated using monolayer graphene (MLG) on Ge (Zeng et al., 2013). An increase in reverse bias current by almost 4 orders of magnitude was reported when a MLG-Ge diode is illuminated with IR light of wavelength 1200 to 1600 nm with the sensitivity being the maximum at 1400 nm. This device works by emission of photo-generated electrons and holes over the potential barrier at the MLG/Ge interface. The barrier height calculated from reverse bias current in the dark was 0.45 eV. The photodetector had a rise time of 23 µs after the light was switched on, to reach the peak current under illumination. It took 108 µs after light was switched off for the excess carriers to recombine and the reverse current to return to its value in the dark.

2.8 Pros and cons of fabricating 3-D Schottky diodes

At this point it is worthwhile to discuss some of the pros and cons of 3D fabrication of Schottky diodes over a planar architecture. First of all, 3-D integration helps in scaling as nanowires have a diameter of tens of nanometers. Vertical diodes can provide connections between devices on different layers of circuitry preventing the need for metallic via fabrication and consumption of a large area, just for diodes on a single layer. Diodes are switching units which can be used as means of addressing memory cells. 3-D diodes can dramatically reduce the area of memory circuits. Another very useful application of vertical diodes is in photodetectors and solar cells. Currently, planar solar cells are textured to absorb more light but

it has already been shown that nanowires can increase the absorption up to 100% for a broad range of the visible spectrum in regular arrays for particular aspect ratios and pitch. Another advantage in using nanowires for solar cells is using coaxial p-i-n junction diodes with the junctions along the radius. This not only provides a very small diffusion path for photon-generated carriers, but also a large short circuit current because of the area exposed to solar radiation. Nanowires can also be formed by combining lattice-mismatched materials because of better strain relaxation. The crystal is confined only in the vertical direction, making it easier for it to deform laterally and accommodate the strain.

The 3-D integration of nanowire devices however, does not come without limitations. The main problem is the creation of models to understand the electrical behavior of 3-D devices. Most of the etching processes have to be limited to dry etching because of stiction-related issues with wet etching. In case of VLS growth, Au as a catalyst is a cause of contamination, especially for Si substrates in which it diffuses very fast and creates mid-gap traps. Surface treatment of vertical devices plays a major role in modifying the electrical characteristics and is still under investigation. Encapsulation of vertical devices in a dielectric is also an issue because a large thickness is required and minimal trapped charges are desirable. Chemical vapor deposition usually has a trade-off between deposition rate and the quality (uniformity, trapped charge density) of material being deposited. The higher the rate, the lower is the quality. This places a direct trade-off between throughput and performance in a mass-production environment.

CHAPTER 3

THEORETICAL MODELING OF NANOWIRE DIODES

3.1 Introduction

The purpose of this chapter is to provide a theoretical background to the working of p-n junction and Schottky diodes. Simulations in Atlas have been used to show the mechanism and the main factors affecting the conduction of current in these diodes. Later in this study, the current measured from actual nanowire arrays is presented. The theory presented in this chapter should provide the background for the extraction of parameters and creation of approximate models for explaining the characteristics observed from real diodes.

3.2 P-n junction and Schottky diodes

This research focuses on two types of diodes: Schottky and p-n junction. At this point it is worthwhile to review the working principle of these diodes. Let us start with the p-n junction diode. A planar p-n junction diode is composed of two oppositely doped regions whose absolute doping concentrations can be equal or different based on the application. When the p-type and n-type regions come into contact, the majority carriers for both sides diffuse into the regions of opposite doping and recombine near the metallurgical junction. This exposes positive dopant ions in the n-type region and negative acceptor ions in the p-type region setting up an electric field from the n-type to the p-type region which opposes and eventually stops further diffusion of majority carriers. The region around the metallurgical junction which is devoid of free carriers due to recombination is known as the space-charge or depletion region. The electric field due to the fixed donor and acceptor ions eventually stops the diffusion of free electrons and holes and fixes the width of the space-charge region. The portion outside of the space-charge region is known as the quasi-neutral region because there electric field there, is zero under equilibrium. The internal electric field at the metallurgical junction sets up a potential barrier for electrons to cross from the n-type region into the p-type and vice-versa.

The energy band diagram of a p-n junction diode at zero bias (left) shows the potential barrier that exists preventing the diffusion of electrons from the n-type region on the right to the p-type region on the

left and vice-versa for holes. The image on the right shows how the potential barrier is lowered by applying a forward bias (positive voltage to the p-type side of the diode) of 0.7V.

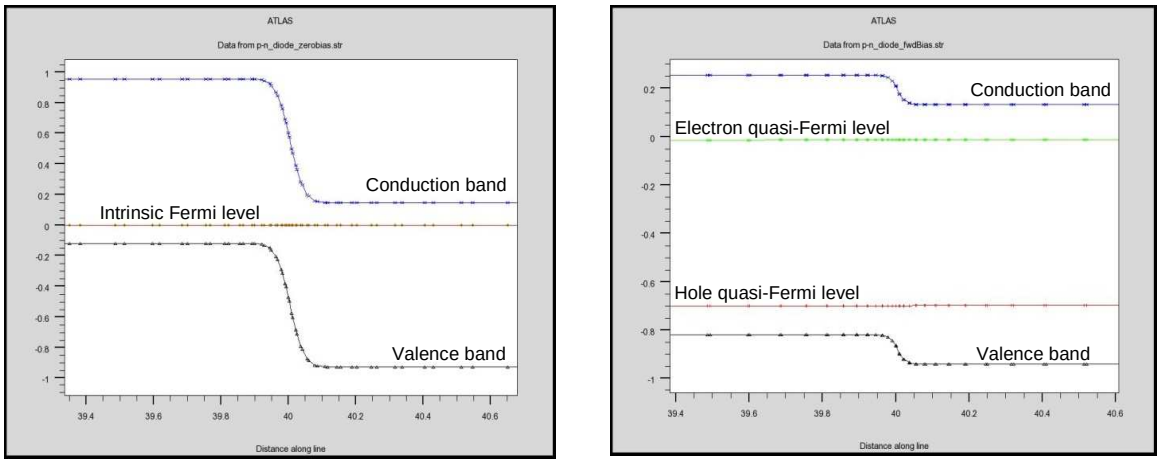


Figure 10. **Energy band diagram of a p-n junction diode during zero bias (left) and forward bias of 0.7 V (right).**

The left part of *Figure 10* represents the energy bands inside a p-n junction diode in equilibrium. Application of external voltage changes the potential of the semiconductor and thus, shifts the intrinsic Fermi level down (positive bias) or up (negative bias) inside the quasi-neutral region. The conduction and valence bands inside the quasi-neutral region shift along with the intrinsic Fermi level and modulate the potential barrier inside the depletion region. Under forward bias, the Fermi level is moved down (or up) in energy inside the p-type (or n-type) regions such that the potential barrier at the metallurgical junction is lowered. Majority carriers cross over to the oppositely doped regions becoming minority carriers. The injection of electrons from the n-type region into the p-type region increases the electron concentration in the p-type region at the edge of the depletion region. They recombine with the holes inside the p-type side and form a gradient in concentration near the edges of the space-charge region. The same is true for holes being injected into the n-type region from the p-type region. The diode current is calculated by adding the diffusion currents due to minority carriers on both sides of the metallurgical junction inside the quasi-neutral region at the edges of the space-charge region. As the minority carriers recombine inside the quasi-neutral regions eventually, their concentration gradient and hence, the diffusion current reduces to zero. However, their recombination forces injection of majority carriers into the quasi-neutral regions from the contacts to maintain charge neutrality. Thus, an electric field is set up inside the quasi-neutral regions

where there are no excess minority carriers and the current is conducted by drift, instead of diffusion. So, in essence, the current near the edges of the space-charge region is totally due to diffusion and transitions into drift as we move away from the junction.

During reverse bias, the Fermi levels are moved away from each other such that the potential barrier becomes higher and the minority carrier concentration decreases at the edges of the space-charge region on both sides of the metallurgical junction. Once again, the total current is calculated by summing up the diffusion currents due to minority carriers at the edges of the space-charge region on both sides of the junction. *Figure 11* shows the energy band diagram and the electric field looking from the p-type into the n-type region of a p-n junction diode under reverse bias.

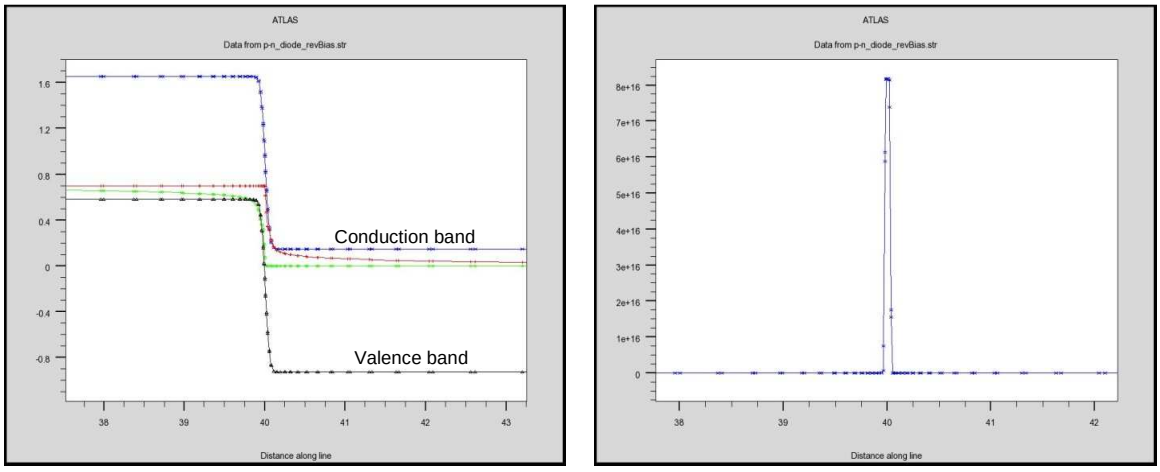


Figure 11. **(Left) Energy band diagram of a reverse biased p-n junction diode (0.7V reverse bias) and (Right) generation of charge carriers inside the depletion region at the junction during reverse bias.**

The mathematical model for current flow through a p-n junction diode is shown in equation (3.1) (Sah, Noyce, & Shockley, 1957):

$$J = qn_i{}^2\left(\frac{D_n}{L_nN_A}+\frac{D_p}{L_pN_D}\right)\left(e^{qV/kT}-1\right)+\frac{qn_iW}{\tau_{SCR}}\left(e^{qV/2kT}-1\right) \tag{3.1}$$

Where, J is the current density through the diode, n_i is the intrinsic carrier concentration, L_n and L_p are the electron and hole diffusion lengths, D_n and D_p are the diffusivities of electron and hole respectively, N_A and N_D are the doping concentrations on the p-type and n-type side respectively, V is the applied bias, k is Boltzmann constant, T is the absolute temperature, W is the width of the depletion region and τ_{SCR} is the minority carrier lifetime inside the space-charge region. The first term on the right hand side of the

equation represents current due to recombination in the quasi-neutral region and the second term represents current through the space-charge region.

The first term in the above expression represents the diffusion current due to the minority carriers at the edges of the depletion region on both sides of the junction. The second term accounts for recombination (or generation) of minority carriers inside the depletion or space-charge region during forward (or reverse) bias. It is important to note that the first term in the diode current expression accounts for current inside the quasi-neutral region. It has been derived assuming that there is no recombination or generation of charge carriers inside the depletion region. The justification for such an assumption is that the high electric field inside the depletion region due to fixed donor and acceptor ions pulls the minority carriers into the quasi-neutral regions in a time shorter than their recombination lifetime. This justification is reasonable for large forward bias and thin depletion regions (high doping) but breaks down in case of low forward bias and wide depletion regions (low doping). Low temperatures also undermine the validity of this assumption because the absolute concentration of minority carriers is reduced. At low temperature, the gradient of minority carriers at the edges of the depletion region is reduced bringing down the current due to recombination in the quasi-neutral region. Thus, any recombination within the space-charge region becomes significant. The opposite is true for high temperatures. So, there is a transition point in voltage on the $\log_{10}$(V) vs. V curve at which the slope of the graph changes abruptly. The current due to recombination in the space-charge region dominates before that point and after that the current is dominated by recombination in the quasi-neutral regions.

The exponential relation between current density and the applied voltage gives a linear relationship between $\log_{10}$(I) and V. The slope will be either *q/2.3kT or q/2x2.3kT* depending on whether the first (quasi-neutral region recombination) or the second term (space-charge region recombination) dominates. In order to better illustrate the current conduction in a p-n junction diode let us plot the results of the current density expression mentioned above. We assume the following typical values of the material properties for a Si p-n junction diode:

τ_{SCR} = 10 µs, $D_p = D_n$ = 10 cm^2/s, $W = 10^{-4}$ cm, $L_p = L_n = 10^{-2}$ cm, $N_D = N_A$ = 5 x 10^{16} cm^{-3}, n_i at 300K = 10^{10} cm^{-3}, k = 8.617 x 10^{-5} eV/K, T = 200K, 300K, 400K and 500K, cross-sectional area = 10^{-4} cm^2. *Figure 12*

plots the forward bias current for a p-n junction diode calculated using equation (3.1). A clear transition in slope from the second term to the first is observed at room temperature but the point of transition moves to lower bias with increasing temperature because the increase in absolute concentration of minority carriers also increases their gradient on the edges of the depletion region inside the quasi-neutral regions and makes the first term more significant. The slope also seems to become more gradual with increasing temperature because of the inverse dependence of the slope of the $\log_{10}(I)$ vs. V curve on temperature.

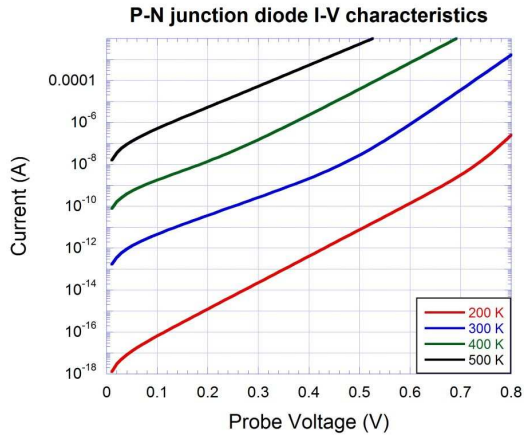


Figure 12. **Current vs. voltage behavior of a Si p-n junction diode during forward bias.**

The two regions with different slope on the $\log_{10}(I)$ vs. V plot with different ambient temperature indicate that the current due to recombination in the quasi-neutral region starts dominating at higher temperature whereas at lower temperature the current due to recombination in the space-charge region dominates. The reason for this calculation is to show that at room temperature recombination in the space charge region plays an important role in determining the current at low forward bias in a p-n junction diode.

Metal-semiconductor diodes, also known as Schottky diodes consist of a junction between a metal and a semiconductor. The difference in work function between the metal and the semiconductor gives rise to a potential barrier known as Schottky barrier and creates a depletion region inside the semiconductor. The magnitude of the Schottky barrier determines the reverse bias leakage current of the diode. Applying a voltage to the metal or the semiconductor moves the Fermi level such that the potential barrier looking from the semiconductor into the metal is modulated and the diode is forward biased when the barrier is low enough for conduction of current. Forward bias current is determined by the energy distribution of majority carriers inside the semiconductor at the interface with the metal. Similarly, the magnitude of the reverse

bias leakage current is determined by the energy distribution of electrons inside the metal at the interface and the height of the Schottky barrier. Since the concentration of electrons inside the metal is much higher than inside the semiconductor, Schottky diodes usually have higher reverse bias leakage current and a softer breakdown compared to p-n junction diodes.

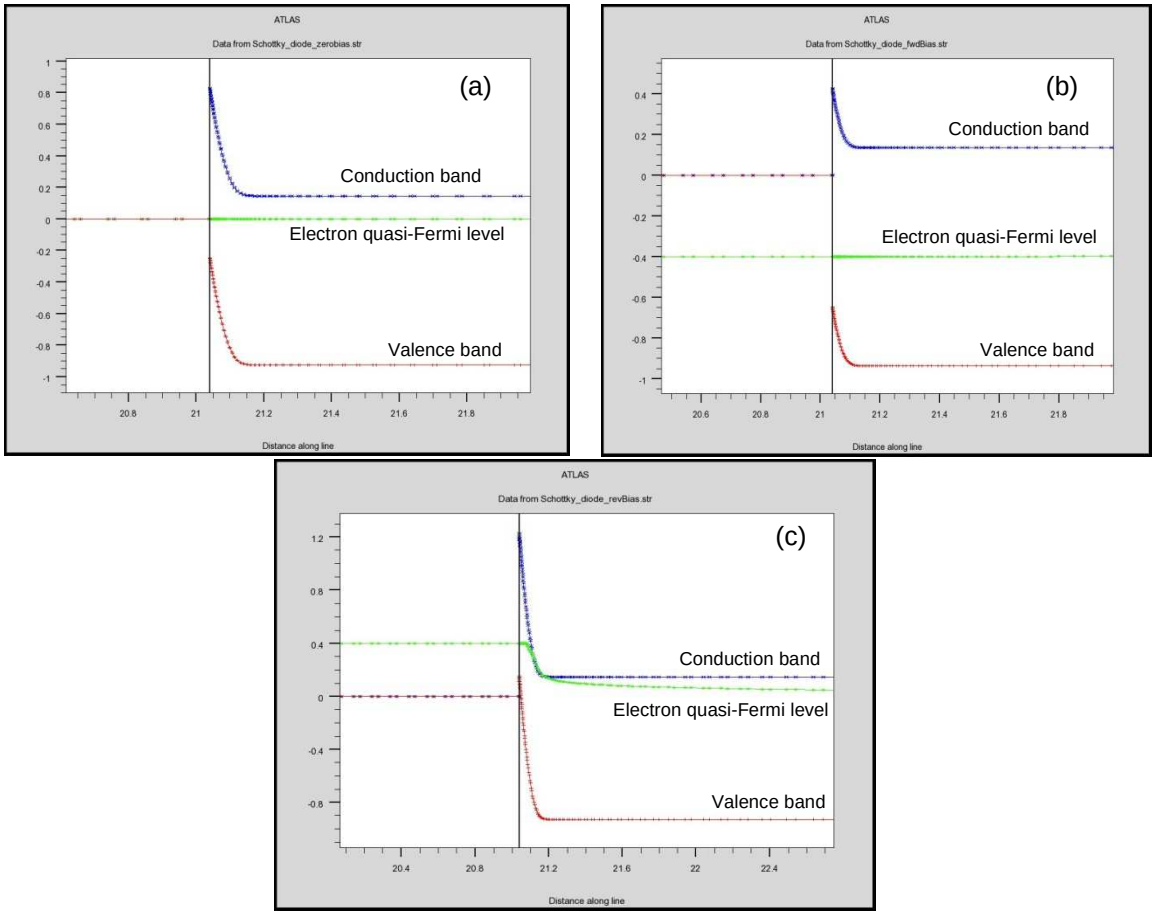


Figure 13. **Energy band diagram at the interface of a Schottky diode with different voltages at the metal contact. (a) 0 V, (b) 0.4 V forward bias and (c) 0.4 V reverse bias.**

Figure 13 shows the energy band diagrams of a Schottky barrier diode with a metal in contact with n-type Si doped to 10^{16} cm^{-3} at zero bias, forward and reverse bias. The structure of the diode is planar and the following diagrams have been plotted looking into the semiconductor from the metal. The simplest model to describe the current through a Schottky diode is the thermionic emission model. The main assumptions taken in deriving the current expression using this model are (a) the Schottky barrier height is much larger than *kT*, (b) there is thermal equilibrium at the metal-semiconductor interface and (b) the existence of a net current flow does not affect this equilibrium. The current expression is actually a

superposition of two current fluxes; one from the semiconductor into the metal and the other from the metal into the semiconductor. The mathematical expression for thermionic emission model is the following (Sze, 1981)

$$J = A^{*}T^{2}e^{-q\phi_B/kT}\left(e^{q(V-Ir_S)/nkT} - 1\right) \tag{3.2}$$

Where, A^* is the Richardson constant, T is the absolute temperature, k is the Boltzmann constant, ϕ_B is the Schottky barrier height, V is the applied bias, n is the ideality factor and r_S is the series resistance. For the purpose of understanding the working principle of a planar Schottky diode, we can neglect the series resistance. With this assumption the expression for current becomes

$$J = A^{*}T^{2}e^{-q\phi_B/kT}\left(e^{qV/nkT} - 1\right) \tag{3.3}$$

Taking natural log on both sides of the above expression we get

$$log_{10}(J) = log_{10}\left(A^{*}T^{2}e^{-q\phi_B/kT}\right) + \frac{qV}{2.303nkT} \tag{3.4}$$

The slope of the $\log_{10}$(J) vs. V curve gives the value of the ideality factor (n) and the y-intercept of the extrapolation of the linear part of the curve gives the value of Schottky barrier height (ϕ_B). The term $A^{*}T^{2}e^{-q\phi_B/kT}$ is the reverse saturation current of the diode. In reality, the series resistance reduces the slope of the $\log_{10}$(I) vs. V curve of the diode for large forward bias. It is interesting to note that in this simple thermionic emission model, the current does not depend directly on the doping concentration inside the semiconductor. Moreover, in real Schottky diodes, the barrier height too, is not a function of the doping concentration and is strongly affected by defects at the metal-semiconductor interface. Based on the energy distribution of these defects and their corresponding occupancy, the Fermi level inside the semiconductor is "pinned" at a fixed energy level independent of the doping concentration in the bulk. Thus, unlike p-n junctions, Schottky diodes are very sensitive to the electrical state of the metal-semiconductor interface. We assume the following values for a Si Schottky diode. The barrier height assumed here is close to that reported for Pt-Si Schottky diodes. The value of Richardson constant (A^*) has been calculated assuming that the effective mass of electrons is equal to their rest mass.

A^* = 120A/ cm^{2}K^2, ϕ_B = 0.9eV, T = 300K, k = 8.617 x 10^{-5}eV/K, area = 10^{-4} cm^2. *Figure 14* shows the effect of changing the ideality factor and the temperature on the forward bias I-V characteristics of a Schottky diode.

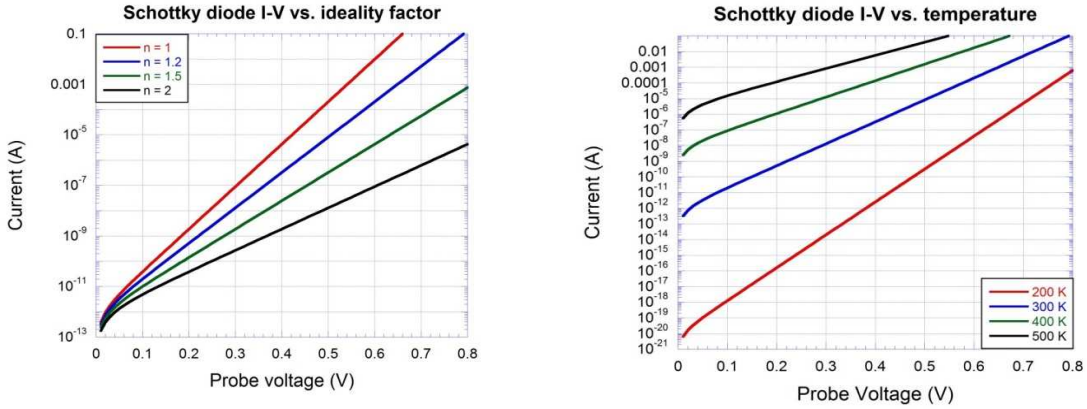


Figure 14. **I-V characteristics of a Schottky diode based on thermionic emission model. (Left) the effect of ideality factor and (right) the effect of temperature.**

The ideality factor accounts for effects which are not well understood in the working of a Schottky diode. Effects like interface defects, recombination in the space-charge region and leakage around the edges of the Schottky contact can increase the value of the ideality factor. The ideality factor affects the slope of the $\log_{10}$(I) vs. V curve of the diode as shown above. The ambient temperature represents the average energy possessed by the majority carriers. Hence their probability of crossing the potential barrier created by the Schottky barrier height at the metal-semiconductor interface increases exponentially with temperature. This is represented in the above figure (on the right), by the increase in y-intercept of the extrapolation of the linear part of the $\log_{10}$ (I) vs. V curve with temperature.

There is another model known as the Diffusion theory which takes into account the recombination of majority carriers within the space-charge region. This theory assumes that (a) the Schottky barrier height is much larger than kT, (b) there are collisions of majority carriers inside the space-charge region which has to be accounted for by mobility, (c) the concentration of majority carriers at the interface and the edge of the space-charge region is not affected by the current flow and (d) the semiconductor is non-degenerate. The current expression using this model is derived by integrating the drift and diffusion currents inside the space-charge region of the diode. The expression for current using this model assuming an n-type semiconductor is as follows (Sze, 1981)

$$J_n = \left\{\frac{q^2 D_n N_C}{kT}\left[\frac{q(V_{bi}-V)2N_D}{\epsilon_S}\right]^{1/2} exp\left(-\frac{q\phi_{Bn}}{kT}\right)\right\}\left[exp\left(\frac{qV}{kT}\right)-1\right] \quad (3.5)$$

In equation (3.5), the term D_n is the diffusion coefficient of electrons, N_C is the density of states in the conduction band, V_{bi} is the potential barrier at the metal semiconductor interface looking from the semiconductor, V is the applied voltage, N_D is the doping concentration, ϕ_B is the Schottky barrier height, k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge and ε_S is the permittivity of the semiconductor. The expression is identical in nature to the thermionic emission model with the exception that it depends strongly on the doping inside the semiconductor and the diffusion coefficient of the majority carriers.

In both the models discussed above, it is assumed that the Schottky barrier height is independent of the bias applied to the diode. In reality this is not entirely true. There is a phenomenon known as image force barrier lowering which reduces the barrier height by a small amount during forward bias and increases it during reverse bias. When an electron is emitted from a metal, a positive charge is induced on its surface which exerts an attractive force on the electron. If the electron is at a distance of 'x' from the surface of the metal this force is equivalent to the force that would exist between the electron and a positive charge which is at a distance of '-x' from the surface of the metal. This attractive force is also known as image force which is given by the following expression (Sze, 1981)

$$F = -\frac{q^2}{16\pi\epsilon_0 x^2} \quad (3.6)$$

Where, ϵ_0 is the permittivity of free space. The potential energy of an electron at a distance 'x' from the surface of a metal in the presence of an electric field E is given by (Sze, 1981)

$$PE(x) = \frac{q^2}{16\pi\epsilon_0 x} + qEx \quad (3.7)$$

This potential energy shapes the Schottky barrier looking into the semiconductor from the metal. The point at which this energy reaches a maximum represents the actual barrier height of the diode and is given by $x_m = \sqrt{\frac{q}{16\pi\epsilon_0 E}}$. The lowering in barrier height due to image force and the external electric field is $\Delta\phi = 2Ex_m$. For metal-semiconductor diodes, the permittivity of free space is replaced by the permittivity of the

semiconductor. In order to illustrate this point better we have plotted the potential energy function for different electric fields to represent different forward and reverse bias conditions of a Si Schottky diode in *Figure 15*.

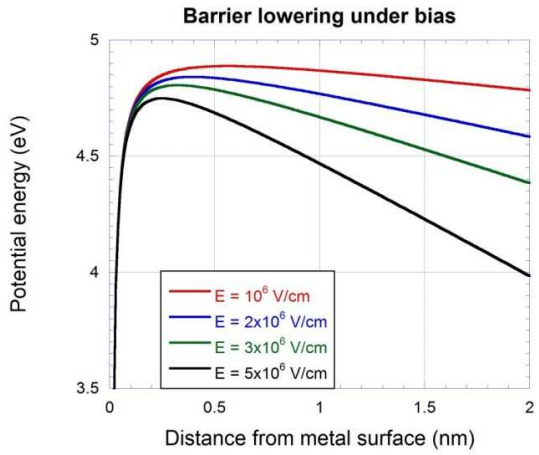


Figure 15. **Potential energy of an electron inside Si with distance away from a metal (Ni) surface under the presence of an electric field.**

The direction of electric field lines is from the right to left for positive values. It has been assumed that the electron is inside Si and the metal is Ni with a work function of 5.0eV. The Schottky barrier is represented by looking from Ni into Si (left to right). The metal ends at $x = 0$ and thus, the electric field which is shown in the figure above is all inside the space-charge region. When the Schottky diode is being forward biased, the electric field inside the space-charge region decreases and the amount of barrier lowering is reduced. Conversely, during reverse bias, the electric field inside the space-charge region increases and there is more barrier lowering. In the case considered here, the ideal potential energy of the electron at $x = 0$ should be 5 eV but it never reaches that value due to image force. The amount by which it is lower than the ideal barrier height is modulated by the electric field at the interface.

In addition to image force barrier lowering, there can also be tunneling of majority carriers through the potential barrier from the metal into the semiconductor to give high leakage currents. In Figure 13(c) the potential barrier for electrons from the metal into the semiconductor becomes narrower during reverse bias increasing the probability of tunneling from the Fermi level inside the metal to the conduction band inside the semiconductor. Tunneling can also happen from the semiconductor to the metal during forward bias provided that the potential barrier is high enough and space-charge region still extends over a

very small distance under the metal-semiconductor interface. Tunneling is a strong function of the energy distribution of charge carriers inside the metal and the semiconductor and hence, varies strongly with temperature and doping. Tunneling leads to an increase in both forward and reverse bias currents. It also increases the ideality factor because at low forward bias the diode starts conducting more current than in the case of thermionic emission over the barrier.

3.3 Nanowire versus planar Schottky diode

Now let us discuss some basic differences which arise due to the structural difference between a nanowire and a planar Schottky diode. The analysis of a three dimensional device cannot be performed in the same way as a planar device because of the difference in geometry. The electric field from the large metal contact at the tip of the nanowire can modulate the concentration of charge carriers on its surface. On the other hand, in a planar Schottky diode, the current is dominated by the electrical nature of the metal-semiconductor interface. The role of the surface of the semiconductor plays a minor role (if any) in determining its I-V characteristics. Fixed charge trapped in the dielectric surrounding the nanowire diodes and the density of electrically active defects or traps, on the surface of the nanowire play a major role in determining the concentration of charge carriers and thus, modulating the conductivity of the diode. Atlas simulator has been used in this research to simulate a 3-D vertical cylindrical nanowire structure representing the real device. *Figure 16* shows a comparison between the cross section through a cylindrical 3-D structure of a nanowire and a planar metal-semiconductor Schottky diode.

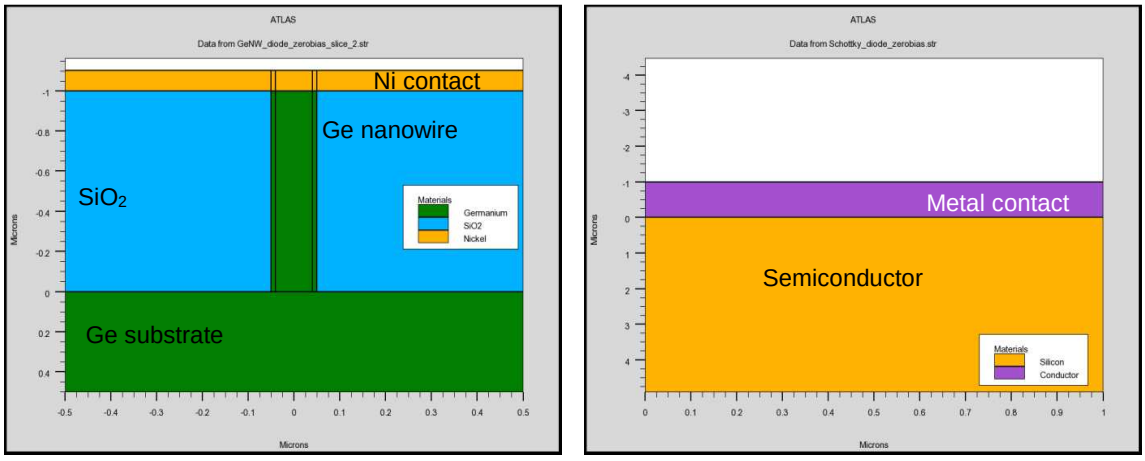


Figure 16. **Schematic representations of the cross sections of a nanowire (left) and planar (right) Schottky diode.**

The simulator uses the drift-diffusion model to calculate the electrical behavior of the nanowire diode. The simulator is capable of using concentration dependent mobility models for estimating the effect of impurity scattering on the current through the diode. For highly doped Schottky diodes, tunneling through the barrier can be implemented. Surface recombination velocity can be set at the surface of the nanowire and the interface with the metal to simulate the effect of recombination due to defects in the actual devices. Acceptor and donor traps can be set at the interface of the nanowire with the dielectric and the metal to introduce bias dependent charge that arises due to trapping and emission of charge carriers.

We now present some basic simulations which show how the geometry of the nanowire diodes makes its analysis different from a planar device. A good point to start will be to observe the potential distribution and electric field as a voltage is applied at the metal contact on the tip of the nanowire. Since the electric field lines arising from the metal contact go through the Schottky barrier and also wrap around the sidewalls of the nanowire, the conductivity of the device can be modulated in a way different from what is possible in a planar Schottky diode.

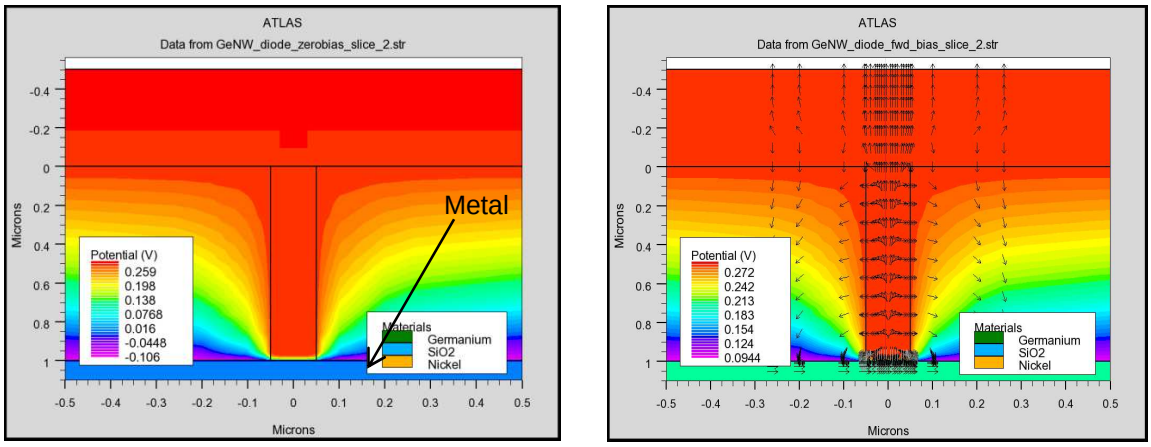


Figure 17. **Potential distribution inside and around a nanowire Schottky diode at 0 V in the metal contact (left) and electric field lines at a voltage of 0.2 V on the metal contact (right).**

Figure 17 shows potential distribution inside a nanowire Schottky diode. The simulator plots Fermi potential which is the difference between the Fermi level and the intrinsic Fermi level. So, the values of potential are not straightforwardly intuitive. The electric field lines on the right in *Figure 17* are in the opposite direction to what they are expected to be because if the fact that Fermi potential is plotted inside the semiconductor. However, it is there to just get the point across that the electric field lines from the

metal contact wrap around the nanowire and directly modulate its conductivity in a 3-D architecture like the structure simulated in this study.

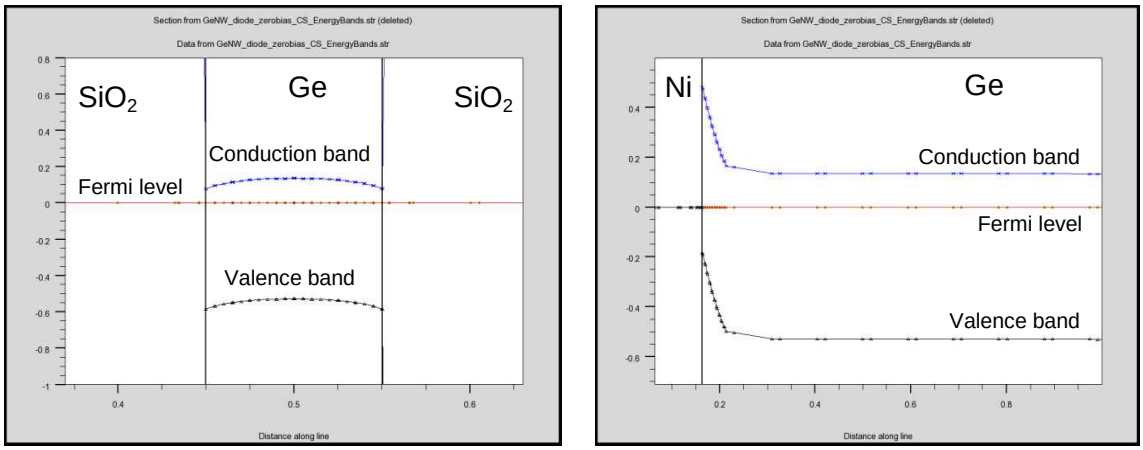


Figure 18. **Energy band diagram across the nanowire (left) and along its length (right)**

Figure 18 presents these energy bands across and along the length of the nanowire structure in *Figure 17*.The energy bands in the horizontal cross section on the left show accumulation of electrons at the edges of the nanowire due to positive fixed charges trapped in the dielectric encapsulating the device. During forward bias, due to the vertical structure of the nanowire, the field lines wrap around it and result in higher electron concentration at the edges of the nanowire than its core, all along its length. Thus, the electric field inside the nanowire is always higher at the edges compared to the center in all directions along the radius of the device. The plots of electric field under zero bias and a forward bias of 0.3 V are shown in *Figure 19*. These horizontal cross sections are taken from a 2-D slice of the nanowire structure.

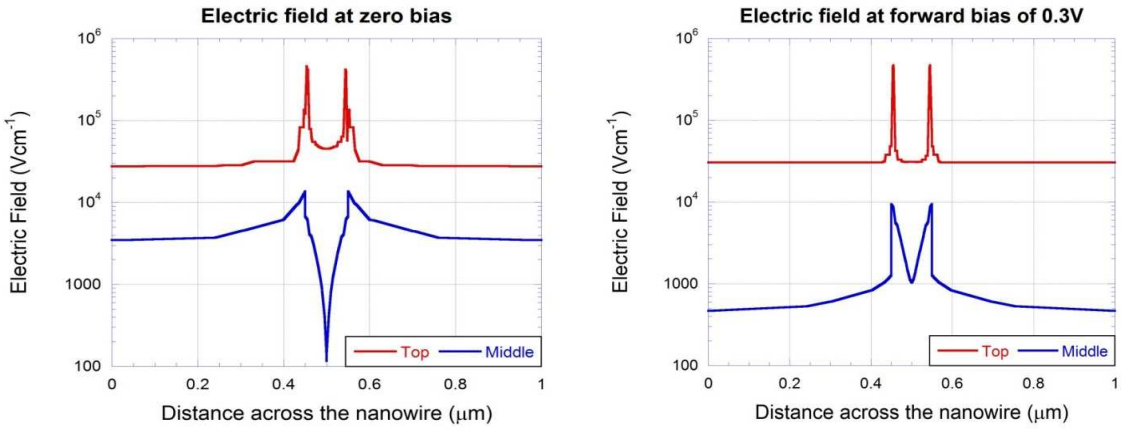


Figure 19. **Electric field across the nanowire at the tip (left) and mid-way along the length (right).**

The electric field along the length of the nanowire is higher at the edges than inside the core. This is due to field lines wrapping around the nanowire and the dimensions of the contact being much larger than the nanowire diameter. The result is crowding of current on the edges of the nanowire which is represented by the current density being very high at the edges plotted in *Figure 20*.

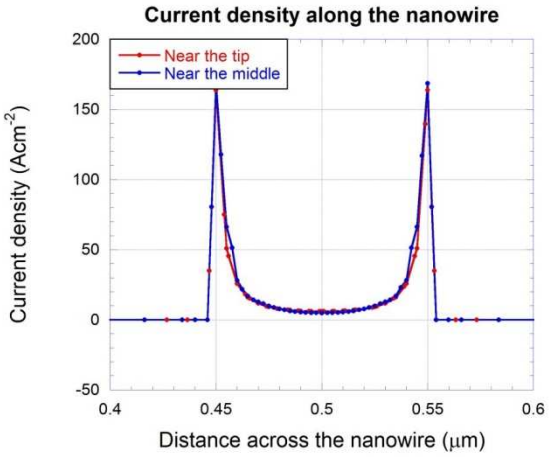


Figure 20. **Current density across the nanowire during forward bias of 0.2V at the tip and mid-way along the length.**

The discussion about potential, electric field and current density in a nanowire shows the basic difference in current conduction mechanisms in a nanowire diode compared to a planar diode. In a planar diode, the electric field stays almost constant at the points which are at the same distance from the metal-semiconductor interface. Thus, we can assume current to be passing through the entire cross section of the diode uniformly. Clearly, that is not the case for the nanowire where the surfaces and edges of the contacts play a major role.

Vertical nanowire diodes are surrounded by a dielectric which can have trapped charges inside it. Spin-on-glass used in this research to encapsulate the nanowires, contains positive trapped charges with a sheet density ~10^{11} cm^{-2}. This should accumulate the nanowire on the edges bending the conduction band towards the intrinsic Fermi level. As the diameter of the nanowire gets smaller, the bending of the conduction band becomes more severe and consequently, the electron concentration inside a thinner nanowire becomes greater than that inside one with a larger diameter. This effect tends to increase the current conducted by nanowires having a smaller diameter. In reality, this effect will be decreased by series resistance which is larger for thinner nanowires and that has not been accounted for in the simulations but

this is to get the point across that with smaller diameter, the overall electron concentration inside the nanowire becomes larger. The following is a plot of the energy band diagrams at 0 V and a forward bias of 0.4 V at the metal contact on the tip of the nanowire. It is clear that due to interface charge, there is more bending of the conduction band towards the intrinsic Fermi level in the thinner (60 nm diameter) nanowire and this effect is enhanced during a positive bias on the top contact. *Figure 21* shows the energy bands across a vertical cut-plane along the length of a nanowire structure simulated in Atlas. It clearly shows how the conduction band has more bending in the 60 nm diameter nanowire which causes it to have a higher overall electron concentration.

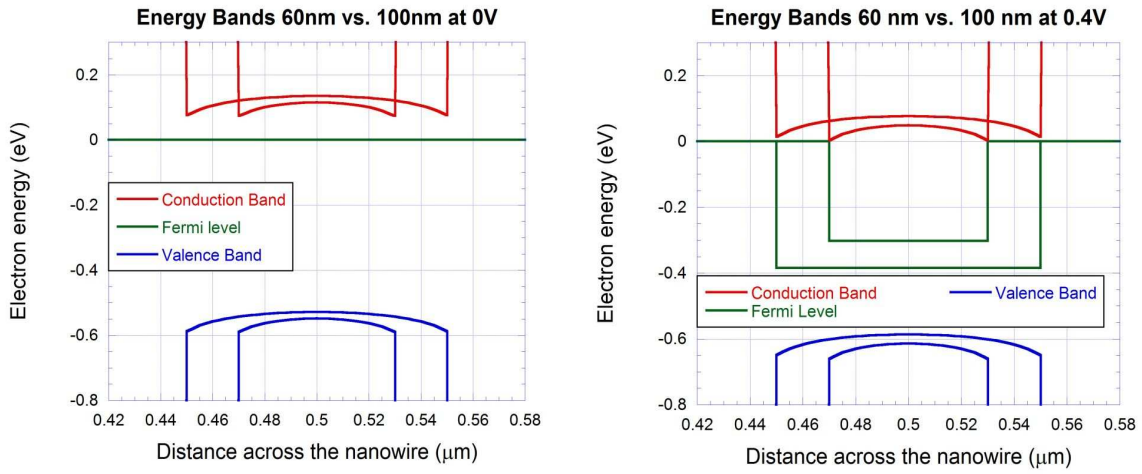


Figure 21. **Energy band diagram inside a 60 nm vs. 100 nm nanowire for 0 V (left) and a forward bias of 0.4 V.**

The electron concentration across the nanowire is mentioned in *Figure 22*.

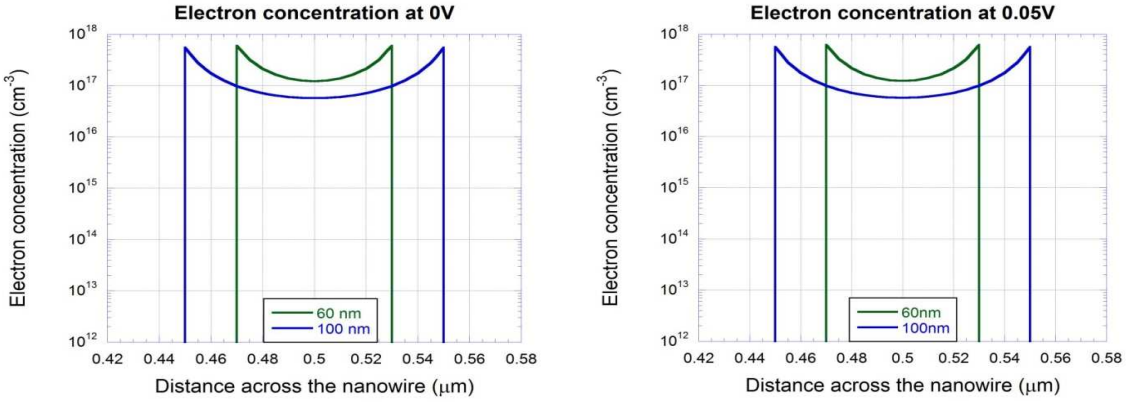


Figure 22. **Electron concentration inside a 60 nm vs. 100 nm nanowire for 0 V (left) and a forward bias of 0.05 V (right).**

The electron concentration is higher inside the 60 nm diameter nanowire compared to the 100 nm because the trapped charge at the Ge-SiO_2 interface bends the conduction band more and creates a higher electric field inside the thinner nanowire. Since the electron concentration is higher, there will also be more scattering of charge carriers causing the mobility to be lesser in a 60 nm diameter compared to a 100 nm diameter nanowire.

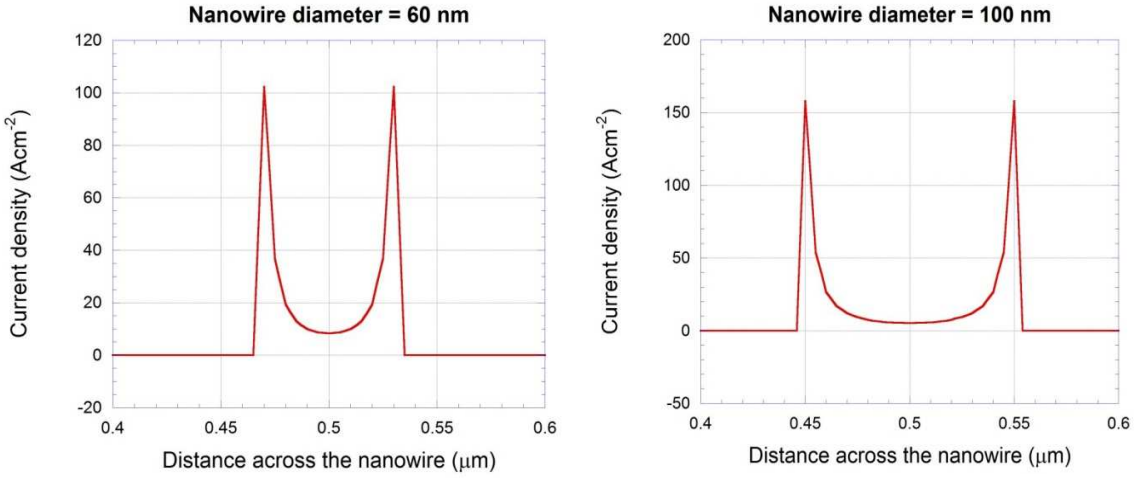


Figure 23. **Current density across a 60 nm (left) and a 100 nm diameter (right) nanowire.**

Figure 23 shows the current density across a 60 nm and 100 nm diameter nanowire. Since the electron concentration is higher in a 60 nm diameter nanowire, the barrier height is more in the ideal case, and the forward bias current is less than for a 100 nm diameter nanowire as shown in *Figure 24*. Another important conclusion from these simulations is that the surfaces play a major role in conduction of current as most of the charge carriers flow closer to the surface.

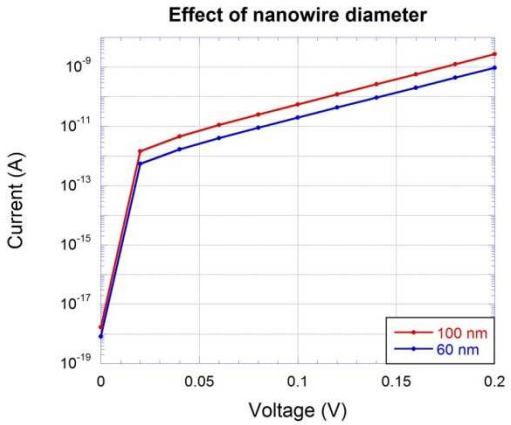


Figure 24. **I-V characteristics of a 60 nm vs. a 100 nm diameter nanowire with interface trapped charge = 10^{12} cm^{-2}.**

Now we observe the effect of minority carrier recombination lifetime on the I-V characteristics of the nanowire Schottky diode. We simulate a 100 nm diameter nanowire varying the minority carrier lifetime in the bulk of the nanowire from 1 ms to 1 ps with a capture cross section of 10^{-15} cm^2.

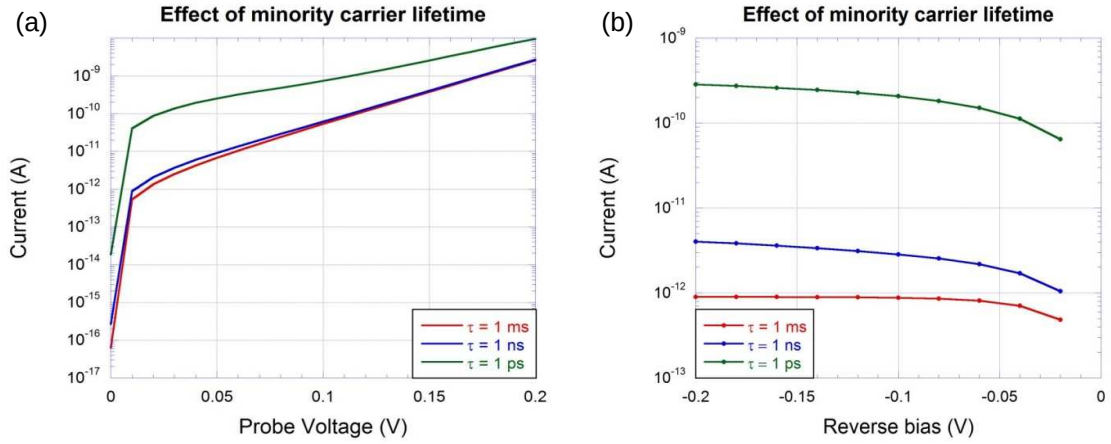


Figure 25. **Effect of bulk recombination lifetime on the I-V characteristics of a 100 nm diameter nanowire (No trapped charge at the interface). (a) During forward and (b) during reverse bias.**

There is an increase in forward and reverse bias current for minority carrier lifetimes below 1 ns in the absence of trapped charge. The magnitude of increase in current due to recombination is much more visible under reverse bias than in case of forward bias. This is because the current that is available during reverse bias is only by the emission of electrons over the Schottky barrier from the metal into the semiconductor whereas during forward bias, thermionic emission of electrons from the semiconductor into the metal is over a potential barrier lesser than the Schottky barrier height by an amount equal to the Fermi

potential of the semiconductor. The conclusion from the simulation shown in *Figure 25* is that increase in recombination rate inside the nanowire can cause the current to increase. We observed in *Figure 24* that just by decreasing the diameter of the nanowire to 60 nm the current was increased due to the positive trapped charge at the interface of the nanowire with the surrounding oxide. Thus, it can be concluded that surface effects rather than bulk, dominate the I-V characteristics of a vertical nanowire Schottky diode.

3.4 Conclusion

In this chapter the analytical expressions for the relationship between current and voltage of p-n junction and Schottky diodes are presented first. The mechanism of current conduction is mainly by diffusion of minority carriers being injected into the p and n-type regions of the diode. Thus, p-n junction diodes are bipolar devices in which the properties of both electrons and holes can affect the net current. Schottky diodes being unipolar (majority carrier) based devices, conduct current only through emission of charge carriers over the potential barrier (Schottky barrier height) at the metal-semiconductor interface. The ideality factor is a quantity used to sum up all the effects which cause the current through a Schottky diode to deviate from the ideal thermionic emission model. We have analytically calculated thermionic emission current at different values of the ideality factor to show its effect. The Schottky barrier height is not constant but varies with the electric field at the metal-semiconductor interface by a mechanism known as image force barrier lowering. Analytical expressions for this effect have been presented and their effect on the Schottky barrier height has been demonstrated by plotting the potential energy of an electron as a function of distance from the metal-semiconductor interface.

We have then made an attempt to show the difference in the way current is conducted in planar diodes compared to nanowires. The main difference is that in planar Schottky diodes, the surface of the semiconductor is not as important in governing the current as in case of nanowires. A vertical n-type Ge nanowire on n-type Ge substrate with a metal contact on its tip has been simulated to show this difference. Since the area of the metal contact at the tip of the nanowire is very large compared to the cross section of the nanowire itself, the electric field lines from the contact wrap around the device and directly affect the concentration of charge carriers along its length. Thus, most of the current in a nanowire diode is conducted very close to the surface. During forward bias (positive voltage at the metal contact), this causes most of

the current to flow close to the surface of the nanowire. Thus, it is concluded that the mobility of the charge carriers is strongly affected by the condition of the nanowire surface.

CHAPTER 4

FABRICATING ARRAYS OF VERTICALLY ORIENTED NANOWIRE DIODES

4.1 Introduction

In this chapter, the process designed to fabricate nanowires has been discussed in detail starting from the layout of the pattern. A brief discussion about electron beam lithography has been presented because it is the key step for transferring the layout on to the substrate. Apart from that, other types of processing like spinning resist; developing the exposed pattern; chemical treatment and metal deposition have been mentioned with the reasons for choosing those methods. Then, the results of bottom-up VLS growth of Ge nanowires on (111) Si and Ge substrates have been presented with the conclusion that it was only possible to grow vertically oriented Ge nanowires with good yield on Ge substrates. Encapsulation of Ge nanowires in spin-on-glass has been presented next. A process for fabrication of vertical Si nanowires on Si substrates using the Bosch process has also been presented. The effect of changing the durations of etching and polymer deposition on the sidewall roughness of the nanowires has been presented. This chapter presents two different processes for (a) bottom-up and (b) top-down fabrication of Si and Ge nanowire diode arrays on Si and Ge substrates respectively. The processes developed here can be used as platforms for development of any vertical nanowire device and thus opens up a large range of possibilities for integration of Si and Ge nanowires into the CMOS process giving a boost to scaling of integrated circuits.

4.2 Bottom-up fabrication using the VLS technique

The Vapor-Liquid-Solid (VLS) method requires that the substrate be patterned with the catalyst metal and the size of the metal particle determines the diameter of the nanowire which grows at that site. The catalyst metal for our process is Au and the substrate is highly doped n-type Si. The reason for this choice of material is that Si and Ge nanowires have been shown to grow on Si substrates using Au as the catalyst (Picraux, Dayeh, Manandhar, Perea, & Choi, 2010) and having a highly doped substrate makes it possible to have an Ohmic back side contact to the wafer without having to explicitly fabricate one.

The entire process of fabrication can thus be divided broadly into the following steps:

- Patterning Au catalyst particles on Si and Ge substrates

- Growing nanowires using the VLS technique
- Making electrical contacts to the nanowires

Each of the above steps can be subdivided into smaller tasks which when performed sequentially, will complete the process. Let us start with the first step.

4.3 Patterning Au catalyst particles on a substrate

The size of the Au catalyst particles controls the diameter of the nanowires grown using the VLS technique. In order to observe the effect of different diameters and number of nanowire diodes connected to a single electrode, we fabricated 20 arrays of nanowires within a ~ 2 x 2 mm^2 area on the substrate. The catalyst particles were square-shaped with the lengths of their edges being 100, 80, 60 and 40 nm. For each size, there were five arrays having 400, 240, 160 and 40 particles. The locations for deposition of these Au particles were defined using electron beam lithography. The remaining part of this section is dedicated to the main features of this process, which are the following:

- The layout
- Spin-coating PMMA
- Electron Beam Lithography
- Developing the pattern
- Metal deposition and lift-off

The subsequent sections will describe in detail how these steps were designed and implemented. Some references from the existing literature will be provided wherever some background is required.

4.4 Designing a layout

The most important step in fabricating a semiconductor device or circuit is designing the layout. In this research our purpose is to fabricate and test semiconductor nanowire diodes. Therefore, the layout had to be flexible enough to allow the measurement of the current-voltage characteristics of an array of diodes as well as an individual diode using external probes. For this purpose, the arrangement of nanowire arrays was important so that there was a clear way to lay down metal lines which contacted all the nanowires. A provision for growing nanowires of different diameters had to be made so that any parameters which change with the diameter of nanowires could be identified. Therefore, different components had to be put

on different layers such that each layer could be fabricated independently and precisely aligned to the other layers. The remaining part of this sub-section will describe each layer of the layout in detail.

4.4.1 Layer 1: Global alignment marks and chip marks

The main purpose of alignment marks is to provide the lithography tool with a reference for calculating the exact location of all the features to be written on a chip. The tool does these calculations based on the layout provided by the user. The global alignment markers are used by the tool to correct for any distortion in the shape of the wafer which is likely to arise due to mechanical handling, high temperature processing, etc. Apart from this, using global alignment markers, the tool calculates the angle by which the wafer is tilted after being mounted on the stage on which lithography takes place. Calculating the tilt is critical because the stage moves as it transfers the pattern onto the substrate. The mechanism which moves the stage has to be programmed to follow the exact angle by which the wafer is tilted otherwise, the positions of different features on the actual pattern would differ from the layout. Therefore, the global alignment markers define in a way, the rows and columns along which the stage of the lithography tool has to be moved.

The chip marks provide the exact locations on those rows and columns where the features are located. Chip marks are also used by the tool to refine the value of the tilt calculated using the global alignment markers. In this way, the global alignment markers and chip marks make it possible to write several layers of features on top of each other in a perfectly aligned manner.

The alignment marks were designed in accordance with the requirements of electron beam lithography. Four global alignment marks (P, Q, R and S) were arranged on four corners of the wafer as shown in *Figure 26*.

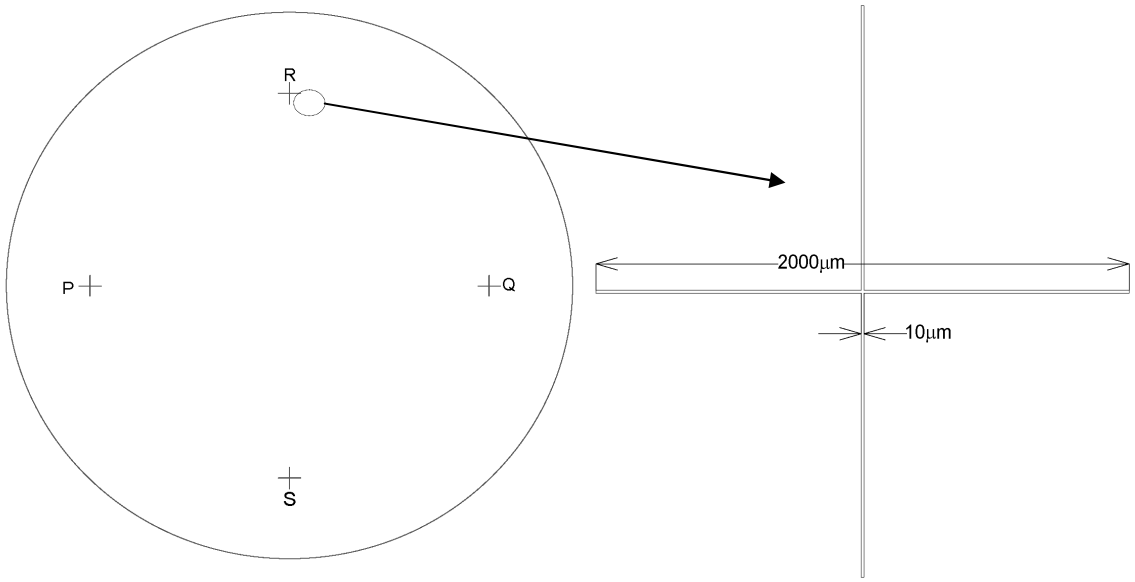


Figure 26. **(a) Arrangement of global alignment marks on the wafer, (b) Dimensions of one alignment marker**

The Si wafer used as substrate to grow nanowires has a diameter of 2 inches as shown in *Figure 26*. The global alignment markers are 2 mm long, 10 μm wide and are 7.5 mm from the edge of the wafer. The nanowires were arranged in arrays at nine different locations on the wafer, each location being called a "chip". So, there were nine identical chips on a single wafer arranged as shown in *Figure 27*. The distance between the centers of any two adjacent chips is 1 cm. Each chip has the design indicated in the above figure. Every chip has three layers defined by different colors in *Figure 27*. The red color represents the local alignment markers or chip marks. The green layer represents the nanoscale clusters of Au which will serve as catalysts for the growth of nanowires and the blue layer represents metal contacts which will be laid down once the nanowires have grown. The subsequent discussion explains the dimensions and purpose of these layers in more detail.

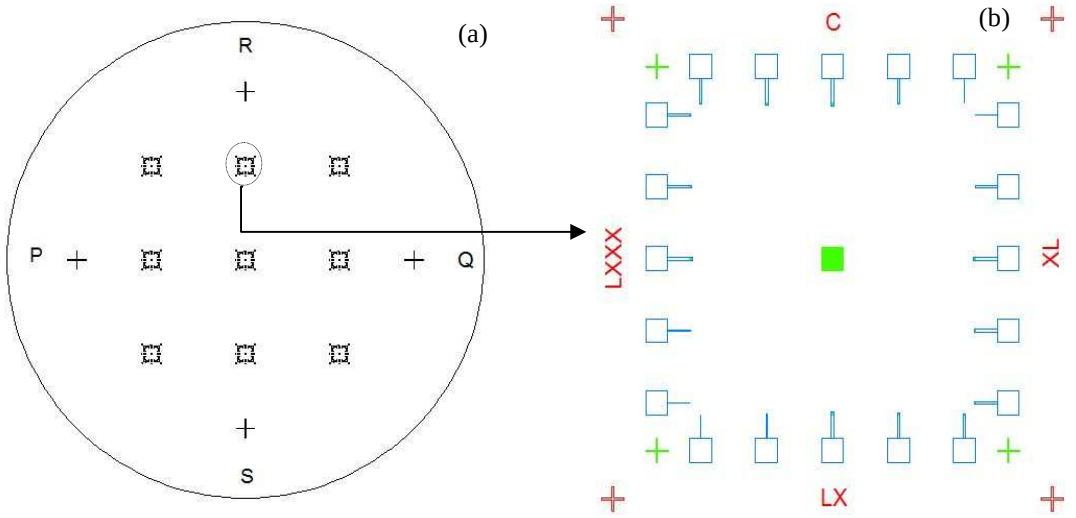


Figure 27. **(a) The arrangement of nine identical chips on the wafer, (b) Enlarged view of a single chip**

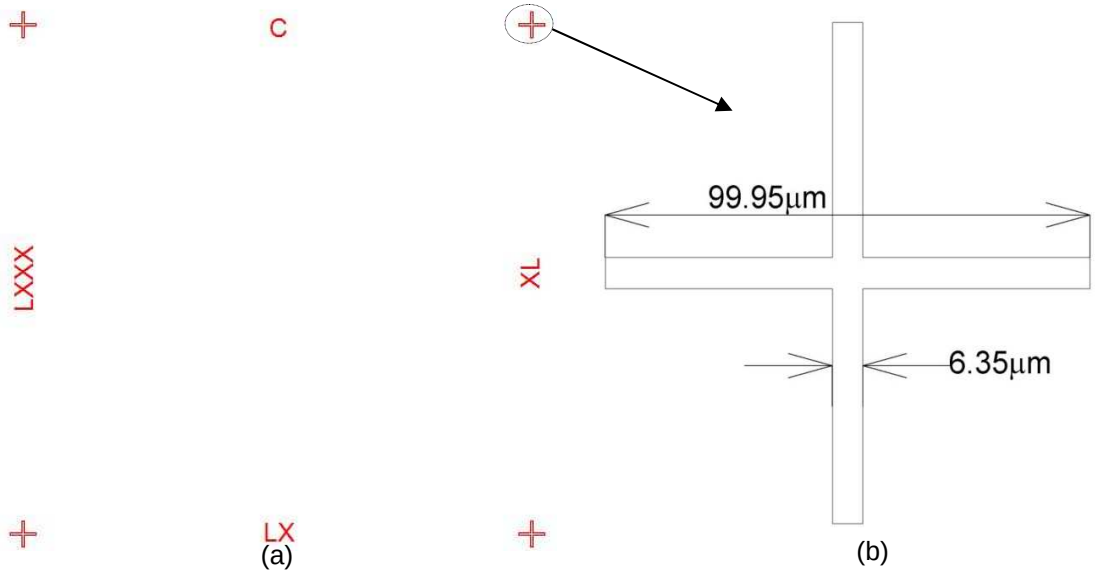


Figure 28. **(a) Layer containing chip marks, (b) Enlarged view of a chip mark**

The red colored layer shown in *Figure 27(b)* has been reproduced in *Figure 28*. The roman numerals signify the size of Au nanoparticles which are shown in the green colored layer in *Figure 27(b)*. Since we have different sizes of nanoparticles in our layout, the roman numerals written along with the chip marks enable us to find where a particular sized nanoparticle is, when we look through a SEM or even an optical microscope. The enlarged view of a single chip mark is shown in *Figure 28(b)*. It is 99.95 µm long and 6.35 µm wide. The material used for this layer is TiW because it has a high melting point and good

adhesion to a Si substrate even if there is some native oxide on it. TiW is also fairly easily spotted under the SEM. However, it does react with HF even in dilute solutions and care has to be taken not to expose these alignment marks to the acid.

4.4.2 Layer 2: Au catalyst particles

Figure 29 shows in detail, the features present in the layer colored green in *Figure 27(b)*. Arrays of nanoparticles are arranged on the boundary of the design and one array of 60 nm by 60 nm nanoparticles is in the center. The number of nanoparticles inside each array is indicated by the number written beside it. The sizes of Au nanoparticles making up the arrays are indicated using arrows. It is evident by looking at *Figure 29* that this design will allow us to measure I-V characteristics of nanowires both individually as well as in arrays.

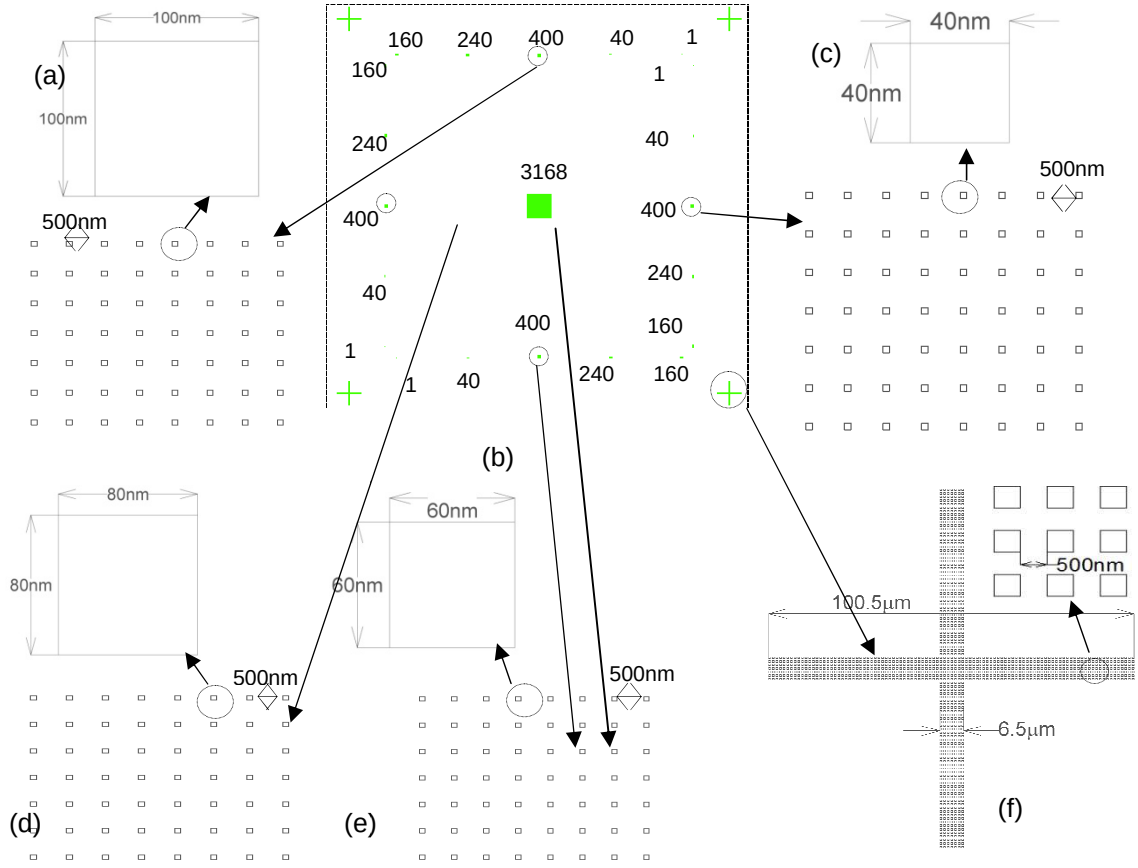


Figure 29. **(b) Layer having Au catalyst particles; (a), (c), (d) and (e) Enlarged views of a 100, 40, 80 and 60 nm particle array and corresponding single clusters (Not to scale); (f) Single dot-matrix chip mark and an enlarged view of its constituent 500 nm particles. (Not to scale)**

In some layouts used in this research, the distance between adjacent catalyst particles was increased to 4 µm for being able to clearly identify the number of nanowires grown vertically. On top of that, the nanowires are of four different sizes from 100 nm down to 40 nm. Such measurements will help us understand how a single nanowire behaves electrically and how the individual properties of several nanowires add up when a large group is considered. We will also come to know what changes in these properties when the size of a nanowire is reduced.

Apart from the above mentioned information, there is another set of chip marks in this layer which is different from the one in the previous layer described in *Figure 28*. These alignment marks are actually groups of 500 nm by 500 nm squares whose centers are 1 µm apart. We call them "dot-matrix" type alignment marks. The name signifies resemblance to the printing style of a dot-matrix printer in which each character is actually a collection of closely printed dots. The purpose of introducing these "dot-matrix" marks is to create a backup plan for aligning the metal contact layer. In case we lose the TiW alignment marks during growth of nanowires, we will not have a reference while laying down the metal contact layer. The idea is to grow thick nanowires on the dot-matrix alignment marks at the same time as the rest of the wafer so that after the growth is complete, we can look at the nanowires grown where the dot-matrix alignment marks are located and the collection of their tips would resemble an alignment mark. Then, the position of this alignment mark can be used as a reference in writing the metal contacts using electron beam lithography.

4.4.3 Layer 3: Metal contact lines

Metal contact lines will be needed to connect the tips of the nanowires to external probes. The blue colored layer shown in *Figure 27(b)* has all the metal contact pads and lines connecting them to the tips of the nanowires as shown in *Figure 30*.

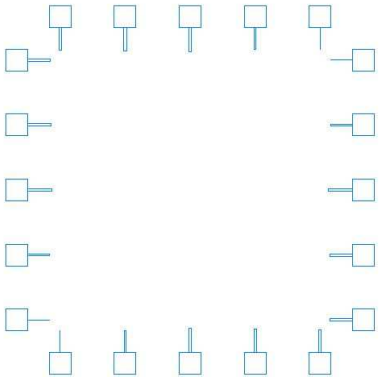


Figure 30. **100 µm by 100 µm metal contact pads and metal lines connecting them to the tips of the nanowires**

The thin metal lines connecting the nanowires to the contact pads have variable width depending on the number of nanowires covered by them. The contact pads are squares of side = 100 µm so that it is easy to locate and probe them externally.

4.4.4 Spin-coating PMMA

We used 950K PMMA in Anisole as photoresist for laying down the layers described above. PMMA is highly sensitive to electron beams and can give very high contrast patterns which are ideal for nanoscale lithography. The manufacturer supplied us with a 6% diluted solution out of which we made two different solutions of 2% and 4% dilution levels. The 2% PMMA solution was used to form 100 nm and the 4% was used to form 200 nm coatings of resist. The resist thickness was chosen based on the thickness of the metal layer to be deposited. For alignment marks in our design the metal thickness is 50 nm and their size is of the order of a few microns so we decided to have a 100 nm resist coating for that particular layer. For the layer of Au nanoparticles it was decided that 200 nm of resist would be sufficient. The main reason was the small size of features on this layer. Metal lift-off is more likely to be successful if the resist layer is 3-4 times thicker than the thickness of the metal layer because there has to be an abrupt discontinuity between the metal layer deposited over the resist and that deposited over the substrate. This discontinuity helps in cleanly lifting off the metal layer over the resist without affecting the deposited pattern to reproduce the layout accurately on the substrate. The need for having this discontinuity increases when the feature size is very small because then if the metal layer over the resist is somehow connected to the one on the substrate, it can peel off entirely, leaving no metal on the substrate. However, there is a risk involved in

writing small features over a thick resist layer. If the exposure dose is even slightly less than the optimum value or if the developing process leaves behind even a monolayer of the resist molecules on the developed area, the metal may not stick to the substrate. So, we kept the exposure dose at a higher than optimum level and over-developed the exposed pattern.

It was observed while designing this process that the thickness of the resist layer at the same spin speed decreases with increase in the size of the sample. The temperature of the solution also affects the thickness of the final coating. In order to determine the correct spin speed for achieving a particular resist thickness, a spin curve was plotted using both 2% and 4% PMMA solutions and it was found that at 1000 RPM, the 2% solution gave a 100 nm and at 3000 RPM, the 4% solution gave a 200 nm thick resist layer on a 2-inch wafer.

4.4.5 Electron Beam Lithography (EBL)

This is the most important step in the entire process. We have used the JEOL 6000 FS/E electron beam lithography system to pattern the resist layer for defining the TiW alignment marks and the Au nanoparticles. Electron beams have a wavelength of the order of Angstroms (10^{-10} m) which allows us to expose nanometer sized features on the resist. Optical lithography cannot be used for directly exposing such small features because light cannot be focused to a point smaller in diameter than 0.25 □m, also known as the Rayleigh limit. Although there are resolution-enhancement techniques (RETs) which have enabled the industry to use optical lithography for exposing 22 nm features but, in academia EBL is the workhorse for fabricating nanometer scale features. Poly Methyl Methacrylate (PMMA) is used as an electron beam resist in electron beam lithography. The molecular structure of PMMA gets altered in the locations where an electron beam is incident on it. This altered resist then becomes soluble in a developer solution leaving behind the unexposed resist on the substrate which acts as a mask for metal deposition. PMMA has a very high sensitivity towards an electron beam which makes it a high contrast resist suitable for exposing nanoscale features. The ability of a resist to reproduce small-sized features on its surface is defined by its contrast which is given by

$$\gamma = \left(log_{10} \left(\frac{D_0}{D_1} \right) \right)^{-1}, \tag{4.1}$$

Where, D_0 represents the minimum dose at which the resist is cleared all the way down to the substrate and D_1 represents the maximum dose below which the full thickness of the resist is retained. The value of contrast expresses the sharpness at which the resist profile changes once exposed to electron beam radiation. The higher the contrast of the resist, the better it is for fabricating small features. In our case the contrast was approximately 1.6.

The dose of exposure of the resist is equal to the product of the beam current and the time of exposure divided by the area over which the beam is incident i.e. spot size of the beam. The lithography tool divides a layout into numerous fields. Each field is further categorized into areas and lines, if any. The tool exposes a line by focusing the beam on a spot for a certain amount of time, blanking the beam and moving to a different location, exposing another spot and so on. A closely grouped collection of such spots results in the formation of a line on the resist. The category of area features covers all two-dimensional figures. An area is exposed by increasing the time of exposure of each spot in order to spread it laterally and decreasing the space between adjacent spots. The space between adjacent spots (known as the shot pitch) and the time of exposure (known as the shot time) can be programmed by the user.

The above discussion points out that the fundamental unit of exposure of a pattern using electron beam lithography is the spot size on which the beam is incident. The spot size is a function of the electron beam current and the numerical aperture

$$d \propto \frac{2\sqrt{I}}{\pi \cdot NA}, \tag{4.2}$$

Where, d is the diameter of the spot, I is the beam current and NA is the numerical aperture of the electron lens which can be increased by decreasing the working distance. Low beam currents and small working distances are good for exposing small features. The accelerating voltage determines the lateral scattering of electrons after entering the resist. Large beam currents give rise to a considerable yield of backscattered electrons which have high energies and wide angles of scattering. Backscattered electrons cause unwanted exposure of the resist surrounding the pattern of interest reducing the sharpness of the exposed design and laterally distorting the shape of the features. This is known as the proximity effect. At nanoscale dimensions, such distortion can change the size of the features entirely, rendering the exposed pattern useless. So, a high beam current is detrimental towards the accuracy of electron beam lithography.

However, if the accelerating voltage is high, the electrons can penetrate deep into the resist without being scattered much. This helps in focusing the beam to a very fine spot but also decreases the sensitivity of the resist towards electron beam radiation because the energy transferred to the resist molecules by the electrons decreases due to reduction in scattering events. Consequently, the same thickness of resist requires a higher dose of radiation than what it would, for lower voltages, to be fully exposed. This translates to an increase in the beam current which tends to increase the spot size. Therefore, a compromise has to be struck between the beam current and the accelerating voltage depending on the application at hand. Thus, electron beams having small current and large accelerating voltages are desirable for exposing nanoscale features but, the current should also be sufficient to transfer enough energy to expose the entire thickness of the resist, all the way down to the substrate.

We used two different beam currents in our process. For exposing the alignment marks a beam current of 1 nA and for the nanoparticles, a beam current of 100 pA was used. The accelerating voltage was 50 kV in both cases. While writing the alignment marks the resist thickness was 100 nm and the dose used was 450 μCcm^{-2} whereas for the pattern of the catalyst particles, the resist thickness was 200 nm and the dose was increased to 800 μCcm^{-2}. The higher dose used for nanoparticles is partially because the resist layer was thicker and also because we wanted to over-expose the pattern slightly to reduce chances of having any unexposed/undeveloped PMMA layer on the pattern.

4.4.6 Developing the pattern

The developer used by us had the following three solutions mixed in the ratio 11:10:1.

1.) Methyl-Isobutyl Ketone (MIBK): Isopropyl Alcohol (IPA) = 1:3

2.) 2-Ethoxyethanol (CS): Methanol = 3:7

3.) Methyl Ethyl Ketone (MEK): Ethanol = 26.5:73.5

The exposed wafer was immersed in the developer for 18 seconds for developing the alignment marks and 20 seconds for the pattern containing nanoparticles. Subsequently, the wafer was rinsed in Isopropyl Alcohol (IPA) and de-ionized (DI) water and blown dry with a nitrogen gun. After each developing step, the wafer was hard baked on a vacuum hot plate at 101 C for 60 seconds to harden the resist and drive away any organic or solvent residue. The hard baking step was very effective in sharpening

the resist profiles and increasing the etch resistance of the resist which helped in RIE de-scum and lift-off after Au deposition.

4.4.7 Metal deposition and lift-off

Metal deposition for the alignment marks was done using sputter deposition and for Au particles using thermal evaporation. The choice of a technique for depositing metal on a pattern depends on the size of the features to be designed. The grain size of the metal layer should be smaller than the features otherwise the grains might clog the openings made in the resist and prevent the metal from actually depositing on the substrate. Sputter deposition is fast but results in larger grain size and is therefore not advisable for depositing nanoparticles. Thermal evaporation results in a very small-grained uniform coating with grain sizes close to tens of nanometers and hence is the suitable choice for deposition of the Au layer.

Lift-off is the process of getting rid of the unwanted metal deposited over the resist layer. The resist is dissolved using a suitable solvent and the metal deposited over the resist comes off, leaving behind only the metal deposited directly over the substrate. The quality of lift-off depends on the resist, its thickness, the type of metal, size of the features on the design and the temperature of the solvent bath. During our process, we observed that TiW had very good adhesion to Si and was unaffected by the presence of native oxide. The TiW lift-off could be accelerated using an ultrasonic bath without worrying about losing any of the alignment marks. However, the situation was very different while doing Au lift-off. Since the features were small, there was a risk of losing the nanoparticles during ultrasonic treatment. Hence, the wafers were kept immersed under Acetone for close to 12 hours after which the unwanted Au layer started lifting off on its own. This process was assisted by a gentle flush of solvent using a syringe.

The following process flows indicate how the alignment marks and the nanoparticle layout was transferred on to Si substrates.

PROCESS FLOWCHART: Phase-1 (Alignment marks)

Fresh n-type Si wafer out of the box ρ = 0.01-0.02 Ω cm
O_2 plasma de-scum (3min @ 100W and 2min @ 50W) + BOE clean 2 min
Spin 100nm PMMA using 2% solution @ 1000 RPM
Write alignment marks using EBL at 450 $\mu C\ cm^{-2}$
Develop (18 sec) + IPA (25 sec) + Hard bake 100 C for 60 seconds
Sputter deposition of TiW (thickness = 50 nm) + Lift-off in Acetone

Phase-2 (Au catalyst particles)

Ultrasonic for 3 min + O_2 plasma de-scum (3 min @ 100 W and 2 min @ 50 W)
Spin 200nm PMMA and write test pattern at 800 $\mu C\ cm^{-2}$.
Develop (**20 seconds)** + IPA (25 seconds) + **Hard bake 100 C for 60 seconds**
RIE de-scum in O_2 plasma at 25 W for 60 seconds
BOE clean for 2 min
Au deposition by thermal evaporation (thickness = 40 nm)

4.5 SEM Images of the pattern of catalyst particles

This section presents images obtained after SEM inspection of the wafers on which the above mentioned process was implemented. The pattern was inspected using a Hitachi S 4700-II SEM. An SEM works by illuminating the sample with an electron beam and detecting secondary electrons which are emitted from the surface of the sample. A detector calculates the yield of secondary electrons from the spot on the surface where the electron beam is incident and projects it in the form of a visual signal on a screen. For obtaining a two-dimensional micrograph, the electron beam is scanned across an area on the sample

surface. The detector has to be close to the sample in order to collect as many of the secondary electrons as possible. Secondary electrons are valence electrons knocked out of their shell by the incident electrons through inelastic collisions. They have very low energies and are emitted from a few nanometers under the surface as shown in *Figure 31*. Thus, a high-resolution image of the substrate surface can be obtained using an SEM. The resolution depends upon the spot size of incident electron beam. The spot size can be made as small as a few nanometers depending upon the accelerating voltage and the beam current.

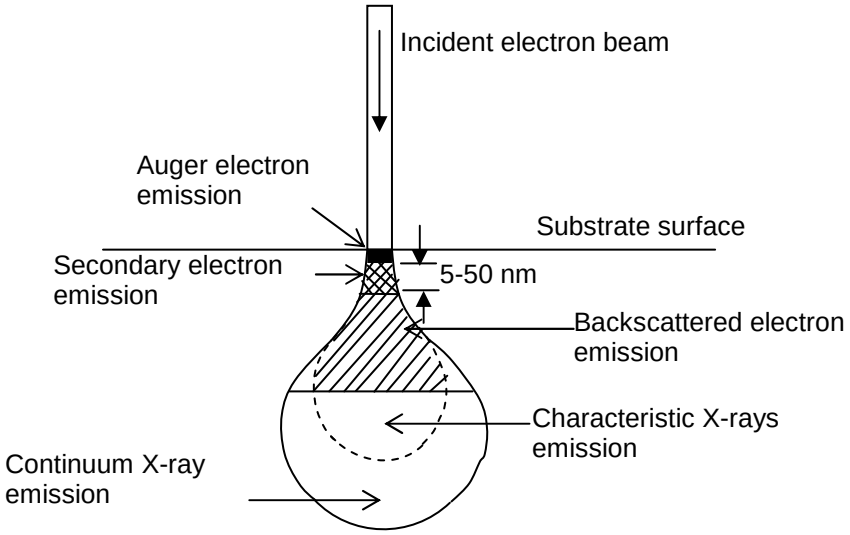
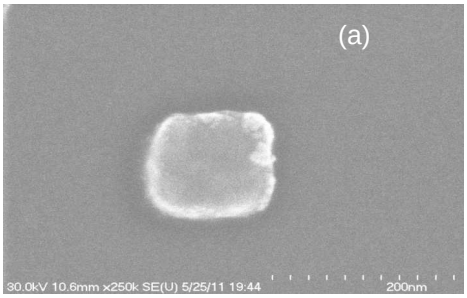
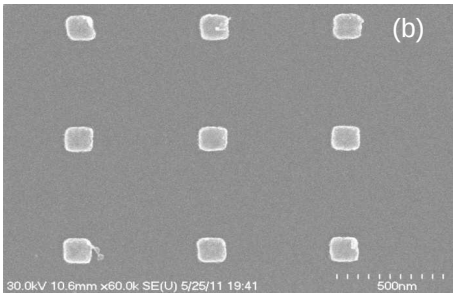


Figure 31. **Interaction of electron beam with a substrate**

For detecting nanoscale features like the ones in this research, the accelerating voltage has to be high and the current has to be kept as low as possible without sacrificing the contrast. We set the accelerating voltage to 30 kV and the beam current as 1.5-2 μA. The working distance was kept between 8-10 mm. The images of Au particles after lift-off are shown in *Figure 32*.





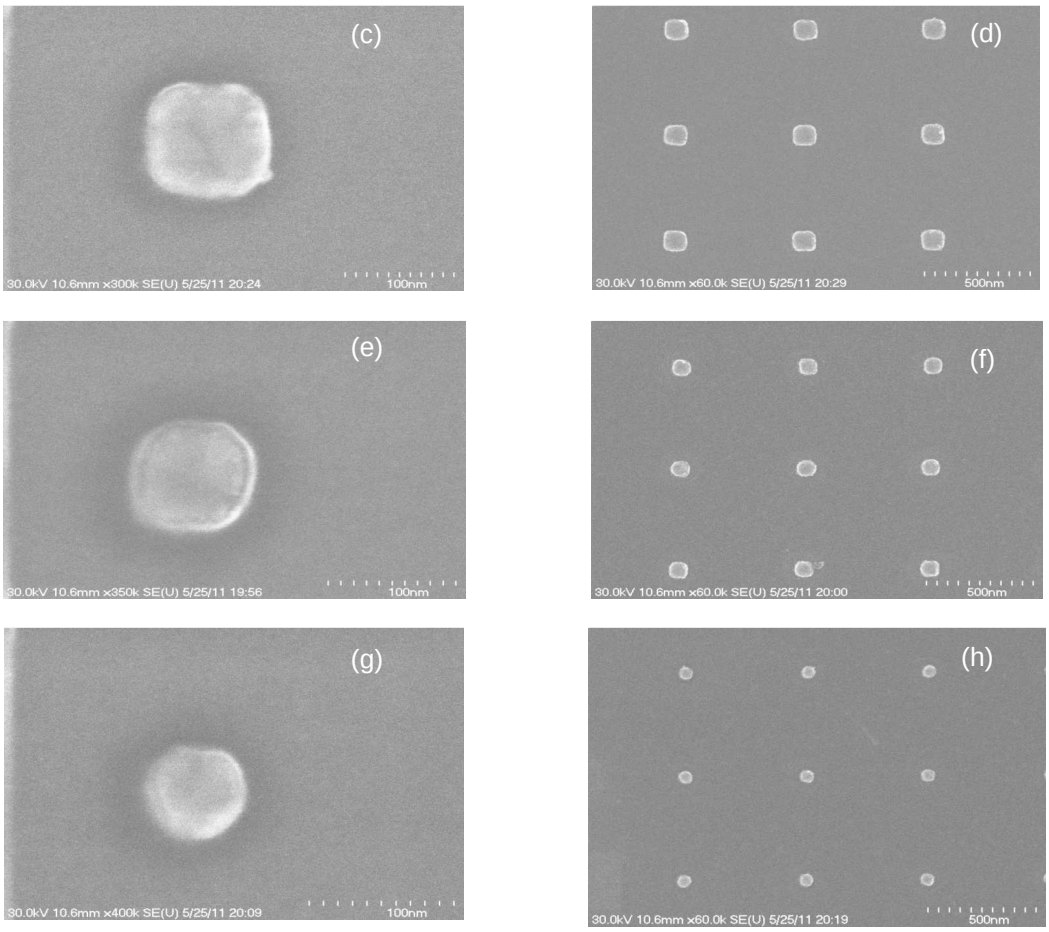


Figure 32. **SEM images of separate Au nanoparticles and their arrays; (a, b) 100 nm, (c, d) 80 nm, (e, f) 60 nm, (g, h) 40 nm**

4.6 Ge nanowire growth using the VLS technique

Germanium nanowires were grown from the Au particles shown in *Figure 32* using the VLS technique. Before starting, the Au patterned Si wafers were subjected to solvent cleaning and native oxide removal using the following processing steps:

1.) Rinse in Acetone and Isopropanol three times.

2.) Remove organic residue using Ozone plasma for 15-20 minutes.

3.) Etch native oxide using 2.5% concentrated HF solution for 1 minute

4.) Rinse with DI water and blow dry with Nitrogen

5.) Load into CVD system for VLS growth

After loading the Au patterned wafer into the CVD chamber, it was pumped down to approximately 10^{-6} Torr. The VLS growth is then carried out as shown in Table 1.

Table 1

Conditions created during VLS growth

Step	**Temp(C)**	**Gas**	**Duration (min)**	**Pressure (Torr)**
Stabilization	480	None	10	10^{-6}
Purge	480	H_2	10	10^{-4} to 10^{-2}
Nucleation	500	H_2, GeH_4, PH_3	1	3
Growth	346	H_2, GeH_4, PH_3	3	3
Cool down	25	No gas	150	10^{-6}

4.6.1 Complete Layout

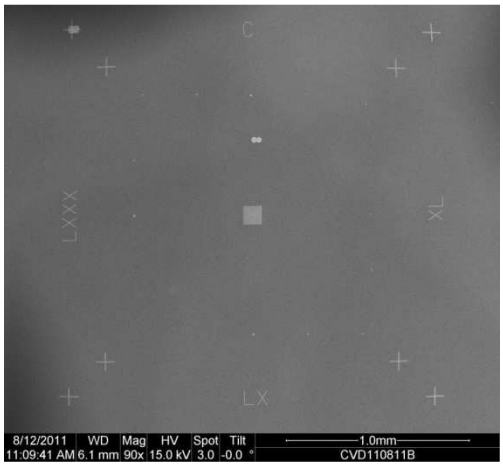


Figure 33. **A zoomed out view of one of the nine chips on the wafer after nanowire growth**

Figure 33 shows a complete view of one single chip present on the wafer. Nine such identical chips are present on one 2-inch wafer as explained in the layout described earlier in this chapter. In the center of the chip we can see the square shaped array consisting of 60 nm diameter nanowires. Also prominently visible, are two sets of four alignment marks each; the outer one consists of solid TiW marks and the inner one consists of Au dot-matrix type marks. On the periphery of the chip inside of the dot-matrix marks, one can see small dot-like features which are actually arrays of 40, 60, 80 or 100 nm

diameter nanowires. The diameter (in nm) of the nanowires along any side of the design is indicated by the Roman numeral written along that side.

4.6.2 Ge Nanowire growth on (111) Si substrates

Ge nanowires grew with good nucleation yield on Si substrates but most of them were oriented in one of the non-vertical <111> directions. The Au catalyst particles also moved away from their lithographically defined locations during nanowire growth, leading to nanowires grown outside the intended pattern. Both these issues were in exact contradiction to the aims of this study as top contacts cannot be made to non-vertical nanowires grown and those grown outside the pattern. *Figure 34* shows the problem stated above.

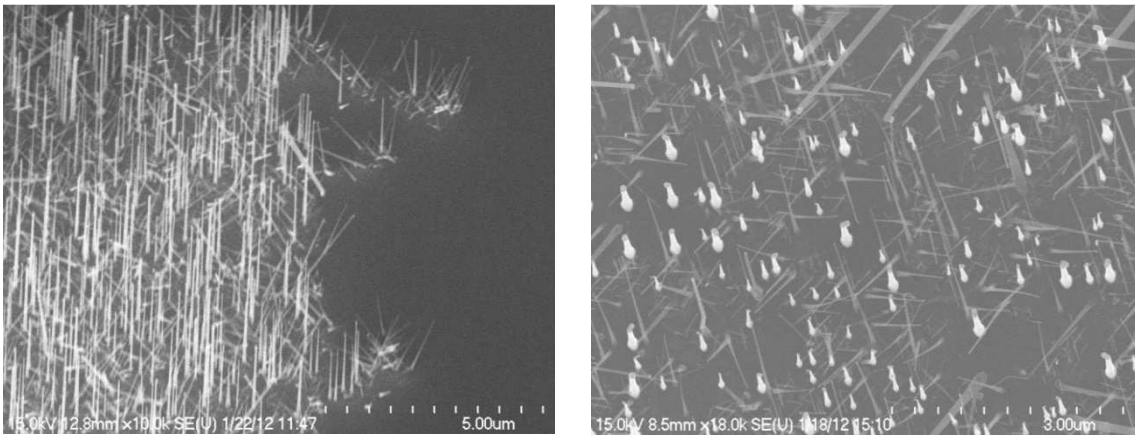


Figure 34. **Ge nanowires on (111) Si substrate. (left) nanowires grown outside the pattern and, (b) non-vertically grown Ge nanowires on Si substrates.**

To prevent the lateral diffusion of Au catalyst particles they were deposited through a pre-defined Si nitride template. A Si nitride layer was deposited on the substrate before depositing the Au particles and selectively etched using 20:1 BOE through a template created in PMMA using electron beam lithography. After liftoff, the Au particles deposited on the Si substrate were surrounded by nitride so that they could not diffuse freely in the x-y plane during nanowire growth. This eliminated the horizontal diffusion but also reduced the nucleation yield of the nanowires as most of the catalyst particles moved to the edges of the windows in the template without nucleating into nanowires as shown in *Figure 35*.

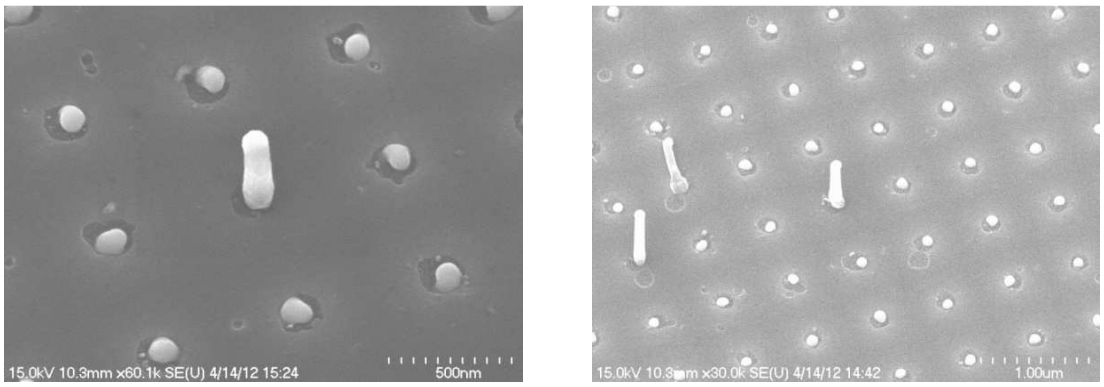


Figure 35. **Ge nanowires on Si substrate grown through a Si_3N_4 template. Nucleation was very poor.**

In an attempt to increase the yield of nucleation of the nanowires, the material of the catalyst was changed from pure Au to an alloy of Au and Ge (88 and 12% by wt.) and deposited through a template made of Si nitride. Even though the nucleation yield was improved but the problem of non-vertically oriented nanowires remained as shown in *Figure 36*.

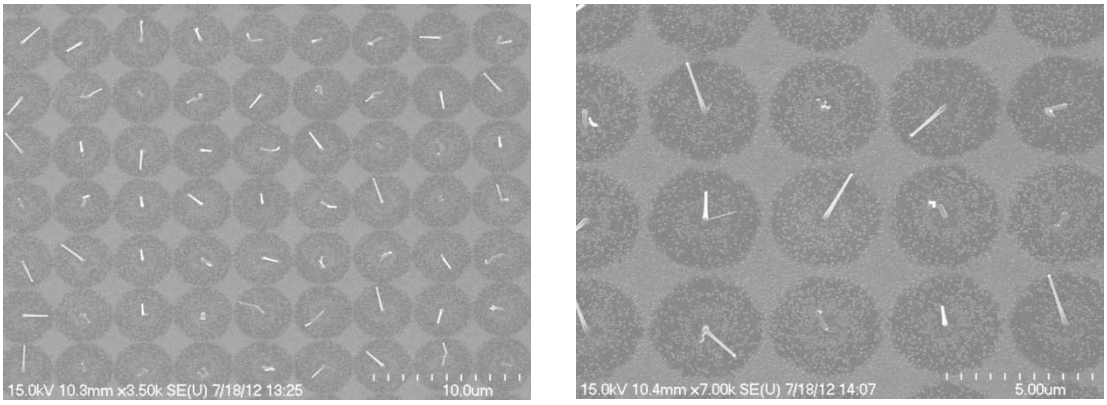
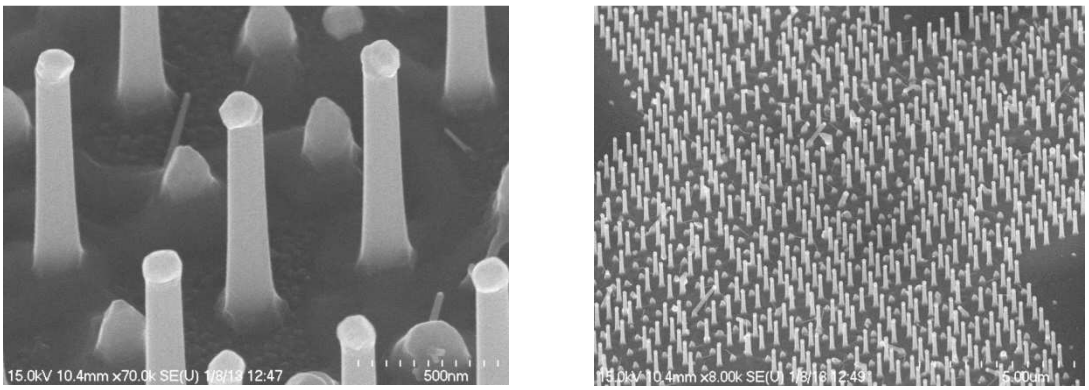


Figure 36. **Non-vertically oriented Ge nanowires grown in Si substrate using Au/Ge alloy as catalyst.**

4.6.3 Ge nanowire growth on (111) Ge substrates

Ge nanowires grew vertically, in lithographically defined positions using the VLS technique on (111) Ge substrates. The same process as described above was used for getting Ge nanowires grown in Ge substrates and yielded the results shown in *Figure 37*.



(a) (b)

Figure 37. **Ge nanowire growth on (111) Ge substrate. (a) Vertically oriented and, (b) Good yield of nucleation and no movement of Au catalyst particles along the substrate during growth.**

The next step after nanowire growth was to encapsulate them in dielectric and make contacts from the top to observe diode-like behavior.

4.6.4 Issues faced during dielectric encapsulation and polishing

The first approach for making top contacts to the nanowires was to deposit Si dioxide using remote plasma enhanced CVD and perform mechanical polishing on the sample to expose the tips of the nanowires embedded in the oxide. However, it was found that mechanical polishing damaged the nanowires and broke off most of them. The SEM images shown in *Figure 38* explain the reason for this problem.

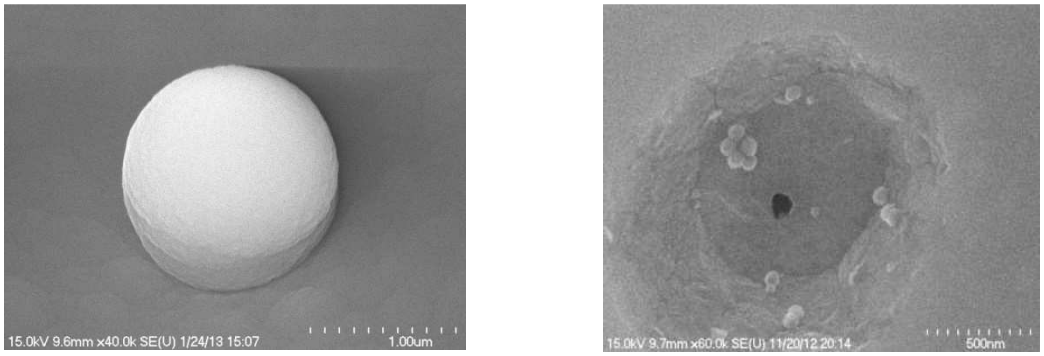


Figure 38. **SEM images of nanowires encapsulated in SiO_2 before (left) and after mechanical polishing (right).**

The deposition of SiO_2 is conformal during CVD and results in the formation of spherical "bump" like structures on the tips of the nanowires. Once these structures undergo polishing, they break off carrying away a significant amount of oxide with them. Without this oxide, the nanowires lose mechanical

support and are broken off from their location which is clearly shown in the SEM image on the right in *Figure 38*.

The hemispherical "bumps" were flattened by sputtering in Ar plasma at 2 mTorr inside a RIE chamber. This eliminated the breakage of nanowires as the bumps no more broke off taking oxide away with them but the nanowires were still found to be damaged after polishing as shown in *Figure 39*. Thus, we decided to eliminate the polishing altogether and come up with an alternative way to encapsulate the nanowires and expose their tips for metal contact formation.

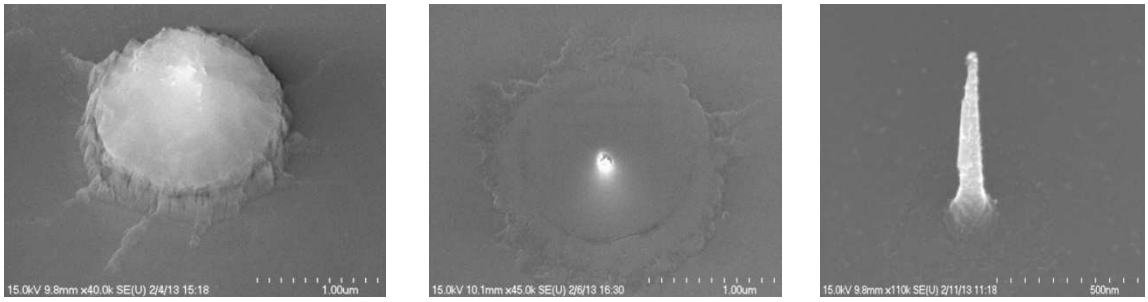


Figure 39. **SEM images of a nanowire tip (Left) after Ar sputtering, (Center) after polishing. (Right) Damage to the nanowire evident after removing all the encapsulating oxide post mechanical polishing.**

4.6.5 Non-uniform doping of VLS grown Ge nanowires

In addition to the problem mentioned above, we found that the doping concentration of P inside the n-type doped Ge nanowires grown using the VLS technique mentioned earlier, increases radially outward and results in a very highly doped "shell" around a moderately doped "core". This has also been reported in literature (Tutuc, Chu, Ott, & Guha, 2006). The reason is believed to be direct incorporation of P atoms into the nanowire through its sidewalls during the VLS growth. The shell doping also decreases along the length of the nanowire towards the tip because of the time for which the nanowire surface is exposed to an incoming flux of dopant atoms during growth.

Even with the problem of nanowires being damaged during polishing, as discussed above, we were able to get some portion of un-damaged nanowires on which we made electrical contacts by sputtering Ni and forming a germanide after rapid thermal annealing. We found that the nanowires behaved as Ohmic conductors and we believe it was because the extremely highly doped shell provided an Ohmic

contact and a leakage path for current and the diode behavior of the core of the nanowire was totally suppressed. *Figure 40* shows Ohmic behavior displayed by arrays of nanowires having different diameters.

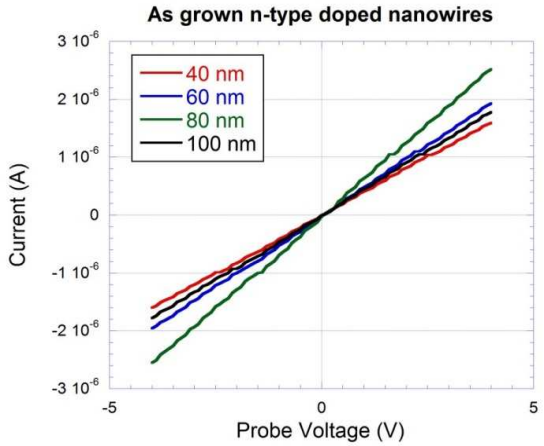


Figure 40. **Ohmic behavior displayed by VLS grown n-type doped Ge nanowires.**

4.6.6 Etching of VLS grown n-type doped Ge nanowires

Due to excessive doping on their sidewalls, VLS grown Ge nanowires have to be etched to remove the heavily doped "shell". Dry etching is good for vertically standing structures but may cause deposition and unknown charged defects to be created on the surface which will affect the electrical characteristics. Therefore, wet etching was chosen for thinning down these nanowires. But before etching the nanowires, it was important to remove the Au at their tips so that direct contact could be made between the top contacts and the Ge nanowires. The Au tips were removed using a 9:1 solution of Transene TFA and hydrochloric acid as described in (Woodruff, Ratchford, Goldthorpe, McIntyre, & Chidsey, 2007). This method does not create any roughness in the nanowire sidewalls and removes Au from the tip as shown in *Figure 41*.

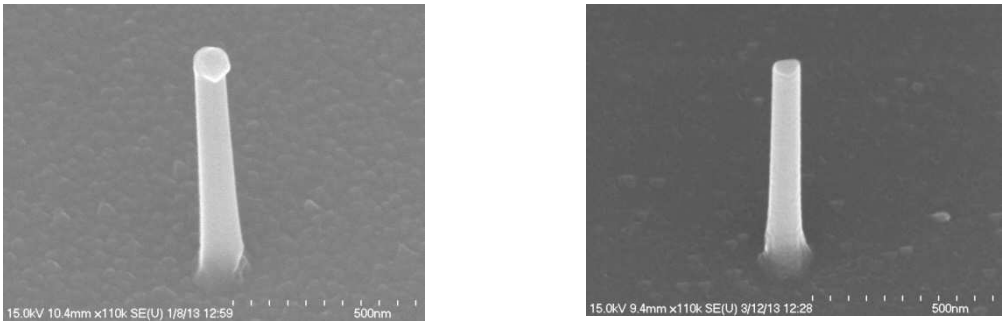


Figure 41. **(Left) Nanowire with Au tip and (right), Au tip removed.**

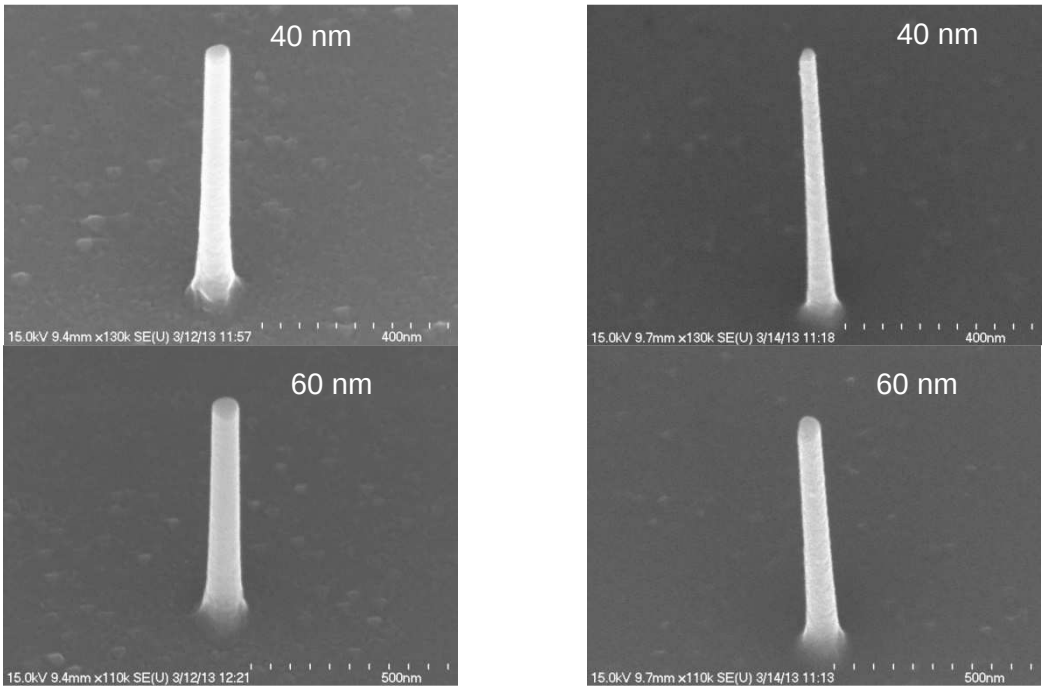
Hydrogen peroxide solution is a strong oxidizing agent and Ge has a native oxide which is soluble in water. We used this property to our advantage by using 0.5% aqueous H_2O_2 solution to etch the Ge nanowires at room temperature. The etch rate of the nanowires was 0.5–1 nm/sec for the samples processed while characterizing this etching process. The diameters of nanowires before and after H_2O_2 etching on the sample studied here are shown in Table 2:

Table 2

Nanowire diameters before and after etching with 0.5% aqueous H_2O_2 solution

Edge length of Au catalyst (nm)	**NW diameter before etching (nm)**	**NW diameter after etching (nm)**
40	59	44
60	83	69
80	103	82
100	114	102

Figure 42 shows SEM images of nanowires before and after H_2O_2 etching.



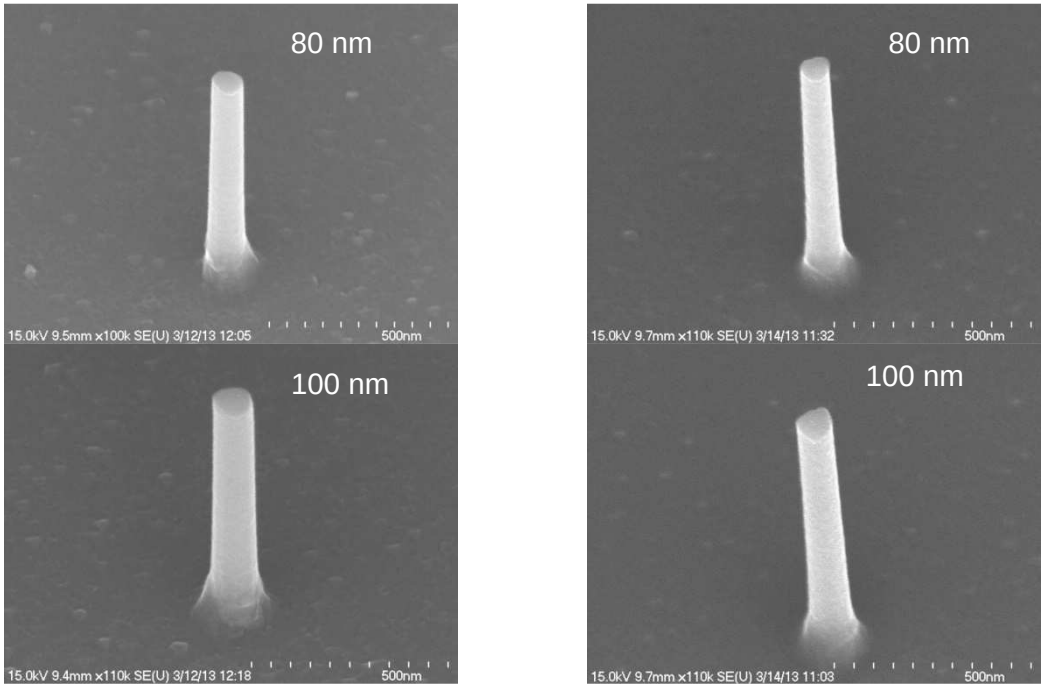


Figure 42. **SEM images of n-type doped Ge nanowires before and after etching with 0.5% H_2O_2.**

4.6.7 Encapsulation of Ge nanowires in spin-on-glass

After etching the nanowires to get rid of excessive doping on the perimeter, they were encapsulated in spin-on-glass. The choice of this technique was guided by the problems faced with deposition of SiO_2 using CVD and mechanical polishing to reveal the tips of the nanowires. Spin-on-glass (SOG) in general, is a polymer containing a Si-O-Si backbone with some other functional groups. Depending on the application, different types of SOG are used. After spin-coating, it needs to be cured at high temperature to release the solvents and leave behind a layer of SiO_x. It is during the cure that the SOG layer shrinks, thereby creating stress. SOG has lower refractive index and higher density of trapped charges compared to deposited oxide but for this application it was the only possible solution we had to encapsulate the nanowires. We used Filmtronics 500F SOG for our purposes because it has low shrinkage (~ 2%) and high resistance to cracking.

Based on the length of the nanowires calculated from the SEM images, the following method was developed:

- Spin coat SOG at 3250 RPM on the nanowire sample.
- Cure on hot plate at 80 C for 1 min.

- Ramp up temperature to 150 C and hold for 1 min
- Transfer to another hot plate at 250 C and hold for 5 min
- Load into a quartz furnace with Nitrogen flow, at 300 C and ramp up to 430 C.
- Hold at 430 C for 60 min.
- Cool down to 100 C in Nitrogen ambient for 60 min.
- Unload the sample.

After spin-coating the SOG a 30 sec RIE etch of SiO_x in CHF_3 + Ar plasma was performed to remove any thin layers of oxide which might be covering the tips of the nanowires. The chamber pressure was set at 30 mTorr and RF power was 200 W. The etch rate of SOG was found to be ~ 100 nm/min which means that ~ 50 nm of oxide was removed from the tips of the nanowires during the etch-back. *Figure 43* shows the nanowire tips after SOG encapsulation (left) and RIE etch-back (right).

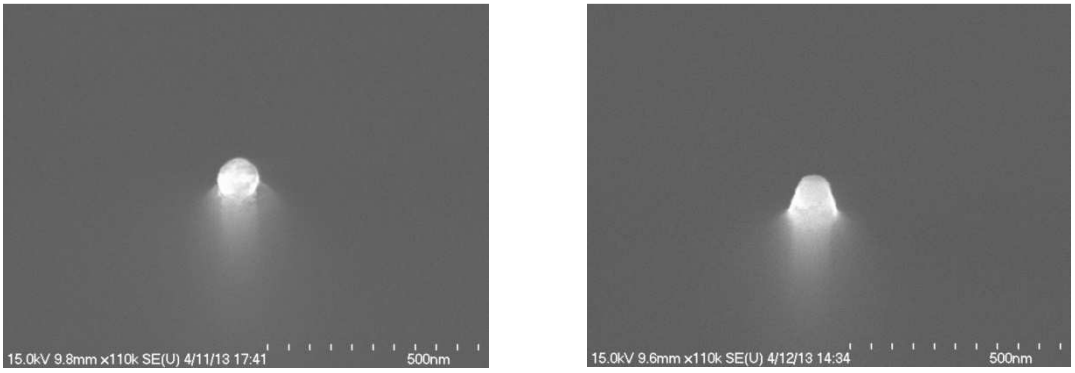


Figure 43. **SEM images of nanowire tips encapsulated in SOG after RIE etch-back.**

4.7 Silicon nanowires by vertical etching

A process for fabrication of vertical Si nanowires using dry etching was also developed to have an alternative method of understanding the rectifying behavior of nanowire diodes. In this process, nanowires are created by vertical reactive ion etching using particles of SiO_2 deposited on a Si wafer using thermal evaporation, as hard mask. The method of patterning and deposition of SiO_2 is exactly similar to that of depositing Au catalyst particles while following the VLS growth technique. The main advantage of this process is uniform doping inside the nanowire which eliminates the problem of Ohmic behavior due to excessive doping. Another benefit of this approach is that the process yields all vertically standing nanowires unlike the VLS technique which is highly sensitive about the material of the nanowire and the

substrate. However, a disadvantage of this technique is surface roughness of the nanowires, which is inevitable because of the nature of the Bosch process and can be reduced but not eliminated. This roughness is likely to create defects which act as recombination centers and modify the I-V characteristics of the nanowires.

4.7.1 Process of fabrication

The process of fabrication of Si nanowires by reactive ion etching is shown schematically in the *Figure 44* (Chandra, Overvig, Tracy, & Goodnick, 2012).

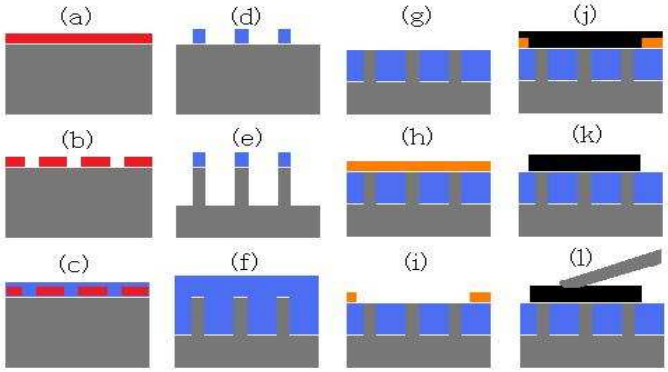


Figure 44. **Schematic representation of fabrication process (not to scale). (a), (b) Positive photoresist spun, patterned and developed. (c) SiO_2 deposited (thermal evaporation). (d) Lift-off in Acetone, leaving SiO_2 islands. (e) Bosch process yields nanowires. (f)-(g) Conformal SiO_2 deposited (RP-CVD) and CMP done to reveal Si tips (h)-(j) Contacts patterned and Nickel deposited by sputtering. (k) Acetone liftoff forming contacts. (l) Electrical probing and characterization.**

The process starts with patterning arrays of square-shaped features of edge length 40, 60, 80 and 100 nm of Si wafers doped to ~ 2 x 10^{15} cm^{-3}. For patterning, the Si wafer was spin-coated with 200 nm thick layer of PMMA and exposed using electron beam lithography. After developing the pattern, a 50 nm thick layer of SiO_2 was deposited using thermal evaporation. Liftoff was done by immersing the sample under Acetone for several hours and gently flushing the solution with a syringe. The liftoff process left behind square-shaped islands of SiO_2 on the wafer as shown in *Figure 45*.

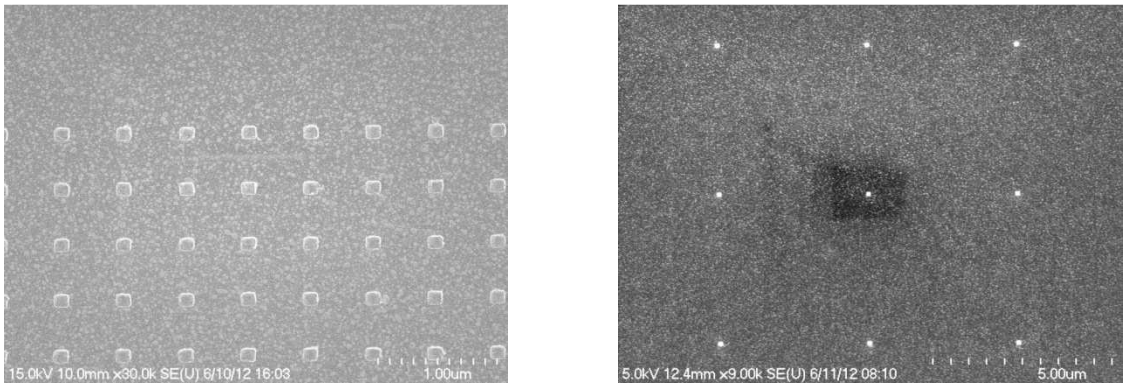
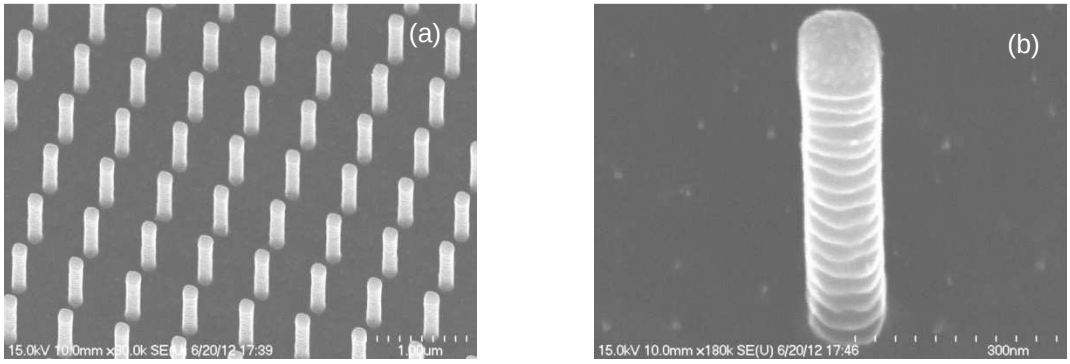


Figure 45. **SiO_2 islands of side-lengths 100 nm and pitch (left) 500 nm and (right) 4□m on the Si substrate.**

No ultrasonic agitation was performed to remove the stray particles of SiO_2 sticking to the substrate because of the risk of accidentally removing the hard mask particles. As we observed, these stray particles did not result in any micro-masking or formation of "grass" like structures during vertical etching. Vertical etching was performed in a Surface Technology Systems (STS) ICP system using the so called Bosch process. Alternating modes of Si etching using SF_6 and polymer deposition using C_4F_8 were utilized for getting vertical nanowires approximately 1µm in length. During etching the plasma contained SF_6 + C_4F_8 with flow rates of 65 sccm and 35 sccm respectively under a pressure of 10 mTorr. C_4F_8 was present during etching for diluting the SF_6 to limit the etch rate of Si and hence the undercutting which results in rough sidewalls. During deposition the plasma contained only C_4F_8 under a pressure of 10 mTorr and flow rate 70 sccm. The RF power was set to 600 W for both, etching and deposition. This yielded an etch rate of ~ 0.5 µm/min which yielded ~1 µm long nanowires in 2 min. *Figure 46* shows SEM images of arrays and single nanowires etched using the recipe mentioned above.



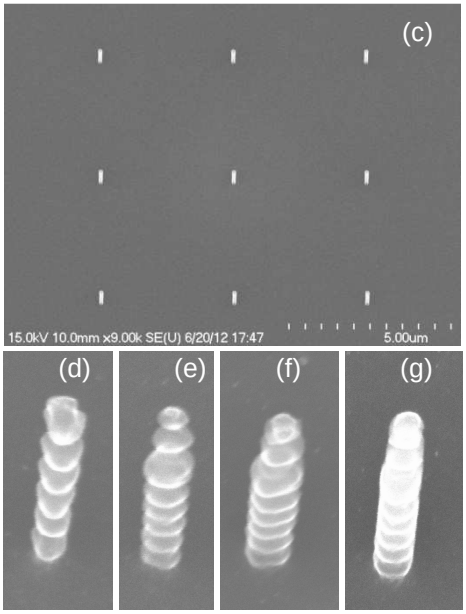


Figure 46. **(a) SEM image of a 500 nm pitch array of 100 nm nanowires after Bosch process using 4 sec etch,2.5 sec deposition cycle. (b) Close-up of a 100 nm nanowire in (a). (c) A 4-micron pitch array of 100 nm diameter nanowires obtained from using 8 sec etch, 5 sec deposition cycle. (d)-(g) SEM images of single nanowires sized 40 nm, 60 nm, 80 nm, and 100 nm obtained from using 8 sec etch, 5 sec deposition cycle.**

The roughness observed on the sidewalls is due to alternating etching and deposition during the Bosch process. By changing the durations of Si etching and polymer deposition we found that there was a trade-off between the number of "scallops" and their depth. We could either have fewer and deep scallops or a large number of shallow scallops on the sidewalls. The latter is better for ensuring good yield and preventing the nanowires from falling over during fabrication. In the experiment shown above 4 sec etch and 2.5 sec deposition gave reasonably shallow scallops and was used to create diodes on which current measurements were made later.

4.7.2 Encapsulation in dielectric and Nickel contact formation

The n-type Si nanowires were encapsulated in SiO_2 deposited using remote plasma enhanced CVD. Mechanical polishing was done to reveal their tips. In this case, the problems of nanowire breakage and damage during polishing were not encountered. *Figure 47* shows nanowires covered in oxide and their tips after polishing.

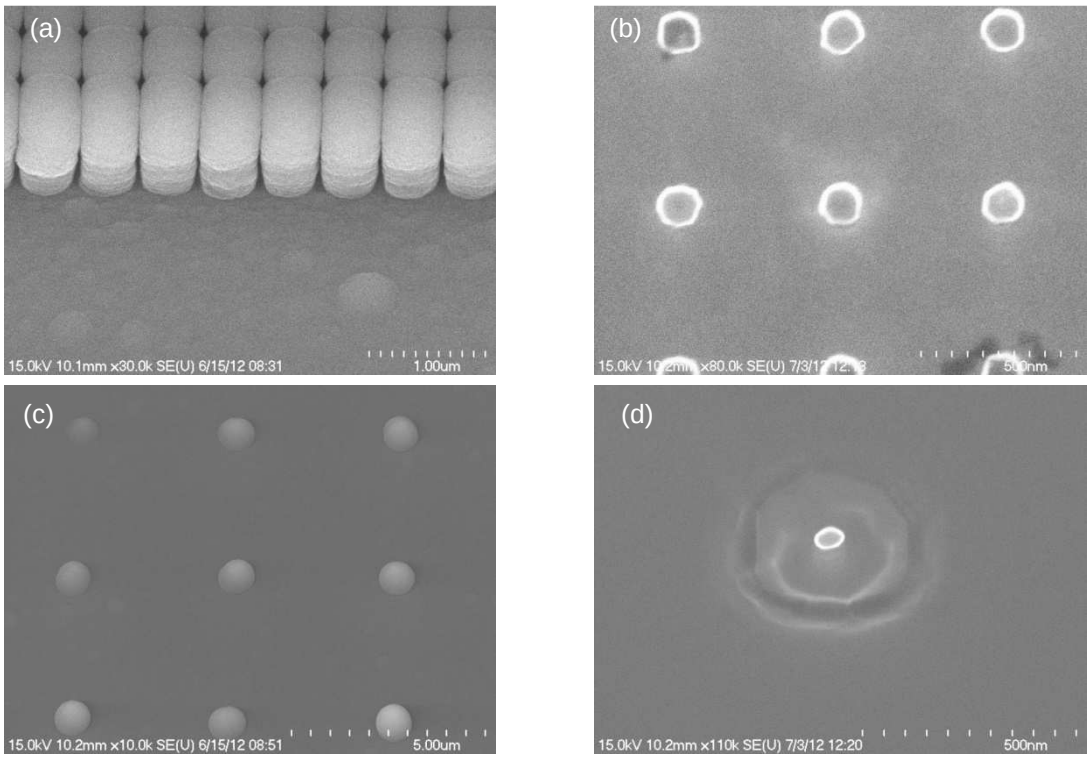


Figure 47. **(a), (c) Conformal oxide deposition on nanowire arrays of diameter (a) 100 nm and (c) 40 nm. (b), and (d) Nanowire tips exposed after CMP. The diameter of nanowires in (b) is 100 nm and in (d) it is 60 nm. The pitch of the array shown in (a) and (a) and (a) and (b) is 500 nm and in (c) and (d) the pitch is 4 micron.**

The thickness of the oxide layer deposited on the nanowires was 755-760 nm. After polishing, the oxide thickness was measured to be ~ 550 nm which gives an estimation of the length of the nanowires after polishing. Metal contacts were patterned and 80 nm thick layer of Ni was deposited using DC magnetron sputtering. The contacts were annealed at 270 C and 330 C in N_2 ambient for 100 sec each. *Figure 48* shows the contact pattern.

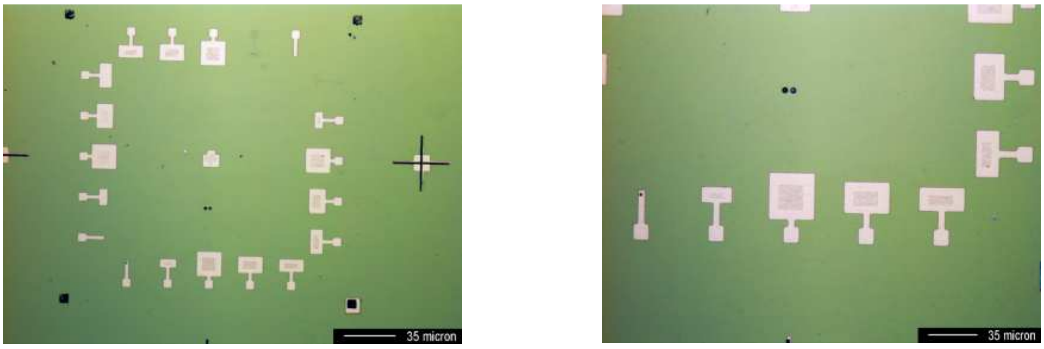


Figure 48. **Nickel contact pattern on (left) all nanowires and (right) 100 nm diameter nanowires.**

CHAPTER 5

ELECTRICAL MEASUREMENTS FROM VLS GROWN Ge NANOWIRES

5.1 Introduction

In this chapter the current versus voltage measurements on VLS grown Ge nanowire Schottky diodes is presented. The measurements were made using Agilent 4155C semiconductor parameter analyzer attached to a probe station. The sample was placed on a chuck having vacuum suction for ensuring good contact and the back of the substrate was grounded. DC voltage was swept on the metal contacts at the tip of the nanowire diodes by contacting with a tungsten probe and the current flowing through the devices was recorded. It is observed that the thermionic emission model is inadequate for explaining the current observed from the nanowire arrays. The ideality factors are close to 2 for all the arrays from which measurements have been recorded. For determining the reason behind the non-ideal conduction in these nanowires it is essential to understand factors the charges trapped in the dielectric, the distribution of defects on their surface and the effect of passivating the nanowire on its I-V characteristics. The Ge nanowires have a non-uniform and high doping which makes the analysis complicated because current can be conducted through thermionic emission as well as tunneling through the Schottky barrier. Moreover, the defects present on the surface of the diodes complicate the current even further. So, the current observed in the Ge and Si nanowire arrays is convoluted by recombination, tunneling and defects on the surface of the nanowires. Also, we do not have measured data from single nanowires of any diameter.

5.2 Electrical behavior of VLS grown Ge nanowire diodes

Before performing I-V measurements on nanowire diodes, we prepared planar Schottky diodes by sputter deposition of circular 0.8 mm diameter Ni contacts on n-type Ge substrates (ρ = 0.005-0.02 Ωcm). The thickness of the layer of Ni was 20 nm and after deposition rapid thermal annealing (RTA) was performed at 350 C for 1 min to form Ni germanide at the contacts. From these diodes, we extracted a Schottky barrier height of 0.5 eV, ideality factor of 1.5 and series resistance of 26 Ω. Planar Schottky diodes have been reported by forming germanide of Ni on the surface of n-type Ge wafers (Han et al., 2005), (Li et al., 2006), (Yao et al., 2006), (Dellas, Minassian, Redwing, & Mohney, 2010), (Gajula et al., 2011). In all these experiments, Ni was deposited on a clean Ge surface and annealed at temperatures in the

range of 300-500 C for 1 to 2 minutes. Low resistance Ni germanide films have been reported on p-type Ge by annealing the deposited Ni layer at 350-400 C for 60 sec (Spann et al., 2005). While fabricating metal contacts on Ge the Fermi level is pinned close the edge of the valence band (Dimoulas, Tsipas, Sotiropoulos, & Evangelou, 2006) because of which, the metal contacts on p-type Ge act as Ohmic and those on n-type Ge act as rectifying or Schottky contacts. The next step was to fabricate Ni germanide contacts on n-type Ge nanowires and observe their I-V behavior. The pattern shown in *Figure 49* was designed for Ni top contacts to the Ge nanowires.

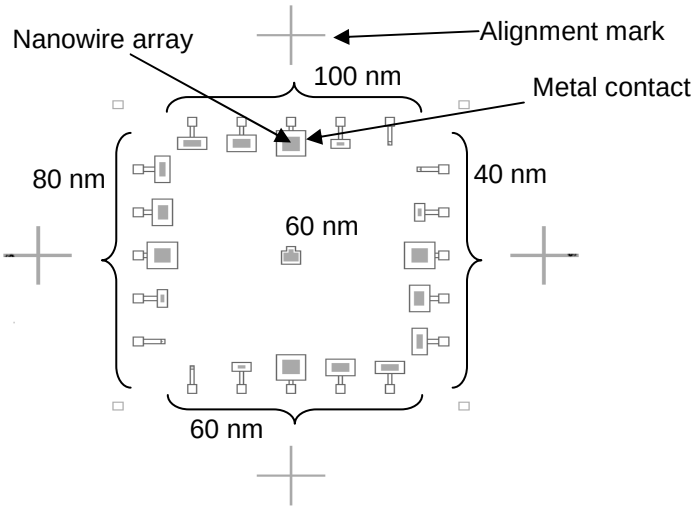


Figure 49. **Layout of the metal contact pattern over the nanowire arrays.**

The growth of Ni germanide in the axial direction on Ge nanowires has been reported in literature (Dellas et al., 2010). It has been observed in that work that axial segments of germanide up to 200 nm in length were formed after annealing at 350 C for 2 minutes. Following this approach, we deposited 80 nm thick Nickel layer using DC magnetron sputtering and annealed the contacts in two steps of 270 C and 330 C for 100 sec each, in a N_2 ambient. This resulted in the formation of Ni germanide on the tips of the nanowires which formed the Schottky barrier. The I-V characteristics of arrays of nanowires having different diameters are shown in the *Figure 50*.

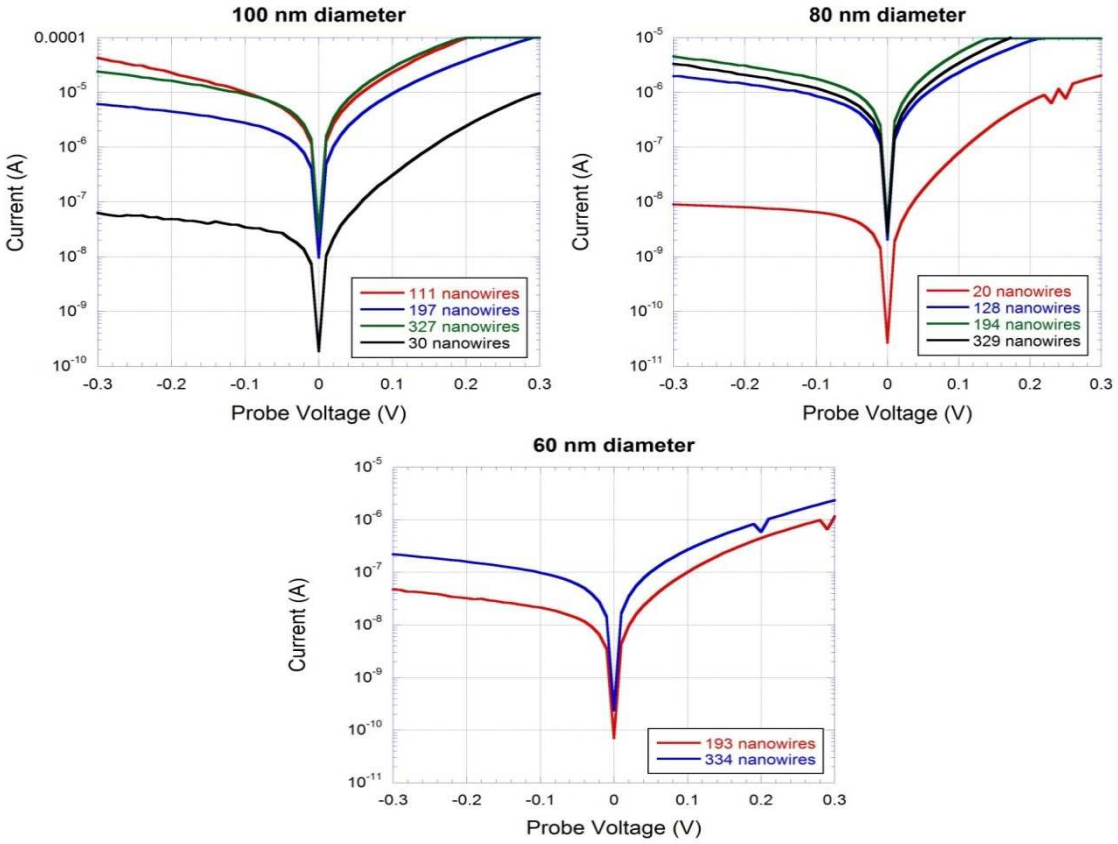


Figure 50. **Current vs. voltage characteristics of nanowire arrays having different diameters.**

5.3 Analysis of the I-V characteristics from VLS grown Ge nanowire diodes

In order to understand the measured electrical behavior of the nanowires, we first compared them to the Schottky thermionic emission model for planar diodes. The mathematical form of the model can be expressed as:

$$I = I_S(exp[q(V - Ir_S)/nkT] - 1) \tag{5.1}$$

$$I_S = AA^*T^2(exp[-(q\phi_B)/kT]) \tag{5.2}$$

Where, q = 1.6 × 10^{-19} C, k = 1.381 × 10^{-23} J/K, T = 294K, A is the diode contact area (assumed circular), and A^* is Richardson's constant, taken to be 112 A $cm^{-2}K^{-2}$. There are three parameters, namely Schottky barrier height (ϕ_B), ideality factor (n) and series resistance (r_S) in this model. Assuming that the diode is under forward bias and the exponential term in equation (5.1) is much greater than 1 we get the following expression

$$I \approx I_S \, exp[q(V - Ir_S)/nkT]$$

If the diode is biased in a region where the current is not limited by the series resistance r_S, the current can be expressed as follows

$$I \approx I_S \, exp[qV/nkT] \tag{5.3}$$

Taking the log base 10 on both sides of equation (5.3) yields:

$$\log(I) = \log(I_S) + \frac{(V)}{2.303nkT} \tag{5.4}$$

Equation (4.4) means that if the logarithm of current (*I*) through a Schottky diode under forward bias is plotted against the voltage (*V*) applied to it, the slope of the graph gives the ideality factor (*n*) and the y-intercept can be used to calculate the Schottky barrier height (ϕ_B) from the relation expressed in equation (5.2). The following values were extracted for these parameters from the I-V measurements. The series resistance shown in Table 3 has been extracted by performing a linear fit to the region of the forward bias I-V characteristics between 0.2 and 0.3 V shown in *Figure 50*.

Table 3

Thermionic emission model parameters extracted from Ge nanowire Schottky diodes

Diameter and no. of NW in layout (nm)	**Actual diameter (nm)**	**No. of NW contacted**	**Ideality factor (n)**	**Barrier height (ϕ_B) (eV)**	**Series resistance (Ω)**
60, 400	53	334	2.1	0.38	8.9×10^4
60, 240	53	193	1.8	0.4	8.6×10^4
80, 40	71	20	1.4	0.38	54.2×10^3
80, 160	71	128	2.0	0.31	11×10^3
80, 240	71	194	1.4	0.32	8.5×10^3
80, 400	71	329	1.9	0.33	3.4×10^3

100, 40	90	30	1.5	0.36	1.1×10^4
100, 160	90	111	1.9	0.27	902
100, 240	90	197	1.9	0.3	1.5×10^3
100, 400	90	327	2	0.29	10^3

The values of ideality factor, which should ideally be unity, are close to 2. This indicates a poor fit with the thermionic emission model. The main reason for this observation is the current being higher than the predicted value at low forward bias. Recombination in the space charge region and tunneling of electrons through the Schottky barrier are possible reasons for high current at low forward bias. Since these nanowires are highly doped and the doping concentration inside them is non-uniform, it is hard to say which of the two possible reasons dominates. We know that surface states play a major role in conduction of current through a nanowire because of its structure. Defects on the surface of the nanowires are expected to change the I-V characteristics from the ideal model. The measured I-V characteristics in *Figure 50* do not show a clear linear relationship between $\log_{10}$ (current) and voltage, thus the thermionic emission model alone is inadequate to explain these characteristics.

5.4 Simulation on a 3-D Ge nanowire structure for fitting the I-V characteristics

A three dimensional structure with a cylindrical mesh was created to represent a single n-type doped (10^{18} cm^{-3}) Ge nanowire encapsulated in SiO_2 using the Silvaco Atlas device simulator discussed in chapter 3 as shown in *Figure 51*. The purpose of the following simulations is to understand how charge carriers conduct current along the nanowire and the effect of introducing electrically active defects or traps on the surface of the nanowire on the I-V characteristics.

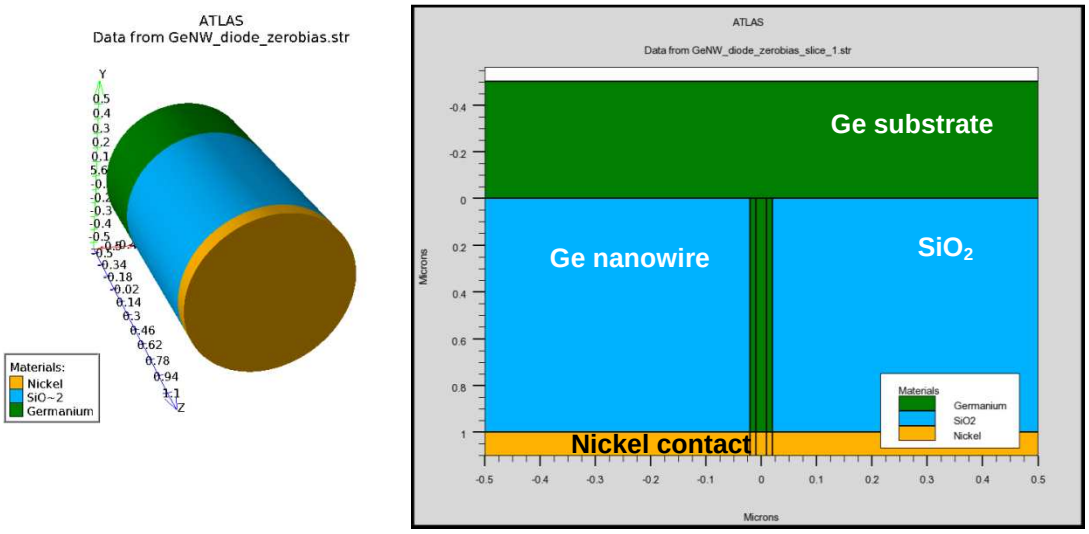


Figure 51. **Nanowire structure created in Atlas, (left) and cross section showing the nanowire encapsulated in SiO_2 (right).**

Spin-on-glass has can have positive trapped charges in it, which are expected to accumulate the surface of the nanowire. *Figure 52* shows the effect of the charge trapped in the dielectric and doping concentration on the electron concentration across the nanowire at the same forward bias voltage. The effects of fixed charge in the oxide are treated as an effective surface charge with sheet densities shown in *Figure 52*.

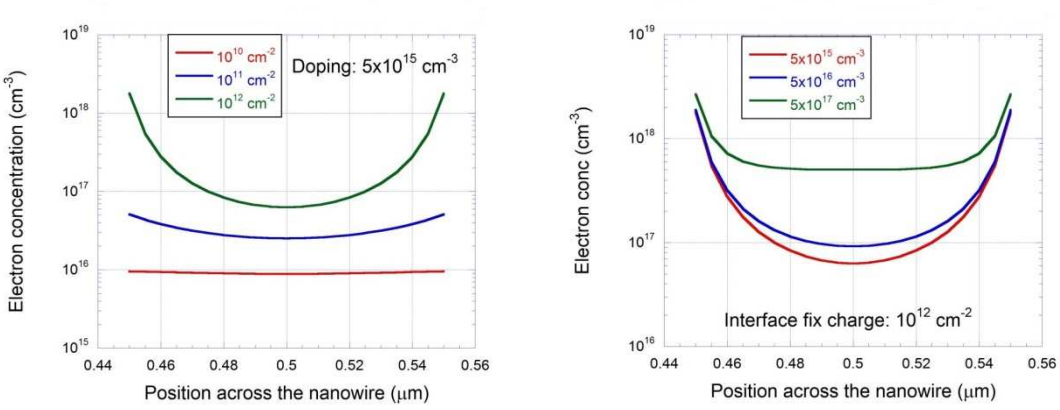


Figure 52. **Electron concentration across the nanowire as a function of fixed charge at the surface of the nanowire (left) and doping concentration (right) for a constant fixed charge on the surface of the nanowire.**

Both factors have a similar effect on the electron concentration, such that most of the electrons are accumulated near the surface of the nanowire.

The presence of traps on the surface of the nanowire can increase the current conducted by the device, especially at low forward bias, by introducing space charge created by trapping or emitting charge carriers. Traps also act as centers for recombination of electrons and holes. At low forward bias, electrons are more likely to recombine with holes injected from the metal contact via trap levels, than being emitted over the Schottky barrier. Thus, traps can increase the ideality factor of a diode. Due to the large ideality factors obtained by fitting the I-V characteristics of the nanowire diodes with the thermionic emission model, we made an attempt to fit the measured I-V characteristics using the density of traps on the surface of the nanowires as fitting parameters.

The location of these traps was set at the sidewalls of the nanowire and on the surface of the substrate on which it stands. In all the simulations, the capture cross-section of the traps is fixed at 10^{-15} cm^2. For modeling recombination inside the nanowire Shockley-Read-Hall (SRH) model is invoked and the carrier lifetime is fixed at 100 µs. This value is based on the range of hole lifetimes reported in the bulk of 10^{14} cm^{-3} doped n-type Ge substrates (Spitzer, Firle, Cutler, Shulman, & Becker, 1955). Hall mobility of charge carriers inside Ge at 300K as a function of doping concentration has been reported in literature (Debye & Conwell, 1954) according to which the expected electron mobility is 1000-2000 $cm^2V^{-1}s^{-1}$ for a doping of 10^{17}-10^{18} cm^{-3}. Electron and hole mobility is set at 3000 and 1000 $cm^2V^{-1}s^{-1}$ respectively in the simulations. This is an overestimation of the mobility as electrons inside nanowires suffer from surface scattering much more than in bulk Ge. Hence, we expect the simulated current to be higher than the measured current in the forward bias region supposed to be dominated by series resistance.

Before discussing the measured I-V characteristics, the effect of traps on the electron concentration, current density and the I-V characteristics of a nanowire diode are shown in *Figure 53*. The donor and acceptor traps are assumed to be mono-energetic with energy levels of 0.5 and 0.3 eV above the valence band respectively. The choice of the energy levels of the traps is arbitrary just for the purpose of observing the effect of the charge they introduce into the nanowire as a function of the voltage. The energy band gap of Ge is ~0.6 eV so, to have the donors close to the conduction band minimum would mean that most of them are positively charged and to have the acceptors close to the valence band maximum would mean that most of them are negatively charged at zero bias. The following figures show electron

concentration, and current density inside the nanowire change with introduction of defects and with the forward bias applied to the nanowire.

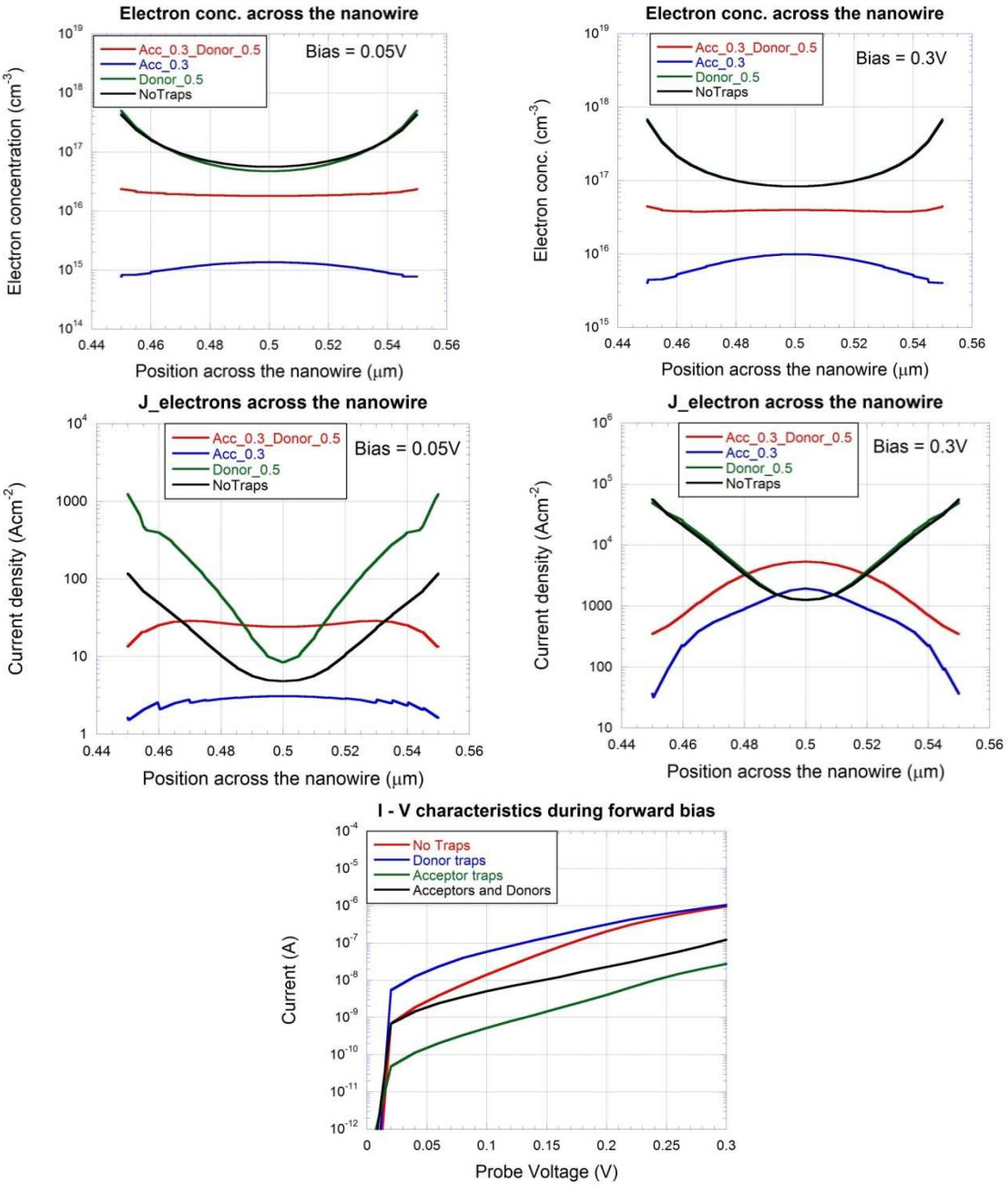


Figure 53. **Electron concentration and current density across the nanowire and I-V characteristics in the presence of both acceptor and donor traps.**

Acceptor traps introduce negative charge when they are occupied with electrons. The negative charge repels free electrons at the sidewalls of the nanowire which is reflected as a drop in concentration

across the nanowire cross section as shown in *Figure 53*. When the positive bias increases the electron concentration tends to increase but is still stays much lower than what it would be in the absence of acceptor traps. This change in electron concentration is directly reflected in the current density across the nanowire which is much lower on the nanowire surface compared to its core. Most of the electron current flows in the core of the nanowire when acceptor traps are present. With donor traps the opposite is true. Electron concentration increases on the sidewalls compared to the core of the nanowire and most of the current flows along the surface.

Finally, we present the results of fitting the I-V characteristics plotted in *Figure 50* measured from the Ge nanowire Schottky diodes.

Table 4

Parameters used to fit the forward bias I-V characteristics of Ge nanowire diodes

NW diameter and # contacted	**Doping conc. (cm^{-3})**	**Schottky barrier height (eV)**	**Acceptor trap density (cm^{-2})**	**Donor trap density (cm^{-2})**	**Acceptor trap energy level (eV)**	**Donor trap energy level (eV)**	**Interface trapped charge density (cm^{-2})**
100 nm, 30	5×10^{16}	0.45	10^{10}	10^{11}	0.3	0.5	5×10^{10}
100 nm, 111	5×10^{17}	0.38	10^{10}	2×10^{11}	0.3	0.5	8×10^{10}
100 nm, 197	10^{17}	0.42	3×10^{10}	3×10^{11}	0.3	0.5	10^{11}
100 nm, 327	4×10^{16}	0.33	5×10^{10}	5×10^{11}	0.3	0.5	10^{11}
80 nm, 20	10^{16}	0.5	10^{10}	10^{10}	0.3	0.5	5×10^{10}
80 nm, 128	10^{16}	0.48	6×10^{10}	10^{11}	0.3	0.5	10^{11}
80 nm, 194	2×10^{16}	0.48	5×10^{10}	9×10^{10}	0.3	0.5	10^{11}
80 nm, 329	10^{16}	0.48	8×10^{10}	9×10^{10}	0.3	0.5	10^{11}
60 nm, 193	10^{16}	0.48	4×10^{11}	10^{9}	0.3	0.5	5×10^{11}

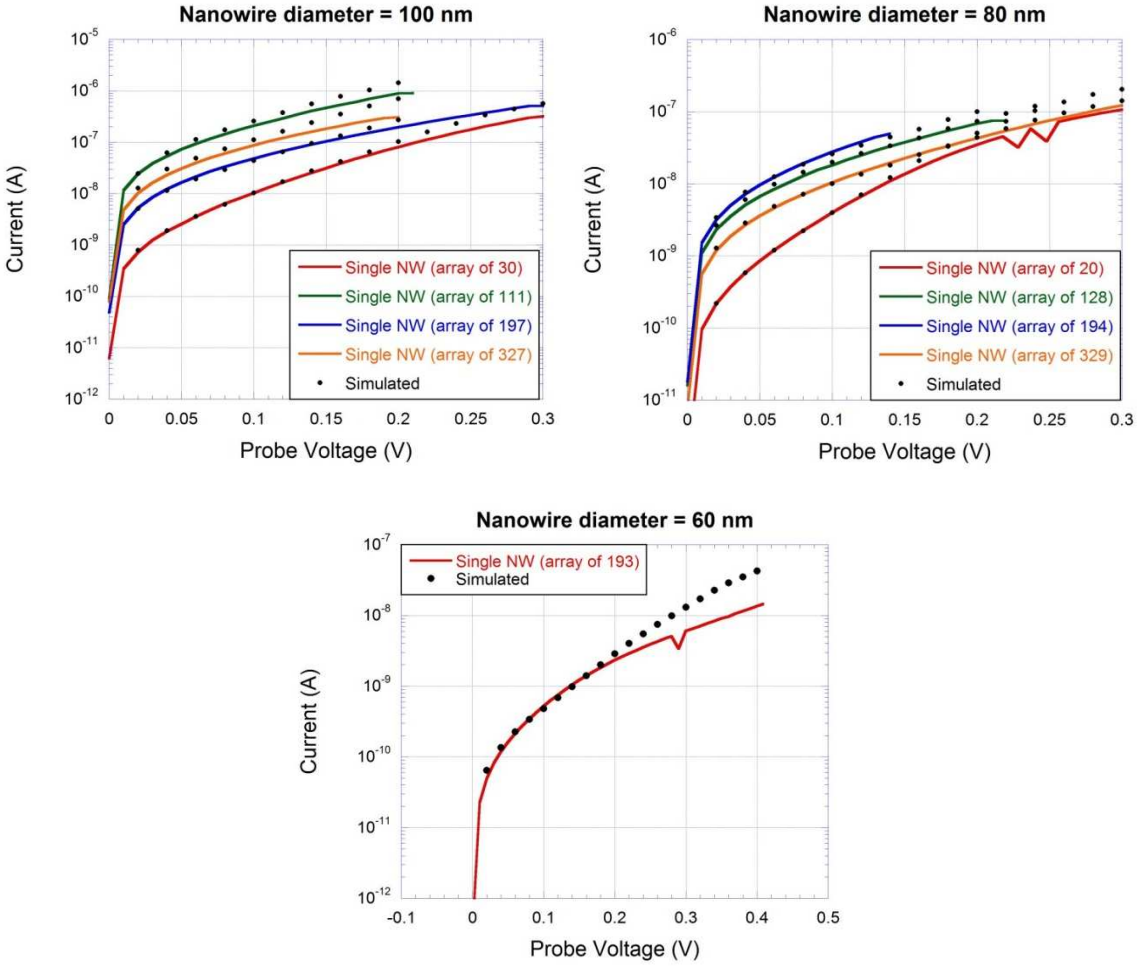


Figure 54. **Comparison between the current measured from arrays of n-type Ge nanowire diodes and the simulation after invoking traps at the surface of the nanowire and the substrate.**

Figure 54 presents a comparison between the current measured from different arrays of n-type Ge nanowire Schottky diodes and the simulations performed to fit the measured current using the density of traps at the surface of the nanowire and the substrate as fitting parameters.

At this point it is important to review the thermionic model parameters extracted from planar Ge Schottky diodes fabricated from Ni contacts on n-type (100) Ge substrates. At 25 C the Schottky barrier height of 0.58 eV and ideality factor of ~ 1.02 have been reported (Yao et al., 2006). The diodes were annealed at 400 C to form NiGe. In another study of Ni Schottky diodes on n-type Ge substrate barrier heights around 0.4 eV were reported for annealing temperatures between 300 and 500 C (Han et al., 2005). Planar Ni Schottky diodes on n-type Ge substrates with ideality factor ~ 1.1 and barrier height 0.63 eV have

been reported (Gajula et al., 2012). These diodes were annealed at 300 C in Nitrogen ambient. Thus, we observe that in literature the ideality factors of planar NiGe Schottky diodes are close to 1 indicating a good fit with the thermionic emission model. The barrier heights reported are also close to 0.6 eV which are higher than what we extract from the nanowire diodes fabricated in this study. This suggests that thermionic emission model is not adequate for predicting the current through vertically oriented nanowire Schottky diodes.

5.5 Current-voltage measurements from vertically etched Si nanowires

The result of I –V measurements on the n-type doped Si nanowire diodes fabricated using vertical etching is shown in *Figure 55*.

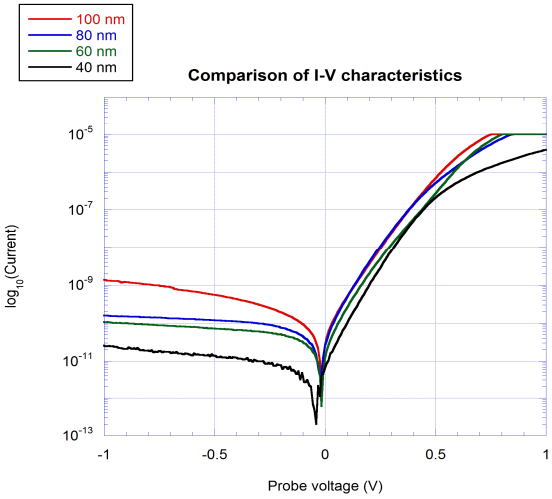


***Figure 55.* I-V characteristics of an array of 400 nanowires of different diameters.**

The I-V characteristics shown in *Figure 55* have been compared with the thermionic emission model for bulk Schottky diodes and the barrier height (ϕ_B), ideality factor (n) and series resistance (r_S) were extracted. Equations (5.1) and (5.2) represent the thermionic model and we use the procedure described in section 5.3 to extract the thermionic model parameters from the measured I-V characteristics as shown in Table 5.

Table 5

Parameters extracted from diode I-V characteristics

Size	40 nm	60 nm	80 nm	100 nm
n	1.85	2.6	1.42	2.01
ϕ_B (eV)	0.683	0.623	0.603	0.554
r_s (kΩ)	88.6	53.3	31.1	24.2

Nanowires are structures in which surfaces play a major role in conduction of current because of their structure. Hence, we observed the relationship between the $\log_{10}$ (current) vs. $\log_{10}$ (radius) of the nanowires. Three arrays of nanowires having the same number of nanowires but each having nanowires of different diameter (40, 60 and 100 nm) were chosen. The graph plotted in *Figure 56* shows the trend.

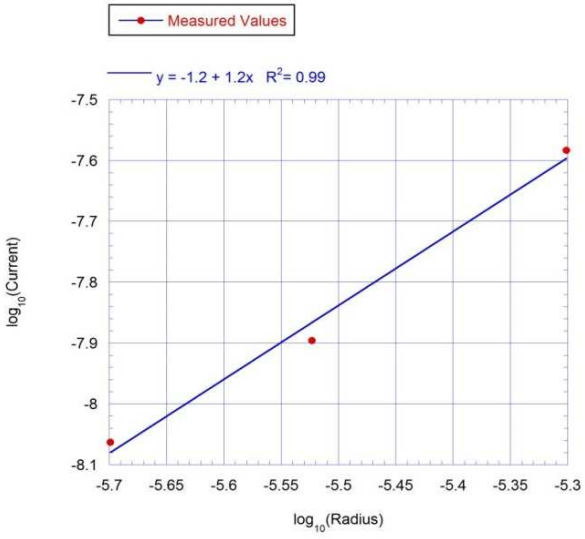


Figure 56. **Logarithmic dependence of current on the radius of the nanowires.**

The trend shows a slope of 1.2 between $\log_{10}$ (current) and $\log_{10}$ (radius) of the nanowires indicating that the current depends on the diameter more than the area of the diode. This indicates that the surface of the nanowires plays a major role in conduction of current through the device which is a big difference from planar diodes. Another comparison is made in between the current conducted by arrays having different number of nanowires. This comparison is not a direct one because there were differences

in the Schottky barrier height, ideality factor and series resistance extracted from arrays having different numbers of nanowires having the same diameter. So, the current was adjusted according to an additional scaling factor apart from the number of nanowires, which depends on the difference in the values of the above mentioned parameters. *Figure 57* shows the results of the comparison.

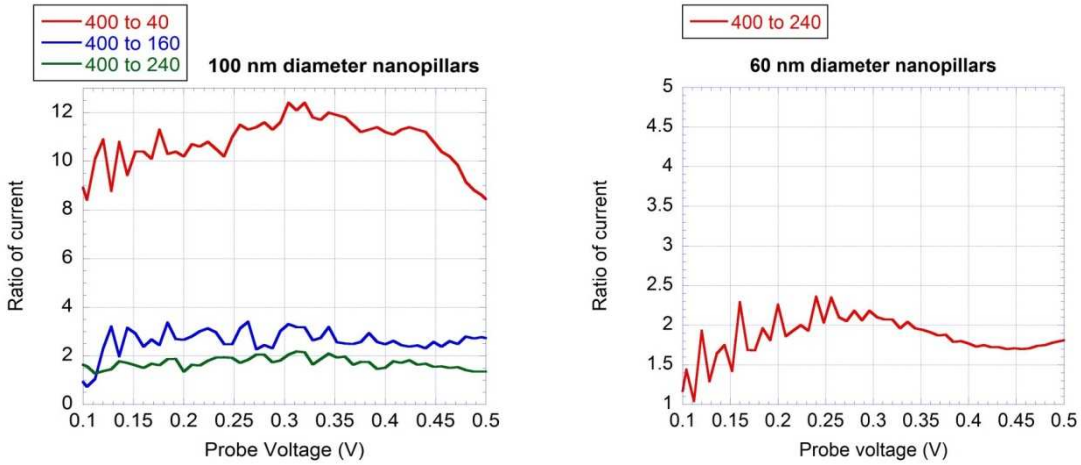


Figure 57. **Ratio of current values for different number of nanowires contacted for 100 nm and 60 nm diameter nanowires.**

The number of nanowires mentioned in each figure is according to the layout shown in *Figure 49.* We observe that the ratio of current conducted by arrays having different number of nanowires having the same diameter is consistent with the expected value.

CHAPTER 6

EFFECT OF SURFACE PASSIVATION ON THE ELECTRICAL CHARACTERISTICS OF SILICON NANOWIRE DIODES

6.1 Introduction

This chapter focuses on studying the effect of surface passivation on the electrical characteristics of Si nanowires fabricated using reactive ion etching. The Si substrates used for creating the nanowires were n-type doped to 10^{15} cm^{-3}. In the previous chapters the importance of the surfaces of the nanowire has been highlighted. After simulating the n-type Ge nanowire Schottky diodes mentioned in the previous chapter it was observed that most of the current flows close to the surface of the device. The dielectric (spin-on-glass) encapsulating the nanowires has charge trapped inside it. Since the contact to the tip of the nanowire is much bigger in area compared to its cross section, electric field lines arising from the top wrap around the surface of the nanowire due to its geometry. The mobility inside a nanowire is considerably less than the bulk semiconductor because of scattering due to defects present on the surface of the nanowire. These defects can not only act as scattering centers but can also introduce fixed charge by trapping charge carriers. The combined effect of the above factors is a deviation from the ideal Schottky diode characteristics which are described by the thermionic emission model. Surface passivation changes the magnitude and polarity of fixed charge present on the surface of the nanowire by satisfying the dangling bonds which would otherwise act as charge trapping and scattering centers.

In this chapter our purpose is to observe and make an attempt to understand the effect of surface passivation on the electrical characteristics of Si nanowire Schottky diodes. We have studied the differences between un-passivated, thermal oxide passivated and amorphous Si passivated nanowire diodes. The chapter starts with prior research about the effect of surface passivation on the electrical behavior of Si nanowires and membranes. Then the process used to fabricate the Si nanowire diodes is presented. In the next section the I-V characteristics measured from these diodes are analyzed using the thermionic emission model. In order to understand the significance of surface charge on the I-V characteristics, forming gas anneal was performed on all the nanowire diodes. The changes before and after annealing, are presented. The most significant change in electrical behavior was observed for thermal oxide passivated nanowires. C-

V measurements were performed to explain the I-V characteristics. In the next section, the current measured from the nanowire diodes is modeled in Silvaco Atlas simulator using the density of electrically active traps at the nanowire surface, as fitting parameters. The final section serves as a conclusion to summarize all the inferences drawn from the experimental results presented in this chapter.

6.2 Surface states and surface recombination velocity in Si nanowires

In any nanowire structure the surface plays a key role in determining the overall electrical characteristics of the device. This is mainly because of the small number of atoms contained within the volume of the nanowire and the comparatively larger number of atoms exposed on the surface area of the device. As a result, surface scattering and surface recombination of charge carriers has always been a concern in nanowires. Several research groups have studied about the chemical and electrical properties of nanowire surface, especially Si nanowires. The mobility of charge carriers inside the nanowire is affected by scattering and recombination at the surface, as well as at the electrical contacts. Transconductance measurements performed on back-gated, horizontal intrinsic Si nanowires have reported a mobility of 5.9 x 10^{-3} $cm^2V^{-1}s^{-1}$ and those on heavily p-type doped Si nanowires have reported a mobility of 3.17 $cm^2V^{-1}s^{-1}$ (Cui, Duan, Hu, & Lieber, 2000). Another study in which similar measurements were made on n-type Phosphorus doped Si nanowires reported mobility values of around 100 $cm^2V^{-1}s^{-1}$ for moderately doped (Si/P ratio 1000) and around 250 $cm^2V^{-1}s^{-1}$ for highly doped (Si/P ratio 4000) nanowires (Zheng, Lu, Jin, & Lieber, 2004). In both the studies, the nanowire surfaces had just a layer of native oxide. The nanowires reported in the above studies were grown using the vapor–liquid–solid (VLS) epitaxy approach, which yields nanowires with relatively smooth sidewalls compared to the top-down approach where nanowires are etched from the substrate using a hard mask. The etching can be wet (e.g. metal assisted chemical etching MACE) or dry (vertical ICP etching). In any case, the mobility of charge carriers in etched nanowires is expected to be lower than in case of VLS grown nanowires. Si nanowires with H-terminated surfaces obtained by HF treatment have been reported to have a mobility of around 1.83 $cm^2V^{-1}s^{-1}$ for nanowires etched from an intrinsic and 4.67 $cm^2V^{-1}s^{-1}$ for those etched from a n-type doped (~ 10^{15} cm^{-3}) Si substrates (C. Guo et al., 2009).

In addition to reducing the mobility, the defects at the surface of etched nanowires also introduce traps which add fixed charge to the nanowire by trapping charge carriers. The type of traps (acceptors / donors) and their energy distribution within the energy band gap is a function of several factors including but, not limited to the type of passivation on the surface, the recipe followed for etching, the dielectric surrounding the nanowire, etc. The density of traps and the amount of fixed charge introduced by them on the nanowire surface strongly affects the surface recombination velocity. Based on the charge introduced by the defects on the surface, the conductivity of the nanowire can be severely affected. Two-probe current measurements performed on back-gated Si nanowires formed using wet etching from a p-type substrate showed the effect of surface passivation on the type of conductivity in the nanowires (Lee et al., 2011). Thermal oxide covered nanowires showed p-type conductivity. However, on removal of the oxide using HF, obtaining H-terminated surface, the nanowires showed n-type conductivity. The authors justified this observation by the fact that previous research has reported Fermi level pinning near the conduction band after H-termination of a Si surface.

A similar observation has been reported for thin SOI membranes doped p-type with a concentration of $\sim 10^{15}$ cm^{-3} (Scott et al., 2009). After treatment with HF, Hall voltage measurements indicated the conductivity to be n-type with a concentration of 1.3×10^{14} cm^{-3}. The reason for this observation was reported to be Fermi level pinning 0.32 ± 0.03 eV below the conduction band minimum. The negative charge introduced at the surface caused the sheet to be inverted and behave as n-type. When the thickness of the layer was increased to 220 nm and the doping was increased to $\sim 10^{19}$ cm^{-3}, the conductivity remained p-type even after HF treatment as the negative charge at the surface was unable to change the conductivity of the layer. The nature of surface states which can be manipulated through chemical reactions has also been reported to change the conductivity of Si nanowires (Haick, Hurley, Hochbaum, Yang, & Lewis, 2006). The surface passivations were native oxide, hydrogen termination and methyl group termination. These nanowires were grown by bottom-up VLS growth and the p-type doping was $\sim 10^{17}$ cm^{-3}. The conductance of these nanowires was measured by two-point and four-point probe measurements while they were laid down horizontally on a thermally oxidized degenerately doped p-type Si substrate. The nanowires demonstrated p-type conductivity in all three cases but the changes in

conductivity with back gate voltage were maximum in case of methyl group-terminated nanowires and least in case of SiO_2 passivated nanowires. This indicates that defects at the nanowire surface due to SiO_2 growth trap and scatter more charge carriers through surface states as compared to the H and methyl group termination. The mobility extracted from conductance measurements was maximum (~130-140 $cm^2V^{-1}s^{-1}$) for methyl group termination, 90-120 $cm^2V^{-1}s^{-1}$ for H-terminated and minimum (~15-20 $cm^2V^{-1}s^{-1}$) in the case of SiO_2 passivated Si nanowires.

The effect of fixed charge introduced by traps on the surface of Si nanowires can be engineered to produce a p-n junction type of structure (C. Guo et al., 2009). First, the authors present the results of two probe measurements with back gate voltage applied to H-terminated n-type doped Si nanowires laid horizontally on an oxidized Si wafer. P-type conductivity was observed proving that H-termination creates surface states that capture electrons and produce negative fixed charge. Using this idea, the authors presented a process to form p-n junction nanowires by switching the passivation from H-termination to SiO_2 along the length of the nanowires. Si nanowires were etched from a n-type doped substrate (~10^{15} cm^{-3}) using metal assisted chemical etching (MACE). They were thermally oxidized to cover the nanowires in SiO_2 and spin-coated with PMMA. Almost half of their length from the top was exposed by etching the PMMA in Acetone and the oxide covering that part was removed in HF yielding a H-terminated surface. Thus, the nanowire had H-terminated Si surface along half of its length and an oxidized surface on the other half. Au was deposited by tilting the sample at 60 degrees to make sure that metal was deposited only on the tip of the nanowires. Ti/Au was deposited on the back of the Si wafer to serve as the other contact. On making contact to individual nanowires from the top, rectifying behavior was observed with the top segment behaving as p-type and the rest of the nanowire as n-type. This study emphasizes the fact that in Si nanowires, the effect of surface traps is much more dominant than in case of bulk Si.

The surface conditions have been found to dominate over the effect of impurities present inside the bulk of the nanowire in determining the lifetime of charge carriers for electrical measurements (Allen et al., 2008). Si nanowires grown using the Au catalyst assisted VLS approach were measured using the electron beam induced current (EBIC) technique in order to determine the minority carrier diffusion length. The diffusion length did not saturate with increase in diameter of the nanowires up to 100 nm and indicated

a surface recombination velocity of ~3 x 10^5 cms^{-1} which can be translated into a surface defect density of ~1.7 x 10^{13} cm^{-2}. Due to the presence of the Au catalyst it can be argued that Au might be responsible for acting as a deep level trap; however, the concentration of Au atoms inside the nanowire was experimentally determined to be less than 5 x 10^{17} cm^{-3} which the interface state density is high enough to overcome. Thus, it was concluded that the surface recombination velocity determines the lifetime of the charge carriers in Si nanowires.

6.3 Process of fabrication

The Si nanowires used in this study were fabricated by vertical dry etching using a Surface Technology System (STS) inductively coupled plasma (ICP) system. N-type doped Si substrates with a doping concentration of 10^{15} cm^{-3} were spin coated with 4% 950k PMMA mixed in Anisole. Rectangular features were created in the resist using electron beam lithography. There were four different edge lengths (100 nm, 80 nm, 60 nm and 40 nm) of these squares which were patterned in the resist. After developing the pattern, a 50 nm thick layer of SiO_2 was deposited using electron-beam evaporation and after lift-off, SiO_2 squares were left on the Si substrate. These squares were used as hard mask for etching the Si, which resulted in approximately 1 micron tall nanowires. *Figure 58* shows a schematic of the fabrication process with the sequence of steps explained below.

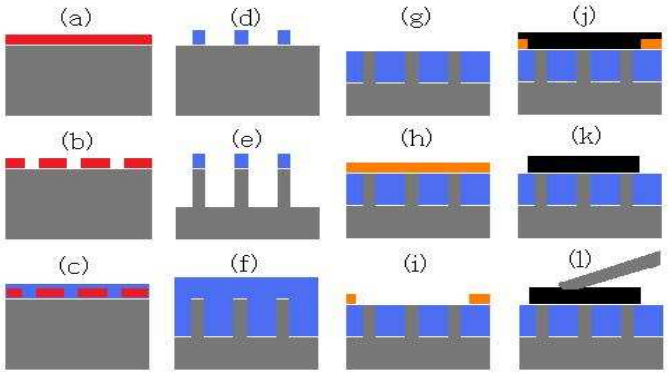


Figure 58. **Schematic illustration of the fabrication process for creating Si nanowires.**

(a) A 200 nm thick layer of PMMA is spin-coated on to a n-type Si substrate (doping 10^{15} cm^{-3}).

(b) Square-shaped features patterned on the PMMA coated substrate using electron beam lithography.

(c) A 50 nm thick layer of SiO_2 was deposited over the patterned substrate using electron beam evaporation.

(d) Square-shaped SiO_2 features with edge lengths measuring 100 nm, 80 nm, 60 nm and 40 nm were obtained after lift-off.

(e) Vertical dry etching resulted in creation of Si nanowires with remnants of the SiO2 hard mask on their tips.

(f) SiO_2 hard mask was removed from the nanowire tips using 20:1 buffered oxide etchant and they were encapsulated in spin-on-glass (SOG) with thickness matching with the length of the nanowires.

(g) Dry etching of the SOG was performed to remove excess oxide and reveal the tips of the nanowires.

(h) Once again, 200 nm thick PMMA was spin-coated to create the pattern for metal contacts on the tips of the nanowires.

(i) Metal contact pattern was developed creating openings in the resist where Ni will contact the nanowire tips.

(j) A 65 nm thick layer of Ni was deposited using DC magnetron sputtering on the metal contact pattern.

(k) After lift-off metal contacts to the Si nanowires were obtained and RTA was performed to form silicide which concluded the formation of the Schottky diodes.

(l) Electrical measurements were performed on nanowire arrays containing different number of nanowires by lowering one probe on top of the metal contact and using the Si substrate as the other contact.

At this point, it is worthwhile mentioning the recipe of dry etching followed here because that is the most critical step developed in this entire process. The etching was basically a Bosch process, where alternating cycles of etching and deposition were used. The durations of etching and deposition were different for the three samples fabricated here, in order to observe the effect of different etch processes on the shape of the nanowires. Other than those factors, the following process flow was followed:

Etching:

- SF_6 + CHF_3 with flow rates of 65 and 35 sccm respectively.

- Chamber pressure = 10 mTorr.
- RF power: platen = 10 W, coil = 600 W.

Deposition:

- CHF_3 with flow rate of 70 sccm.
- Chamber pressure = 10 mTorr.
- RF power: platen = 0 W, coil = 600 W.

Three samples were prepared for this study. The Si nanowires on the first sample were passivated by a thermally grown oxide up to a thickness of 21 nm. The second sample was passivated by deposition of amorphous Si using CVD up to a thickness of 30 nm. The third sample was left un-passivated to be used as a reference. These samples will henceforth be addressed as Si #1, Si # 2 and Si # 3 respectively in the remaining part of this chapter. The durations of etching and deposition during vertical etching for the three samples are mentioned in Table 6.

Table 6

Durations of etching and deposition cycles for etching the Si nanowires

Sample ID	**Etch duration (sec)**	**Deposition duration (sec)**	**Total # of cycles**
Si # 1 (Thermal oxide 21 nm)	8	5	10
Si # 2 (a-Si 30 nm)	7	5	11
Si # 3 (un-passivated)	6	5	15

The SEM images representative of the nanowires on these three samples are shown in *Figure 59*.

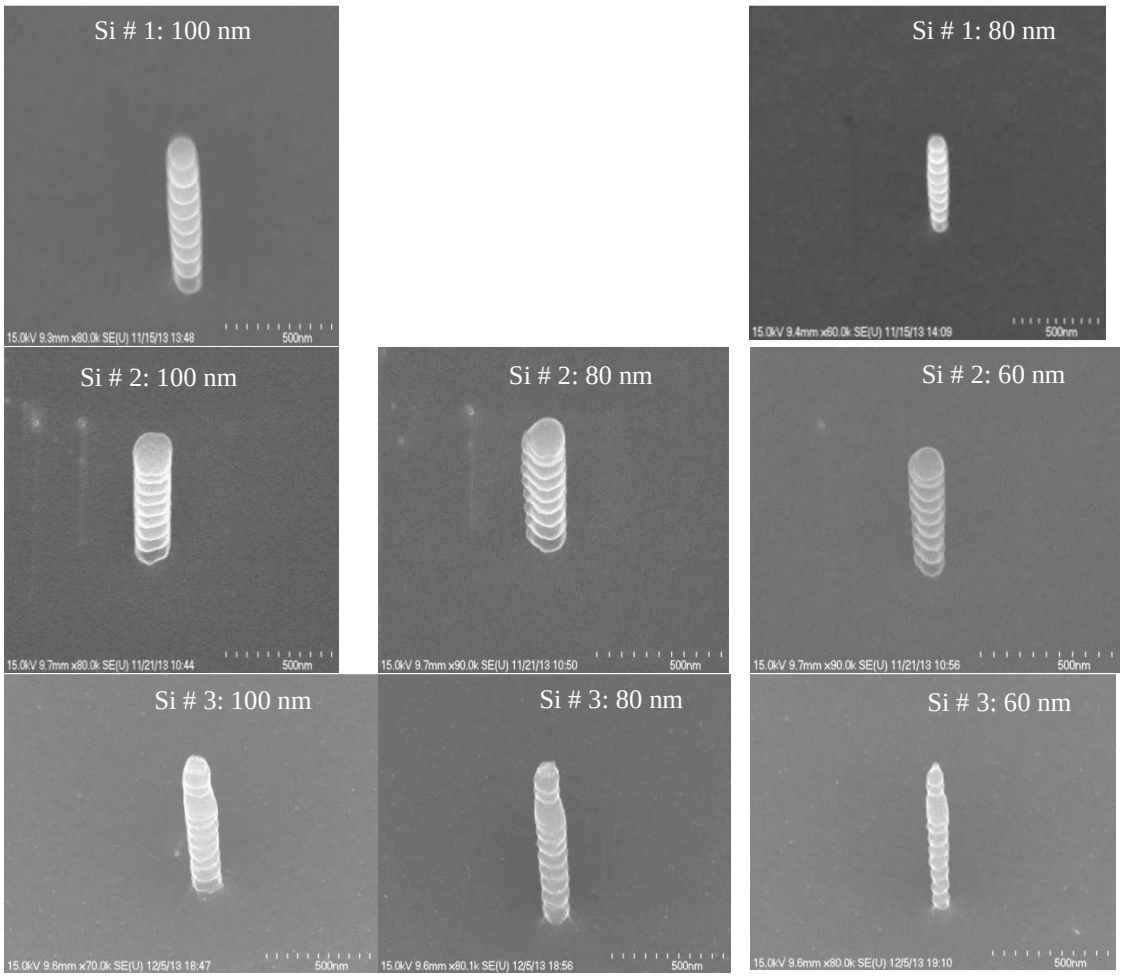


Figure 59. **SEM images of Si nanowires etched using recipes having different etching and deposition times.**

The first recipe (Si # 1), was unable to yield 60 nm nanowires because of excessive undercutting. For the second recipe (Si # 2), the 60 nm diameter nanowires were fine but the 40 nm nanowires were again lost due to undercutting, which is already evident from the shape of the 60 nm diameter ones. Therefore, for the final sample, the etching time was reduced to 6 sec and nanowires of all four diameters were obtained. However, during further processing the 40 nm diameter nanowires were lost because there was still some undercutting at that diameter which could not be prevented just by adjusting the durations of etching and deposition.

Figure 60 shows a photograph of the Ni contacts to the tips of the Si nanowires. Each side of the pattern has five contacts which are connected to arrays having different numbers of nanowires of same

diameter. Each side represents one of the four diameters (100 nm, 80 nm, 60 nm and 40 nm) designed in the layout.

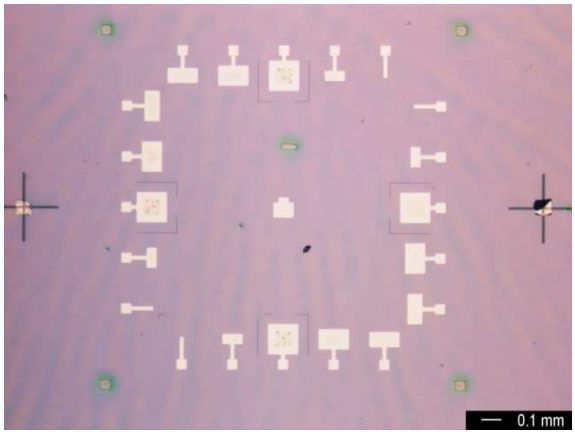
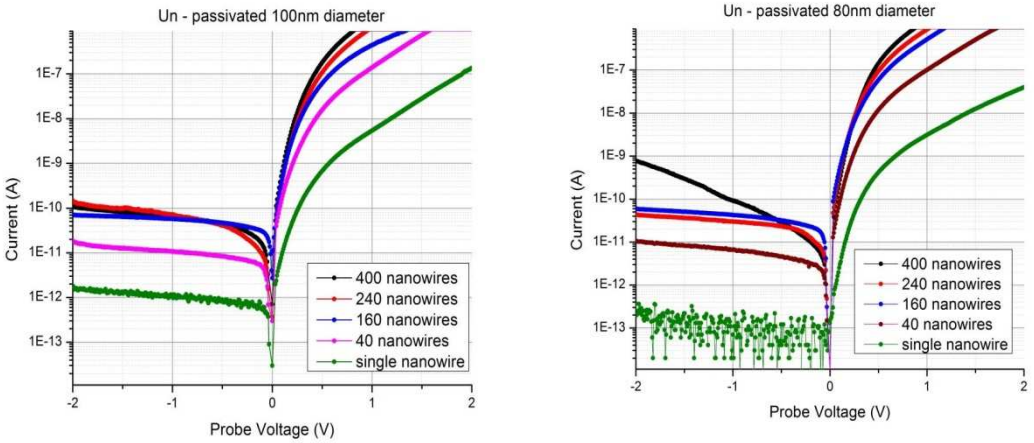


Figure 60. **Nickel top contacts to the Si nanowires.**

6.4 Electrical measurements on the Si nanowire Schottky diodes

Current versus voltage measurements shown in *Figure 61*, *Figure 62* and *Figure 63* were performed on the Si nanowires using an Agilent 4155C parameter analyzer. Voltage was applied at the top contacts, the back of the substrate was grounded and current flowing through the nanowire arrays was recorded.



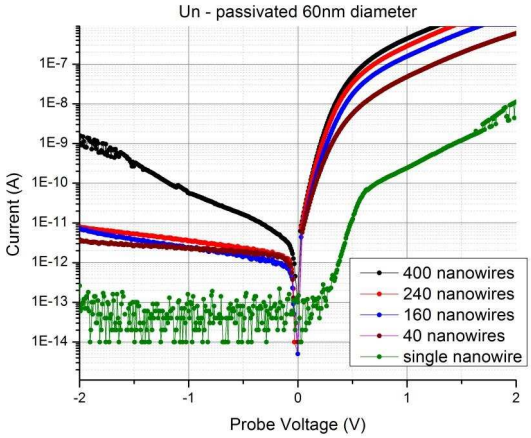


Figure 61. **Electrical characteristics measured from un-passivated Si nanowire Schottky diodes for three different diameters.**

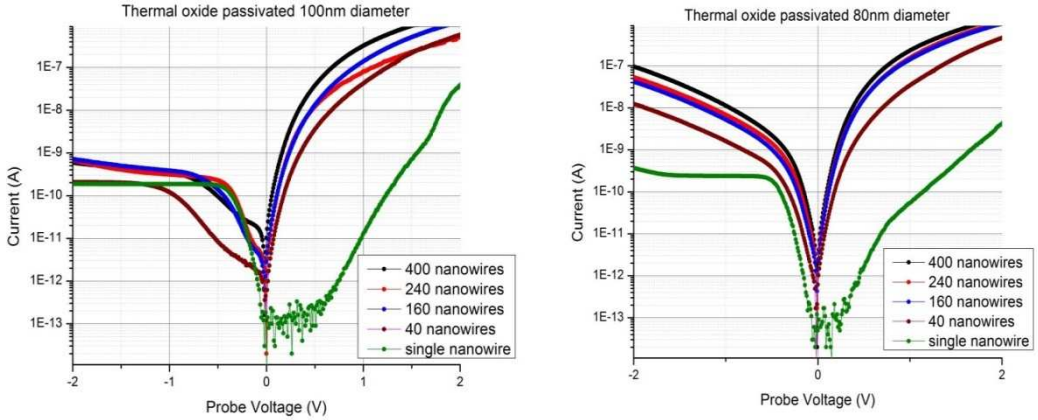


Figure 62. **Electrical characteristics measured from Si nanowire Schottky diodes passivated with 21 nm thick thermal oxide.**

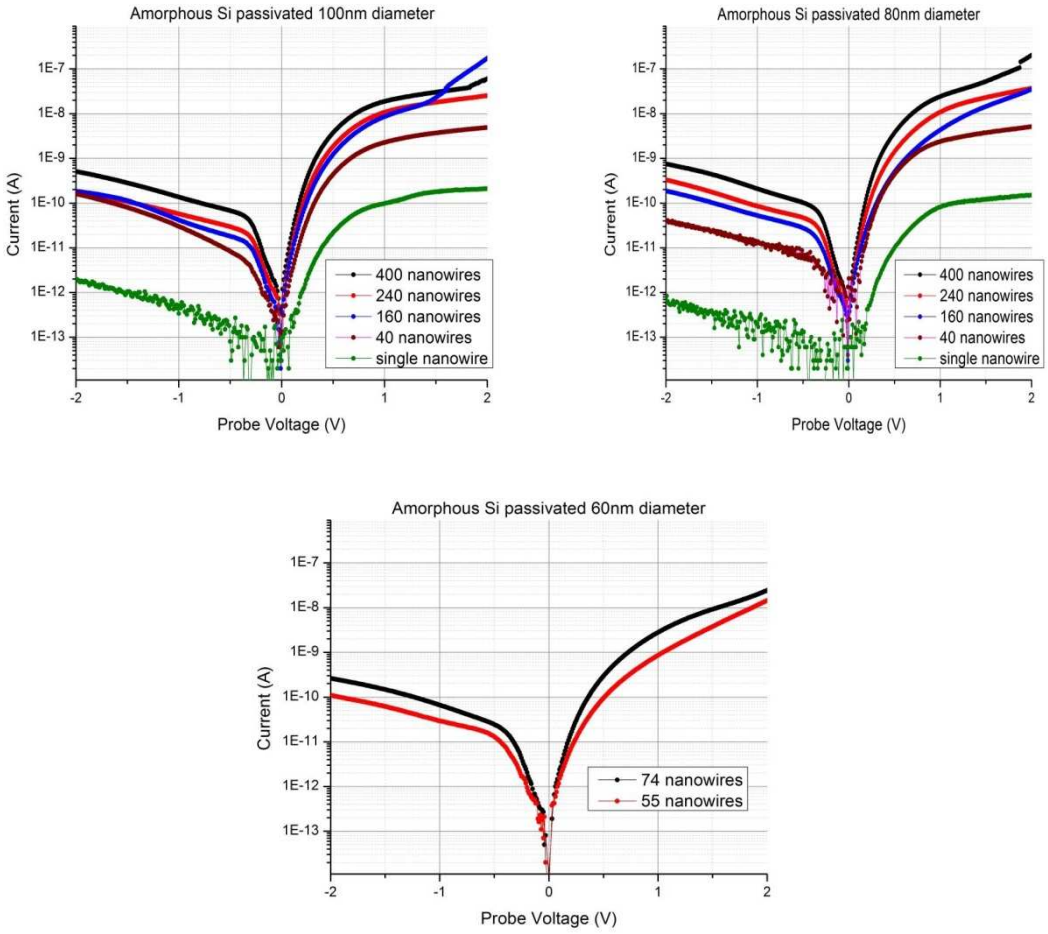


Figure 63. **Electrical characteristics measured from Si nanowire Schottky diodes passivated with 30 nm thick amorphous Si.**

Using the procedure discussed in chapter 5 in section 5.3, an attempt was made to fit the forward bias current of the diodes to the thermionic emission model and the parameters extracted are given in Table 7, Table 8 and Table 9. The range of voltages used for extraction of the following parameters was between 0 V and 0.5 V as series resistance can usually be neglected at low forward bias.

Table 7

Thermionic emission parameters extracted from un-passivated nanowire diodes

Diameter (nm)	**No. of nanowires contacted**	**Schottky Barrier Height (ϕ_B)**	**Ideality factor (n)**
100	400	0.59	1.5
	240	0.59	1.5
	159	0.58	1.6
	40	0.55	1.9
	1	0.53	2.0
80	400	0.61	1.4
	240	0.58	1.5
	158	0.55	1.8
	40	0.57	1.7
	1	0.56	1.6
60	398	0.63	1.4
	240	0.62	1.5
	160	0.62	1.5
	40	0.58	1.7
	1	0.7	1.9

Table 8

Thermionic emission parameters extracted from thermal oxide passivated nanowire diodes

Diameter (nm)	**No. of nanowires contacted**	**Schottky Barrier Height (ϕ_B)**	**Ideality factor (n)**
100	400	0.6	1.7
	240	0.64	1.5

	160	0.61	1.7
	40	0.62	1.6
	1	0.72	3.9
80	400	0.63	1.5
	240	0.62	1.5
	160	0.62	1.5
	40	0.61	1.6
	1	0.64	3.8

Table 9

Thermionic emission parameters extracted from amorphous Si passivated nanowire diodes

Diameter (nm)	**No. of nanowires contacted**	**Schottky Barrier Height (ϕ_B)**	**Ideality factor (n)**
100	400	0.68	1.6
	240	0.69	1.5
	160	0.68	1.7
	40	0.66	1.7
80	398	0.68	1.5
	238	0.68	1.6
	159	0.67	1.8
	39	0.64	2.1
	1	0.61	3.1
60	74	0.65	1.9
	55	0.65	2.3

Although there is a fluctuation in the measured values, on the average, the thermionic emission model parameters show that the Schottky barrier height for amorphous Si passivated nanowires is the

highest, followed by thermal oxide passivated ones and the lowest barrier height is found for un-passivated nanowires. The ideality factors range between 1.5 and 2 for the nanowire arrays and even go up to ~ 3 for single nanowires indicating a poor fit with the thermionic emission model. Planar Schottky diodes formed by depositing Ni contacts on Si substrates have been reported to yield an ideality factor around 1.03 and barrier heights of ~ 0.7 eV (Coe & Rhoderick, 1976). The ideality factors extracted from nanowire diodes fabricated here indicate that the thermionic model alone is not adequate to predict the current through these devices. The barrier heights extracted here for amorphous Si passivated nanowire diodes are closest to those reported for planar diodes.

Based solely on the barrier heights extracted from the Schottky model, one might be encouraged to qualitatively conclude that the better the surface passivation, the higher the barrier height and thus, surface passivation has an effect on the barrier height of nanowire diodes. For planar diodes, it is well known that the barrier height is specific for a certain combination of a metal and semiconductor irrespective of the doping concentration because of Fermi level pinning at the interface of the two. The surface states created at the metal-semiconductor interface are the cause of this pinning. In the case of nanowire diodes, the electrically active defects at the nanowire surface are even more likely to affect the current than in planar diodes. Also, the ideality factors being greater than 1 are evidence that the fit with thermionic emission model is not a good basis for understanding the I-V characteristics of these diodes.

Apart from charge arising due to defects at the surface of the nanowire, there is also some fixed charge trapped inside the spin-on-glass as well. In order to determine the density of charge trapped in the spin-on-glass (SOG), we conducted capacitance measurements on a MOS structure fabricated by spin-coating SOG on a Si substrate and depositing Al contacts on top. Due to the thickness of the SOG (~530 nm), the amount of trapped charge was high and we could not observe the full C-V curve from inversion to accumulation but from the data we gathered, the charge was found to be positive with an estimated density of 10^{11} ~10^{12} cm^{-2}. The C-V curve obtained from a 530 nm thick SOG layer on a p-type doped Si substrate (~10^{15} cm^{-3}) is shown in *Figure 64*.

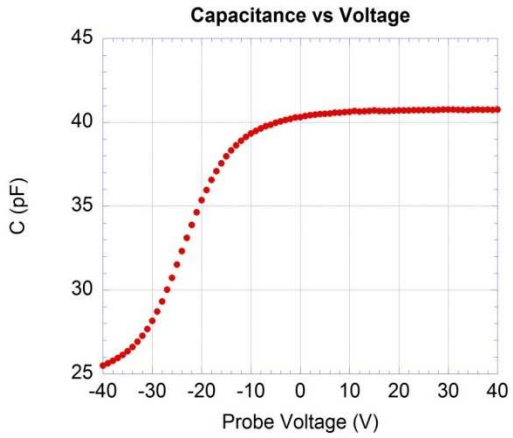


Figure 64. **Capacitance vs. voltage curve of a 530 nm thick layer of SOG on a p-type doped Si substrate.**

6.5 Effect of forming gas anneal on the I-V characteristics

Forming gas anneal (FGA) passivates dangling bonds on the surface of Si leading to re-arrangement of the bonds between Si atoms on the surface as H atoms form new bonds with them. This process reduces the number of dangling bonds based on the availability of reactive hydrogen and Si sites. These dangling bonds behave as traps, capturing charge carriers and creating space charge inside the nanowire. The local density of states (LDOS) and energy level inside the band gap introduced by traps is a function of the doping type and concentration of the Si. STM imaging of hydrogen terminated n-type Si surfaces have been widely reported in literature (Haider et al., 2009), (Ryan, Livadaru, DiLabio, & Wolkow, 2012), (Schofield et al., 2013). All these studies have reported the effect of biasing the substrate on the charge state of the dangling bonds. It has been observed that the substrate bias with respect to the STM tip affects the charge state of the dangling bond and also affects the chemical reactivity of species reacting at that site. For a negative bias to the substrate, the dangling bonds appear negatively charged and appear as positively charged for a positive bias. Dangling bonds can either capture or release electrons and thus can be held responsible for introducing both positive and negative charge inside the device.

The present nanowire diodes were annealed at 375-380 C for 10 min in a forming gas ambient. This treatment should be sufficient for reaction of the surface with hydrogen atoms. The comparison between the I-V characteristics of the nanowires before and after FGA is shown in *Figure 65*. The I-V characteristics from the 40 nanowire array and the single nanowires of diameter 100 nm are presented here. The other arrays follow a similar trend in terms of change in current due to annealing.

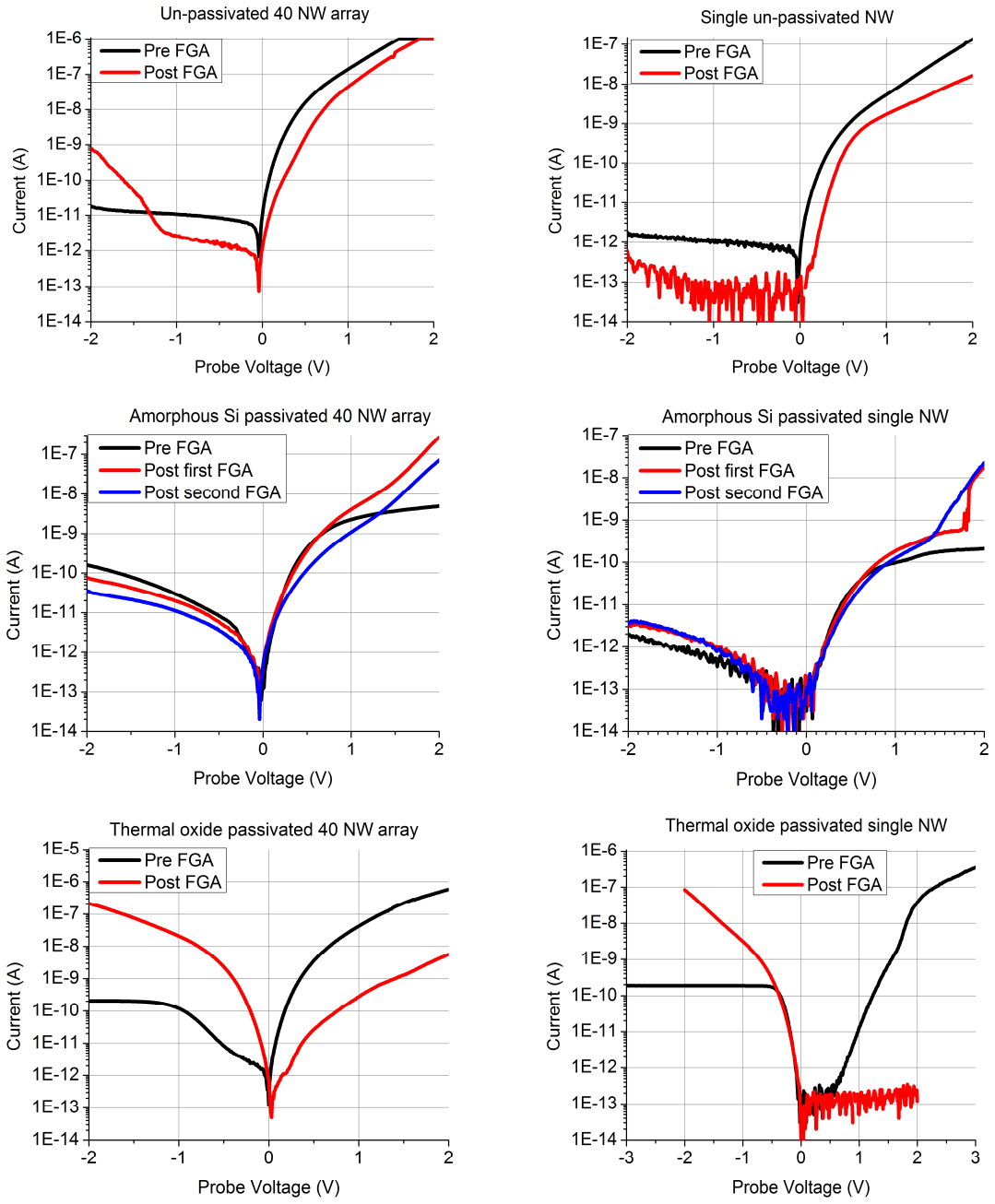


Figure 65. **Comparison between I-V characteristics of 100 nm diameter diodes before and after FGA for the un-passivated, a-Si passivated and thermal oxide passivated nanowires.**

In order to study the effect of annealing on the current, we focus on the measurements recorded from single nanowires as the information in those measurements is not complicated by contributions from several devices. The forward bias current in un-passivated and amorphous Si passivated nanowires

decreases as shown in *Figure 65*. The thermal oxide passivated diode shows negligible current under forward bias after annealing. Under reverse bias, the current in un-passivated nanowire diode is reduced, while that in amorphous Si passivated diode is increased and for the thermal oxide passivated nanowire the reverse bias current is order of magnitude greater than the other two samples. Based on the prior research on hydrogen passivation of n-type Si nanowires, it has been reported that negative fixed charge can be created on the surface of the nanowire during hydrogen passivation (Jie et al., 2008), (C. S. Guo et al., 2009). The observations on forward and reverse bias current suggest that the magnitude of negative charge is highest on the surface of thermal oxide passivated nanowires, followed by the amorphous Si passivated and least on the un-passivated ones. We discuss below, the reasons behind the change in I-V characteristics starting with thermal oxide passivated nanowires.

For the thermal oxide passivated nanowires, the 40 nanowire array after annealing shows close to ambipolar behavior while the single nanowire seems to have been inverted. The change in I-V characteristics of the single nanowire are of particular interest. The forward bias characteristics show very low current which is below the noise floor of the instrument until at least 2V, implying that there are not enough electrons in the nanowire to conduct the current under forward bias. This result suggests that there is negative fixed charge on the nanowire surface, which is enough to keep it depleted even up to ~ 2V. The substrate is n-type doped and almost 500 microns thick. It is possible to invert that substrate with a negative charge on its surface but the rest of it will still conduct as n-type doped semiconductor. So, the overall picture is a n-type nanowire depleted of electrons on top of a n-type substrate which might have a depleted or inverted surface but has a relatively large number of electrons in its quasi neutral region. During reverse bias, both the nanowire and the substrate are depleted. Simulations show that it takes only approximately -0.5V to deplete the nanowire of holes all along its length even when there is no fixed negative charge present on its surface. So, in the real diode, it is safe to assume that it gets fully depleted along its length at -0.5V. In order to justify the large current under reverse bias, we propose the following hypothesis. As negative voltage is applied at the top contact, the holes generated inside the nanowire as well in the depletion region along the surface of the Si substrate should be collected at the metal contact on the tip of the nanowire as there is no barrier for holes flowing from the semiconductor into the metal. The depletion

region rapidly spreads along the length of the nanowire as the bias is increased causing more holes to be generated inside the depletion region and being collected at the top contact. Once the nanowire is fully depleted which is around -0.5 V, the depletion region starts spreading horizontally along the Si substrate since the negative charges present on the nanowire surface should also be present all along the substrate. This provides a very large area for generation of holes limited only by the area of the top contact to the nanowire. As the bias is increased, the current should begin to saturate because the depletion region is not expected to grow beyond the area defined by the top contact. As soon as inversion is reached, the depletion region will stop growing in area and the current will then be dependent on the rate of generation of holes in the inversion layer underneath the contact.

In order to test this hypothesis, capacitance measurements were performed on 100 nm diameter thermal oxide passivated nanowires by contacting the probe to the metal contact on the tip of the nanowire. Before mentioning the results of capacitance versus voltage measurements on the nanowires it is necessary to look at the state of the net charge present on the surface of the Si substrate. Once the charge on the substrate is identified it can be automatically assumed that the same exists on the surface of the nanowires because they have been etched from the substrate itself. There are some 50 by 50 micron square shaped metal pads on top of the SOG on the samples. There are no nanowires underneath these 50 by 50 micron pads. However, since the thickness of the SOG is upwards of 500 nm the capacitance is very small. A quick calculation assuming the dielectric constant of the SOG to be 3.9 places the capacitance of one such pad to be 0.17 pF under accumulation of the substrate. The noise floor of the measurements setup is ~1 pF. So, for the purpose of measurement these pads are not large enough. Hence, we used Hg probe with a circular pad having an area of approximately 0.2 cm^2. For this area assuming the thickness of the SOG to be 500 nm and its dielectric constant to be 3 the capacitance should be roughly 1.0 nF under accumulation which is well within the measurement range. The C-V measurements on the three different surfaces; un-passivated, thermal oxide passivated and amorphous Si passivated, are shown *Figure 66*. The frequency of the AC stimulus was 10 KHz and the LCR meter was set to series mode for making these measurements.

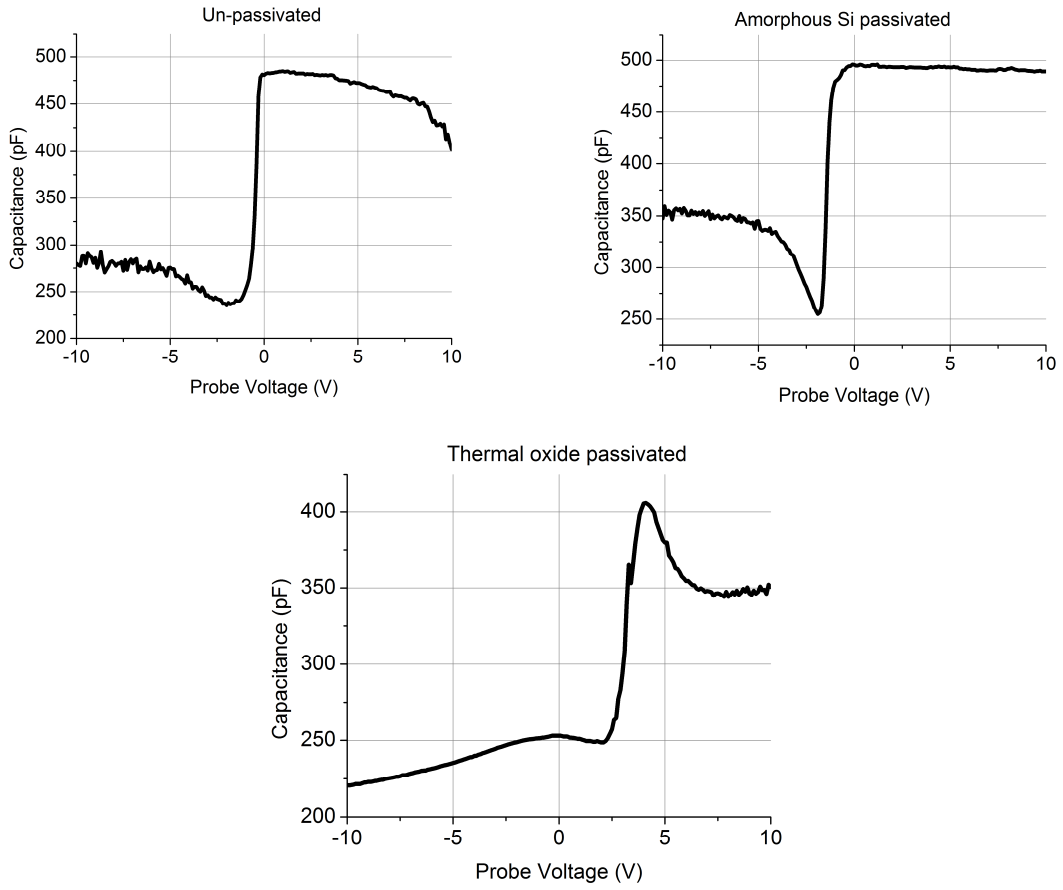


Figure 66. **C-V measurements on different Si substrates using Hg probe.**

The flat band voltage of a MOS capacitor is calculated from the following expression.

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{OX}} - \frac{1}{C_{OX}} \int_0^{tox} \frac{x}{t_{OX}} \rho_{OX}(x) - \frac{Q_{IT}(\phi_S)}{C_{OX}} \tag{6.1}$$

Where, V_{FB} is the Flat band voltage, ϕ_{MS} is the difference in work function between metal and semiconductor, Q_f is the sheet charge density of fixed charge trapped in the dielectric, C_{OX} is the capacitance of the dielectric under accumulation, ρ_{OX} is the volume charge density of trapped charge distributed in the dielectric, t_{OX} is the thickness of the dielectric and Q_{IT} (ϕ_S) is the sheet charge density at the semiconductor/dielectric interface as a function of the surface potential of the semiconductor. Here, our purpose is to get a reasonable approximation of the charge trapped inside the spin-on-glass (SOG) for each of the surface passivations studied here. For the sake of simplicity, we collapse all the charge in the oxide

and the Si/SOG interface into a single term namely, the sheet charge density at the surface of the nanowire and the substrate. Thus, the simplified expression for calculating the flat band voltage becomes:

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{OX}} \tag{6.2}$$

We know that the doping concentration of the Si substrate and the nanowires is 10^{15} cm^{-3} so the difference in work function between Ni and Si in this case is 0.71 eV. One method to estimate the flat band voltage is using the Debye length of the semiconductor as described in (Piskorski & Przewlocki, 2010). The doping concentration of the substrate and the nanowires is known to be 10^{15} cm^{-3} from which the Debye length can be calculated using the following expression

$$L_D = \sqrt{\frac{kT\varepsilon_S\varepsilon_0}{q^2 N_D}} \tag{6.3}$$

Where, ε_S and ε_0 are the dielectric constant and the permittivity of Si and vacuum respectively, k is the Boltzmann's constant, T is the absolute temperature, q is the elementary charge and N_D is the doping concentration of the Si substrate. The capacitance at flat band without any charge trapped inside the dielectric (C_{sFB}) is determined by the following expression

$$C_{sFB} = \frac{\varepsilon_S\varepsilon_0}{L_D} \tag{6.4}$$

Once C_{sFB} is known, the flat band voltage is determined from the C-V curve by finding the voltage at which the capacitance is equal to C_{FB} which is calculated as

$$C_{FB} = \frac{C_{OX}.C_{sFB}}{C_{OX} + C_{sFB}} \tag{6.5}$$

Then the relation between V_{FB}, C_{OX}, Q_f and ϕ_{MS} is used to determine Q_f in units of C/ cm^2 and number of charges trapped cm^{-2}. The Debye length of the Si substrate in this case comes out to be 1.29 x 10^{-5} cm which yields a C_{sFB} of 8 x 10^{-8} F cm^{-2}. Table 10 shows the values of C_{FB}, V_{FB} and Q_f (as C/ cm^2 and # charges/ cm^2).

Table 10

Values of C_{FB}, V_{FB} and Q_f extracted from C-V measurements for different surface passivations

Surface passivation	**C_{FB} (pF)**	**V_{FB} (V)**	**Q_f (C/ cm^2)**	**Q_f (# charges/ cm^2)**
Un-passivated	466	-0.3	+2.5 x 10^{-9}	+1.5 x 10^{10}
Thermal oxide	342	+3.2	-4.4 x 10^{-9}	-2.8 x 10^{10}
Amorphous Si	480	-1.0	+4.3 x 10^{-9}	+2.7 x 10^{10}

The actual device consists of two structures in parallel: the MOS structure formed by the metal/SOG/substrate and the nanowire itself. *Figure 67* shows the circuit representing the nanowire diode.

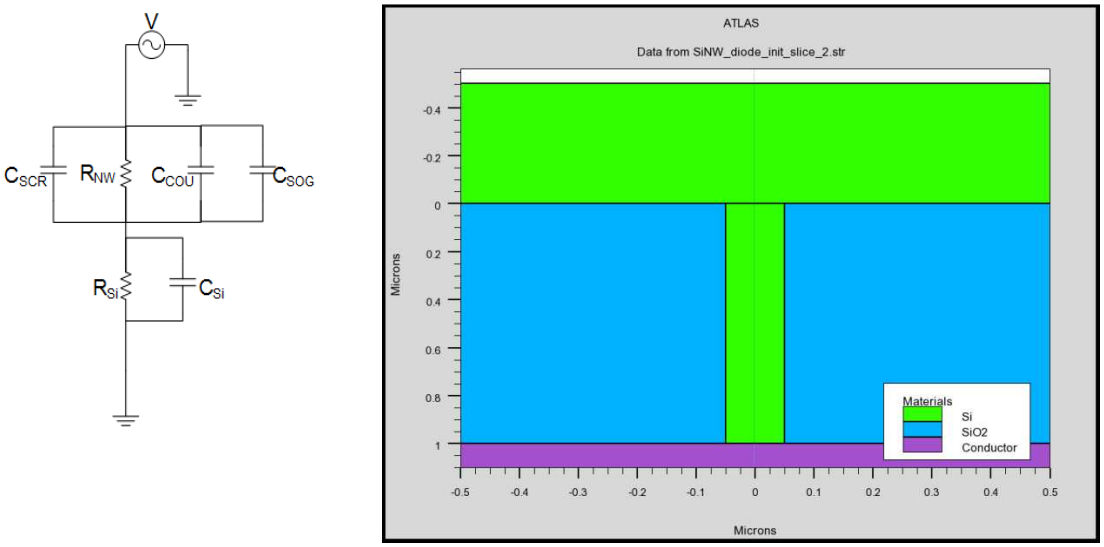


Figure 67. **(Left) Equivalent circuit diagram and (right) cross section of a single nanowire structure created in Atlas simulator.**

The term C_{SOG} represents the capacitance formed by the metal contact/SOG/Si substrate, C_{SCR} is the capacitance due to the depletion region formed inside the nanowire due to the Schottky barrier, R_{NW} is the resistance of the quasi-neutral region inside the nanowire and R_{Si} is the resistance of the Si substrate, C_{COU} represents a capacitive coupling which is likely to exist between the surface of the nanowire and the large metal contact on its tip, R_{Si} represents the resistance of the Si substrate and C_{Si} is the bias-dependent capacitance which might be offered by the Si substrate depending on whether it is accumulated, depleted or inverted. We first estimate the values of some of these capacitances to get a first order idea about which ones are important and which ones can probably be neglected to simplify the equivalent circuit model.

These estimates for C_{SOG} and C_{SCR} are based on the diameter of the nanowires and the thickness of the SOG surrounding them. The C_{SOG} is small because of the thickness of the SOG. The largest contact pads to the nanowire diodes are 25500 square microns in area. The thickness of the SOG is 500 nm on average among the three samples studied here. This yields a capacitance of 1.8 pF which is barely the noise margin of the measurement setup. Thus, we should not expect to observe the changes in capacitance when the substrate goes from inversion to accumulation and vice versa while making C-V measurements on the tips of nanowire arrays. The capacitor due to C_{SOG} can thus be considered negligibly small and its reactance so large that it can be treated as an open circuit. C_{SCR} is the depletion region capacitance of the nanowire. The cross-sectional area of the largest (100 nm diameter) nanowires is 7.9 x 10^{-11} cm^2. The largest array of nanowires has 400 of them which make the largest possible cross-sectional area due to the nanowire tips on the sample to be 3.14 x 10^{-8} cm^2. With this area the capacitance of the depletion region varies inversely as its thickness along the length of the nanowire. We estimate a practical upper bound on the space-charge region capacitance assuming the width of the region to be only 1 nm. For a 1 nm wide depletion region at the tip of an array of 400 nanowires the capacitance is 0.33 pF. As the space charge region inside the nanowire becomes larger C_{SCR} will decrease and thus, can be neglected from the circuit diagram. So, finally we are left with the equivalent circuit in *Figure 68*.

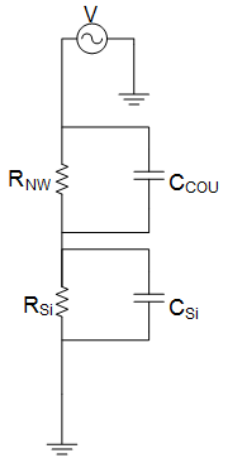


Figure 68. **Equivalent circuit diagram for C-V analysis after neglecting C_{SCR} and C_{SOG}.**

There are three different regions of operation of the nanowire diode when the voltage on the metal contact is swept from negative to positive bias. When the voltage is positive, the nanowire and the Si

substrate should be accumulated and when the voltage is negative the nanowire is depleted to a certain width along its length and the Si substrate may or may not be depleted depending on the voltage and the fixed charge present on the surface. When the negative bias is large enough, the nanowire and the Si substrate can be inverted. So, the three regions of operation are accumulation, depletion and inversion.

The significance of showing the equivalent circuit model is to understand the C-V measurements made on the tip of the nanowire arrays. The capacitance meter can be set to either series or parallel mode for making the measurements. None of these modes can represent the device accurately for all the three regimes namely accumulation, depletion and inversion. The LCR meter sees the device under test as shown in *Figure 69*.

Figure 69. **(Left) Bridge circuit in the LCR meter. (Right) phase diagram between the resistance and reactance of the device as seen by the capacitance meter.**

The diagram on the right represents the phase relation between the resistive and reactive components in the circuit on the left. The net impedance of the circuit is Z which is composed of both resistive (R) and reactive (X) components. There is a bridge circuit inside the LCR meter as shown in the figure. The net impedance of the device under test (DUT) appears as Z_X and the impedance Z_1 inside the meter is adjusted until the bridge is balanced i.e. there is no current flow across the component represented by D. The bridge is considered to be balanced at this point and the impedance of the DUT is calculated by the following expression

$$Z_{DUT} = \left({}^{Z_3}/_{Z_2}\right) Z_1 \tag{6.6}$$

Where Z_3 and Z_2 are known fixed impedances, Z_1 is adjusted by the meter until the bridge is balanced so that is also known. The voltage applied to the circuit consists of a DC bias on which a AC signal is superimposed. The phase difference between Z_{DUT} and the applied voltage is represented by θ in the phase

diagram. In case the LCR meter is set to the parallel mode, the admittance of the device (Y_{DUT}) is calculated from the inverse of the impedance. The equivalent circuit diagrams for the DUT as understood by the LCR meter in series and parallel modes are shown in *Figure 70*.

Figure 70. **The equivalent circuit for the DUT as seen by the LCR meter in series (left) and parallel (right) modes.**

In case of the series mode the impedance of the DUT is

$$Z_{DUT} = R - \frac{j}{\omega C}, \tag{6.7}$$

While in parallel mode the admittance of the DUT is calculated, which is given by

$$Y_{DUT} = G + j\omega C. \tag{6.8}$$

In both cases the component of the impedance or admittance which is in-phase with the applied AC voltage gives the resistance (R) or conductance (G) and the out-of-phase component gives the capacitance (C) of the DUT. Clearly, the equivalent circuit of the nanowire diode does not classify as either a totally series or totally parallel equivalent circuit. However, the parallel mode is more suitable to represent the device because if the capacitors are removed from the equivalent circuits shown in *Figure 68*, the structure is reduced to the resistance of the nanowire and the Si substrate. Thus, the LCR meter was set to parallel mode when making measurements on the nanowire diodes. We start by deriving the net admittance of the nanowire diode for the equivalent circuit shown in *Figure 68* and then proceed to derive the admittance for forward and reverse bias where the nanowire and the Si substrate can be in accumulation, depletion or inversion. The circuit in *Figure 68* is re-drawn in *Figure 71* in terms of conductance to derive its net admittance.

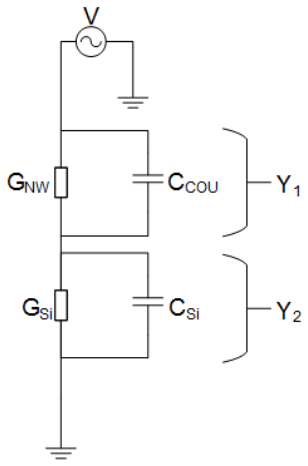


Figure 71. **Equivalent circuit diagram of the nanowire diode for small signal analysis under depletion.**

The net admittance of the circuit is a series combination of Y_1 and Y_2.

$$Y_1 = G_{NW} + j\omega C_{COU};\ Y_2 = G_{Si} + j\omega C_{Si}; Y_{NET} = \frac{Y_1 Y_2}{Y_1 + Y_2}$$

$$Y_{NET} = \frac{(G_{NW}G_{Si} - \omega^2 C_{COU}C_{Si}) + j\omega(G_{Si}C_{COU} + G_{NW}C_{Si})}{G_{NW} + G_{Si} + j\omega(C_{COU} + C_{Si})} \tag{6.9}$$

$$Y_{NET} = \frac{[(G_{NW}G_{Si} - \omega^2 C_{COU}C_{Si}) + j\omega(G_{Si}C_{COU} + G_{NW}C_{Si})][(G_{NW} + G_{Si}) - j\omega(C_{COU} + C_{Si})]}{[G_{NW} + G_{Si} + j\omega(C_{COU} + C_{Si})][G_{NW} + G_{Si} - j\omega(C_{COU} + C_{Si})]}$$

After simplification we get the following expression for the net admittance

$$Y_{NET} = \frac{G_{NW}{}^2 G_{Si} + G_{Si}{}^2 G_{NW} + \omega^2 G_{Si} C_{COU}{}^2 + \omega^2 G_{NW} C_{Si}{}^2 + j\omega\left(G_{Si}{}^2 C_{COU} + G_{NW}{}^2 C_{Si} + \omega^2 C_{COU}{}^2 C_{Si} + \omega^2 C_{COU}{}^2 C_{Si}\right)}{(G_{NW} + G_{Si})^2 + \omega^2 (C_{COU} + C_{Si})^2}$$

The net conductance and capacitance from the above expression are

$$G_{NET} = \frac{G_{NW}{}^2 G_{Si} + G_{Si}{}^2 G_{NW} + \omega^2 G_{Si} C_{COU}{}^2 + \omega^2 G_{NW} C_{Si}{}^2}{(G_{NW} + G_{Si})^2 + \omega^2 (C_{COU} + C_{Si})^2} \tag{6.10}$$

$$C_{NET} = \frac{G_{Si}{}^2 C_{COU} + G_{NW}{}^2 C_{Si} + \omega^2 C_{COU}{}^2 C_{Si} + C_{COU} C_{Si}{}^2}{(G_{NW} + G_{Si})^2 + \omega^2 (C_{COU} + C_{Si})^2} \tag{6.11}$$

We first discuss the conductance measured from the nanowire diodes. The I-V characteristics of the nanowire diodes can be used to calculate the differential conductance which can be a good estimate of G_{NW}. G_{Si} when the Si substrate is accumulated, can just be approximated from

$$G_{Si} = \frac{A}{\rho L} \tag{6.12}$$

Where A is the area of the substrate which conducts current below the nanowire, ρ is the resistivity of the Si substrate and L is its thickness. For a doping concentration of 10^{15} cm^{-3} G_{Si} comes out to be 3.86 x 10^{-4} S. The maximum differential conductance of the array of nanowires from DC I-V measurements is ~10^{-5} S. Thus, under forward bias the Si substrate is under accumulation and G_{Si} is much greater than G_{NW}. C_{Si} should not be considered under forward bias as it should be shorted out by the accumulation layer of electrons present on the surface of the substrate. In general the terms involving the square of a capacitance are much smaller than those involving the square of a conductance. Hence, as an approximation, after neglecting the terms containing ${C_{COU}}^2$ and C_{Si} in equation (6.10) we get

$$G_{NET} \approx \frac{{G_{Si}}^2 G_{NW}}{{G_{Si}}^2} = G_{NW} \tag{6.13}$$

The comparison between conductance measured under forward bias (accumulation) from arrays of nanowire diodes and the differential conductance extracted from I-V measurements on the same nanowires are presented in *Figure 72*, *Figure 73* and *Figure 74*.

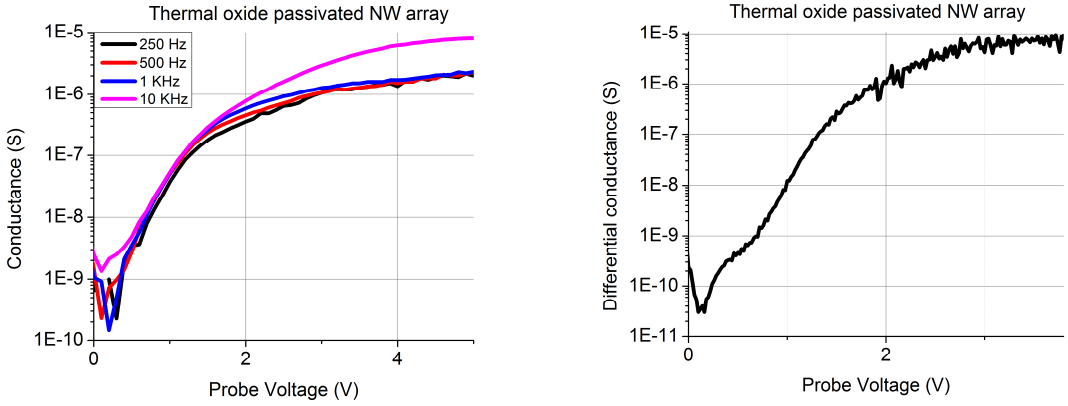


Figure 72. **AC conductance (left) and differential conductance (right) measured from an array of 400 thermal oxide passivated nanowire diodes.**

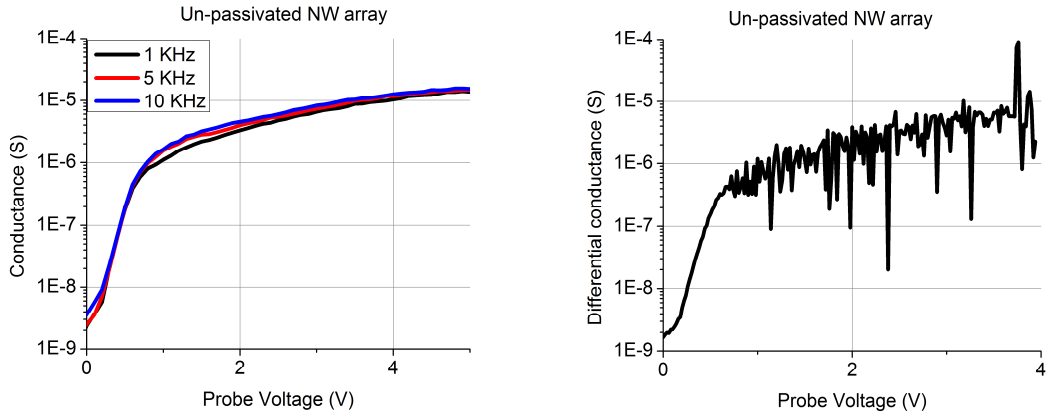


Figure 73. **AC conductance (left) and differential conductance (right) measured from an array of 400 un-passivated nanowire diodes.**

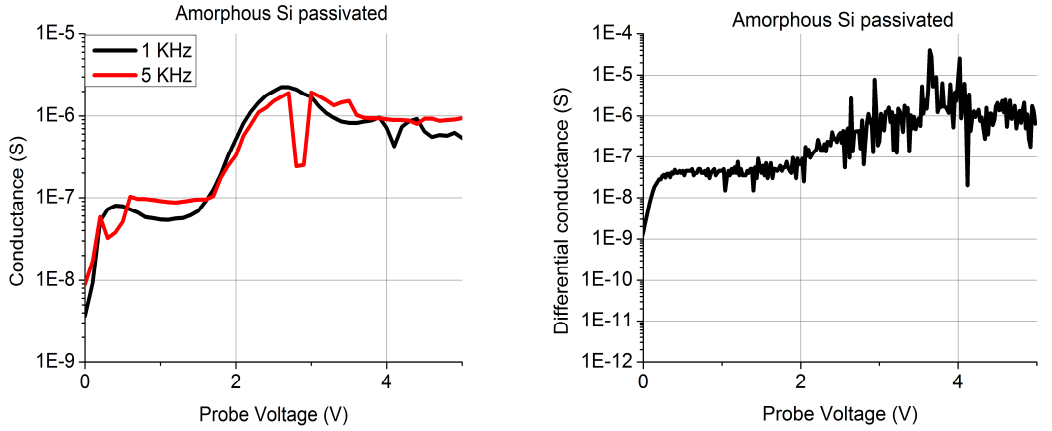


Figure 74. **AC conductance (left) and differential conductance (right) measured from an array of 400 amorphous Si passivated nanowire diodes.**

In all cases the net AC conductance follows the same trend and is close to the differential conductance G_{NW} which supports the approximation in equation (6.13). The measured conductance shows an increase with increasing frequency of the measurement but only at large forward bias. The frequency dependence is the maximum in thermal oxide passivated and minimum in un-passivated nanowires. Equation (6.10) suggests that frequency dependence of the conductance under forward bias is possible if C_{COU}^{2} is no more negligible compared to G_{Si}. Hence, the model suggests that the capacitive coupling between the nanowire and the metal contact C_{COU} under forward bias is the minimum in case of un-passivated and maximum in thermal oxide passivated nanowires. Hence, we can conclude that the net AC conductance of the nanowire diode

under forward bias is approximately equal to the differential conductance of the nanowire itself but the capacitive coupling with the metal contact can add frequency dependence to it.

We now consider the capacitance measured from the nanowire diodes under forward bias. Neglecting C_{Si}, the net capacitance of the device simplified from equation (6.11) is given by

$$C_{NET} \approx \frac{{G_{Si}}^2 C_{COU}}{{G_{Si}}^2 + \omega^2 {C_{COU}}^2} \tag{6.14}$$

The capacitance measured under forward bias from arrays of nanowire diodes is presented in *Figure 75*.

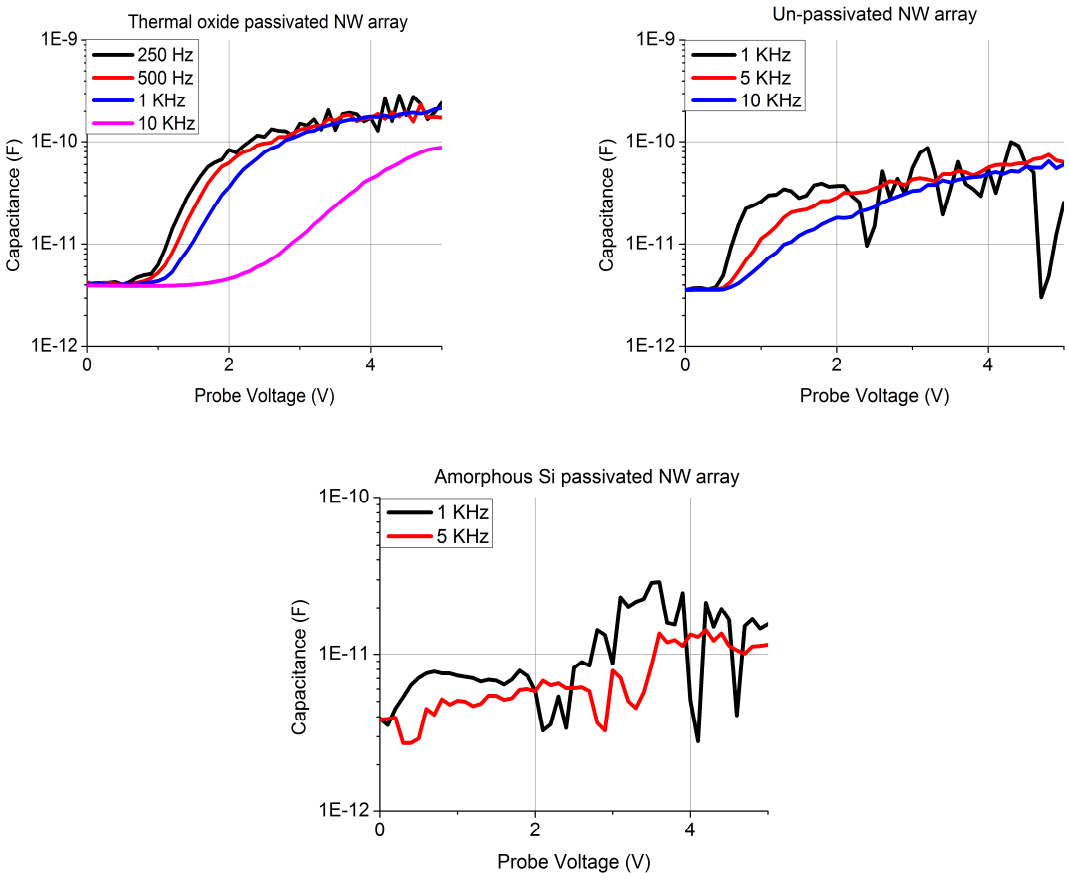


Figure 75. **Capacitance measured under forward bias from arrays of 400 nanowires. (Top-left) Thermal oxide passivated, (Top-right) Un-passivated and (Bottom) Amorphous Si passivated nanowires.**

The net capacitance of the nanowire arrays is reduced as the frequency of the measurement is increased. This is correctly predicted by the expression in equation (6.14). The dependence of net capacitance upon DC bias should come from C_{COU} as G_{Si} is not expected to increase with the bias as the Si

substrate is already accumulated. The increase and then apparent saturation of capacitance with voltage under forward bias indicates that the C_{COU} increases as the nanowire gets strongly accumulated along its length and the electrons present close to its surface can react faster to the changes in the voltage applied at the metal contact as the forward bias is increased.

We will now discuss the conductance and capacitance observed under reverse bias.

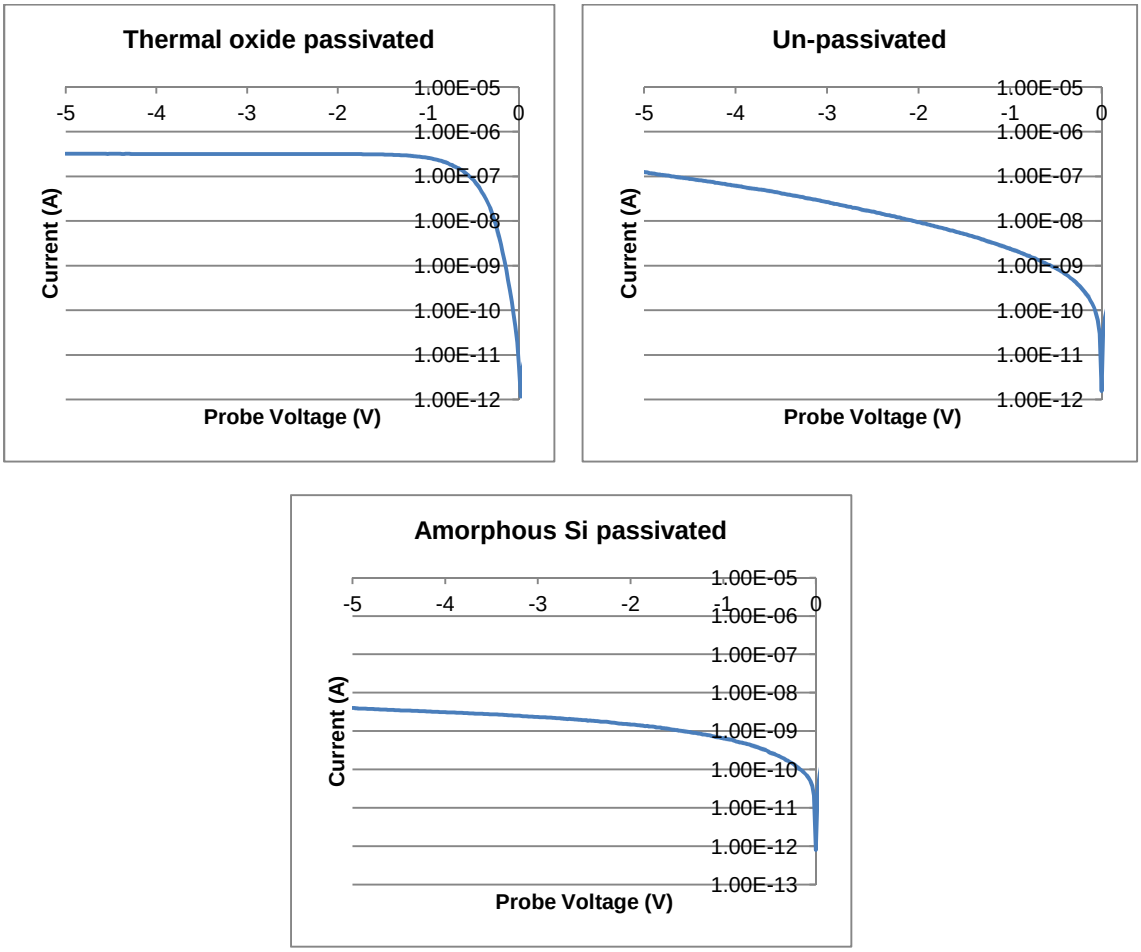


Figure 76. **Reverse bias current versus voltage from an array of 400 thermal oxide passivated, un-passivated and amorphous Si passivated nanowire diodes.**

The depletion region is expected to grow along the length of the nanowire and then spread along the surface of the Si substrate under reverse bias. From the reverse bias current of thermal oxide passivated nanowires in *Figure 76*, we observe that due to creation of a depletion region along the surface of the Si substrate under the area covered by the metal contact pad, there is a sharp increase in reverse bias current due to generation of holes in that region. Beyond a certain reverse bias, the current saturates indicating that

inversion is achieved and the depletion region cannot grow any more. In amorphous Si passivated and un-passivated nanowire diodes the reverse bias current does not increase sharply and does not saturate. So, it is most likely that the depletion region does not spread as rapidly along the Si substrate in case of amorphous Si passivated and un-passivated nanowires as it does for thermal oxide passivated nanowires. First we present the situation where the depletion region seems to be limited to the nanowire and explain the conductance and capacitance measured from amorphous Si passivated and un-passivated nanowire diodes. When the depletion region has not started spreading along the Si substrate, C_{Si} can still be neglected and the net conductance can still be approximated by equation (6.13). G_{NW} is even lower compared to G_{Si} as the nanowire is depleted of electrons. Thus, the AC conductance is expected to follow the same trend and be approximately equal to the differential conductance measured from the nanowire diodes. AC conductance and differential conductance measured from DC I-V characteristics is shown in *Figure 77* and *Figure 78*.

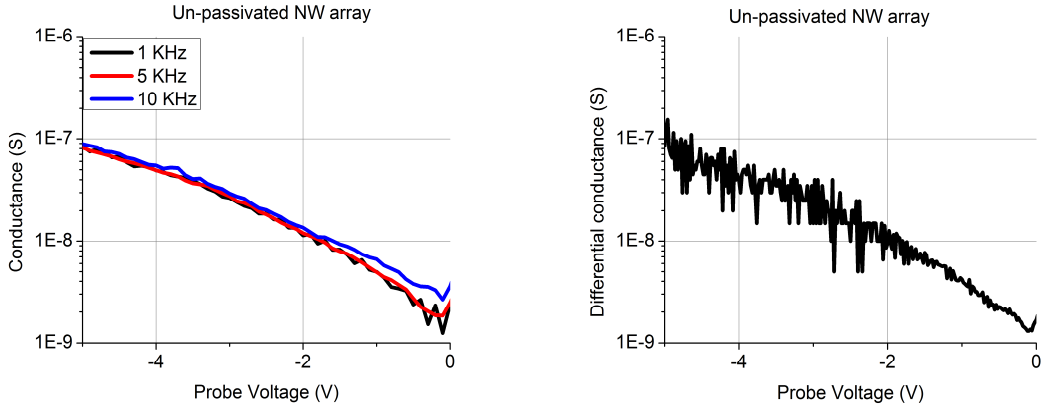


Figure 77. **AC conductance (left) and differential conductance (right) measured from an array of 400 un-passivated nanowire diodes.**

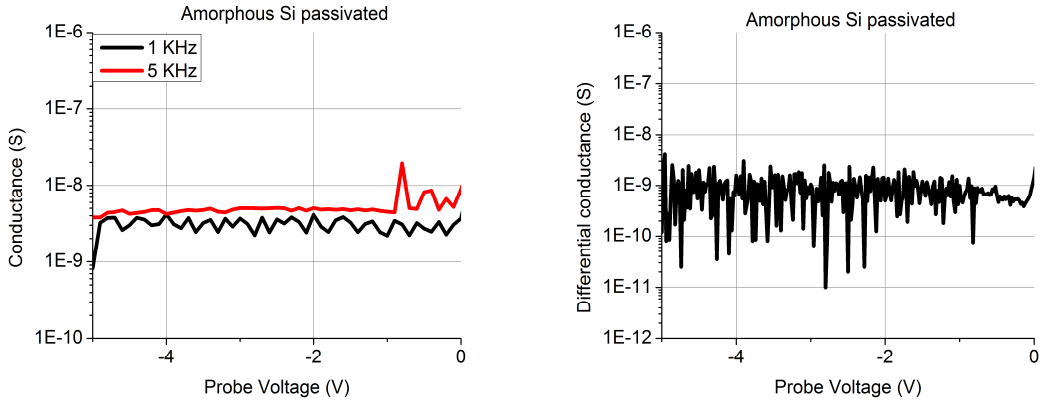


Figure 78. **AC conductance (left) and differential conductance (right) measured from an array of 400 amorphous Si passivated nanowire diodes.**

The capacitance measured during reverse bias, from arrays of amorphous Si passivated and un-passivated nanowires are shown in *Figure 79*.

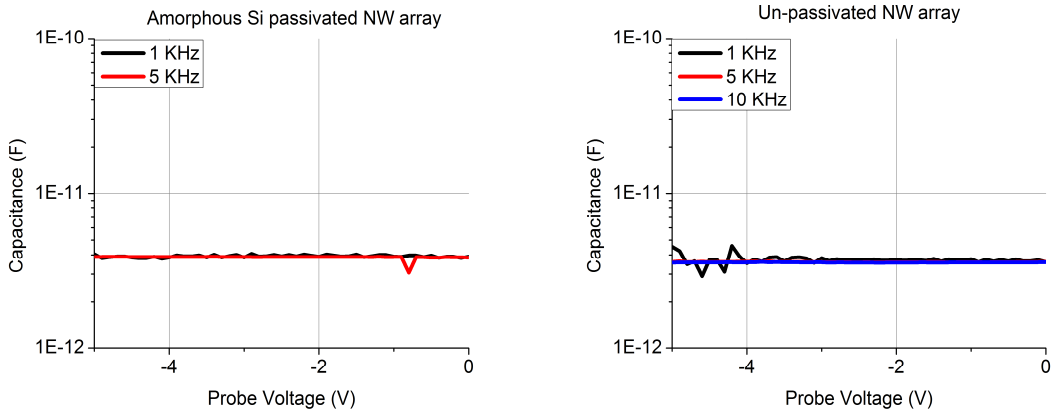


Figure 79. **Capacitance measured at different frequencies from an array of 400 amorphous Si passivated nanowires (left) and un-passivated nanowires (right).**

In both cases, there is no dependence of the capacitance on the frequency of the measurement. To derive the net capacitance in this case, we can simplify equation (6.11) by neglecting the frequency dependent terms and C_{Si} since the Si substrate is still considered to be accumulated. The net capacitance is

$$C_{NET} \approx \frac{\frac{{G_{Si}}^2}{{G_{NW}}^2} C_{COU}}{\left(1 + \frac{G_{Si}}{G_{NW}}\right)^2} \approx C_{COU} \tag{6.15}$$

The coupling capacitance between the nanowire and the metal contact at its tip seems to be very low when it is depleted. One probable cause for this can be that holes being minority carriers cannot respond to rapid

changes in the applied voltage as they need to be thermally generated. Thus, the net capacitance remains at the noise floor of the measurement setup and is independent of the frequency of measurement.

We now try to explain the conductance and capacitance measured from thermal oxide passivated nanowire diodes.

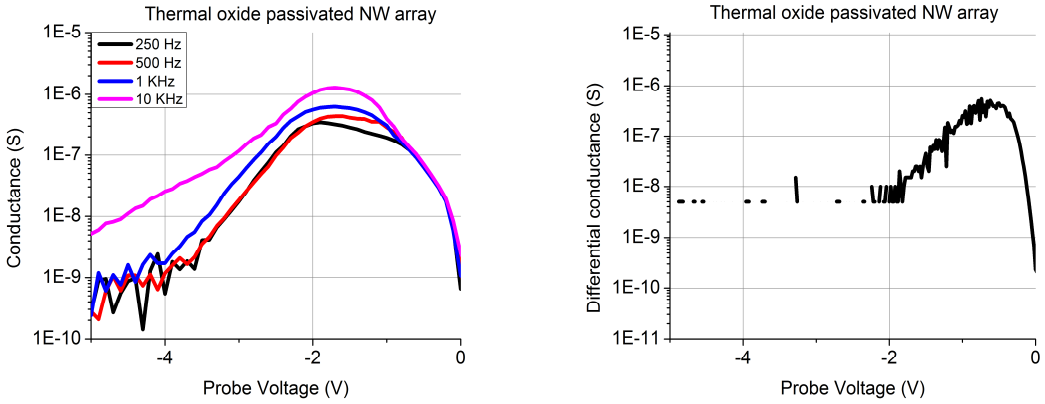


Figure 80. **(Left) AC conductance and (right) differential conductance extracted from DC I-V measurement from an array of 400 thermal oxide passivated nanowire diodes.**

Figure 80 shows the comparison between AC conductance and differential conductance extracted from DC I-V measurement on an array of 400 thermal oxide passivated nanowire diodes. From the net conductance of the nanowire diode shown in equation (6.10) the frequency independent part is the following

$$G_{NET} \approx \frac{{G_{NW}}^2 G_{Si} + {G_{Si}}^2 G_{NW}}{(G_{NW} + G_{Si})^2} \tag{6.16}$$

For the initial part of the reverse bias, the net conductance seems to be independent of the frequency and follow G_{NW} until it reaches its maximum around -1V. G_{Si} is expected to decrease sharply as the depletion region spreads into the Si substrate. G_{NW} is the maximum around -1V after which it starts decreasing sharply and becomes negligible around -2V. Frequency dependence starts to show in the measured conductance around -1V after which it is directly proportional to the frequency of measurement. Hence, it is probable that the frequency dependent terms in equation (6.10) become significant after G_{NW} becomes negligible. With increasing reverse bias, as the Si substrate also gets inverted, C_{Si} becomes low. The conductance of an inverted nanowire is negligible so we can also neglect G_{NW} from equation (6.10). C_{COU} for an inverted nanowire will also be negligible. Thus, for strong inversion i.e. large reverse bias, all the

terms in the numerator of the net conductance in equation (6.10) become negligible. Thus, the conductance tends to reach the noise floor of the measurement setup as the nanowire diode reaches strong inversion.

We will now try to explain the capacitance measured from arrays of 400 thermal oxide passivated nanowire diodes.

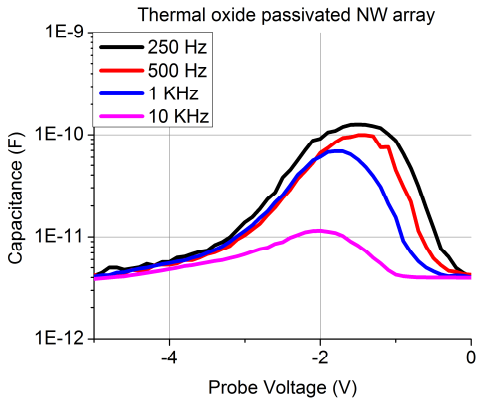


Figure 81. **Capacitance measured from an array of 400 thermal oxide passivated nanowire diodes.**

The capacitance measured from an array of 400 thermal oxide passivated nanowire diodes is shown in *Figure 81*. In order to explain the trend seen in the capacitance we consider the frequency independent terms in the net capacitance from equation (6.10)

$$C_{NET} \approx \frac{{G_{Si}}^2 C_{COU} + {G_{NW}}^2 C_{Si}}{(G_{NW} + G_{Si})^2} \approx \frac{\frac{{G_{Si}}^2}{{G_{NW}}^2} C_{COU} + C_{Si}}{\left(1 + \frac{G_{Si}}{G_{NW}}\right)^2} \tag{6.17}$$

During low reverse bias when the depletion region inside the Si substrate is thin, C_{Si} is very high. The conductance of the Si substrate is expected to decrease sharply as the depletion region starts forming on its surface so the term containing the ratio of G_{Si} to G_{NW} becomes small and the net capacitance of the nanowire diodes is expected to be governed by the value of C_{Si}. For a depletion region 10 nm thick C_{Si} is 264 pF. The net capacitance of the nanowire diode array plotted in *Figure 81* shows a maximum of ~100 pF which is close to the calculated value of C_{Si} for a frequency of 250 Hz. The frequency dependence however, is considerable indicating that the term containing C_{COU} + C_{Si} in the denominator may still be significant. This is in agreement with the assumption that the depletion region width is still small. As the reverse bias is increased, the value of C_{Si} decreases because of increase in the width of the depletion region.

At strong reverse bias, the net capacitance of the nanowire diodes seems to be governed by the ratio of G_{Si} to G_{NW} only as it becomes independent of the frequency and its value tends to reach the noise floor of the measurement setup. This is an expected result from the approximate expression for the net capacitance stated in equation (6.17).

6.6 Modeling the I-V characteristics

Now that we know how the depletion region behaves with the voltage applied to the nanowire diodes, we can make an attempt to simulate the current measured during DC sweep. The simulator provides the opportunity to introduce non-idealities into the diode and observe their effects to help us determine what factors are responsible for controlling the current in our devices. We start by comparing an ideal nanowire diode with the current observed from un-passivated nanowires. For simulating an ideal nanowire diode a structure was created in Silvaco Atlas for a single Si nanowire of diameter 100 nm. Mobility inside Si nanowires has been reported to range from approximately 1 to 250 $cm^2V^{-1}s^{-1}$ (Zheng et al., 2004), (C. Guo et al., 2009). The Schottky barrier height was fixed at 0.58eV which was extracted from thermionic emission model fitting on the data from un-passivated nanowire diodes. The nanowire stands on a n-type Si substrate and the doping of both the nanowire and the substrate is 10^{15} cm^{-3}. Bulk mobility for electrons which is 10^3 $cm^2V^{-1}s^{-1}$ and for holes which is 500 $cm^2V^{-1}s^{-1}$ has been assumed in these simulations.

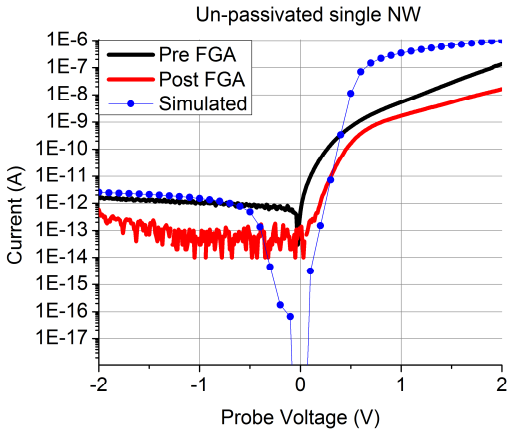


Figure 82. **Comparison of the I-V characteristics measured from a single 100 nm diameter un-passivated nanowire diode with simulation performed on an ideal single 100 nm diameter nanowire diode.**

The minority carrier lifetime used in these simulations is 100 µs which is based on the values reported in literature for bulk Si. The doping concentration in the Si nanowires and the substrates used in

this study is 10^{15} cm^{-3}. At a doping level of 10^{16} cm^{-3}, the minority carrier lifetime is experimentally reported to be ~10^{-5} sec with a trend which shows that it will be approximately 100 µs for a doping of 10^{15} cm^{-3} (Tyagi & Overstraeten, 1983). In another report the minority carrier lifetime for a doping of 10^{15} cm^{-3} is expected to be dominated by SRH and is calculated as 200 µs (Schroder, 1997).

We start the comparison between simulation and measurement shown in *Figure 82* from the reverse bias. The measured current decreases after forming gas anneal (FGA). We know from Hg probe measurements that there is a net positive charge on the Si surface of un-passivated nanowires after FGA. This should cause the current to increase under both forward and reverse bias but the opposite is observed. The reverse bias current is strongly dependent on generation of holes inside the depletion region formed in the nanowire. The density of defects on the surface of the nanowire is directly proportional to the density of holes generated during reverse bias. Thus, a probable cause for the reduction in reverse bias current after FGA can be a reduction in surface generation velocity of holes in the depletion region.

Under forward bias the ideality factor from the measured current is higher than the ideal diode. At low forward bias the current is much higher. If there is recombination in the depletion region under the metal contact, it can increase the current at low forward bias. The current due to thermionic emission has an exponential relationship with the applied voltage. The current due to recombination depends on the defect density inside the depletion region and the minority carrier lifetime. Thus it can be much higher than the thermionic emission current at low forward bias voltages. At large positive bias, the simulated current becomes much larger than the measured current, suggesting a higher resistance offered by the nanowire towards the flow of electrons. The increase in resistance can be due to a reduction in mobility of charge carriers inside the nanowire. *Figure 83* shows the comparison of the simulations with the measurement by changing the mobility of electrons and holes inside the nanowire from bulk values to 10 $cm^2V^{-1}s^{-1}$ and fixing the sheet charge density at the surface of the nanowire and the Si substrate to be 1.5 x 10^{10} cm^{-2} calculated from Hg probe C-V measurements on the SOG.

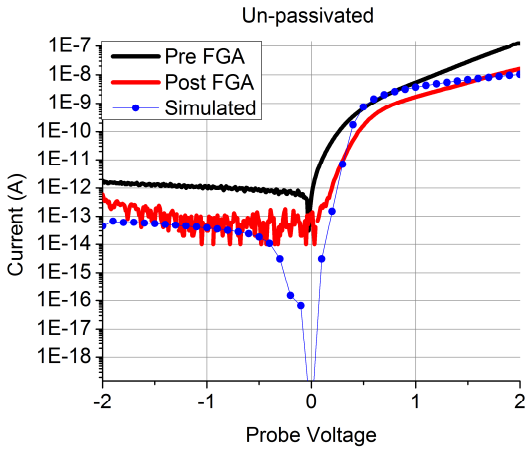


Figure 83. **Comparison between simulated and measured current from a single un-passivated 100 nm diameter nanowire diode with electron and hole mobility as 10 $cm^2V^{-1}s^{-1}$ and fixed charge density at the Si/SOG interface is set to positive 1.5 x 10^{10} cm^{-2}.**

The fit during forward bias is still not good mainly because the ideality factor is high in the actual diode, possibly due to recombination current at low forward bias. The current during reverse bias matches relatively well with simulation showing that the mobility is considerably less than the bulk value in these nanowire diodes. The fact that the current was reduced after FGA can be indicative of a reduction in the net positive charge at the Si/SOG interface. We now make a similar comparison between simulation and measurement for amorphous Si passivated nanowires shown in *Figure 84*.

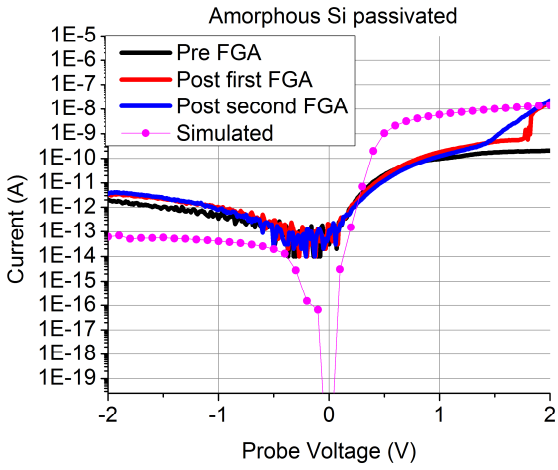


Figure 84. **Comparison between simulation and measurement of a single amorphous Si passivated nanowire diode when the mobility of electrons and holes is set to 10 $cm^2V^{-1}s^{-1}$ and fixed charge density at the Si/SOG interface is set to positive 2.7 x 10^{10} cm^{-2}.**

The reverse bias current is almost an order of magnitude larger and the forward bias current is considerably smaller than the simulated current. Further reduction in mobility alone does not seem to be a probable cause of this difference because that will reduce the reverse bias current even further. However, if the rate of generation of holes increases inside the nanowire due to an increase in the density of defects that could possibly explain the increase in reverse bias current. Further investigation into the energy distribution of defect levels on the nanowire and the substrate should provide the causes behind the differences observed here. A similar comparison for thermal oxide passivated nanowire diodes is shown in *Figure 85*.

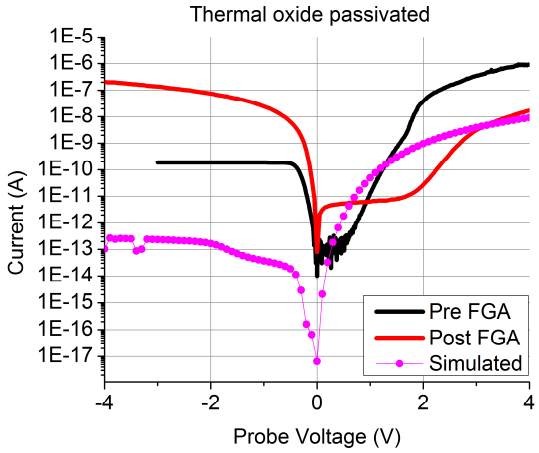


Figure 85. **Comparison between simulated and measured current for a single thermal oxide passivated nanowire when bulk mobility is considered and fixed charge density at the Si/SOG interface is set to negative 2.8 x 10^{10} cm^{-2}.**

In *Figure 85* it is clear that the simulated current is much lower than the current measured through the actual diode. *Figure 86* shows the depletion region, the concentration of holes and the current density in a cross-section of the three 3-D cylindrical structure of a nanowire diode simulated under reverse bias.

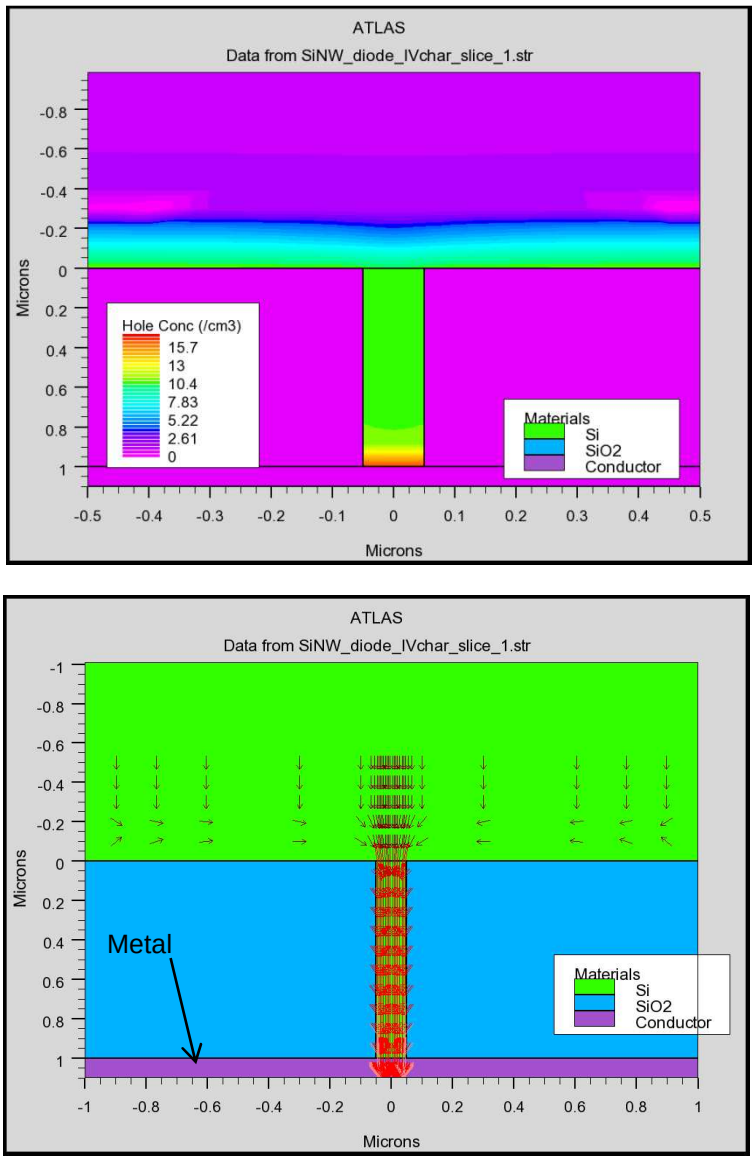


Figure 86. **Cross-section of the cylindrical nanowire diodes structure simulated in Atlas. The voltage applied to the metal contact is -5V. (Top) Contours representing hole concentration (Bottom) Contours representing hole current density (Acm^{-2}) and vectors representing the current density due to holes inside the structure.**

The current during reverse bias for thermal oxide passivated nanowires is much higher compared to that for amorphous Si passivated and un-passivated devices. The simulated current is almost two to three orders of magnitude lower than the measured current. In order to understand the possible cause for this discrepancy we have plotted the hole concentration and hole current density in *Figure 86*. The arrows indicate the vector representing hole current density in the Si substrate and the nanowire. The simulation

shows that there is a depletion region on the surface of the Si substrate due to the fixed negative sheet charge of density 2.8 x $10^{10}$$cm^{-2}$ present on the substrate and the nanowire and the negative voltage applied at the metal contact to the tip of the nanowire. The holes generated thermally in this region are pulled towards the nanowire by the electric field of the metal contact as shown by the vectors of hole current density. Since there is no barrier towards the flow of holes into the contact, they can be collected as reverse bias current. The main reason for the simulated current being 2-3 orders of magnitude lower than the measured value can be the difference in area of the depletion region between the real device and the simulated structure. The area of depletion region in a single real nanowire diode is that of the Ni contact pad at its tip which is equal to 4.7 x 10^{-5} cm^2. The area of the cylindrical structure simulated in Atlas is just 7.8 x 10^{-9} cm^2. The difference in area is ~ 6000 which can possibly explain why the simulated reverse bias current is so low.

Under forward bias, the simulated current is lower than the measured current. We also observe that the measured current tends to abruptly increase by two orders of magnitude. The simulator has made an assumption that the flat band voltage is entirely due to fixed charge at the surface of the nanowire and the substrate which does not move during application of voltage at the metal contact on the tip of the nanowire. In reality, if the negative charge is mobile such that at a certain positive bias on the metal contact, there is some net movement of negative charge towards the metal contact, it will increase the accumulation of electrons on the substrate as well as the nanowire and increase the current. The charge distribution inside the spin on glass coupled with the study of the energy distribution of defect levels within the band gap is still needed to build a suitable model inside the simulator for predicting the current through the nanowires.

6.7 Fitting the I-V characteristics using traps

So far, we have tried to compare the simulation to the measured current using the ideal thermionic emission model. It is clear from *Figure 83* and *Figure 84* that the ideality factor is greater than 1 for the actual nanowire diodes. The simulator can account for that by introducing traps on the surface of the nanowire and the substrate. However, the parameters needed to simulate traps include the following

- Trap density on the surface (cm^{-2})

- Energy level relative to valence band maximum and conduction band minimum (eV)
- Type of trap (acceptor or donor)
- Capture cross section (cm^2)

We do not have experimentally available information for these parameters. So, in order to show that the presence of traps can change the ideality factor, we fixed the energy level and the capture cross section and changed the density of traps to fit the current measured from the diodes. The traps were assumed to be mono-energetic with energy level 0.8 eV above the valence band maximum for donors and 0.8 eV below the conduction band minimum for acceptors. The capture cross section for both types of traps was assumed to be 10^{-15} cm^2.We first present the results of the fit between simulated and measured current before the diodes were subjected to forming gas anneal.

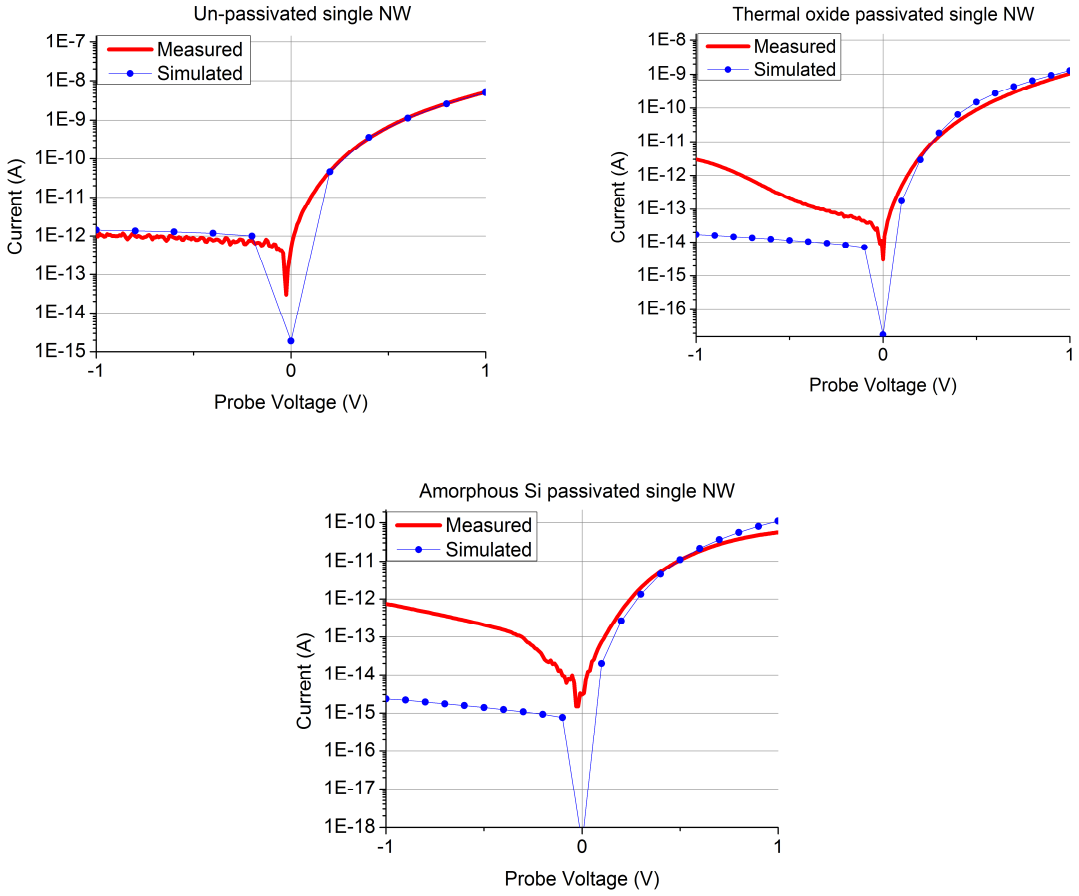


Figure 87. **The fit between measured and simulated I-V characteristics before forming gas anneal for un-passivated, thermal oxide passivated and amorphous Si passivated nanowire Schottky diodes.**

The following values of fitting parameters were used to create the fit shown in *Figure 87*.

- Un-passivated: density donor traps = 3 x 10^{11}cm^{-2}; acceptor traps = 3.5 x 10^{11}cm^{-2}
- Thermal oxide passivated: density of donor traps = 3.75 x 10^{11}cm^{-2} and acceptor traps = 5.1 x 10^{11}cm^{-2}
- Amorphous Si passivated: density of donor traps = 1.19 x 10^{12}cm^{-2} and acceptor traps = 1.44 x 10^{12}cm^{-2}

After forming gas anneal the fitting was performed only for un-passivated and amorphous Si passivated nanowire diodes. The I-V characteristics of thermal oxide passivated nanowires changed so much that it was not possible to fit the forward bias characteristics by using traps density as a fitting parameter. The results are shown in *Figure 88*. The energy level of traps and their capture cross section was still kept unchanged. The density of traps used as fitting parameters for I-V characteristics of amorphous Si passivated and un-passivated nanowire diodes were the following

- Un-passivated: Acceptor trap density = 2.2 x 10^{11} cm^{-2}, Donor trap density = 4.7 x 10^{11} cm^{-2}
- Amorphous Si passivated: Acceptor trap density = 1.39 x 10^{12}cm^{-2}, Donor trap density = 1.16 x 10^{12} cm^{-2}

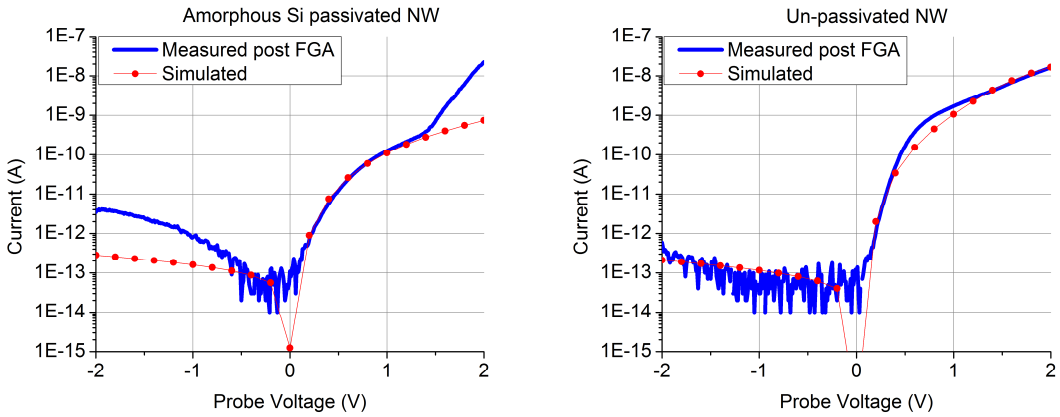


Figure 88. **The fit between measured and simulated I-V characteristics after forming gas anneal for un-passivated, thermal oxide passivated and amorphous Si passivated nanowire Schottky diodes.**

6.8 Conclusions

In this chapter, we have experimented with the Bosch process for the creation of vertical Si nanowires by changing the durations of the etching and deposition cycles. The minimum undercutting was obtained from 6 seconds of etching and 5 seconds of polymer deposition. There can be other ways of modulating the undercut and the smoothness on the sidewalls of the nanowires by changing other parameters like plasma RF power, DC bias on the platen, etc. and there already are several studies available in literature regarding that but, our aim here was to observe the effect of surface conditions on the electrical characteristics of the nanowire. So, we focused on obtaining a reasonable number of nanowire devices which could be tested by changing the surface condition and not on engineering the roughness on the sidewalls.

After fabrication, 21 nm of thermal oxide was grown on one sample, 30 nm amorphous Si was deposited on the other sample and the third sample was left un-passivated. Nickel contacts were formed on top of the nanowires after encapsulating them in spin-on-glass. The DC I-V characteristics obtained from these devices had ideality factors between 1 and 2 indicating a poor fit with the thermionic emission model. Forming gas annealing at 370 C for 10 minutes developed a net negative charge on the surface of thermal oxide passivated nanowires and a net positive charge on un-passivated and amorphous Si passivated nanowires. A small signal AC equivalent circuit has been proposed for the nanowire diode and used to derive the net admittance. Under different bias conditions, the net admittance is approximated qualitatively by observing the measured conductance and capacitance. The capacitive coupling between the nanowire and the large metal contact at its tip seems to dominate the net capacitance of the device under forward bias. Under reverse bias the net capacitance depends on the ratio of G_{Si} to G_{NW} and becomes measurable only when the depletion region spreads from the nanowire on to the surface of the Si substrate. If the depletion region remains limited to the nanowire, the ratio is large and makes the net capacitance too small to be measured.

The flat band voltages of the substrate in case of thermal oxide passivation, amorphous Si passivation and no passivation were +3.2V, -1V and -0.3V respectively. Since the reverse bias current comes from generation of electron-hole pairs inside the depletion region, thermal oxide passivated

nanowires show a current which is much larger than the other two passivations during reverse bias. In order to predict the current through these nanowire diodes, the energy distribution and local density of states of the traps will have to be experimentally determined which has not been performed in this study and is a matter of further research in this field. To summarize, this chapter has described experimental observations of the electrical characteristics of Si nanowire Schottky diodes under different surface passivations. It has highlighted the factors that need to be understood to develop a model which can predict the behavior of a nanowire Schottky diode.

CHAPTER 7

CONCLUSIONS OF THE STUDY

In this chapter we summarize the contribution of this study towards the knowledge about nanowire diodes. There have been several studies in the field of nanowire growth and characterization. Not only semiconductor nanowires but, oxide and even metallic nanowires have been grown bottom-up using the Vapor-Liquid-Solid (VLS) technique. However, relatively few studies have focused on creating a process of fabrication for vertically oriented nanowire devices such that they can be integrated with pre-existing planar devices. Designing such a process is extremely important to bring nanowires into the mainstream of microelectronic device manufacturing. We have developed bottom-up and top-down processes for fabrication of vertical Ge and Si nanowires. There were numerous challenges during the process including but not limited to non-uniform doping, non-vertical growth during VLS and excessive undercutting during ICP etching. Innovative solutions were developed to overcome these problems and in the process of developing those solutions we have highlighted the major differences between nanowire and planar device fabrication.

After fabricating Ge Schottky diodes, the DC current vs. voltage measurements showed deviation from the thermionic emission model which is usually adequate for planar devices. The search for reasons behind the non-ideal behavior led us to concentrate on the effect of surface passivation of the nanowire diodes on their electrical behavior. We improved the vertical dry etching process for fabrication of Si nanowires by making it more repeatable and robust and then analyzed the differences in current between amorphous Si passivated, thermal oxide passivated and un-passivated nanowire diodes. On analyzing the DC I-V characteristics it was once again found that the ideality factors were greater than 1 indicating a poor fit with the thermionic emission model. Forming gas annealing was performed on the diodes to observe the differences due to changes in the charge created by passivation of the defects on the nanowire surface. The net charge density on the surface of the Si substrate and the nanowires was determined from capacitance versus voltage measurements on the MOS structure formed by Hg probe/SOG/Si substrate. C-V measurements performed on the Ni Schottky contact at the tip of the nanowires showed qualitatively, how the capacitive coupling between the nanowire surface and the Ni contact affects the I-V characteristics

under forward bias and the change in width of the depletion region formed inside the nanowire and the Si substrate under reverse bias affects the current in that range of voltage applied to the diode. Finally, simulations were run in Atlas to show that the current predicted by the thermionic emission model was quite different compared to that measured from the nanowire diodes. Donor and acceptor traps on the surface of the nanowire and the substrate were then introduced in the simulations and the measured current under forward bias was shown to fit with the simulations. This emphasizes the fact that traps on the surface of the nanowire and the substrate can increase the ideality factor of the Schottky diode.

Nanowire devices are highly beneficial for scaling down integrated circuits but a reliable process can only be developed after understanding the nature of charge on their surface. The cause of this charge has to be precisely controlled to ensure the performance expected out of the devices. Using the processes developed in this study, more complex nanowire devices can be fabricated. The effect of different surface passivations presented here can be used to engineer the electrical behavior of those devices in a controlled manner. This study has shown how vertical nanowire devices can be fabricated and also highlighted the key factors which need to be studied to control their electrical behavior.

Future work should focus on characterizing the type and energy distribution of electrically active defects on the surface of the nanowire. The capacitive coupling between the surface of the nanowire and the large metal contact at its tip makes it critical to investigate the capacitance of the dielectric being used to encapsulate the nanowires as a function of the frequency of measurement. DC bias and frequency dependence of the coupling capacitance, conductance of the substrate and the nanowire should be worked out for utilizing the equivalent circuit model developed in this study for predicting the capacitance of nanowire diodes and compare them with planar diodes. The ultimate goal should be to build a DC and AC analytical model for a vertically oriented nanowire Schottky diode. Only then can nanowires be integrated with planar devices and more complex devices fabricated using them as the building blocks.

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BIOGRAPHICAL SKETCH

Nishant Chandra earned his Bachelor's degree in Electronics and Communication Engineering from Jaypee Institute of Information Technology University in March 2009. He received his Master of Science degree in Electrical Engineering from Arizona State University in May 2013. In spring 2010 he started the Master of Science degree program in Electrical Engineering at Arizona State University and in fall 2010, integrated it with the Doctor of Philosophy program in Electrical Engineering. In 2010 he worked with Dr. Dieter K. Schroder on four-point probe characterization SiC wafers and published it in the Journal of Solid-State Electronics Elsevier in 2011. While pursuing his degree he worked as a Research Associate in the department of Electrical Engineering. He participated in the Research Experience for Undergraduates (REU) initiative of the National Nanotechnology Infrastructure Network (NNIN) and mentored two students during the summer of 2011 and 2012. He presented a part of his research in the 2012 IEEE Nanotechnology Materials and Devices Conference in fall 2012. During summer 2013 he did an internship in Globalfoundries, a well-known industry for manufacturing electronic devices where he developed a method for ultra-fast (1 microsecond duration) measurement of the degradation in threshold voltage due to bias temperature instability in 20 nm technology node metal oxide semiconductor field effect transistors (MOSFETs). Nishant has been a member of the Eta-Kappa-Nu (HKN) engineering honor society (Epsilon-Beta chapter) at Arizona State University since 2010. He has attended and volunteered to organize several events with the society. Nishant's dissertation, *Nanowire specialty diodes for integrated applications*, was supervised by Prof. Stephen M. Goodnick.