Modeling of Solid State Transformer for the FREEDM System Demonstration

by

Youyuan Jiang

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Graduate Supervisory Committee:

Raja Ayyanar, Chair
Keith Holbert
Srabanti Chowdhury

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ABSTRACT

The Solid State Transformer (SST) is an essential component in the FREEDM system. This research focuses on the modeling of the SST and the controller hardware in the loop (CHIL) implementation of the SST for the support of the FREEDM system demonstration.

The energy based control strategy for a three-stage SST is analyzed and applied. A simplified average model of the three-stage SST that is suitable for simulation in real time digital simulator (RTDS) has been developed in this study. The model is also useful for general time-domain power system analysis and simulation. The proposed simplified average model has been validated in MATLAB and PLECS. The accuracy of the model has been verified through comparison with the cycle-by-cycle average (CCA) model and detailed switching model. These models are also implemented in PSCAD, and a special strategy to implement the phase shift modulation has been proposed to enable the switching model simulation in PSCAD.

The implementation of the CHIL test environment of the SST in RTDS is described in this report. The parameter setup of the model has been discussed in detail. One of the difficulties is the choice of the damping factor, which is revealed in this paper. Also the grounding of the system has large impact on the RTDS simulation. Another problem is that the performance of the system is highly dependent on the switch parameters such as voltage and current ratings. Finally, the functionalities of the SST have been realized on the platform. The distributed energy storage interface power injection and reverse power flow have been validated. Some limitations are noticed and discussed through the simulation on RTDS.

DEDICATION

I dedicate this work to the memory to my best friend, my dear brother *Junhong (EJ) Pan*. You are dearly missed.

ACKNOWLEDGMENTS

First, I would like to express my deepest appreciation and thanks to my advisor, Dr. Ayyanar, for his guidance, encouragement and invaluable support during my study at Arizona State University. I am also grateful to Dr. Holbert and Dr. Chowdhury for serving as members of my committee.

Finally, I would also like to thank my family, friends and classmates for their moral support and willingness to help throughout this process. Without you, none of this would be possible.

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INTRODUCTION

1.1 FREEDM System

Increasing concerns about global energy shortage and climate change have led to rapid development and deployment of renewable energy such as solar and wind energy. Integrating renewable energy into existing power grid and delivering the energy to the consumer centers efficiently becomes big challenge. The Future Renewable Electrical Energy Delivery and Management (FREEDM) systems center proposed such a system and it is called the FREEDM system [1][2]. It is the "internet for energy" based on power electronics, high speed digital communication, and distribution control [3]. The FREEDM system is expected to

- Allow plug and play of any energy resource or storage device, anywhere and anytime
- Manage distributed energy resources and storage devices through Distributed Intelligence
- Pioneer a scalable and secure communication backbone
- Be capable of being totally isolated from the central grid, if necessary, continuing to operate based on 100% renewable energy
- Provide perfect power quality and guaranteed system stability
- Have improved efficiency, operating the alternating current system with a unity power factor.

The FREEDM system center conducts research activities according to the strategic plan [4] as shown in Figure 0.1. The research program is organized into the fundamental research (system theory, advanced storage, and post-silicon power devices), enabling technology development (secured communication, distributed grid intelligence, high-frequency and high-voltage power conversion, and distributed energy storage devices), and system demonstration (large scale system simulation (LSSS), hardware in the loop (HIL), and green energy hub (GEH)).

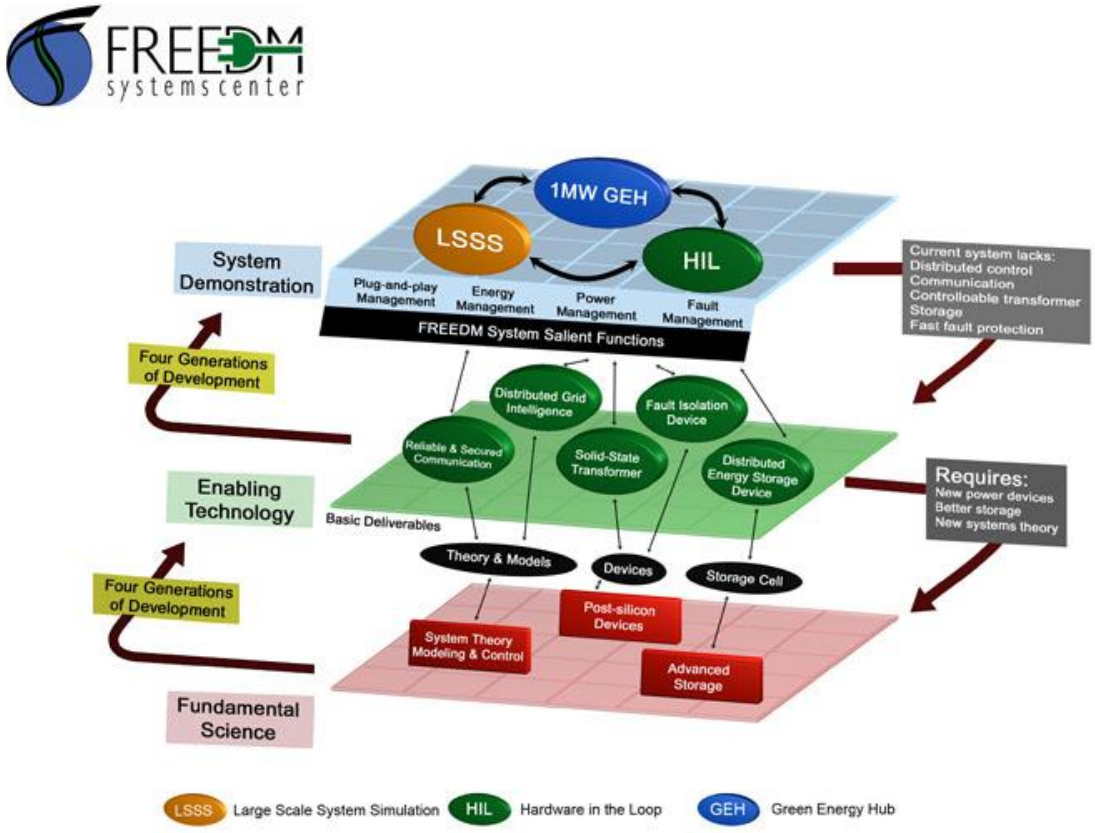


Figure 0.1 FREEDM Strategic Plan [4]

The HIL testbed is one of the three primary testbeds along with the Green Energy Hub (GEH) and the Large Scale System Simulation (LSSS) as shown in Figure 1. The GEH testbed is primarily composed of physical FREEDM components, while the LSSS consists solely of off-line (non-real-time) simulated components. The HIL testbed fills the gap between the two testbeds by providing a platform to study physical and simulated components together. This mixture of real and simulated hardware allows studying components in a more easily controlled and safer environment when compared to testing with all physical components.

1.2 Solid State Transformer

The Solid State Transformer (SST), which is also called power electronic transformer (PET) [5] in some references, is proposed to replace the traditional distribution transformers. It uses the high frequency power electronic converters to change the incoming ac voltage to a high frequency signal, achieving galvanic isolation with a high frequency transformer, and then uses other converters to generate required voltages form the resulting signals. It is an essential component in the FREEDM system. Due to the high frequency operation, compared with the traditional power distribution transformer, the SST has several advantages such as reduced volume and high power density, high efficiency, better power quality and flexible control over the reactive power and active power, and also the

power electronics structure of the SST enables it to integrate with distributed energy resource (DER), distributed energy storage (DES) [6][7].

A lot of topologies have been proposed for the SST [6]-[18]. In [8], an approach to classify the SST topologies and select the appropriate configuration according to the specific needs was introduced. As shown in Figure 0.2, all the possible SST topologies are grouped into four categories: a) single-stage with no DC link, b) two-stage with low voltage DC (LVDC) link, c) two-stage with high voltage DC (HVDC) link, and d) three-stage with both HVDC and LVDC links. In [6], a comprehensive comparison of six representative SST topologies has been conducted. Figure 0.3 and Figure 0.4 show two representative SST topologies. The ac-dc isolated boost based SST belongs to the configuration b) two-stage SST with isolated ac-dc, and the ac-dc dual active bridge (DAB) based SST belongs to the configuration c) three-stage with isolated dc-dc. Both the topologies have good performance and flexible functionalities. But in practice, the leakage inductance of the high frequency transformer makes the ac-dc isolated boost based SST more difficult to implement and control. The three-stage DAB based SST is easier to implement and this topology is selected for the FREEDM system.

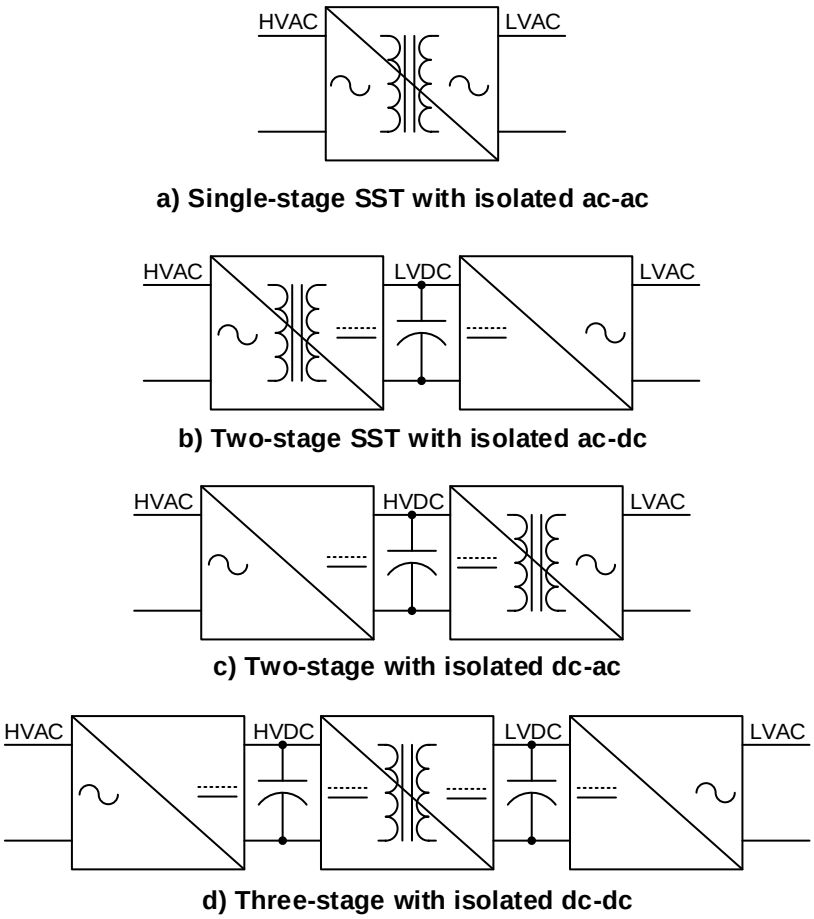


Figure 0.2 SST configurations

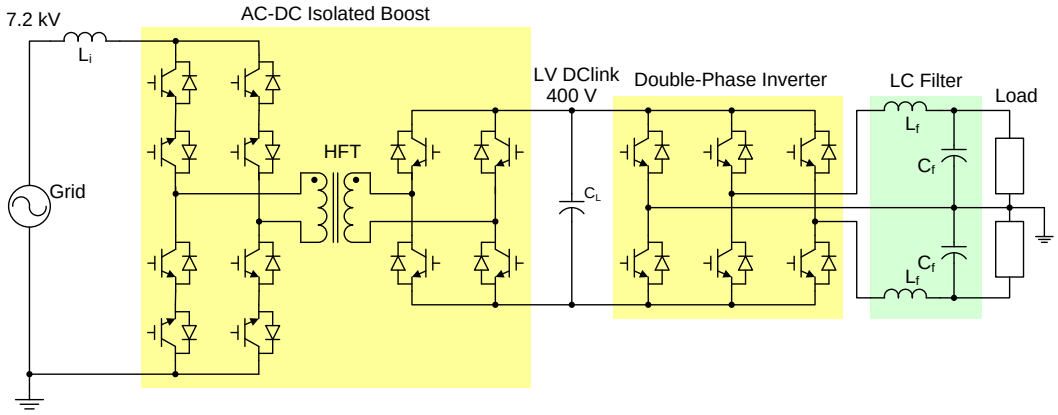


Figure 0.3 AC-DC Isolated Boost based SST

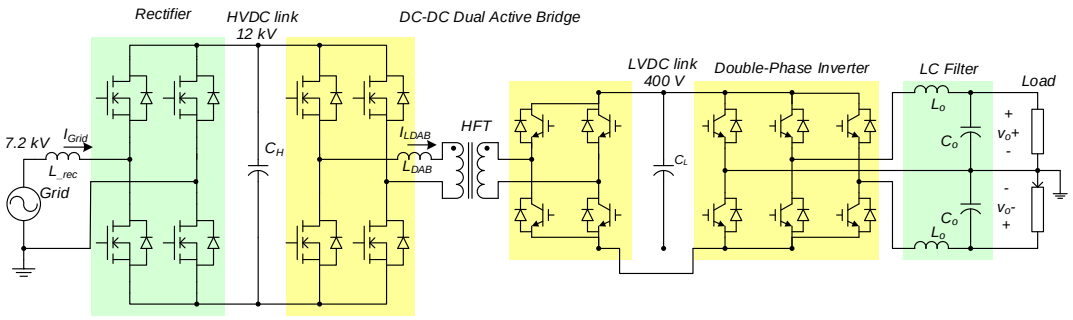


Figure 0.4 Three-stage Dual Active Bridge based SST

1.3 Real Time Digital Simulator (RTDS)

The Real Time Digital Simulator (RTDS) is a fully digital electromagnetic transient power system simulator that solves electromagnetic transient simulations in real time [19][20], it is a combination of advanced computer hardware and comprehensive software and it could be used for high speed simulations, closed-loop testing of protection and control equipment and HIL applications. It is a cost-effective replacement for transient network analyzers and analogue/hybrid simulators.

The RTDS Simulator is currently applied to many areas of development, testing, and studying of the following:

- protective relaying schemes
- integrated protection and control systems
- control system for HVDC, SVC, synchronous machines, and FACTS devices
- general AC and DC system operations and behavior
- interaction of AC and DC systems
- interaction of various electrical installations (e.g. between two HVDC systems)

- demonstration and training

The interface between the RTDS and the external equipment is provided by the Giga-Transceiver Input/Output cards, which are built in the RTDS. They include the Gigabyte Transceiver Analog Input (GTAI), Gigabyte Transceiver Analog Output (GTAO), Gigabyte Transceiver Digital Input (GTDI), and Gigabyte Transceiver Digital Output (GTDO).

RSCAD is a user-friendly interface used to create a working environment familiar to the power system engineer. This software is the main interface with the RTDS hardware and is designed to allow the user to perform all of the necessary steps to prepare and run simulations, and to analyze simulation results.

Specifically, the small time step VSC sub-network in RSCAD makes the implementation of high frequency power electronics converters in RTDS possible. It operates with the time step in the range of 1-4 us and can be interfaced to large scale simulations operating with time step of 50 us. Two- and three-level converters can be freely configured for PWM switching frequency < 2 kHz according the RTDS manual.

1.4 Research Objectives

This paper is a part of the project in the FREEDM system in its effort to construct a HIL test bed in Real Time Digital Simulator (RTDS). The destination HIL system is mainly used to demonstrate the intelligence of the future smart grid, which include distributed grid

intelligence (DGI), intelligent fault management (IFM), intelligent energy management (IEM), intelligent power management (IPM), and some other relative areas.

A five-node test system as shown in Figure 0.5 is proposed in this paper. Four SST units are implemented in RTDS using average model. In order to improve the performance of the simulation, a simplified average model is proposed and verified in this paper. The other one SST unit is implemented as detail switching model in RTDS, and the controller hardware in the loop (CHIL) is built up to control the behavior of the SST unit.

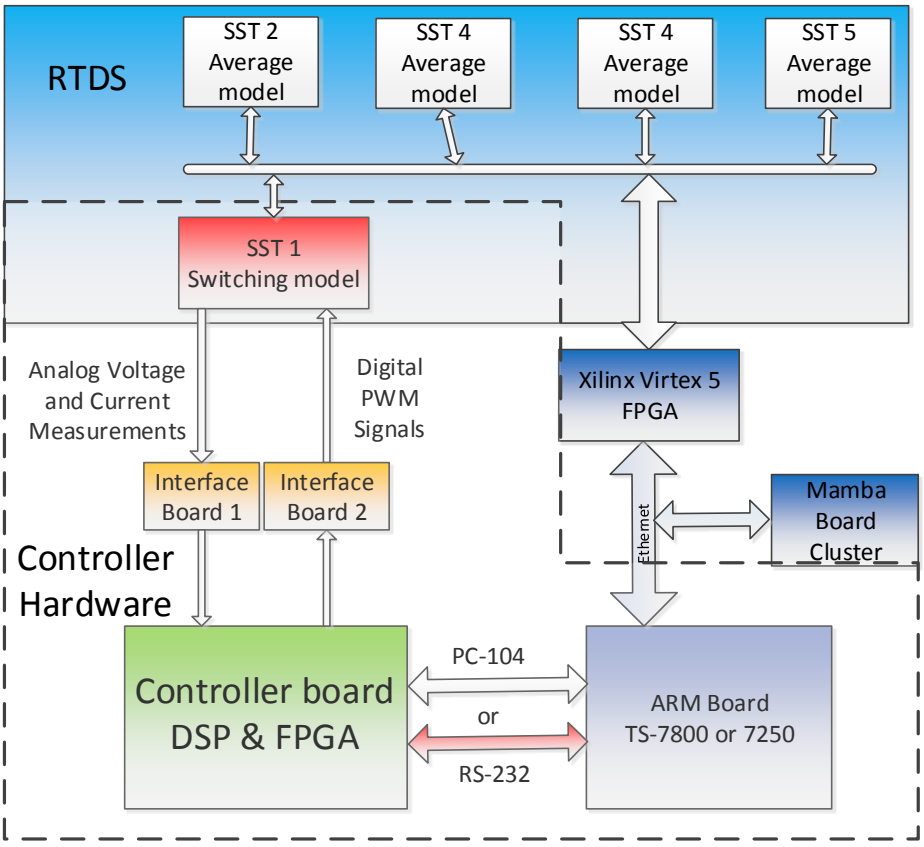


Figure 0.5 A Five-node Test System

1.5 Organization

This report is structured as follows:

In Chapter 1, the FREEDM system, the SST, the RTDS, and the research objectives are presented.

The SST configuration and the energy based control strategy is presented in detail in Chapter 2.

In Chapter 3, a simplified model of SST that is suitable for simulation in RTDS is proposed. The simulation and comparison of the simplified model with the detailed switching model are presented.

In Chapter 4, the controller hardware in the loop implementation of the SST unit in RTDS and the simulation results are presented and discussed.

Conclusions and future work are presented in Chapter 5.

SST CONFIGURATION AND CONTROL STRATEGY

1.6 Solid State Transformer Configurations

In this project a representative three-stage SST configuration shown in Figure 0.1 is adopted. The three-stage topology consists of a PWM full bridge AC-DC converter (the rectifier stage), a DC-DC stage with high frequency isolation, and a PWM DC-AC converter (the inverter stage). Compared with the topology in Figure 0.4, the dual half bridge topology is used for the DC-DC stage instead of dual active bridge (DAB). Both DAB and DHB provide bi-directional power flow and galvanic isolation, and they have the same operation principles and the same control strategies. The reason that the DHB is used here is that the Gen-II SST built at North Carolina State University is using this topology and it is expected that the SST modeled in RTDS is as similar as possible to the actual plant.

The parameters of the SST circuit components are listed in Table 0.1.

Table 0.1 The SST parameters

L_i	R_{Li}	C_H	C_L	L_f	L_o	C_o
0.4 H	2 ohm	66 uF	16800 uF	8.5 mH	0.001 H	120 uF

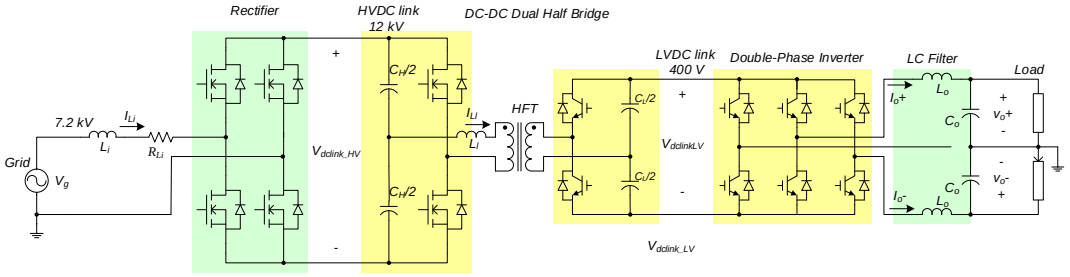


Figure 0.1 Diagram of three-stage SST (DHB based) and its control strategy

1.7 SST Control Strategy

Figure 0.2 shows the traditional negative feedback system with pre-filter. The *P(s)* is the plant transfer function, *K(s)* is the designed controller, and *W(s)* is the pre-filter. The *r* is the reference command, d_i is the disturbance at the plant input, d_o is the disturbance at the plant output, and *n* is the sensor noise which is usually high frequency. The objective of the controller design is to make the output follow the reference command, reject the impact of the disturbances d_i and d_o, and attenuate the sensor noise *n*.

In order to design a feedback control system for a specific plant, the first step is to find the plant transfer function. After this, a typical controller such as proportional integral (PI) controller, K-Factor controller [21], or proportional resonant (PR) controller can be adopted and designed based on the specific requirement for each control loop.

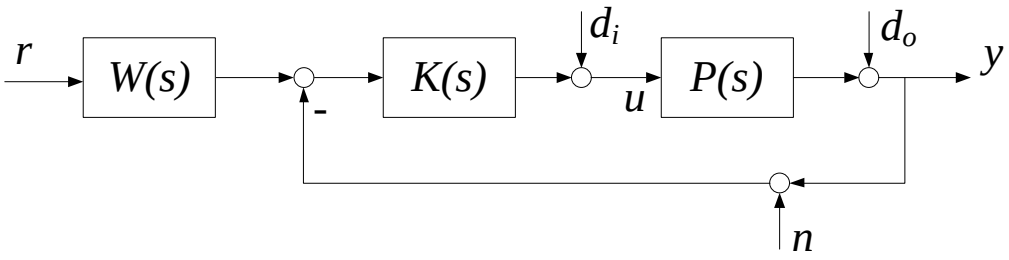


Figure 0.2 Nominal negative feedback system with pre-filter

1.7.1 Cycle by Cycle Average Model

In order to derive the plant transfer functions for the SST, the cycle by cycle average (CCA) model need to be found at the first step. The CCA average model [22] of a power

converter is based on the concept of taking average of the currents and voltages over a switching cycle at steady state, it ignores the switching frequency and higher order harmonics and is accurate enough for general simulations. The volt-second balance principle for inductors and ample-second balance principle for the capacitors are applied during the process of deriving the CCA model for power converters.

Assuming ideal switches with no switching losses, the CCA model can be derived by replacing the AC-DC rectifier stage and DC-AC inverter stage by ideal transformers with turns ratio equals to the corresponding duty ratio and replacing the DHB or DAB by an equivalent gyrator model [7]. The model is shown in Figure 0.3.

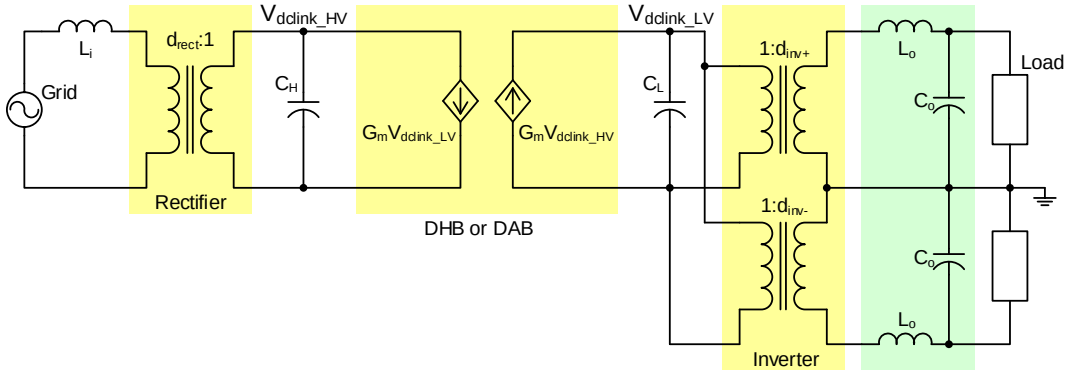


Figure 0.3 Average model of the three-stage SST

Here, L_i is the grid connected inductor, C_H is the equivalent high voltage DC link capacitor, C_L is the equivalent low voltage DC link capacitor, L_o and C_o are the output filter inductor and capacitor respectively, V_{dclink_LV} is the voltage of the low voltage DC link, while V_{dclink_HV} is that of the high voltage DC link. The parameter d_{rec} is the turns ratio of

the rectifier, d_{inv+} and d_{inv-} are the turns ratio of the double phase inverter. The parameter G_m differs for DHB and DAB and can be derived as follows:

For DHB, the power transferred is given by [23]:

$$P_{DHB} = \frac{nV_{dclink\_HV}V_{dclink\_LV}}{4\pi\omega L_l}\phi(\pi - |\phi|) \tag{0.1}$$

The parameter G_m for DHB is given by:

$$G_m = \frac{n}{4\pi\omega L_l}\phi(\pi - |\phi|) \tag{0.2}$$

For DAB, the power transferred is given by [7]:

$$P_{DAB} = \frac{nV_{dclink\_HV}V_{dclink\_LV}}{\pi\omega L_l}\phi(\pi - |\phi|) \tag{0.3}$$

The parameter G_m for DAB is given by:

$$G_m = \frac{n}{\pi\omega L_l}\phi(\pi - |\phi|) \tag{0.4}$$

Here, n is the turns ratio of the high frequency transformer, and ϕ is the phase shift of the DAB or DHB in radius, ω is the switching frequency in rad/s, and L_l is leakage inductance of the DAB or DHB referred to the primary side.

1.8 Energy Based control strategy for three-stage SST

The inverter stage of the SST regulates the AC output voltages with an outer voltage control loop and an inner current control loop. Proportional resonant (PR) controllers [27]

are typically used for the inverter stage to achieve zero steady state error. The DHB regulates the voltage of the low voltage DC link based on the phase shift control technologies, and the rectifier stage interfaces with the power system grid and regulates the voltage of the high voltage DC link. Phase-lock loop (PLL) is typically employed to synchronize with the grid. The inverter stage provides an interface for renewable energy resources with AC output, and the low voltage DC link of the SST provides a port for energy storage devices and DC forms renewable energy resource integration.

Bi-directional power flow is required for the SST, and reactive power control is also necessary which requires the SST to have decoupled active and reactive power control capability. Instantaneous reactive power (IRP) p-q theory [24] is widely used to achieve the goals. In a three phase power system, the instantaneous voltages and currents can be transformed into orthogonal alpha and beta components using the Clark transform and then converted into rotating d- and q- components using the d-q transform. With the d-q transform converting the sinusoidal quantities into DC quantities, and with feed forward control the active power and reactive power can be decoupled and controlled by the d-component of the current or q-component of the current irrespectively depending on the definition of the rotating framework. For the single phase application, the d-q transform can be not applied directly. An imaginary phase which is 90 degree lagging the original phase A is hypothesized to make the d-q transform applicable [9].

Typically, the controllers are designed independently for the three stages and then cascaded together. The interaction among the stages may lead to instability. Usually, the input and output impedances of the cascaded stages need to be examined according to the impedance criterion to ensure stability [7].

A novel energy based control strategy for the three-stage SST is proposed in [25]. By using the energy based control strategy, the control design for the rectifier and DC-DC stage are decoupled, and avoids the need for the impedance checking and the control design process is simplified. This method is applied in this paper. It is noted that in the following sections, most of the equations are taken from [25] and slightly changed in this report.

Figure 0.4 shows the energy based control strategy. Here e_1 and e_2 are the energy of the high voltage DC link and low voltage DC link irrespectively.

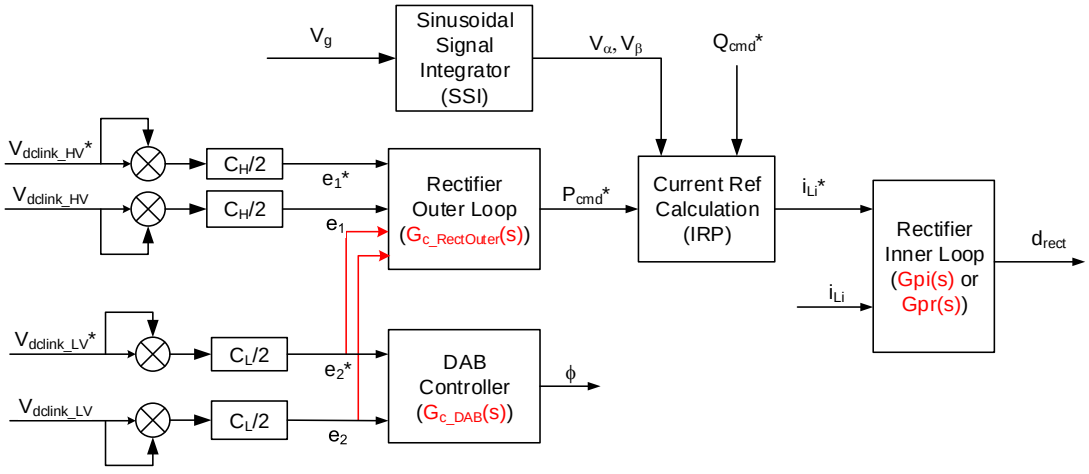


Figure 0.4 Energy based control strategy

1.8.1 Basic idea of the energy based control

In order to explain the energy based control principle, the equivalent model DHB (or DAB) in Figure 0.3 is redrawn in Figure 0.5 which including both the high voltage DC (HVDC) link and low voltage DC (LVDC) link. Here e_1, e_2 represent the energy of the HVDC capacitor and LVDC capacitor respectively, p_i denotes the instantaneous power that flows into the HVDC link capacitor from the rectifier, and p_o represents the instantaneous power that goes into the inverter through the LVDC link capacitor.

$$\begin{aligned} p_i &= P_I - Q_I \cos(2\omega t - \phi_I) \\ p_o &= P_O - Q_O \cos(2\omega t - \phi_O) \end{aligned} \tag{0.5}$$

Here P_I, Q_I, and Φ_I are the AC input active power, reactive power, and power factor angle respectively and P_o, Q_o, and Φ_o are the AC input active power, reactive power, and power factor angle respectively.

By controlling the instantaneous power flowing into and out of the capacitor, the voltage of the DC link can be controlled by controlling the energy of the capacitor. When the energy of the capacitor is constant, the voltage is constant. This is the basic idea of energy based control.

$$p_1 = p_2 = P_{DAB} = \frac{2n}{\pi\omega L_l \sqrt{C_H * C_L}} \phi(\pi - |\phi|) \sqrt{e_1 * e_2} \tag{0.6}$$

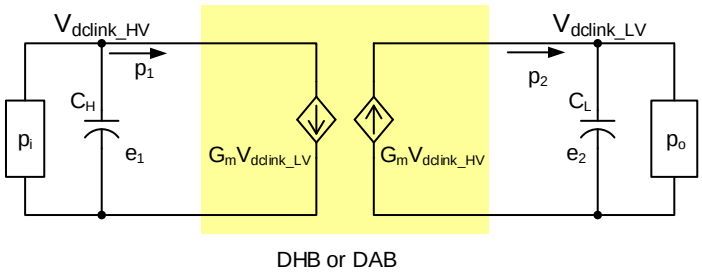


Figure 0.5 Equivalent DHB (or DAB) model including the DC link capacitors

1.8.2 Sinusoidal signal integrator (SSI)

To apply the IRP theory to single phase application, a sinusoidal signal integrator (SSI) [26] is used to generate two orthogonal signals (V_α and V_β) from the grid voltage V_g.

Figure 0.6 shows the block scheme of SSI. Here ω_0 is the fundamental frequency of the grid voltage in rad/sec. The relationship between V_α, V_β and V_g is as follows:

$$\frac{V_\alpha(s)}{V_g(s)} = \frac{2k_a s}{s^2 + 2k_a s + \omega_0^2}$$
$$\frac{V_\beta(s)}{V_g(s)} = \frac{2k_a \omega_0}{s^2 + 2k_a s + \omega_0^2} \qquad (0.7)$$

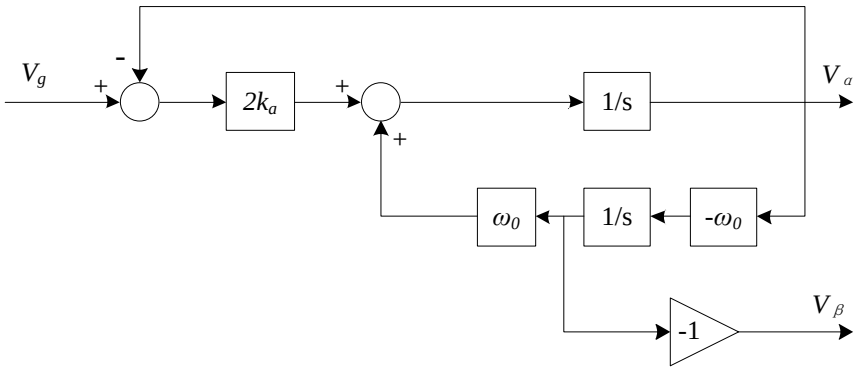


Figure 0.6 Sinusoidal signal integrator filter block scheme

Here, K_α is a constant that used to regulate the performance of the SSI. Typically, K_α = 50 is applied.

A time domain simulation of SSI is shown in Figure 0.7. It is shown that at steady state the α-component is exactly the same with the original signal, which makes the PLL un-necessary, while the β-component has a phase lag of 90 degree.

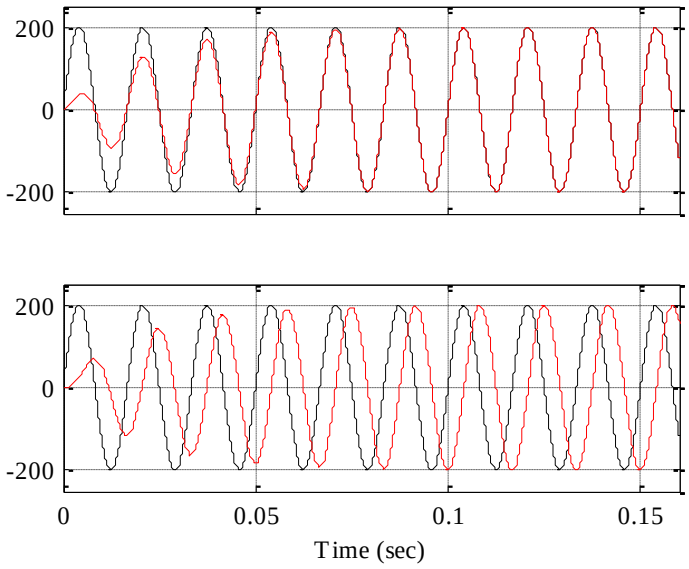


Figure 0.7 Time domain simulation of sinusoidal signal integrator

1.8.3 Current reference calculation

Under the IRP theory, the active power and reactive power can be calculated as:

$$\begin{aligned} P &= i_\alpha v_\alpha + i_\beta v_\beta \\ Q &= i_\alpha v_\beta - i_\beta v_\alpha \end{aligned} \tag{0.8}$$

Here P and Q are instantaneous active power and reactive power respectively; i_α, i_β, v_α, and v_β are the α-β current and voltage signals. From (2.7), the command for the inner current loop could be calculated from the active power and reactive power commands P_{cmd}* and Q_{cmd}*.

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{2}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} \tag{0.9}$$

Here, the gain of "2" in (2.8) is because the average power commands in IRP theory for single phase application are twice of the actual average values.

Because the beta component got from the SSI is a fictitious component, only the alpha component is used for the current reference. Thus the current reference is given by:

$$i_{Li}^* = i_\alpha^* \tag{0.10}$$

1.8.4 Controller Design for the Rectifier Inner Loop

Figure 0.8 shows the block diagram for the current controller and system plant. A proportion resonant (PR) current controller together with the grid voltage feed forward is employed to achieve zero-steady-state-error sinusoidal reference tracking.

The plant transfer function is:

$$G_f(s) = \frac{V_{dclink\_HV}}{sL_i + R_i} \tag{0.11}$$

The designed PR controller is

$$G_{pr\_\mathrm{Rec}}(s) = \frac{0.04189s^2 + 20s + 5953}{s^2 + 142100} \tag{0.12}$$

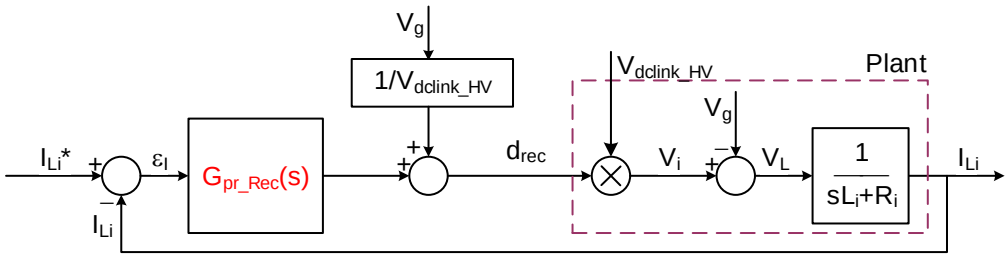


Figure 0.8 The rectifier inner loop

The bode diagram of the PR controller and the open loop transfer function are shown in Figure 0.9 and Figure 0.10 respectively. The bandwidth is 1350 rad/sec (215 Hz), and the phase margin is 69.2 degrees. This provides robustness to the control system.

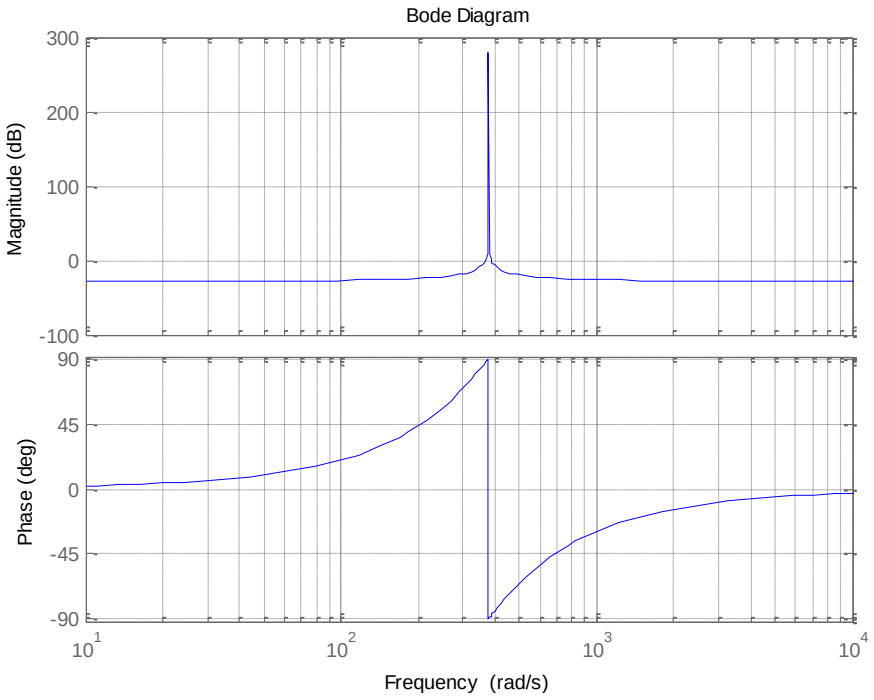


Figure 0.9 Bode diagram of $G_{pr\_Rec}(s)$

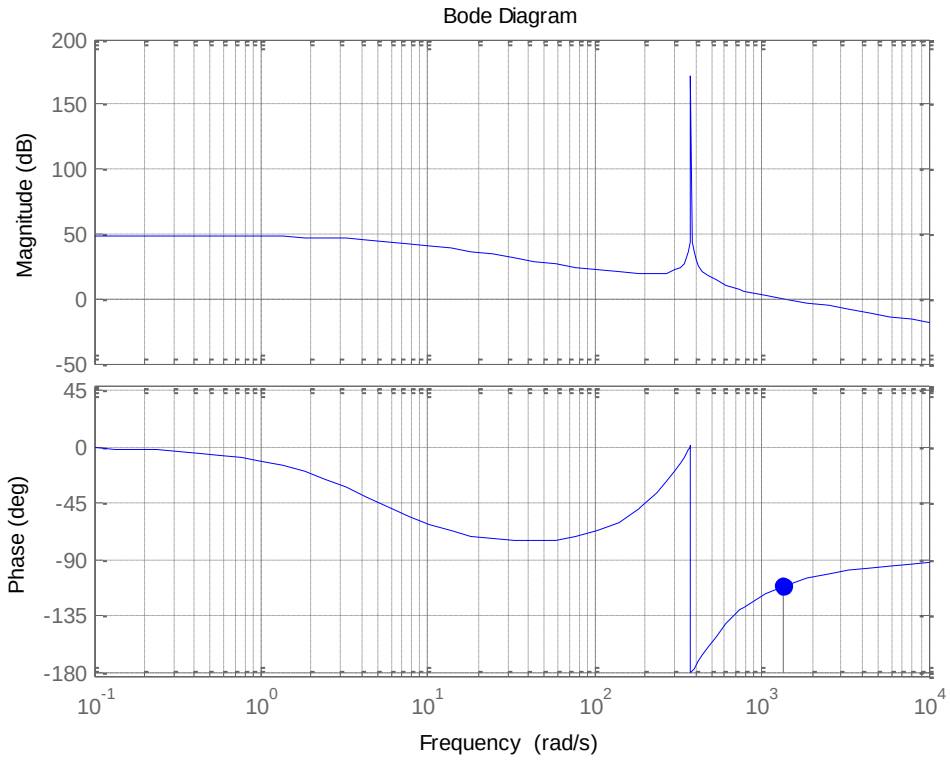


Figure 0.10 Bode diagram of the open loop transfer function $G_f(s)*G_{pr\_Rec}(s)$

1.8.5 Controller Design for the Rectifier Outer Loop

When energy based control is used, the negative feedback control system is shown in Figure 0.11. Here, e_T is the total energy of the high voltage DC link and low voltage DC link and is equal to the sum of e_1 and e_2; e_T* is the reference command for e_T. The high bandwidth inner control loop is treated as a unity gain ($G_{rec\_inner}(s)$ = 1) since it is much faster than the outer loop. The plant transfer function is an integrator with all the other

items been treated as disturbances. To achieve zero-steady-state-error, either PI control or K-factor control could be used. In this project, K-factor control is employed.

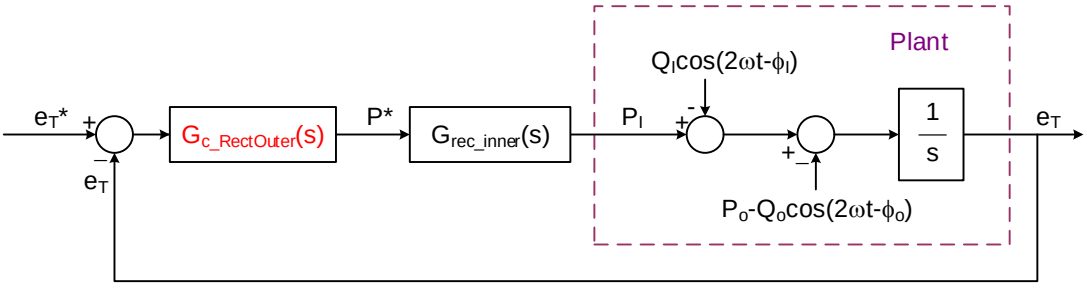


Figure 0.11 The rectifier outer loop

The designed controller is:

$$G_{c\_RectOuter}(s) = \frac{0.0594s + 1}{4.031*10^{-6}s^2 + 0.0009453s} \tag{0.13}$$

The bode diagram of the K_factor controller and the open loop transfer function are shown in Figure 0.12 and Figure 0.13 irrespectively. The bandwidth is 62.8rad/sec (10 Hz), and the phase margin is 60 degrees. This provides robustness to the control system.

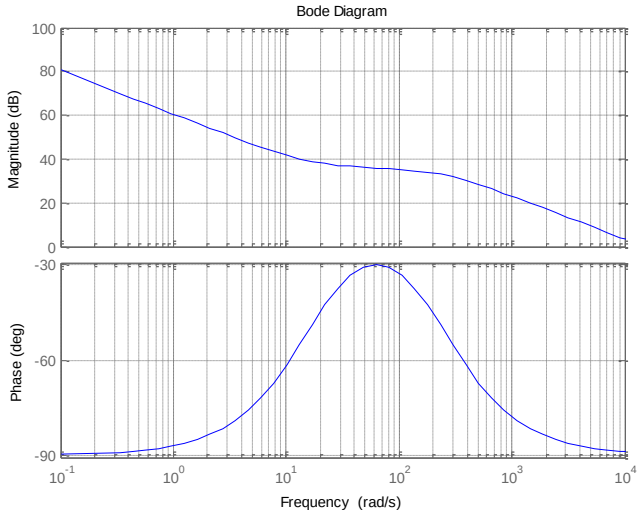


Figure 0.12 Bode plot of $G_{c\_RectOuter}(s)$

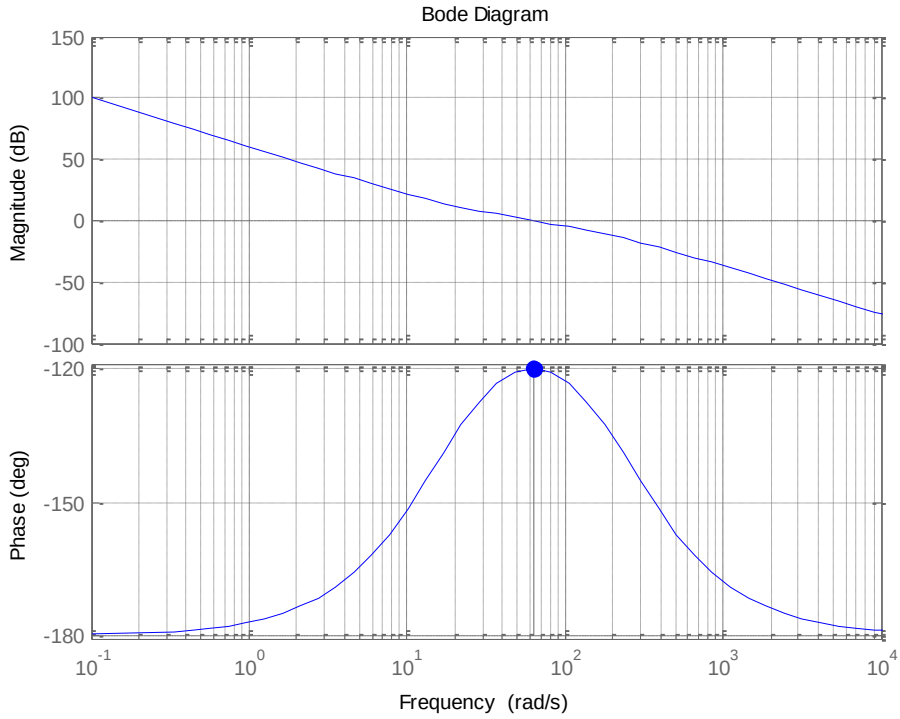


Figure 0.13 Bode plot of the open loop transfer function for rectifier

1.8.6 Control design for the DHB and DAB

Figure 0.14 shows the block diagram for the DHB (and DAB) controller design.

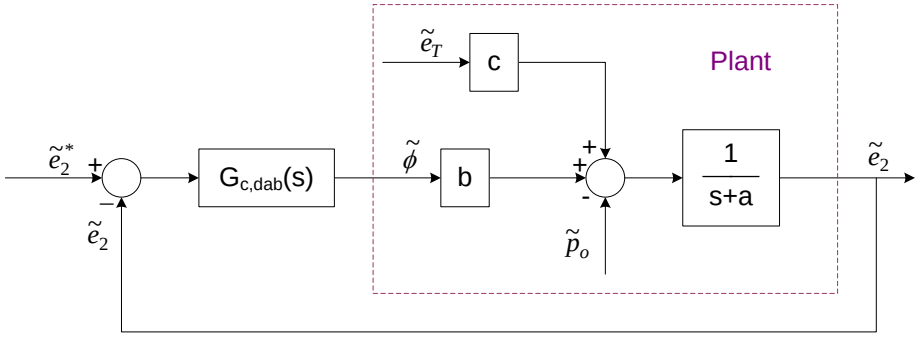


Figure 0.14 The DAB control loop

The differential equation used for the DAB control design is

$$\frac{de_2}{dt} = p_{dab}(e_T, e_2, \phi) - p_o \tag{0.14}$$

Linearizing it gives the small signal equation

$$\begin{aligned} \frac{d\tilde{e}_2}{dt} &= \frac{\partial p_{dab}}{\partial e_2}\tilde{e}_2 + \frac{\partial p_{dab}}{\partial \phi}\tilde{\phi} + \frac{\partial p_{dab}}{\partial e_T}\tilde{e}_T - \tilde{p}_o \\ &= -a\tilde{e}_2 + b\tilde{\phi} + c\tilde{e}_T \end{aligned} \tag{0.15}$$

where,

$$\begin{cases} \dfrac{\partial p_{dab}}{\partial e_2} = \dfrac{k}{2} f(\Phi) \dfrac{1}{\sqrt{(E_T - E_2)E_2}} (E_T - 2E_2) = -a \\ \dfrac{\partial p_{dab}}{\partial \phi} = k\sqrt{(E_T - E_2)E_2}\,(1 - 2|\Phi|/\pi) = b \\ \dfrac{\partial p_{dab}}{\partial e_T} = \dfrac{k}{2} f(\Phi) \dfrac{1}{\sqrt{(E_T - E_2)E_2}} E_2 = c \end{cases} \tag{0.16}$$

where $f(\phi) = \phi(1 - |\phi|/\pi)$ and Φ, E_T, and E_2 are steady state values for the corresponding variables.

The transfer function for the plant is

$$G_{E\_DAB}(s) = \frac{E_2(s)}{\Phi(s)} = \frac{b}{s+a} = \frac{k\sqrt{(E_T - E_2)E_2}\,(1 - 2|\Phi|/\pi)}{s + \dfrac{k}{2} f(\Phi) \dfrac{1}{\sqrt{(E_T - E_2)E_2}} (2E_2 - E_T)} \tag{0.17}$$

The plant turns out to be a first order system and a simple control system can be designed and applied.

$$G_{c\_DAB}(s) = \frac{0.00594s + 1}{0.0002717s^2 + 0.6372s} \tag{0.18}$$

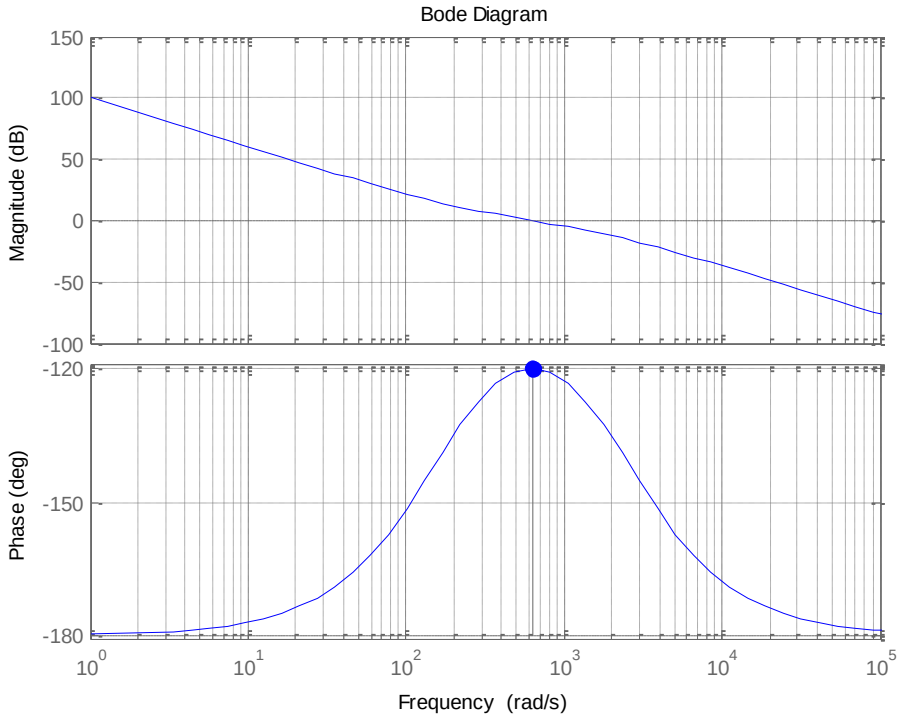


Figure 0.15 Bode diagram for $G_{c\_DAB}(s)*G_{E\_DAB}(s)$

1.8.7 Control design for the Inverter

The main control objective of the inverter is to regulate the ac output voltage to be sinusoidal with correct RMS value (±120 V in this work). The double loop control system is typically applied. A current limiting feature is applied to avoid large current during short-circuit faults at the output. The control diagram is shown in Fig. 2.9. The bandwidth of the voltage loop and current loop are designed to be 100 Hz, and 1 kHz, respectively.

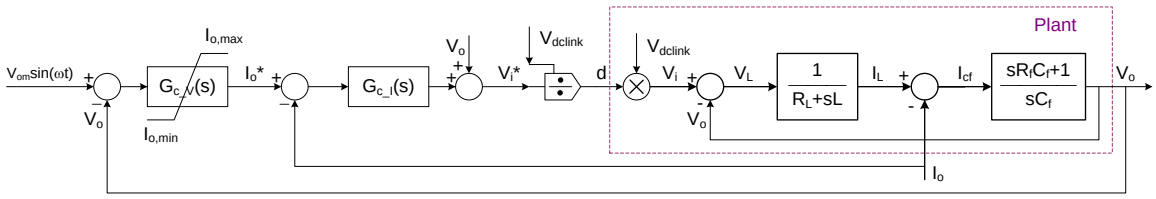


Figure 0.16 Control diagram of the inverter

1.9 Summary

In this chapter, the energy based control strategy is analyzed in detail. The simulation results will be shown in Chapter 3 for comparison with the simplified average model.

SIMPLIFIED AVERAGE MODEL

The simplified average model for SST is derived in this chapter. The simulation results and the comparison with the detailed switching model are presented. The implementation in PSCAD is also introduced.

1.10 Simplified Average Model

The CCA model was introduced in Section 2.2.1. The CCA model still has high bandwidth controllers and hence the simulator has to use a small time step for the simulation. For power system level studies, the high frequency dynamics are usually not of interest and the high bandwidth controllers would take a large amount of time to solve during the simulation. Also for the future smart grid studies, especially when DER and DES are integrated through the SST, the CCA model of the SST would become heavy burden for the computers. This necessitates the need for a simplified average model that could be solved in a reasonable amount of time.

Also, in order to support the HIL system simulation, the SST model in RTDS has to satisfy the following requirements:

- To have the main functionalities such as active power control, reactive power control, and power factor control.
- Provide an integration port for integration of DER and DES.
- To be able to run at a fixed time step of 50 us.

Such a simplified average model of the SST is obtained by the following steps and it is shown in Figure 0.1.

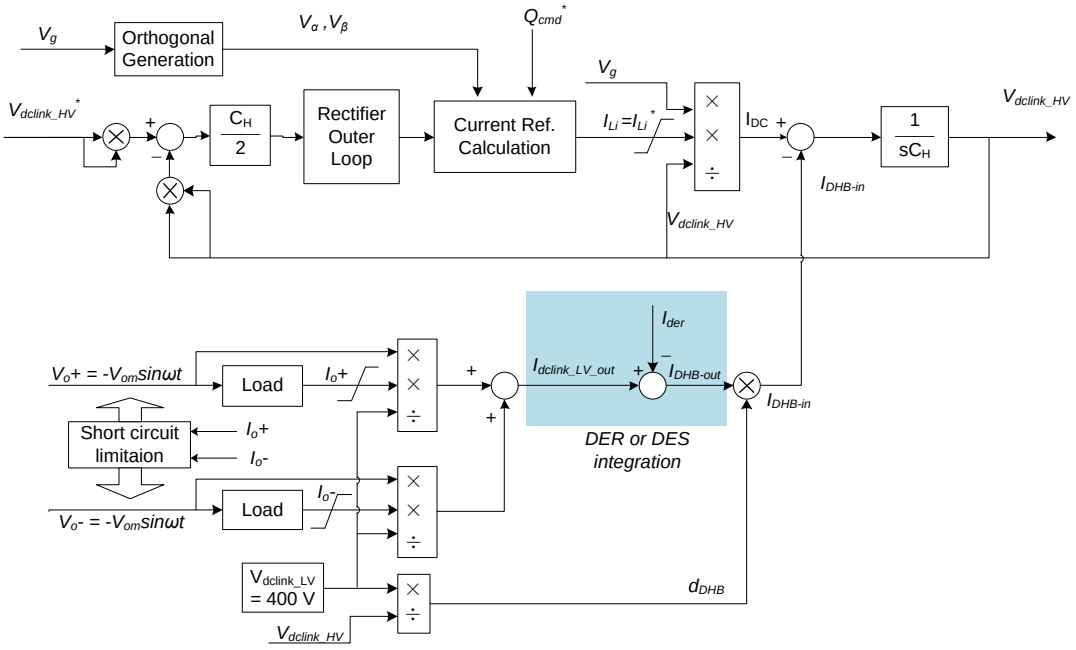


Figure 0.1 Simplified average model of the SST

First, eliminate the high bandwidth controllers. For the SST, both the inverter inner current loop and the rectifier inner current loop have high bandwidths and they are assumed to be ideal and consequently $I_{Li} = I_{Li}^*$.

Second, the control of the rectifier stage and DAB or DHB is decoupled and the dynamics associated with the low voltage DC link and the L, C filters are decoupled with the grid and they do not have significant impact to the grid and can be ignored. The dynamics of the high voltage DC link is relevant to the grid impact and it is kept in this model. Consequently, the voltage of the low voltage DC link is assumed to be constant at 400V (V_{dclink_LV} = 400V), and the inverter output is assumed to equal to the reference

($V_{o+} = -V_{om}sin\omega t$ and $V_{o-} = -V_{om}sin\omega t$). And because the control of the DHB (or DAB) is to maintain the low voltage DC link voltage constant, the DHB (or DAB) are modeled as an ideal transformer with the turns-ratio equal to d_{DHB} as shown in Figure 0.1

Furthermore, the DER and DES are modeled together as an injected current source I_{der}. This provides a convenient way to integrate the DER and DES. The DER and DES could also be modeled as injected power P_{DER}, in which case the power transferred by the DAB or DHB, the power through the inverter, and the DER and DES power should maintain balance all the time since the dynamics on the low voltage dc link are ignored.

The *Current Ref. Calculation* block is discussed in Section 1.8.3 and the orthogonal generation is implemented as shown in Figure 0.6.

In addition, current limitations for both the rectifier and inverter are applied. Also the high voltage dc link is detected to provide over-voltage and under-voltage protection. This is not shown in the Figure 0.1 Simplified average model of the SST.

1.11 Simulation Results

The simplified SST average model has been tested and verified compared with both the CCA average model and the full switching model built in MATLAB and PLECS.

Figure 0.2 shows the implementation of the switching model in MATLAB and PLECS and Figure 0.3 shows the implementation for the simplified model.

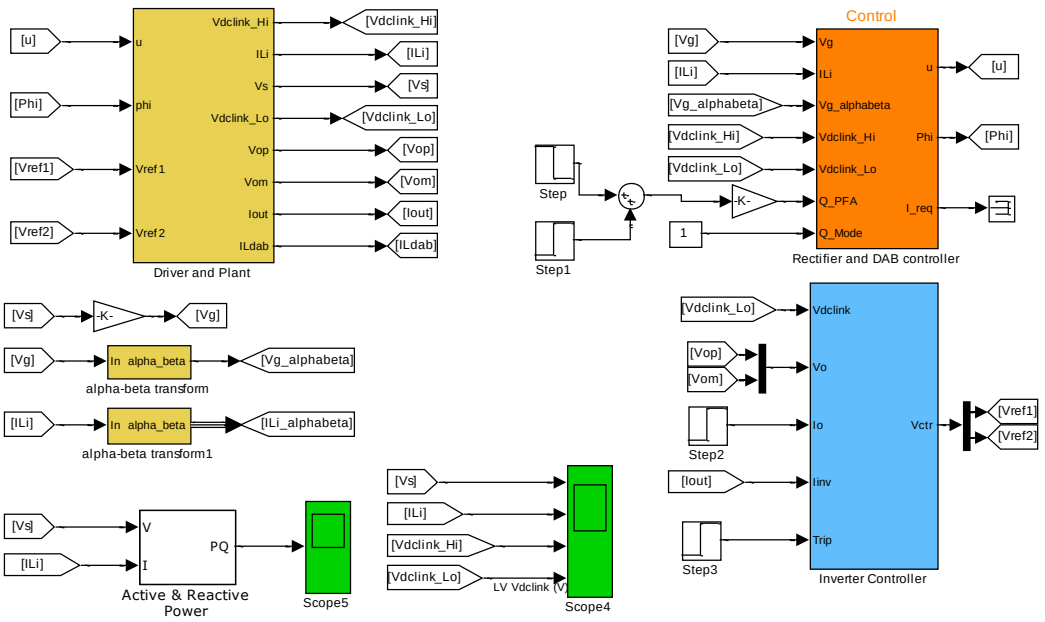


Figure 0.2 Switching model of SST implemented in MATLAB

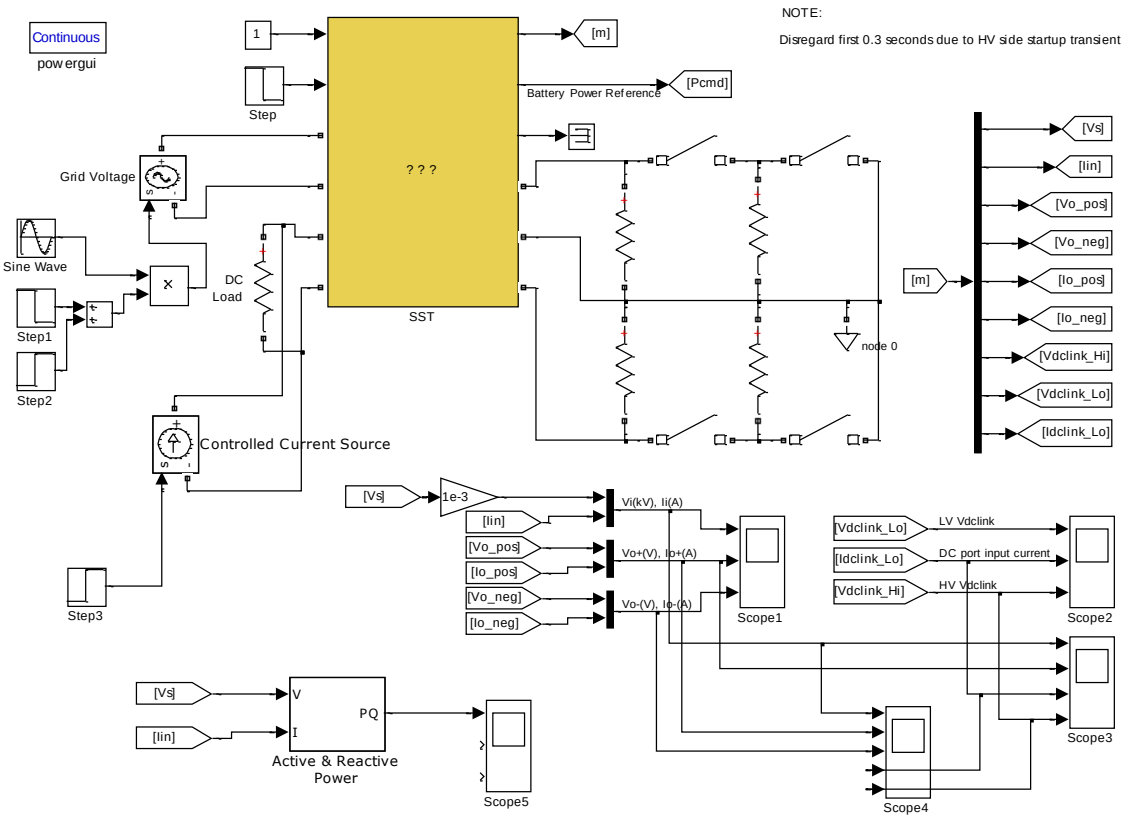


Figure 0.3 Simplified model of SST implemented in MATLAB

The following events are simulated:

- The system is initially full loaded and an AC load step down is applied at t =0.2s.
- Input voltage sag starts at t=0.4s.
- Input voltage sag ends at t=0.6s.
- Reactive power command is applied at t=0.8s to let SST inject a power of 6000 var to the grid.
- A 12 kW DER (modeled as a 30A injected current) is applied at the low voltage DC link at t=1.0s and then removed at t=1.2s.
- The SST absorbs a reactive power of 6000 var at t=1.35s.

The simplified average model and the CCA model are modeled in MATLAB, and the switching model is modeled in MATLAB together with PLECS with switching frequency of 10 kHz. The bandwidths of different controllers are listed in Table 3.1. The simulation duration is 1.5 seconds.

Table 0.1 The SST controller bandwidths

Controller	**Bandwidth (Hz)**
Rectifier outer loop	10
Rectifier inner current loop	200
DAB and DHB controller	100
Inverter outer loop	100
Inverter inner current loop	1000

Figure 0.4 shows the comparison of the dynamic response to the above events by running both the simplified model and full switching model of the SST, and Figure 0.5 shows the plot of active power and reactive power from the three different models.

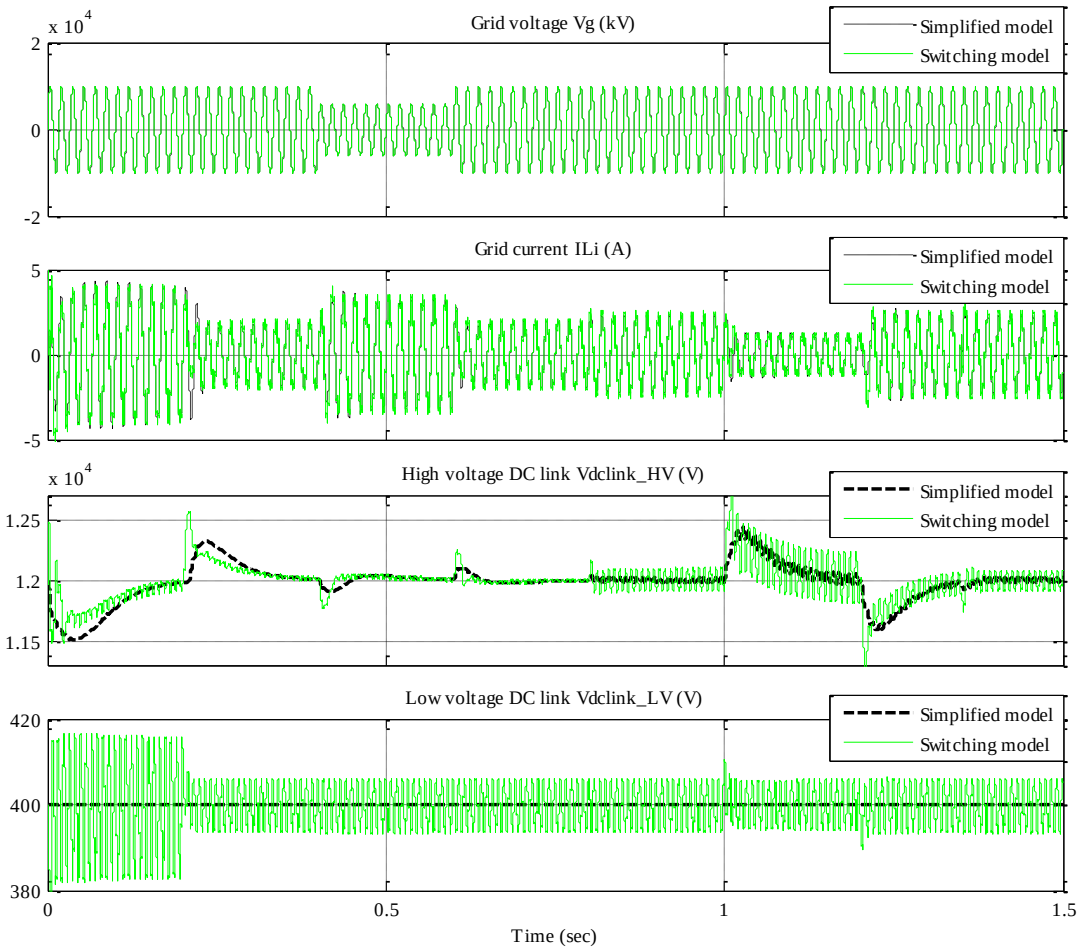


Figure 0.4 SST responses to different contingencies

In Figure 0.4, the grid voltage and current, the high voltage DC link, and the low voltage DC link are plotted. It is seen that the responses from the simplified average model and the detailed switching model are in close agreement with each other. The simulation results using the CCA model are not shown here, but the waveforms from the

CCA and simplified model are almost indistinguishable. From the switching model, the dynamics on the low voltage DC link are very small and it is neglectful. This supports the assumptions made previously that the dynamics is mainly relative to the high voltage DC link and the low voltage DC link dynamics could be ignored. The simplification of the low voltage DC link and the inverter state does not compromise the accuracy of the simulation results.

In Figure 0.5, the waveforms from the simplified and CCA model are almost identical and they are very close to the results from the switching model. It is shown that the simplified model has all the main functionalities of the SST, it supports independent active power and reactive power control, bi-directional power flow, integration of DER and DES, and also it gives accurate simulation results.

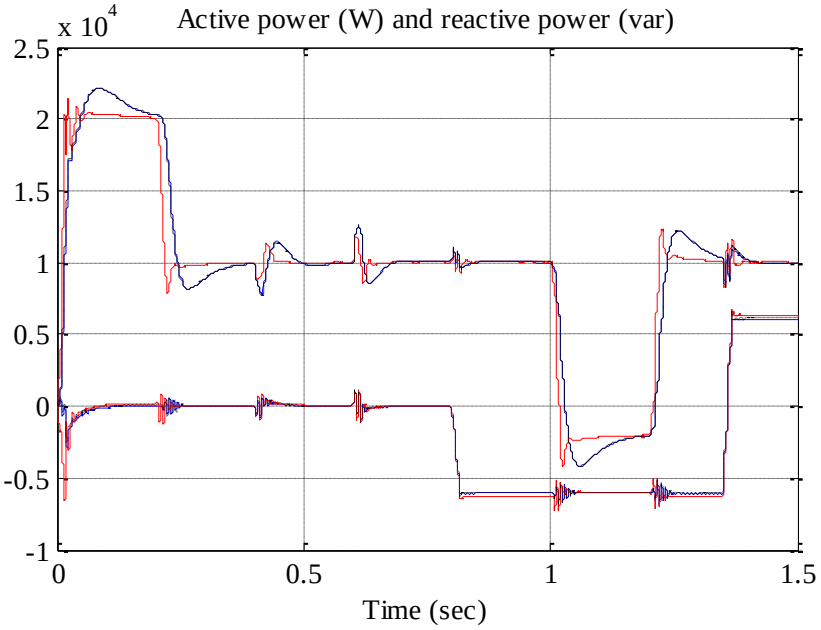


Figure 0.5 Active power and reactive power of the SST

Figure 0.6 simulates a short circuit contingency at the inverter side. The short circuit fault is applied at the positive phase leg at $t = 0.1$s. It is seen that the short circuit current is limited to the maximum current and the voltage is brought to almost zero while the voltage and current on the other output leg are normal; the short circuit voltage cannot go to exactly zero or else the simulation solver will not converge.

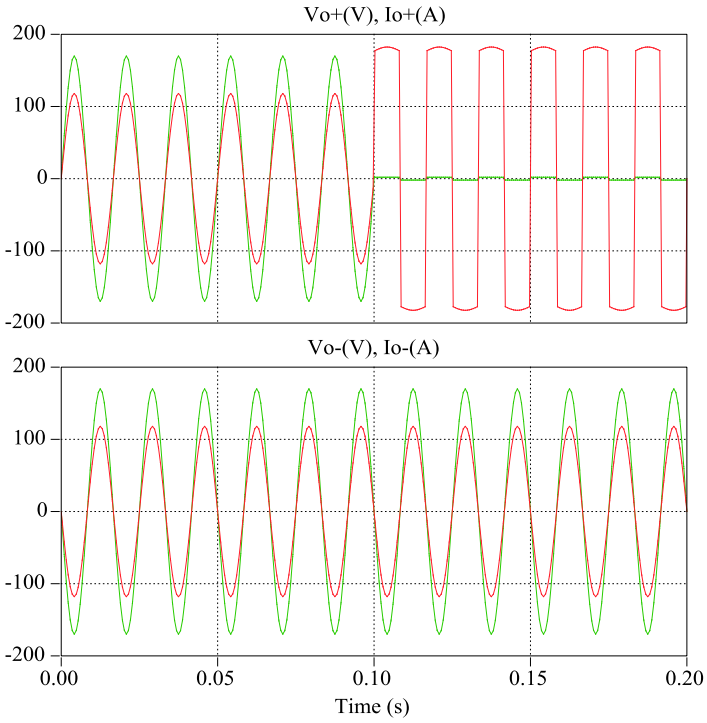


Figure 0.6 Short-circuit response of the inverter stage

The simplified model has been tested with the fixed time step Simulink solvers ode2, ode3, ode4, and ode5 with a fixed time step of 50us. For simulation duration of 1.5 seconds, the simplified model takes only several seconds running with a fixed time step of 50us.

1.12 Implementation in PSCAD

Since the PSCAD has pretty similar work environment as the RSCAD, except that the RSCAD is a real time version, implement the SST in PSCAD would be of great help before it is implemented in the RSCAD.

In this section, both the switching model and simplified model are implemented in PSCAD. During the process, it is found that most of the components implemented in MALTAB and PLECS can be translated into PSCAD by finding the corresponsive components. One challenge encountered during the process is about how to implement the phase shift modulation for DAB and DHB. It is not a problem when the power flows from the rectifier to the inverter, but it would become a problem when the power flows from the reverse direction because the time delay module in PSCAD cannot be applied a negative value. The problem is solved in this report by introducing an artificial phase delay of one cycle (2π rad angle difference) as shown in Figure 0.7.

Here, S1 and S2 represent the firing pulses for the switches on the high voltage side of the DAB (or DHB), while S3 and S4 represent those for the low voltage side. From the figure, it is shown that initially, if no delay is applied, when the power flow if reversed, the firing pulses for S3 and S4 need to lead the firing pulses of S1 and S2 by a certain angle φ, this will make the delay module have a negative value which is not allowed. The solution is an initial one switching cycle time delay (2π rad angle difference) is applied to all the firing

pulses. Then, although the angle φ is still negative, the angle (2π +φ) is positive now. Because S1 and S2 also have a delay of 2π, S3 and S4 is relatively leading S1 and S2 by an angle of φ. This is successfully implemented in PSCAD with multi time delay modules as shown in Figure 0.8.

Both switching model and simplified model of SST are successfully implemented in PSCAD as shown in Figure 0.9 and Figure 0.10 respectively. The same contingencies are applied for the switching model, and the results are shown in Figure 0.11. The results are the same as that simulated in MATLAB and PLECS as shown in Figure 0.4.

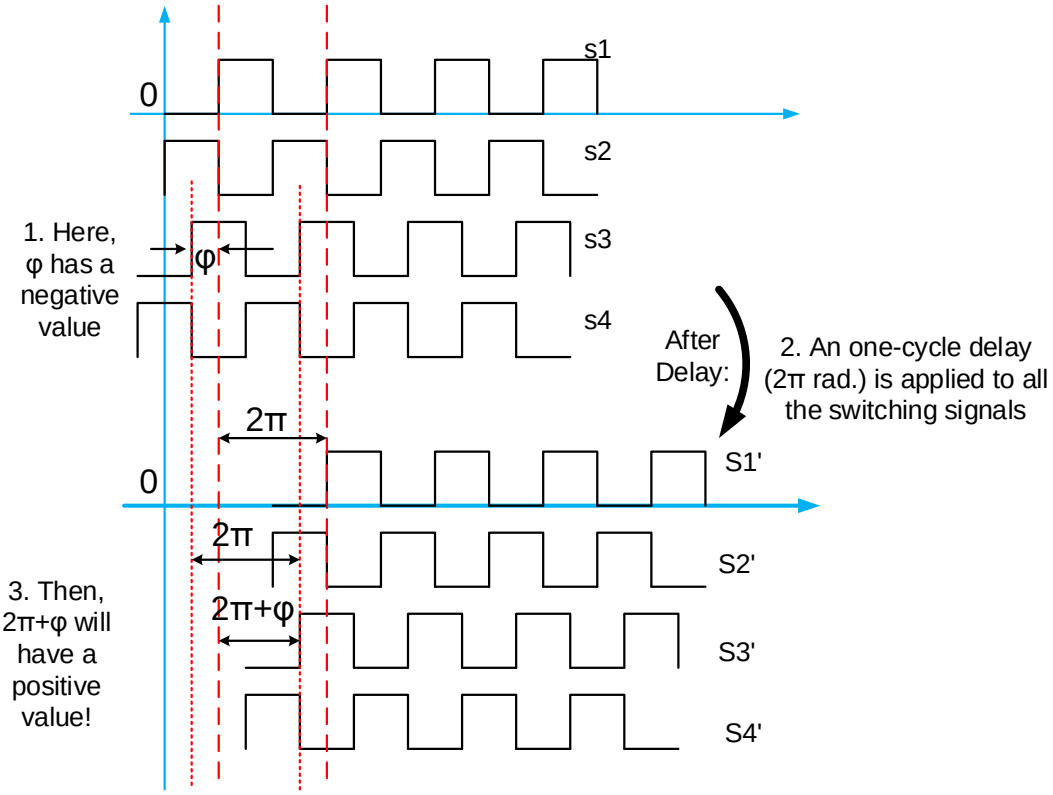


Figure 0.7 Strategy to realize the phase shift modulation in PSCAD

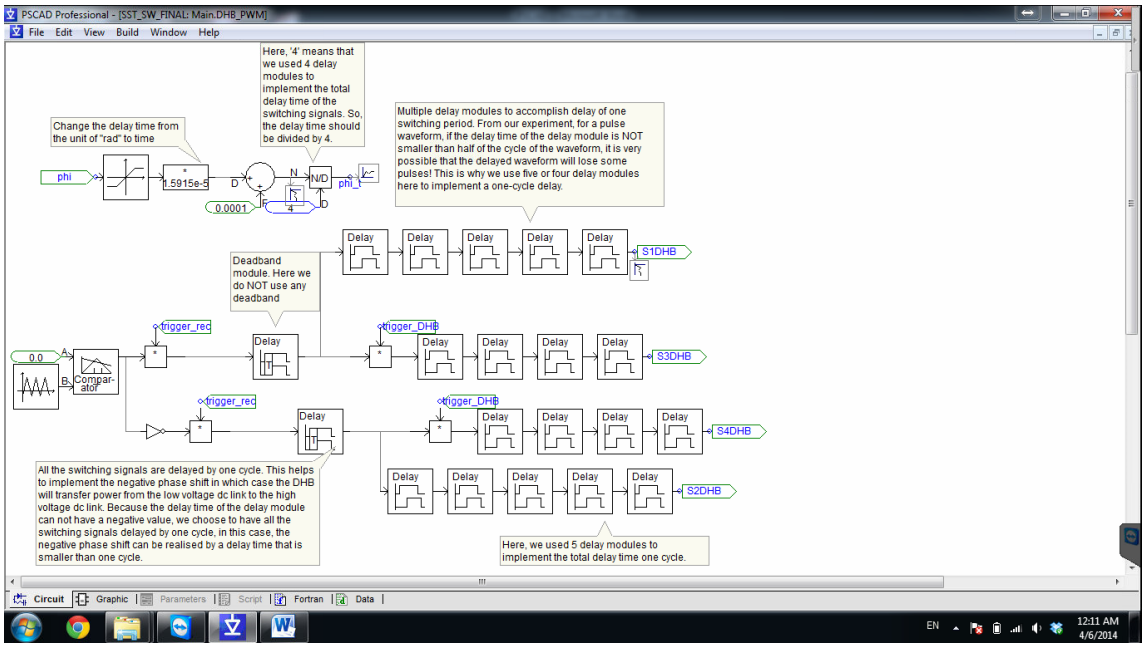


Figure 0.8 Implementation of phase shift modulation in PSCAD

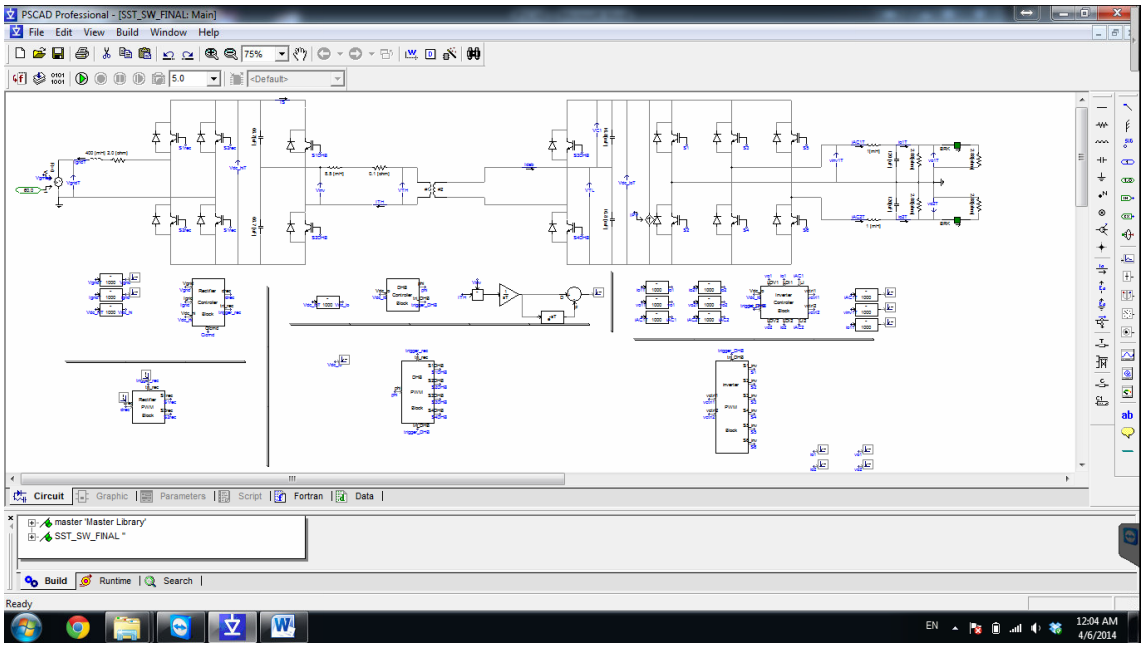


Figure 0.9 Switching model of SST in PSCAD

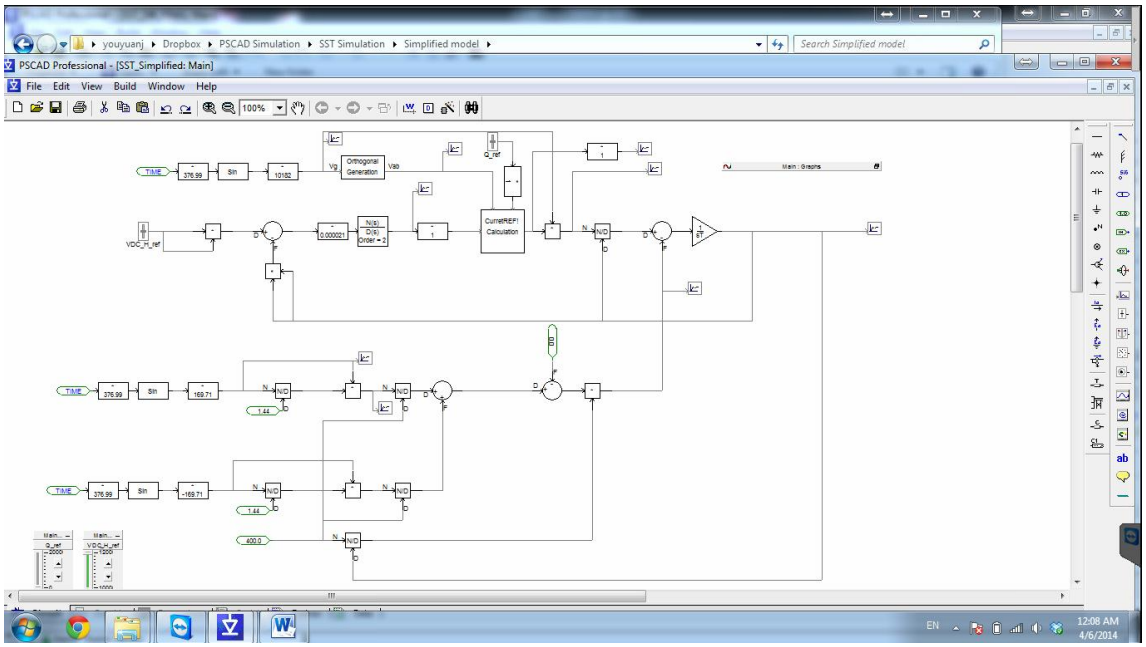


Figure 0.10 Simplified model of SST in PSCAD

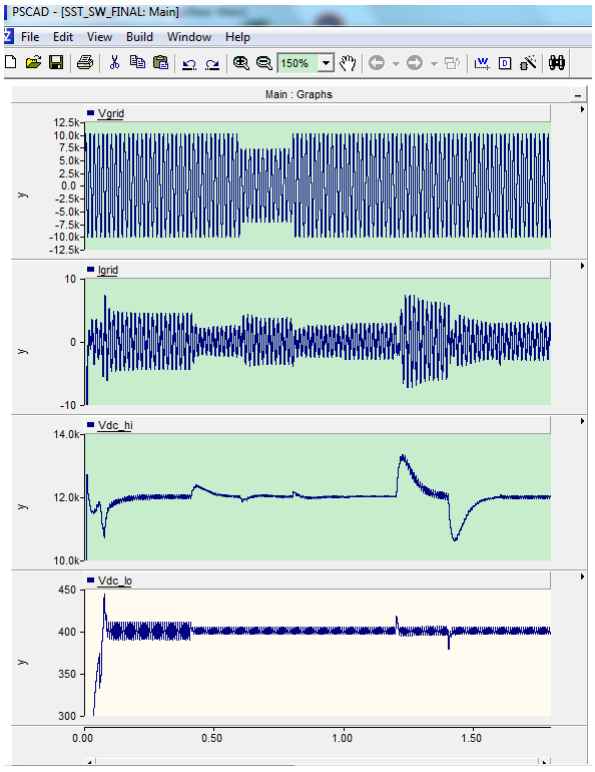


Figure 0.11 Simulation results in PSCAD

1.13 Discussion

The proposed simplified average model is useful for time-domain power system simulation and analysis. Because the high voltage DC link and the rectifier outer loop are kept in the simplified model, the dominant dynamics relative to power system contingencies are kept too. Thus the simplified model is effective to perform power system dynamic studies. Also the simplified model can be used for fault management studies. Both the rectifier and inverter states have current limitations and the high voltage DC link can also be detected to provide under-voltage protection (UVP) and over-voltage protection (OVP). Attention has to be paid when apply short circuit fault at the inverter side, a minimum short circuit impedance of 0.05 ohms has to be applied, or else it will cause convergence problem. The simplified model has the capability of independent active power and reactive power control, but if the SST modeled in the simplified model needs to provide additional control capabilities such as grid voltage support and grid frequency support, additional control block such as frequency or voltage droop control can be added to the simplified model. This is not addressed in this paper.

CHIL IMPLEMENTATION

In this chapter, the CHIL hardware environment setup, the implementation of switching model of the SST, the implementation of the digital controllers, and the simulation results are presented.

1.14 Hardware Setup

Figure 0.1 shows the hardware connections of the CHIL environment for RTDS. It includes two interface boards, and controller board, and the TS-7800 ARM board. The TS-7800 ARM board is used to communicate with the DGI platform and is not included in this paper.

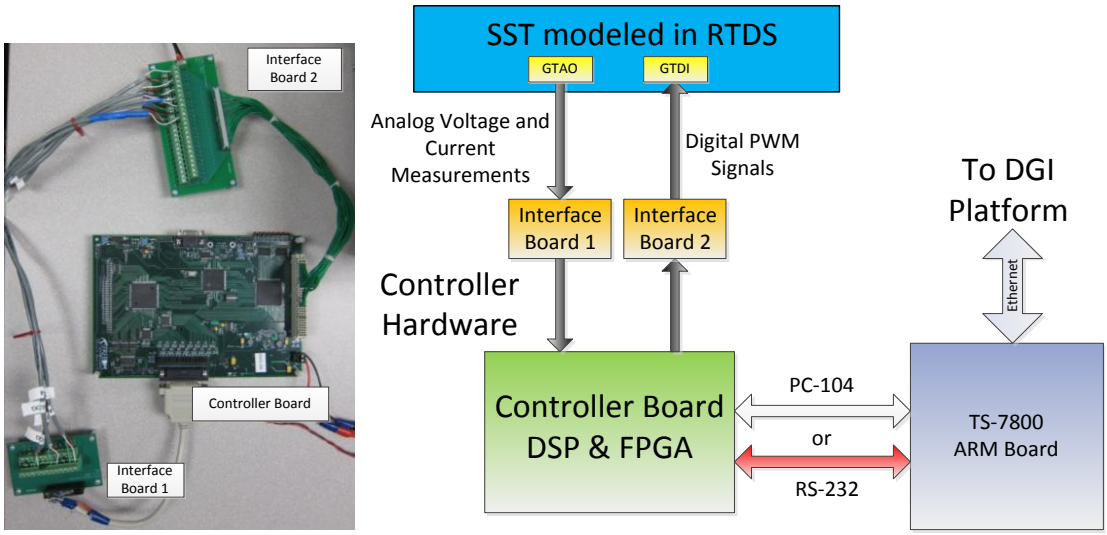


Figure 0.1 The CHIL environment set up for RTDS

1.14.1 Controller board

The picture of the controller board is shown in Figure 0.2. The main components on the board are the DSP chip (TMS230LF28335), two FPGA units (PC 104 FPGA and PWM FPGA) and the AD conversion (ADC) unit. The ADC on the controller board receives the measured signals from the RTDS through the interface board 1 and send the signals to the PC 104 FPGA. The AD 7606 chip is used for the ADC, it is an 8 channel 16-bit ADC, and has an input range from -10V to +10V. The PC 104 FPGA deals with the signals from ADC and delivers them to the DSP board. The PC104 connector is also connected to the PC104 FPGA, it is mainly used for high speed communication. Since complex FPGA code needs to be developed to realize the PC104 communication, RS 232 serial communication is used instead. The controllers are implemented in the DSP. The DSP generates the required control signals (duty ratios for the switches), converts them into PWM signals, and deliver them to the PWM FPGA. The PWM FPGA assigns the PWM signals to pre-defined pins on the PWM connector and transfer them to the RTDS through the interface board 2.

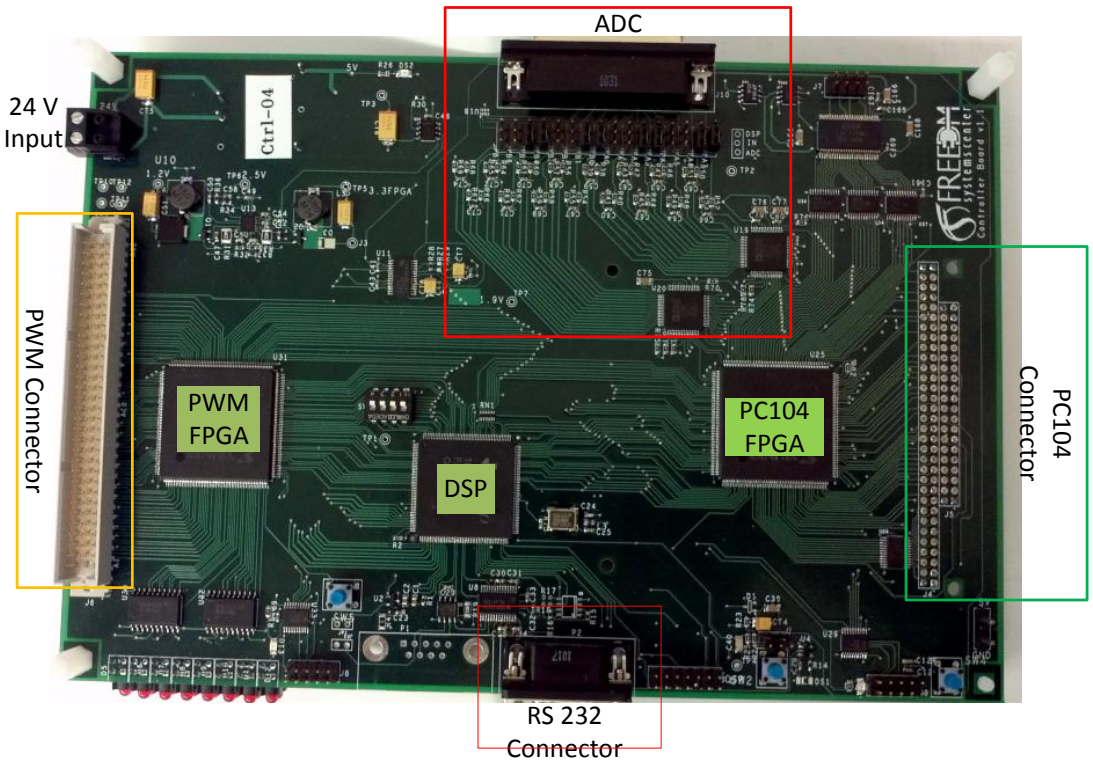


Figure 0.2 The picture of the controller board.

1.14.2 GTAO and GTDI cards and Interface boards

The GTAO provides optically isolated analogue output from the simulation to external equipment. The card has a total of 12 outputs which can be sent from either regular or small timestep simulations running on the RTDS. The GTAO uses 16-bit d/a's and can range between a maximum of ±10 Vpeak. Since the ADC on the controller board has exactly the same input voltage range, the interface board 1 is pretty simple and only used to map the signals. Figure 0.3 shows the diagram of the GTAO.

The GTDI provides optically isolated digital input to the real time simulation from external equipment. The GTDI input is current driven (~10 mA), allowing a wide range of input voltages to be connected to the card by providing the appropriate value of current limiting resistor. Figure 0.4 shows the plot of the GTDI designed interface board 2 diagram, Figure 0.5 shows the schematics of the interface board 2.

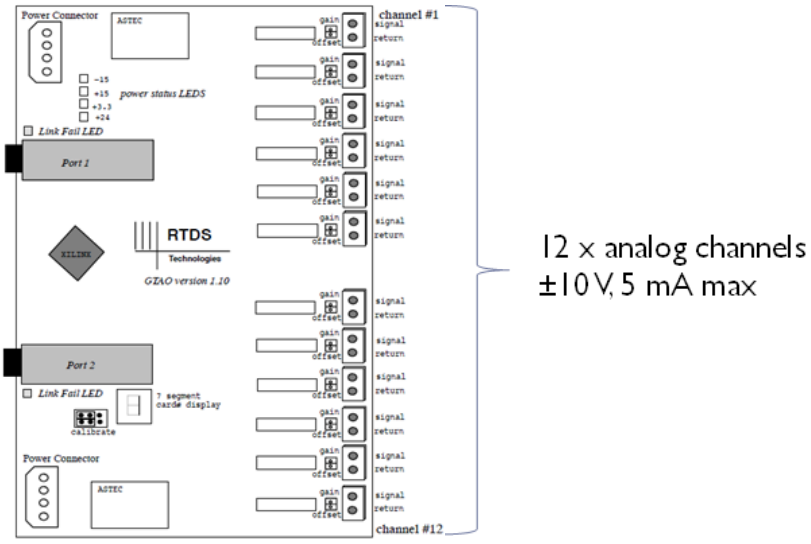
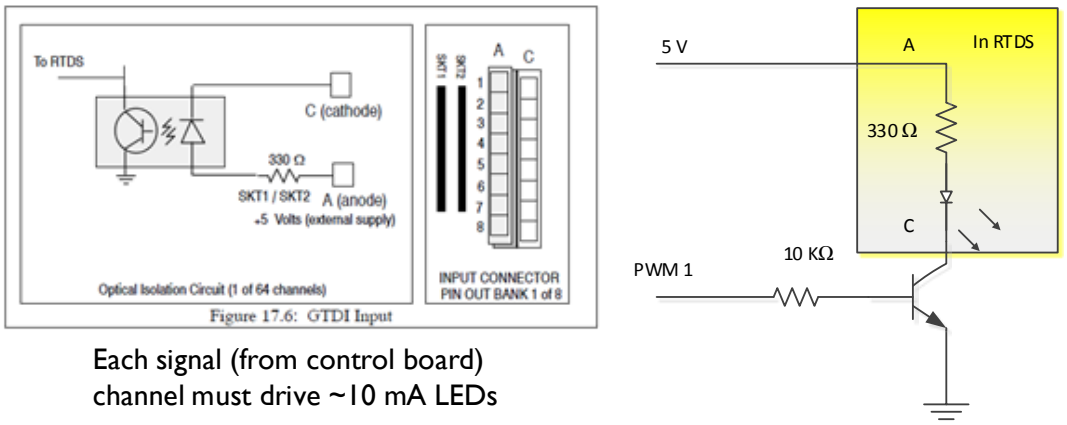


Figure 0.3 Diagram of GTAO



A) GTDI Diagram

B) Diagram of Interface Board 2

Figure 0.4 Diagram of GTDI and the interface board 2

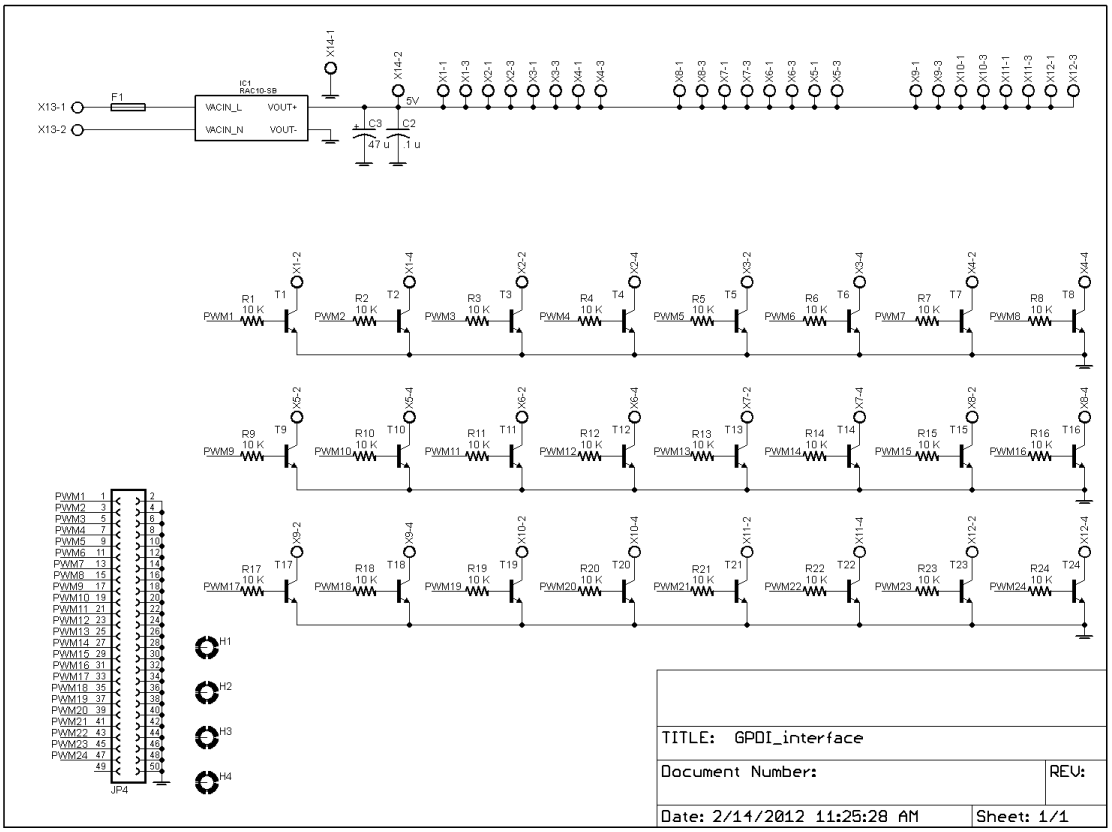


Figure 0.5 Schematics of the interface board 2

1.15 SST Settings in RTDS

1.15.1 Switch settings in RTDS

In the small time-step VSC sub-network of RTDS, the switch (it is called valve in RTDS) is modeled as a small inductance *L* while it is on and as a large capacitance *C* in series with a resistance *R* while it is off. The philosophy of the RTDS small time-step real time simulation is that by properly choosing the values of the inductance, capacitance and resistance such that they have the same conductance when represented using the Dommel

algorithm. Thereby the Dommel network conductance will not change when the switches switched between the on and off states [20][28]. The values of *R*, *L*, and *C* could be solved according to:

$$L = \frac{\sqrt{2}(\Delta T * F)v}{i} \tag{0.1}$$

$$C = \frac{(\Delta T * F)^2}{L} = \frac{\Delta T * F}{\sqrt{2}} \frac{i}{v} \tag{0.2}$$

$$R = \frac{2L}{\Delta T} - \frac{\Delta T}{2C} = (2\sqrt{2}F - \frac{\sqrt{2}}{2F}) \frac{v}{i} \tag{0.3}$$

$$\tau = RC = 2\Delta T F^2 - \frac{\Delta T}{2} \tag{0.4}$$

Here F is defined as $F = \frac{1}{2(\sqrt{\delta^2+1}-\delta)}$, which is only dependent on δ, the selected damping factor, ΔT is the RTDS small time simulation step, v is rated switch voltage, and i is the rated switch current. The parameter δ has a typical range of 0.85 to 1.33 according to [20]. It is said to be between 0.7 and 1.33, while 0.9 is recommended by RTDS as the default value. The following section will show that the best choice of the damping factor should be the smallest value that is allowed in RTDS, which is 0.7. Here, the time constant τ represents the rise time of the voltage over the switch when the switch turns from on state to off state. To get a better performance of the simulation, we expect the time constant to be as small as possible. Figure 0.6 shows that F^2 increases as δ increases. Since in (4.4) the time constant τ increases when F^2 increases, it is concluded that the time constant will increase when the damping factor increases. It can also be

concluded that the parameters L, C, and R will increase when the value of the damping factor δ get increased. Table 0.1 lists several sampled calculation results.

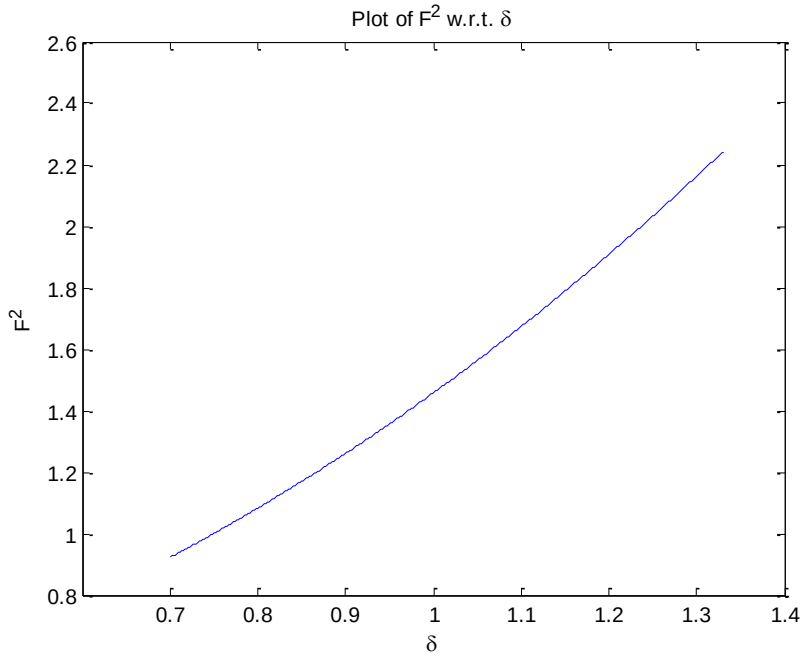


Figure 0.6 The relationship between F^2 and δ.

Table 0.1 Different factor relationships with the damping factor

δ	F	F^2	$2\sqrt{2}F - \frac{\sqrt{2}}{2F}$
0.7	0.9603	0.9222	1.9799
0.9	1.1227	1.2604	2.5456
1.33	1.4970	2.2410	3.7618

Typically the RTDS sub-networks operate with small time steps in the range of 1-4 us. In this paper, the simulation time step is found to be $\Delta T = 2.222\ \mu s$ while the large time step is 50 μs. When δ = 0.7, the minimum time constant is obtained to be τ_{min} =

2.9873 μs, while δ = 0.9, τ = 4.4902 μs. This means that if the damping factor is chosen to be 0.9, the switch voltage will take $5 * \tau$ = 22.451 μs to rise up which is typically smaller than 1.5 μs for actual IGBT devices [22]. In order to make the rise time as small as possible, the minimum value of the damping factor is used. But this is not strict since the overshoot is not considered.

For the selection of voltage and current over and through the switch, the RTDS manual suggests to choose the rated voltage and current, and then adjust the parameters to get the best performance. In the case of this paper, after iteratively adjustments, the final selection of the parameters for the SST is listed in Table 3. The equivalent *R*, *L*, and *C* are also shown in Table 0.2. Figure 0.7 shows the screenshot when setting the switch parameters.

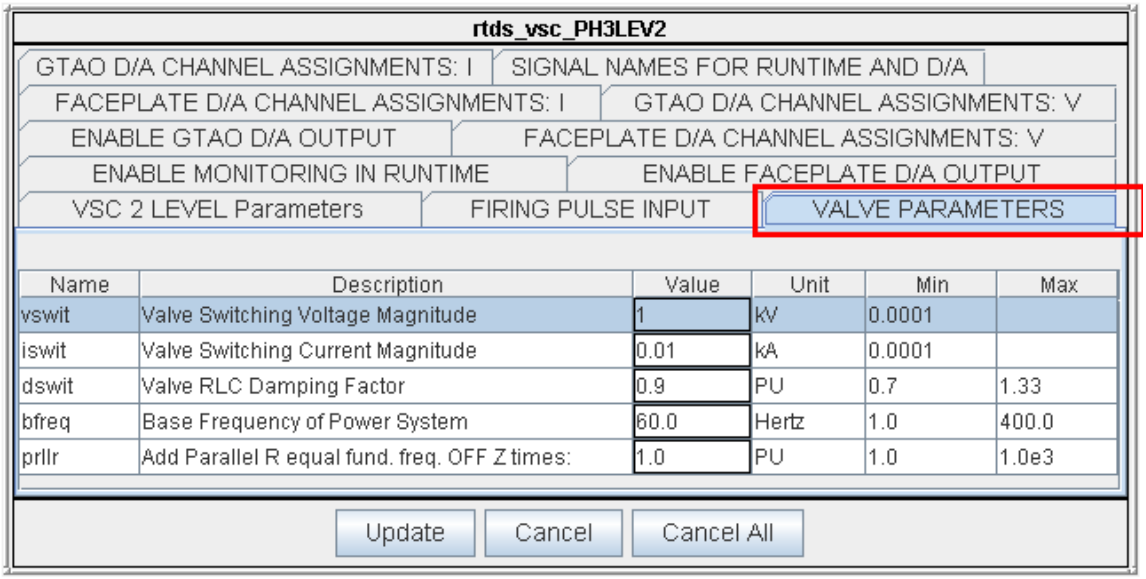


Figure 0.7 Screenshot of the switching settings in RTDS

Table 0.2 Switch settings and equivalent parameters in RTDS

Parameters	REC	DHB1	DHB2	INV
Vswit (Valve Switching Voltage Magnitude)	12 kV	12 kV	0.4 kV	0.4 kV
Iswit (Valve Switching Current Magnitude)	0.0004 kA	0.0018 kA	0.75 kA	0.0125 kA
Valve ON inductance (H)	0.0905406	0.0201201	1.60961e-6	9.65766e-5
Valve OFF series capacitance (uF)	5.0300e-5	0.000226351	2.82939	0.0471565
Valve OFF series resistance (ohm)	59397	13199.3	1.05595	63.3568

1.15.2 The transformer settings in RTDS

The settings of the transformer are obtained by transforming the values listed in Table 1 to per unit values based on the rated voltage and current of the transformer. Table 0.3 gives the setting of the transformer in RTDS. Figure 0.8 shows the screenshot when setting the transformer in RTDS.

Table 0.3 The transformer settings in RTDS

Parameters	Description	Value
Vw1t	Rated Winding 1 RMS Voltage	6.0 kV
Vw2t	Rated Winding 2 RMS Voltage	0.2 kV
MVA	Rated 1-Phase Transformer MVA	0.02 MVA
Frqt	Transformer Base Frequency	2000.0 Hz
Rput	Total Winding Resistances	0.00005556 pu
xput	Total Winding Reactances	0.0593412 pu

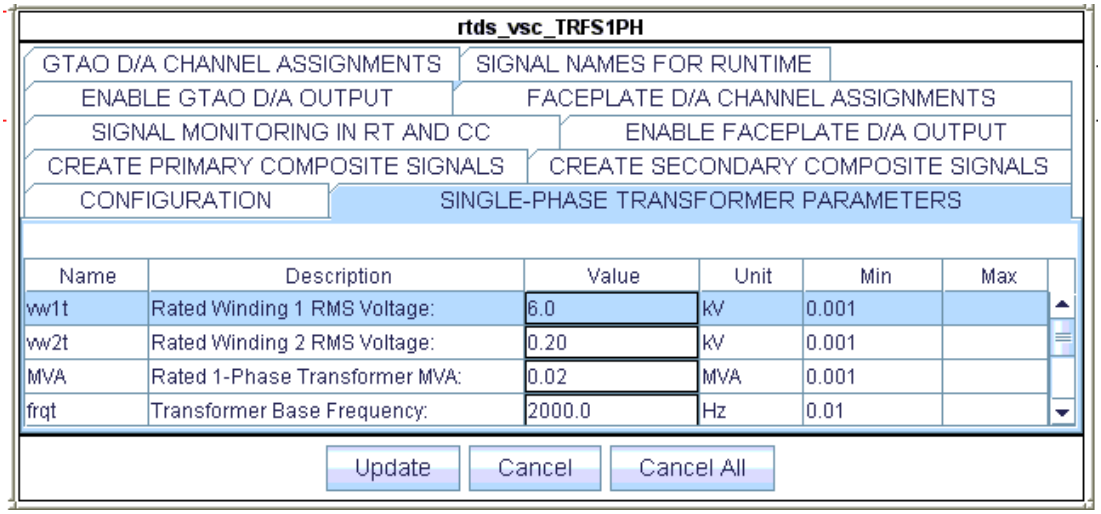


Figure 0.8 Screenshot of the transformer settings in RTDS

1.16 Simulation Results and Discussions

1.16.1 Simulation Results

Since the DSP supports maximum 12 PWM outputs, the SST simulated here has been modified as shown in Figure 0.9. The double phase inverter in Figure 0.1 is modified to be a full bridge inverter. The circuit parameters are the same as listed in Table 0.1. By this way, the total switch number is reduced to 12 and the internal PWM module of the DSP can be used to generate the firing pulses.

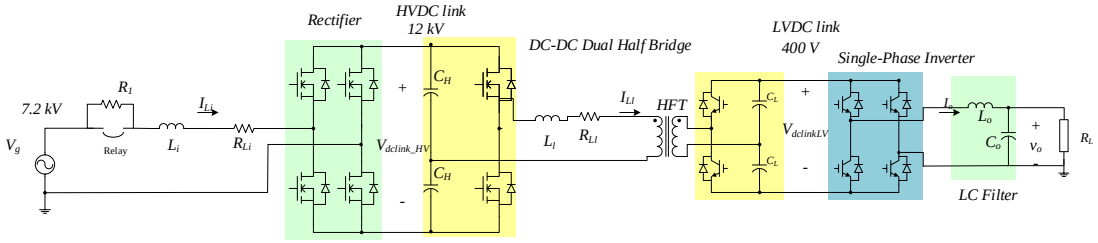


Figure 0.9 Diagram of DHB based three-stage SST

The final implementation of the SST system in RTDS is shown in Figure 0.10. The four blocks at the bottom of the figure is called firing pulse conditioner. They are used to assign the PWM signals received from external devices (the controller board in this paper) to specific switches.

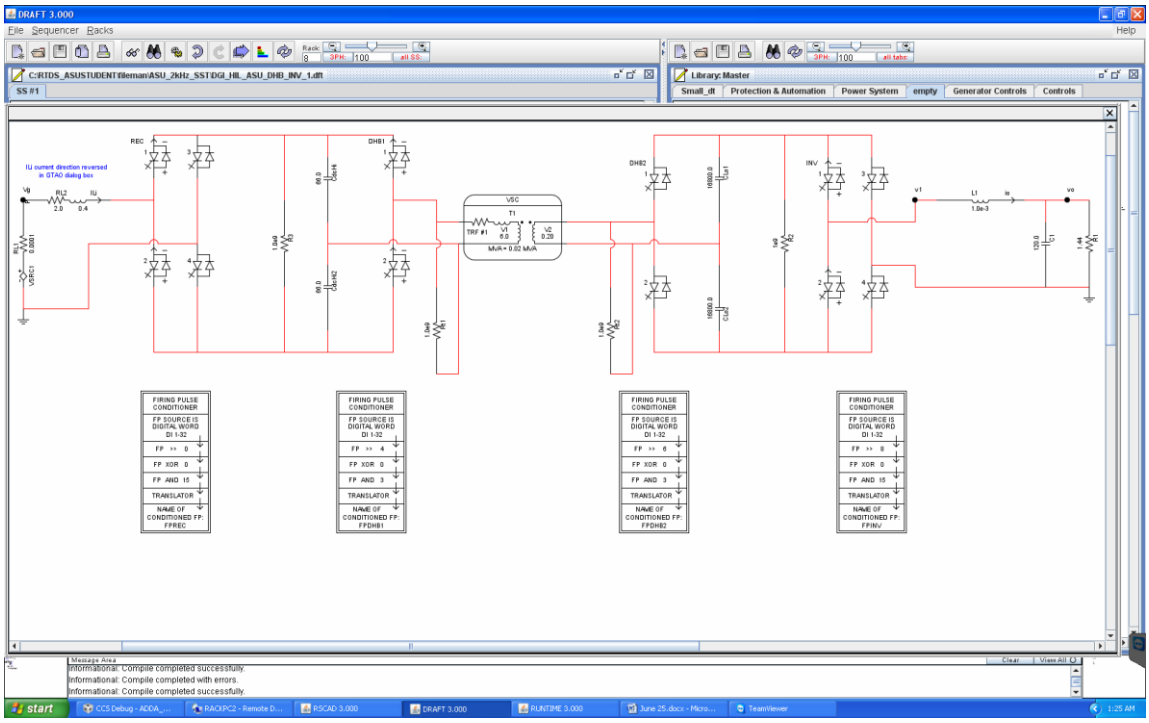
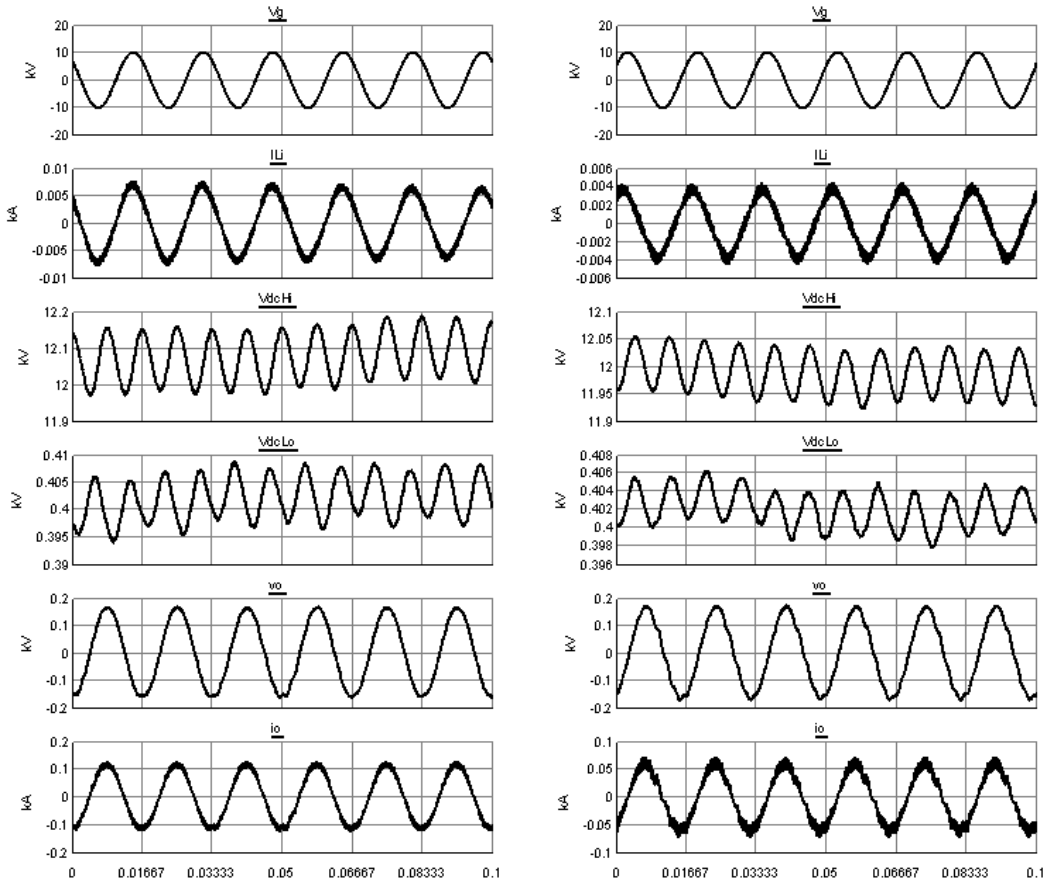


Figure 0.10 Implementation of the SST in RTDS

Different load conditions are simulated and the results are shown in Figure 0.11(a) and (b). The V_g is the grid voltage, i_{Li} is the current through the grid connected inductor, V_{dcHi} is the voltage of the high voltage dc link, V_{dcLo} is the voltage of the low voltage dc link, and the v_o and i_o are output voltage and current of the inverter respectively. The switching frequency is 2 kHz. For Figure 0.11(a) the load is set to be 10 kW while for Figure 0.11 (b) it is 5 kW. It is clear that the basic functionalities described in Chapter 2 are well fulfilled: the inverter generates the desired output voltage, the low voltage dc link is well regulated to be 400 V through the DHB, and the high voltage dc link is maintained to be 12 kV. The independent active power and reactive power control is also realized but not shown here.



(a) 10 kW load (b) 5 kW load

Figure 0.11 Simulation results in RTDS with 10 kW load and 5 kW load

The implementation with the energy device interface is shown in Figure 0.12. Because there is not any energy storage device model in RTDS, a constant dc voltage source is used instead. One special note about the implementation is that special attentions have to be paid when apply any grounds. In RTDS, grounds have to be applied some time in order to make the simulation cases work. In this situation, a large resistance is recommended.

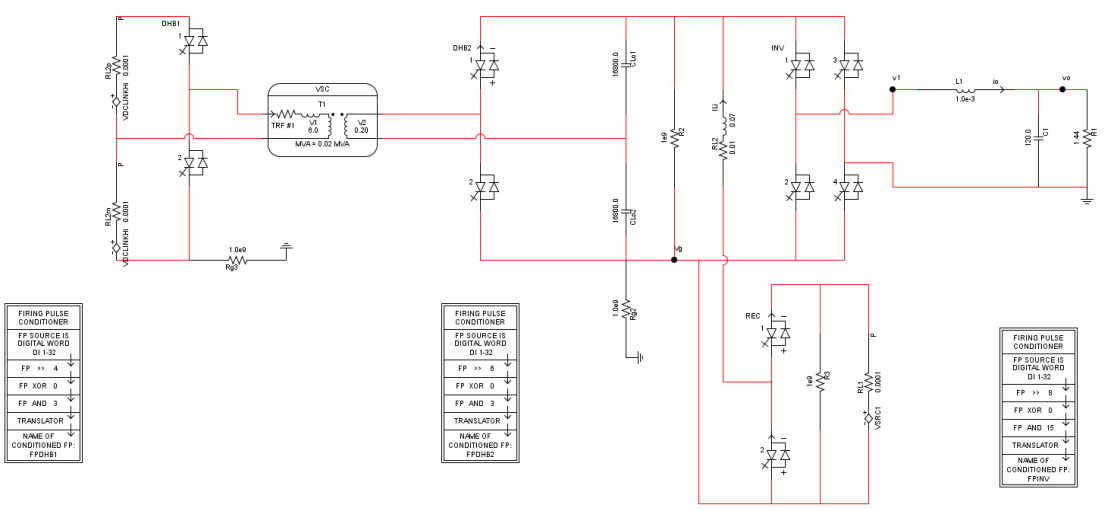


Figure 0.12 Implementation of the energy storage interface in RTDS

The simulation results for the energy storage interface are shown in Figure 0.13(a). Figure 0.13(b) shows the plot being zoomed at 0.07 second. In Figure 0.13(a), the DES is injecting 40 kW active power to the SST while the load is only 10 kW. The extra power is fed to the grid as proved by the plot of I_{dclink}. Even the large spikes exist when turning off, the negative cycle by cycle average DC current shows the power is fed into the high voltage DC link. This validates the function of reverse power flow of the DHB from low voltage side to the high voltage side.

1.16.2 Discussion

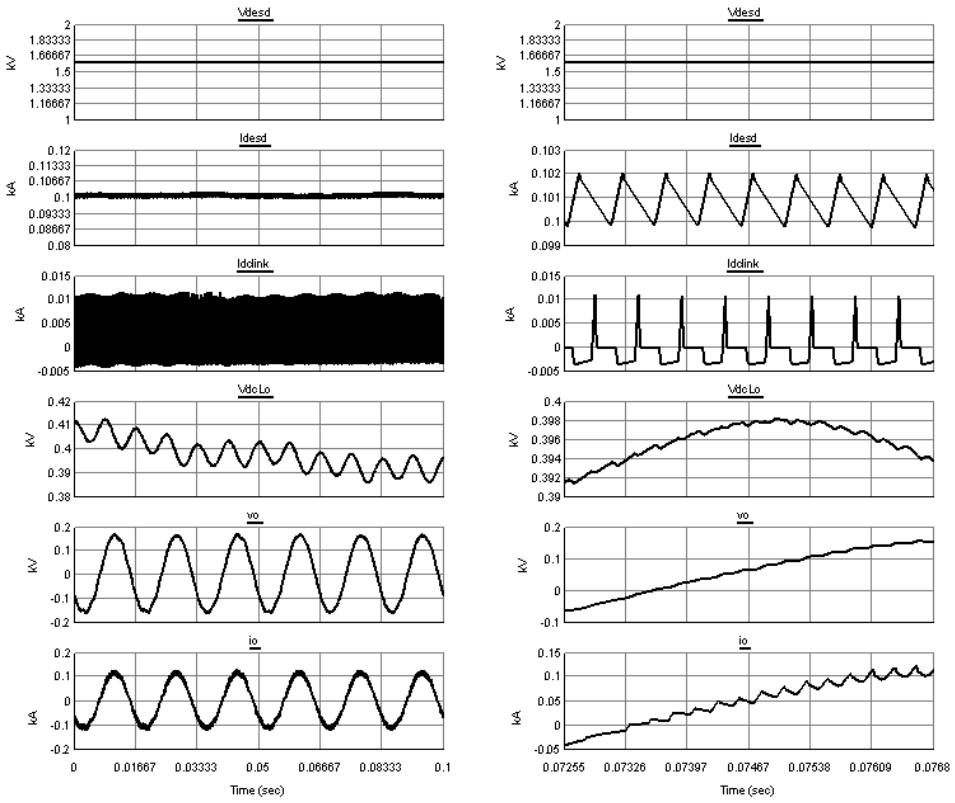
Though the basic functionalities are realized, some limitations are noticed through the simulations.

First, judging from the grid voltage and current, for both the cases of 10 kW load and 5 kW load, the artificial switching losses, caused by the specific implementation of the small time step model, is high.

Second, because of the high frequency transformer, the DHB is hard to regulate.

Third, it is noticed that the stabilities of each stage of the SST system are tightly related.

Without proof the authors suspect that the root cause for this behavior lies with the switch model deficiency in RTDS compared to many of the mathematical simulation platforms such as MATLAB, PLECS or PSCAD. It is seen from Table 0.2, the equivalent on-state inductance of the rectifier switches is about 90 mH, and the one for the high voltage side of the DHB is about 20 mH, which is much larger than the leakage inductance of the high-frequency transformer. Also, due to the modeling method of the switch, the input and output impedance of each stage has been greatly changed, which brings in some unexpected factors for the stability of the whole systems. So when a complex power electronics circuit is implemented in RTDS, the researchers have to pay close attention to the robustness of the system.



(a) Storage supply power to the SST (b) Zoomed view of the plots

Figure 0.13 Simulation results of the energy interface in RTDS

1.17 Summary

This Chapter described the implementation of the CHIL testbed of SST in RTDS. The parameter setup of the model has been discussed in detail. The functionalities of the SST have been realized on the platform. Some limitations are noticed and discussed through the simulation on RTDS.

CONCLUSIONS AND FUTURE WORK

1.18 Conclusions:

In this report, the energy based control strategy has been analyzed and applied for the three-stage SST. A simplified average model of three-stage SST that is suitable for RTDS simulation has been proposed. Simulation and comparisons have been conducted in MATLAB and PLECS to verify the accuracy of the proposed model. A special phase shift modulation has been proposed to enable the implementation of switching model of the SST in PSCAD.

This report has described the implementation of the CHIL test environment of the SST in RTDS. The parameter setup of the model has been discussed in detail. The functionalities of the SST have been realized on the platform. Some limitations are noticed and discussed through the simulation on RTDS.

1.19 Future Work:

Based on the studied in this report, the following recommendations are considered for the future work:

- Implement the simplified average model on the RTDS platform.
- Refine the performance of the CHIL simulation in RTDS, try to reduce the artificial switching losses.
- Use an additional controller board to control the DES in RTDS, and integrate it

with the existing CHIL testbed for the SST.

- Combine the CHIL and average model, build up the five node demonstration system.

REFERENCES

[1]. G. T. Heydt, “Future renewable electrical energy delivery and management systems: Energy reliability assessment of FREEDM systems,” PES General Meeting, 2010 IEEE, pp. 1-4, July 2010

[2]. A. Q. Huang, M. L. Crow, G. T. Heydt, J. P. Zheng, S. J. Dale, “The Future Renewable Electric Energy Delivery and Management (FREEDM) System: The Energy Internet,” Proceedings of the IEEE , vol. 99, issue 1, pp. 133-148, Jan. 2011

[3]. A.Q. Huang, “FREEDM system - a vision for the future grid,” PES General Meeting, 2010 IEEE, pp. 1-4, July 2010

[4]. FREEDM website: http://www.freedm.ncsu.edu/index.php?s=1&p=8

[5]. Ronan, E.R.; Sudhoff, S.D.; Glover, S.F.; Galloway, D.L., “A power electronic-based distribution transformer,” Power Delivery, IEEE Transactions on , vol.17, no.2, pp.537-543, Apr 2002.

[6]. S. Falcones, Xiaolin Mao, R. Ayyanar, “Topology comparison for Solid State Transformer implementation,” Power and Energy Society General Meeting, 2010 IEEE , pp.1-8, July 2010

[7]. Harish K. Krishnamurthy, “Control Strategies for a Universal Fully Modular Power Conversion Architecture,” Ph.D. Dissertation, Arizona State University, 2008

[8]. Heinemann, L.; Mauthe, G., "The universal power electronics based distribution transformer, an unified approach," Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual, vol.2, no., pp.504-509 vol.2, 2001.

[9]. Tiefu Zhao; Liyu Yang; Jun Wang; A.Q. Huang, "270 kVA Solid State Transformer Based on 10 kV SiC Power Devices," Electric Ship Technologies Symposium, 2007. ESTS '07. IEEE, vol., no., pp.145-149, 21-23 May 2007.

[10]. J. L. Brooks, “Solid state transformer concept development,” in Naval Material Command. Port Hueneme, CA: Civil Eng. Lab., Naval Construction Battalion Center, 1980.

[11]. Jih-Sheng Lai; Maitra, A.; Mansoor, A.; Goodman, F., "Multilevel intelligent universal transformer for medium voltage applications," Industry Applications Confer-

ence, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005, vol.3, no., pp. 1893-1899 Vol. 3, 2-6 Oct. 2005.

[12]. Iman-Eini, H.; Farhangi, S.; Schanen, J.-L.; Aime, J., "Design of Power Electronic Transformer based on Cascaded H-bridge Multilevel Converter," Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on, vol., no., pp.877-882, 4-7 June 2007.

[13]. D.Wang, C.Mao, J.Lu, S.Fan, F.Peng, "Theory and application of distribution electronic power transformer" Elsevier, Electric Power Systems Research, 2006.

[14]. Iman-Eini, H.; Farhangi, S., "Analysis and Design of Power Electronic Transformer for Medium Voltage Levels," Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE, vol., no., pp.1-5, 18-22 June 2006.

[15]. Kang, M.; Enjeti, P.N.; Pitel, I.J., "Analysis and design of electronic transformers for electric power distribution system," Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE , vol.2, no., pp.1689-1694 vol.2, 5-9 Oct 1997.

[16]. Cha, H.J.; Enjeti, P.N., "A three-phase AC/AC high-frequency link matrix converter for VSCF applications," Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual, vol.4, no., pp. 1971-1976 vol.4, 15-19 June 2003.

[17]. Jin Aijuan; Li Hangtian; Li Shaolong, "A three-phase four-wire high frequency AC link matrix converter for power electronic transformer," Electrical Machines and Systems, 2005. ICEMS 2005. Proceedings of the Eighth International Conference on, vol.2, no., pp.1295-1300 Vol. 2, 29-29 Sept. 2005.

[18]. Kheraluwala, M.N.; Gascoigne, R.W.; Divan, D.M.; Baumann, E.D., "Performance characterization of a high-power dual active bridge DC-to-DC converter," Industry Applications, IEEE Transactions on, vol.28, no.6, pp.1294-1301, Nov/Dec 1992.

[19]. The RTDS website: http://www.rtds.com/index/index.html

[20]. RTDS User Manual

[21]. N. Mohan, First Course on Power Electronics and Drives, Year 2003 Edition.

[22]. R.W. Erickson and D. Maksimovic, Fundamental of Power Electronics, 2nd edition, 2001, Kluwer Academic Pulbishers, NJ, USA

[23]. Joehong Kim, Hong-Seok Song, Kwanghee Nam, “Asymmetric duty control of a Dual-Half-Bridge DC/DC converter for single-phase distributed generators,” IEEE Trans. On Power Electronics, vol. 26, no. 3, pp. 973-982, March 2011

[24]. M. T. Haque, “Single-phase PQ theory,” Power Electronics Specialists Conference, 2002, vol. 4, pp. 1815-1820, 2002

[25]. Xiaolin Mao, S. Falcones, R. Ayyanar, “Energy-based control design for a solid state transformer,” Power and Energy Society General Meeting, 2010 IEEE, pp. 1-7, July 2010

[26]. L. R. limongi, R. Bojoi, G. Griva, A. Tenconi, “New control scheme for single-phase active power filters,” Power Electronics Specialists Conference, 2008, vol. 4, pp. 2894-2900, 15-19 June 2008

[27]. R. Teodorescu, F. Blaabjerg, U. Borup, and M. Liserre, “A New Control Structure for Grid-Connected LCL PV Inverters with Zero Steady-State Error and Selective Harmonic Compensation,” Proc. IEEE APEC’04, vol. 1, pp. 580-586, 2004

[28]. T. Maguire and J. Giesbrecht, “Small time-step (<2 usec) VSC model for the Real Time Digital Simulator,” presented at the International Conference on Power System Transients (IPST’05) in Montreal, Canada on June 19-23, 2005, (paper no. IPST05-168)