Biosensors and CMOS Interface Circuits

by

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ABSTRACT

Analysing and measuring of biological or biochemical processes are of utmost importance for medical, biological and biotechnological applications. Point of care diagnostic system, composing of biosensors, have promising applications for providing cheap, accurate and portable diagnosis. Owing to these expanding medical applications and advances made by semiconductor industry biosensors have seen a tremendous growth in the past few decades. Also emergence of microfluidics and non-invasive biosensing applications are other marker propellers.

Analyzing biological signals using transducers is difficult due to the challenges in interfacing an electronic system to the biological environment. Detection limit, detection time, dynamic range, specificity to the analyte, sensitivity and reliability of these devices are some of the challenges in developing and integrating these devices. Significant amount of research in the field of biosensors has been focused on improving the design, fabrication process and their integration with microfluidics to address these challenges.

This work presents new techniques, design and systems to improve the interface between the electronic system and the biological environment. This dissertation uses CMOS circuit design to improve the reliability of these devices. Also this work addresses the challenges in designing the electronic system used for processing the output of the transducer, which converts biological signal into electronic signal.

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Chapter 1

INTRODUCTION

Biosensor is a device that uses specific biochemical reactions mediated by isolated enzymes, immunosystems, tissues, organelles or whole cells to detect chemical compounds usually by electrical, thermal or optical signals [1]. They are composed of a receptor and a transducer which converts the chemical or physical changes into a corresponding electrical signal. Since their introduction as an enzyme electrode by Clark in 1962 [2] there has been a tremendous advancement in the biosensing technology. Several biosensing devices and concepts such as cyclic voltammetry, impedance spectroscopy and field effect transistor based detection methods have been developed in the past few decades.

Figure 1.1 shows the basic working of a biosensor system [3]. It involves detection of the analyte by the transducer and converting the biological signal into an electrical signal. The electronics system is mainly composed of the readout and signal processing circuits. This work presents non-specific, receptor free sensors for both cellular and molecular sensing. This allows us to use a single device to detect multiple targes/analytes as we will demonstrate herein

Field Effect Transistor (FET) based detection methods provide an attractive means to analyze the content of a biological sample because of its direct conversion to electrical signals. In addition, FETs could be easily integrated on a silicon wafer. The conductance of the field effect transistor is modulated by the potential on the gate of the device. They are preferred in applications where it is necessary to measure weak signals, since they have a high signal to noise ratio, and high output impedance. One of the most popular FET based biosensor is an Ion Sensitive Field Effect Transistor (ISFET), which senses pH of an analyte. Chapter 2 discusses ISFETs in detail. Threshold voltage drift in these devices is known to cause measurement errors, and hence a technique to reduce the drift

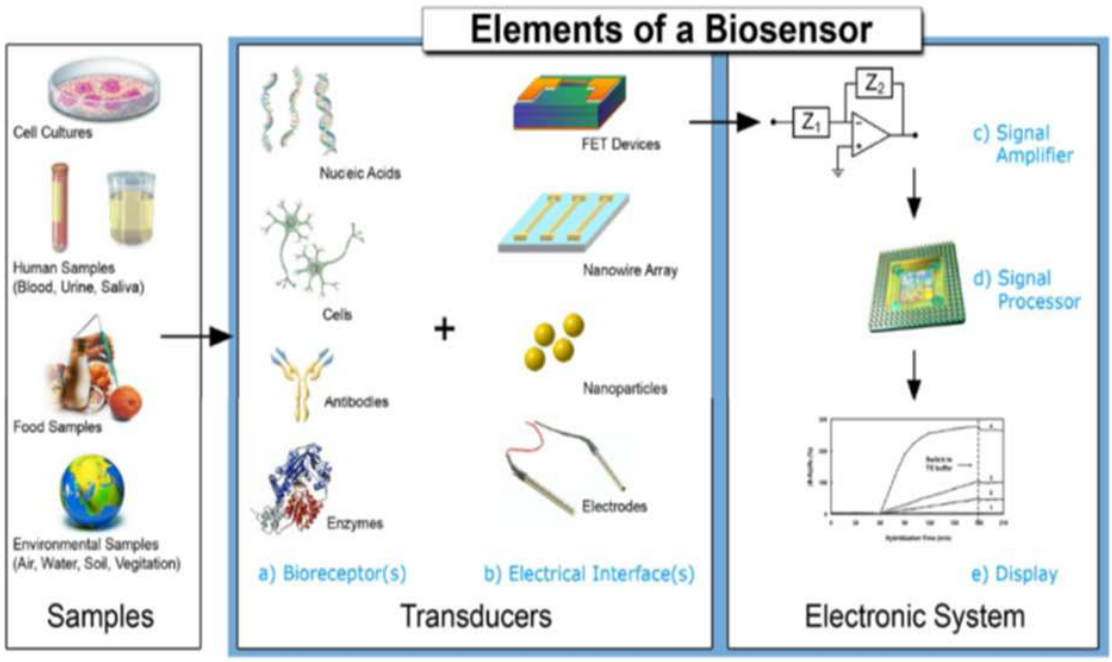


Figure 1.1: The basic working of a biosensor with samples, tranducers, and signal processing is shown. A biosensing system composes of a transducer which detects the sample/analyte and converts it into an electrical signal for signal processing by the electronic system [3]

is presented in Section 2.2. Process variations and gradients in oxide thicknesses result in mismatch in these devices. Section 2.3 presents a way to programme these devices to reduce the mismatch. ISFET on a flexible substrate is presented in section 2.4 which increases the area of these sensors and allows us to integrate the reference electrode.

Due to the small size of ISFETs they can be used to monitor the pH of cell culture media in microsystems, as shown in chapter 3. These provides us with a very powerful and alternative way to perform cell viability and effects therapeutic drugs like staurosporine have on the tumor cells, presented in Section 3.2 of Chapter 3.

ISFET's success as a biosensor is partly due to the fact that they can be integrated in a CMOS process with relative ease, apart from the challenges in packaging the CMOS die for microfluidics. Hence we can take advantage of the advances made by semiconductor

industry. This allows us to design low power, low noise, precision analog and highly dense digital circuits for processing the electric signals generated by the biosensors. Chapter 4 discusses the circuit used to mitigate drift in the threshold voltage of ISFETs. Chapter 5 and Chapter 6 present a readout circuit used for processing signals from the biosensor. Chapter 5 discusses techniques used to design low noise amplifiers. Chapter 6 shows the design and measurement of a dual slope analog to digital converter.

Further in Chapter 2 a low power CMOS amplifier is designed to record neural signals. The amplifier used should have low noise in the bandwidth of interest since the neural signal, local field potential and neural spikes, have very small magnitude. The neural amplifier can be used to record the neural signal while they are being stimulated by flexible OLEDs provided by the ASU Flexible Display Center.

Chapter 2

ISFET

2.1 Background

Ion Sensitive Field Effect Transistors (ISFETs) have been used extensively since they were introduced by Bervgeld in 1970 [4]. They are field effect transistors where the gate contact is replaced by a reference electrode in the electrolyte as shown in the Figure 2.1. Since in an ISFET the metal connection to the reference electrode is defined as a remote gate any interfacial potential, at the gate of the device, is described in terms of threshold voltage (V_t) of the device [5]. Threshold voltage of an ISFET is given by equation 2.1 [5].

$$V_t = E_{ref} - \Psi + \chi^{sol} - \left(\frac{\phi_{Si}}{q}\right) - \left(\frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}}\right) + \phi_f \tag{2.1}$$

Here E_{ref} is the potential of the reference electrode and $\Psi + \chi^{sol}$ is due to the potential at insulator and electrolyte interface. Ψ is a function of pH of the solution, which in turn modulates the threshold of the device.

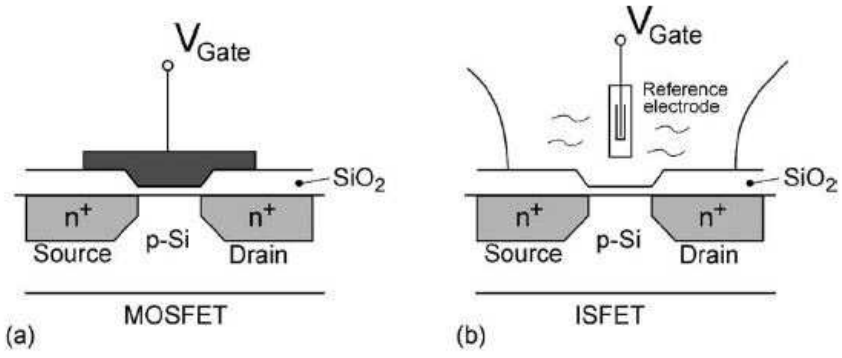


Figure 2.1: Comparison between an ISFET and a reference electrode to a MOSFET [5]. a) A conventional MOSFET with gate electrode. b) An ISFET with floating gate electrode.

The pH sensitivity of an ISFET arises from the interaction of protons with the insulator gate surface sites which changes the surface potential at the gate insulator and electrolyte interface. The pH sensitivity is given by the Nernst equation [6].

$$E = E^{\circ} + \frac{RT}{nF} \ln \frac{a_{ox}}{a_{red}} \tag{2.2}$$

where

E = Measured galvanic potential of the electrode in equilibrium with the solution

E° = Standard potential of the electrode at pH 7

R = Universal gas constant = 8.314 J/mol*K

T = Absolute temperature in Kelvin = 298.15 K

n = charge number of the electrode reaction (number of moles of electrons involved in the reaction)

F = Faraday's constant (96,500 C/mol)

a_{ox} = Chemical activities on the oxidized side of the electrode reaction

a_{red} = Chemical activities on the reduced side of the electrode reaction

In the case of a dilute solution the activity can be the same as the concentration.

$$E = E^{\circ} + 2.303 \frac{RT}{nF} \log \frac{[OX]}{[R]} \tag{2.3}$$

where [OX] is the concentration of the oxidised species and [R] is the concentration of the reduced species. With n = 1 for the valence electrons of hydrogen ions in equation 2.3 at T = 298 K, it transforms into the following equation.

$$E = E^{\circ} + 0.05915 \log \frac{[OX]}{[R]} \tag{2.4}$$

This is similar to Henderson-Hasselbach equation [7] which gives the pH of mixtures of acids and bases given by following equation:

$$pH = pK_a + \log \frac{[A^-]}{[HA]} \tag{2.5}$$

Since pH manifests as a change in threshold voltage, the relation between Ψ (in threshold equation 2.1) and pH [4] is given by equation 2.6

$$\Delta\Psi = -2.303\alpha \frac{RT}{nF} \Delta pH \tag{2.6}$$

where α is given by

$$\alpha = \frac{1}{\frac{2.3KT}{q^2}\frac{C_s}{\beta_s} + 1} \tag{2.7}$$

where C_s is the double layer capacitance and β_s is the surface buffer capacity.

Thus with α equal to 1 a Nernstian response is obtained having a sensitivity of 59.1 mV/pH. But for insulators having $alpha$ smaller than 1 (e.g. SiO_2) a sub-Nernstian response is obtained.

ISFETs have been used extensively to measure pH because of their small size, lower power dissipation, and lower manufacturing cost. However they suffer from drift in threshold voltage which causes error in the measurement of the pH. The drift in threshold voltage has limited the commercial viability of the ISFET. Temperature dependent[8], transport dependent [9], pH dependent[10][11][12], insulating gate dependent [10] and

split between a fast and slow response [13] are some of the factors which have been proven to cause drift in the ISFETs.

2.2 Drift and modeling the ISFET

An ISFET has been fabricated in SensoNor MultiMEMS process. The ISFETs fabricated using the MultiMEMS are p-channel field effect transistors having a width of 5460 μm and length of 6 μm. We measured the current through the channel of the ISFET using Keithley 2636A. Initially the ISFET were characterized using a buffer having a pH of 4, 7 and 10. This allows us to characterize the device and obtain the sensitivity of the device. Figure 2.2 shows the transfer characteristics of the ISFET fabricated in SensoNor Multimems process.

2.2.1 Threshold drift

As discussed earlier ISFETs suffer from drift in the threshold voltage. Drift in threshold can be observed by measuring the source current of the ISFET as shown in the Figure 2.3.

Compensating pH sensors for threshold voltage shift involves calibrating them before every measurement cycle. Several methods have been used to compensate for the drift [14][15][16]. We proposed and demonstrated resetting the drift by cycling the vertical electrical field of the ISFET [17]. Vertical electric field is dependant on the potential of the reference electrode and the substrate potential where as horizontal electric field is due to the potential on drain and source region of the electric field. In the Figure 2.4a, a vertical electric field is cycled to reset the drift in the threshold voltage. Electric field having different duty cycle were tested to obtain minimum off time. It was observed that an off time as small as 30 seconds for an on time of 1000 seconds is enough to reset the drift in the threshold voltage as shown in the Figure 2.4b.

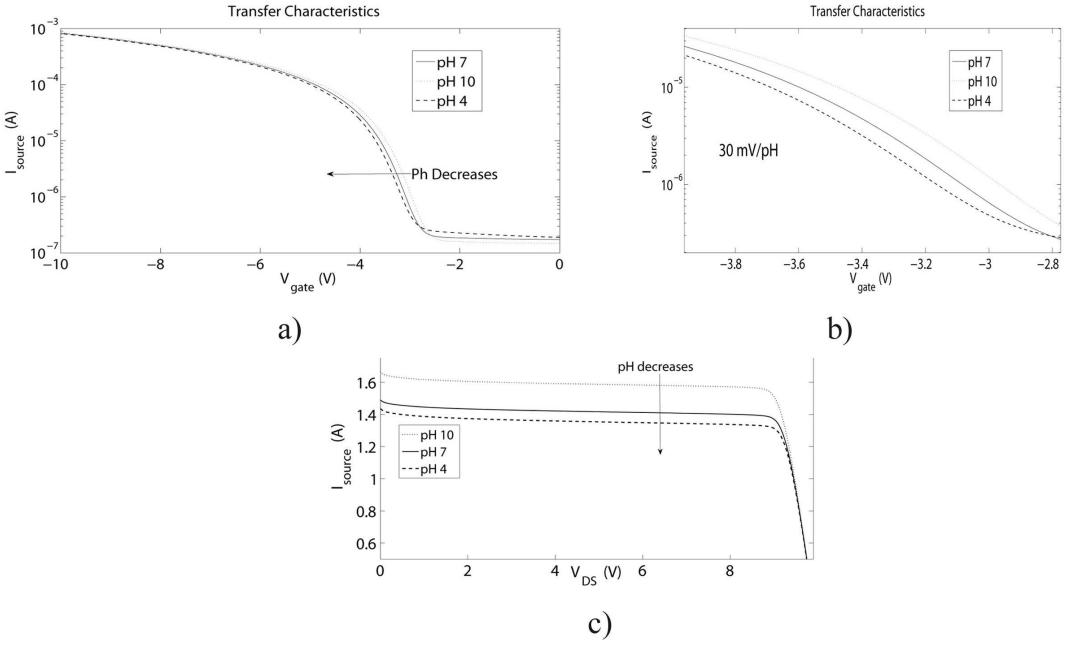


Figure 2.2: a) Transfer characteristics of an ISFET fabricated in SensoNor Multimems process. The transfer characteristics were obtained by using pH buffers having different values to obtain sensitivity of the device to pH. b) The figure shows the change in threshold voltage of the ISFET. A sensitivity of 30 mV/pH was obtained as compared to a nernstian response of 59 mV/pH. c) The figure shows the source current plotted against drain to source potential for different pH solutions.

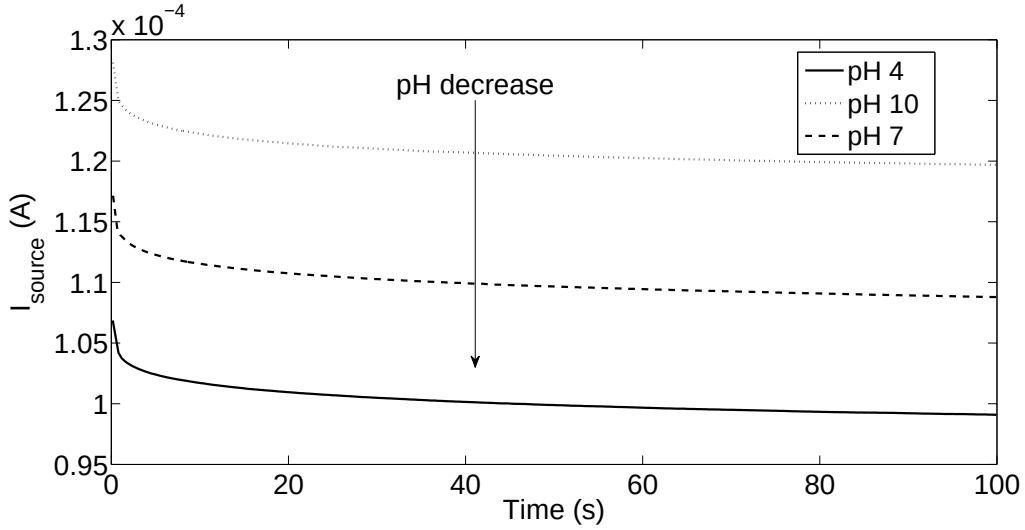
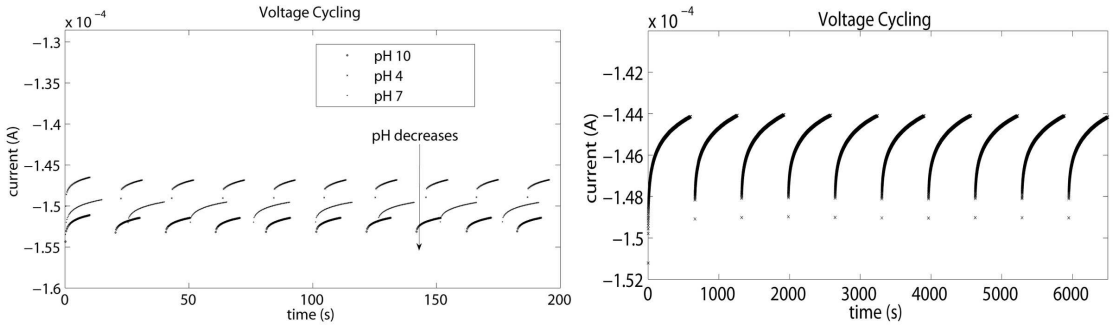


Figure 2.3: Current measured over time using buffers with pH of 4, 7, and 10. The decrease in current is due to the drift in threshold voltage of the device.



a) b)

Figure 2.4: a) The figure shows reset in the drift of the threshold voltage for different pH solutions. Cycling vertical electric field has been shown to reset the drift in the threshold voltage [18]. b) Gate voltage cycling with small off time to show the reset in drift. An off time of 30 seconds was enough to reset the drift in the ISFET. This allows accurate and continuous measurement of pH [17].

2.2.2 TCAD model

To understand the physics of the drift and reset, a model of the ISFET was created using Silvaco TCAD. A physical-based simulation was performed in ATLAS to examine the physical mechanism of ISFET threshold voltage drift. A p-channel FET was modeled using ATHENA process simulator having dimensions of the ISFET fabricated in SensoNor MultiMEMS process. The simulated model was fabricated according to the steps provided in the SensoNor MultiMEMS design guide [19].

TCAD is generally used to model semiconductor devices with electrons and holes as the carrier. Therefore to model an ISFET, which has its gate in the form of a reference electrode dipped inside an electrolyte, using TCAD a user defined material was deposited on top of the insulator layer to emulate the electrolyte. By doing so we are modeling the ions inside the electrolyte by electrons and holes. All user defined materials in ATHENA are considered to be insulators with properties that can be altered to meet the requirements for a simulation. We modified the properties of the user defined material to align with the conditions of an ionic solution as specified by Chung *et al.* [20]. In an ionic solution

the charge distribution (φ) in the ionic double layer is given by the Poisson-Boltzmann equation 2.8

$$\frac{\delta^2\varphi}{\delta x^2} = -\frac{q}{\varepsilon}\left[C_0^{Na^+}\exp\left(\frac{-q\varphi}{kT}\right) - C_0^{Cl^-}\exp\left(\frac{-q\varphi}{kT}\right)\right] \tag{2.8}$$

where $C_0^{Na^+}$ and $C_0^{Cl^-}$ are the concentration of Na^+ and Cl^- in the electrolyte, k is Boltzmann's constant, T is the temperature in Kelvin, ε is the permittivity of the electrolyte, and q is the total charge of the ions in the double layer equal to the charge number of the ion (z) multiplied by the elementary charge (e) ($q = ze$). This equation can be modified to give the Fermi-Dirac distribution of electrons and holes given by the equation 2.9

$$\frac{\delta^2\varphi}{\delta x^2} - \frac{q}{\varepsilon}\left[p_0\frac{1+e^{\frac{E_i-E_v}{kT}}}{1+e^{\frac{E_i-E_v}{kT}}e^{\frac{q\varphi}{kT}}} - n_0\frac{1+e^{\frac{E_c-E_i}{kT}}}{1+e^{\frac{E_c-E_i}{kT}}e^{\frac{q\varphi}{kT}}}\right] \tag{2.9}$$

so that an intrinsic semiconductor can be used to model the electrolyte. In equation (2.9), n_0 and p_0 are electron and hole concentration, E_i is energy of fermi level in an intrinsic semiconductor, E_c is the energy of the conduction band, and E_v is the energy of the valence band. To satisfy the Fermi-Dirac conditions, half the band gap (E_g) of the intrinsic semiconductor minus the charge distribution multiplied by an elementar should satisfy the equation $\frac{E_g}{2} - q\varphi \gg kT$.

$$\frac{E_g}{2} - q\varphi \gg kT \tag{2.10}$$

The density of states for the valence band and conduction band (N_c and N_v respectively), were specified according to the molar concentration of the ionic solution. A bandgap of $1.5\,eV$ was set for the electrolyte to model it as a modified semiconductor. The bandgap value was determined by extracting experimental parameters. The model required a Debye length larger than the size of the simulated ions in solution. The Debye length

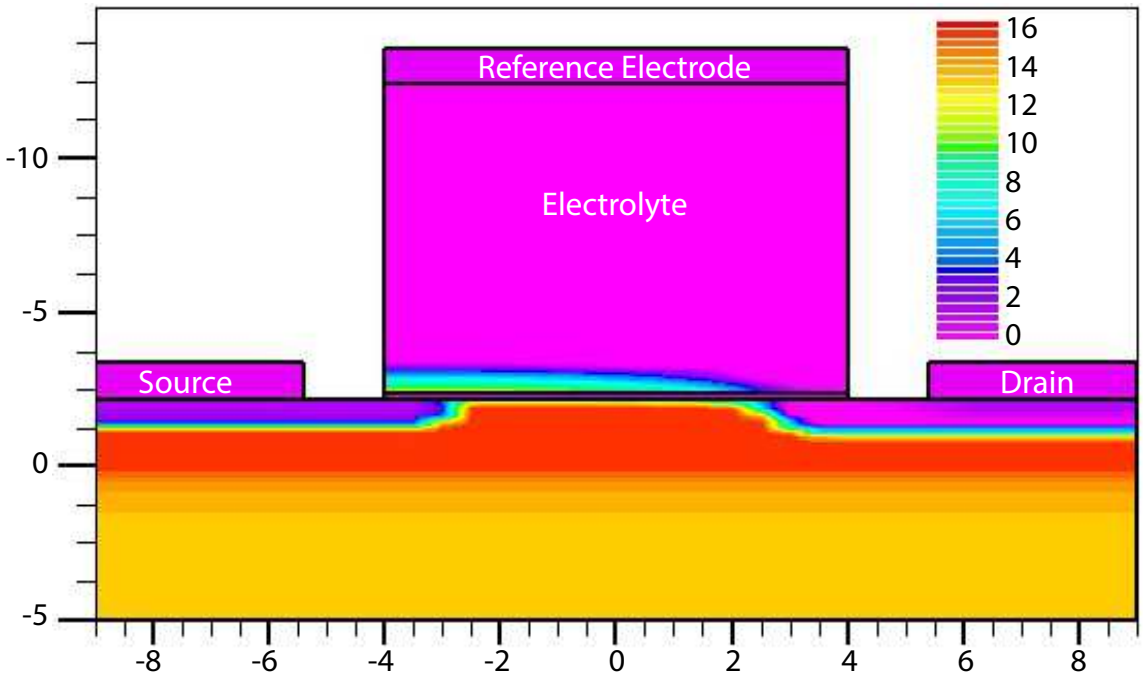


Figure 2.5: Cross section of the structure of the ISFET as modeled in Silvaco TCAD. The electron concentration during ISFET operation is indicated by coloring (log value of electrons per cm^3). Device dimensions indicated on the axes are in microns. [17]

decreases as the ionic concentration increases; therefore, the maximum concentration we could simulate was approximately $500\,mM$.

The relative permittivity of the defined material was set to 80 to match the properties of water. The mobility of electron and holes was set to the values for Cl^- and Na^+ ions in water ($6.88 \times 10^{-4}\,cm^2V^{-1}s^{-1}$ and $4.98 \times 10^{-4}\,cm^2V^{-1}s^{-1}$ respectively [21]). Properties for electron affinity ($3.9\,eV$) and the recombination lifetime of electrons ($1 \times 10^{-3}\,s^{-1}$) and holes ($1 \times 10^{-3}\,s^{-1}$) were set by curve fitting the simulated and experimentally obtained curves. Gold was used as a reference electrode to match the experimental setup. The final structure of the modeled ISFET is shown in Figure 2.5.

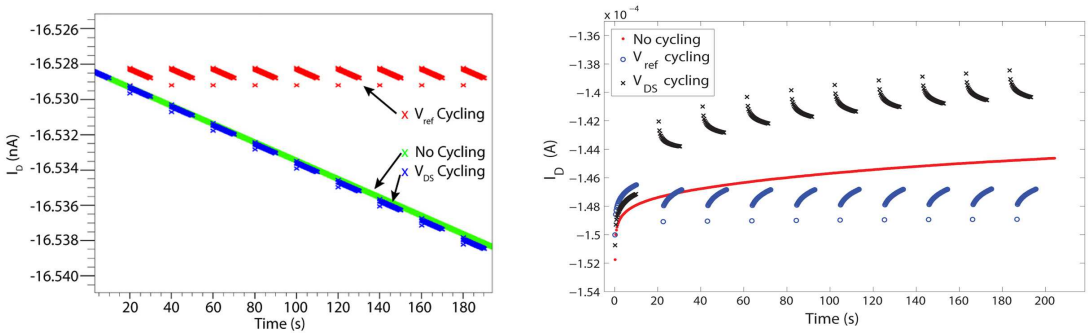
The Shockley-Read-Hall(SRH) and Lombard mobility models were used to simulate the drift in threshold voltage and the reset characteristics. These are standard models used for MOSFET simulations. SRH was used to model the generation and recombina-

tion inside the semiconductor. The Lombard mobility model considers mobility due to the transverse electric field. The curve fitting was done using I_{DS} vs V_{ref} values obtained from the static DC solution. The gate voltage was ramped from $0V$ to $-20V$ while keeping the drain at $-2V$ to obtain the I_{DS} vs V_{ref} curves. During simulations, the source and the substrate were kept at $0V$ while the drain was held at $-2V$. The reference voltage was kept at $-10V$ while performing transient simulations. All of the voltages used in the model reflect the experimental conditions. Simulations were performed for a model with a unit width so the current obtained was per μm of device width. The width of our fabricated ISFET was 5460 μm; the current values obtained during simulations are multiplied by the width for a comparision to our experimental results.

Figure 2.6a shows results from the ISFET model and compares it with experimentally obtained results shown in the figure 2.6. Cycling of vertical electric field effectively resets the drift in the ISFET whereas cycling horizontal electric field has no effect on the threshold drift. We simulated a unit ISFET width so the currents were much smaller than experimental values. The distance between the reference electrode and the gate oxide was also scaled. Since the model created in the TCAD had a scaled dimensions the current value is different from the measured results shown in the figure 2.4.

2.3 Device Mismatch and calibration

The pH sensors suffer from drift as shown previously in the Figure 2.3, but that can be mitigated by vertical field cycling as shown in the Figure 2.4. However two identical sensors suffer from mismatch, and thus they require external calibration. Mismatch is the process that causes time-independent random variations in physical quantities of identically designed devices [22]. In terms of a pH sensors mismatch can cause variation in current output while measuring the same pH value as shown in the Figure 2.7.



a) b)

Figure 2.6: a)Results from the model created in Silvaco TCAD showing the drift in drain current (green), the effect of V_{ref} cycling (red), and the effect of V_{DS} cycling (blue). The model produced a scaled current of $90\,\mu A$, which is very close to the experimental values of $146\,\mu A$. b)Experimental results showing drift in drain current, the effect of V_{ref} cycling, and the effect of V_{DS} cycling.[17]

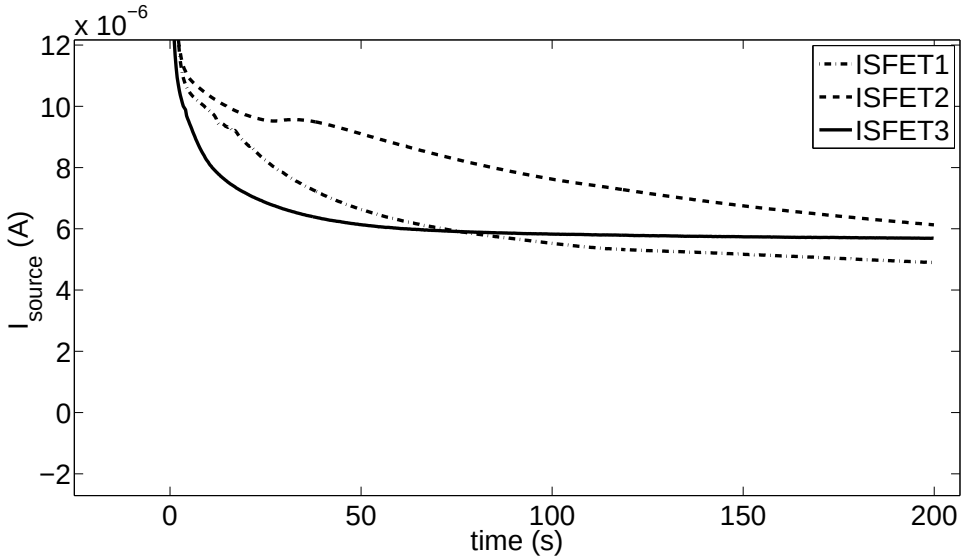


Figure 2.7: ISFET current measured with a buffer having pH 10. All the devices used for the measurement have the same width and length. The measurements are taken from devices on three different chips. In addition to the mismatch, caused due to process variation, there is a time dependent drift in the threshold voltage.

There are various techniques which are used to reduce or remove the mismatch in the devices. Component mismatch can be reduced by using larger devices, common centroid and symmetrical layout. From a design perspective mismatch in OPAMPs can be reduced by chopping, correlated double sampling and auto zeroing as will be discussed in the Chapter 5. Another unique way of reducing the mismatch is by using floating gate transistor as a programmable device [23].

2.3.1 Floating gate ISFET

Floating-gate structures have been widely used to program the threshold voltage of the field effect transistors. Their use as a non-volatile memory was first shown in 1967 by kahng and Sze [24]. But more recently they have been used as an analog memory [25],a floating gate fourier processor [26], to perform offset cancelation in amplifiers [27] among others. Programming of these devices have been demonstrated with an accuracy of 0.2% over three decades [28].

A cross-section and a circuit schematic of a floating gate is shown in the Figure 2.8. The floating node is surrounded by SiO_2 and does not have a direct DC path to ground. The charge on the gate is stored on the floating node and hence providing long term memory [29]. A configurable ISFET was designed having a floating node as shown in the Figure 2.9. Figure 2.10 shows the response of the floating gate ISFET to buffers having different pH values, which demonstrates the use of these devices as pH sensors.

2.3.2 Programming the floating gate

Floating gate transistors are programmed using hot electron injection, Fowler-Nordheim tunneling and ultraviolet (UV) light [30][31]. For programming the floating gate ISFET hot electron injection is used to decrease the threshold voltage of the device and Fowler-Nordheim tunneling is used to increase the threshold voltage.

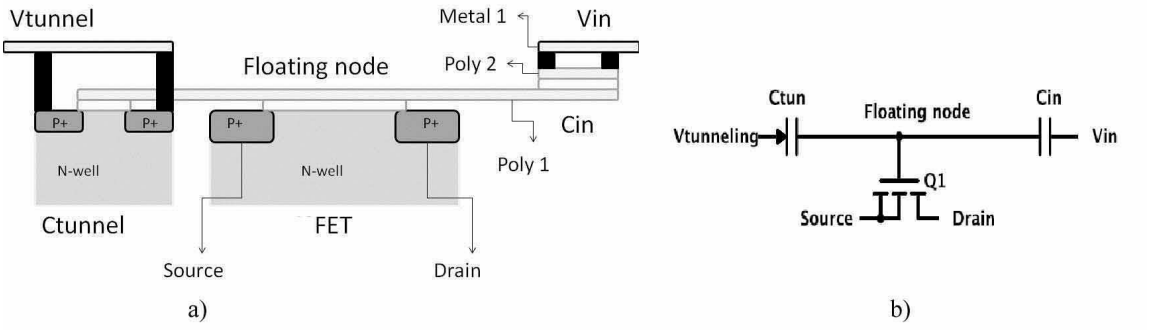


Figure 2.8: a) Cross-section of the floating gate field effect transistor showing the C_{tun} and C_{in} .b) Circuit schematic of a floating gate p-channel FET with its input signal capacitively coupled through C_{in}. The tunneling junction is capacitively coupled through C_{tun}.

Hot electron injection occurs in a field effect transistor when there is a high electric field present across the channel. When drain to source electric field is high the hot-hole impact ionization forms holes and electron pairs near the drain end of the channel. These electrons while travelling through the channel gain kinetic energy and when their energy exceeds that of silicon - silicon dioxide barrier they get injected into the oxide and are transported into floating gate [29] as shown in the Figure 2.11. The efficiency of a floating gate injection is not constant and is highest for subthreshold operation [29], thus the floating gate ISFET is operated in sub-threshold regime while performing injection as can be seen by the biasing condition in the Figure 2.11. The subthreshold current I_s is given by the following equation:

$$I_s = I_{s0} e^{\left(\frac{\Delta V_s - \kappa \Delta V_{fg}}{U_T}\right)} \tag{2.11}$$

where I_s is the subthreshold channel current of FET in saturation, I_{s0} is the bias current for ΔV_{fg} change in floating gate voltage, κ is the fractional change of surface potential

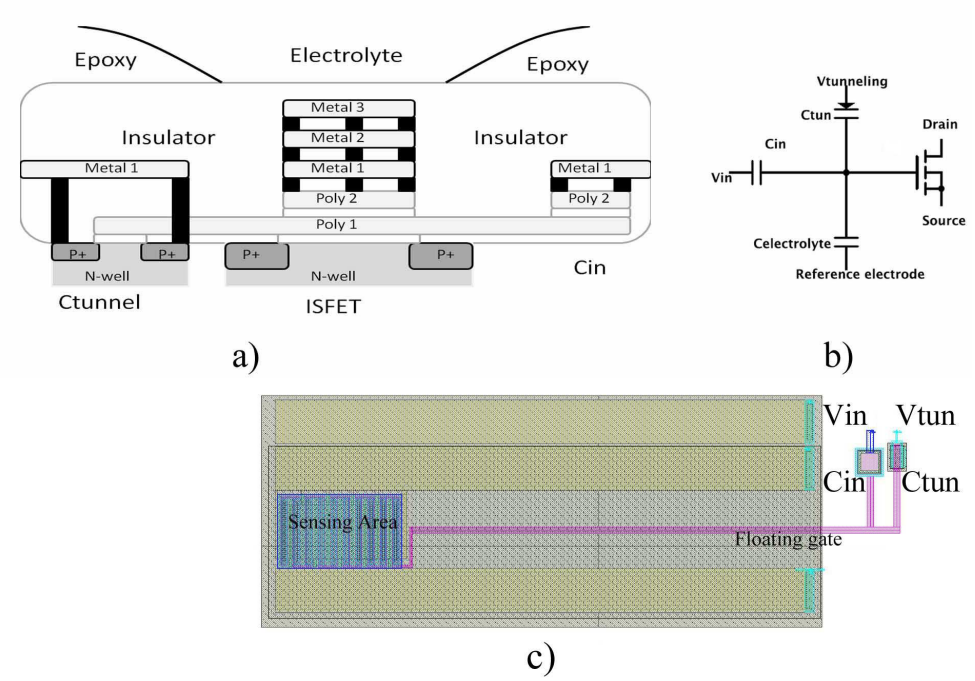


Figure 2.9: a) Cross-section of the floating gate ISFET. The floating gate device is a p-channel ISFET with the gate connected to the N-well capacitor and a poly-poly capacitor. The metal stack is there to reduce the distance between the electrolyte and the gate. b) Circuit schematic of a floating gate p-channel ISFET with its input signal capacitively coupled through C_{in}. The tunneling junction is capacitively coupled through C_{tun}. Ions inside the electrolyte form an ionic double layer which is shown in the schematic by $C_{electrolyte}$. c) Layout of the floating gate ISFET. The input junction V_{in} is coupled through a poly-poly capacitor and the tunneling junction V_{tun} is coupled through a MOS capacitor.

of p-channel ISFET due to variation in potential at the floating node, U_T is the thermal voltage.

Fowler-Nordheim tunneling is defined as a process of tunneling of electron through silicon - silicon dioxide barrier. The tunneling junction is a metal oxide capacitor (C_{tun}) in the Figure 2.9. In case of tunneling, the difference in voltage between the tunneling junction (V_{tun}) and the floating gate V_{fg} reduces the effective width of the barrier which allows some of the electron to move through the oxide. Tunneling removes charges from the floating gate and effectively increases the threshold voltage of the device. A MOS capacitor is used for the purpose of tunneling instead of a poly-poly capacitor because

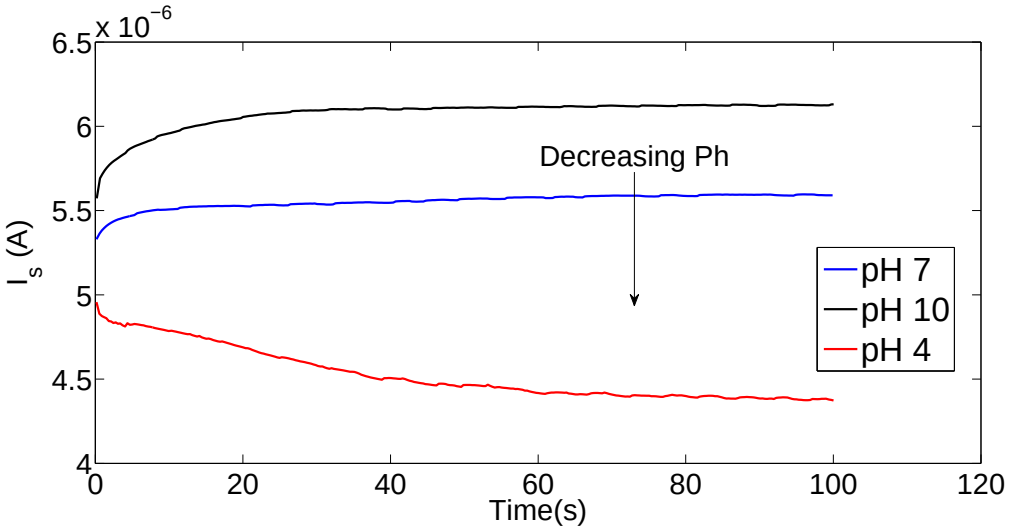


Figure 2.10: The figure shows the sensitivity of the ISFET to change in pH. Floating gate ISFET channel current is plotted against time. The plot also shows the drift behaviour of the floating gate ISFET. Biasing condition for each plot were as follows V_{tun} = V_{source} = V_{in} = 4.2 volts and V_{drain} = $V_{electrode}$ =2 volts. Ag/AgCl is used as a reference electrode.

of substantially better quality of oxide, which reduce the number of trap sites[29]. The tunneling current is given by the classical model of electron tunneling in silicon - silicon dioxide system [32] which is given by the following equation:

$$I_{tun} = I_0 e^{\left(\frac{\varepsilon_0}{\varepsilon_{ox}}\right)} = I_0 e^{\left(\frac{t_{ox}\varepsilon_0}{V_{tun}-V_{fg}}\right)} \tag{2.12}$$

where ε_{ox} is the electric field in the oxide, V_{tun} is the tunneling voltage, V_{fg} is the potential on the floating node, ε_0 is a device parameter which is dependant on the process.

In general performing tunneling and injection can be used to program the threshold voltage of the device as shown in the Figure 2.12. The Figure 2.12 demonstrates programming of the floating gate ISFET. In this situation, a source to drain voltage of 5 volts was applied for less than one second using Keithely 2636A source and measurement unit. Also the tunneling voltage V_{tun} is held at the same voltage as the source where V_{in} is held at voltage such that during the injection the device is below threshold voltage, where the

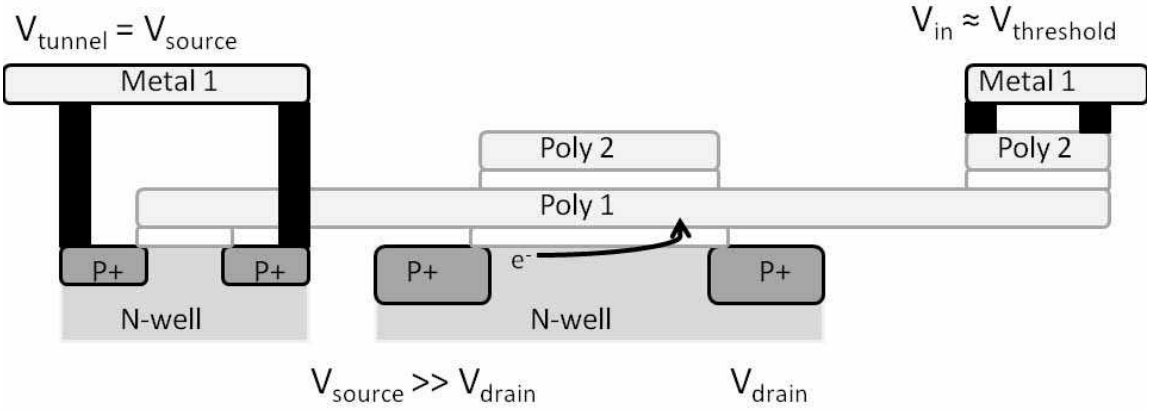


Figure 2.11: Cross-section of the floating gate ISFET showing the electron injection with the biasing condition. The source voltage (V_{source}) is 5 volts for 0.5 μm but is varied as discussed in the figure 2.14 to achieve different injection rate.

efficiency of injection is the highest. During tunneling the V_{tun} is held at 12 volts for less then a second to remove the charges from the floating node. MATLAB is used to control the Keithely and due to the finite delay between the software and the hardware accurate programming cannot be performed.

However the programming completed in Figure 2.12 does not allow us to reduce the mismatch between the pH sensors. To accurately program these devices a precise control on the number of charges getting injected into the the floating node is required. This can be done using a varying pulse width [33] or by keeping the pulse width constant

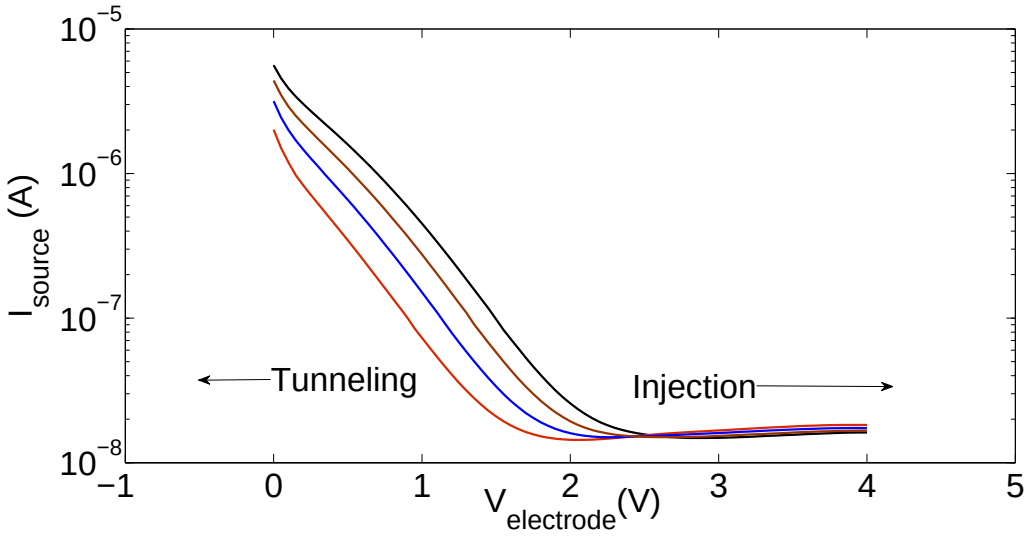


Figure 2.12: Channel current plotted against voltage on the reference electrode. Electron injection decreases the threshold voltage and tunneling increases the effective threshold of the device.

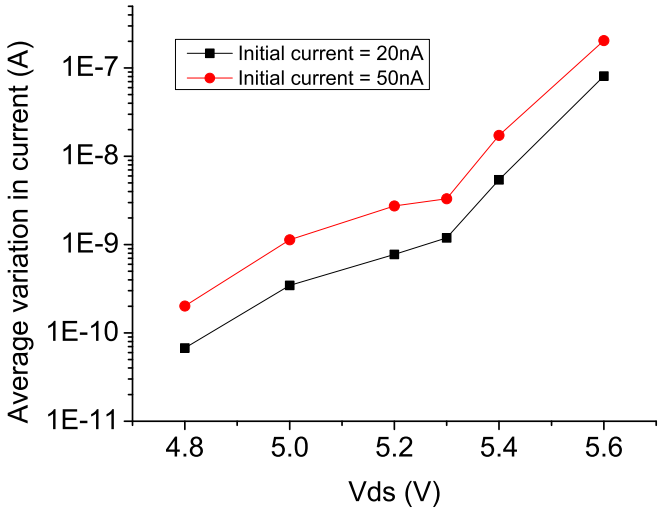


Figure 2.13: The difference is averaged over ten data points taken using the same drain to source voltage values as shown in the figure 2.14. The plot shows the variation of current for different drain to source voltage for an initial current of 50 nA and 20 nA.

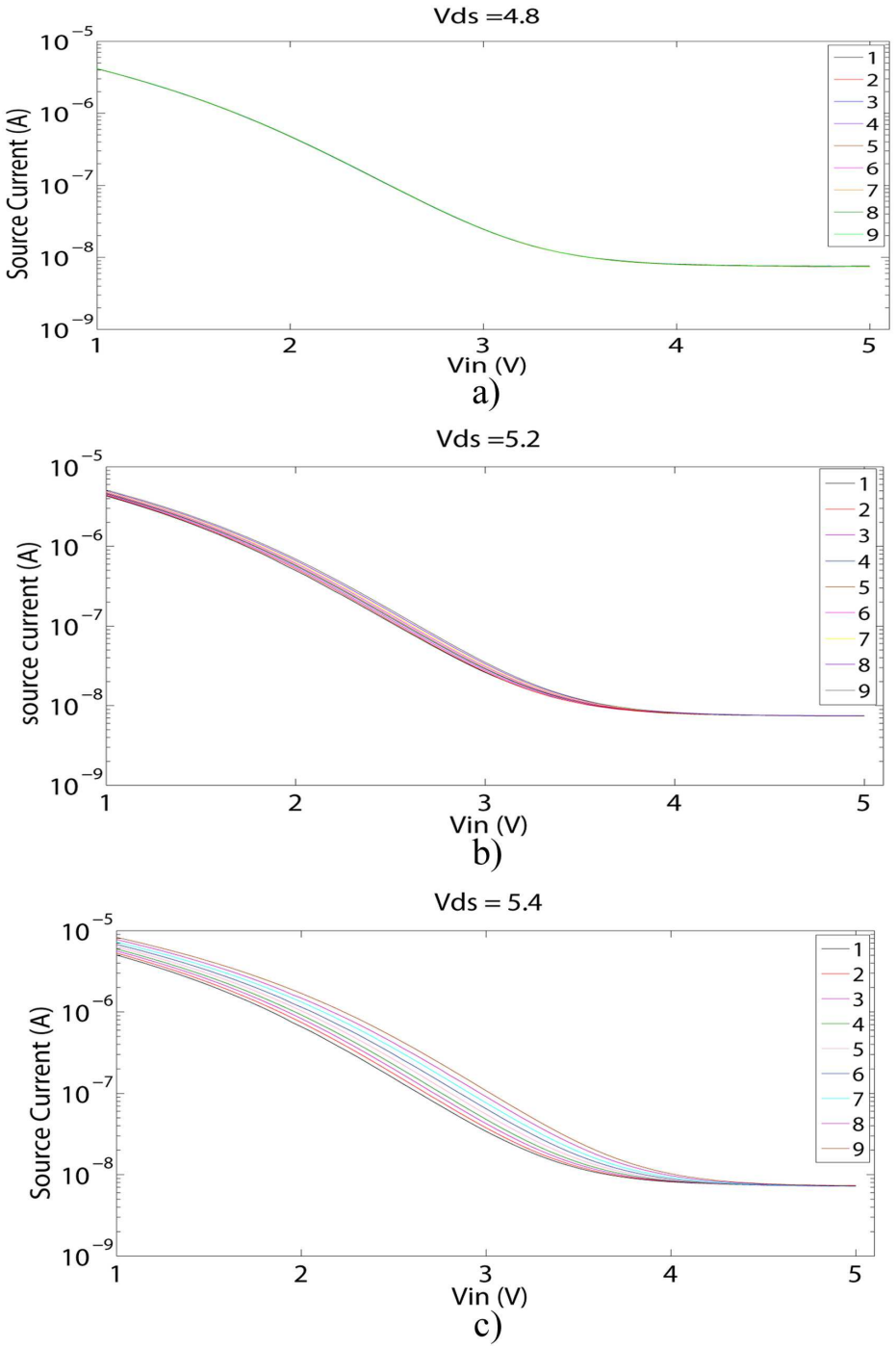


Figure 2.14: The figure shows the transfer characteristics of the floating gate ISFET. a)Plot with drain to source voltage of 4.8 volts b) Plot with drain to source voltage of 5.2 volts c) Plot with drain to source voltage of 5.4 volts. As can be seen in the plots the shift in the threshold voltage increases with the increase in drain to source voltage.

and varying the drain to source voltage. Thus injection is used to precisely control the threshold voltage and the tunneling is used to remove charges, like a global erase.

In this work we use a constant pulse width and vary the drain to source voltage while keeping the input voltage (V_{in}) such that the device is always in sub-threshold regime. A constant pulse width of 10 ms is used to inject charges into the floating node. We use MATLAB to control the arbitrary waveform generator and the source/measure unit. During programming of the device the potentials on tunneling junction (V_{tun}), drain, source and the substrate are kept at the same DC voltage where as the input gate voltage V_{in} is kept so that device is operating in subthreshold. After that the drain voltage is ramped down to 0 volts for a constant time of 10 ms. Figure 2.14 shows plots having different injection rates depending on the drain to source potential. These steps were repeated to obtain the set of curves shown in the Figures 2.14a, 2.14b or 2.14c. An average change in current after each injection was calculated and plotted against the drain to source voltage to obtain the rate of injection as seen in Figure 2.13.

Depending on the initial current of two different pH sensors they can be programmed to reduce the mismatch between them by using the injection rate shown in the Figure 2.13.

Figure 2.15 shows the area of the pH sensors integrated on a 0.5 μm CMOS process. They have been layed in the center of the chip away from the bond pads which are insulated using UV curable epoxy.

2.4 ISFETs on PolyEthylene Naphthalate (PEN) flexible substrate

Flexible substrate has been successfully used for large area OLED display [34]. Taking advantage of the large area and the flexible substrate a prototype of TFT based pH sensor was designed [35].

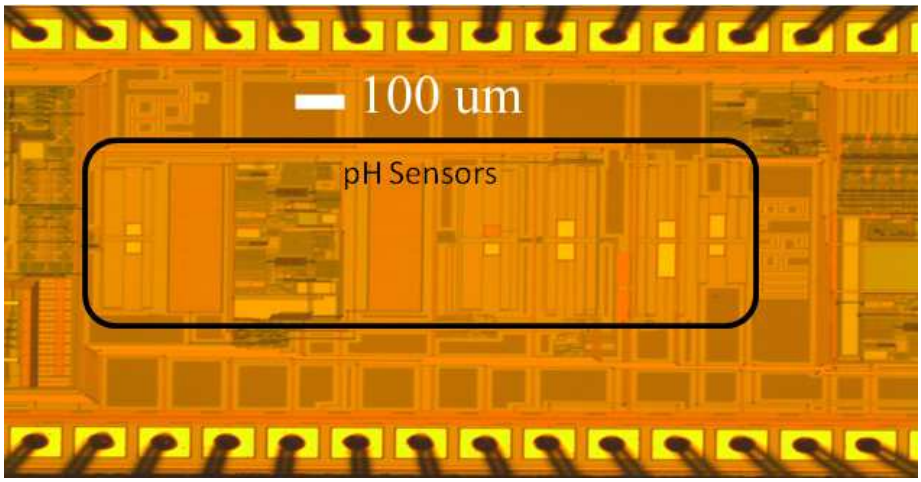


Figure 2.15: Shows the area of pH sensors integrated on a 0.5 μm CMOS process.

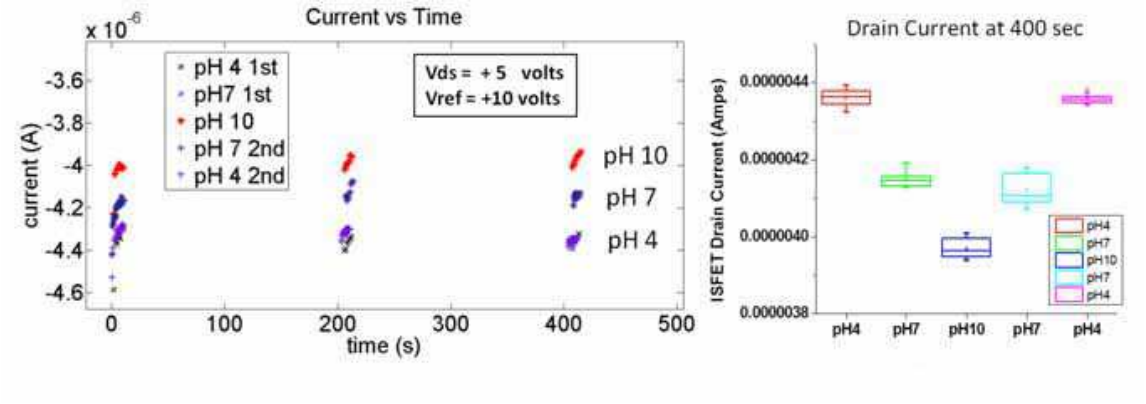


Figure 2.16: (a) The figure shows the current output for different pH values. Drain current was sampled for 10 seconds (b) The figure shows box plot of the drain current for different pH values. It shows the repeatability of the pH sensors i.e giving the same current for the same concentration of H^+ ions.[35]

The ISFETs provided by FDC have a 125 μm thick flexible Dupont Teijin Films Teonex® polyethylene naphthalate (PEN) plastic substrate [35]. A flexible extended gate ISFET prototype was built having $W/L = 9\mu m/9\mu m$ and a 1 mm wide extended gate as shown in Figure 2.17. A silver/silverchloride (Ag/AgCl) reference electrode was printed on the nitride passivation layer. The assembled device is shown in the Figure 2.17.

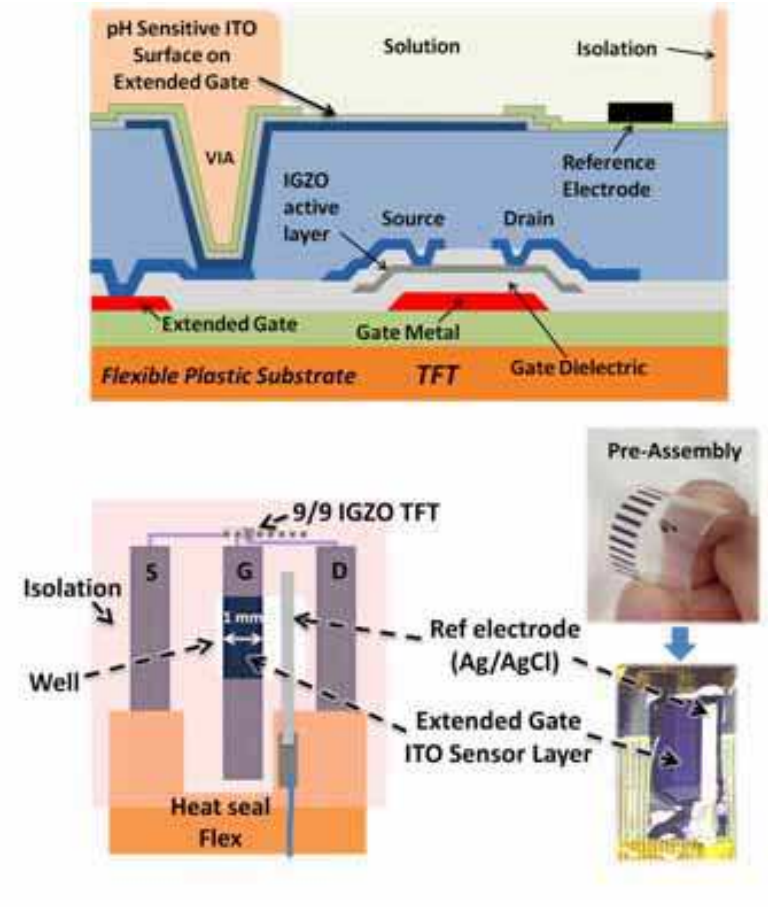


Figure 2.17: (a) Cross-section of the flexible ISFET having $W/L = 9\mu m/9\mu m$. (b) 1mm wide extended gate of the flex ISFET with Ag/AgCl as the reference electrode. (c) Flexible ISFET assembled at flexible display center. [35]

A 3 mm long shallow well for the pH solution was formed over both the extended ITO gate and Ag/AgCl reference electrode using a thin layer of solvent-free epoxy. This created an active (ITO) sensor area of approximately 1 x 3 mm. The drain, source, and reference electrode leads on the PCB were then connected to a Keithley SourceMeter to measure the current-voltage device characteristics, with the gate bias on the reference electrode set to +10 volts, and the drain-to-source bias set to +5 volts. The well was then filled with different pH buffer concentrations using the sequence of pH 4 $\rightarrow$ pH 7 $\rightarrow$ pH 10 $\rightarrow$ pH 7$\rightarrow$ pH 4, with a sample interval of 400 seconds for each pH concentration, and with the ISFET drain current sampled from 0 to 10, 200 to 210, and 400 to 410 seconds in

each interval as shown in Figure 2.16. As shown in Figure 2.16, a decrease in the flexible ISFET drain current was correctly observed as the pH concentration increased from pH 4 to pH 10, confirming decreasing H^+ ion protonation of the ITO extended-gate electrode surface as the pH concentration was increased. ISFET stability and discrimination were also shown to improve at longer measurement intervals with an observed average 4.7% difference in measured ISFET drain current between the three different pH buffer concentrations at 400 seconds (Figure 2.16). Devices shown in this section were provided by Flexible Display Centre (FDC) at ASU. They were designed, built and assembled by Joseph Smith who is a principal engineer at FDC.

Chapter 3

Cell Culture

3.1 Basics of cell culture and microenvironment

Cell cultures refers to removal of cells from plants or animal and growing them in a favourable artificial environment. The cells may be removed from the tissue directly and disaggregated by enzymatic or mechanical means before cultivation, or they may be derived from a cell line or cell strain that has already been already established [36]. Cell culture has been an integral part of biological research for the past century. It provides a means to study the behavior of animal cells, either under normal conditions or the stress of an experiment. The growing use of cell culture in fields including cancer research, stem cell research, and vaccine production has drastically increased this market to the one that is worth billions of dollars. Advancements in these various fields often rely on cell culture experiments for critical data. However, many of the methods for performing this research have been largely unchanged in the past century.

Cells reside in an atmosphere composed of soluble factors, cellmatrix interactions, and cellcell contacts, and do so while living within an environment with specific physicochemical properties (pH, oxygen tension, temperature, and osmolality) as shown in the Figure 3.1 [37]. Changes in pH of the cellular growth media have been shown to affect the growth and the maximum population density of cancer cells [38]. Moreover, it has been suggested that local variation of pH in the micro-environment of a cell's surface may be a significant factor in controlling cell behavior in culture and *in vivo* [39]. Due to the importance of measuring the pH, we investigate the feasibility of Ion Sensitive Field Effect Transistors (ISFETs) to accurately assess cell culture media.

This chapter shows the measurement taken using the ISFETs discussed in the chapter 2. We monitor the pH of cell culture media, which provides insight into the metabolism

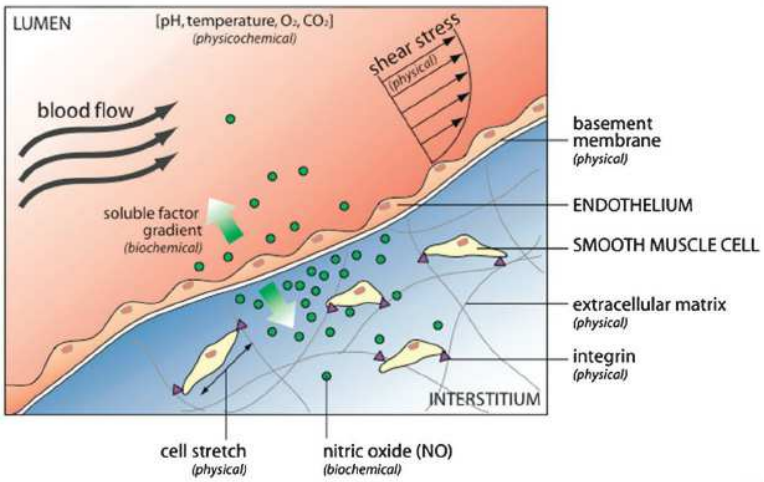


Figure 3.1: The microenvironment of the cells consisting of physical, biochemical and physicochemical factors. pH is one of the physicochemical factors and it affects the behaviour of the cells [37].

of the cells, by culturing them on top of the pH sensor. Figure 3.2 shows the packaged chip on which the cells are cultured.

3.2 Breast cancer cells

Breast cancer is the most prevalent form of cancer in women; in fact, approximately 12.3 percent of women will be diagnosed with breast cancer at some point during their lifetime [40]. We aim to improve patient outcomes by creating sensors to assess the effects of therapeutic drugs on breast cancer cells in real-time. Real-time monitoring of breast cancer cells under the effects of therapeutic drugs can also provide greater insight into the mechanisms involved than more traditional *in vitro* assessments.

The environmental acidity or pH of living cells and tissues is one of the major factors that influence molecular processes involved in cell cycle progression, cell proliferation and differentiation [41]. The microenvironment of the tumor cells is intrinsically acidic mainly due to accumulation of lactic acid as a result of increased aerobic and anaerobic glycolysis by the cancer cells [42][43]. Glycolysis is a metabolic pathway that converts

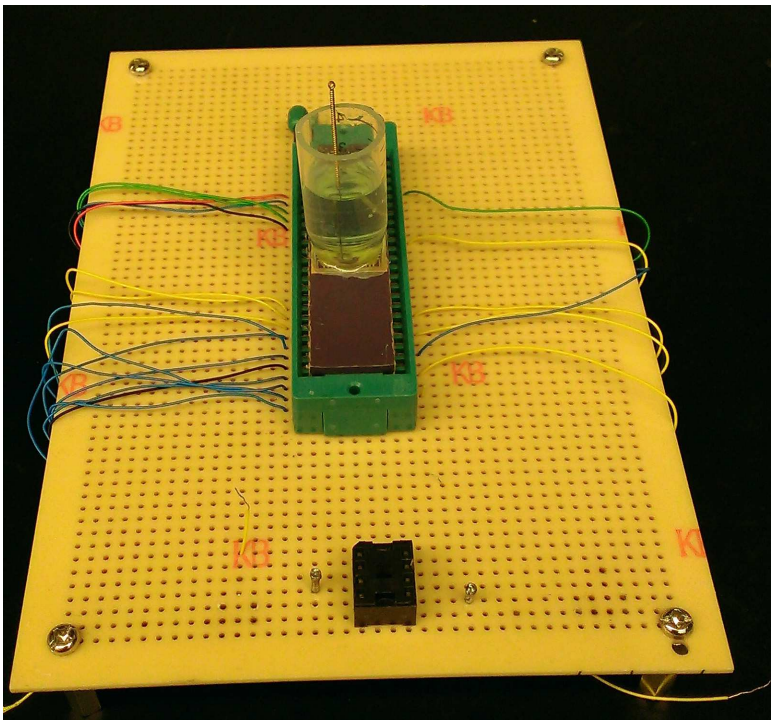


Figure 3.2: Packaged pH sensor on which the cells are cultured.

glucose into into pyruvate. The environmental acidity also greatly influences the response of cancer cells to various treatments [41]. Thus monitoring the pH of the tumor cells has a potential for therapeutic exploitation [44].

For our experiments we used breast cancer cell line SKBR3 (human mammary adenocarcinoma). The growth media used for the cell culture was made using ATCC-formulated McCoy's 5a medium with 10% fetal bovine serum. These cells were cultured on top of an ISFET using standard cell culture procedures and techniques. The cells were allowed to grow over a period of four days, and their growth was monitored by measuring the pH of the cell culture media. As shown in the Figure 3.3 the pH of the cell culture media decreases with an increase in the density of the cells. This is due to the increased glycolysis by the cancer cells.

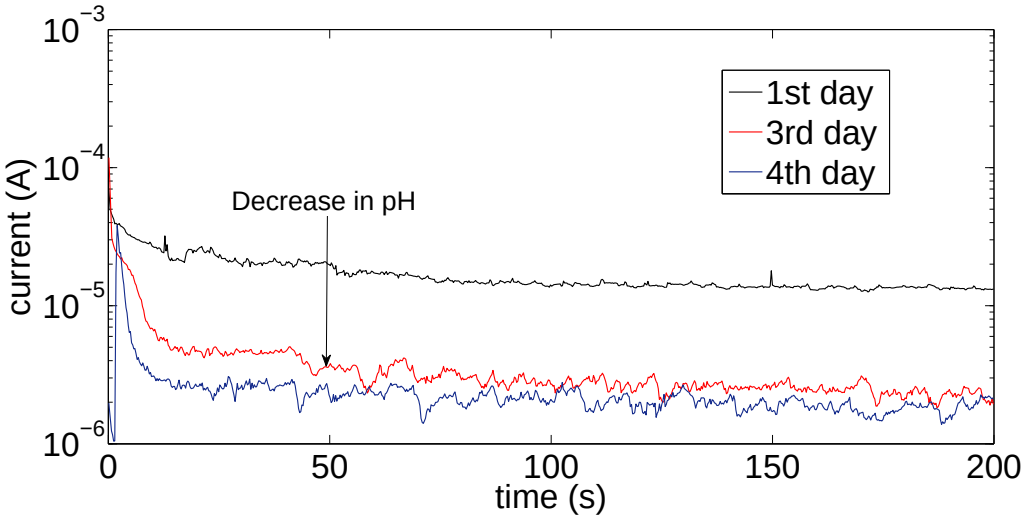


Figure 3.3: Plot showing current output of the ISFET over time. The pH of the cell culture media was measured over a duration of four days.

Staurosporine is an alkaloid, separated from streptomyces staurosporesa. It inhibits protein kinase, which is an enzyme responsible for cell signalling [45]. It is generally administered after dissolving in Dimethyl Sulfoxide (DMSO). A combination of staurosporine, DMSO and the growth media was used to treat the cells grown on top of an ISFET. We replaced the growth media, of the breast cancer cell whose activity is to be monitored, with the solution containing a combination of DMSO, staurosporine and growth media. Figure 3.4 shows the effect of staurosporine on the breast cancer cell. To confirm that the increase in pH is due to the change in cell activity, rather than the DMSO or staurosporine itself, the same experiment was conducted in the absence of breast cancer cells. This is shown in Figure 3.5. The glitch in the current is due to change in the position of the electrode while replacing the solution.

3.3 Discussion

Future work would include measuring intracellular pH of different breast cancer cells like human mammary adenocarcinoma (SKBR3 and MCF7) and T lymphocytes. A continuous

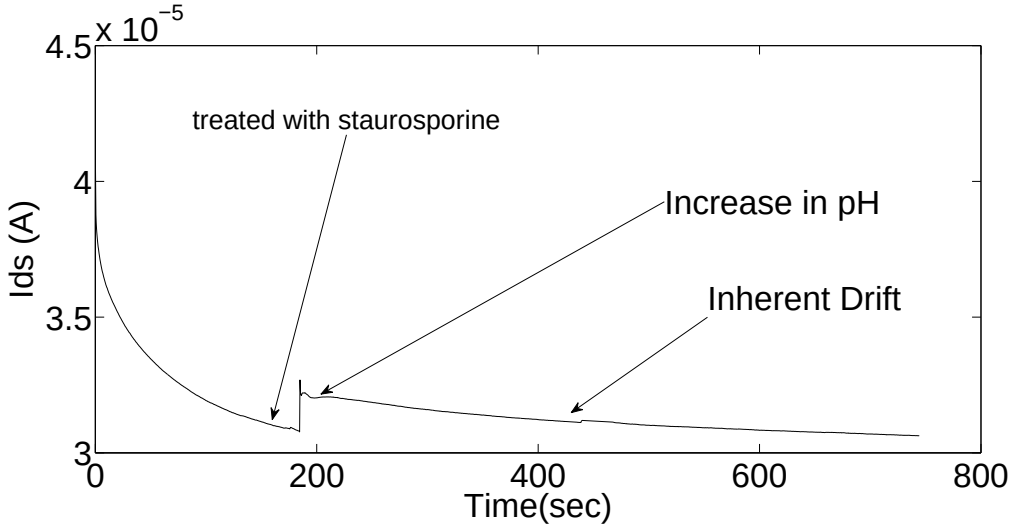


Figure 3.4: Plot showing the variation in pH of the cell culture media when treated with staurosporine. There is change of 1.43 μA

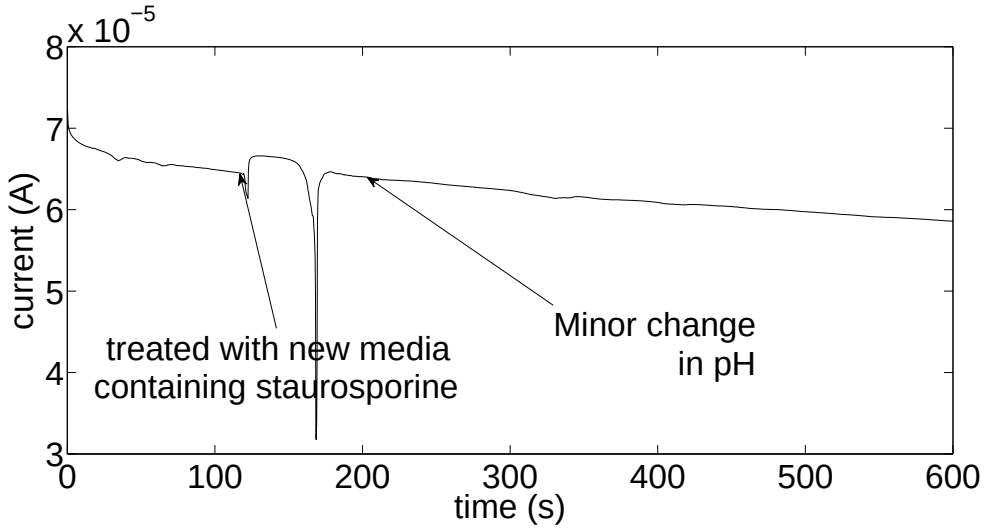


Figure 3.5: Plot showing minor change in pH when media having no cells is treated with the solution containing staurosporine. There is change of 10 nA.

monitoring system having integrated sensors allows us to perform cell viability and the sensitivity to different drugs. Measuring the pH of t-cells allows us to monitor the immune response in humans and animals, this could be faster than the conventional Enzyme Linked Immunosorbent SPOT (ELISPOT).

Chapter 4

Pulse Width Modulation

4.1 Background

ISFETs have an intrinsic drift in threshold voltage as discussed in Chapter 2. As shown in Figure 2.4 the threshold drift in an ISFET can be reset by cycling the vertical electric field. In [17] this was done using MATLAB software and by cycling the potential on the reference electrode. However this does not allow us to monitor the pH continuously since there is a finite amount of time for which the ISFETs are in the cutoff region. To create a continuous monitoring system that implements the cycling, we need to use two or more ISFETs. While any given ISFET is reset, the others could be used to monitor the system. However, this is not possible if the reference electrode is modulated, since it is common to all the devices. Thus we proposed a backgate modulation scheme to allow us to reset individual devices independently. Figure 4.1 shows reset in threshold voltage drift by cycling back gate of the ISFET.

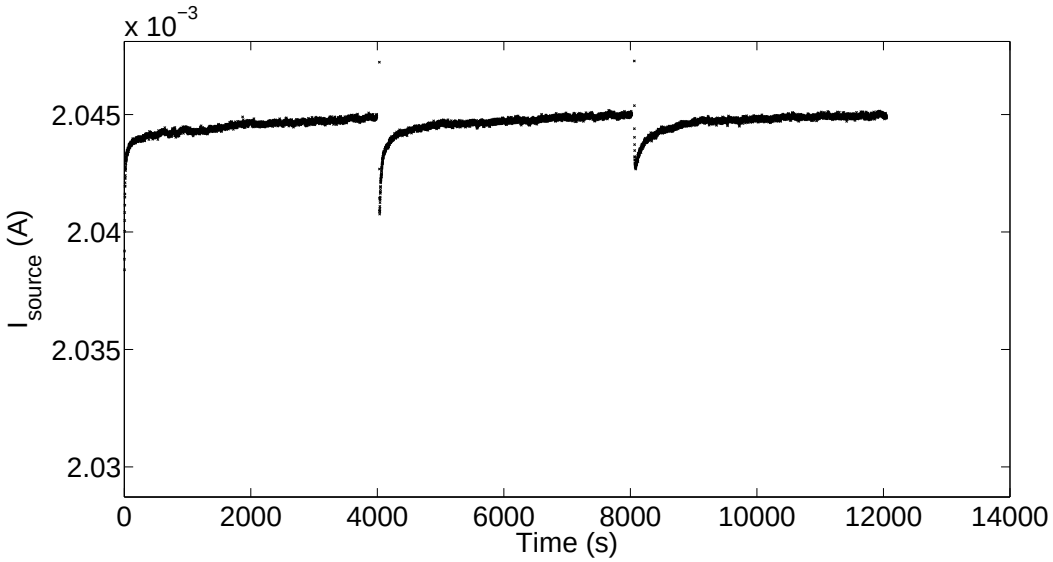


Figure 4.1: Cycling of vertical electric field using back gate.

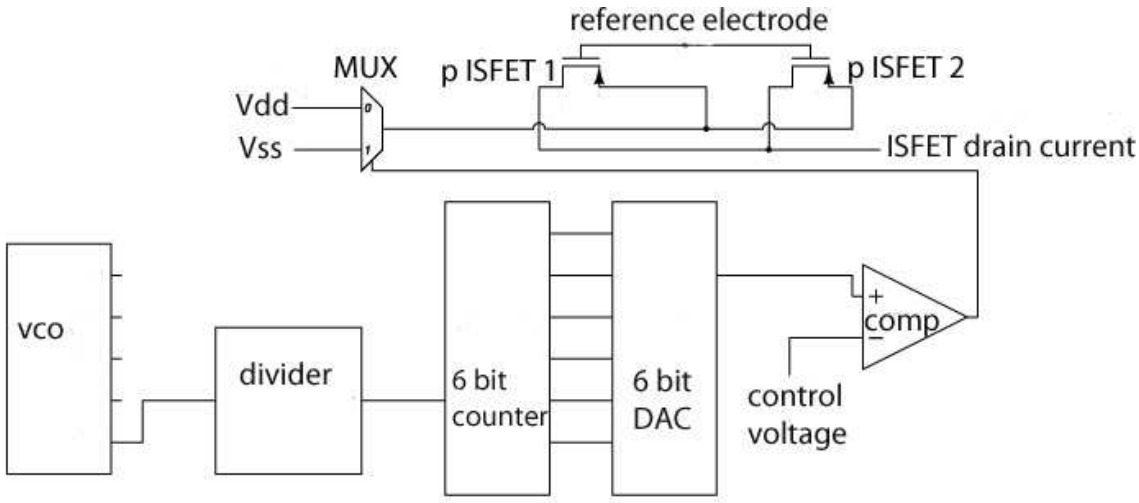


Figure 4.2: Pulse width modulation circuit for cycling vertical electric field of the ISFET[18].

In Figure 4.1 the cycling of the vertical electric field is done using MATLAB software and hence not useful for application where the senors have to be deployed for long term monitoring. A pulse width modulation circuit, shown in the Figure 4.2, which can modulate the vertical electrical field of two or more ISFETs would be appropriate for such an application.

4.2 PWM circuit and output

The PWM circuit consists of a ring oscillator which provides the on-chip clock, 6 bit counter, 6 bit Digital to Analog Converter (DAC), and a comparator as shown in Figure 4.2. The ring oscillator consists of five inverter stages with passive resistor and Metal Oxide Semiconductor (MOS) capacitors. Passive resistors with resistances of 890 KΩ and 8 pF MOS capacitors are used to reduce the frequency of the ring oscillator down to 11.9 kHz since our application requires low frequency due to drift characteristics. All the five resistors have a common centroid layout to reduce the mismatch caused by the process variations. MOS capacitor were used since they have a smaller area compared to

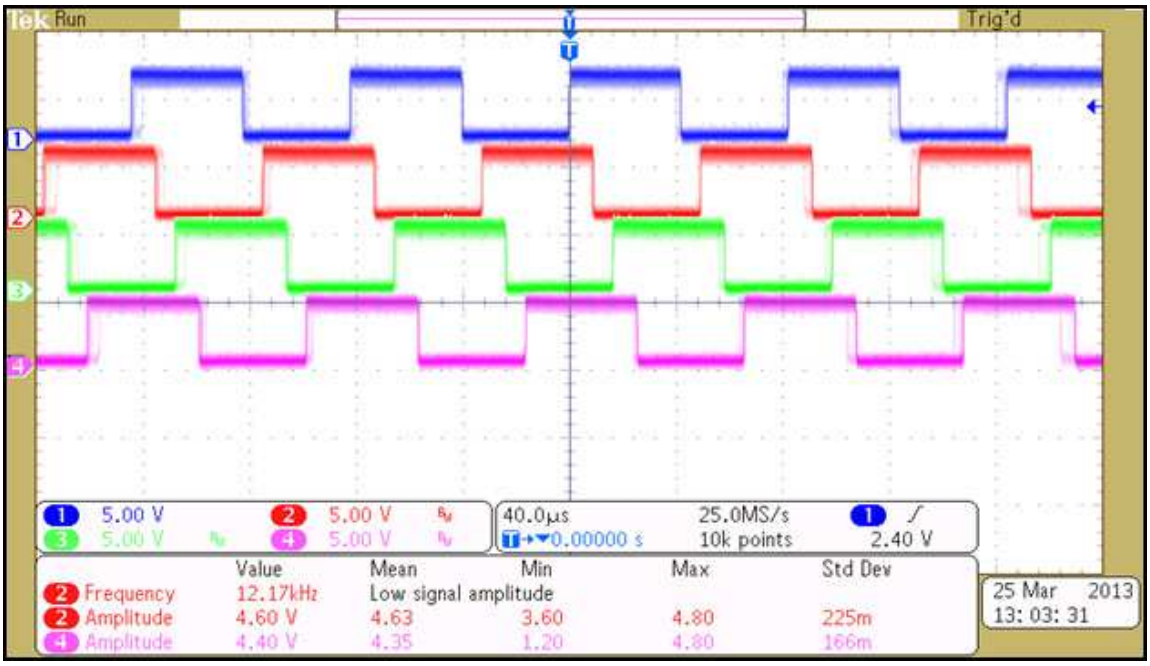


Figure 4.3: Output of the ring oscillator. It has a frequency of 12.17 khz with power supply of 5 volts.

polysilicon capacitors. The output of the ring oscillator is shown in the figure 4.3. It has a frequency of 12.17 Khz with a power supply of 5 volts.

Figure 4.4 shows simulated output of PWM. The figure shows the basic principal behind pulse width modulation. Control voltages are used to obtain different duty cycles.

The output shown in the Figure 4.3 is divided by 100,000 using D-flip flops and combinational logic. The divided output is used as an input to a 6 bit counter, 6 bit DAC and a comparator which provides pulse width modulation depending on the control voltage. In addition to changing the control voltage, which changes the duty cycle of the output, the supply voltage can be tuned to change the period of the output waveform.

A resistor string DAC is used with the value of all the resistors being 4.9 kΩ (high resistance polysilicon resistor). The value of the resistors was selected for the DAC after taking into account the trade-off between area (higher resistor value) and power (smaller

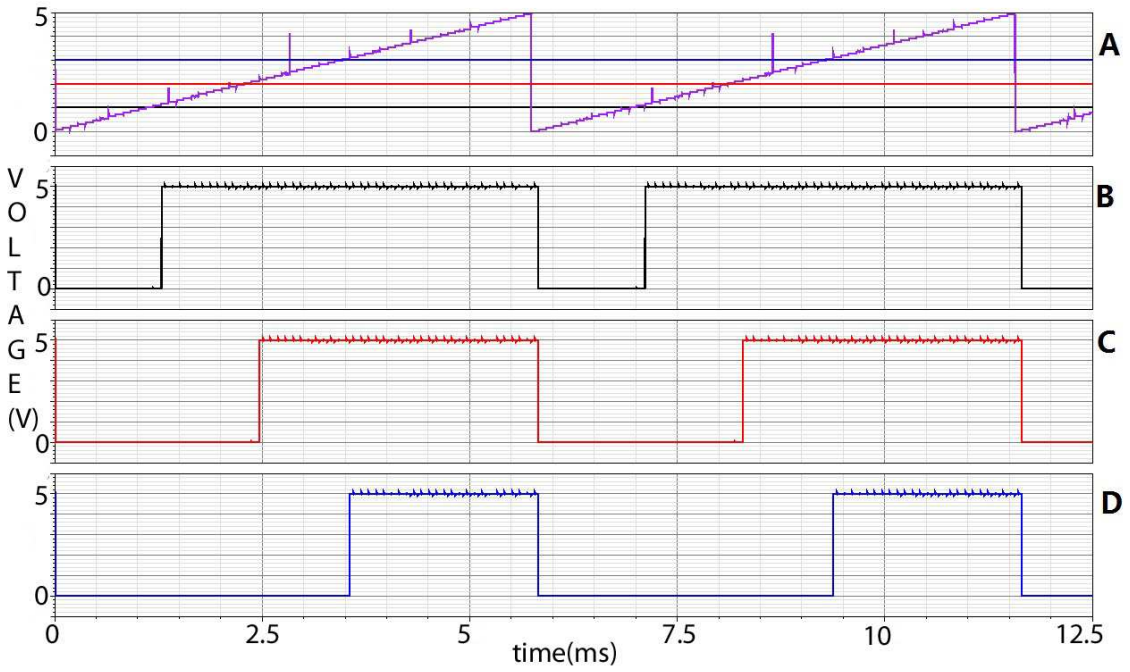


Figure 4.4: Simulation results for the PWM circuit without the divider showing the DAC output (purple) and DC control voltage (red) for the comparator (A), and PWM output corresponding to control voltages of 1 V (B), 2 V (C) and 3 V (D) respectively. By varying the control voltage, the duty cycle of the circuit is modified. For a given application a DC value for the control voltage would be chosen based on the specific parameters.

value). Transmission gates are used as switches, and they derive their input from the 6 bit counter. Transmission gates allow a full swing at the input to pass without any voltage drop at the output but occupy larger area. To simplify the layout, transmission gates have been used for all the switches in the DAC instead of replacing them with pass transistors on the nodes where the full swing is not expected.

The comparator has an offset of 10 mV obtained by performing an overdrive recovery test. The comparator has a preamplifier, cross-coupled inverter and cross-coupled NAND gate. The cross-coupled inverter is pre-charged every clock period. The cross-coupled NAND gate is used for regenerative feedback to latch the output of the com-

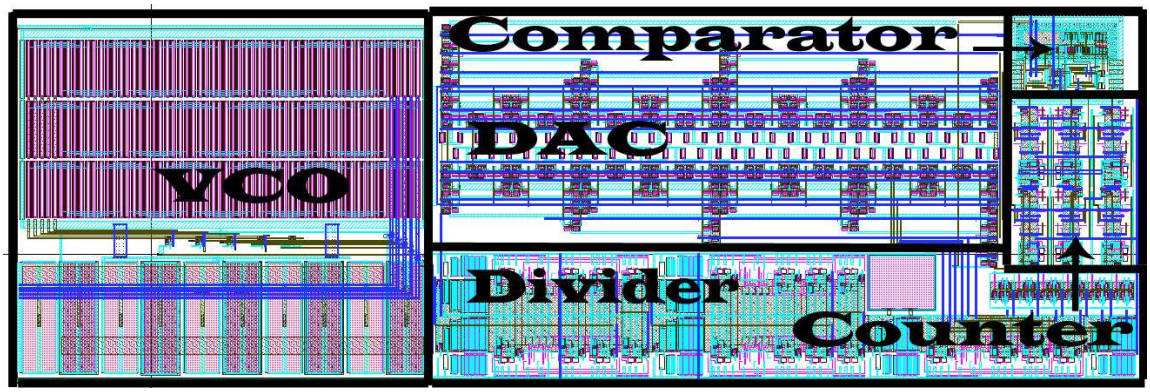


Figure 4.5: The layout of pulse width modulation circuit fabricated in a 0.5 μm technology. The area occupied by the pulse width modulation circuit is 320 μm $\times$ 1000 μm

parator. Dynamic comparators are high speed and have lower power consumption. The preamplifier used in the comparator reduces the input offset voltage.

The modulated waveform is used as a select line for the 2 to 1 multiplexer, whose inputs are hard wired to VDD and GND to cycle between the two ISFETs. The multiplexer is connected to the source and the body of ISFET1 and through an inverter to ISFET2, allowing us to monitor the pH continuously by alternating between the two ISFETs.

The output period is varied by tuning the power supply and the duty cycle is can be varied by controlling the comparator voltage. Figures 4.6 and 4.7 shows output of pulse width modulation circuit. Figure 4.5 shows the area and layout of pulse width modulation circuit in a 0.5 μm technology.

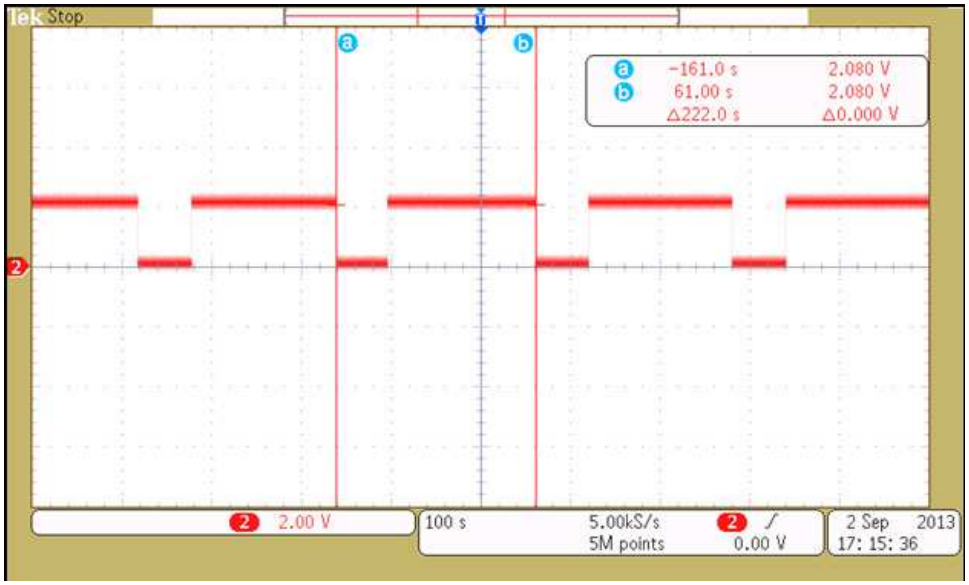


Figure 4.6: The pulse width modulated waveform with power supply equal to 2 volts. Comparator voltage is set to 0.5 volts.

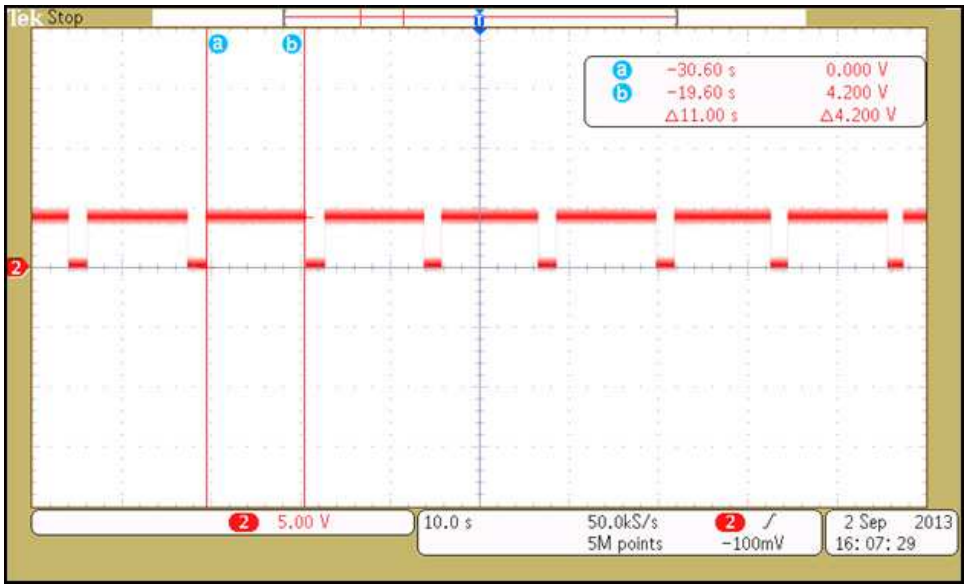


Figure 4.7: The pulse width modulated waveform with a higher duty cycle. The power supply voltage is tuned to 4 volts to show tuning of frequency

Chapter 5

Operational Transconductance Amplifier

Operational Transconductance Amplifiers (OTA) are at the heart of the majority of analog signal processing circuits. They are used as a part of Analog to Digital Converters (ADC) and Transimpedance amplifiers, which make the front end of analog readout circuits. A chopper stabalized folded cascode amplifier as shown in figure 5.1 was fabricated in 0.5 μm process to be used as a part of the readout circuit. A Folded cascode amplifier has an advantage of having a high output swing, high gain-bandwidth product, high input common mode range and possibility of using it at lower supply voltage. Since there are two branches in a folded cascode amplifier it requires higher current requirement compared to a telescopic cascode amplifier having the same gain and -3 dB bandwidth. A cascoded current mirror, to improve the Common Mode Rejection Ratio (CMRR), is biased by wide swing biasing circuit not shown in the figure.

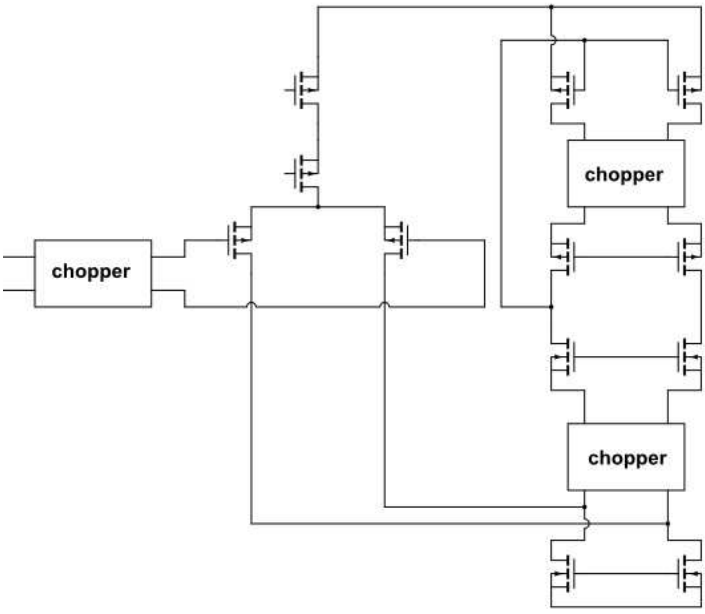


Figure 5.1: Chopper stabilized folded cascode amplifier without biasing circuit

5.1 Offset and flicker noise Cancellation

Biological processes generally occur at very low frequencies. At low frequency the noise in the transistor is dominated by flicker noise. Flicker noise is due to fluctuation in conductance and it has a power spectral density which is inversely proportional to frequency (1/f)[46]. This combined with the DC offset of an amplifier may degrade the signal measured from the biosensor. Various offset cancellation and flicker noise cancellation techniques have been used [47]:

1. Autozeroing (Az)
2. Chopper Stabilization
3. Correlated Double Sampling (CDS)

AZ and CDS are generally used in discrete time system. A chopper stabilized amplifier achieves the lowest drift and offset performance. They are widely used to build precision operational amplifiers. Taking into consideration that our system is continuous time a chopper stabilization was used to remove the offset and 1/f noise. Chopper stabilization uses modulation to transpose the signal to a higher frequency, where there is no 1/f noise, and demodulates it back to the baseband after amplification. In the process 1/f noise and the offset is modulated to the chopping frequency. A CMOS amplifier has finite gain and bandwidth because of which the amplifier output (after the low pass filter) is $A_0 * V_{in} * 8/\pi^2$, assuming that the gain of the amplifier stay constant (A_0) till twice the chopping frequency[47]. Figure 5.2 shows the basic principle behind chopping. As a rule of thumb $f_{signal} < f_{chop} < f_{unity}$ where f_{signal} is the frequency of the processed signal, f_{chop} is the chopping frequency and f_{unity} is the bandwidth of the amplifier. A non overlapping clock generator as shown in the Figure 5.3 was used to generate the necessary non overlapping clock.

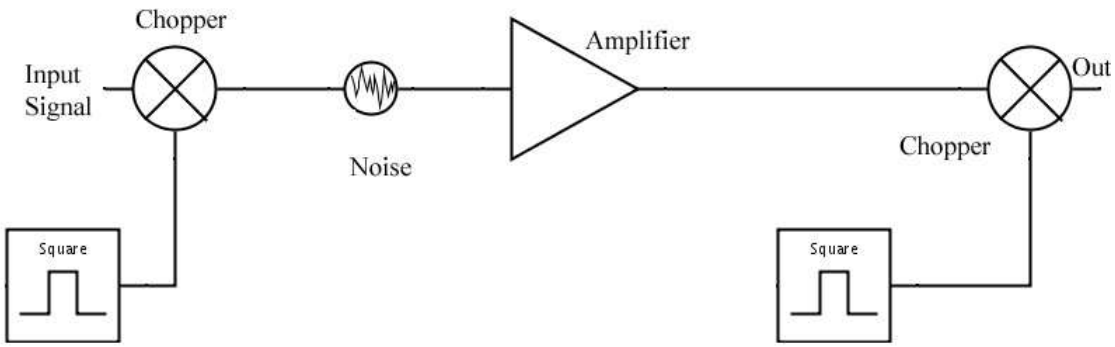


Figure 5.2: System level schematic of a chopper stabilized amplifier

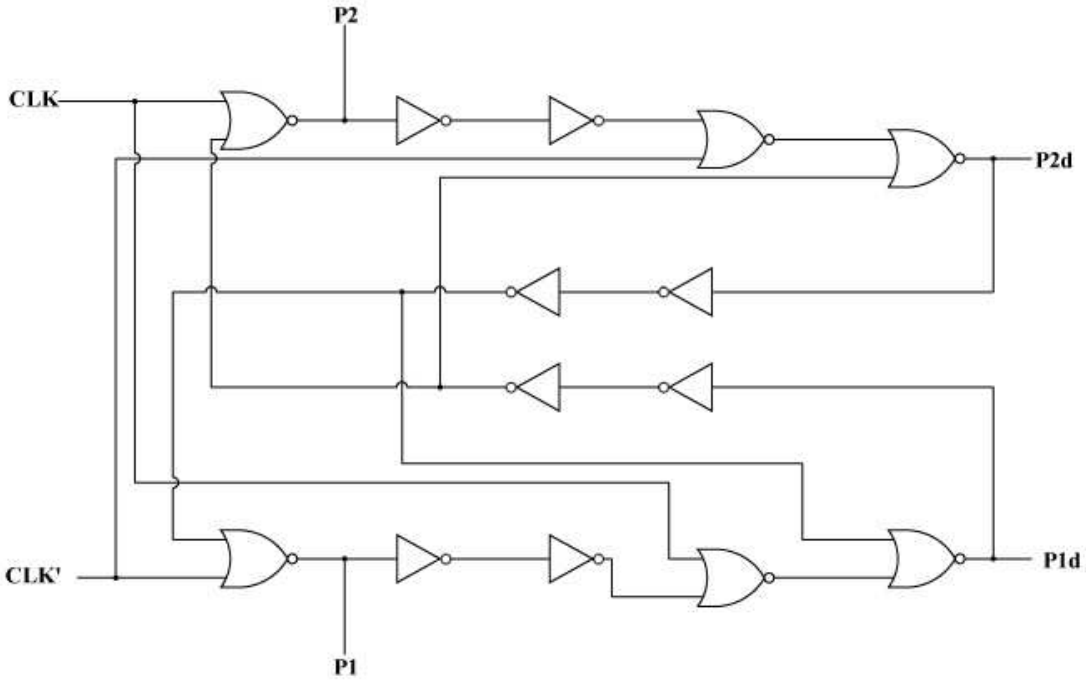


Figure 5.3: Schematic of a phase non-overlapping clock generator. It generates two phases and their delayed version.

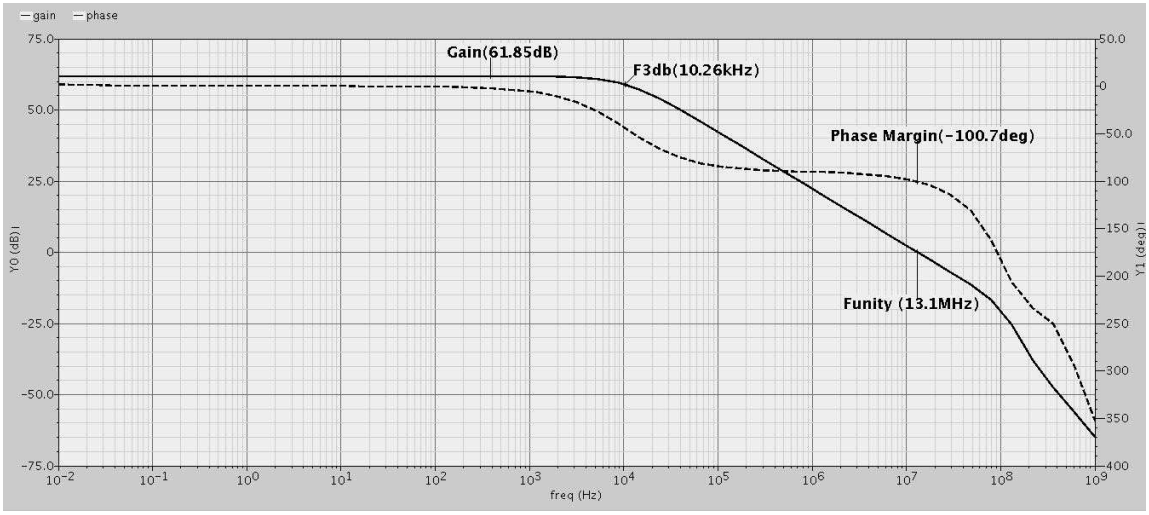


Figure 5.4: AC response of the chopper stabilized folded cascode amplifier

5.2 Simulated and measured data

To obtain AC response of the amplifier a Periodic Steady State (PSS) analysis was performed along with periodic AC analysis. Input referred noise was simulated using periodic noise analysis. All the analysis performed here is done using spectreRF. Figure 5.4 shows the AC simulation of the folded cascode amplifier. Since f_{3dB} of the amplifier is 10 KHz the chopping frequency used is 100 KHz, which follows the rule of thumb described earlier. Figure 5.5 compares the input referred noise measured with and without chopper stabilization. As can be seen from the Figure 5.5 at very low frequency the $1/f$ noise is dominant and in case of the biosensors, where in general signal output is very low, it will become the limiting factor and thus will determine the dynamic range of our readout circuits. To increase the dynamic range of the readout circuits chopper stabilization is necessary, which reduce the input referred noise.

Figure 5.6 shows measured data of the folded cascode amplifier in source follower configuration. Figure 5.7a shows the configuration used to perform spectrum analysis of the output of the amplifier. A 20 Khz is given as an input to the OTA as shown in the Figure 5.7b and a spectrum analyzer is used to measure the output of the amplifier

Figure 5.5: Input referred noise of the folded cascode amplifier. Chopping reduces the input referred noise to 25 $\mu V/Hz^{1/2}$

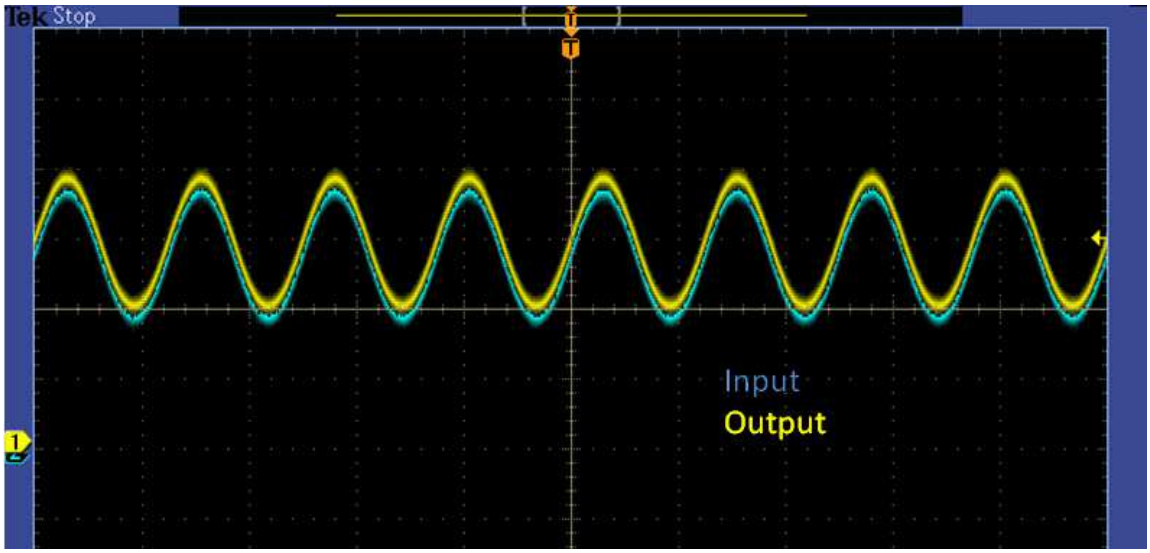


Figure 5.6: Transient analysis of the folded cascode amplifier in source follower configuration having a 20 Khz input. The measurement done using the setup shown in the figure 5.7a

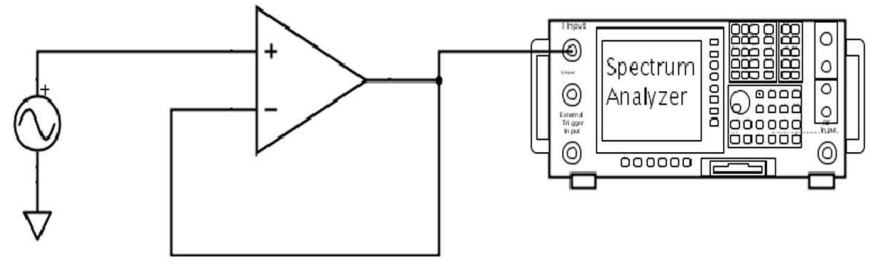
Table 5.1: OTA specification

Specification	Value
Gain	61.85 dB
-3 dB cut-off frequency	10.26 kHz
Funity	13.1 MHz
Phase margin	80°
Chopped input referred noise at DC	25.1 $\mu V/Hz^{1/2}$
Chopping frequency	100 kHz
PSRR	64 dB
CMRR	95 dB
Slew Rate	$6\,V/\mu s$
Power consumption (5 volts power supply)	1.8 mW
Area	$210\mu m * 209\mu m$

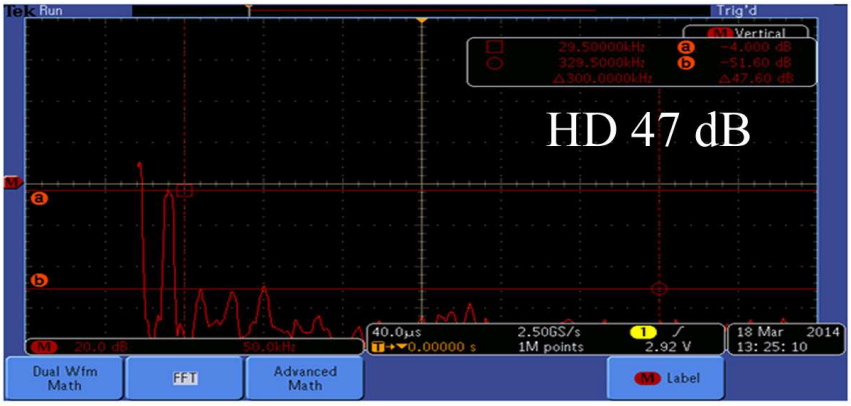
as shown in the Figure 5.7c. Figure 5.7c shows the spectrum of the output signal and distortion caused by the amplifier. Table 5.1 shows the specification of the designed OTA. Figure 5.8 shows the layout of the OTA described here. Some of the layout techniques used to reduce the mismatch in the device were common centroid layout, laying dummy devices and symmetric layout.

5.3 Transimpedance amplifier

Transimpedance amplifiers are the most commonly used current to voltage converters. They form a part of the analog front end used for the readout of electrical signals produced by a transducer. Our work involves using transimpedance amplifier to convert the current produced by an ion sensitive field effect transistors. The amplifier used in the transimpedance amplifier has the same specification as the OTA described in the previous section. Chopping is not used while using the OTA as a transimpedance amplifier since it tends to inject charges into the device which it is trying to measure and eventually offset the advantage of chopping.



a)



b)

c)

Figure 5.7: a) Source follower configuration for the OTA to analyze the output of the OTA. b) Fast Fourier Transform (FFT) of the input signal having a frequency of 20 kHz. c) FFT of the output signal at 20 kHz and the distortion caused by the amplifier when a full scale input is given as the input.

Figure 5.8: The figure shows the layout of the OTA. Common centroid layout technique is used for the input differential pair.

Figure 5.10 shows the measurement of voltage vs time with buffers having different pH values. The measurements are performed using setup shown in the Figure 5.9. The ISFET used has the characteristics shown in the Figure 2.2 in Chapter 2.

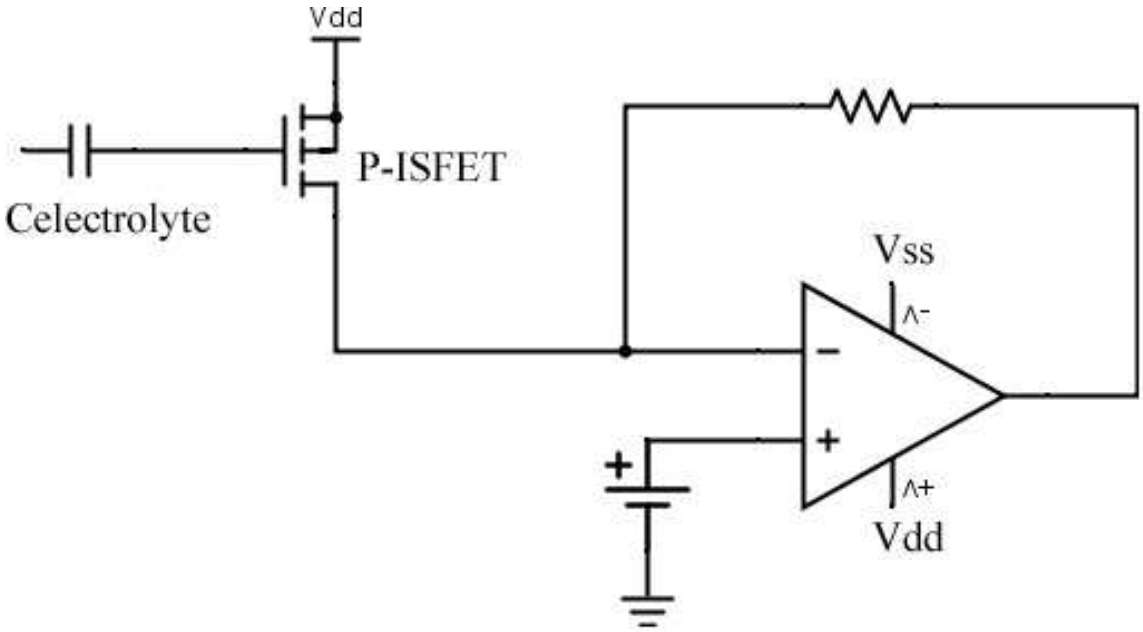


Figure 5.9: A schematic diagram showing a transimpedance amplifier used to convert current from p-channel ISFET to voltage. The amplifier has the specification given in table 5.1 without the chopping. The power supply used is 5 volts which is the typical power supply voltage for the 0.5 μm process.

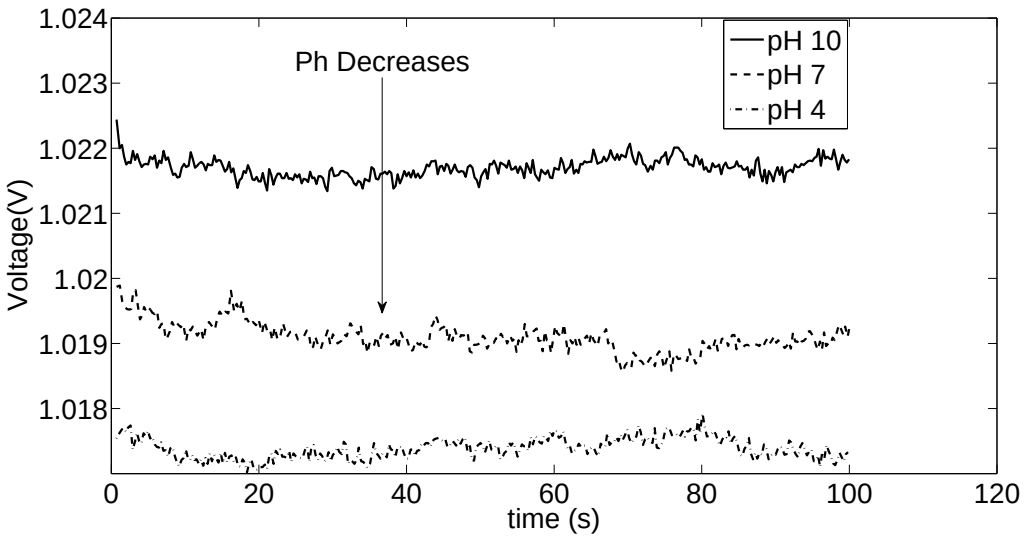


Figure 5.10: pH measurement performed using the described transimpedance amplifier. The setup shown in Figure 5.9 is used to perform the measurements.

Chapter 6

Analog to Digital Converter

6.1 Introduction

Digital circuits are robust, immune to noise, and able to attain increasingly higher speed and computation density due to the advances in Very Large Scale Integration (VLSI) [48]. For these reasons, it is attractive to perform signal processing and computation in digital domain.

The fact that the physical world is composed of analog signals hinders us from performing data acquisition in digital domain. Figure 6.1 shows an Analog to Digital Converter (ADC) acting as an interface to the physical world. The output of a biosensor is a continuous time analog signal which needs to be converted to a digital signal for signal processing. Figure 6.2 shows the signal chain of a pH sensor's readout circuit.

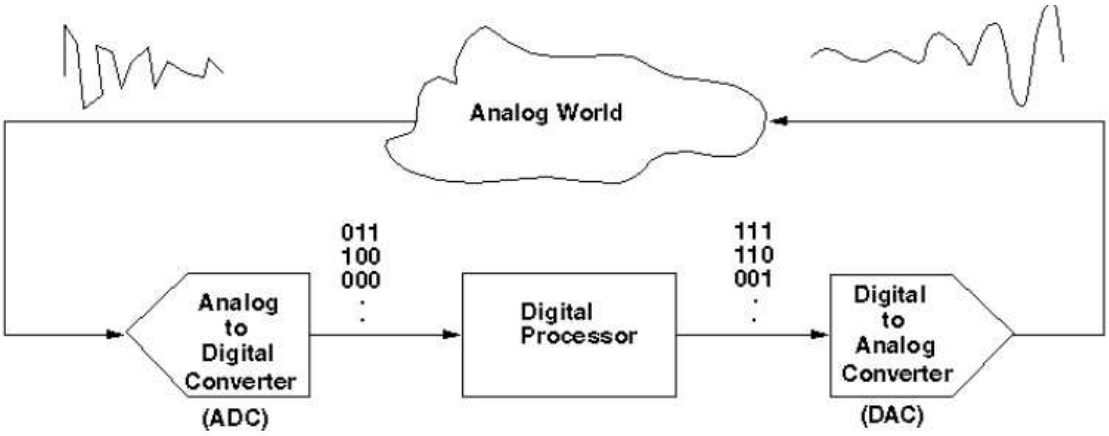


Figure 6.1: Analog to digital converter acting as an interface between the physical (analog) world and digital signal processor. [49]

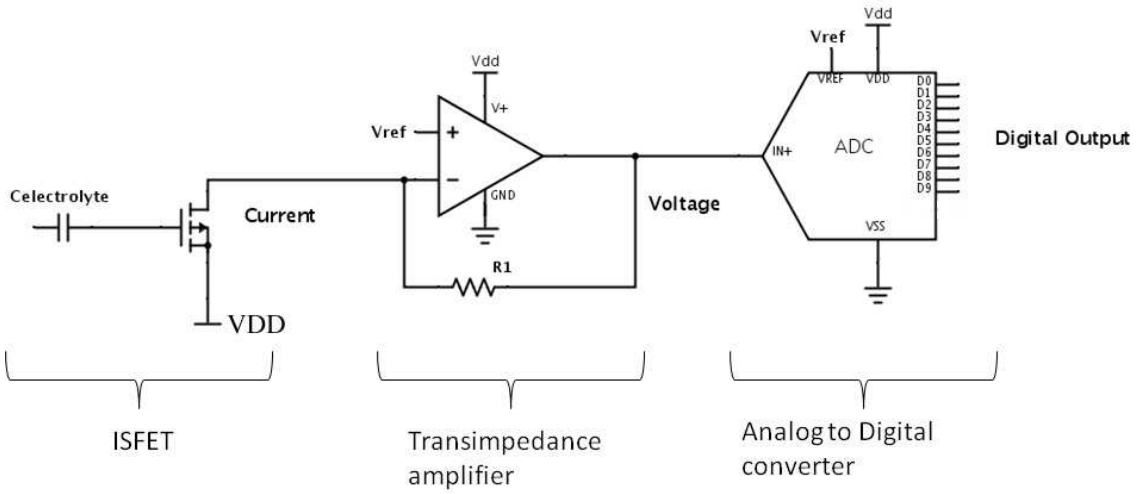


Figure 6.2: The figure shows the signal chain of a pH sensor readout circuit. The transimpedance amplifier serves as the analog front end for the readout circuit. An Analog to Digital Converter also forms a critical part of the readout.

6.2 Motivation

There are several ADC architectures which can be used as a part of the readout circuit. Table 6.1 shows a simple ADC matrix which is helpful in choosing the ADC architectures. A comparison of ADC architectures with respect to their resolution and sampling rate is given in the Figure 6.3 [50].

The readout circuit in this work is designed for reading the output of biosensors, in particular a pH sensor. The pH sensor here is being used to monitor the pH of the cell culture media as discussed in Chapter 3. Other application include monitoring the acidification of oceans, where pH has changed by 0.11 between 1751 and 2004 [51]. Thus the application requires an ADC which has a medium to high resolution at low bandwidth, good noise rejection and fairly low power consumption.

A dual slope ADC provides high resolution and good noise rejection for low bandwidth applications. It also has a high linearity and low power consumption. Thus it was more feasible to design a 10 bit dual slope ADC.

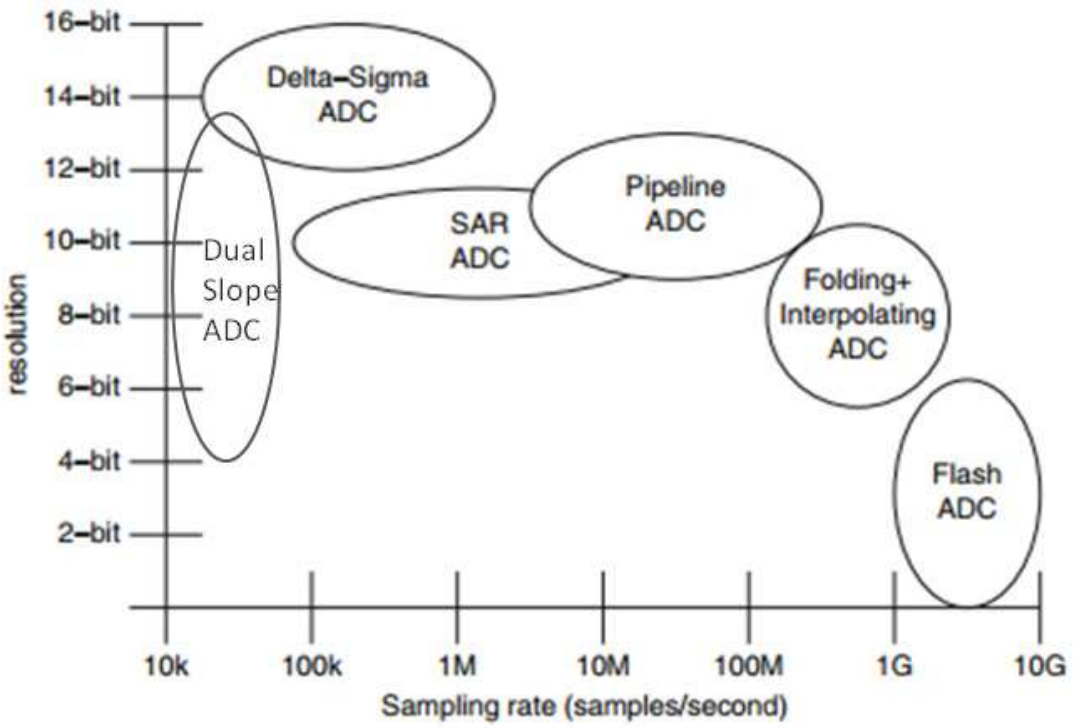


Figure 6.3: The figure shows a plot comparing the resolution and the sampling rate of different ADC architectures (Adapted from [50]).

Table 6.1: Analog to digital converter architectures

Architecture	Power	Sampling Rate	Resolution
Flash	Very high	6.5 G	6 bits
SAR	Medium	100 K	12 bits
Dual Slope (Integrating architectures)	Low-Medium	Dc signal	16 bits
Pipeline ADC	Medium	500 M	18 bits
Sigma Delta ADC	Low-Medium	300 k	24 bits

6.3 Integrating and Dual Slope ADC

Integrating ADCs are ideal for high resolution low speed application. They have a good noise rejection and are good at digitizing low bandwidth signals. Conventionally they are

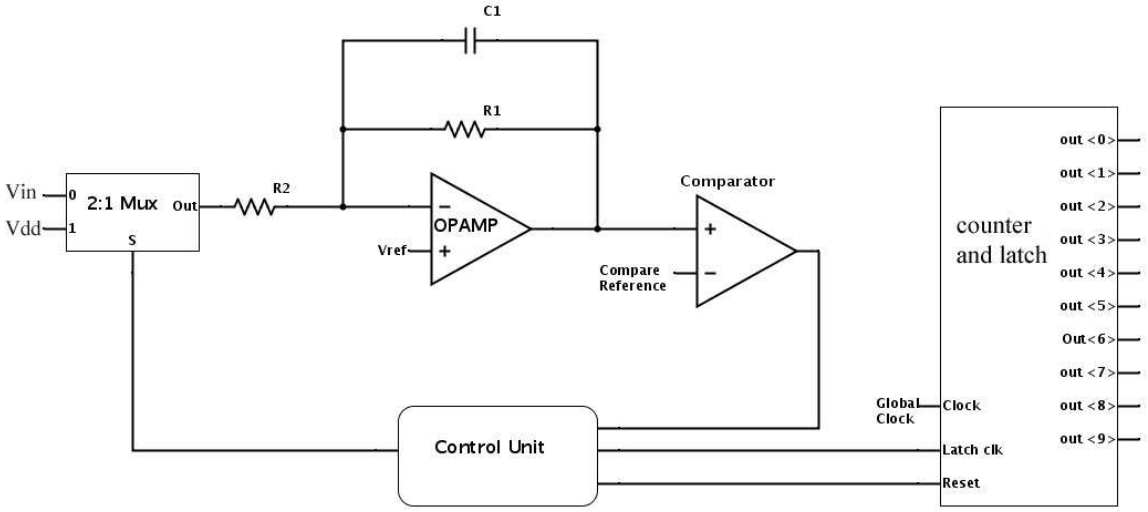


Figure 6.4: A simplified diagram of a 10 bit dual slope ADC.

used in a digital multimeter to read DC voltages. But recently they have been used as a part of a current acquisition circuit for a amperometric biosensors [52].

A simplified diagram of a dual slope ADC is shown in the Figure 6.4. A dual slope starts with integrating an unknown input voltage for a fixed length of time t_1. This part where the ADC integrates the unknown input signal is known as run up [53]. The output voltage at the end of run up is due to the integration of input voltage on the feedback capacitor and is given by Equation 6.1.

$$V_o(t_1) = -\frac{1}{RC}\int V_{in}(t_1)dt \tag{6.1}$$

where V_o is output voltage of the integrator, V_{in} is the input voltage, R is the input resistor, C is the feedback capacitor and t_1 is the run up time.

At the end of run up the input of the integrator is switched to a reference voltage and the feedback capacitor is discharged through the input resistor. This portion is known as run down and during this time a counter keeps track of the time it takes to discharge the capacitor. The value of the counter is latched when the output of the integrator reaches a

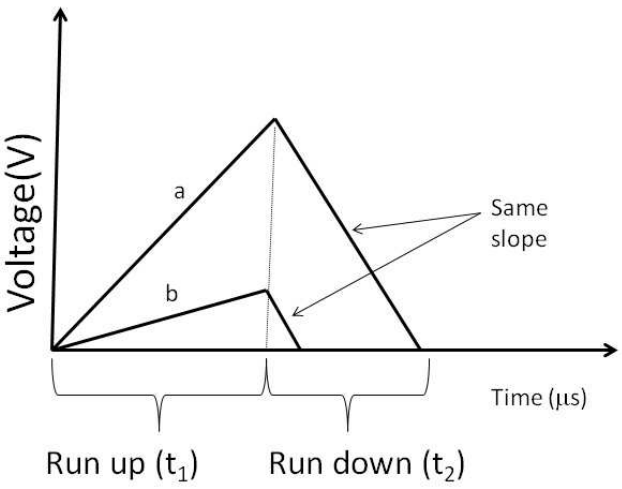


Figure 6.5: The output waveform of a dual slope ADC. Run up phase of the ADC is when unknown input voltage is integrated for a fixed time. Run down is the phase when the feedback capacitor is discharged with a constant slope. A larger input voltage is integrated in (a) compared to (b) and hence it takes longer time to discharge. This discharge time is counted using a counter and given as an output.

specified reference voltage, given to the comparator. The time for run down (t_2) is given by the equation 6.3. Figure 6.5 shows the output waveform of the dual slope ADC integrator.

$$\frac{V_{in}}{RC}t_1 = \frac{V_{ref}}{RC}t_2 \tag{6.2}$$

$$t_2 = \frac{V_{in}}{V_{ref}}t_1 \tag{6.3}$$

As can be seen by the equation 6.3 the conversion time and hence the accuracy is not dependent on the component values. Thus the resolution of a dual slope ADC is not

affected by process variation. The dual slope has a trade off between the speed and the resolution. The conversion time doubles with every bit increase in the resolution. Hence a dual slope ADC is well suited for our application where resolution is important and the conversion time is fast enough for the slow changing biological processes like growth of breast cancer cells.

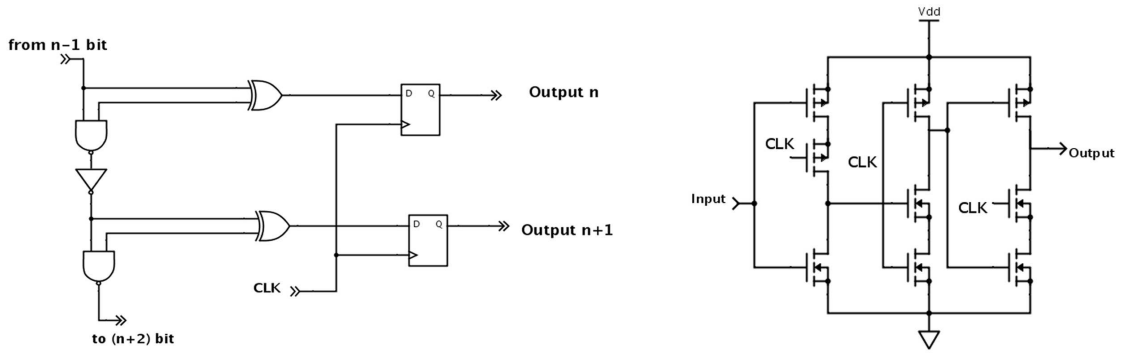
6.4 Design and Simulation Results

The chopper stabilized dual slope ADC discussed in Chapter 5 was used as a part of the integrator. Since there is a trade off between the speed and the resolution a 10 bit ADC was designed. This required designing a 10 bit counter and a latch. Pass transistors were used as the switches instead of optimizing for the voltage levels, to reduce the layout effort. The control unit as seen in the Figure 6.4 controls the MUX select, the reset on the counter and decides when to latch the output of the counter.

The 10 bit counter is designed using Nand and Xor gate with D-flip flop. The flip flop used has a True Single Phase Clock (TSPC) architecture. Figure 6.6a shows two bit counter used to design the 10 bit counter and 6.6b shows the TSPC flip flop. The flip flop has a setup time of 70 ps and hold time of 126 ps. The clock to Q delay of the flip flop is 482 ps.

Figure 6.7 shows a 1 bit reset latch used. The latch and the counter both form a part of the 10 bit counter and latch for the dual slope ADC. They are controlled by the control logic, which is a combination of gate and flip flop, depending on the output of the comparator. The latch has a setup time of 351 ps, which is measured with reference to the falling edge of the clock. The D to Q delay of the latch is 433 ps.

The comparator has a preamplifier, cross-coupled inverter and cross-coupled NAND gate. The cross-coupled inverter is pre-charged every clock period. The cross-coupled NAND gate is used for regenerative feedback to latch the output of the comparator. Dy-



a) b)

Figure 6.6: a) Schematic of a 2 bit counter. b) The D-flip flop has an architecture of a True Single Phase Clock (TSPC). The flip flop, designed in a 0.5 μm process, has a setup time of 70 ps and a hold time of 126 ps. The Clock to Q delay of the flip flop is 482 ps.

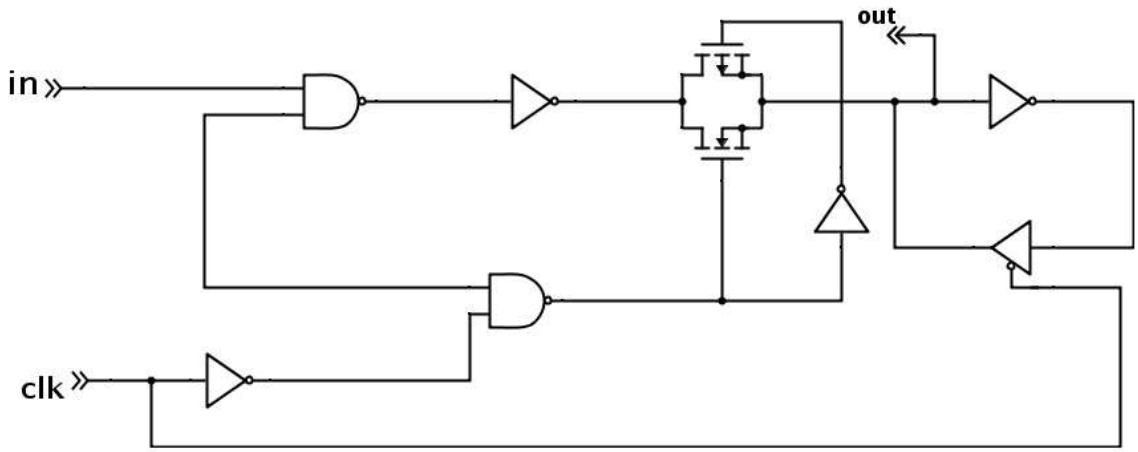


Figure 6.7: Schematic of a 1 bit latch. The setup time of the latch is 351 ps.

namic comparators are high speed and have lower power consumption. The preamplifier used in the comparator reduces the input offset voltage. The offset voltage of the comparator is 10 mV, obtained using overdrive recovery test.

The Figure 6.8 shows the layout of the dual slope ADC designed in 0.5 μm technology.

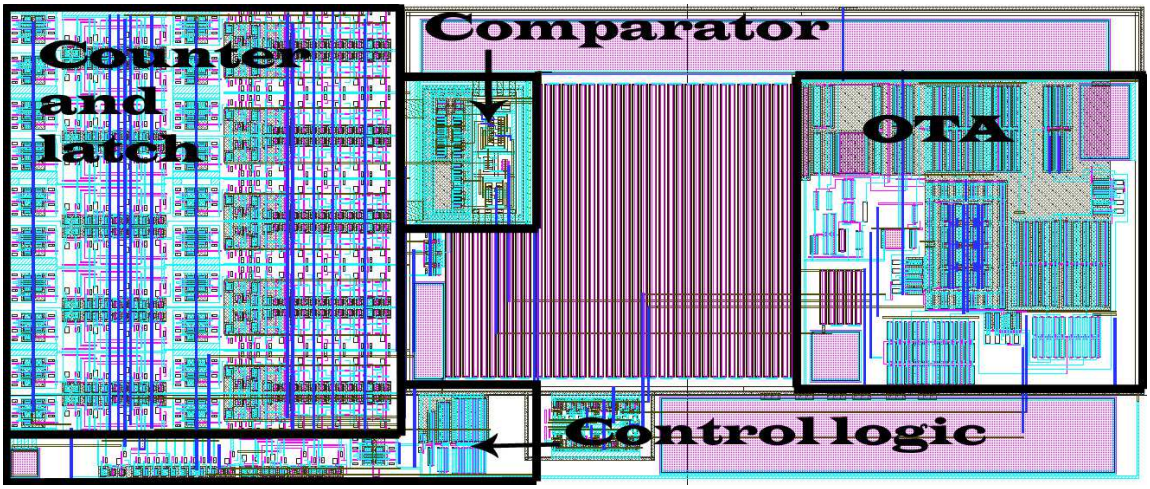


Figure 6.8: The layout of the dual slope ADC designed in 0.5 μm process. Individual components of the ADC are also shown in the figure. The total area of the layout is 322 μm $\times$ 773 μm

Initial characterization of an analog to digital converter is done using a digital to analog converter at the output for ”back-to-back” testing. This is shown in the Figure 6.9. The DAC and input source used should have a higher linearity compared to the ADC which is being characterised. To see the response of the chopper stabilized dual slope ADC a full scale sinusoidal input signal was given to the ADC and the output of the DAC was analyzed shown in the Figure 6.10. Figure 6.10a shows the output of the DAC and Figure 6.10b shows the power spectrum of the sinusoidal output. The power spectrum of the output is obtained by performing FFT in MATLAB with a hann window [54]. The signal to noise ratio of the ADC is 56.3 dB and a effective number of bits equal to 9.

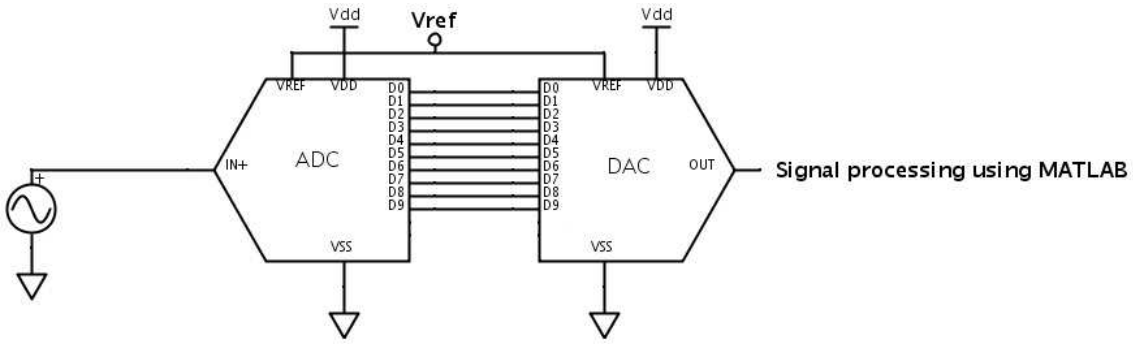
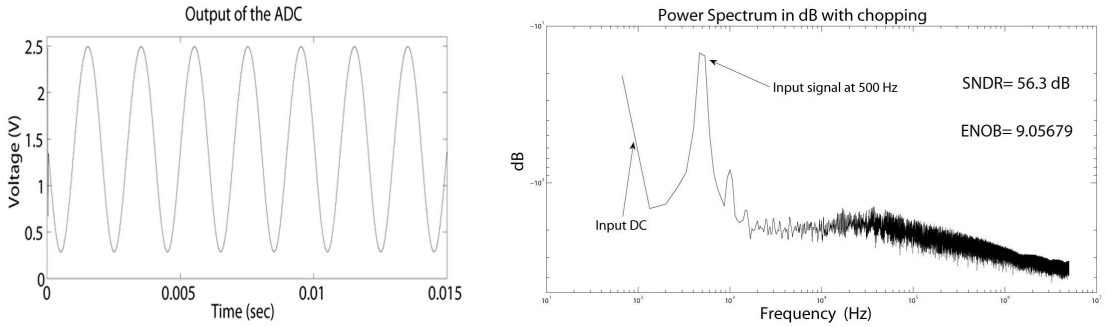


Figure 6.9: Initial characterisation of an analog to digital converter is done using a digital to analog converter at the output for “back-to-back“ testing



a) b)

Figure 6.10: a) Response of the ADC to a sinusoidal input having a frequency of 500 Hz. b) Power spectrum of the output of the ADC. The ADC has a Signal to Noise Ratio (SNR) of 56.3 dB and Effective Number of Bits (ENOB) equal to 9.05

Chapter 7

Low Power Neural Amplifier

One of the primary goals of neuroscience is to extract and process meaningful signal from the central nervous system [55]. This has created a demand for designing of low power neural interface circuits capable of monitoring the activity of neurons. Action potentials typically have an amplitude of 500 μV and have a frequency between 100 Hz to 7 KHz where as a local field potential has an amplitude of 5 mV and a frequency below 1 Hz [56].

Neural recording systems in the modern age require carefully designed electronics that allow transcutaneous, bi-directional data transfer. The general idea is to capture the brain signals via an electronic circuit that comprises of an electrode, an operational amplifier, and transmit these signals to a receiver circuit that also has an amplifier. Several integrated system have been designed to extract these signals [56][57][58].

7.1 Design of low power neural amplifier

Amplifiers used for neural recordings should have low noise, since the signals are weak, and low power dissipation so that the surrounding tissues are not damaged [56]. If the heat flux increases above 80 mW/cm^2 it will cause necrosis of the surrounding tissue [59]. Thus the electronics systems designed to perform neural recording should have power dissipation in the μW scale. Keeping these constraints in mind an OTA having a power supply of 1.8 volts was designed, shown in the Figure 7.1. This OTA is used as a part of the Neural amplifier shown in the Figure 7.2a. The layout of the neural amplifier is shown in the Figure 7.2b. There is a DC offset while recording the neural signals due to electrochemical effects at the electrode-tissue interface [60]. This will saturate the output of the neural amplifier and hence input capacitor is used to remove the DC offset. The midband gain is given by the ratio of input capacitor and feedback capacitor (C_{in}/C_{fb}).

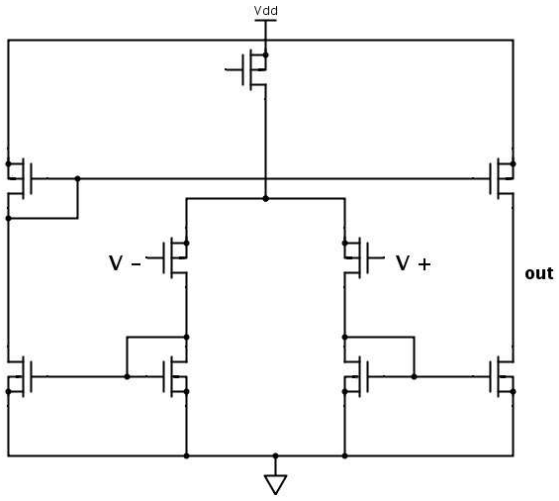
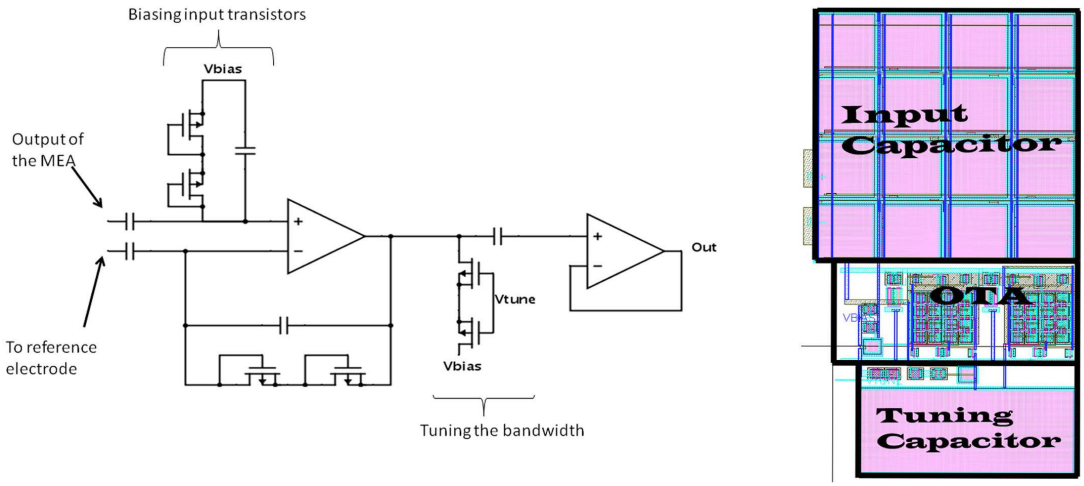


Figure 7.1: Schematic of the operational transconductance amplifier used as a part of the neural amplifier.

Table 7.1: Neural amplifier specification

Specification	Value
Gain of neural amplifier	33 dB
Bandwidth	692.7 mHz - 114 KHz
Power	13.13 μW
Input referred noise	2.38 $\mu V/Hz^{1/2}$
PSRR	46 dB
CMRR	50 dB
Power supply	1.8 volts
Area	$166\mu m * 300\mu m$

The AC gain of the neural amplifier is shown in the Figure 7.3a also shown is the input referred noise of the amplifier. A transient measurement was performed on the neural amplifier chip which is shown in the Figure 7.3b. Table 7.1 shows the specification of the neural amplifier and the OTA used. Due to the large input capacitors used the area of the neural amplifier is $166\mu m * 300\mu m$.



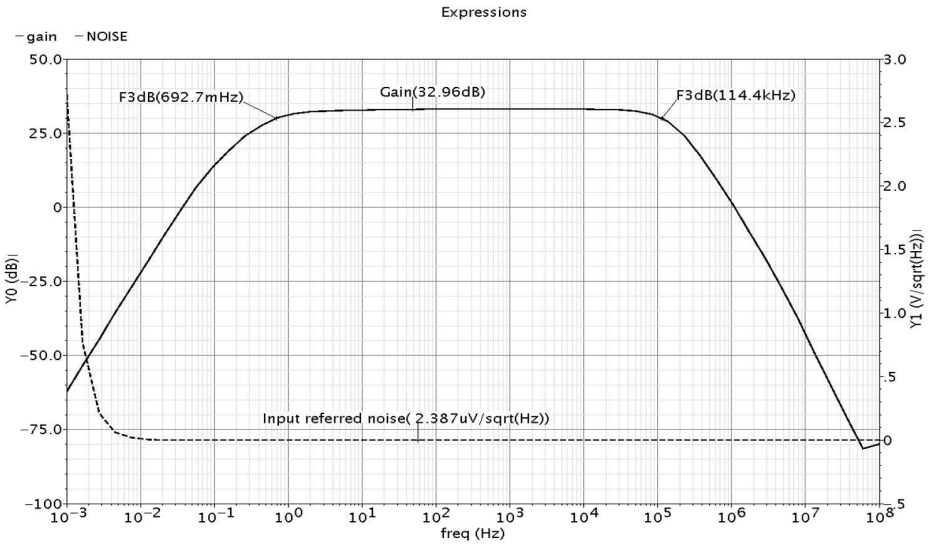
Schematic of a neural amplifer Layout

Figure 7.2: a) Schematic of the neural amplifier employing the OTA shown in the figure 7.1. It has tuning filter at the output of the first stage which allows us to tune the bandwidth. Input capacitor are used to remove the DC offsets. b) Layout of the neural amplifier having input capacitor layed in a common centroid fashion. The area of the neural amplifier is $166\mu m * 300\mu m$.

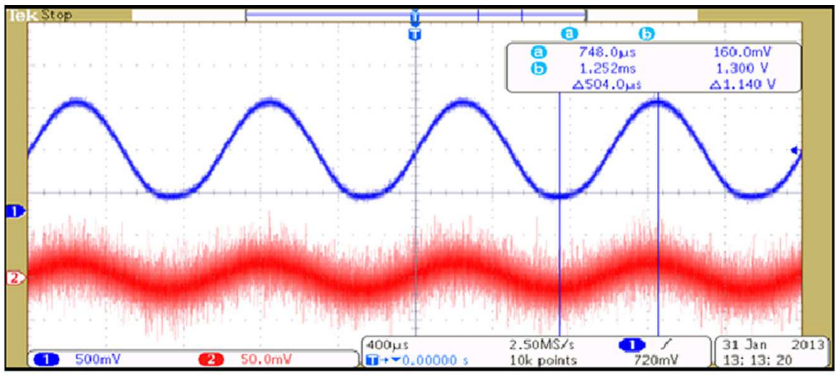
7.2 Multi channel neural amplifier

The neural amplifier designed in chapter 7 can be used to measure the action potentials of a neuron. A chip having multiple neural amplifier to read the output of micro electrode array was designed as shown in the figure 7.4.

Eventually an array of neural amplifier, like the one shown in the figure 7.4, would be used along with the optogenetics technology developed at ASU. Optogenetics is a technology that allows targeted, fast control of precisely defined events in biological systems as complex as freely moving mammals [61]. The technology has potential to treat and diagnose numerous neurological/physiological diseases and disorders [62].



a)



b)

Figure 7.3: a) The AC gain of the neural amplifier is 33 dB and has an input referred noise of 2.38 $\mu V/Hz^{1/2}$ b) Transient measurement performed on a neural amplifier designed in a 0.5 μm process.

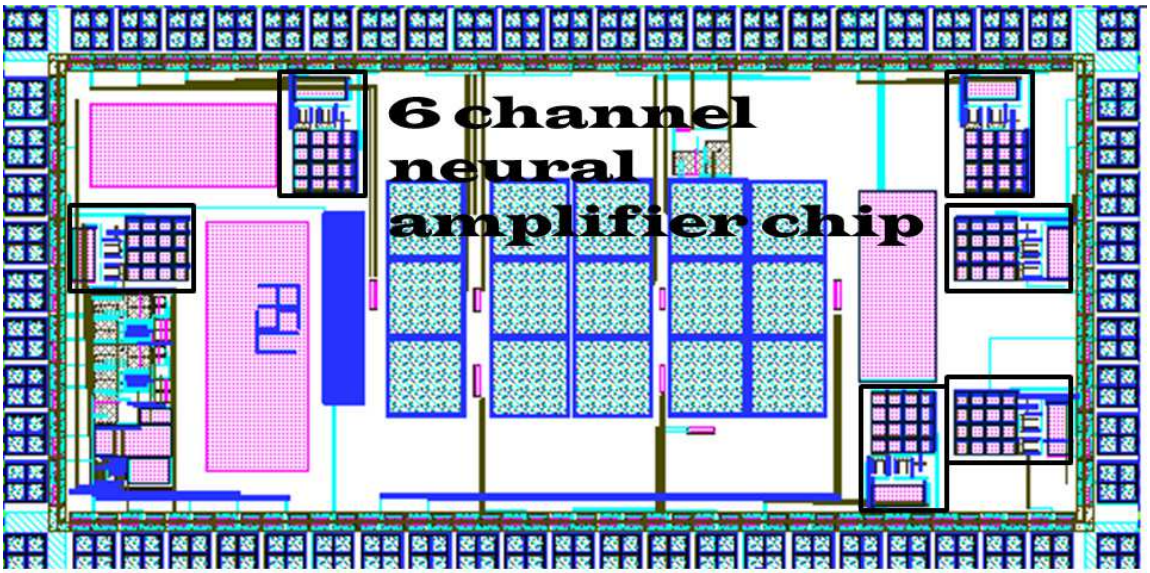


Figure 7.4: Array of neural amplifier layed in 0.5 μm are highlighted the figure. Multiple amplifiers allow us to read the output of micro electrode array.

Chapter 8

Discussion

The readout circuit designed in this work is discrete as shown in the Figure 8.1. The readout system consisting of the transimpedance amplifier and the dual slope analog to digital converter is layed separately to characterize them individually. Also having individual components of the readout separately layed out and not as a system allowed us to use the readout circuits with ISFETs designed with different fabrication processes(SensoNor, ISFET on PEN and ISFET on conventional CMOS process).

8.1 Flexible ISFET

Future work would include integrating the readout system to process the output of multiple sensors. Potential applications of such a integrated system would be to monitor cell growth inside multiple microfluidic channels. An example of flex integrated with a microfluidic channel is shown in the figure 8.2. Figure 8.3a shows ISFETs on plastic sub-

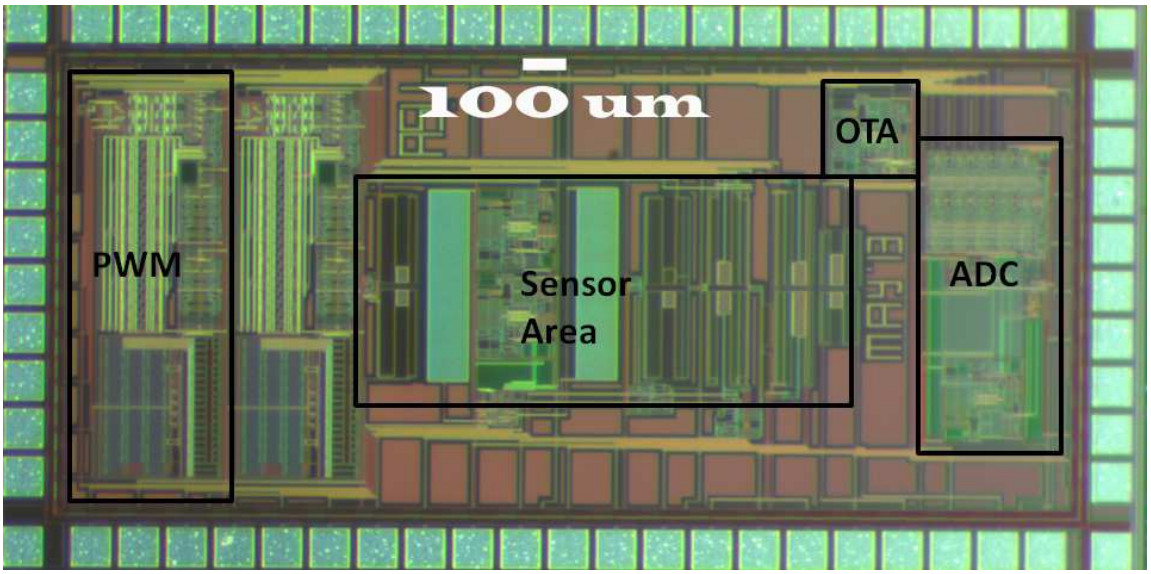


Figure 8.1: The figure shows the die area of all the circuits designed in this work. The circuits were designed in 0.5 μm process.

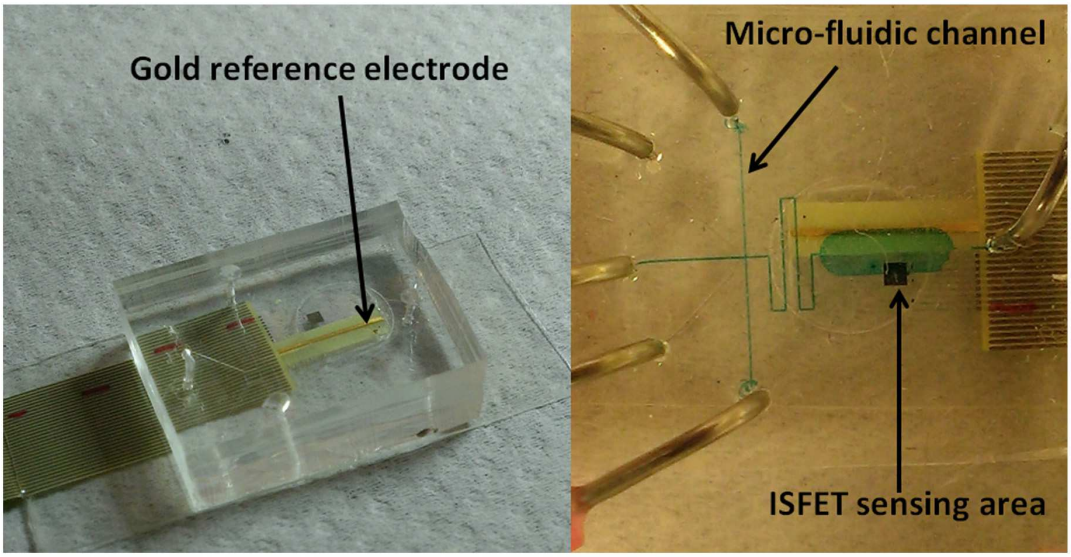


Figure 8.2: a)The figure shows cross-section of PolyDiMethylSiloxane (PDMS) layed on top of a flexible ISFET. b) The figure shows how a flexible ISFET could monitor the pH of the electrolyte inside the microfluidic channel.

strate monitoring pH of the electrolyte in two different chambers. Fluid flowing through the central chamber prevents the electrolyte from two chambers from diffusing into each other shown in Figure 8.3b. Monitoring pH in two different chamber allows us to perform experiments in controlled environment. Potential applications would include drug delivery [63][64][65], autonomous incubation of cell culture [66][67] and the detection of localized pH change to detect nucleic acid [68].

8.2 Flexible fringed capacitor

Capacitive sensing with the CMOS process has been used for antibody-antigen recognition, bacterial growth monitoring, DNA detection, toxic gas detection, and cell localization and monitoring [69]. In addition to this the system designed here could be used to detect changes in glucose [70][71]. The basic operation of all of the capacitance sensors

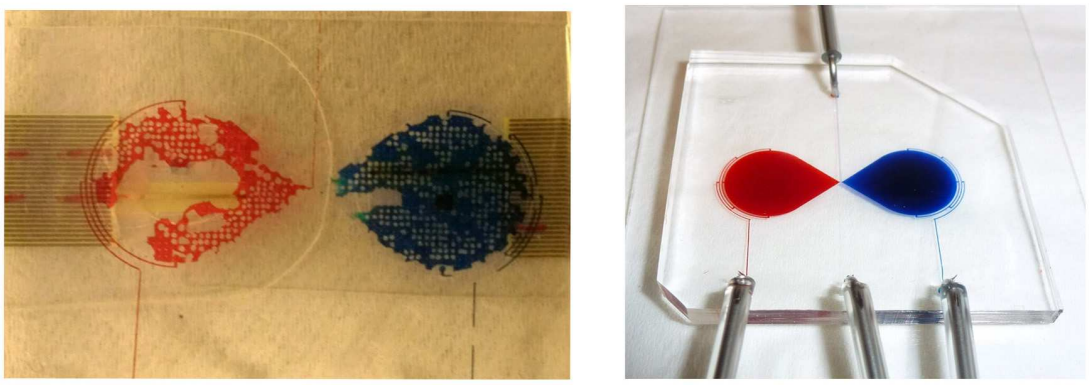
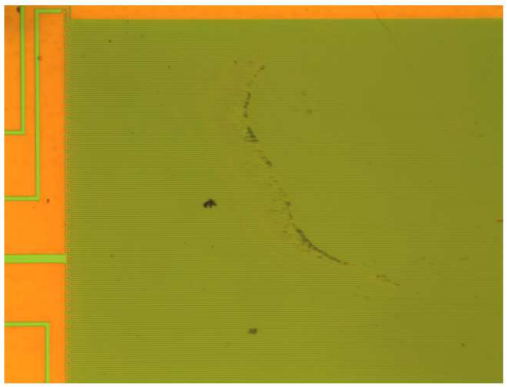


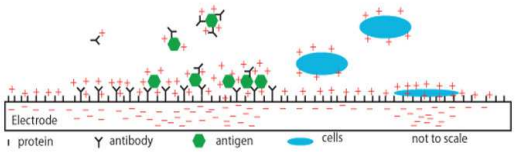
Figure 8.3: a) Two different ISFET can be used to monitor the pH in different chamber to perform controlled experiment. b)The figure shows how fluid flowing through the central channel which prevents diffusion between the chambers.

is similar: interdigitated electrode structures are manufactured using the top metal layer and the capacitance is measured between the two metal areas. The addition of positively charged biological particles (proteins, antibodies, cells etc.) between the sensing structures changes the capacitance that is measured by both effectively changing the distance term (d) in the standard capacitance equation $C = \frac{\varepsilon_R \varepsilon_0 A}{d}$ and the relative permittivity (ε_R).

The biological particles and agents that are potential targets for capacitive sensing vary in size and charge making a universal system with a variable range desirable. The system presented here would be suitable for sensing changes down to the femtofarad range as was seen in some permittivity sensing [73] and sensing cell attachment [74] up to the nanofarad range as seen with cell proliferation measurements [75].

Since the changes in capacitance is small a switch capacitor as shown in the Figure 8.5 was designed in a 0.5 μm process. The layout of the designed circuit is shown in the Figure 8.6. The switch capacitor circuit is designed to perform bottom gate sampling and to reduce the effects of parasitics. The parasitics capacitance is large for this





a) b)

Figure 8.4: a) Interdigitate capacitor on flexible substrate b) Interdigitated capacitive structures can be used to detect the presence of biological materials from protein or antibodies to cells. This is due to the change in fringed capacitance [72].

particular application of switch capacitor circuit since the C_{sense} and $C_{reference}$ are external interdigitated capacitor on flex.

The switch capacitor circuit accumulates charges on the feedback capacitor, which is larger compared to the input capacitor, depending on the changes in capacitance of the sense capacitor (C_{sense}) compared to reference capacitor (C_{ref}). The transfer function of the schematic shown in the figure 8.5 can be derived by conservation of charge.

$$\Delta q_{reference} = C_{reference}[V_{ref} - V_{ref}] - C_{reference}[V_{dd} - V_{ref}]z^{-\frac{1}{2}} = -C_{reference}[\frac{V_{dd}}{2}]z^{-\frac{1}{2}} \tag{8.1}$$

$$\Delta q_{sense} = C_{sense}[V_{ref} - V_{ref}] - C_{sense}[V_{ss} - V_{ref}]z^{-\frac{1}{2}} = C_{sense}[\frac{V_{dd}}{2}]z^{-\frac{1}{2}} \tag{8.2}$$

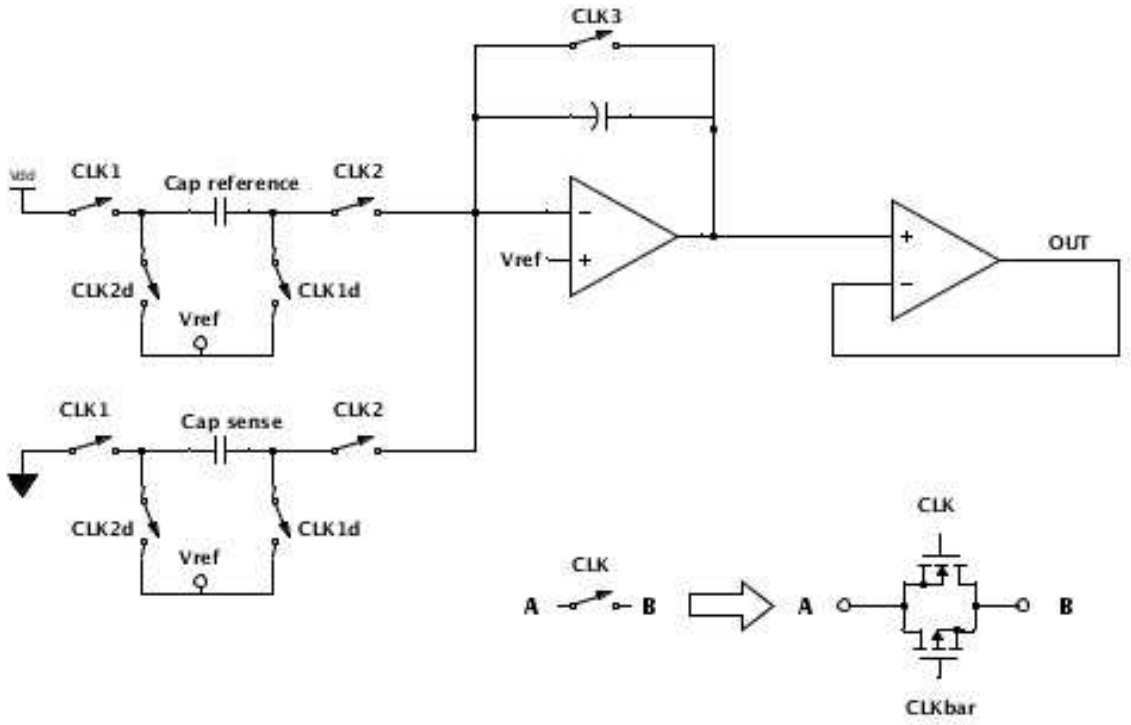


Figure 8.5: Switch capacitor circuit designed in a 0.5 μm process. The two input capacitor would be the interdigitated capacitor fabricated on PEN as shown in the figure 8.4a. The feedback capacitor act as a reservoir of charge and is designed on the integrated chip. The switches are pass transistor gates as shown in the figure. The OTA used is the one discussed in the chapter 5.

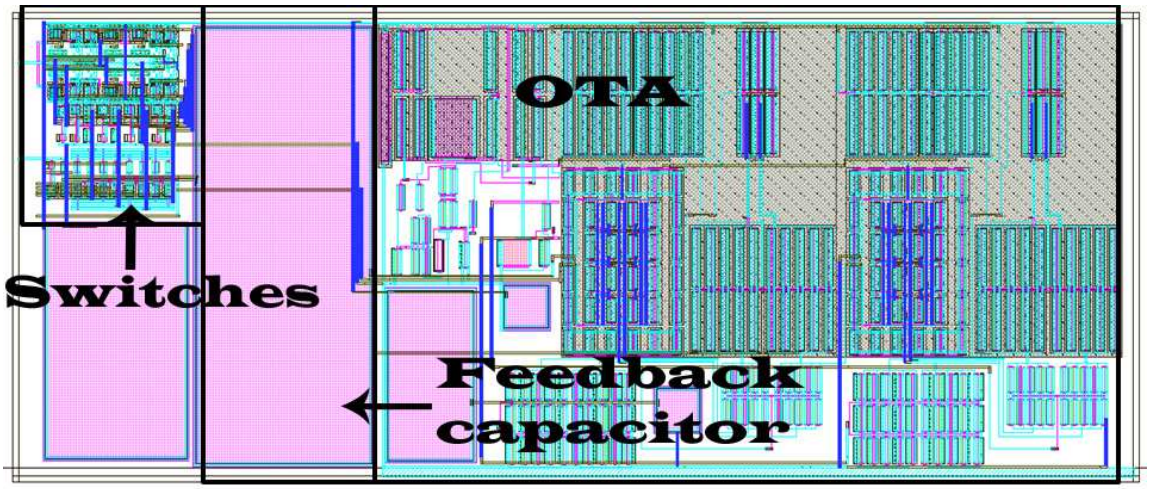


Figure 8.6: The layout of the switch capacitor circuit. The digital part is kept away from the analog OTA to reduce the noise from these components.

$$\Delta q_{feedback} = C_{feedback}[V_{out} - V_{ss}] - C_{feedback}[V_{out} - V_{ss}]z^{-1} = C_{feedback}[V_{out}][1 - z^{-1}] \tag{8.3}$$

From conservation of charges we have

$$\Delta q_{feedback} + \Delta q_{sense} + \Delta q_{reference} = 0 \tag{8.4}$$

Using equations 8.1, 8.2 and 8.3 in the equation8.4 we have the following transfer function for the output of the switch capacitor circuit:

$$V_{out} = -\frac{C_{sense}}{C_{feedback}} \frac{z^{-\frac{1}{2}} V_{dd}}{2[1 - z^{-1}]} + \frac{C_{reference}}{C_{feedback}} \frac{z^{-\frac{1}{2}} V_{dd}}{2[1 - z^{-1}]} \tag{8.5}$$

A simulation of the circuit was performed to understand the operation of the circuit as shown in the Figure 8.7. Clock 1 and Clock 2 are used during the normal operation of the circuit where the charge is accumulated on the feedback capacitor. The period of clock 1 and clock 2 is 500 ns. Clock 3 is a reset pulse to discharge the feedback capacitor. Different sizes for sense capacitor is used to simulate the change in fringe capacitance.

8.3 Conclusion

Biosensors have wide ranging applications in the field of biochemistry and medical diagnosis. Since their introduction in 1954 there has been a substantial research and development in this field partly owing to the advances made in microelectronic industry. The focus of this work was to use CMOS to calibrate, process and develop techniques to analyse biological signals.

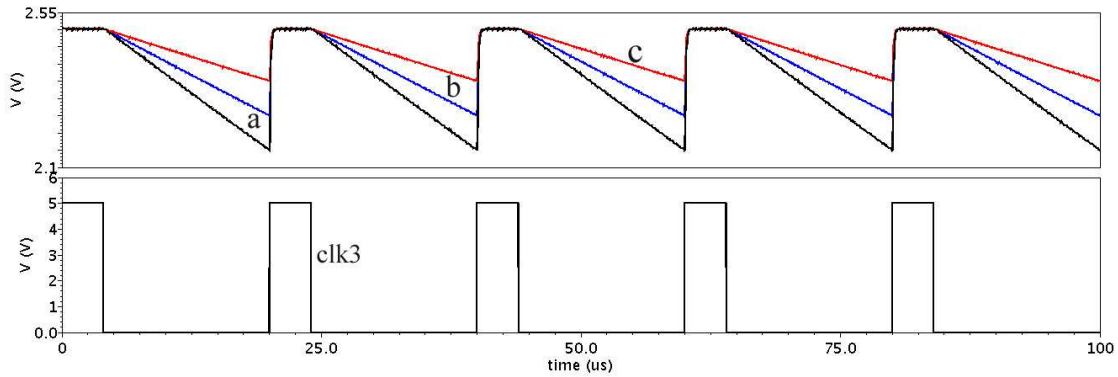


Figure 8.7: Simulation of the switch capacitor circuit shown in the figure 8.5. Simulation were performed with three different sizes of the capacitor C_{sense} while keeping the reference capacitor (C_{ref}) at 10 pF. The three different output waveforms shown in the figure correspond to the following capacitor (C_{sense}) sizes a)10.05 pF b) 10.03 pF c) 10.01 pF. Clock 3 is the reset pulse to discharge the feedback capacitor.

This work demonstrates the idea of drift management, allowing the device to drift in a normal but in a repeatable pattern. A TCAD model was created to investigate the drift mechanism in ISFET and develop potential methods to mitigate it.

The work also presents an array of ISFETs, designed in a conventional CMOS process, for long term continuous monitoring of pH. Vertical electric field of the ISFET is moodulated, by controlling the substrate potential, to mitigate the drift in the threshold voltage of the ISFET.

The mismatch between ISFETs, caused due to process variation and variation in post fabrications steps, could lead to measurement errors when employing multiple sensors. This work presents a floating gate ISFET to accurately program and calibrate these devices.

This work also demonstrates the use of biosensors, specifically an ion sensitive field effect transistors, as an alternative to conventional cell viability platforms to test the sensitivity of drugs. Initial measurements for the response of human mammary adenocar-

cinoma cells to staurosporine, a potential breast cancer therapy drug, was provided with an eventual goal of designing a point-of-care device for targeted drug therapy.

Further this work investigates and designs a read out circuit to employ the signal processing capability offered by CMOS technology. A transimpedance amplifier and a dual slope analog to digital converter was designed in a 0.5 μm process to read the output of the pH sensors.

The work also employs CMOS circuits to interface with other biosensing platforms such as fringed capacitance to detect biological events or cell viability and micro electrode array to measure signals from the neurons. In a step towards this a low power neural amplifier was designed to measure low bandwidth action potentials. Also a switch capacitor circuit was fabricated in 0.5 μm process to sense small changes in capacitance of a interdigitated capacitor in turn detecting biological events such as antibody-antigen docking or monitoring cell growth.

This work also investigates alternate processes for analysing biochemical events. A thin film transistor based flexible ion sensitive field effect transistor and a interdigitated capacitor on a flexible substrate was presented. Though the processing capabilities of CMOS circuits make it indispensable the flexible technology has an advantage in that it allows a larger and cheaper sensing area. Thus making it attractive to develop a process which integrates CMOS on PEN, capitalizing on the best of both the technologies.

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