A Radiation Hardened Pulse based D Flip-Flop

by

Sushil Kumar

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Graduate Supervisory Committee:

Lawrence Clark, Chair
Bertan Bakkaloglu
Umit Ogras

ARIZONA STATE UNIVERSITY

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ABSTRACT

The D flip flop acts as a sequencing element while designing any pipelined system. Radiation Hardening by Design (RHBD) allows hardened circuits to be fabricated on commercially available CMOS manufacturing process. Recently, single event transients (SET's) have become as important as single event upset (SEU) in radiation hardened high speed digital designs.

A novel temporal pulse based RHBD flip-flop design is presented. Temporally delayed pulses produced by a radiation hardened pulse generator design samples the data in three redundant pulse latches. The proposed RHBD flip-flop has been statistically designed and fabricated on 90 nm TSMC LP process. Detailed simulations of the flip-flop operation in both normal and radiation environments are presented. Spatial separation of critical nodes for the physical design of the flip-flop is carried out for mitigating multi-node charge collection upsets. The proposed flip-flop is also used in commercial CAD flows for high performance chip designs. The proposed flip-flop is used in the design and auto-place-route (APR) of an advanced encryption system and the metrics analyzed.

ACKNOWLEDGMENTS

I would like to thank my family for supporting me and my educational career. I would also like to thank Prof. Lawrence Clark for giving me this opportunity to work various wonderful projects and for being source of inspiration throughout my masters. It had been by dream to work on complete RTL to GDS flow of ASIC design. I would also like to thank Dr. Bertan Bakkaloglu and Dr. Umit Ogras for taking time to serve as panel members on my defense committee.

I leave the research group with fond memories of working with my colleagues. My sincere thanks to Sri, Chandru, Vinay, and Sandeep for all the technical discussions and debates we had in the lab.

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Chapter 1 INTRODUCTION

The flip flop (FF) is the most widely used sequential element in digital CMOS VLSI design. Flip-flops serve both as memory elements and as a synchronization element to enforce sequence, i.e., to distinguish the current data from the previous data or next data. Therefore, we can also refer to them as sequencing elements [1]. Sequencing elements delay data that arrives too early, preventing it from catching up with previous data. As the speed of the chip increases with every generation, more pipeline stages are being added to increase the pipeline depth, which allows greater frequency operation.

This chapter discusses an overview of latches and FFs, along with radiation effects in space environment. Focus is given particularly to single event effects and single event mitigation (SEEs) in detail.

1.1. Latches

Latches are the basic building blocks for FFs. Latches are controlled by a clock signal and can operate in one of two states, either transparent or opaque, at a given time. When a latch is transparent, it lets data pass from input to output, analogous to a traffic light signal, where the car is allowed to pass through for a green light. Contrarily, when a latch is in the opaque state (i.e., a red light) it doesn't allow data to pass from input to output. The data has to wait for the latch to transition to the transparent state to pass the value. Contrary to flip-flops, which sample data at a clock edge or transition, latches are designed to be transparent on one of the clock phases, either low or high, called

transparent low and transparent high latches respectively. The waveforms for a FF and a latch, which is transparent for logic high, have been compared in Fig 1.1.

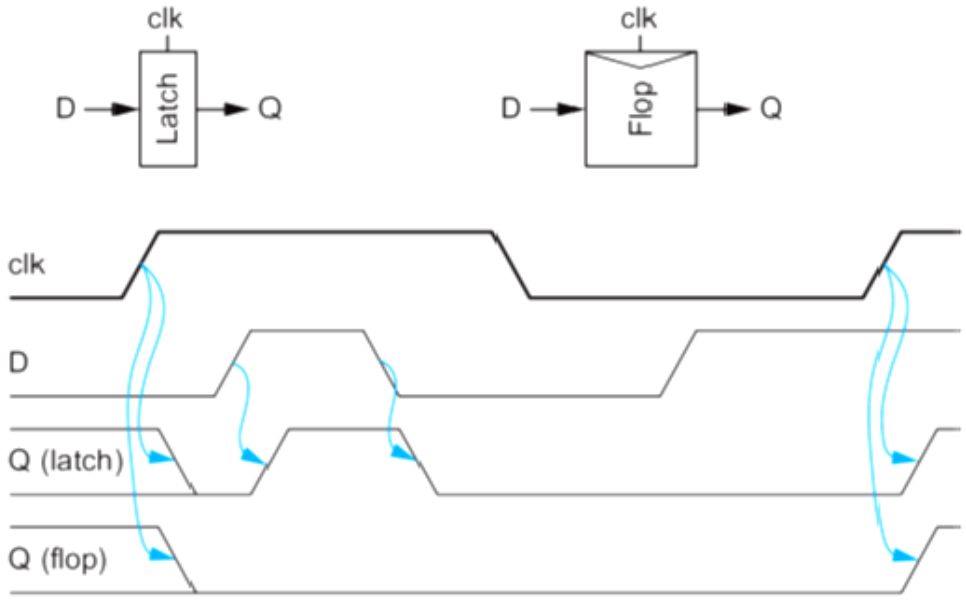


Fig. 1.1. Basic timing of latches and flip-flops (After [Weste-05]).

The latch has two input signals, clock (clk) and data (D), and one output (Q).At the high phase of the clock, data propagates to the output Q after a certain delay known as $t_{D\text{-}Q}$ .The delay from the clock edge to the output is $t_{clk\text{-}Q.}$ The delay of the latch depends upon both the process technology and the circuit topology.

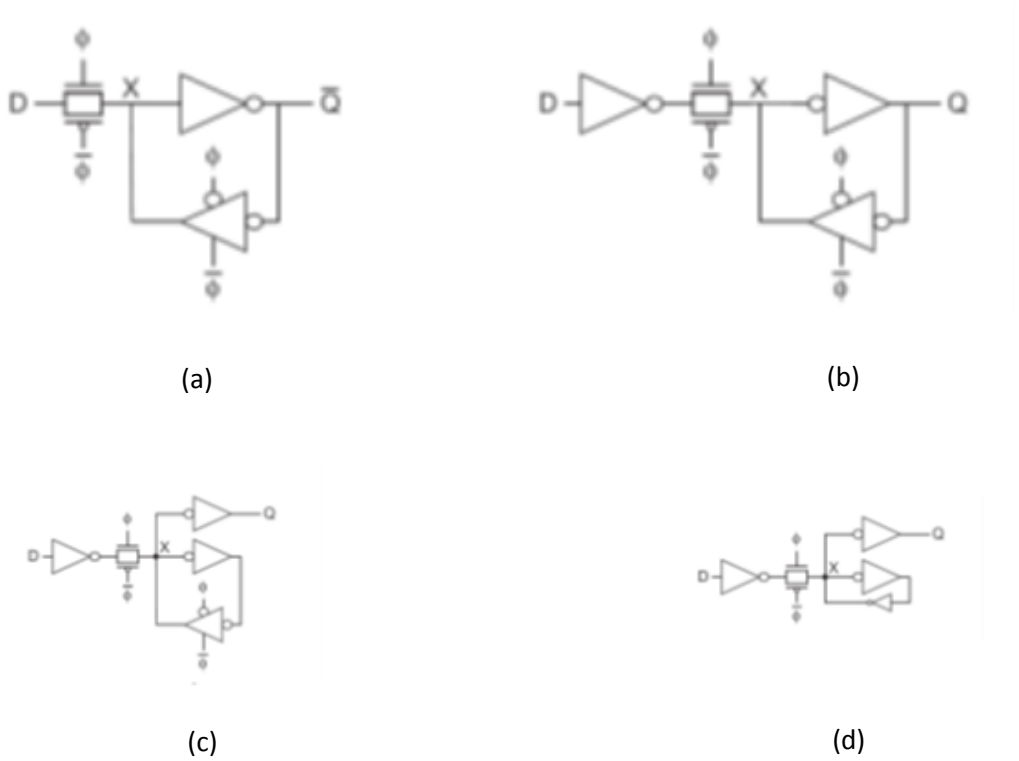


Fig. 1.2. Various styles of latches (After [Weste-05]).

Fig.1.2(a-b) shows various latch designs, which include tri-state inverters in their feedback. One drawback of these latches is that the storage nodes (which are the same as the output nodes) are being exposed to external circuitry. Such designs are generally avoided as any noise on the storage node can upset the data stored in the latch.Fig.1.2(c) shows the most commonly used latch in a real design and can be found in commercial foundry libraries. The latch contains tri-state inverters in the feed-forward and feedback paths. The output node and storage node are distinct and separated by a buffer making the design much more noise immune. Fig.1.2 (d). shows another variation of the same latch. This latch lacks a tri-state inverter in its feedback loop. Instead, a weak feedback inverter

in used to latch the data. Such designs are called jam latches because as they rely on ratioed gates for successful operation. Clock loading is reduced due to the absence of tri-state inverter from the feedback loop. However, greater current is required to overcome the feedback path and these are potentially problem at various process, voltage and temperature (PVT) corners. All three latches mentioned above have inverter at D input for decoupling storage and input nodes.

1.2. The D Flip- flop

FF's like latches are also sequencing elements. However, unlike latches they operate at the rising or falling edge of the clock and not in either clock phase. FFslatch the input state to output state triggered by the rising or falling edge of the clock. A generic FF is made of two back-to-back latches one called the master latch and the other called the slave latch. For a positive edge triggered flip-flop a negative latch (transparent during clock low) is followed by positive latch (transparent during clock high). Fig. 1.3 show a basic static cmos flip-flop circuit.

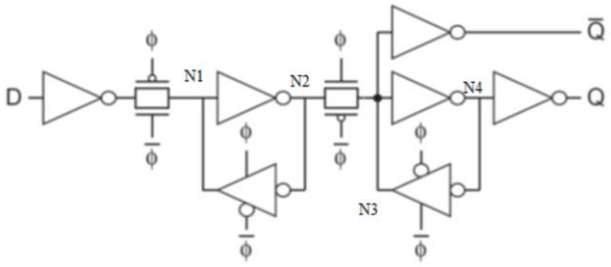


Fig. 1.3. Schematic for D flip-flop (After [Weste-05]).

The FF is a standard component of most design libraries. It has the advantage of having a tri-state feedback which ensures no contention during the sampling edge. However, one of the disadvantages, more clock loading presented to the driving circuit. In case of multiple flip-flops being driven by the same clock, network clock drivers are added for clock distribution. The flip-flop is never transparent from D to Q because the pass gates of the master and slave stages are enabled bycomplimentary clock signals. When master is transparent, slave is opaque and vice-versa. This makes sure thatdata is stored at the output for one cycle. For a positive edge triggered flip-flop, before the rising phase of the clock, correct data must be available at node N2 of the master latch (shown in Fig. 1.3), also called the setup node of the flip flop. Similarly after the rising edge,data must be held for a minimium time for reliable data latching. New data should notpropogate to node N1 (also called the hold node of the FF) during the closing phase of the master latch. The slave latch is transparentat the positive phase of the clock and the desired logic state propogates to output pin Q. Node N3 and N4 are referred to as slave-hold and slave-setup nodes respectively. Slageve setup node is important as after setting the value at this node clock phase can be changed. Slave hold node should not update any new value while closing the slave latch from D input. The time it takes to latch the new value from clock rising edge is referred to as t_{clk-Q}(shown in Fig. 1.1).

While designing a synchronous system with FFs, sequencing elements introduce a dead time period in which no useful logic is computedand theflip-flop is busy with its operation,which is given by the expression,

$$t_{dead} = t_{clk-Q} + t_{setup}. \quad (1.1)$$

where $t_{clk-Q}$is the delay from clock rising edge to ouput pin and $t_{setup}$is referred to as setup time of the FF. Since the dead time of the FF is not useful time, in pipelined design t_{clk-Q} and t_{setup}must be minimized to achieve better performance.

The t_{setup} is defined as the minimium time before clock rising edge for which data should be held constant. So before rising edge it should be ensured that the data propagates Node N2 (shown in Fig 1.3), else, either the data will not get latched to output or t_{clk-Q} will be longer than usual which would trigger system error.

The FF hold time is the minimium time afterclock rising edge for which data should be constant. During the rising edge of flip-flop, new data should not race into the latch to corrupt data at node N1. Fig. 1.4 shows the pictorial representation of setup and hold time.

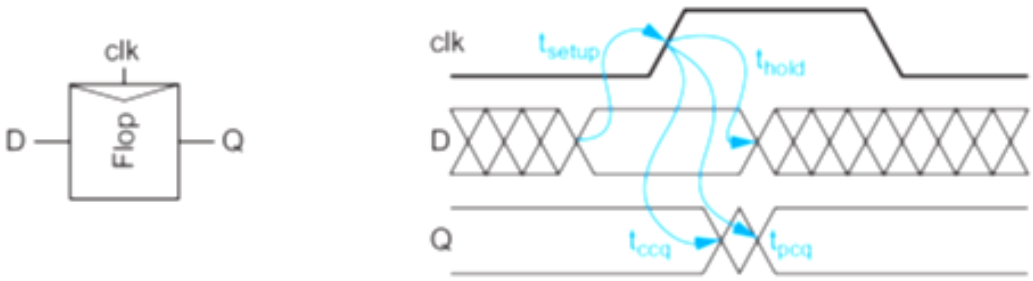


Fig. 1.4. Setup and hold timing diagrams (After [Weste-05]).

The above figure shows two delays for the t_{clk-Q} one is t_{CCQ} which is contaminational t_{clk-Q} referred as minimum $t_{clk-Q.}$ The t_{pcq}which is the propagation t_{clk-Q} or maximium $t_{clk-Q.}$ This happen due to complementary clock signals being fed to pass

transistors of transmission gate. Delay of one inversion causes one value to propagate later than other.

The measurement of setup and hold time can be simulated by moving the data transition point closer to the rising edge of the clockwhile measuring the $t_{clk\text{-}Q}$. Fig. 1.5 showssample setup and hold analysis results on a (clock to qdelay) t_{cq} vs (data to clock delay)$t_{D\text{-}clk.}$

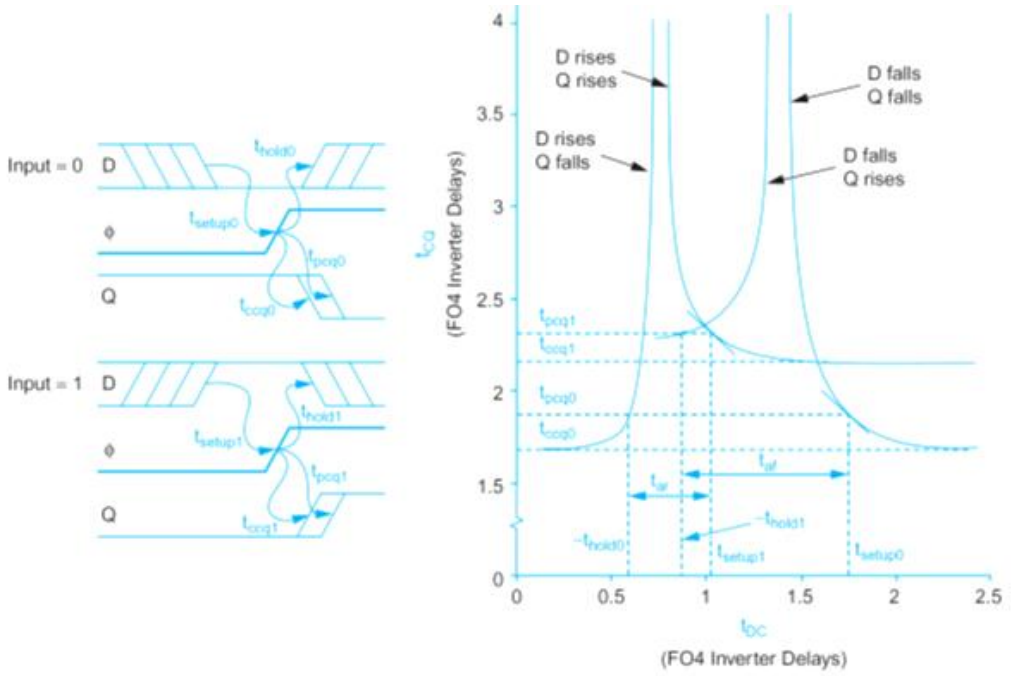


Fig. 1.5. Flip-flop setup and hold time calculation (After [Weste-05]).

It shows that the simulated value of t_{CQ} delay was obtained for four different combinations (D&Q / falling &rising).The setup times $t_{setup0}$and $t_{setup1}$are the setup times for D to transition before the clock, so that data is captured with the -1 slope of t_{CQ} . Hold times t_{hold0} and t_{hold1} are the times for which the data D must be held after the clock edge

so that the actual value to be captured is not corrupted by the next state transition. The aperture width t_a is the width of the window around the clock edge during which data must not transition for the FF to operate with a proapagation delay less than t_{pcq}. The aperture times for rising and falling inputs are

$$t_{ar} = t_{setup1} + t_{hold0} , \qquad (1.2)$$

$$t_{af} = t_{setup10} + t_{hold1} .$$

Fig. 1.5 shows that as time between t_{DC} decreases, the t_{CQ} delay increases exponentially. This is caused by data arriving too close to the clock edge with the FF not having enough time to resolve the output. Any violation of setup and hold may cause a timing violation. In order to mimimize dead time, the point where the slope of the curve equals-1is chosen as t_{setup} of the FF as it gives the minimium combination of $t_{setup} + t_{CQ}$. As discussed earlier, we have differnt delays for setup time, hold time time for different data and clock transitions.

During the system level timing analysis, setup and and hold time violations are referredto as max-delay and min-delay violations, respectively. Fig.1.6 shows two flip-flops in a pipelined dessign with a combinational delay in between.

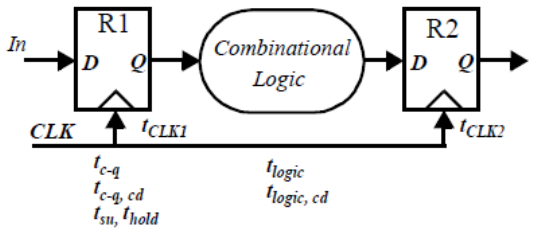


Fig. 1.6. A pipelining circuit.

The maximum operating time period of the circuit is given by

$$T_{cycle} >= T_{c\text{-}q} + t_{logic} + t_{su}. \quad (1.3)$$

The above expression determines the highest frequency of the machine. A max-delay violation occurs when data from the previous flip-flop doesn't propagate through the combinational logic to the next FF in time to meet the its setup time. As this violation is due to the propagation delay through the logic elementsbetween the FFs, it is a frequency dependent problem and can be addressed by lowering the frequency. A min-delay violation occurs when the data from the previous FF races through the shortes combinational logic path and violates the hold time

$$T_{hold} >= T_{c\text{-}q,cd} + t_{logic,cd}. (1.4)$$

Hold time errors are not frequency dependent and thus fixing these of utmost importance when designing the chip. The hold time violation can be solved by adding delays between the stages of the flip flop and must be done during the design phase of the chip.

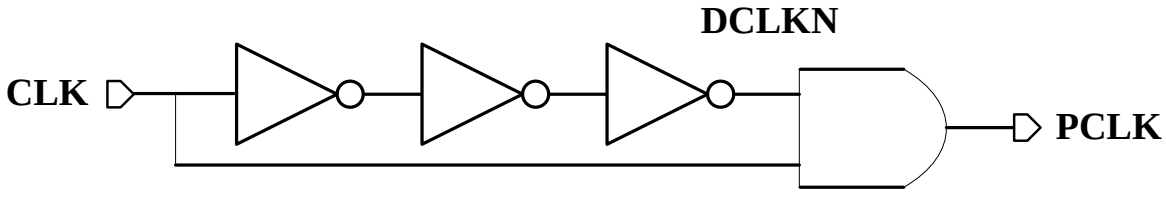
1.3. Principle of pulse clock based flip-flops

The conventional FF has two latches, a master followed by a slave latch stage in the master-slave configuration which increases the overall circuit area. A pulse-clocked FF consists of a single latch that samples the data at the positive phase of a pulse

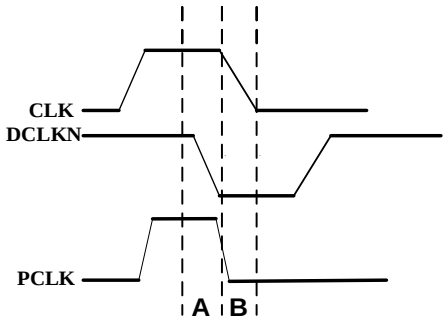
generated by a pulse generator. The data is held constant during the entire duration of the pulse and the width of the pulse is made large enough to latch the data successfully.

The output of the pulse generator isa clock pulse which is derived from global clock. Ideally the pulse generator is shared across multiple such pulse clock latches for area and power efficiency. Since the number of clocked transistors are reduced, this configuration results in reduced power consumption [18].

A major disadvantage of the pulse based FF is that during the positive phase of the pulse the flip-flop is transparent. This would result in any changes to the data being propagated to the output. Thus the data has to be held constant during the entire pulse duration. Timing parameters of pulse-clocked based latches (t_{setup}, t_{hold} $t_{clk\text{-}Q}$) is measured to the closing edge, i.e., the pulse end. Since, timing of any latch depends upon latching the value to the setup node before closing the latch. We can model a pulse-clocked latch as a FF triggered on the rising edge of the pulse, with a positive setup and lengthy hold time. This model makes the pulse based FFs relatively easy to integrate into CAD flows. Fig. 1.7(a) and (b) show a simple pulse generator and timing diagram for the pulse generator.



(a)



(b)

Fig. 1.7. Schematic representation and waveforms of pulse generator.

The window A shown in Fig. 1.7(b) shows the positive setup time. Hold time is represented by window B. The setup and hold timings are measured from closing edge of pulse as reference.

1.4. Space Radiation

Radiation is the emission of energy as electromagnetic waves or as moving subatomic particles, especially high-energy particles that cause ionization [2]. When an energized particle strikes integrated circuits, any interaction between the circuitry and the impinging particle is referred to as a single event effect (SEE). SEEs are troublesome for aerospace applications[19].A single event transients (SET) is defined as a momentary voltage excursion (voltage spike) at a node in an integrated circuit. The voltage spike is originally formed by the electric-field separation of the charge generated by an ion passing through or near a circuit junction. Under certain conditions, the voltage spike can propagate away from where it was generated and eventually appear at the circuit's output.

Radiation generated SET which upsets architectural state also known as single event upset(SEU) are the primary reasons for failure mechanism behind several spacecraft[3-6].

There are four major primary sources of SEE due to space radiation: plasma, trapped particles, solar particles, and cosmic rays [7]. The last three are known to cause SEE because they have higher energy content in comparison to the plasma. Another environmental factor is the geomagnetic field which strongly influences plasma or particle motions and locations [8]. The sun also has a major impact on plasma density, ionizing radiation levels and magnetic field characteristics. The sun goes through an eleven year cycle with four years of solar minimum followed by seven years of solar maximum. During the major solar event the helium ions may increase rapidly by three to four orders of magnitude than ordinary solar flares. Solar activity affects the level of electrons, protons, and cosmic rays. Their intensity at Solar min and max is tabulated below.

Table 1. Constituent particles during Solar flare min and max.

	Solar Min	Solar Max
Electron Intensities	lower	higher
Protons Intensities	higher	lower
Cosmic Ray Population	peak level	Low level

Solar flares are a major contributor to the overall radiation flux. A major solar flare can emit energetic protons that reach Earth within 30 minutes of the flare's peak. One to four days after a flare, a slower cloud of solar material and magnetic fields reach Earth, storming the magnetosphere and resulting in a geomagnetic storm. Geomagnetic

storms have been directly correlated to the incidence of spacecraft charging. Fig. 1.8 shows the geomagnetic field.

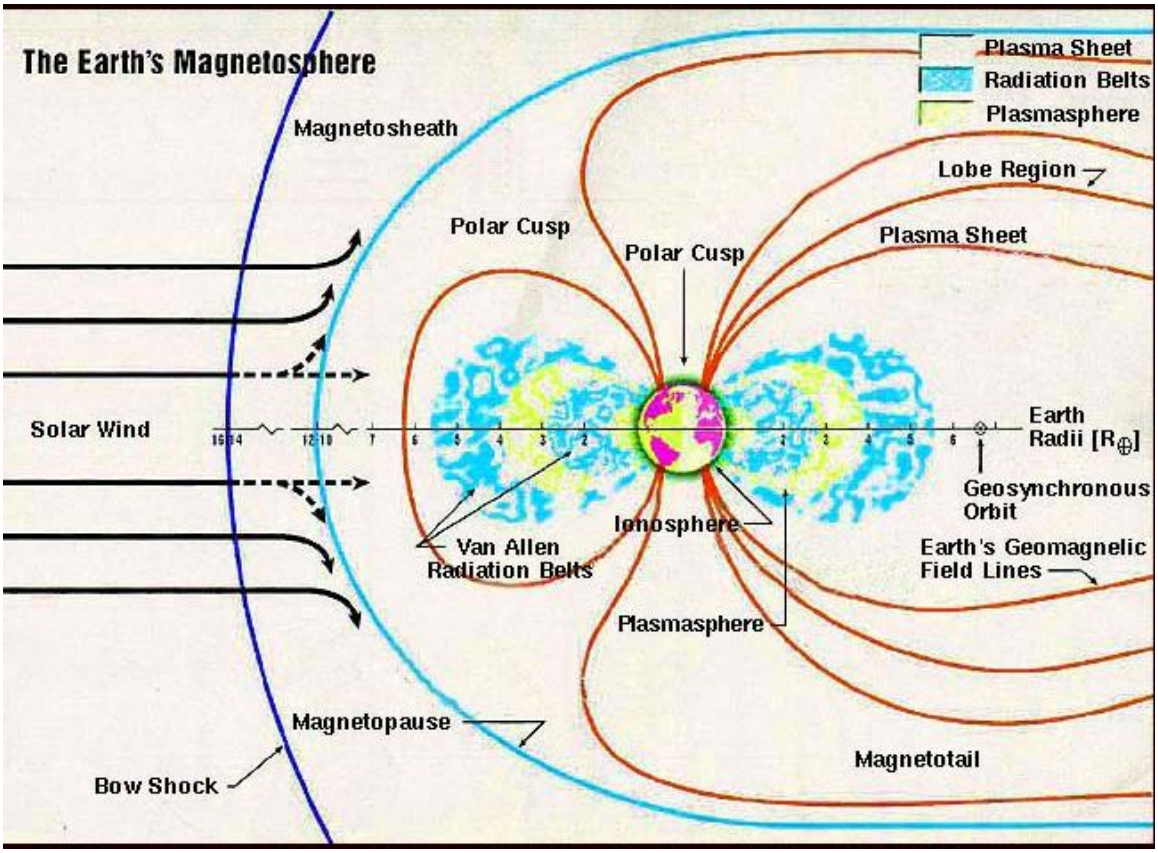


Fig. 1.8. Earth Magnetosphere (After [7])

Plasma consists of equal collection of positive ions and electrons with relatively low energy ranging from few eV to a few KeV. As a spacecraft traverses through space, it comes in contact with an unbalanced flux of electrons or ions which causes the spacecraft surface to collect the charge. This charge can affect the electrical system of the spacecraft. Most spacecraft systems are shielded to protect from the accumulated charge.

The Earth's magnetosphere is a dynamic environment because of its interaction with solar winds and the sun. It extends nearly 10 earth radii, but can very well change by a factor of two [9]. The magnetosphere traps the charge particles, mostly electrons and protons that contribute to the trapped radiation. The Van Allen belt consists of two zones where photons and electrons reside in the inner and outer belts respectively. In the inner belt, proton fluxes with energies less than 500 MeV dominate, while the outer belt consist of high flux electrons with energies about 7 MeV. The inner belt traps charged particles because of Earth magnetosphere. Particles originating from cosmic and solar sources are attenuated by the Earth's magnetosphere. The Earth's magnetic field provides natural shielding from both cosmic and solar particles depending primarily on the inclination and secondarily on the altitude. As inclination reaches auroral to polar regions, a satellite is outside the protection of the geomagnetic field lines. At polar orbits intense fluxes of energetic electrons, known as precipitating electrons, propagate down along magnetic field lines (and create the aurora). As altitude increases, the exposure to these particles gradually increases. During large solar events or magnetic storms, magnetic field lines are compressed allowing cosmic and solar particles to penetrate lower altitudes and inclinations. The galactic particle population peaks at solar minimum; whereas the solar particle levels peak at solar maximum.

The composition of galactic cosmic rays includes: 85% protons, 14% alpha particles, and 1% nuclides with Z>4, but heavy ions of Z>26 (iron) are rare. The cosmic rays include particles with energies from 0 to over 10 GeV. The bulk of these heavy ions are Hydrogen (proton), He (alpha), Carbon, and Oxygen with peak energies around 1 GeV.

The cosmic rays have a very low flux compared to trapped particles, but have much higher energy; hence, which is difficult to shield against. The table below summarizes the three main components of space radiation with the effect on CMOS devices.

Table 2. Summarizes the radiation sources and radiation effects on devices.

Radiation Source	**Particle type**	**Primary Effects in Devices**
Trapped radiation belts	Electrons	Ionization damage
	Protons	Ionization damage; SEE in sensitive devices
Galactic cosmic rays	High energy charge particles	Single-event effects
Solar flares	Electrons	Ionization damage
	Protons	Ionization damage; Single-event effects
	Lower energy heavy charged particles	Single-event effects

The next section discusses the impact of such radiation on integrated circuits.

1.5. Radiation Effects in devices and circuits

Radiation effects can lead to degradation, malfunction or even permanent damage in electronic circuits and devices [10].There are two main kinds of SEEs: Single event upset(SEU) and Single event transient (SET). In 1975, the two Engineers from Intel found concentrations of uranium and thorium in the packaging material emitting alpha

rays. These alpha particles induced soft errors (SEU) in a DRAM in a terrestrial environment.

Radiation interactions with the target material depends upon the material type, mass, atomic number, density of target material, kinetic energy, the charge state of the incoming particle etc. An ion travelling through a circuits loses kinetic energy primarily through columbic interactions with the silicon leaving a trail of charge in its path. The distance travelled by a particle in a silicon is proportional to the kinetic energy the particle has and the density of the material. The Linear Energy transfer (LET) depends upon the material through which it passes. The energy loss or LET is normalized by the density of the solid. The units of LET is MeV-cm^2 = (MeV/cm)/(mg/cm^3). The LET is a function of the ion's mass, energy and density of silicon, given by the expression

$$LET = \frac{1}{\rho}\frac{dE}{dx}(MeV - cm^2/mg), \qquad (1.5)$$

where dE/dx is the energy loss per unit length and ρ is the silicon density in mg-cm^3. The maximum LET value near the end of the particle's range is called Bragg peak [12].It is known that an electron-hole pair is produced by every 3.6eV energy equivalent particle and that the density of silicon is 2328mg/cm^3 , thus calculating using the formula above measures that LET of 97MeV-cm^2/mg corresponds to a charge deposition of 1pC/um . Hence the charge collected is usually formulated as,

$$Q = 0.01036\ LETpC/um. \qquad (1.6)$$

This implies charge collection is a function of silicon and does not depend on circuit scaling. As charged or ionizing particles hit silicon, the ions create a track of electron-hole pairs(shown in Fig. 1.9). A "funnel" structure is formed by the silicon which extends into the depletion region along the ion's path. The drift and diffusion current components will go to favorably biased diffusion node. These currents disrupt the charge in the junction and may change the state of the diffusion node and cause an ‘upset’. The upset current gradually dissipates as electrons and holes start recombining to remove the collected charge. The upset interval depends upon the incident angle from which it strikes the junction [13-14].

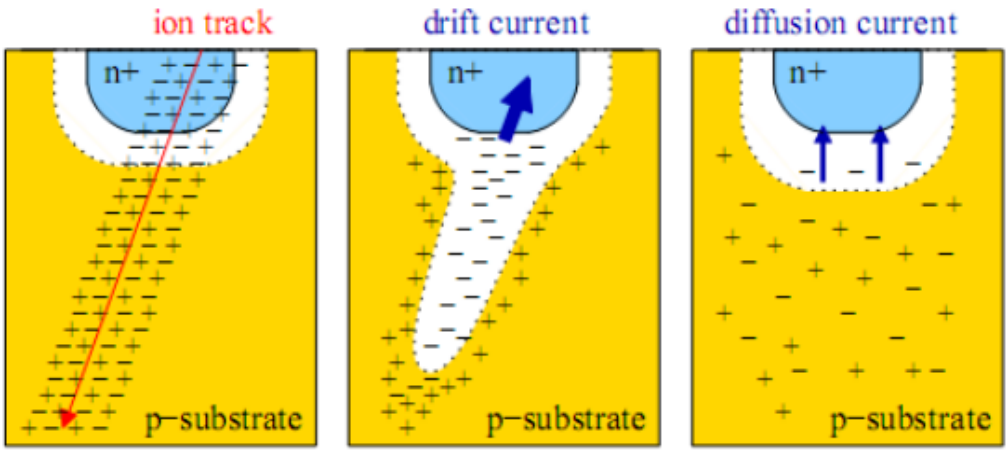


Fig. 1.9. Ion striking semiconductor junction (After [17]).

SETs are temporary glitches in combinational logic generated due to the charge collection by the ionization particle strikes. The width in ps of the glitch is dependent on charge collected by the silicon . It also depends on the capacitance and current drive of the node that is hit by the ion. As technology scales, current drive, V_{DD} and circuit node

capacitances also reduces . The charge deposited by the ion does not scale and remains constant which makes the combinational circuit more susceptible to an ion strike [15]. Depending upon the SET pulse width, the glitch may pass through many logic stages without dissipating. Fig. 1.10 below shows critical transient width vs. feature size. We can see that as the feature sizes decreases the critical transient width decreases exponentially. Only glitches with width greater than the critical transient width propagate as a regular signal in a chain of combinational gates [16].

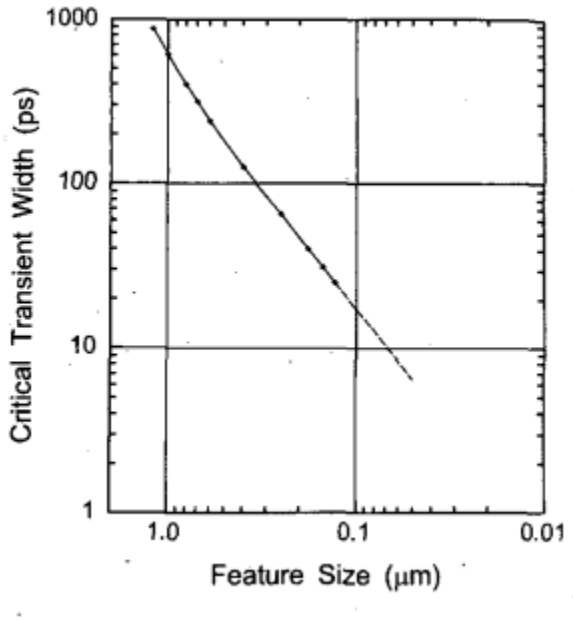


Fig. 1.10. Critical transient width required to make upset vs. feature size (After [16]).

SET glitches are temporary but when latched by a sequential element such as a flip-flop or latch, becomes a (SEU). Single event strikes at the latch or FF also contribute to SEU corrupting the machine state. SETs are frequency dependent, with more edges

available for sampling incorrect data as frequency increases. Fig. 1.11 shows the SET particle passing through a series of combinational gates.

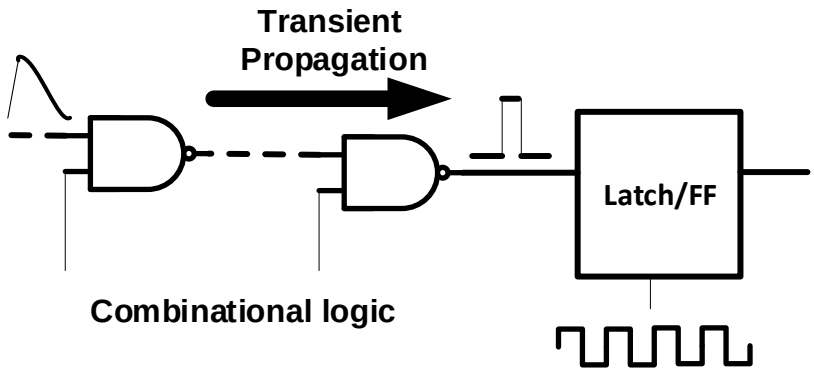


Fig. 1.11. SET hitting and propagating through combinational gates.

1.6. Multi bit upset (MBU)

Multi-bit upsets (MBU) are multiple upsets produced by a single impinging particle. MBU probability is strongly dependent on node spacing, feature size, and supply voltage. As feature sizes shrink, MBUs are becoming more of an issue. The Linear Energy Transfer (LET), range, track radius, and angle of incidence of the particle inducing upset are also important. In general, particles that deposit more energy, have a longer range, and have a larger radius are more likely to induce MBU. Since a single event induces an MBU, the MBU fail pattern is typically contiguous and follows a trajectory. In accelerated experiments, care must be taken when taking data to ensure that adjacent bit errors caused by separate events are not to be considered MBUs. Statistical methods on tested parts can be applied to sort out adjacent upsets that appear to be MBU

as well as fast bitmapping. Fig. 1.12 shows block representation of single bit upset and multi bit upset in a memory array.

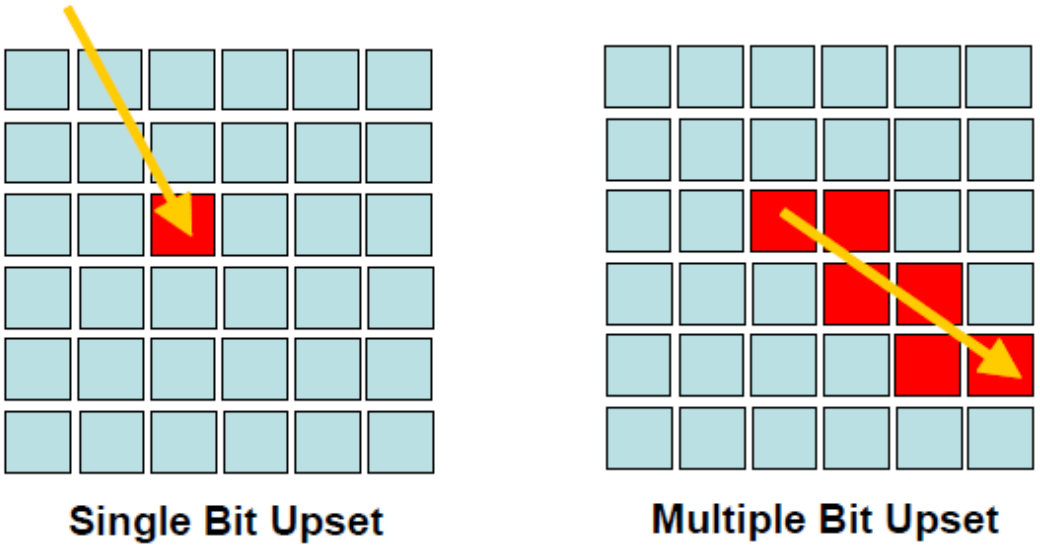


Fig. 1.12. A schematic representation of single bit upsets and multiple bit upsets in a regular memory array (After [17])

Conclusion:

In this chapter, basics of CMOS latches and flip-flops implementation were discussed. This chapter also introduces various sources of radiation and their effects on devices and circuits. Chapter 2 focuses on the Radiation Hardening by Design (RHBD) techniques and a brief survey of different radiation hardened latches and FFs.

Chapter 2 Radiation hardening

Radiation hardening can be applied at any level of abstraction. It can be at the device level, circuit level or at the architectural level. A hardening technique is generally chosen to meet the application requirements. The basic types of hardening techniques are shown as below:

2.1 Radiation hardening by process (RHBP)

Radiation hardening by process focuses on modifying the IC fabrication process to be structurally hard to particle strikes. Process steps are changed to modify the parameters that are affected by SEE. An example is bulk silicon have 10X more charge collection volume than silicon on insulator (SOI). Typical bulk technology uses epi thickness of 2µm comparing with thin film SOI of 0.2µm or less. While modifying the process, the impact on the performance of the device under normal operating conditions is minimized. RHBP involves changing steps, like silicon nitride passivation layer and thinning field oxide, for fixing oxide threshold shifts [18]. Resistive hardening [19] involves adding intentional resistances to the storage nodes of sequential elements. This results in increasing the time constant larger than Q_{crit} of these circuits and is consequently harder to upset. Another major disadvantage of this technique is that it is not commercially viable due to low demand, making it unsuitable for mass production and large document costs, which must be recouped by small volumes and limited number of designs. The costs and increasingly difficult development RHBP technology

(most modern known is 120 nm) lags the commercial process (28 nm chips are in production) by at least five generations in the semiconductor industry [20].

As IC technology advances in terms of linear dimensions, Q_{crit} is required to upset the node decreases due to inherent scaling in the new process. The RHBD techniques using a commercially viable process [27] with no changes in process steps and are increasingly becoming more attractive today.

2.2 Radiation hardened by design (RHBD)

Radiation hardening by design generally utilizes circuit design measures in order to achieve hardness the design using standard foundry processes [20]. This results in lower cost per chip, making it cost effective. Hardening by design also gives flexibility to designers to harden the circuit depending upon the chip functionality. A layout based method can be followed to increase the sizes of transistors such that the critical node capacitance increases, a higher Q_{crit} is required to upset the node making the circuit less vulnerable to radiation induced errors [21].

The other widely used technique is logic based hardware redundancy using a majority voter, which forms the basis for triple modular redundancy (TMR) logic systems [22]. Fig. 2.1. shows the block diagram for the TMR design. In this scheme, combinational and sequential logic circuits are replicated thrice and then passed through a majority voter as shown in Fig. 2.1.

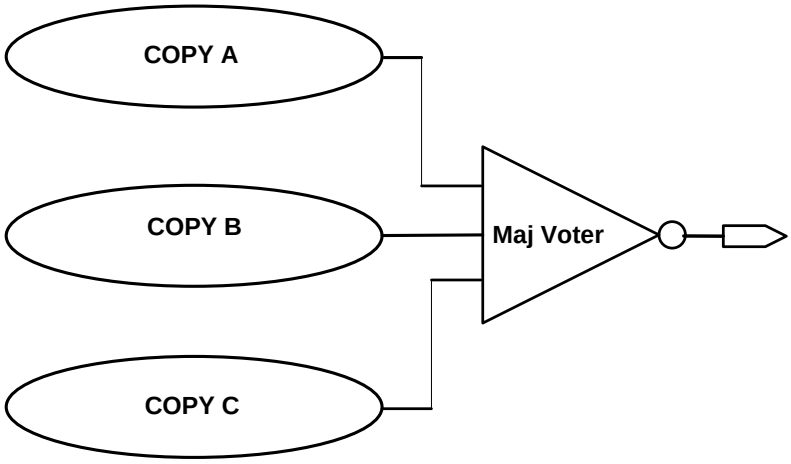


Fig. 2.1. TMR redundancy scheme.

If even one copy of the node is corrupted by SEE, two copies of the logic will be correct and the final output computed will be correct. However, multi-bit-upsets (MBU),caused by high energy particles incident upon circuit, can cause this scheme to fail as two out of three copies are corrupt and evaluated to wrong output. Thus, the redundant copies have to be spatially separated in layout. If two blocks are spatially separated by large distances, it is less likely to upset multiple copies of the same logic and output will be correct. In order to utilize area efficiently, most designers prefer interleaving multiple cells in layout while designing TMR circuits [21].

Another general method of filtering radiation errors is temporal hardening [23]. As implied, this method is time based. In this method, the logic signal is delayed by delay elements and sampled at different time intervals to check for consistency. The propagation delay of the delay element should be greater than measured SET so that

delay can outlast a SET. Fig. 2.2. below shows circuit diagram of the temporal hardening scheme discussed here.

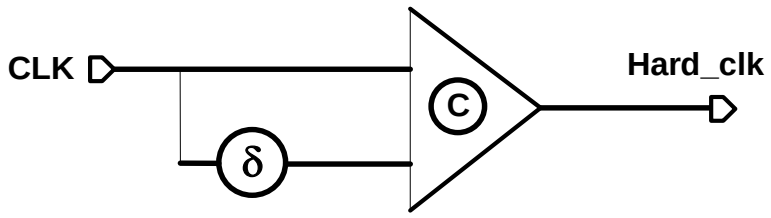


Fig. 2.2. Temporal hardening (Delay element with Muller-C (non-inverting)).

Fig. 2.2. shows the clock input and delayed version of the clock being fed to the Muller-C element. The Muller-C elements has inverting output that of input if both the inputs agrees and if one of the inputs does not match the other, the output node tri-states. If an SET strikes any node, both inputs of the Muller-C mismatch and it the circuit retains its previous value. This element serves as a hardening element, since the output cannot be incorrect unless both the inputs get hit simultaneously. If this element is present at the CLK input of the FF then data has to be hold stable for at least δ time.

These element limits the maximum frequency of the circuit by increasing the dead time.

2.3 RHBD Latches

RHBD latch designs focus on making the building blocks of the sequencing element radiation harden. There have been numerous circuits designed over the past 25 years to mitigate the SET and SEU. The most widely used circuit is dual interlocked storage cell (DICE) latch.

2.3.1 DICE Latch

The DICE was published by Calin et.al, where SEU immunity for this memory element was described [24]. Fig. 2.3. shows the operation and concept of a DICE latch. This is not an actual circuit but the principle of operation.

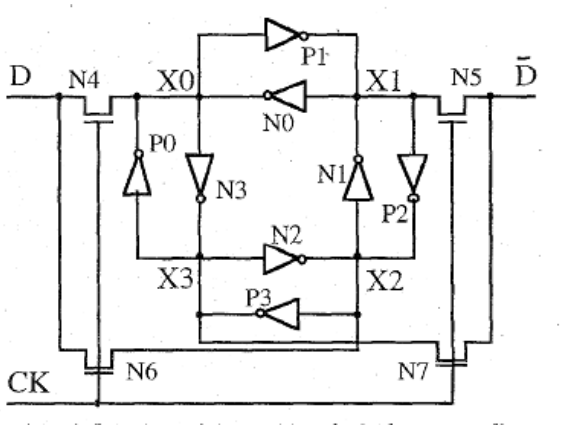


Fig. 2.3. DICE principle (After [24]).

The upset immune DICE has four storage nodes labeled X0-X3. It has four cross coupled networks; P1 and N0, P2 and N1, P3 and N2, P0 and N3. The storage nodes store two pairs of complementary value (i.e 1010 and 0101). All four storage nodes can be accessed through four separate access transistors, with pairs connected to the same input D and Dbar. This structure relies on "dual node feedback control" to achieve immunity. This implies that each of the four nodes is controlled by the two adjacent nodes located in the diagonal. Any strike on the single node cannot disturb the latched value in this circuit, as it has quadruple storage nodes connects in a cross coupled fashion. This is realized with four cross coupled inverters as shown in Fig. 2.3. However, half of each inverter can

be eliminated. The circuit in Fig. 2.3 then simplifies to two cross coupled inverters shown in Fig. 2.4. i.e. with transistors N0-N3 and P0-P3.

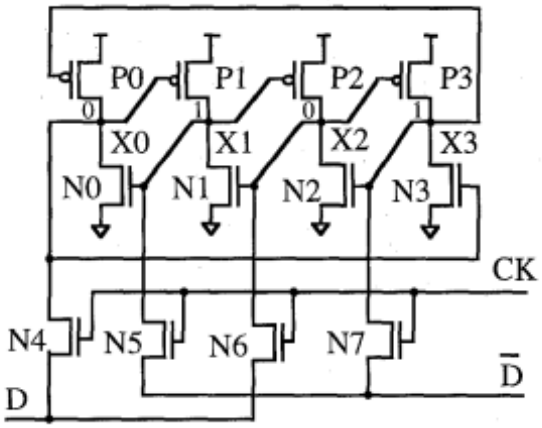


Fig. 2.4. DICE circuit (After [24]).

The difference between the working principle and the actual circuit is the removal of an NMOS or PMOS transistor from each of the inverters, as shown in Fig. 2.3. The feedback to each of the dual redundant storage nodes is from a previous node. However, key is that the NMOS and PMOS gate driving predecessor are not to the same nodes, so two of the storage nodes must have their logical states reversed to upset the cell. An example of a SEU forcing node X0 to be driven low is shown in Fig. 2.5.

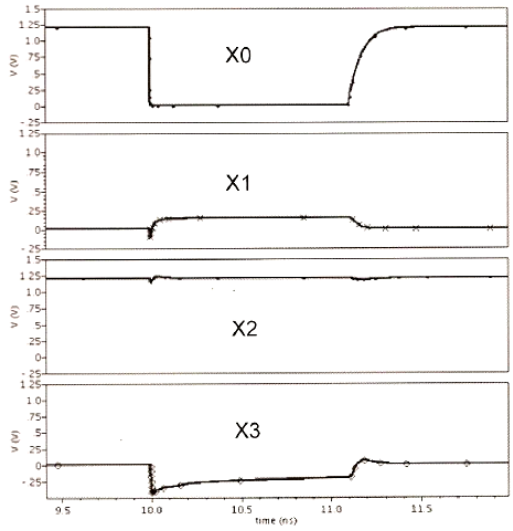


Fig. 2.5. Waveforms Showing SET strike at node X0 of the DICE latch.

Node X0 collects negative charge pulling X0 down for approximately 1 ns. During this time, the transistor P1 (Fig. 2.4) turns on opening the path from V_{DD} to V_{SS} through node X1. Node X3 becomes tri-state by the transient turning off transistor N3. Because of this, node X3 is easily couple below Vss by node X0, shown in Fig. 2.5. Nodes X1,X2 and X3 retains their logical state. When the node X0 has finished collecting charge, it charges back up VDD. After that X1 returns to Vss. All the nodes get restored to their original states as the three nodes are unaffected by SEU at this point.

2.3.2 Delay Filter DICE (DF-DICE)

Delay Filter Dual Interlocked Storage cell (DF-DICE) utilizes temporal sampling principle to protect against SET for every input [25]. Fig. 2.6. shows the schematic for the DF-DICE

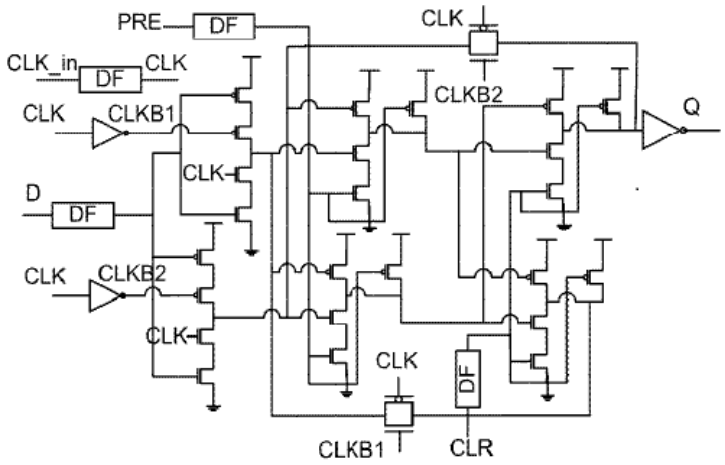


Fig. 2.6. Schematic for DF-DICE latch (After[25]).

DF block shown in Fig. 2.6 is delay filter which is delay element and the Muller-C element as shown in Fig. 2.2. This FF is hard to every input including D and CLK, as the DF block is present at every input. This design can be scaled to tolerate SETs of higher value by increasing the propagation delay of the delay element used in the DF block. This shows cost of filtering an SET is linearly proportional related to the width of the transient pulse. Since there is a linear relationship between the width of the transient pulse and the LET of the incident ion. So, the cost of soft error mitigation is proportional to the desired SET tolerance. The following table shows the comparison result for the DF DICE latch and FF against conventional DICE latch and FF. The area comparison were made based on the layout implemented in MOSIS SCMOS rules for 6-metal single poly .TSMC 0.18 micron technology. The results are tabulated in Table 3.

Table 3. Area comparison between DICE and DF DICE(After [25]).

Transient Threshold	DF-DICE latch Area (um^2)	Increase per latch	DF-DICE Flip-flop Area (um^2)	Increase per flip-flop
250ps	82160	54%	117515	31.7%
450ps	94413	77%	129768	45.5%
650ps	131936	100%	142424	59.7%
850ps	119925	124%	154878	73.5%
1200ps	145638	172%	179787	101.5%

2.4 Triple modular redundant technique

Triple modular redundant or latches and flip-flops mitigate SETs and SEUs through employing spatial hardening by creating multiple critical nodes and physically separating them in layout. This requires the desired circuitry to be placed and triplicated along with the sequential logic. Outputs are voted by circuitry such as majority voters. Ion strikes may affects one of the three node circuits, correct values from other two circuits vote out the incorrect logic level as shown in Fig. 2.7 below

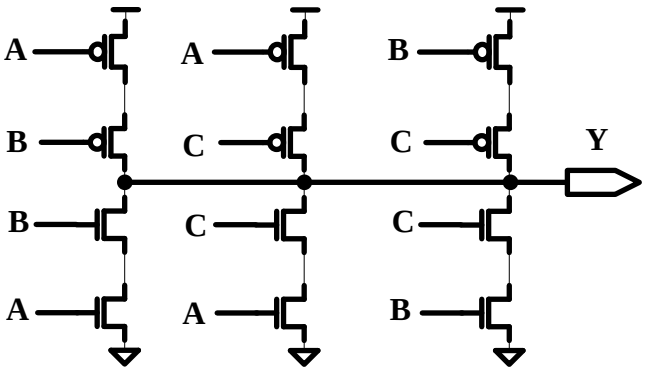


Fig. 2.7. Schematic of Majority voter

The majority voter is a cmos circuit that compares the input value and outputs the value that two or more inputs agree on. The truth table is shown in Table. 2. The gate shown is inverting in nature.

Table 4. Majority Voter truth table.

MAJORITY VOTER TRUTH TABLE

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

The disadvantage of TMR circuits is in terms of size and power because the circuit is replicated thrice. A variant of the TMR scheme was used in Built-In Soft Error Resilience FF (BISER FF) [26]. Fig. 2.8. shows the block level implementation for the BISER FF.

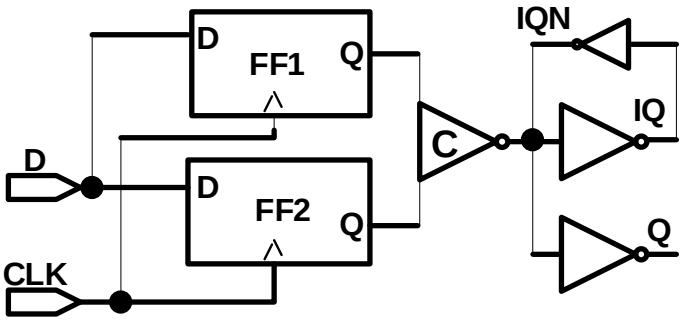


Fig. 2.8. Schematic of BISER FF(After [26]).

The BISER FF has two FFs in parallel and works on the principle that if one of the nodes are affected, the Muller-C tri-states and retains the correct logic state. However, this does not protect against multi bit upsets (MBU). Even single event upset at D will propagate all through both the flip flops and Muller-C elements capture the wrong value. It is not hard to any upset in CLK inputs as well. In the original BISER paper, the output inverter is missing and the output and storage node are same. This should be avoided at all cases as output noise can couple to the storage node and flip the output. Output inverter is used to decouple the storage node from the output node. This design is almost equal to five latch design as the C element and feedback keepers take silicon area of a latch. The two FF comprises of 4 latches. In order to make the circuit hard to MBU the two parallel flip flops should be interleaved in the layout.

2.5 Temporal Hardening

An alternative approach is to implement three independent flip-flops where each clock input of the flip flop is delayed by a delay Δt (see Fig. 2.9.).

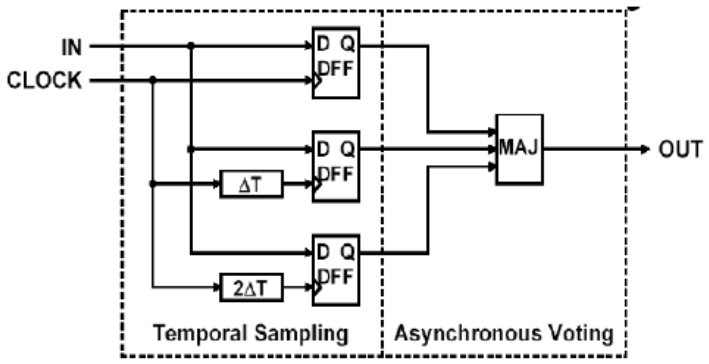


Fig. 2.9. Temporal Sampling at clock input (After [23]).

If the single event transient appears at the D input, then it will propagateto the D inputs of the all flip-flops simultaneously. The clocks however, do not propagate at the same time. Since Δt is longer than the SET width, the glitch on the D input will be corrected to its original state before the delayed clock by Δt and 2Δt. Two copies of the output of the FF will be correct. When this reaches the majority voter, the value at the final output will be always correct. Majority voter performs temporal voting, in this case at least two of the three copies match. The key drawbacks in using the temporal design in a RHBD are their big sizes because of the presence of the delay element. One major problem with delay element it should have more propagation delay then SET width designed for. Since, with the technology scaling each gate is becoming faster, making delay match to SET width requires many gate stages making delay element bigger in size. Dead time of the flip flop also increases because of increase of setup rime. While designing a temporal latch, it is important to account for the longest SET that is likely to occur in the radiation environment of interest.

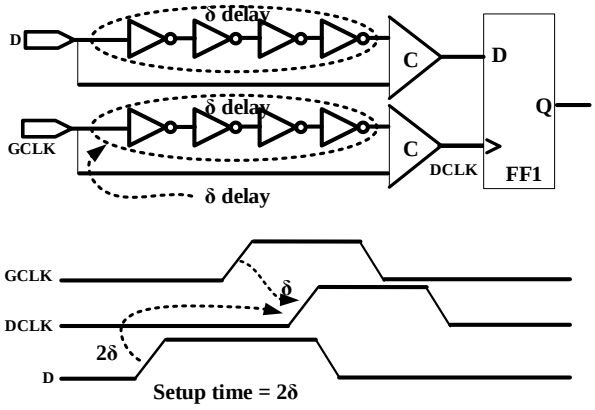


Fig. 2.10. Setup timing parameters for temporal sampling.

Fig.2.10. example shows temporal delay filter with Muller-C element at CLK and D input. The flip flop receives a derivative clock DCLK which is the delayed version of the GCLK. For the proper operation of the circuit the data has to be set 2δ before the DCLK. If SET of duration δ occurs during first δ phase during set up time, Muller-C element gets the correct value in the later half. If SET occurs in later phase, output of the Muller-C was already at correct state and is not affected by SET. Another Temporal FF using delay element is shown in Fig. 2.11 below.

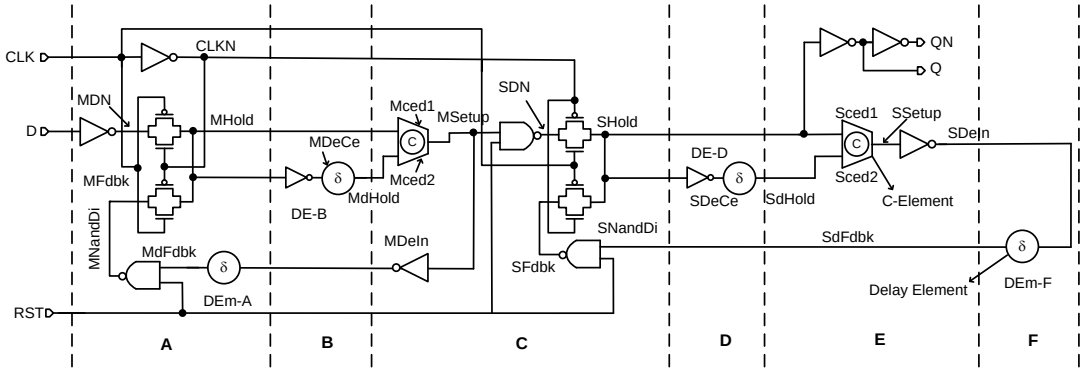


Fig. 2.11. Temporal FF using delay elements (After [21]).

As we had previously discussed , designing delay element takes multiple gate stages to match the delay of SET width. Moreover, It consumes more power also. The Temporal FF shown in Fig. 2.11. uses four delay elements per flip flop. The entire circuit was laid out in TSMC 90m and it was observed 58 % of the area is taken by these delay elements. Any scheme without the delay elements will be more area and power efficient. As we discussed in chapter 1, pulse based FF have shared pulse clock generator driving multiple FFs. Since, Pulse clock generator is driving multiple FFs in parallel we can

temporally delay the clocks in pulse clock generator using the delay elements to drive all FFs. The no. of delay elements is decreased by manifold making it more area efficient and power efficient.

Conclusion

This chapter discussed the commonly used RHBD techniques. A brief literature survey on RHBD latches has been done. A novel flip flop is proposed in the next chapter which utilizes techniques mentioned above along with a pulse clocked based methodology.

Chapter 3 Temporal Triple Pulse Clock Hardened FF

Chapter 2 discusses the constraint of using delay element in temporal FF design. It uses four delay elements which makes more area and power inefficient. As stated earlier pulse based FF have the shared pulse clock generator (PCG) driving multiple FFs. Clocks can temporally be separated in PCG to save upon on number of delay element to make more efficient design. The initial proposed circuit is shown in Fig. 3.1

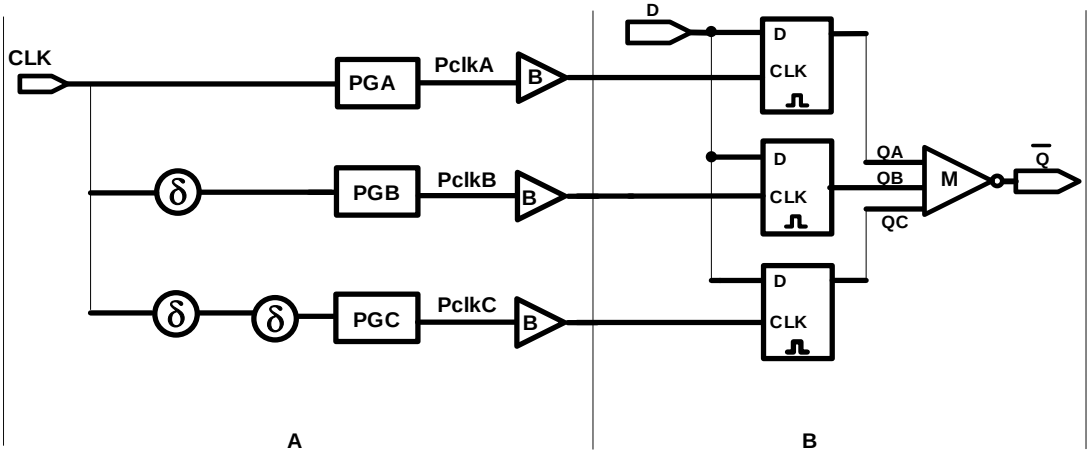


Fig. 3.1. Initial proposed Temporal pulse based FF.

The circuit consists of a PCG and triple modular redundant (TMR) latches with a majority voter(Fig. 3.1). PGA, PGB and PGC are pulse clock generators. PGA input is clock input while PGB and PGC inputs are temporally separated clocks by δ and 2δ from clock. The PCG generates three pulses which are δ apart from each other. Window B shows TMR latches along with majority voter. Circuit operates to work in normal conditions without SET but in presence of SET glitches at clock and high phases it fails

to latch the correct data. Simulation showing the case when SET low hit the clock input is shown in Fig. 3.2.

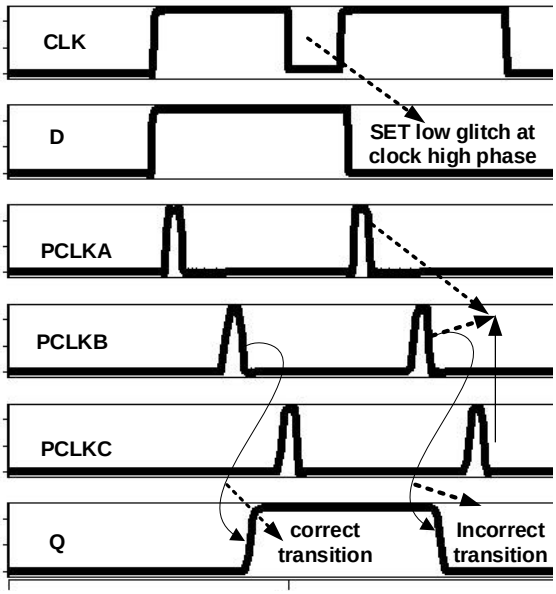


Fig. 3.2. Waveforms for initial proposed Temporal pulse based FF.

It is observed that FF is not hard to clock input . Similarly any glitch at the D1CLK will be also propagated to D1CLK and D2CLK and will generate false pulses which will evaluate to wrong result. Circuit must be protected against CLK, D1CLK and D2CLK . A delay filter (DF) implementation discussed in chapter 2 can protect against SET against this input. So DF is introduced at the inputs (CLK, D1CLK and D2CLk) along with Muller-C element. Little variation over the existing FF will be discussed in next section.

3.1 Circuit Design

The proposed temporally pulse clocked TMR FF (TPC-TMR-FF) consists of three pulse clock generator (PCG) and a triple modular redundant (TMR) latches with a majority voter(Fig. 3.1). The operation principle of TPC-TMR-FF is based on that of the pulse-clocked latch which behaves a FF as shown in Fig. 2.3.

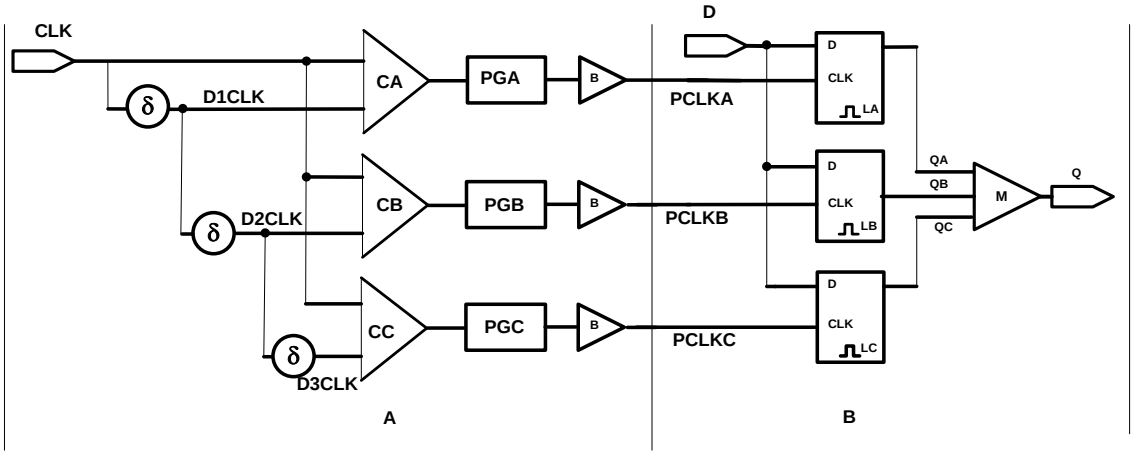


Fig. 3.3. Schematic of the TPC-TMR-FF . Window A represents temporal pulse generator and window B represents three latches and a majority voter.

PCG includes delay elements, Muller-C elements (marked as CA, CB, CC), pulse generators (marked as PGA, PGB, PGC) and buffers . The two inputs of Muller-C element CA are clock (CLK) input and delayed version of CLK, which is labeled as D1CLK. The Muller-C element only propagates the rising edge only if both the inputs matches each other. In normal operation, the clock will be generated at the Muller-CA's output after a propagation delay equal to that through the Muller-C element following D1CLK generation.

Similarly, CLK and a delayed (by an amount of δ) version of D1CLK (referred to as D2CLK) is passed through another Muller element CB. By design, D2CLK is temporally separated from CLK by an amount of 2δ and thus the Muller element CB's output is generated 2δ after the clock edge. In the same way, CLK and delayed version of D2CLK (referred to as D3CLK) is passed through Muller element CC to generate a clock 3δ after the CLK input. This circuit is termed as temporal because of three sampling points that are δ, 2δ, 3δ after the clock.

The Muller elements CA, CB, and CC's outputs are applied to the inputs of pulse generators PA, PB, PC respectively in order to generate three pulses that are δ delay apart from each other. The pulse generator (shown in Fig. 1.7(a)) generates a pulse of width duration equal to 3 inverter delays. Its output is buffered in order to share the temporal pulse generator with multiple latches to implement multi-bit FFs. Size of the buffer depends on the number of FF that need to be used in a group. Since, using the pulse generator results in an overhead, grouping multiple FFs reduces the overhead per flip flop. Thus, increasing the area and power efficiency of the TPC-TMR-FF .

The three buffered pulse outputs are fed to the positive level triggered latches' CLK pin. D inputs of each of these latches are connected to the FF D inputs. The output of all these latches is fed to the non-inverting majority voter to obtain final output Q.

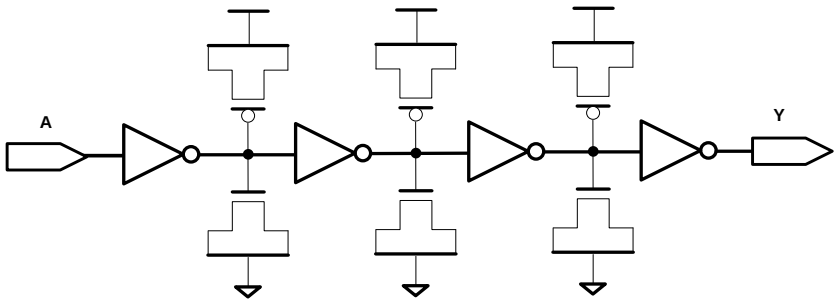


Fig. 3.4. Schematic of the delay element. It is a chain of 4 inverters with loading capacitors in between to load the stages that increases the circuit delay.

The delay element provides finite delay between input and output. A basic circuit consists of a chain of inverters. Layout was done for chain of inverters to get the same delay, but the size of the layout was much bigger than proposed delay element. So, delay element shown in Fig. 3.2 was designed to decrease the area of the FF. Delay element is a basic element for many RHBD FFs; any improvement in terms of its silicon area is significant.

The proposed delay element is a chain of four inverters with loading capacitors between two stages. Loading capacitors at the input and the output were not used in-order to avoid loading at the input and slow transitions at output. Circuit delay was increased by the use of longer channel lengths (L), which ultimately reduces the W/L ratio of the transistor and hence, decreases the current drive that leads to an increase in the delay. Choosing W, L value of transistors were not done arbitrarily in order to increase the delay. SET recovery time is also an important factor in radiation-hardened circuit design and was therefore considered while designing this circuit. This delay element, when hit by an SET, should recover faster than the gate that exhibits the worst recovery response

to an SET in the library or else it will be the worst gate in the technology. For this purpose, PMOS of the inverters were sized better than those of the NOR3 and the NMOS were sized better than NAND3 NMOS. The process design kit (PDK) used for whole design is TSMC90 low power process.

Delay element has propagation delay of 600 ps (at typical corner at 25^{o} C with the post-layout netlist) was chosen for the proper operation of the TPC-TMR-FF . Pulse width generated by the pulse generator PA, PB and PC are equal to 180 ps (proper methodology for determining pulse width is explained later) at typical 25^{o} C. The duration of SET glitch is 400 ps. The delay of delay element (δ), of 600 ps ensures pulse width of duration 180 ps with an interval of at least 400 ps between the first pulse's falling edge to the second pulse's rising edge. Any SET occurrence can hit one of the pulse generated at a time. No two pulses will get hit at the same time since they are separated by a δ of 600ps.

Window B has three latches that are transparent during high phase of the clock. Outputs from the three latches are connected to the majority voters' inputs. Majority voter circuit only propagates correct output if two or more copies are correct. Since the latches used here work during positive clock phase, particles with higher LET (threshold that produces more than 400 ps temporary glitch) strikes can hit two pulses at a time and the TPC-TMR-FF can generate a wrong output. The designed TPC-TMR-FF can only filter SETs of duration maximum to 400 ps. Scaling of delay element is required to filter larger duration SETs, increasing the size of pulse generator.

3.2 TPC-TMR-FF Timing

Fig. 3.3 shows the basic operation and timing for the TPC-TMR-FF in the absence of an SET. The D input of TMR latches is asserted during high phase of the clock. Since, the pulse width is enough to pass D input to output a value through the latch, data input D must be asserted before the rising edge of PCLKA. In the absence of SETs, output will be correct if two latches sample the correct value. The D input can be de-asserted after the falling edge of PCLKB. All the clocks i.e. PCLKA, PCLKB, and PCLKC, are derivatives (delayed by a duration of δ) of original clock (CLK). The timing parameters of the TPC-TMR-FF is measured taking falling edge of PCLKB as reference are t_{setup}= δ + setup time of the latch, t_{hold} = hold time of the latch and

$t_{clk\text{-}q}$= t_{pd} (latch + majority gate) .

These timings are clearly illustrated in Fig. 3.3.

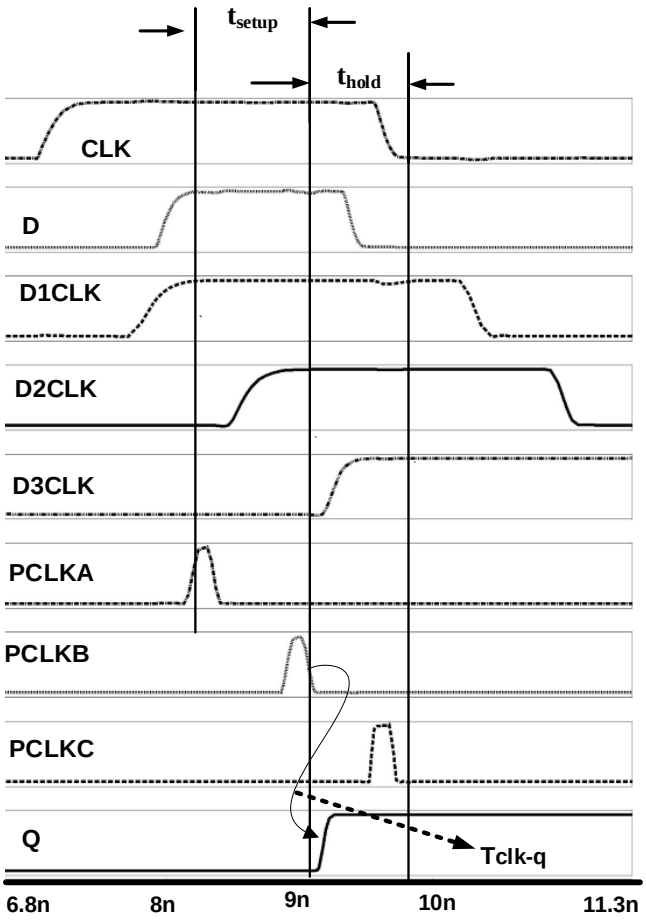


Fig. 3.5.Normal operation of the TPC-TMR-FF under no SET. Hold time is equal to hold time of latch.

The TPC-TMR-FF can operate correctly in absence of SET with a hold time just equal to the hold time of latch, which is sufficient to get the correct output. But, this is not true for case when there is SET. In presence of SET, PCLKA or PCLKB can go wrong (Fig. 3.4 shows SET low during PCLKA generation) and correspondingly LA and LB can capture incorrect value. LC latch can correct the output if the data is held long enough till the PCLKC falling edge. Fig. 3.4 shows operation of TPC-TMR-FF in

presence of SET where PCLKA gets SET low during its generation. The different timings with PCLKB falling edge as reference is t_{setup} = δ + setup time of the latch ,

t_{hold} = δ + hold time of the latch and t_{clk-q}= t_{pd}(δ+latch + majority gate) .

Observe that t_{setup} is not changed while t_{hold} and t_{clk-q} have increased by a time duration of δ .

The dead time of the FF is large (in range of 1.5 ns), which makes it slow. t_{pd} is propagation delay (t_{clk-q} max-delay) which is δ more than t_{cq} contamination delay(t_{clk-q} min delay). A minimum logic of δ is required between the FFs to avoid any hold violation in a pipeline design While designing a shift register using this FF, a δ hold buffer was placed in between the FFs.

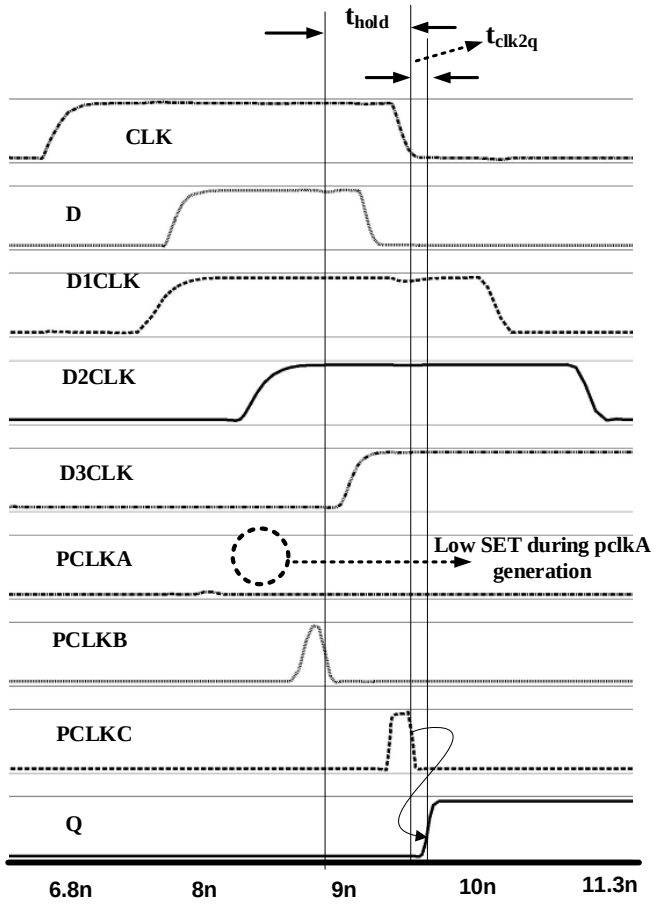


Fig. 3.6. Operation of the TPC-TMR-FF with SET at PCLKA. Hold time is equal to hold time δ+ hold time of the latch.

3.3 SET SIMULATION METHODOLOGY

The TPC-TMR-FF was comprehensively simulated to confirm the validity of the circuit hardening against SETs and SEUs. The hspice modeling for SETs was used for all the simulations in order to ensure that an accurate representation of an ion strike's effects was applied to the circuit.

Simulations were done with SETs disturbing single node and double node at the same time. There can be four different broad categories of SETs that can change the normal waveform. These are shown in Fig. 3.5 on CLK input.

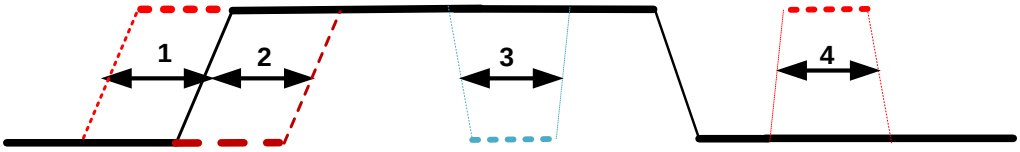


Fig. 3.7. SET simulation methodology. Four different kinds of SET resulting in early arrival, delaying and temporary glitches in the normal waveform.

In the Fig. 3.5, SET type 1 and type 2 represents SET high and low during the clock rising edge causing early arriving and delaying the clock signal respectively. Type 3 and 4 represent temporary low and high glitch during CLK high and low phase respectively. Any other SETs lies in one of the categories discussed above.

3.3.1. HSPICE MODELING FOR THE SETs

Accurately simulating the effects of ionized particles striking a circuit is critical when verifying a circuit's radiation hardness before beginning physical design. In many cases, the use of standard CAD simulation elements doesn't sufficiently emulate how a circuit reacts in a radiation environment. There are other complex models that have been already developed, such as semiconductor defects [27], charge cloud shape vs. time [28], and formulas for the drain currents initiated by charge collection [29]. However, circuit simulations do not usually require this level of detail.

For our simulation we used hspice model to emulate the SET. Hspice code for emulating the SET is given below.

****** Hspice modeling for emulating the SET low******

```
.param set_time = 10n

V_ctrl_h control_node 0 PWL (0 0 'set_time-0.01n' .001   (set_time)  pvdd
'set_time+0.4n'   pvdd set_time+0.41n'   .001)

G_Switch_h clkb  nh VCR PWL(1) control_node  0 0v,100g 1v,1p

R_load_h nh vss!  100
```

****** End of hspice modeling for emulating SET low******

The above hspice code models a voltage controlled resistor whose value depends upon the voltage of control_node. Control_node is a piecewise linear function of voltage whose value is a pulse of duration 400 ps. Resistor is connected between the node that is hit and the ground power node (vss!) as per the code. When the value of control_node is 0, then resistance value changes to 100 GΩ and it is equivalent to open circuit or no SET at all at given clkb node in this case.

When the value of the control_node becomes 1, the resistance value is changed to 1pΩ and becomes equivalent to a short circuit and the node gets connected to 0V. In the example given above, SET is applied from 10n to 10.4 ns. It stays at 0V for a duration of 400 ps and afterwards when control_node turns back to 0, the node changes back to the original state. This model can be converted into SET high model just by changing one

end of the resistor from vss! to vdd!. Fig. 3.6 shows an hspice simulation result using the above model.

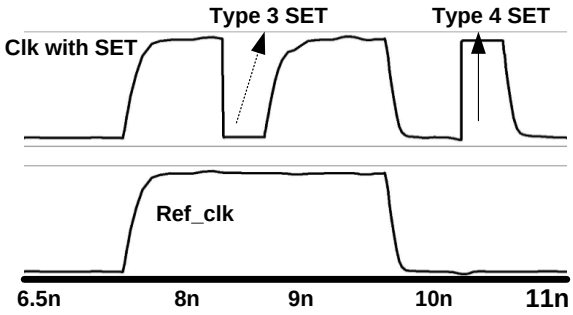


Fig. 3.8. SET simulation methodology type 3 and type 4 is shown on CLK input. Temporary glitches have the duration of 400 ps.

3.3.2. SET Simulation on Proposed FF

Hspice model discussed in the previous section was used for testing the hardness of TPC-TMR-FF against SETs and SEUs. Fig. 3.7 shows the simulation result with SET type 4 (clock high glitch at low input) particle hitting the clock node of the flip flop at 12.4 ns. It can be observed that clock glitch gets propagated to all the D1CLK, D2CLK, and D3CLK. The Muller-C element filters out any glitches at its output as both inputs differ. None of the Muller-C elements propagate the false transition at the clock input. Nor does any of the Pulse clock generators receive any input and the final output Q remains at the previous state as desired.

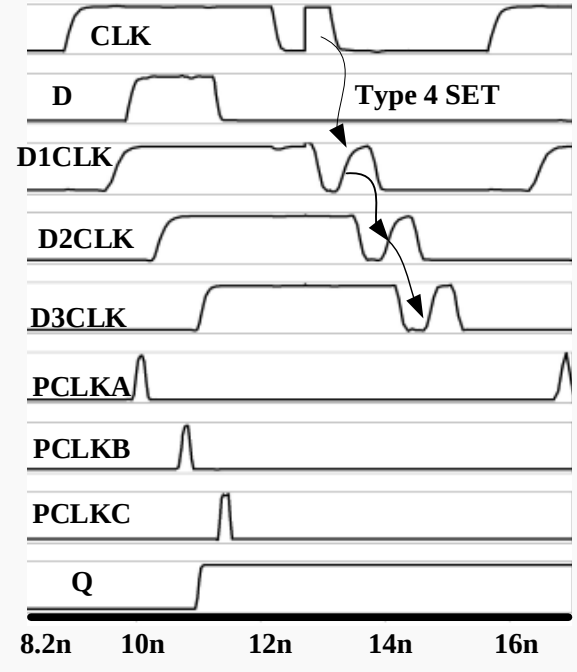


Fig. 3.9. Type 4 SET at CLK input. D1CLK, D2CLK, and D3CLK propagate the glitch but the Muller-C element filters out the glitch. output Q state is retained.

A simulation depicting that the TPC-TMR-FF is hard to SET at input D is shown in Fig 3.8. Since the pulses are separated by δ time, any SET at D will propagate to one of the latch state but the other latches will sample the correct value of D giving correct output. Fig. 3.8 shows that the latch LA samples incorrect value because of incorrect value of D during its sampling but the latches LB and LC samples the correct value, (D is corrected by that time)thereby resulting in a correct output at Q.

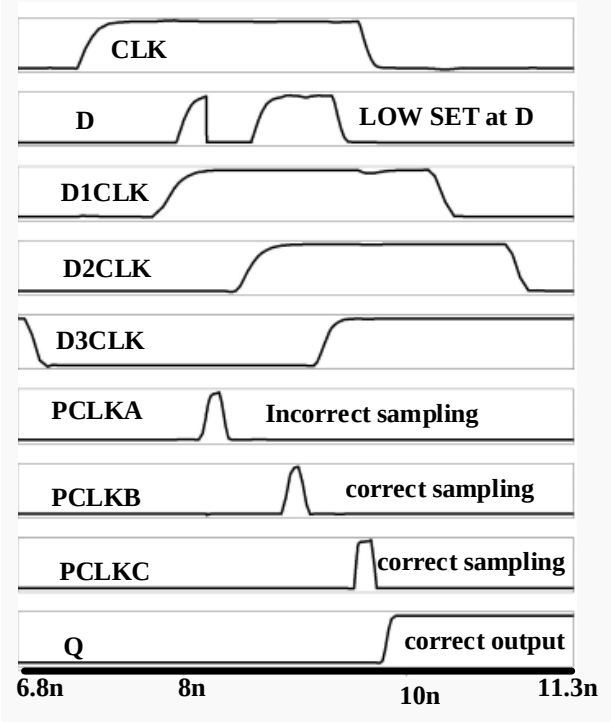


Fig. 3.10. SET low at D input. PCLKA samples the incorrect value but PCLKB and PCLKC samples the correct value giving the correct output.

Since TPC-TMR-FF is a combination of pulse generator and latches, it is important which node of pulse generator can go adjacent with the node of the three latches from a physical design point of view. TPC-TMR-FF is simulated for two simultaneous hits at two different nodes, a node from pulse generator, and a node from three latches. Fig. 3.9 shows a case when there is a simultaneous hit on PCLKC and QB node of the latch. Node QC doesn't latch correct value as PCLKC pulse was not generated because of SETs. Node QB of the latch is now incorrect because of SET at QB. Out of the three inputs of majority gates, two are wrong, which results in the majority gate evaluating a wrong output.

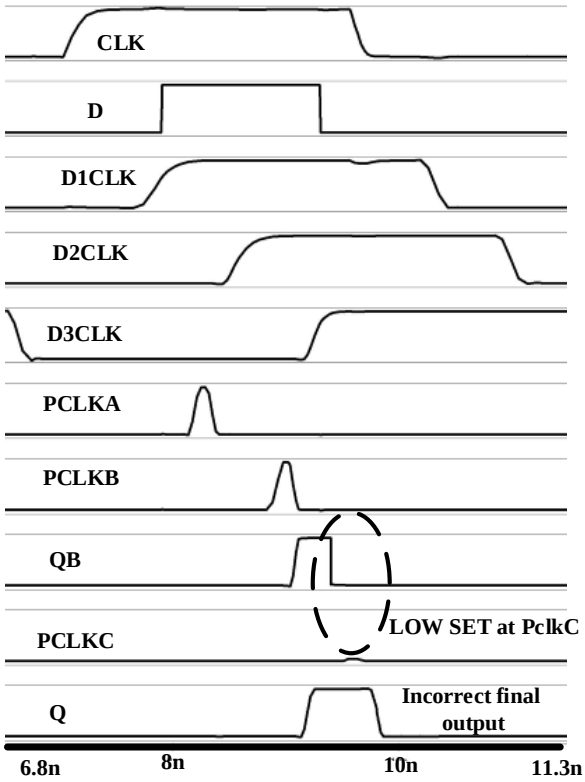


Fig. 3.11. Dual SET hit on QB input of majority gate and PCLKC. The final output is incorrect since two inputs of the majority gate are incorrect.

Fig. 3.10 shows case of simultaneous hits on PCLKA and QA. Node QA does not latch correct value because of the SET at PCLKA. Node QA has a wrong value, but QB and QC have correct values that make a correct transition at Q.

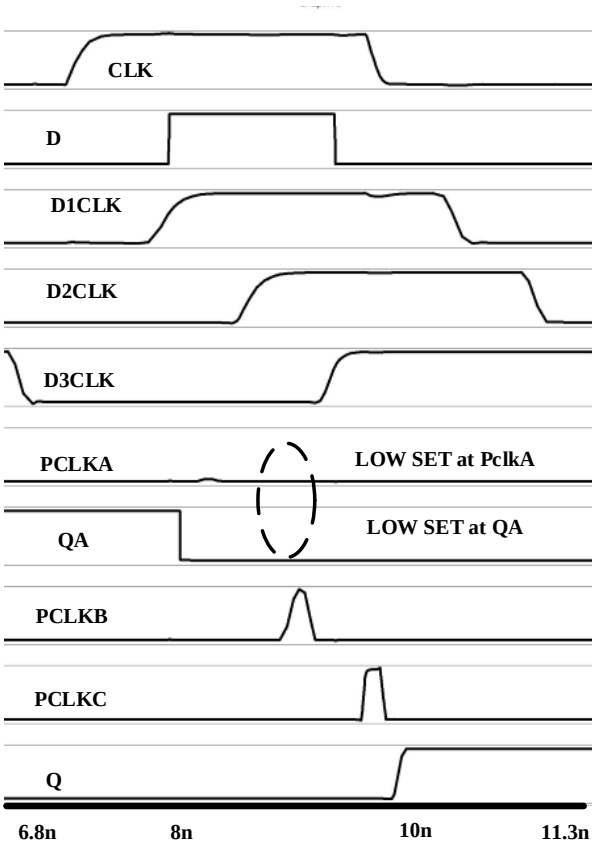


Fig. 3.12. Dual SET hit on QA input of majority gate and PCLKA. The final output is correct since two inputs of the majority gate are correct.

Table 5. shows simultaneous dual fault analysis indicating which latch nodes need to be separated from which pulse clock generators nodes. The value 0 denotes passing cases, while 1 marks failure that can't go next to each other.

Table 5. Showing simulation results for simultaneous dual fault analysis on pulse generator and latch nodes. 0 show pass and 1 show failures.

	D	QA	QB	QC
CLK	0	0	0	0
D1CLK	0	0	0	0
D2CLK	0	1	1	0
D3CLK	0	1	1	0
PCLKA	0	0	1	1
PCLKB	0	1	0	1
PCLKC	0	1	1	0

3.4. Layout for the proposed TTPCFF

The physical design of the FF was implemented in the TSMC 90nm LP process. Following [30], vertical interleaving was employed between two FFs to create a multi-bit cell. The advantage of vertical interleaving is that it spaces critical nodes to decrease the probability of simultaneous hits , multiple node charge collection while maintaining high transistor density across cell. Since there are two FFs and each one has three latches, there will be a total of 6 latches and the majority voter's physical location can be shared by both. This means that two FFs can be physically laid-out in 7 standard cell height. The standard cell height in this technology is 1.96 µm, which makes the total height of the latches and majority voter 13.72µm.

The layout for the temporal pulse generator should be done taking into consideration that an SET can hit its multiple nodes at the same time or one node in temporal pulse generator and another node in the interleaved flip flop can get hit. Table 5. is referred in order to combine pulse generator and interleaved latches layout. Fig. 3.11 shows the floorplan for the proposed FF layout. Fig. 3.12 shows the actual layout

implemented in TSMC 90 nm process. The pulse generator design is 8 standard cell height, i.e., 15.68µm tall. Complete layout for the two bit interleaved FF is rectilinear. Auto place and route flow for rectilinear placement is followed in CAD flows. In pulse generator design, there are 3 delay elements that use significant area. Any scalability for higher LET can be performed by increasing the delay element size that results in the pulse generator size being increased. In order to decrease the overhead, multi-bit FFs are is designed to save area.

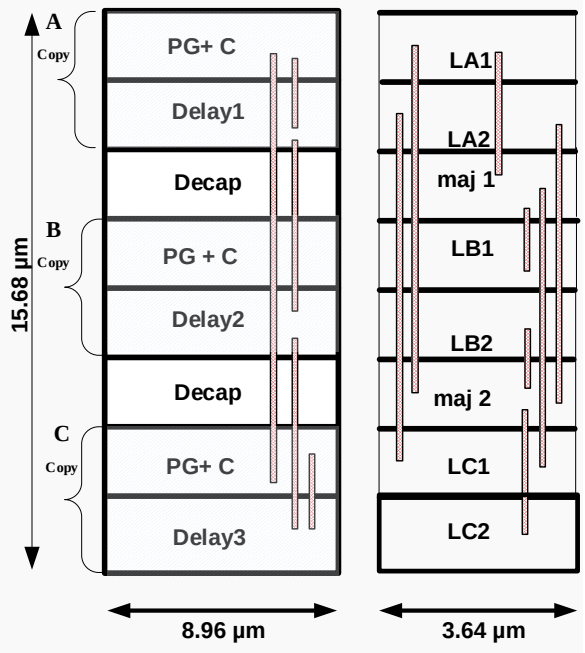


Fig. 3.13. Floor plan for the pulse generator and interleaved two FF design. Interleaved FFs were placed in columns for multi-bit design.

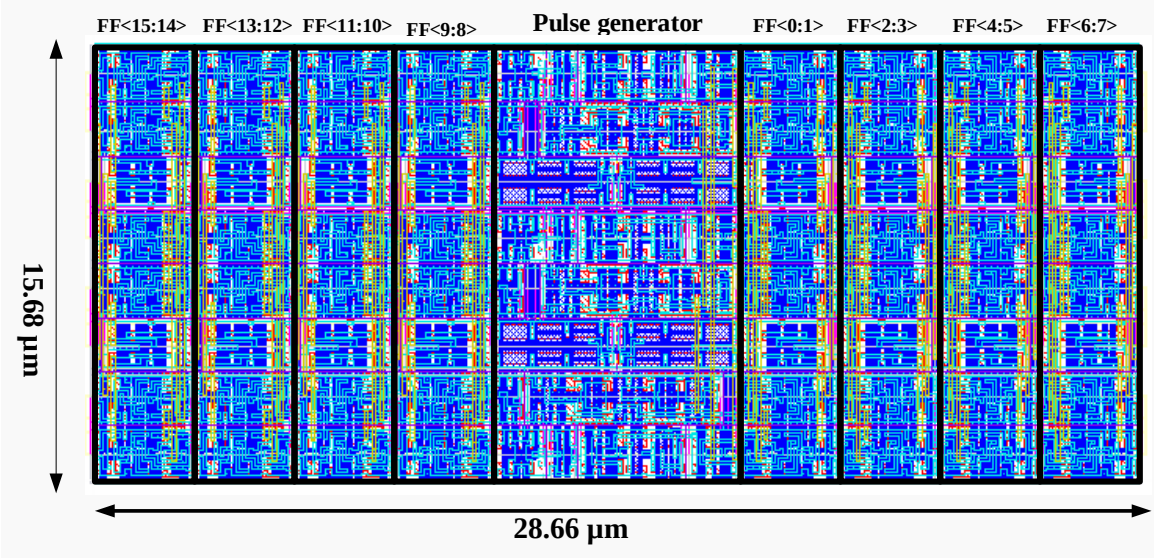


Fig. 3.14. Layout for the 16 bit FF implemented in TSMC 90 nm technology. The cell is 25.66 µm wide and 15.68 µm tall.

The power rails, which are at the top and bottom of standard cells in the used commercial foundry process, separate the standard cell rows through the use of metal 1. This means that vertical interleaving had to be completed using the vertical M2 routes. The layout was done with the minimum use of vertical M2 routes. 54 tracks were left unused for facilitating easier routing of power grids during auto place and route. Fig. 3.13 shows M2 track for 16 bit FF.

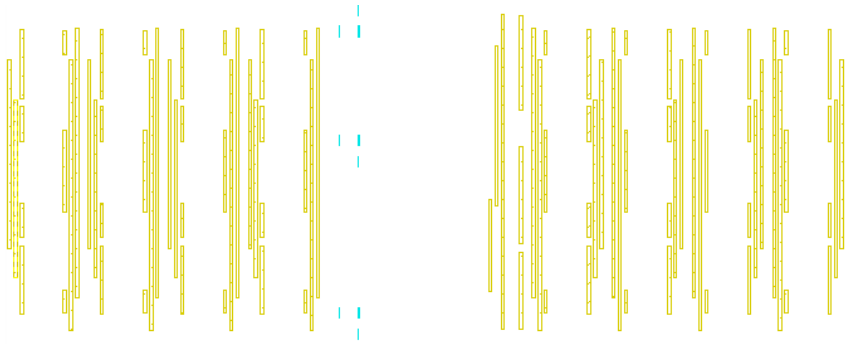


Fig. 3.15. M2 tracks (yellow wires) for the 16 bit interleaved TPC-TMR-FF.

3.5. Determination of Pulse width

Any latch requires minimum transparency high period to propagate the data from input to output. The approach of finding the pulse width required with one simulation is not sufficient to determine its value. Both systematic and random mismatches are exacerbated by the CMOS feature size scaling. Many circuits are sensitive to mismatches between identical transistors. In many cases, the transistors are not adjacent and may see substantial differences in voltage and temperature. Modern day technology processor has more and more number of sequencing elements, so a statistical method for determining the correct pulse width is required. This method ensures that latches will function correctly under process, voltage, and temperature variations.

Monte Carlo (MC) simulation can be used to find the effects of random variations on a circuit. It consists of running a simulation repeatedly with different randomly chosen parameter offsets. To use MC simulation, the statistical distributions of parameters must be a part of the model . MC models for the transistors were provided in the model file of the process design kit used for our design. The MC measure statements report average, minimum, maximum and standard deviation computed from N (no. of simulation specified in transient analysis) repeated simulations. For determining the correct pulse, we varied pulse width statement from 20 ps to 200 ps and ran MC simulation for each value of pulse width for 1000 simulations. The hspice statements for the aforementioned experiments are shown below

```
Vclk_pulse E 0 PULSE 0 1.2 1n 1p 1p pulse_width
.TRAN 100p 2n START=0.0 SWEEP MONTE=1000
```

Then number of pass were measured for each pulse width is measured and normal distribution function was found and correspondingly mean and deviation of the pulse width required value are plotted in Fig.3.14.

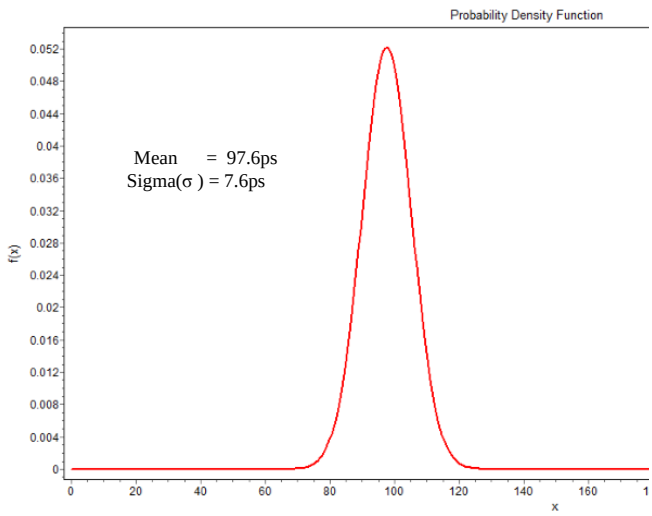


Fig. 3.16. Normal distribution of the required pulse width.

The mean (μ) and the sigma (σ) value for the latch characterization are 97.6 ps and 7.6 ps respectively. For a 4σ point, the pulse width required is 97.6 + 4* 7.6 = 128 ps. If we ensure the 128 ps from a pulse generator, the probability of failure will be 0.00632%, i.e. 63 in million.

Similar simulation holds true for pulse generator design too. One simulation for characterizing the pulse generator is not sufficient. Therefore, MC simulation was carried out for pulse generator too. Each time pulse width mean and sigma were calculated and then μ- 3σ point of pulse generator was checked with 128 ps (μ+ 4σ of pulse width required). The designs were altered and simulations were done again if the pulse width

was not enough. After a series of experiments, correct pulse width mean and sigma of the pulse generator was found. Fig. 3.15 shows the mean and sigma for the pulse generator.

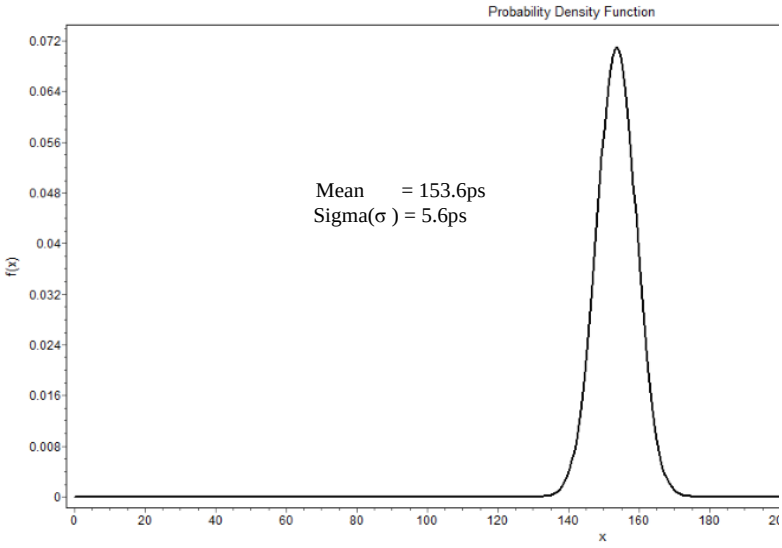


Fig. 3.17. Normal distribution of pulse width generated by pulse generator.

Pulse Width μ -3σ point is 136.8 ps compared to 128 ps (μ+ 4 σ of pulse width required). We still have 8 ps of margin after accounting for the worst-case random variation that can happen in the system. Designing with such a margin will never let system fail due to PVT variation.

Conclusion

In this chapter we have introduced a novel FF named TPC-TMR-FF . Different simulation results with single and dual hits were summarized. Physical design for the multi-bit FF was also shown along with the statistical method of generating the pulse

width. The following chapter discuss how TPC-TMR-FF will be used in various CAD flows for synthesis and auto place and route.

Chapter 4 CAD flows and power analysis for TPC-TMR-FF

4.1 Synthesis and APR Implementation

To further acknowledge the substantial size and speed penalties, the use of the hardened, multi-bit cell in a practical application, synthesis and auto placeand route (APR) design flows are used. Cadence RTL Compiler (Cadence RC) for synthesis and Cadence Encounter for APR CAD tool is used.

In order to start synthesis, the individual (single bit)TPC-TMR-FF is characterized first. This is needed due to the limitation in Cadence RC. Cadence RC cannot synthesize directly with multi-bit FF. The TPC-TMR-FF is characterized with the Encounter library characterizer (ELC), a CAD tool for generating liberty (timing) file. Since, TPC-TMR-FF is temporal pulse generator (TPG), a FF depending upon three clock pulses is difficult to understand for timing tool. Moreover, any timing tool does not calculate the timings for radiation hardened circuit. Tool calculates the value for unhardened design which works under the influence of no SET. The correct values for timing can be only hand hacked to use in synthesis for radiation hardened application. A FF from library is characterized with matching load at its input and output as TPC-TMR-FF to get the required arcs. Simulations with different corners (FF,SS,TT) is done on the extracted netlist to obtain the worst case t_{setup} , t_{hold} and t_{clk-q} for the TPC-TMR-FF . The worst case setup (t_{setup}) time is measured at FF corner, as setup edge is the rising edge of PCLKA. While worst case t_{hold} or t_{clk-q} is measured at SS corner as these are at falling edge of PCLKB and PCLKC respectively. Two different liberty files are made for

two cases in the presence and absence of SET as they have a δ (delay element propagation delay = 600 ps) difference between the t_{clk-q} and t_{hold} timings.

This is necessary to get the proper hold buffers between the FFs in pipeline design.

Single bit FF liberty file must be hacked to make multi-bit FF liberty file. An excerpt from the Liberty User Manual shows a general format when using bundles is

```
cell(inv) {
        area : 16 ;
        cell_leakage_power : 8 ;
        bundle(Z) {
                members(Z0, Z1, Z2. Z3) ;
                direction : output ;
                function : "D" ; }
        bundle(D) {
        members (D0, D1, D2, D3) ;
        direction : input ;
        capacitance : 1 ; } }
```

This format is manually applied to the ELC output .lib file after hacking the timings for the hardened flip flop. Once the .lib for the single bit and multi-bit FF is generated , the synthesis design flow is run for the given Advanced Encryption Standard (AES) design. RHBD designs requires hardened state elements and since library is delivered with unhardened FFs, attributes are set in synthesis script to avoid choosing from library flip flops and gaters. Synthesis tool has to choose the TPC-TMR-FF as sequential FF. RHBD temporal clock gaters is also designed and liberty files were

passed in the synthesis run. After mapping the AES design to generic gates, it is then mapped to single bit FF . Once it is mapped to single bit FF, attributes is set for using multi-bit FF by the of following commands and incremental synthesis is run.

```
set_attribute use_multibit_cells true /
set_attribute force_merge_seqs_into_multibit_cells true /
set_attribute use_multibit_seq_and_tristate_cells true /
synthesize -to_mapped -incremental
set_attribute multibit_cells_from_different_busses true /
synthesize -to_mapped -incremental
```

All the FF should be converted into multi bit FF provided all grouped FF have same clk. At last synthesis step, Encounter database is written to get the configuration file and timing constraint in encounter format.

Cadence Encounter is used for APR the design. APR requires geometrical data information of the pins, blockages and area of all cells. Cadence Abstract generator is used for this purpose. Abstract generator generates all the required information and write it to Library Exchange Format (LEF) file.

Encounter configuration file is modified in order to include the technology file and all the custom block LEFs. Design is loaded by loading the configuration file after invoking the Encounter. After successful loading the design standard APR flows are run (Including inserting Well tap, Power planning, Placement , Clock-tree synthesis , Post optimization and globalDetailroute) in order to finish the design . All the Custom blocks geometrical database system (GDS) are obtained through Virtuoso. Whole design

GDSII was obtained by merging all the custom blocks GDS and standard cell GDS. The following tables shows the setup and hold mode timing parameters after post clock tree synthesis. The design snapshot from Encounter with all the metal routes is also presented with the metal density.

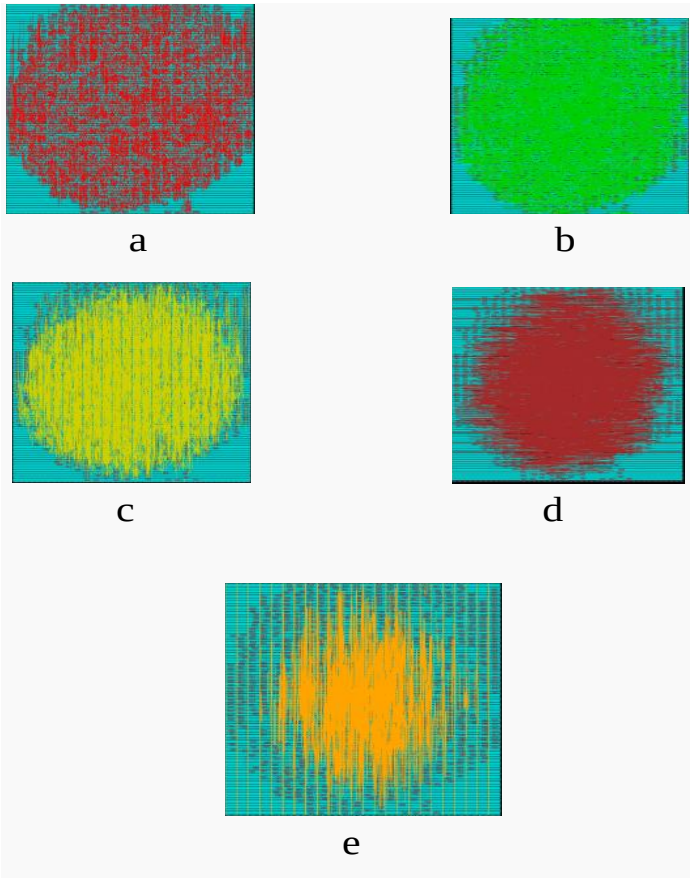


Fig. 4.1. Metal layers (2-6) routing in Encounter.

Table 6. Density of metal layers used.

Layer used	% of the routes used

M2	16.18
M3	23.12
M4	17.96
M5	21.12
M6	9.98

A snapshot for DRC and LVS clean is shown below .

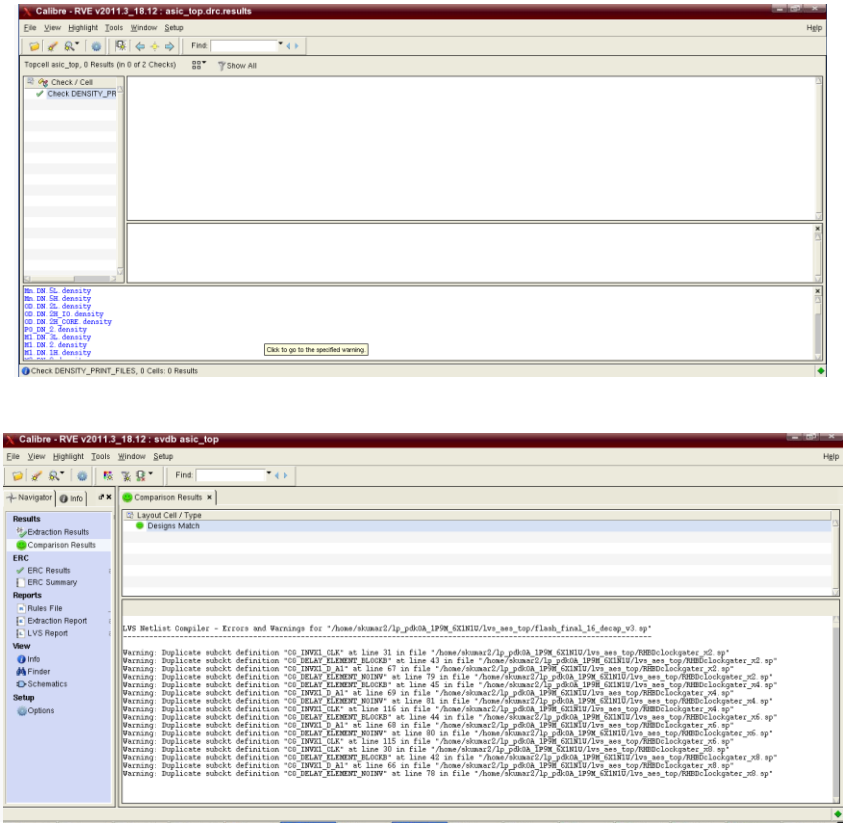


Fig. 4.2. DRC and LVS snapshot for AES design.

4.2. Power Consumption Analysis

Simulations are run on the TPC-TMR-FF to determine power consumption. Two different circuits are simulated for TPC-TMR-FF. One with TPC and eight FFs in parallel and other with TPC with sixteen FFs. This is done to determine the power of TPC and TMR latches separately. TPC consists of delay elements along with three pulse generators which consume majority of power. The outputs of these FFs are loaded with FO4 sized inverters. The simulation was run at a temperature of 25^{o} C, VDD = 1.2 V and at the typical process corners. Simulations were done to emulate the correct activity factors for the circuit. Clock activity factor is taken to α=0.1 and data activity factor to be α=0.05. The power measured for one bit FF with TPC averaged for one FF is 7.7fJ per cycle.

4.3. Comparison with BISER and Temporal FF

Same simulation for power were ran on the BISER FF[] and Temporal FF[21] for doing comparison with TPC-TMR-FF. For these FFs , the energy consumption for the same activity factor measured for TPC-TMR-FF is 5.91fJ and 9.66fJ

We can observe that reducing the delay element saves a lot of power. Comparison over other parameters are summarized in the table below.

Table 7. Comparison with different flip-flops

	BISER FF	Temporal FF	TPC-TMR-FF
Area	36.3 μm^2	67.97 μm^2	28.8 μm^2
Power	5.91 fJ /cycle	9.66 fJ /cycle	7.77fJ/cycle
Noise immunity	NO	YES	YES
Hardness	Not hard to D/ CLK	Hard to D/CLK	Hard to D/CLK

Chapter 5 Conclusion

This work discusses a novel FF named TPC-TMR-FF. It consists of temporal pulse clock generator and TMR latches. The reduction of delay elements over other temporal FF has a great advantage in terms of area and power. The proposed FF is hard to any upset in D and clk input also. Also simulation methodology for testing against SET is also discussed . Simultaneous strikes on two different nodes is simulated to determine which critical nodes cannot be placed adjacent in layout. Noise immunity and hardness over BISER FF is also improved by not exposing the storage node to the output node. Multi -bit FF design flow is used for synthesis and APR the AES design to verify the feasibility of using the proposed FF in modern CAD flows.

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