Extending Efficiency in a DC/DC converter with automatic mode switching from PFM to PWM

by

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ABSTRACT

Switch mode DC/DC converters are suited for battery powered applications, due to their high efficiency, which help in conserving the battery lifetime. Fixed Frequency PWM based converters, which are generally used for these applications offer good voltage regulation, low ripple and excellent efficiency at high load currents. However at light load currents, fixed frequency PWM converters suffer from poor efficiencies

The PFM control offers higher efficiency at light loads at the cost of a higher ripple. The PWM has a poor efficiency at light loads but good voltage ripple characteristics, due to a high switching frequency. To get the best of both control modes, both loops are used together with the control switched from one loop to another based on the load current. Such architectures are referred to as hybrid converters. While transition from PFM to PWM loop can be made by estimating the average load current, transition from PFM to PWM requires voltage or peak current sensing.

This theses implements a hysteretic PFM solution for a synchronous buck converter with external MOSFET's, to achieve efficiencies of about 80% at light loads. As the PFM loop operates independently of the PWM loop, a transition circuit for automatically transitioning from PFM to PWM is implemented. The transition circuit is implemented digitally without needing any external voltage or current sensing circuit.

ACKNOWLEDGMENTS

First and foremost, I would like to thank my advisor and mentor Dr. Bertan Bakkaloglu, for giving me this opportunity to work on this wonderful project and for being source of inspiration throughout my masters. It had been by dream to work on power management IC design and thanks to professor's guidance and motivation, I am finally able to. I would also like to thank Dr. Hongjiang Song and Dr. UmitOgras for taking time to serve as panel members on my defense committee.

I leave the research group with fond memories of working with my colleagues. My sincere thanks to Amit Kumar, KarthikPappu, AbhiramMumma Reddy, NavankurBeohar, KoushikMalladi, Debasis Mandal and Chao Fu for all the technical discussions and debates we had in the lab.

I would also like to thank James Laux for his support with the cadence software. I would also like to thank all the professors who taught me for their knowledge sharing

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1 Introduction

1.1 Background

As the market for increasingly small and portable electronic devices grows, there is a strong emphasis on preserving the battery charge, used to power these portable devices. Devices such as smart phones, PDA's etc. are required to run longer on a single battery charge to preserve battery lifetime. Thus a highly efficient power management IC is necessary to supply to these systems.

Switching converters are preferred to LDO's for high current applications as they offer higher efficiencies. Most of these switching converters are PWM based working at a high fixed switching frequency. The architecture of one such converter is shown below

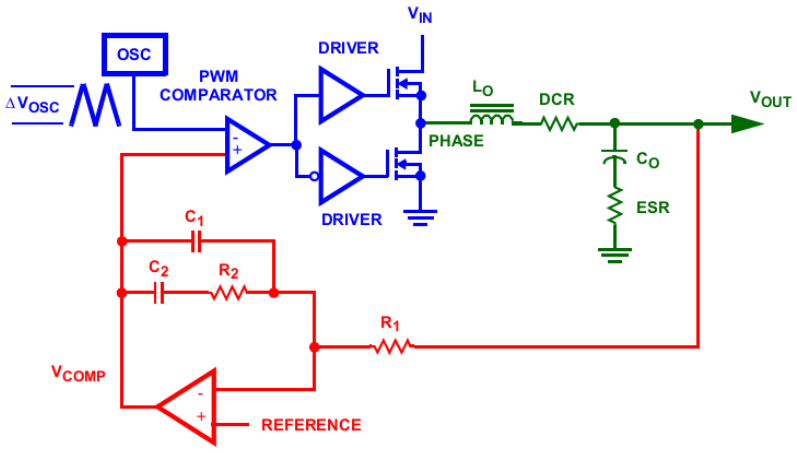

Figure 1: PWM based switching converter

With a view to reduce power consumption, all portable devices come with a Sleep/Standby mode, where the current consumption is between µA to a few mA. The fixed frequency switching converters suffer from poor efficiencies at these load currents,

because switching losses start becoming significant. The figure below shows the distribution of losses in a fixed frequency converter (Erickson & Maksimovic).

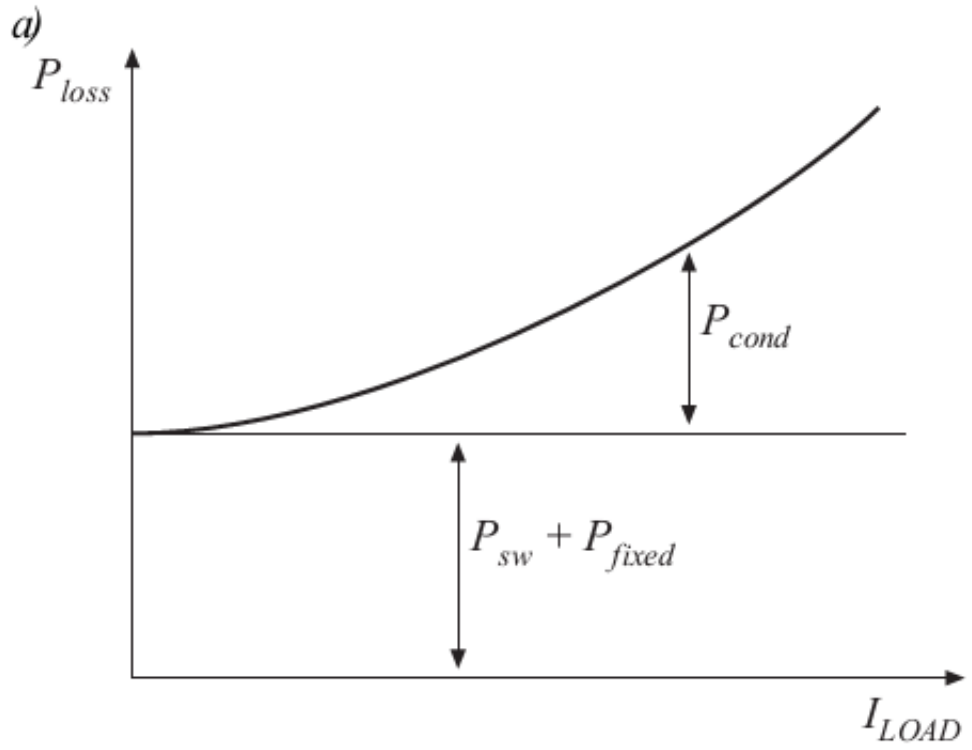

Figure 2: Variation of losses in a fixed frequency converter

As illustrated in Figure 2, a conventional DC/DC converter has substantial fixed losses, which are independent of the load current. These fixed losses lead to significant battery current at no load. The total power loss in a switching power converter can be expressed as

$$P_{loss} = P_{cond}\,(Iload) + P_{fsw} + P_{fixed}$$

whereP_{cond} stands for the conduction loss in the MOSFET and inductor resistances. This is function of the load current. P_{fsw} is the power loss to due to turning on and off of the switching MOSFET's. This is a function of the switching frequency. P_{fixed} is the fixed component of losses, which does not depend on load current or switching frequency. It is

usually depends on the current consumed by the power management IC to supply to the load.

As the conduction losses depend on the load current, the equation suggests that at light load currents, the frequency dependent losses can be reduced to achieve lower losses and hence higher efficiency. This is illustrate in the figure below

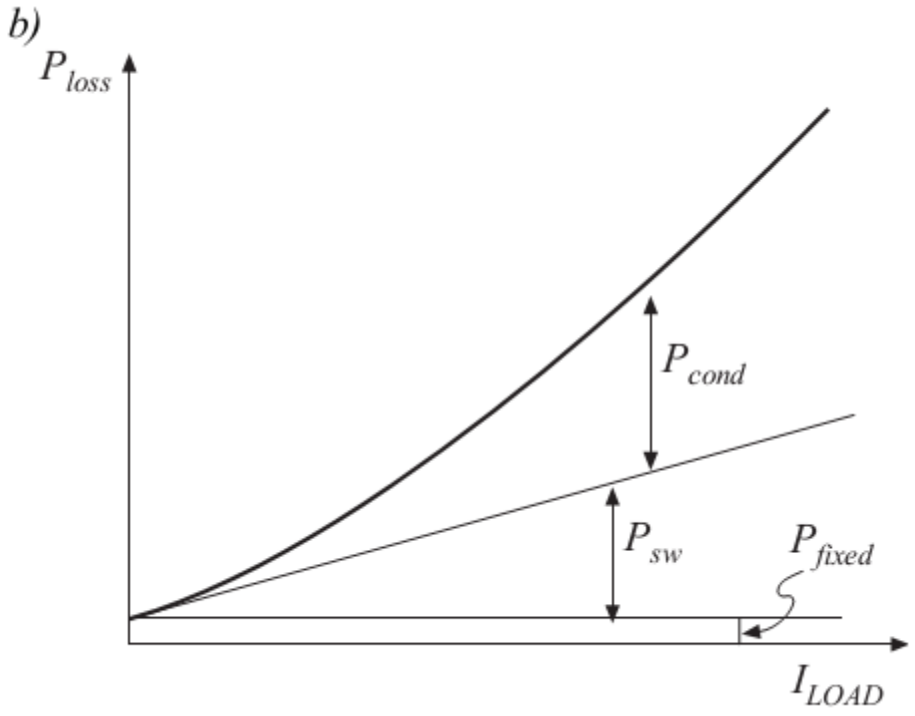

Figure 3: Variation of losses in a variable frequency converter

If frequency is made scalable is with load current, then the switching frequency losses can be reduced at light load currents. This is achieved by using Pulse frequency modulation (PFM) control. The PFM control achieves higher efficiency at light load currents, at the cost of a higher ripple in the output voltage and increased harmonics due to the variation of the switching frequency with load current. There are three popular implementations of the PFM architecture, which are discussed in the following section.

1.2 Existing PFM architectures

Depending on the variable being controlled, PFM architectures can be divided into three types

1.2.1 Hysteretic PFM

One implementation for achieving PFM is by using a simple hysteretic comparator as the feedback element. The comparator compares the feedback voltage to an upper triggering and a lower triggering voltage. An implementation of this is shown below.

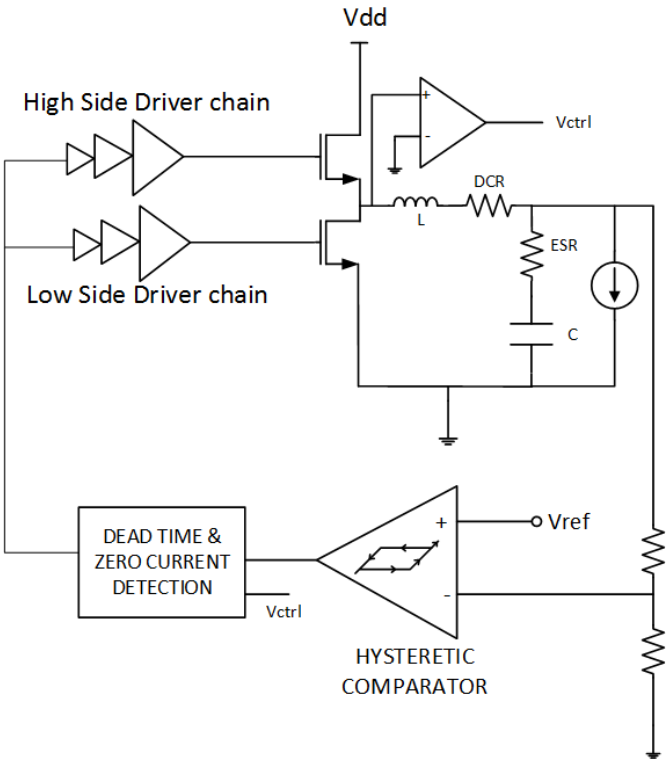

Figure 4: Hysteretic Comparator architecture

The working of this PFM architecture can be explained as follows. If the output goes lower than the lower threshold voltage, the comparator trips and turns on the upper MOSFET. The upper MOSFET stays on till the output hits the upper threshold voltage of the comparator. The comparator trips again and turns off the upper MOSFET and turns

on the lower MOSFET after a dead time. As this is a synchronous buck architecture, zero current detection is required to prevent negative current i.e. current from the load to the switches. The basis for this negative current and implementation of the zero current detector is discussed in Section 3.5. The ripple in this architecture is decided by the hysteresis band.

While the hysteretic PFM is simple to implement, as only a hysteretic comparator is needed, its efficiency at extremely light loads (in the order of μA's to 10's of mA's) is reduced, as there is no limit put on the peak inductor current.

1.2.2 Constant on time PFM

In the constant on time architecture, the time for which the high side MOSFET is turned on is kept constant. An implementation of this shown below(Xiao, Peterchev, Zhang, & Sanders, 2004)

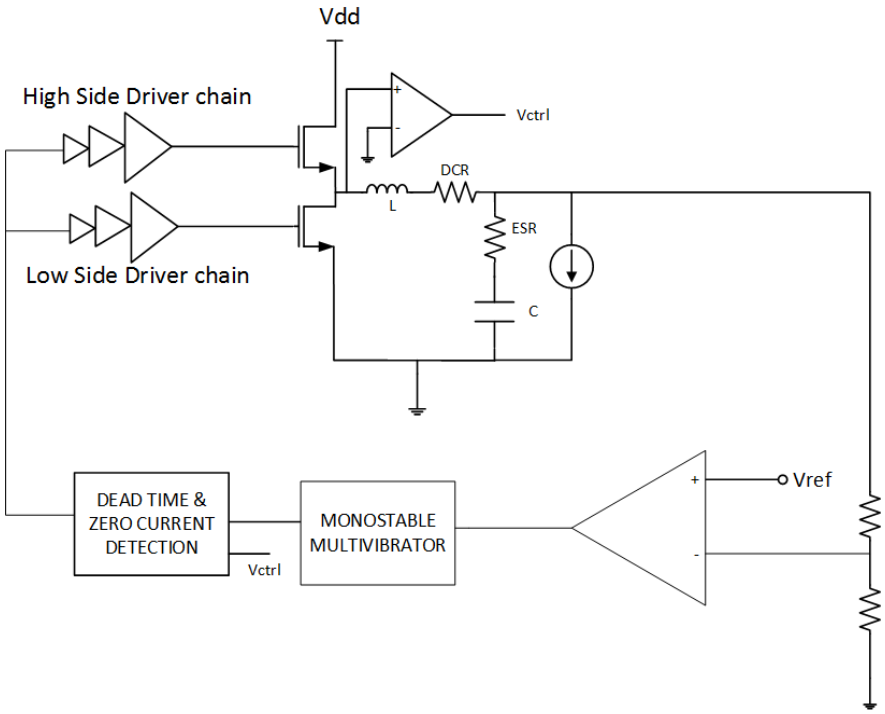

Figure 5: Constant on time PFM architecture

The element used for generating the constant on time is a monostablemultivibrator or a one shot. The one shot, as the name suggests, generates a single pulse of a defined time width in response to a trigger signal. The output of the one shot is given to a S-R latch, whose output turns on the high side FET for the fixed on time, decided by the one shot.

The on time in the constant on time cannot be kept too small, as a low on time leads to larger inductor current swings and more ripple(Wong & Man, 2008)

The minimum on time is decided by the equation

$$t_{on\_min}^2 \left(\frac{Vin - Vref}{2LC}\right) + t_{on\_min} \left(\frac{(Vin - Vref) * ESR}{L} - \frac{Iout}{C}\right) - Vhyst = 0$$

If on time is kept below this value, pulse bursting occurs as is seen in the figure below

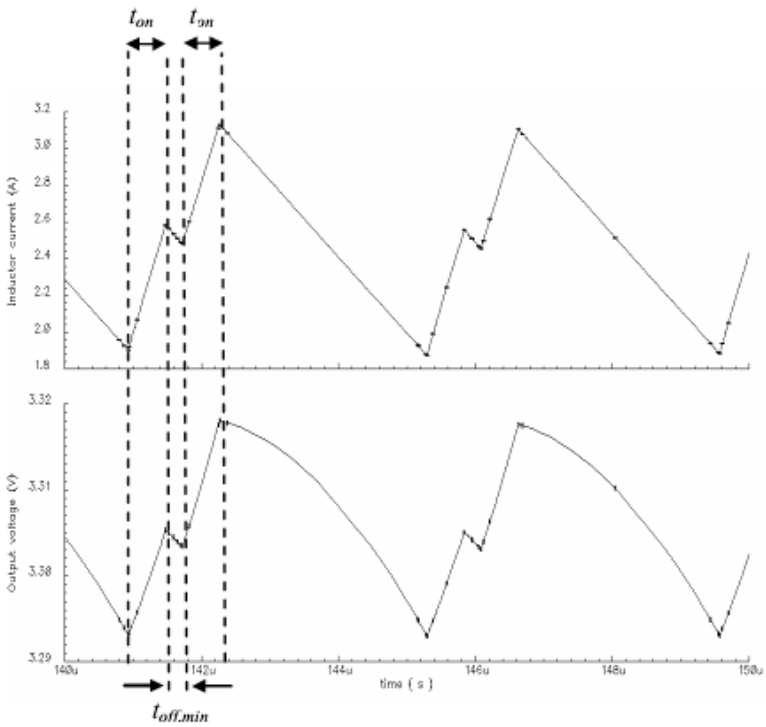

Figure 6: Pulse bursting in COT converters

1.2.3 Multi Pulse PFM

Both constant on time and hysteretic control replenish the charge lost in the output capacitor with a single pulse. However, the peak inductor current is not limited in both these architectures. If PFM is implemented with an upper limit on the peak inductor current, multiple pulses are required to charge the output capacitor. These pulses increase with increasing load current. This architecture is popularly known as Burst Mode PFM or Pulse skipping(Angkititrakul & Hu, 2008). An implementation of this architecture is shown below

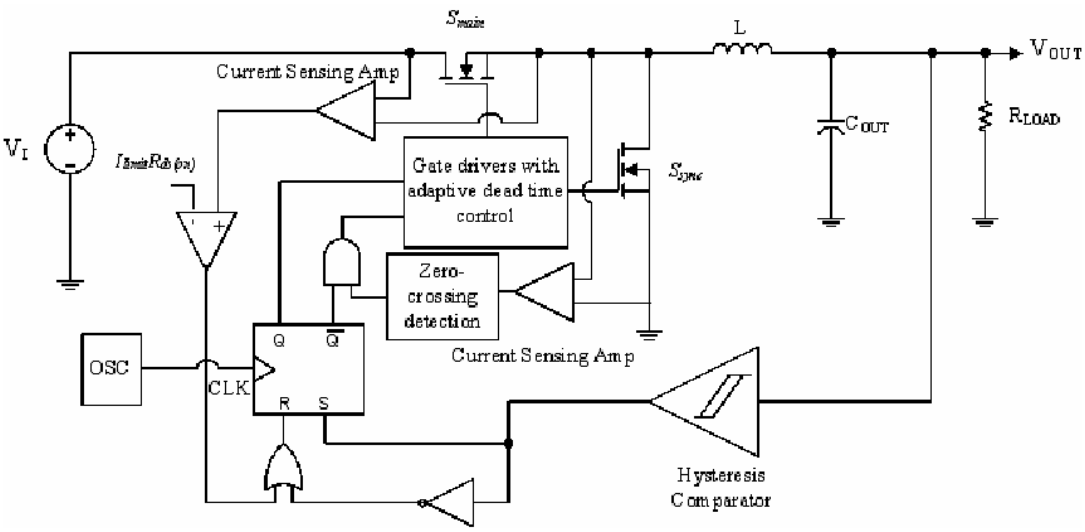

Figure 7: Pulse skipping architecture

The current sense amplifier senses a voltage proportional to the peak current and gives compares this to a voltage proportional to the current limit. When the inductor current exceeds the this limit, the high side MOSFET switches off and low side MOSFET is turned on to discharge the output capacitor, till the inductor current becomes zero and both switches are turned off. The output capacitor now discharges through the load, and a higher load leads to more pulses.

The waveforms for this multi pulse architecture are shown below for two load currents, 50mA and 180mA respectively.

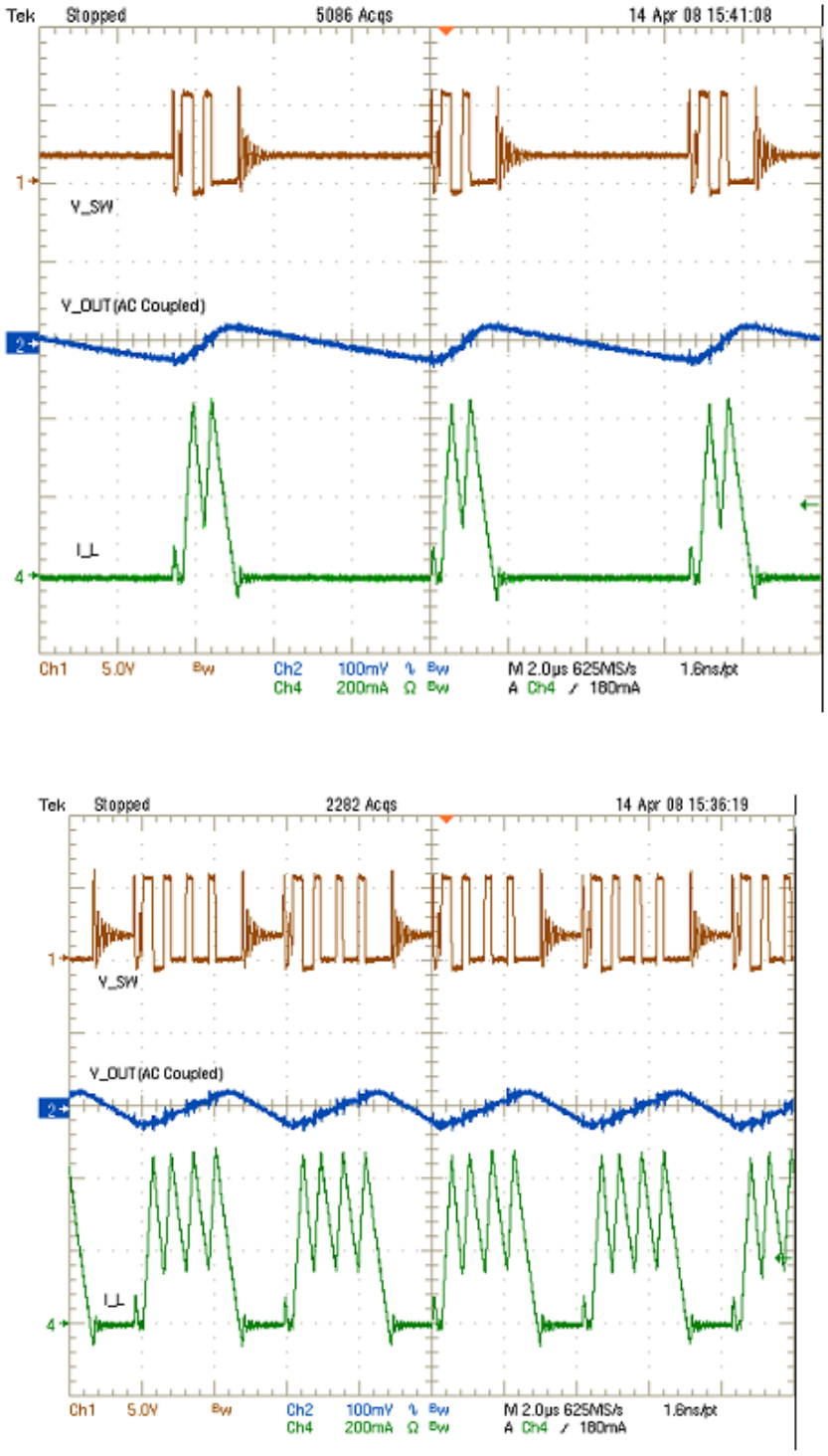

Figure 8: Pulse skipping waveforms

1.3 Thesis organization

After reviewing the architectures mentioned above, the hysteretic PFM architecture is chosen for implementation, as it is simple to implement and does not suffer the pulse bursting problem of the constant on time PFM. The top level diagram of the PFM block implemented in this research is shown below

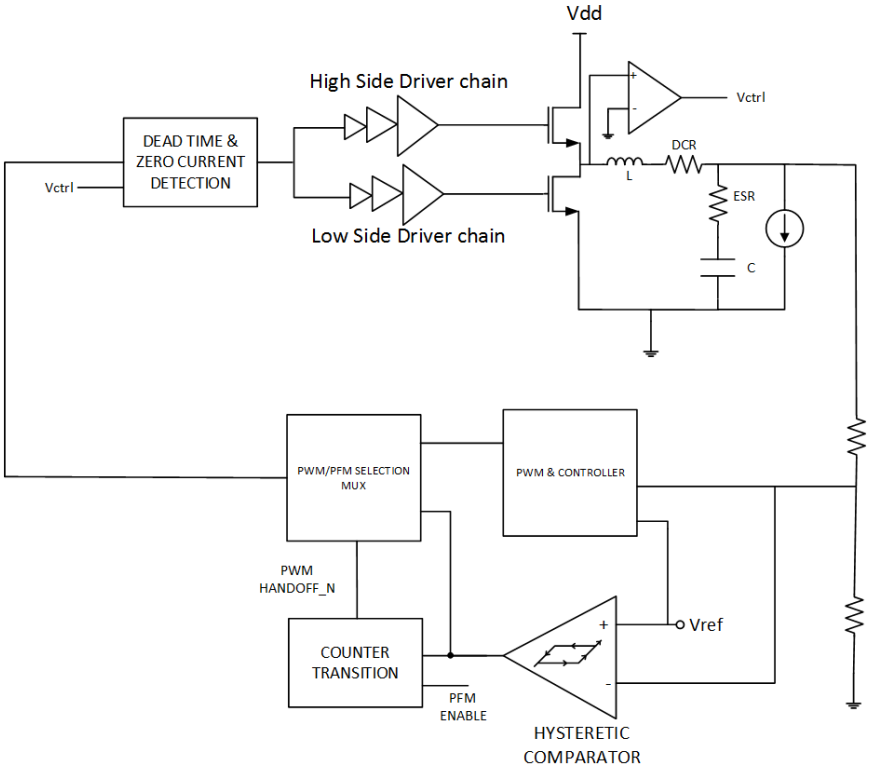

Figure 9: Top level View of PFM architecture

The following sections discuss the various components in this architecture. Chapter 2 surveys the various automode transition techniques available to transition from PFM to PWM. Chapter 3 discusses the implementation of the .various blocks shown in the figure above as well as the derivation of the operating frequency. Chapter 4 presents the results from cadence implementation of the solution. Chapter 5 concludes the research and suggests future improvements

2 Survey of auto mode transition techniques

The pulse frequency modulation loop and the pulse width modulation loop are used as two independent loops to have a high efficiency over a wide range of load currents. The control can be handed over to the pulse frequency modulation loop, when the average dc current drops below a predefined threshold. However the same average current sensing cannot be used to switch from the PFM to PWM loop. In this section, circuits which are used to automatically transition from PFM to the PWM loop are discussed

2.1 High Efficiency DC-DC Converter with Auto-mode Transition

The block diagram(Shin, Heo, Ko, & Park, 2010) shows the DC-DC converter composed of a PFM controller, a PWM controller, switch transistors, a loop filter, and a mode selector

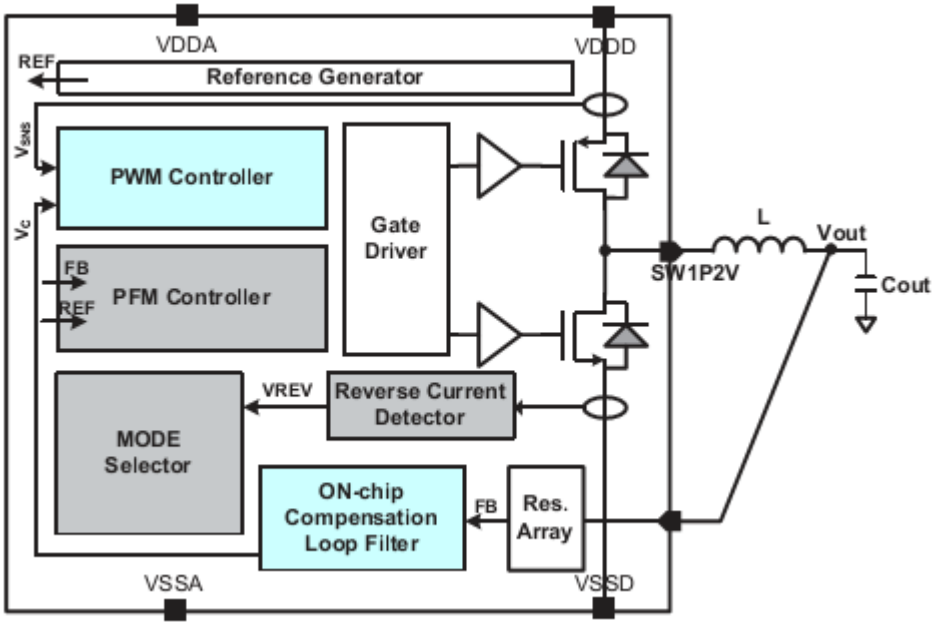

Figure 10: Block diagram of Hybrid PWM-PFM architecture

The PFM architecture here is implemented through hysteretic control, where the output voltage is compared to an upper threshold and lower threshold voltage as shown in Figure 11. When the voltage is below the lower threshold

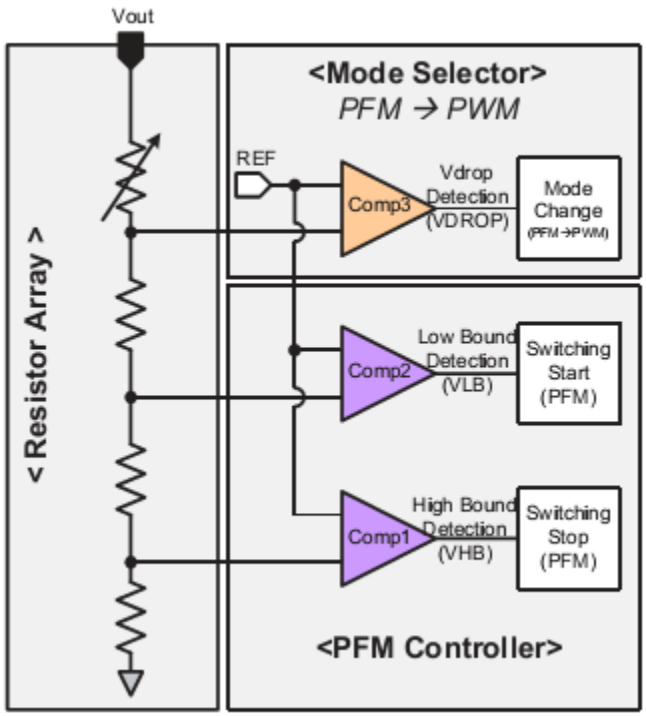

Figure 11: PFM architecture and Detection circuit

The transition circuit is shown above represented by Comp3.The basis for the detection is as follows. As the load current increases and the loop needs to transition to PWM, the output voltage drops and becomes lower than a threshold voltage, switching the output of the comparator Comp3.

The disadvantage of the techniques is use of a tunable resistor array to generate the threshold. As the resistors need to have a large value to limit the current leakage, they would occupy significant layout area when integrated on chip.

2.2 Fast Mode-Switching Technique in Hybrid-Mode Operation

The synchronous regulator here is .realized using a current mode control along with the voltage mode control(Chen, Hsieh, Huang, & Chen, 2008). The entire PWM/PFM configuration for the converter is shown below

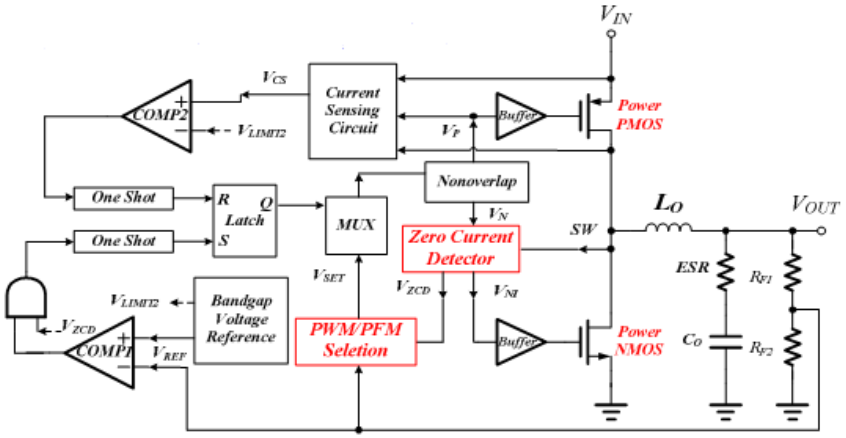

Figure 12: Current mode PWM/PFM architecture

The PFM loop is realized through constant on time control. The working is as follows.

The Comparator COMP1 along with the zero current detector (signal Vzcd) generate a triggering signal for the one shot, which turns on the high side PMOS through the SR latch (S=1 & R=0). As the inductor current increases it hits the current limit and latch gets reset (R=1 & S=0). The inductor current decreases and once it hits zero, both FET's are turned off to prevent switching losses.

The transition from PFM to PWM loop is done by comparing the feedback to a fixed threshold as shown in Figure 13. The VPFM signal shown in the figure is an active high signal, which is high when the system is working

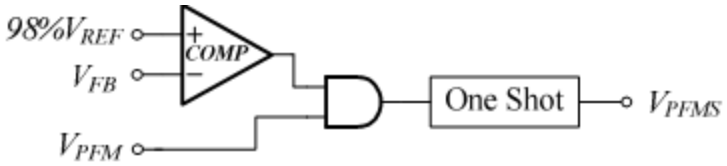

Figure 13: PFM-PWM transition using one shot

When the feedback voltage drops below 98% of the Reference voltage, and the system is operating in PFM i.e. VPFM=1, the one shot triggers through the AND gate and generates a pulse with a finite on time, VPFMS.The rising edge of this signal is used to trigger the transition from PFM to PWM.

The disadvantage of this technique is the generating a voltage which has a different value than the reference voltage. This also limits the programmability of the threshold for PFM to PWM transition.

2.3 Auto Mode transition using SENSEFET current sensing

In this architecture, three modes are used to enhance efficiency for various load ranges. The block diagram of the tri mode buck converter is shown below(Huang, Chen, & Kuo, 2007).

The converter uses PWM, PFM and a dither skip mode, in which the pulses are dithered to reduce output ripple. The PFM in this converter is implemented using a hysteretic comparator. The comparator is only powered in the PFM mode and shut down in the other two modes, to reduce losses. The converter also utilizes optimum width switching, where the width of the power MOSFET is changed, to get higher efficiencies

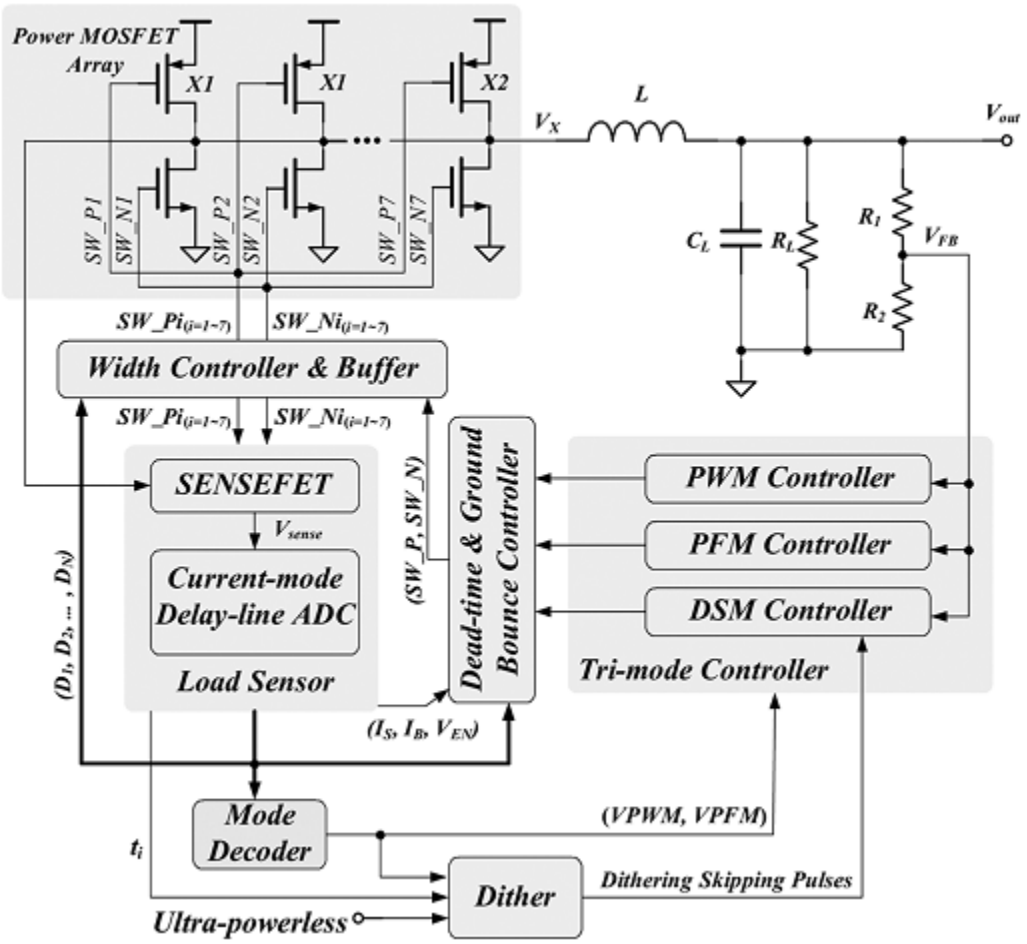

Figure 14: Tri Mode Buck Converter

For the transition between different modes, the peak load current is sensed using a SENSFET as shown below

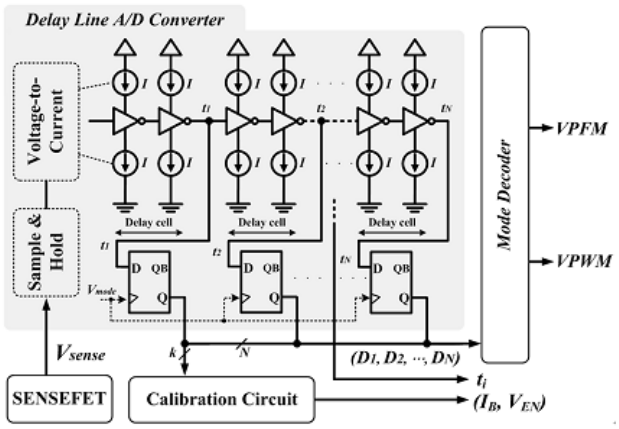

Figure 15: SENSEFET based auto transition

The SENSEFET voltage Vsense is proportional to the load current and has a peak value given by

$$Vsense_{peak} = \frac{R_{sense}}{1000} * Iload + \frac{\left(1 - \frac{Vin}{Vout}\right) * R_{sense}}{2000 * L * f} * Vout$$

Where Rsense is the sense resistor expressed in ohms.

The sensed voltage is sample and held to get the peak voltage. This voltage is converted into a current using a V-I converter, which drives a delay line based A/D converter. The code given out by the A/D converter is decoded, on basis of which a decision is made on the mode of operation, to achieve the highest efficiency.

As this system uses a SENSFET based current sense, it is only useful when the power MOSFET's are on the same die as the other signal processing circuits.

For the converter, discussed in this research, the power FET's are external to the die. Also there is only one reference voltage in the chip, which makes the voltage comparison method infeasible.

Therefore an indirect estimation of load current is done using a digital technique, which does away with the need for current or voltage sensing and can be integrated with systems with either an internal or external power MOSFET.

3 Design, Modeling and calculations

3.1 System Modeling using PLECS™

The Pulse frequency modulation loop is implemented using a simple hysteresis comparator and zero current detector. The hysteretic comparator can be modeled using a window comparator and a SR flip flop which is required for memory. The modeling of hysteretic comparator is shown below

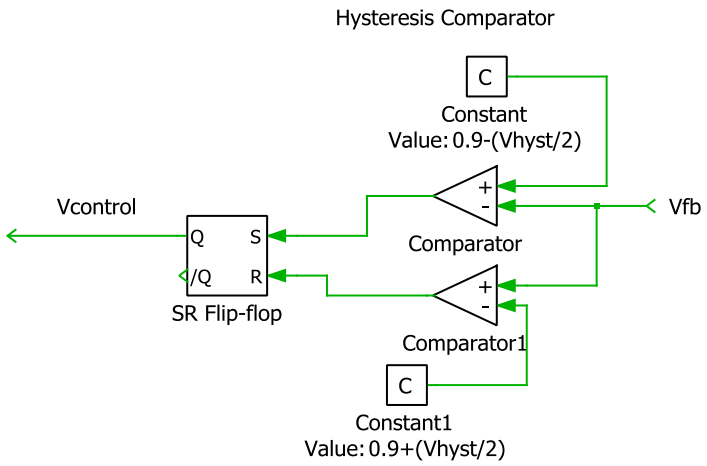

Figure 16: Hysteretic comparator ideal model

The comparator can be represented mathematically by the following equation

$$Vout = \begin{cases} Vdd, & Vin < Vltp \\ 0, & Vin \geq Vutp \end{cases}$$

Where Vltp&Vutp are the lower and upper triggering points for the comparator

The memory of the comparator i.e. preserving its previous state is represented by an S-R latch

This together with the zero current detector, which prevents the flow of inductor current in the negative direction in the low side MOSFET, form the PFM loop

The system modeled in PLECS is shown below

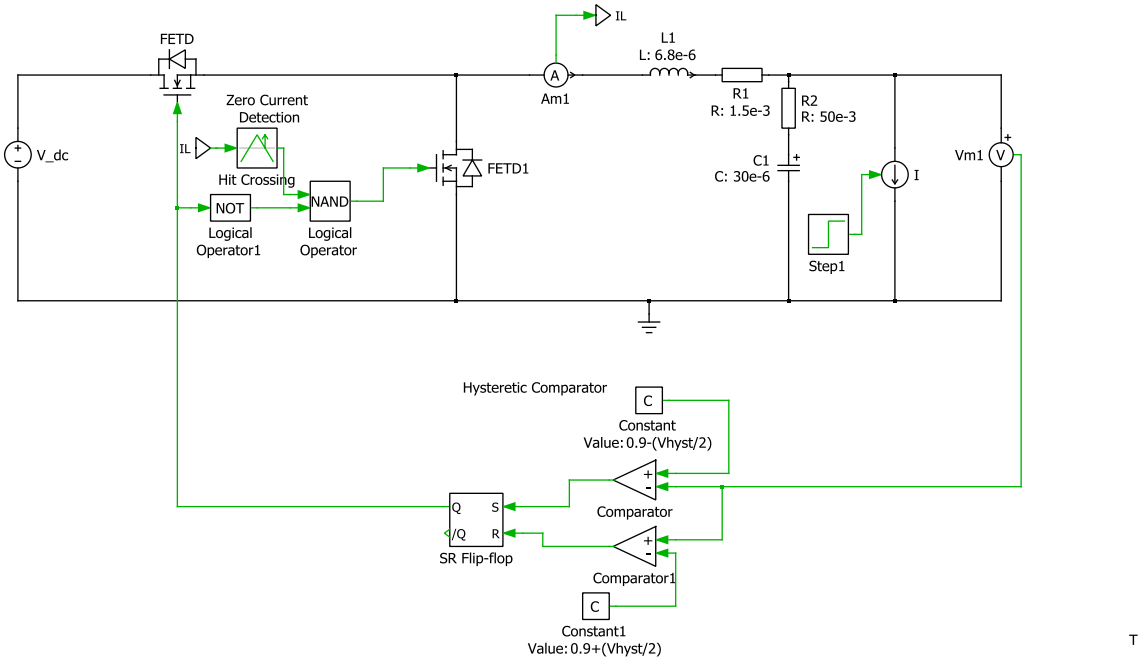

Figure 17: Ideal Model for hysteretic PFM

The waveforms of the ideal model are as follows

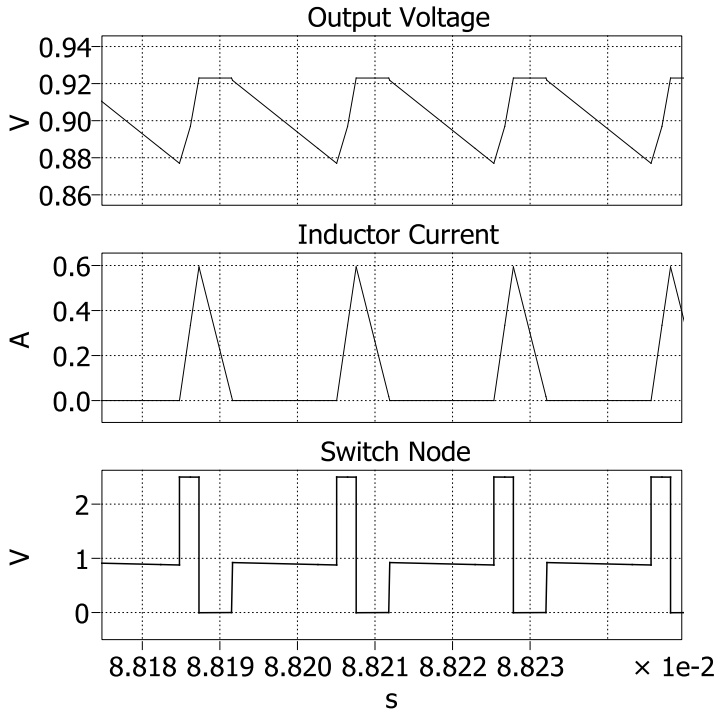

Figure 18: Plotted waveforms from ideal model

3.2 Derivation for Operating frequency

As the frequency of switching is being modulated to achieve a higher efficiency at lower currents, the frequency has to be derived using basic current voltage relationships for the inductor and capacitor. The derivation is as follows

The inductor current waveform in the PFM mode of operation is shown below

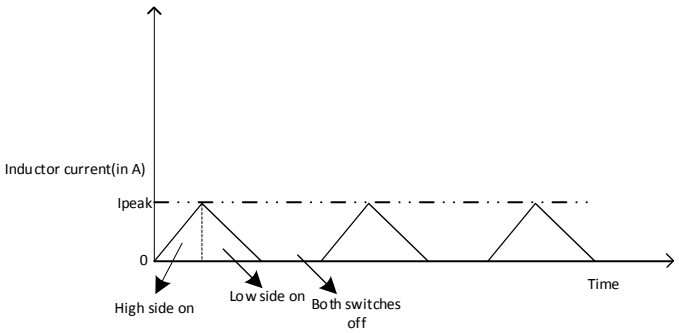

Figure 19: Inductor current in PFM operation

The inductor current equation, when the high side MOSFET is on can be written as

$$IL(t) = \frac{Ipeak}{Ths} * t \quad 0 \leq t < Ton$$

Where Ths is the time when the high side switch is on

From inductor Volt second balance we know that

$$\frac{Ipeak}{Ths} = \frac{Vin - Vout}{L}$$

Where Vin is the input voltage to the buck converter, Vout is the output voltage and L is the value of the inductor being used

Thus the inductor current during the high side on time can be rewritten as

$$IL(t) = \frac{Vin - Vout}{L} * t \quad 0 \leq t < Ton$$

The current through the output capacitor is simply the load current removed from the inductor current. This is shown in the figure below

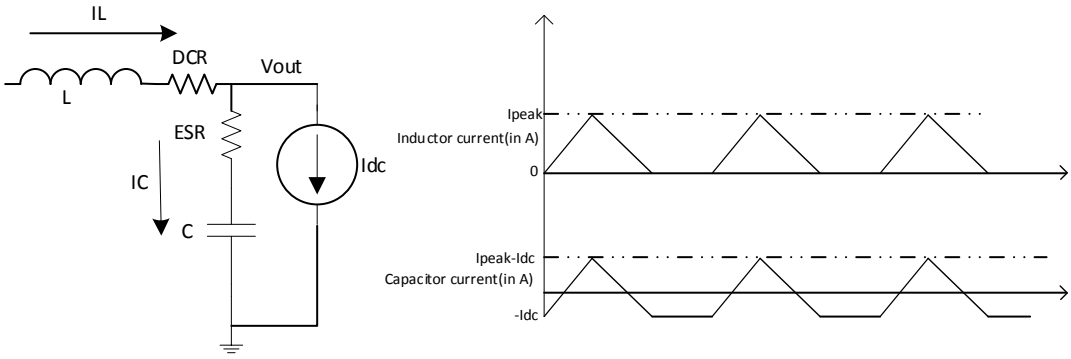

Figure 20: Current in output capacitor

The current in the capacitor is therefore written as

$$IC(t) = IL(t) - Idc$$

$$=> IC(t) = \frac{Vin - Vout}{L} * t - Idc \;\; 0 \leq t \leq Ths$$

The output voltage can be written as

$$Vout(t) = Vc(t) + VESR(t)$$

$$=> Vout(t) = \frac{1}{C} * \int IC(t)dt + (IC(t) * ESR) \;\; 0 \leq t \leq Ths$$

Due to use of a hysteretic control, the output voltage is allowed to change between the hysteresis band set by the comparator

$$Vout(Ths) - Vout(0) = Vhyst$$

$$Vhyst = VLTP - VUTP$$

Where the UTP and LTP are the upper and lower triggering point voltages for the comparator respectively.

The expression for output voltage can be rewritten after substituting for IC (t) and integration as

$$Vout(t) = \frac{1}{C}\left(\frac{Vin - Vout}{2 * L} * t^2 - Idc * t\right) + \left(\frac{Vin - Vout}{L} * ESR * t - Idc * ESR\right) + k$$

Where k denotes the constant of indefinite integration

$$=> Vout(0) = k - Idc * ESR$$

$$Vout(Ths) = \frac{Vin - Vout}{2LC} * Ths^2 \; + Ths\left(\frac{Vin - Vout}{L} ESR - \frac{Idc}{C}\right) + k - Idc * ESR$$

Thus subtracting these two expressions and equating it to the hysteresis band we get

$$Vhyst = \frac{Vin - Vout}{2LC} * Ths^2 \; + Ths\left(\frac{Vin - Vout}{L} ESR - \frac{Idc}{C}\right)$$

$$=> Ths^2\left(\frac{Vin - Vout}{L}\right) + Ths\left(\frac{Vin - Vout}{L} * C * ESR - \frac{Idc}{C}\right) + C * Vhyst = 0$$

The on time of the high side switch can be obtained by solving this quadratic equation

The peak current can also be determined from this on time as

$$Ipeak = \frac{Vin - Vout}{L} * Ths$$

The time for which the low side switch is on can be determined from volt second balance for the inductor

$$(Vin - Vout) * Ths = Vout * Tls$$

$$Tls = Ths * (\frac{Vin}{Vout} - 1)$$

From the inductor current waveform, the average value of the waveform is the total dc current flowing in the load

$$Iload = \frac{AreaunderI - tcurve}{Totaltimeperiod}$$

$$AreaunderI - tcurve = 0.5 * Ipeak * (Ths + Tls)$$

$$Totaltimeperiod = \frac{0.5 * Ipeak * (Ths + Tls)}{Iload}$$

Substituting for Tls and Ipeak we get

$$Totaltimeperiod = \frac{Ths^2 * Vin * (Vin - Vout)}{2 * Iload * Vout * L}$$

$$OperatingFrequency = \frac{1}{TotalTimeperiod} = \frac{2 * Iload * Vout * L}{Ths^2 * Vin * (Vin - Vout)}$$

Thus an expression for operating frequency in PFM is derived. It can be seen here that operating frequency is directly proportional to the DC load current.

The expected waveforms for this operation are as follows

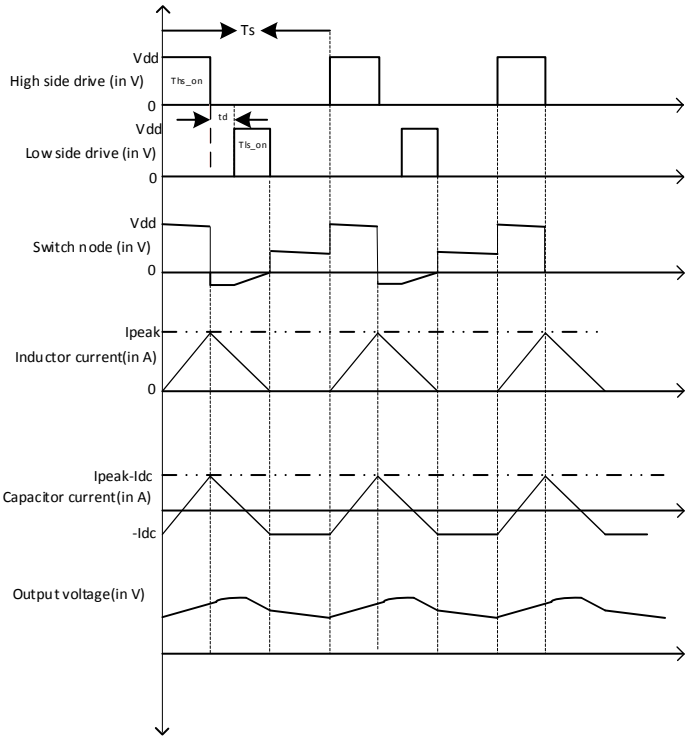

Figure 21: Waveforms for PFM operation

3.3 Hysteretic stage design for comparator

The controller in the presented PFM architecture is a hysteretic comparator. The hysteresis is implemented internally as shown below.(Allstot, 1982)

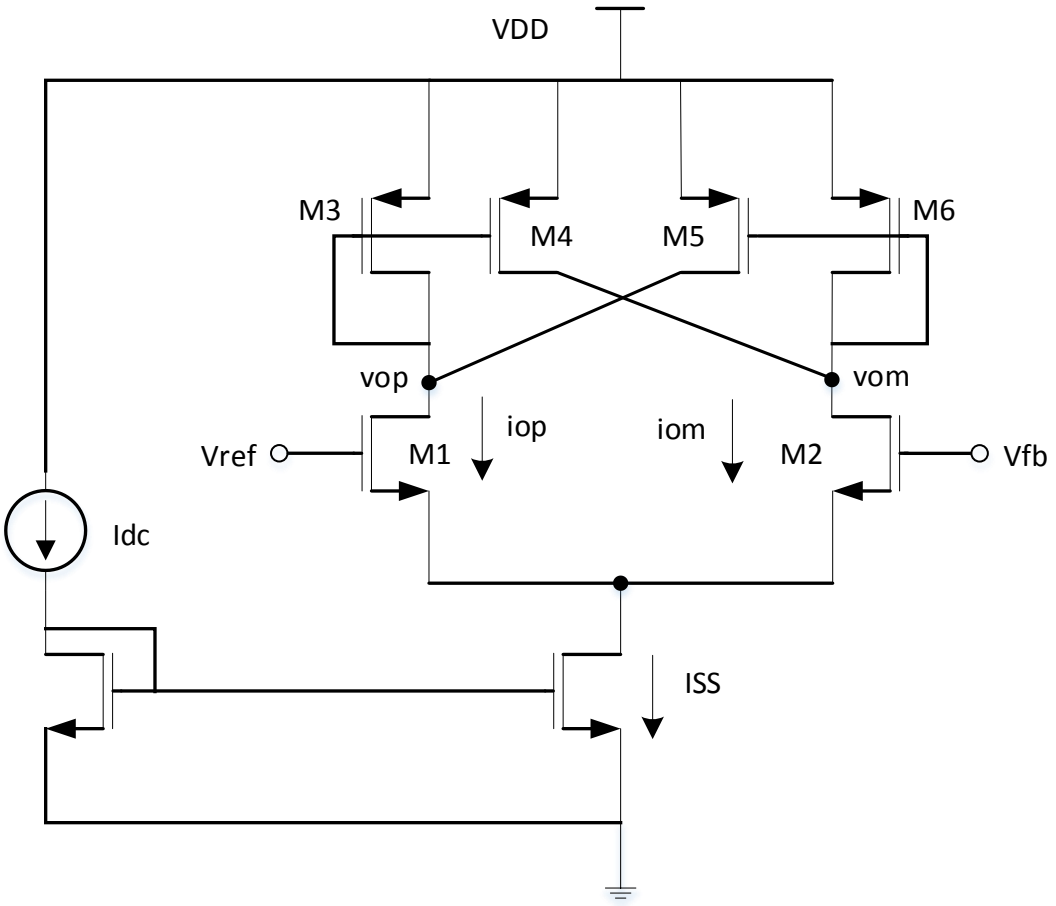

Figure 22: Internal hysteresis comparator first stage

The circuit uses positive feedback using the transistors M4, M5 to increase the gain of this stage. The working of the comparator can be explained as follows(Holberg).

If the node denoted as Vfb has a voltage much lower than the other node denoted as Vref, then the current iop would be much larger than iom.

This will make M3 & M4 in Figure 22 conduct more than M5 & M6(as the gate source voltages of M3 & M4 are set by iop while that of M5 & M6 by iom).This makes output node Vom to be set to Vdd.

As the voltage at Vfb node is increased, the current switches from one branch to the other so that iom increases while iop falls. This current iom, is sourced by M4 into M2.At the switching point where Vfb=VUTP=Vref+Vhyst/2, the output vom switches from Vdd to 0, and transistor M6 and M5 turn on, preserving the state till the input starts going down

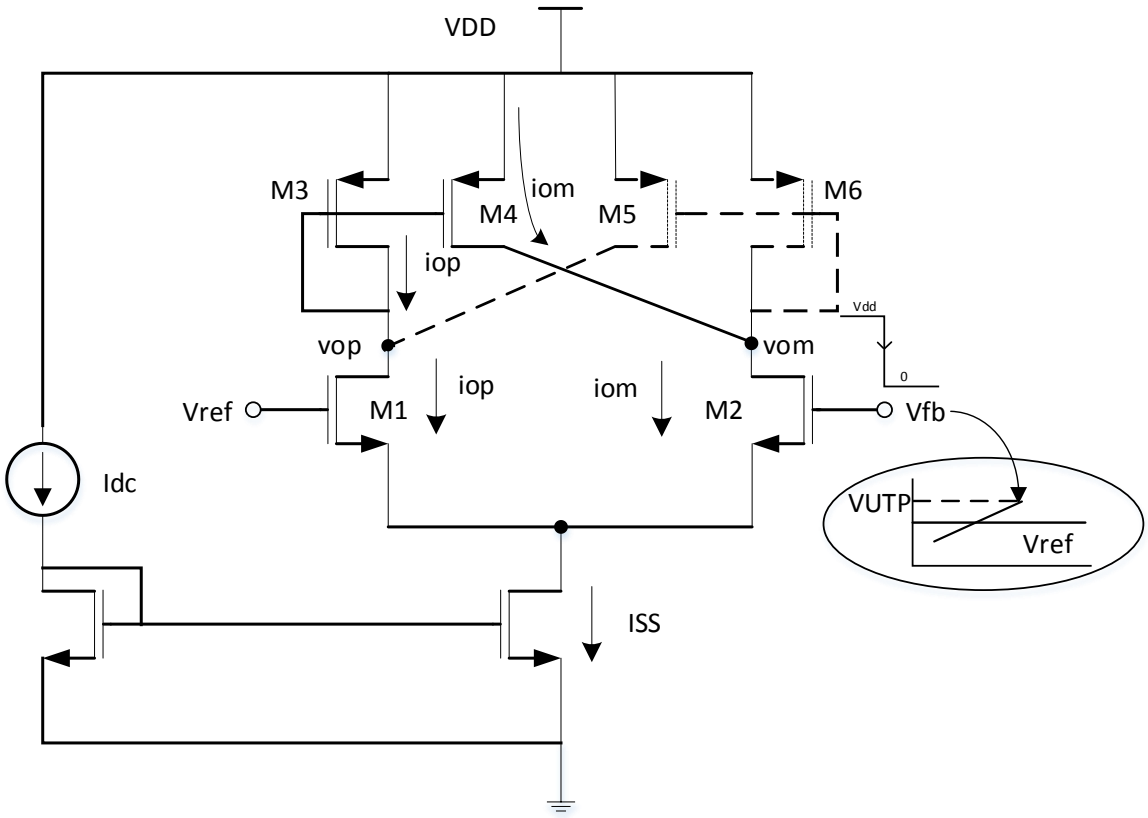

Figure 23: Hysteresis circuit when input reaches upper triggering point

A similar analysis can be done for when the voltage Vfb goes below the lower triggering point i.e. VLTP and it can be shown that the output node makes a transition from 0 to Vdd as is shown in the figure below

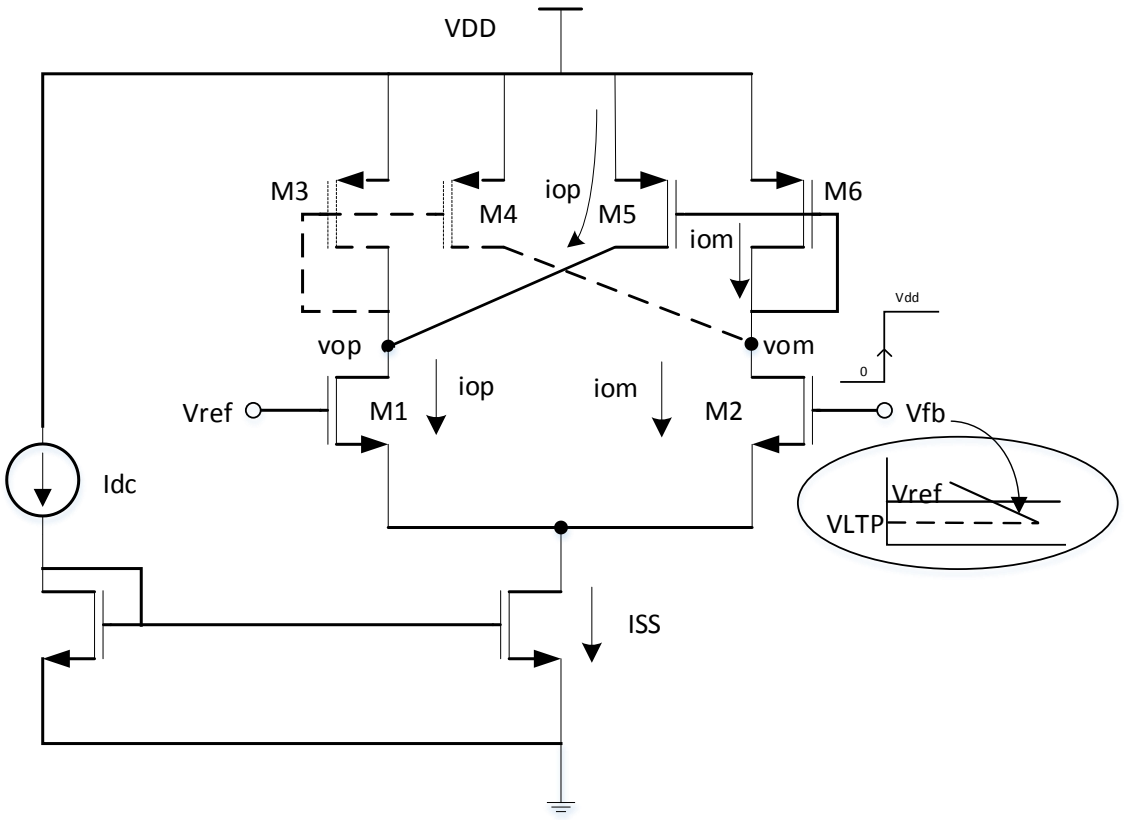

Figure 24: Hysteresis circuit when input reaches lower triggering point

3.3.1 Calculations for hysteresis band

The widths of M3 and M6 have to be set equal to each other, while the widths of M4 and M5 have to be equal to each other. Thus

$$\beta_A = \beta_{M3} = \beta_{M6}$$

$$\beta_B = \beta_{M4} = \beta_{M5}$$

When Vfb = VUTP=Vref+Vhyst/2 M3 mirrors the current in M4

$$iom = \frac{\beta_B}{\beta_A} * iop$$

The currents iom and iop can be related to the input voltages Vfb&Vref as follows

$$gm(Vfb - Vref) = iom - iop$$

$$Vfb - Vref = \frac{iom - iop}{gm}$$

Also the sum of iop and iop is ISS

$$ISS = iom + iop$$

From the previous equations hysteresis band can be rewritten as

$$Vref + \frac{Vhyst}{2} - Vref = \frac{Iss}{gm} * \frac{\beta_B - \beta_A}{\beta_B + \beta_A}$$

$$=> \frac{Vhyst}{2} = \frac{Iss}{gm} * \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1}$$

Thus the hysteresis band can be written as

$$Vhyst = \frac{2 * Iss}{gm} * \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1}$$

It can be seen from this equation that the necessary condition for hysteresis is

$\beta_B > \beta_A$ i.e.

$$\left(\frac{W}{L}\right)_{M4,M5} > \left(\frac{W}{L}\right)_{M3,M6}$$

3.4 Current mode comparator

The hysteresis stage by itself is not sufficient to generate a transition signal and needs to be connected to a comparator stage, which generates it output through a buffer. For this design, a current mode comparator is used, as it has higher speed and bandwidth compared to the conventional voltage mode comparator(Abedinpour, Bakkaloglu, & Kiaei)

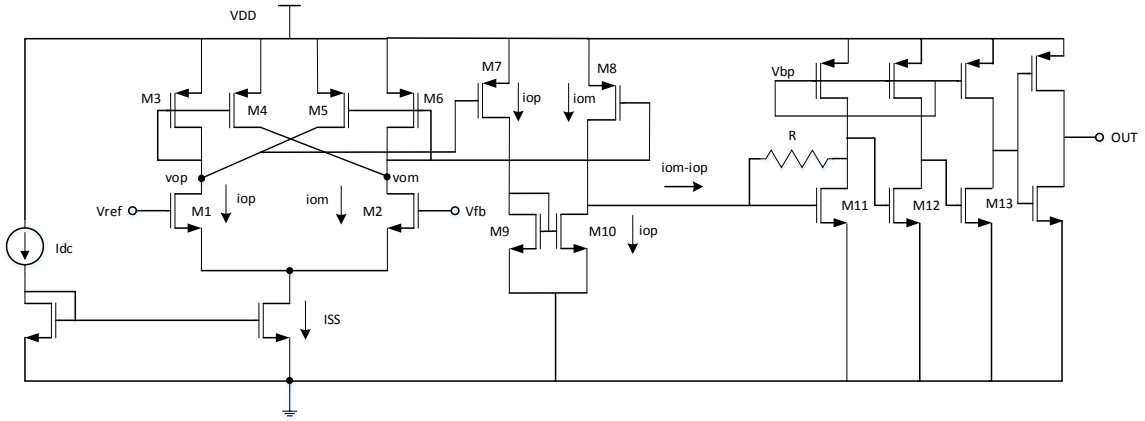

Figure 25: Current mode comparator

The current subtractor consisting of M7-M10 takes in the currents from the hysteresis stage and passes the difference to a series of common source amplifiers. The first amplifier of this series of amplifier uses a resistive feedback to reduce its input and output impedances. This reduction in output impedance reduces the voltage swing of the first amplifier, thus causing the following inverting amplifiers to be faster in the transient response. The resistor in this circuit should have a lower value to allow for a higher current to flow.(Abedinpour, Bakkaloglu, & Kiaei)

3.5 Zero Current Detector

3.5.1 Basis for circuit

In a synchronous buck converter operating at low load currents, the inductor current can flow from load to the low side switch i.e. negative direction. This can be explained as follows.

When the low side switch is turned on, the inductor current reduces. At low load currents, this eventually falls to zero. When the current in the inductor is zero, the inductor is demagnetized completely and acts like a wire with a parasitic resistance of the coil. At this point, the output voltage is higher than the voltage at the switching node. As the output and switching node are connected by a DC resistance of the inductor (since the inductor is no longer magnetized), current begins to flow from the output to the switching node. This is shown in the figures below

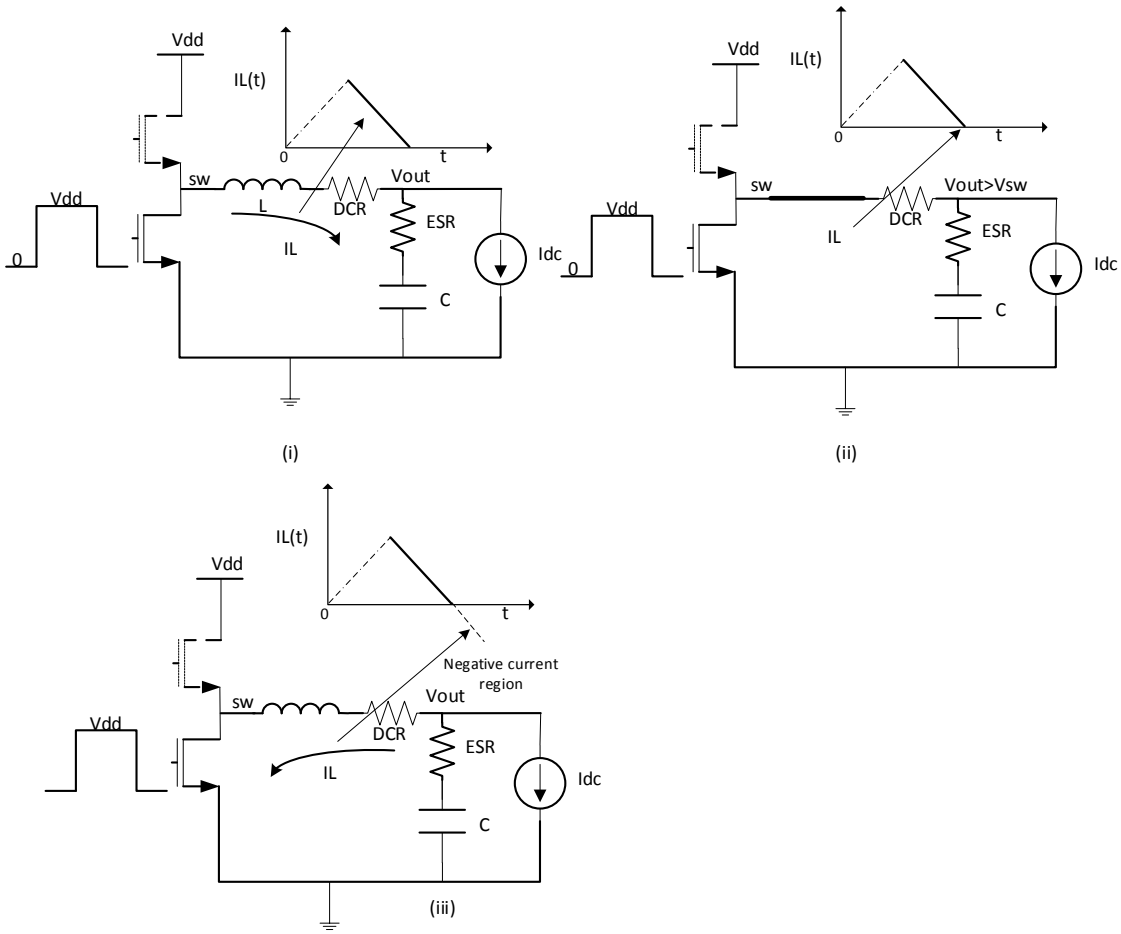

Figure 26: Cause for negative current

3.5.2 Architecture of Zero Current detector

The zero current detector detects the condition when the inductor current goes negative and turns off the low side switch. As this similar to having a diode as the low side element, which only allows the unidirectional flow of current, this is also called as Diode Emulation Mode (DEM).

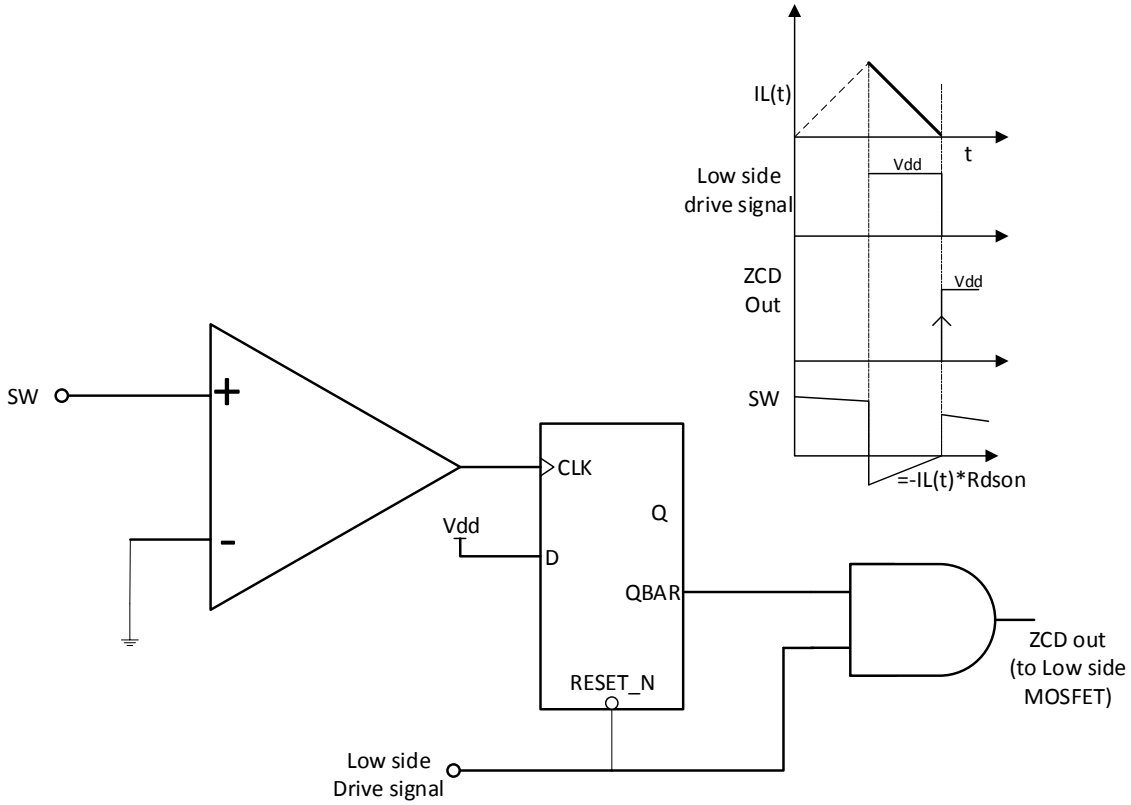

Figure 27: Zero current detector architecture

The zero current detector chain indirectly detects the zero current detection by detecting a zero voltage at the switching node. As the switching node equals

$$Sw(t) = -IL(t) * Rdson$$

the switching node voltage increases to zero as the inductor current reduces. The time instant when the zero current occurs coincides with the time instant when there is zero voltage at the switching node. If the current goes negative, the voltage at the switching node would become positive. The switching node voltage changing from positive to negative is utilized to make the zero current detector.

The output of the zero voltage comparator, which compares the switching node voltage to the ground, is used as a sampling clock for a D flip flop. The data pin of the flip flop is always pulled high. As the zero current condition needs to be detected when the low side switch is on, the flip flop is only active when the low side switch is on. It is reset, when the low side switch is off and the high side switch is on. The output of the flip flop is then ANDed with the low side drive signal so that low side switch is turned off when the output of the D flip flop goes low.

3.5.3 Zero Voltage Comparator

The zero voltage comparator is the first component in the zero current detector and detects when the switch node voltage crosses zero and becomes positive, when the low side drive signal is high. The comparator consists of three stages, a high bandwidth low gain pre amplifier stage which is followed by a series of high gain amplifier stages. The output is generated by a chain of inverters(Pai, 2010)

It can be seen inFigure 28 that a resistor Roffset has been added to the first stage. This resistor introduces an intentional negative offset in the inputs. This ensures that when the switch node is just below the ground voltage, the comparator output switches to Vdd.

The value of Roffset can be changed to increase or decrease this offset. A smaller value of Roffset will make the outputs switch when the input is a few microvolts below zero, while a larger value will make the comparator switch states when the input is a few millivolts below zero.

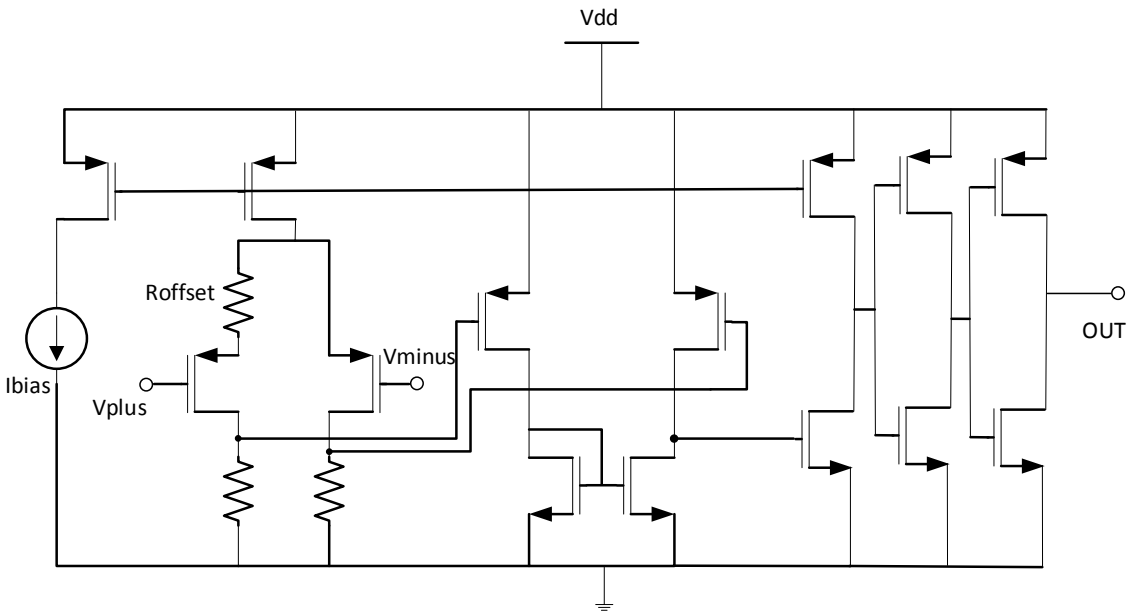

Figure 28: Zero Voltage comparator

3.6 Transition from PFM to PWM

3.6.1 Algorithm and Timing

The transition from PFM to PWM is done using a digital counter in a predefined time window. The algorithm used for this transition is shown below

For making the transition between the two loops, two signals namely PFM enable and PWM Handoff are used. As the names of the signals suggest, the PFM enable is an active high signal which switches the multiplexer input while the PWM Handoff is an active low signal, which is the output of the circuit used to make the transition from PFM to

PWM. The PWM Handoff signal controls the PFM Enable signal through a logic circuit, which takes the low going edge of the PWM Handoff signal as a trigger and after a predefined delay makes the PFM enable signal low.

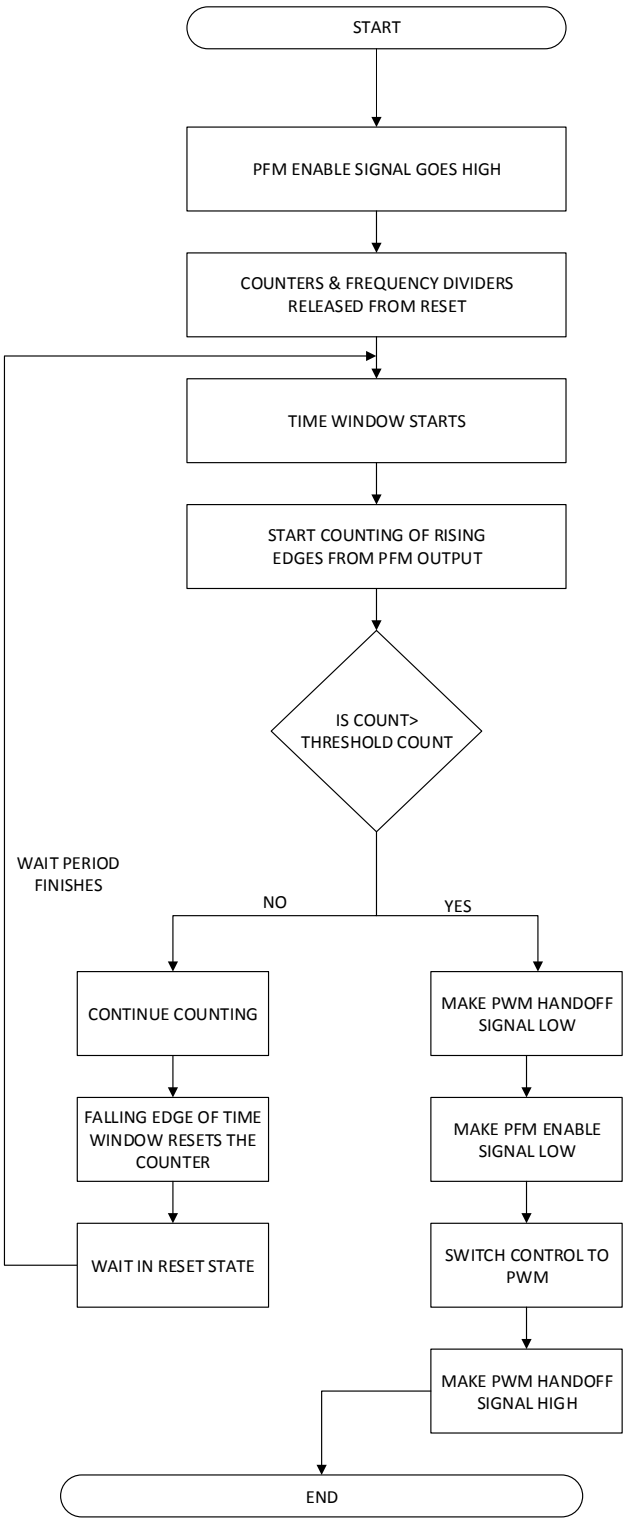

Figure 29: Algorithm for PFM to PWM transition

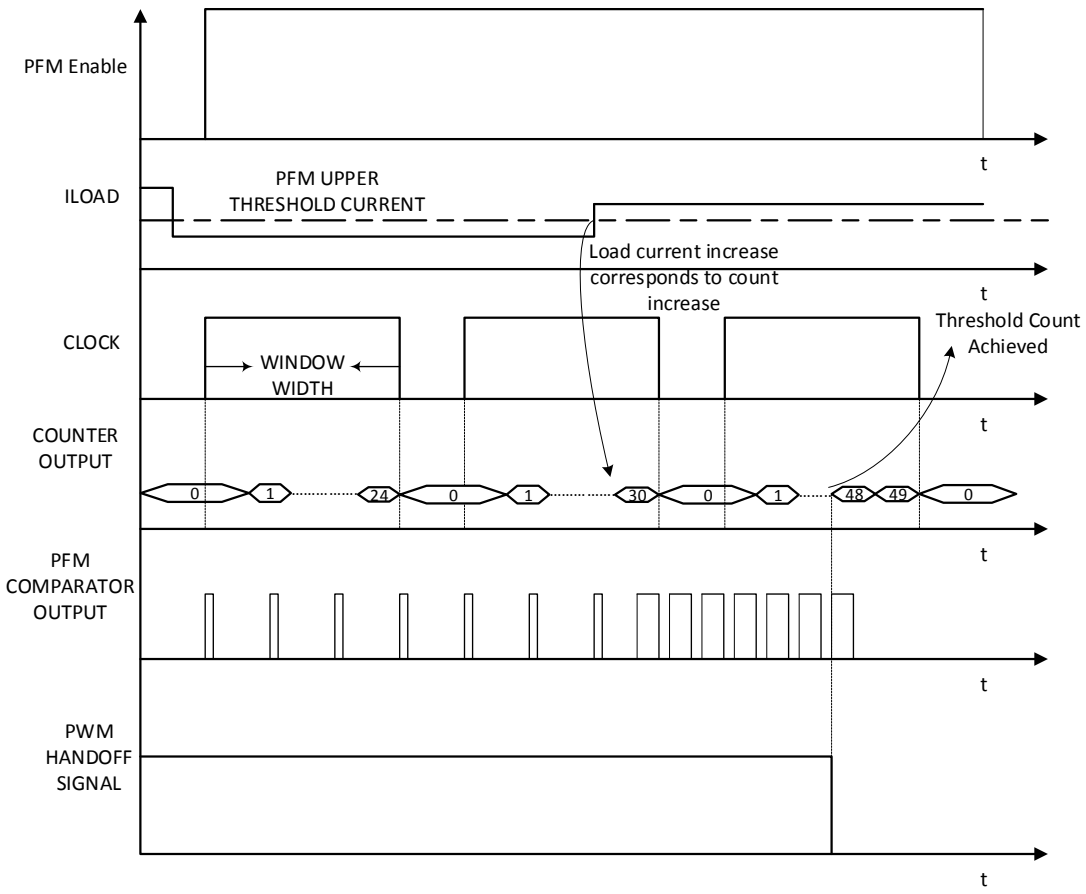

Figure 30: Timing waveforms for Transition circuitry

It can be seen from the above waveforms that a falling edge of the clock signal resets the counter and the counting starts again after a wait period. When the load current increases above the PFM upper threshold, the final count achieved increases. As it is seen, if this current increase does not make the count reach the threshold count in the first cycle, it can be captured in the next cycle of counting.

3.6.2 Implementation of logic circuit

The digital circuit implemented from the algorithm is shown in the figure below. It consists of a 6 bit counter, a clock divider & a comparator.

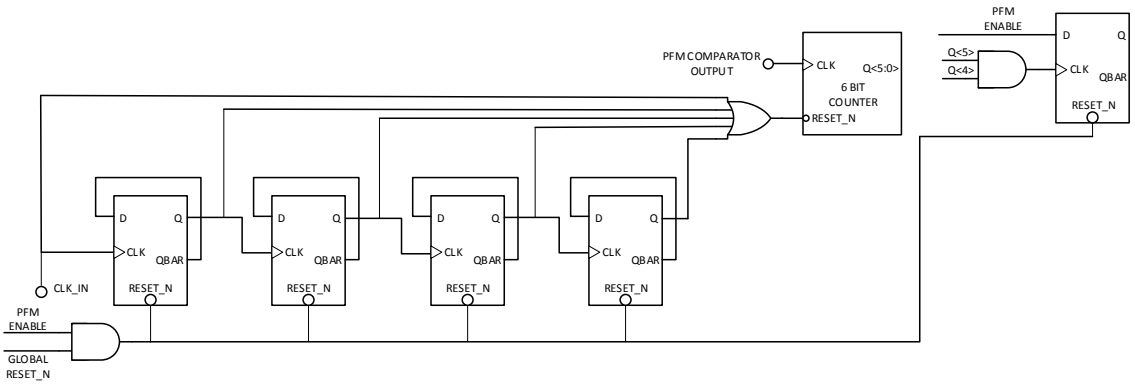

Figure 31: Logic Circuit for Transition

If the time period of the input clock is Ts, which is a 50% duty cycle clock, then the output of the clock divider after the OR Gate is given by

$$Ts_{output} = 8 * Ts + 4 * Ts + 2 * Ts + Ts + \frac{Ts}{2}$$

3.6.3 Calculations for Threshold Count

The following are the input conditions for which the threshold current for PFM-PWM transition is calculated

PARAMETER	VALUE
Input voltage	5V
Output Voltage	0.9V
Output Inductor	6.8µH
Output Capacitor	30µF
Equivalent series resistance (ESR)	45mΩ
Switching Frequency in PWM	1MHz
Hysteresis Band	46mV

Table 1: Parameters for calculation of threshold current for PFM to PWM

The current for which the transition occurs should be such that the inductor current in PWM cannot be negative i.e.

$$Iload_{Transition} \geq \frac{\Delta I_L}{2}_{inPWM}$$

$$\Delta I_L = \frac{Vout * (Vin - Vout)}{Vin * fsw_{PWM} * L}$$

Substituting the values from Table 1 we get

$$\frac{\Delta I_L}{2} = 54mA$$

The current for which the transition occurs from PFM-PWM is selected as 420mA

From the expression for total time period we have

$$Totaltimeperiod = \frac{Ths^2 * Vin * (Vin - Vout)}{2 * Iload * Vout * L}$$

$$\&Ths^2 \left(\frac{Vin - Vout}{L}\right) + Ths \left(\frac{Vin - Vout}{L} * C * ESR - \frac{Idc}{C}\right) + C * Vhyst = 0$$

Substituting the values from table in these two equations and plotting against dc load current, we obtain a plot for Time period in PFM vs. the load current

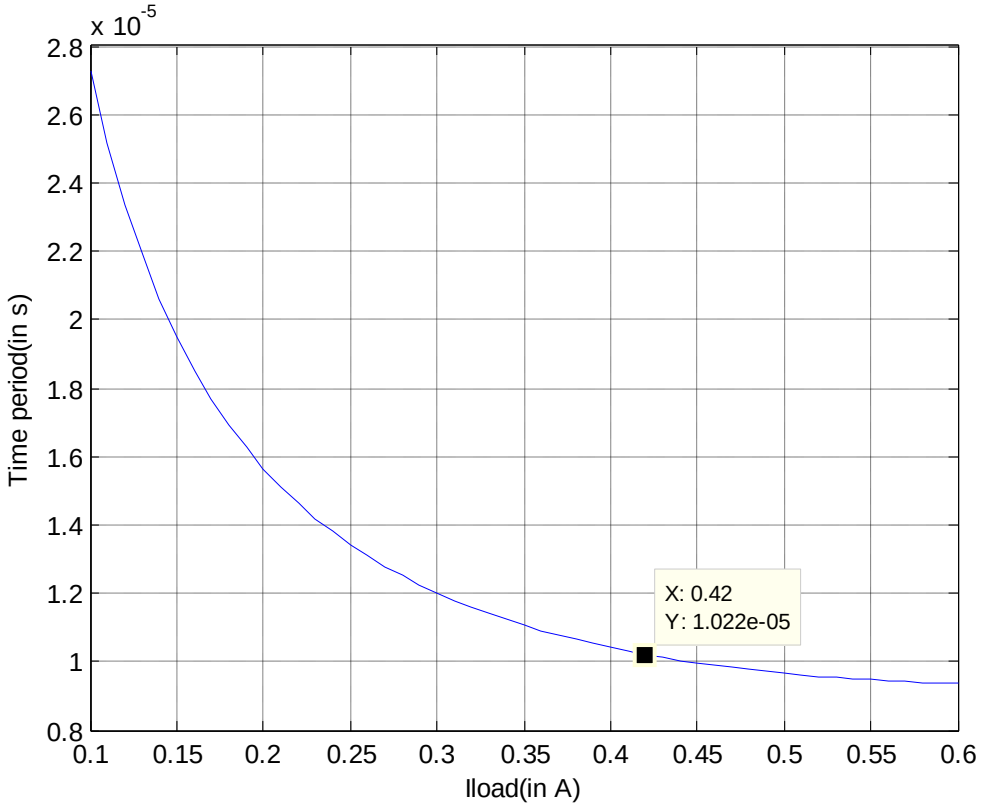

Figure 32: Time Period vs. DC load current in PFM

The calculations for the threshold count are as follows

$$Inputclocktoclockdividerchain = 1\mu s * 16$$

$$WindowTimewidth = (8 + 4 + 2 + 1 + 0.5) * 16\mu s = 496\mu s$$

$$TimePeriodfor\ 420mA = 10.2\mu s$$

$$ThresholdCount = \frac{496\mu s}{10.2\mu s} = 48$$

Therefore if the count exceeds 48, the comparator triggers and the PWM handoff signal falling edge is captured by the flip flop.

4 RESULTS

The results of post layout simulation with R+C+CC extraction is presented this section along with calculations for efficiency with the given power stage components

4.1 Layout

The layout of the PFM blocks which include the hysteretic comparator, the zero current detector, the digital blocks for automode transition are shown, The blocks which provide dead time and level shifting for driving the external power MOSFET's are also included in this layout.

The total layout area is 449µm × 189µm.

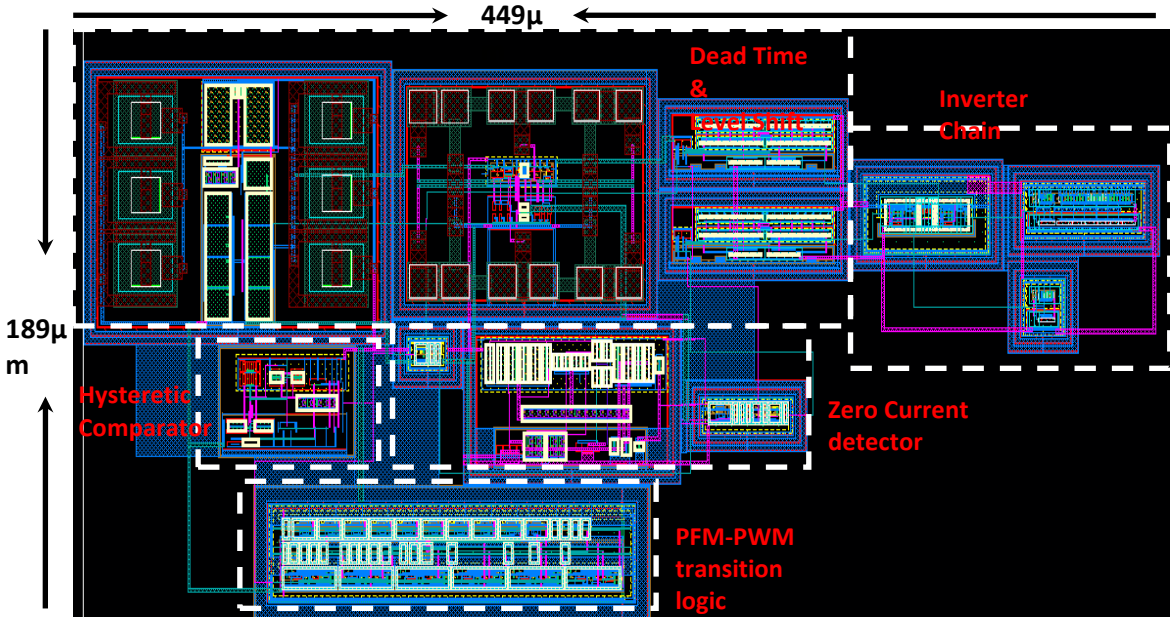

Figure 33: Layout

4.2 Hysteretic PFM results

The output of the hysteretic PFM, at 300mA of dc load current is shown below

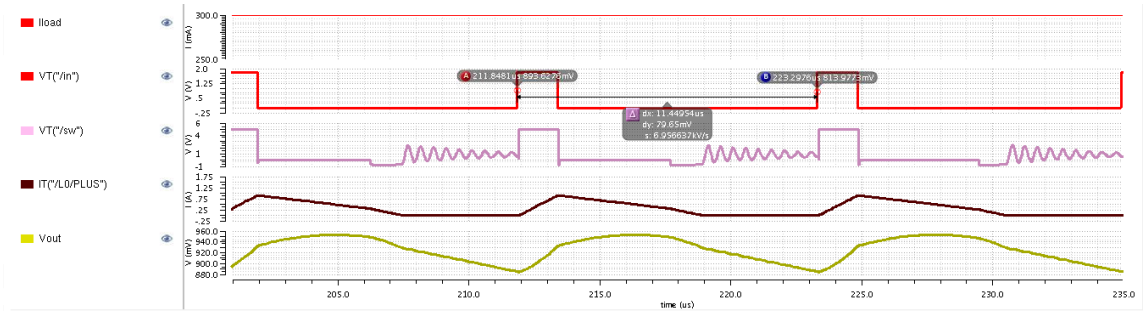

Figure 34:PFM simulated waveforms at 300mA

The three phases of PFM operation can be seen here, the high side turning on followed by the low side turning on and both FET's turning off leading to a discontinuous conduction mode. The time period of the waveform is seen as 11.45µs while that predicted by the mathematical model is 11.73µs.

The ripple of the PFM waveforms is designed to be limited by the hysteresis band. However the output voltage is seen to increase beyond the upper threshold of the hysteresis window. The hysteretic band and the total ripple are shown in the figures below

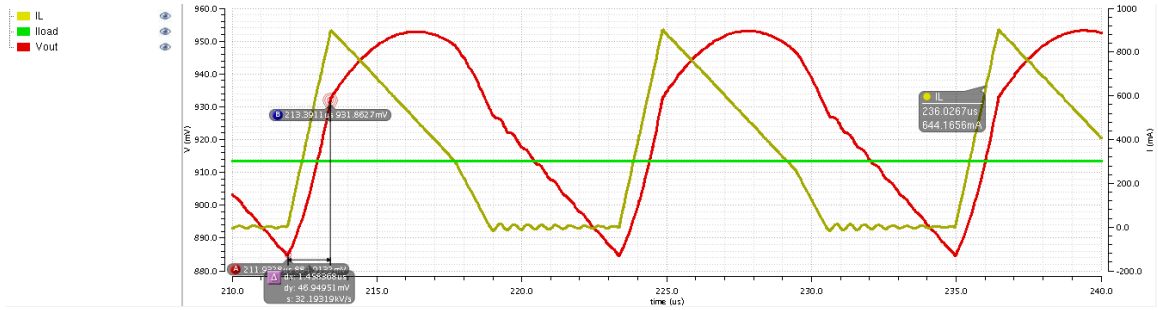

Figure 35:PFM hysteresis band in output voltage

The PFM hysteretic band of the comparator is designed to be 40mV. As the ratio of the output voltage to the feedback is 1.125, the output ripple gets scaled up by this factor and

is therefore 46mV. The hysteretic band observed from extracted simulations is approximately 47mV.

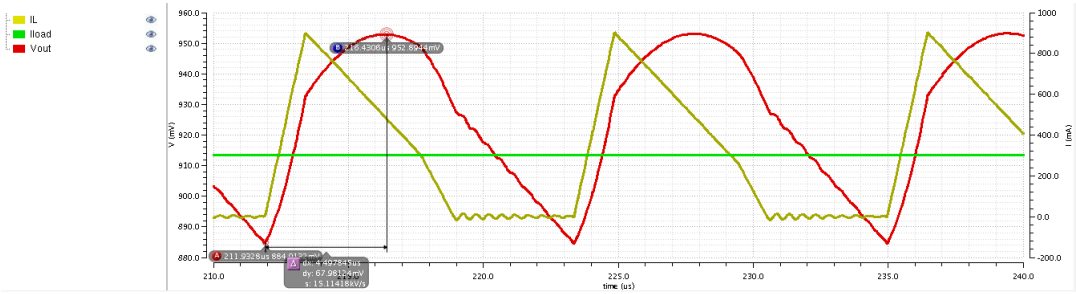

Figure 36: PFM total ripple

It can be seen in the above figure that when the inductor current decreases, the output voltage continues to rise for some time. The reason for this is as follows

The output voltage is the sum of the voltage across the capacitor and the equivalent series resistance. When the inductor current reduces, the capacitor current is still positive till the inductor current reaches the dc current. When the low side switch is on, the equations for the inductor current and the capacitor current are

$$IL_{LS}(t) = Ipeak - \frac{Vout}{L}(t)$$

$$=> IC_{LS}(t) = Ipeak - \frac{Vout}{L}(t) - Iload$$

Therefore the output voltage when the low side switch is on can be expressed as

$$Vout_{LS}(t) = \frac{1}{C}\int IC_{LS}(t)dt + IC_{LS}(t) * ESR$$

$$=> Vout_{LS}(t) = \frac{(Ipeak - Iload)t}{C} - \frac{Vout}{2LC}t^2 + (Ipeak - Iload)ESR - \frac{Vout * ESR}{L}t$$

If this equation is double differentiated with respect to time, the result is a constant negative number, which means that the voltage increases for some time after which it decreases, that is it hasalocal maxima.

Thus it is the ESR and the output capacitor which cause the output ripple to be higher than the hysteresis band.

The Hysteretic architecture has a fast transient response as the control element is a comparator, which quickly corrects for any changes in the output voltage. The transient response of the hysteretic PFM is shown for a 50% load step.

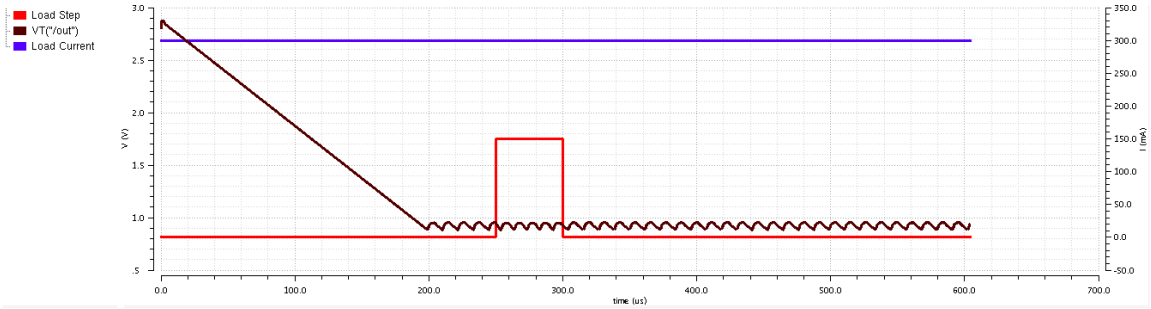

Figure 37: PFM transient response

4.3 Plot for time period in PFM

A parametric sweep of the extracted simulation results is performed by varying the load current from 100mA to 500mA with a step of 50mA. The time period is swept with the load current and is shown below

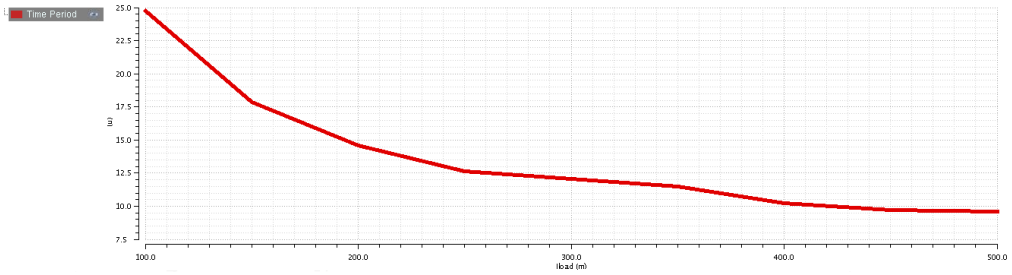

Figure 38: Time period vs. Load current in extracted simulations

The results from the extracted simulations are compared with that from the calculations done for the PFM. The graphs are superimposed and shown here

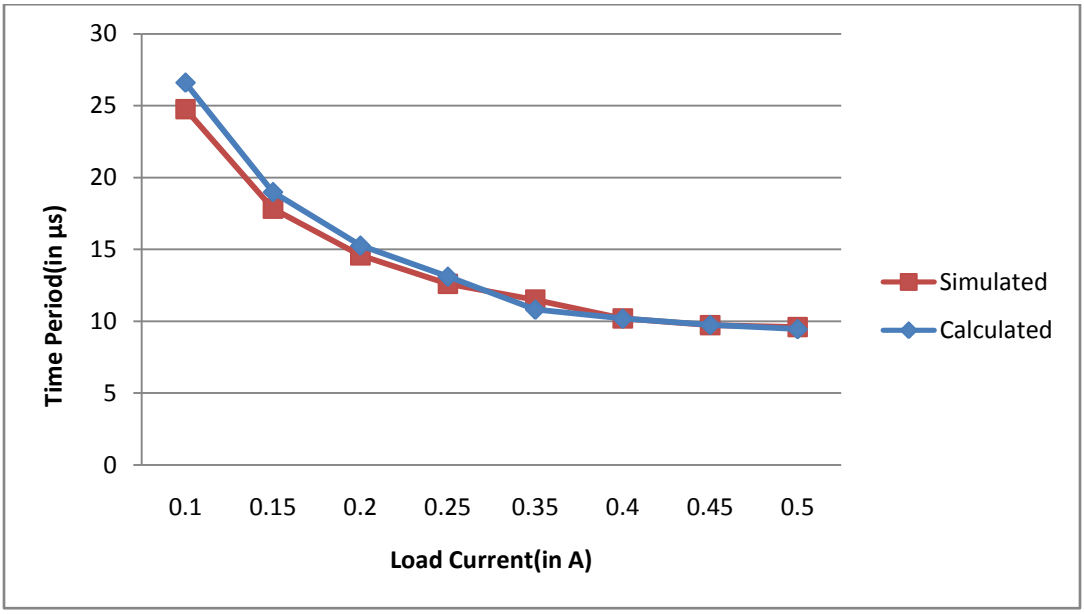

Figure 39: Simulated vs. Calculated time period values

The current for which transition from PFM to PWM is done is chosen as 400mA from these plots.

4.4 Efficiency

PFM enhances efficiency at light loads by reducing the switching losses.

The description of the loss components is as follows

1. The High side switching loss is the loss associated with the high side MOSFET when it turns on and turns off respectively.
2. The diode reverse recovery loss is associated with the reverse recovery of the body diode in the low side switch.
3. Gate drive losses are due to both the high and low side switches and can be attributed to the power lost when charging the gate of a MOSFET

4. During each switching cycle, the Coss (lumped output capacitance of the MOSFET's) must be charged. The Coss losses are due to this
5. When the high side FET turns on before the low side FET turns on, a dead time is allowed when both switches are off, to prevent cross conduction of the switches. If the dead time is too long, the body diode of the low side FET can be forward biased causing losses. In PFM, the dead time losses are only calculated when the low side turns. The dead time losses when the high side switch turns would be close to zero as the inductor current has reduced to zero before the high side switch is turned on.
6. The conduction losses are the ohmic losses , contributed by the current flowing through the on resistance of the switches and the DC resistance of the output inductor
7. Fixed losses are the losses seen in the control POL IC and the driver IC. A major contributor to these is the quiescent current consumed in the LDO, used to provide the supply to the various blocks in the control POL IC.

A table summarizing these losses and the equation used to calculate these is shown below.

.

Loss component	Description	Equation
High side switching loss	Switching loss when high side MOSFET is turned on	$\frac{Vin * Iout}{2} * fsw * (ts_{LH} + ts_{HL})$
Diode Reverse recovery loss	Reverse recovery of Low side body diode	$Q_{RR} * Vin * fsw$
Gate drive losses	Losses contributed by the gate charge	$2 * QG * Vin * fsw$
Coss Losses	Losses due to charging and discharging of the MOSFET output capacitance	$Coss * Vin^2 * fsw$
Conduction Losses	Losses in DCR and on resistance of FET	$Iout_{rms}^2 * (DCR + Rds_{on})$
Dead Time losses	Losses which occur during the dead time in the low side body diode	$DT * Vdiode * fsw * Iout$
Fixed Losses	Quiescent losses in the IC	N/A

Table 2: Summary of loss components

A bar graph which shows the contribution of each of these components to the total losses is shown below, for PFM mode at 100mA of load current.

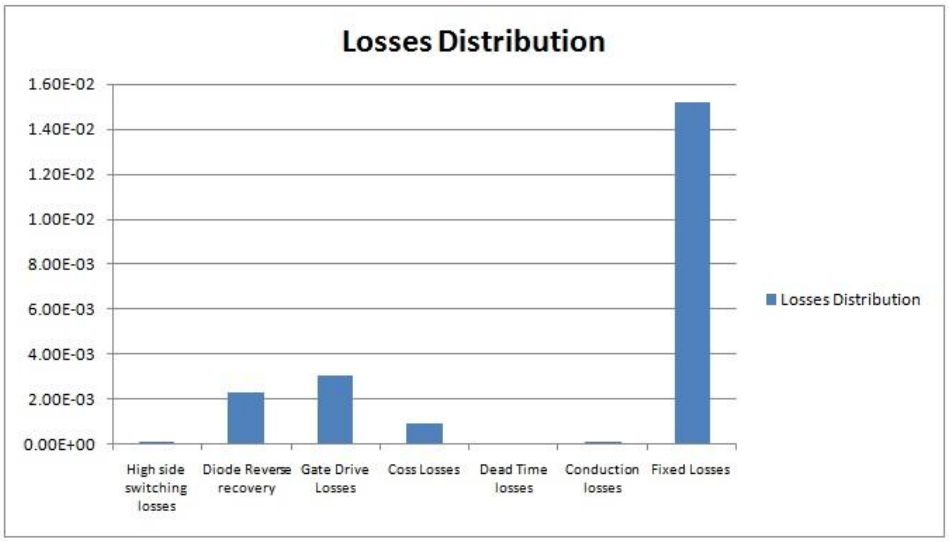

Figure 40: Distribution of losses in PFM

The major contributors to the loss at this load current are the diode recovery and the gate charge losses, both of which are frequency dependent.

The PFM efficiency curve plotted over a load current range of 100mA to 500mA with 0.9V output voltage and 5V input voltage is plotted in Figure 41. The maximum efficiency is 93% at 500mA while the efficiency at 100mA of load current is 82%.

The PFM and PWM efficiencies are compared in Figure 42. The PWM efficiency is plotted from 100mA to 10A while the PFM efficiency is plotted over 100mA to 500mA

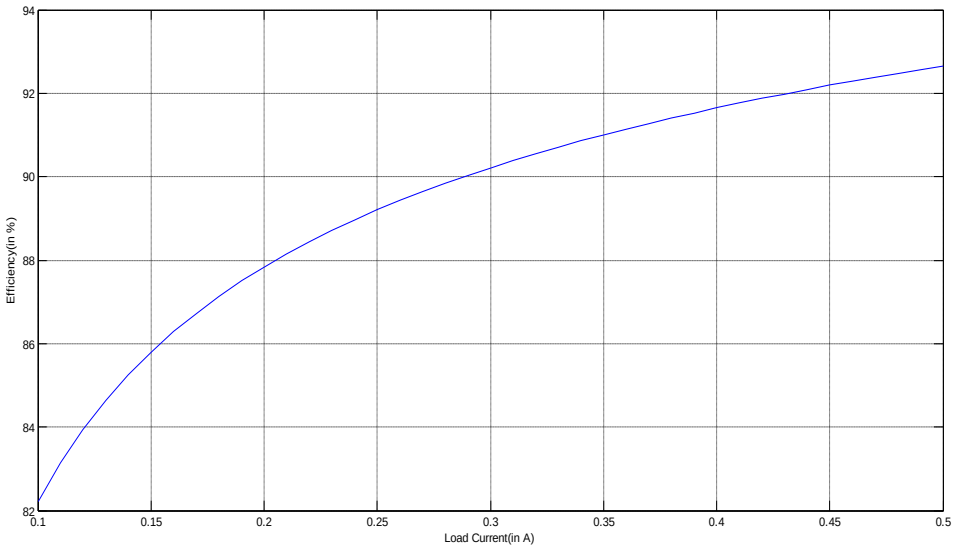

Figure 41: PFM efficiency variation

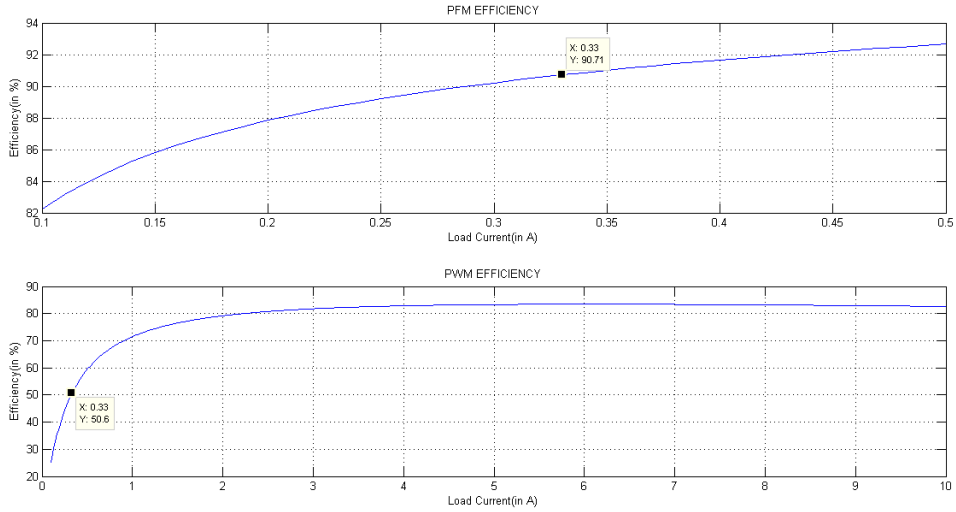

Figure 42: PFM vs. PWM efficiency

It can be seen in the above figure that for 330mA load current, PWM offers a efficiency of about 50% while the corresponding efficiency for PFM is 90%.

4.5 Transition from PFM to PWM plots

Transition from PFM back to the PWM is done in Ultrasim (without using extracted circuit) with an ideal PWM loop, so as to accelerate the time taken for the simulations. The current for which the transition will occur is 400mA and the count for which transition happens is 400mA. The transition plots are shown below.

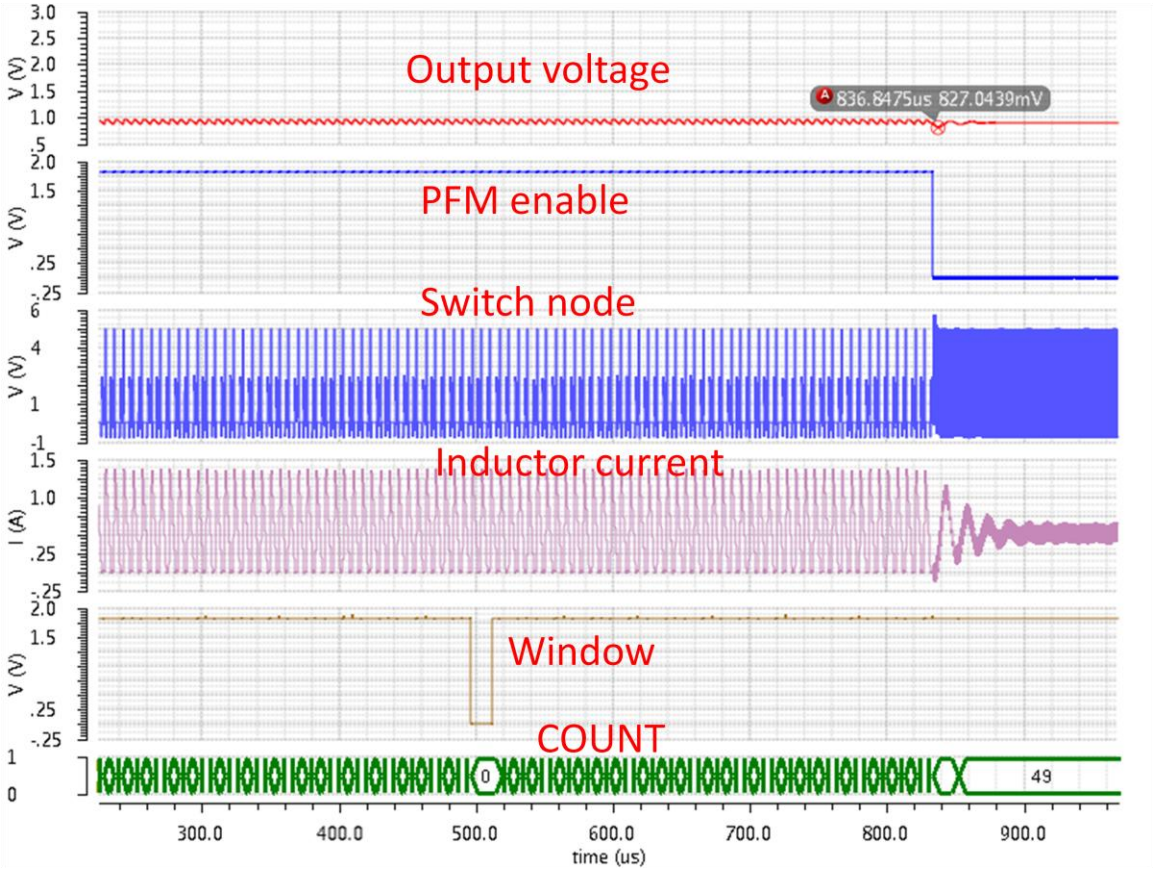

Figure 43: PFM to PWM transition

In the above figure, it can be seen that when the count reaches 48 the condition for PWM is detected and control is transferred. Also, the jump to the final count is not immediate and it takes a few counting cycles for the count to reach the threshold i.e. 48. If the increase in load current is not picked up in one window it will be in the next.

5 CONCLUSION & FUTURE WORK

A PFM hysteretic converter has been implemented in IBM 0.18 micron technology. The following are the specifications met for the design

Input Voltage	5V
Output Voltage	0.9V
Power MOSFET used	Sis376DN
Switching Frequency in PWM	1 MHz
Maximum Current in PWM	10A
Load Current Range in PFM	100mA-420mA
Minimum Efficiency	82% @100mA
Current for transition for PFM to PWM	420mA
Ripple in PFM	< 75mV

Table 3: Summary of results

5.1 Future Work

5.1.1 PFM implementation

It can be seen that while PFM offers good efficiency at low loads, the ripple is large. One can achieve good ripple characteristics and good efficiency by adding peak current limiting in PFM.

5.1.2 Programmability of Transition Circuit

The digital circuit has been currently implemented using standard cells. The threshold count is fixed at 48. The circuit can be made programmable by implementing it in RTL and making the threshold count programmable through SPI write.

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