Calibration of MEMS capacitive accelerometers using Electrical Stimulus BIST

by

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ABSTARCT

Built In Self-Test (BIST) circuit for MEMS accelerometer:

The applications which use MEMS accelerometer have been on rise and many new fields which are using the MEMS devices have been on rise. The industry is trying to reduce the cost of production of these MEMS devices. These devices are manufactured using micromachining and the interface circuitry is manufactured using CMOS and the final product is integrated on to a single chip. Amount spent on testing of the MEMS devices make up a considerable share of the total final cost of the device. In order to save the cost and time spent on testing, researchers have been trying to develop different methodologies.

At present, MEMS devices are tested using mechanical stimuli to measure the device parameters and for calibration the device. This testing is necessary since the MEMS process is not a very well controlled process unlike CMOS. This is done using an ATE and the cost of using ATE (automatic testing equipment) contribute to 30-40% of the devices final cost. This thesis proposes an architecture which can use an Electrical Signal to stimulate the MEMS device and use the data from the MEMS response in approximating the calibration coefficients efficiently. As a proof of concept, we have designed a BIST (Built-in self-test) circuit for MEMS accelerometer. The BIST has an electrical stimulus generator, Capacitance-to-voltage converter, $\sum \Delta$ ADC. This thesis explains in detail the design of the Electrical stimulus generator.

We have also designed a technique to correlate the parameters obtained from electrical stimuli to those obtained by mechanical stimuli. This method is cost effective since the additional circuitry needed to implement BIST is less since the technique utilizes most of the existing standard readout circuitry already present.

ACKNOWLEDGMENTS

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CHAPTER 1: INTRODUCTION

The number of day-to-day applications which use motion sensing, inertial sensing have been increasing exponentially. The most popularly used sensors for these applications are Micro-Electro-Mechanical systems (MEMS). Their applications range from orientation sensing in small devices like Phones to pivotal applications like crash detection mechanism in automobiles.

MEMS have become very popular because of their small size and they can be easily fabricated on a silicon substrate. They are small integrated devices that combine electrical and mechanical elements for sensing or actuating purposes and these can be easily combined with IC chips. These are devices that convert non-electrical quantities like acceleration, angular velocity, pressure into electrical signal and vice-versa. The readout and support circuitry are implemented on an IC fabrication process and the MEMS are fabricated through a micromachining sequences that selectively remove/add parts of silicon to form the three-dimensional electromechanical elements. Micromachining enables transducers to be miniaturized by shrinking their size considerably reducing their cost of fabrication and integration with the electronics on the same silicon chip makes its beneficial.

The MEMS devices are used as Pressure sensors, inertial sensors, RF MEMS, optical MEMS, bio MEMS. One of the most important applications of MEMS devices are inertial sensors consisting of accelerometers and gyroscopes.

1.1 Accelerometers:

Micro-accelerometers are one of the important classes of MEMS devices that hold the second largest sales capacity after pressure sensors. They are widely used in many applications such as automotive safety, biomedical applications, oil and gas exploration. Accelerometers with high resolution and high accuracy are used in areas like earthquake detection, GPS-augmented inertial navigation, geophysical sensing. High performance accelerometers are utilized in ultra-small size, large volume portable devices like cellular phones and handheld devices. Acceleration is measured in distance/time^2 and the commonly used unit is "g". One "g" is a unit of acceleration equal to the earth's gravity at sea-level which is equal to 9.8 m/s^2. The common applications where the accelerometers can be used are [1]:

- Tilt/ Roll

- Vibration detection

- Orientation Detection

- Impact/ crash detection

The number of applications which use MEMS inertial sensors are increasing and they are finding many uses in the field of Bio-systems.

1.2 Types of accelerometers:

There are different types of accelerometers and are classified on the basis of transduction principle. Some of the common methodologies include Capacitive, Piezo-resistive,

Piezoelectric, Tunnelling, Optical, Heat transfer, Hall effect, Thermal, Interferometric etc. Few types are explained below:

- Capacitive: Consists of proof-mass and series of parallel plates. Acceleration causes the spring-mass system to move, thus changing the capacitance between the plates.

- Piezoelectric: Piezoelectric crystal mounted to mass-voltage output converted to acceleration.

- Piezoresistive: Consists of beams whose resistance change based on acceleration

- Tunneling: Consists of a cantilever structure with variable gap between an integrated tunneling tip and a conducting electrode causes electron tunneling in the gap and this principle can be used to detect extremely sensitive accelerations.

- Interferometric: The inter digital system forms an optical diffraction grating where the displacement of the proof mass relative to the support substrate is measured with a standard laser diode and photo detector.

1.3 Organization of thesis:

This thesis consists of six chapters. The first chapter presents the brief overview of the MEMS devices. The second chapter introduces the MEMS accelerometer and discusses about the theory and properties of the MEMS accelerometers. In the third chapter, there are discussions regarding the BIST architecture and the various methodologies which were tested during the research for the BIST architecture.

The fourth chapter presents in detail the Signal generation techniques used in the BIST architecture. It explains in detail the three different techniques that have been designed and their advantages and disadvantages on the whole.

Chapter five elaborates the statistical methods that have been developed as a part of this thesis. It elaborates the process of developing the statistical framework to map the electrical response to that of the mechanical calibration coefficient. Chapter six is conclusion and future work.

CHAPTER 2: MEMS ACCELEROMETERS

2.1 Theory:

There are different types of accelerometer and they are mostly categorized based on the transduction principles. The most common types are capacitive accelerometer, piezoelectric accelerometer. This section discusses in detail about the capacitive accelerometer. The following figure shows the structure of a typical capacitive accelerometer [2].

The capacitive accelerometers are typically are composed of movable proof mass with plates. The proof mass is suspended through a spring and the plates attached to the proof mass are movable. There is a system of plates which are fixed and this is used as reference frame. There is free-space capacitance between the movable plates and the fixed plates. The deflection of the proof mass causes the plates to move with respect to the reference frame and this creates change in capacitance. The capacitances C_1, C_2 between the plates are:

$$C_1 = \frac{\varepsilon_A}{x_1} = \frac{\varepsilon_A}{d+x} = C_0 - \Delta C; \quad C_2 = \frac{\varepsilon_A}{x_2} = \frac{\varepsilon_A}{d-x} = C_0 + \Delta C$$
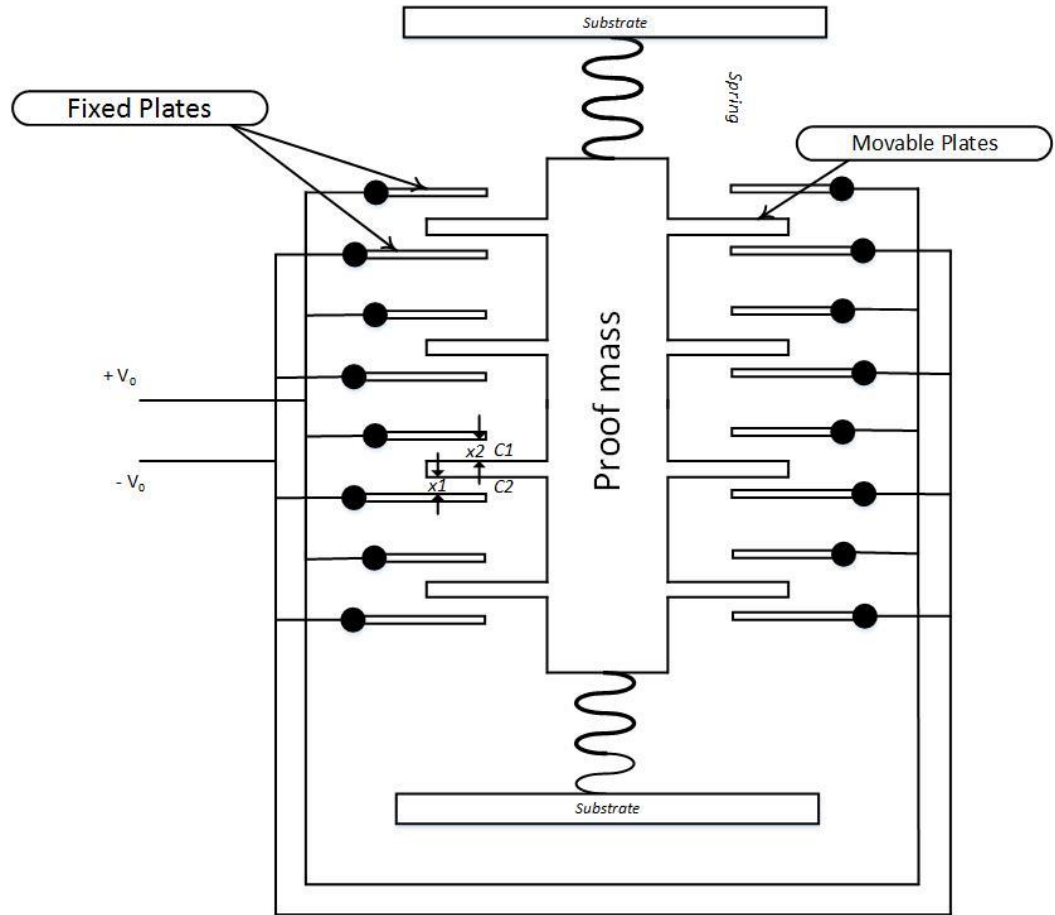
Figure 0-1 Comb style accelerometer

When the acceleration is zero, the capacitances C_1, C_2 are equal since $x_1 = x_2$. When the acceleration is applied, the change in the distance between the plates results in a change in the Capacitance difference. Then the difference in the capacitance can be calculated as:

$$C_1 - C_2 = 2\Delta C = \frac{2x\varepsilon_A}{d^2 - x^2}$$

Thus by measuring ΔC, we can calculate the distance using the above equation. The above equation can be simplified to:

$$x = \frac{d^2}{\varepsilon_A} \Delta C = \frac{\Delta C}{C_0} d$$

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The displacement is proportional to the capacitance difference ΔC. Typically, the capacitive difference is small and very hard to detect. So we use many parallel plates and the change in the capacitance of each plate adds up and this can be detectable easily depending on the number of devices. The accelerometer can be simplified in terms of mechanical parameters to the following schematic:
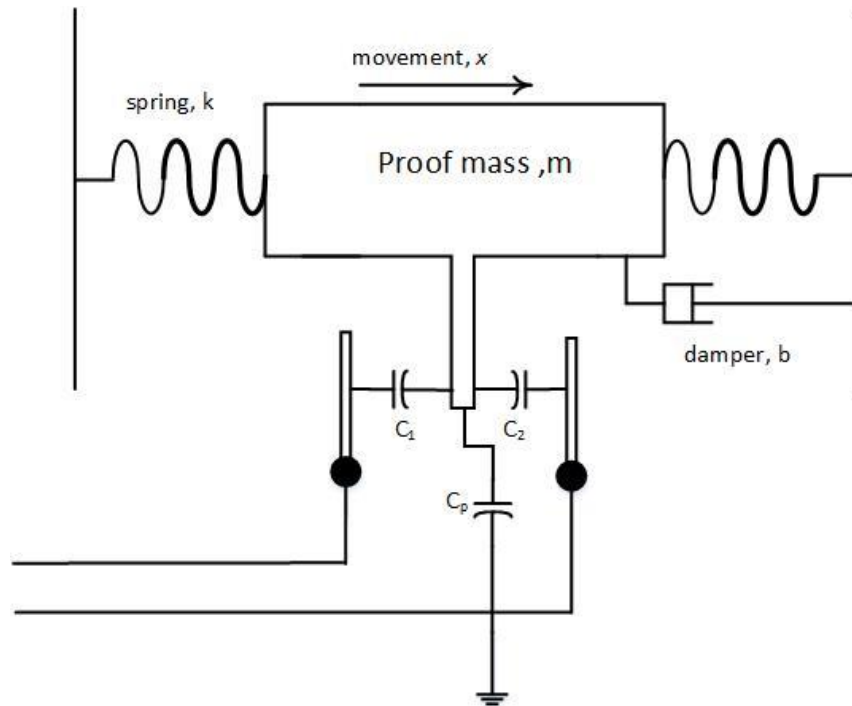
Figure 0-2 Structure of MEMS accelerometer

The above system is a mass-spring-damper system and can be represented using a second order differential equation:

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = ma_{ext}$$

Where k – Spring constant

a_{ext} – external acceleration

b – damping coefficient

m – proof mass

Using Laplace transform, the above equation converts to a second-order transfer function:

$$\frac{X(s)}{A(s)} = \frac{1}{s^2 + s\frac{b}{m} + \frac{k}{m}} = \frac{1}{s^2 + s\frac{\omega_r}{Q} + \omega_r{}^2}$$

Where $\omega_r = \sqrt{\frac{k}{m}}$, is the resonant frequency and $Q = \omega_r/b$, is the quality factor. At low

frequencies $(\omega \ll \omega_r)$

$$\frac{X}{A} \approx \frac{1}{\omega_r{}^2}$$

Thus we can observe that the sensitivity is inversely proportional to the square of the resonant frequency which means the lower the resonant frequency the higher the sensitivity. The lower limit of the resonant frequency is bounded by many factors such as mechanical shock resistance, spring constant, effective mass and manufacturability.

The effective spring constant (K) of accelerometer is expressed by:

$$K = K_{mechanical} - K_{electrical} \text{ [N/m]}$$

The mechanical and electrical stiffness of the structure are given by :

$$K_{\text{mechanical}} = 4\, E_x h \left(\frac{w_t}{l_t}\right)^3$$

$$K_{electrical} = \frac{1}{2}\, V_{DC}{}^2\, \frac{N_e \varepsilon_o h\, l_e}{d^2}$$

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Where E_x -Young's modulus of silicon in the sense direction;

N_e – total number of sense electrodes

h - Height, w_{t} – width, l_t - length of the tethers

d – Initial gap spacing

V_{DC} – applied DC voltage to the sense capacitors.

2.1.1 Pull-in voltage:

The voltage applied at which the excited proof mass sticks to fixed plate and this cause instability of the device. This can cause permanent damage to the device and this is can occur in two ways: Dynamic, due to electrostatic action and Static, due to inertial and damping effects. To determine the point of instability, we analyze the net force equation:

$$F_{net} = F_{electrostatic} + F_{elastic} = C_0 d_0 \frac{V^2}{2(d_0 - x)^2} - kx$$

Differentiating the equation w.r.t 'x' and solving the equation gives the $X_{critical}$ point at which the system goes unstable.

$$x_{critical} = \frac{1}{3} d_0$$

The pull-in voltage is the voltage at which the system becomes unstable can be obtained as:

$$V_{pi} = \sqrt{\frac{8 d_0^2 k}{27 C_0}}$$

When the voltage is higher than the pull-in voltage, the elastic force can no longer compensate for the electrostatic force and the movable mass will stick to the fixed plate causing short circuit. To prevent this from happening in accelerometer, a mechanical stopper is designed and placed to prevent the sticking.

2.1.2 Stoppers:

A large shock might cause the accelerometer to move vigorously and during this movement there is a possibility that the proof mass sticks permanently to the fixed plate. A stopper is used prevent the proof mass from sticking to the fixed plates due to movement from large shocks. The sticking phenomena depends on the contact area, so it is important to design the stopper geometry for avoiding large contact surfaces with movable part. The figure shows picture of anchors and stoppers.
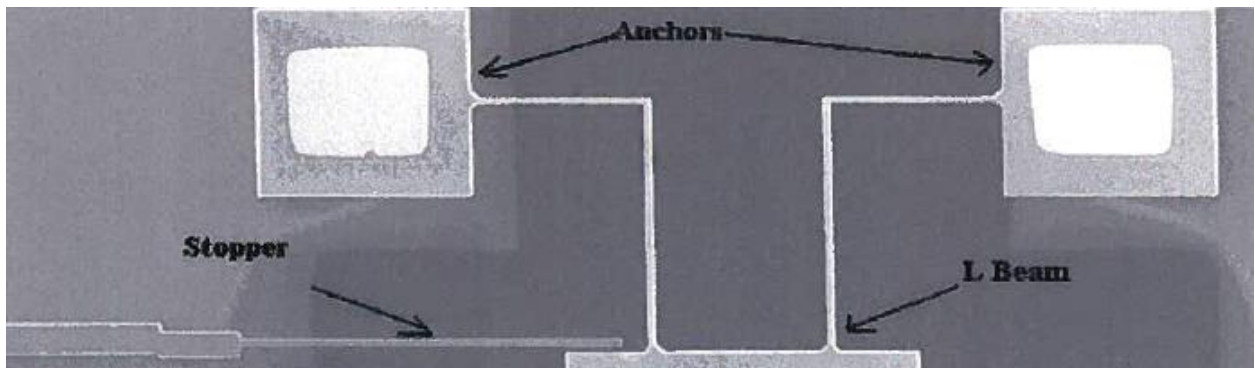
Figure 0-3 Stopper and anchors in accelerometer

2.2 Accelerometer related Errors:

i. Non-linearity: When a high acceleration is applied to the device, the voltage produced is not proportional to the acceleration and the output voltage will saturate near the pull in voltage. The non-linearity also occurs when there are imperfections that are produced during the fabrication process.

ii. Hysteresis: The mass of the accelerometer might move even after the acceleration on the device is stopped. This might cause instability in the system.

iii. Noise: There is mechanical noise and Brownian noise which is present in the accelerometer. There is also an additional noise which is caused due to working of the electronic circuitry present on the chip.

iv. Cross coupling: When the accelerometers are operating in the open loop, they have unwanted oscillations or vibrations due to the presence of off axis oscillations of the proof mass. This can be reduced by using a closed loop approach forcing the proof mass to be at rest by applying voltage across the plates.

CHAPTER 3: BACKGROUND

3.1 Previous Work:

A lot of research and study has been done on testing and calibration of MEMS capacitive accelerometers in the past. The conventional methods used for testing and characterization for MEMS are very resource intensive. The aim of this research is to perform test and calibrate the MEMS accelerometer by using only the electrical stimulus test bench without applying acceleration.

Research has shown that measurements and results from electrical tests correlate to that of the mechanical tests. Many researchers have used parameters that can be measured through electrical stimulus excitation and map it to correlate to accelerometers sensitivity.

In [3], they have designed a two-step process in which they first characterize the MEMS device using standard mechanical stimulus. In the second stage of study they use an electrical stimulus as a test input and then characterize the DUT's. When electrical test input stimulus is applied to the capacitive plates, there is a displacement of plates. This displacement of plates is measured for both the mechanical and electrical stimulus and they are correlated. They have used a single parameter to measure and map the electrical stimulus response to that of the mechanical response.

The authors and researchers in [4] have used the combined information derived from resonance frequency and pull-in voltages to calibrate the MEMS device. They introduced a methodology where they apply a asymmetric actuation voltage to create acceleration of

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the plates. They have used a pull-in voltage based solution to auto-calibrate the MEMS device.

In [5], the authors have used three parameters that can be measured electrically to correlate the sensitivity of the MEMS accelerometer. The three parameters that were used were the natural pulsation, the pull-in voltage and the electrostatic sensitivity. They use the sensitivity information to calibrate the MEMS accelerometer. The natural pulsation or the resonance frequency occurs when the phase shift across the MEMS accelerometer is about 90^0. They have used PLL to lock on the required phase shift and they determine the resonance frequency. The static sensitivity is measured by applying a small voltage step signal to both the plates and they calculate the sensitivity for both the plates. If there is no offset in the plate system, the sensitivity is same. The pull-in voltage is the voltage at which the spring force is not sufficient to compensate for the electrostatic force. The pull-in voltage is measure by applying by applying a slow moving ramp signal to the proof mass and the electrical parameter V_p is measured.

In [6], the author proposes a new method to electrically test and calibrate capacitive accelerometers. The author uses the following four parameters to test and calibrate the accelerometers. They apply a sweeping electrical signal to the MEMS device and observe the frequency at which the MEMS device has a 90 phase shift. The electrical frequency at which the phase shift of the device has the phase shift is the natural Frequency. They introduce a new parameter Non-Linearity in the prediction parameter. They apply a large signal step voltage and compare the deviation of the output voltage with respect to the small-signal behavior.

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$$NL = \frac{G_A \cdot V_{testNL} - Sv \cdot 1.65^2}{Sv \cdot 1.65^2}$$

They use other features of Electrical sensitivity and first-stages gain to map to the mechanical calibration coefficient. They use MARS regression model instead an analytic method to improve the accuracy of the system. They claim to have a reduction factor higher than 6 on the dispersion of sensitivity before and after calibration.

The previous research work included the use of parameters like pull-in voltage to calibrate the device. But subjecting a device to its pull-in voltage might render the MEMS device useless and it might cause the proof mass to stick to the plates. The use of PLL to determine the phase shift of 90^0 of the device is a good solution to determine the resonance frequency. The time consumed by the PLL to lock will be more depending on the resonant frequency range. Typically the resonant frequency is few KHz and the time consumed by the PLL to lock into that range is around few milliseconds. This is a time consuming process and this is not suitable in real time implementation during the device calibration.

This research demonstrates a novel mechanism where we use electrical sub-system to excite the MEMS to obtain the analog output voltage of the device. The output voltage of the device will be mapped to the mechanical calibration coefficient. In this methodology we use the presently existing readout circuitry and introduce less complexity. By using this methodology we would be able to get rid of the mechanical stimulus testing and would just need an electrical stimulus based test approach.

Architecture Design:

The MEMS accelerometer typically consists of a movable finger between two fixed fingers. This will make up a set of variable capacitors whose value change with acceleration. In order to detect the change in capacitance, we use CMOS circuit to detect. The common topologies which are used to detect the change are as follows:
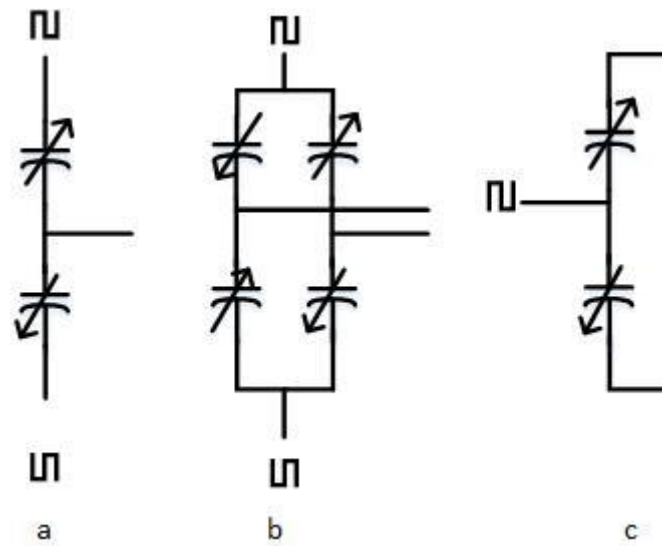
Figure 0-1 Common topologies of connecting readout circuit

There are two configurations: Half-bridge and Full-bridge. The half bridge uses single ended readout circuits. The change in capacitance is compared against a reference cap. A sine wave or square wave of high frequency is applied to the capacitors to create a charge flow between nodes. In single ended, non-idealities and parasitic capacitances will not be balanced and this may cause erroneous observations.

The full bridge circuitry has four capacitors of which two are reference caps and the other two are capacitors from accelerometer. The circuit is differential and the non-idealities,

common mode noises and effect of parasitic capacitors will be cancelled to a great extent. The configuration in (c) has a pseudo-differential structure where the signal is applied to the common mode and the output signal is readout differentially.

3.2 Typical Readout circuitry architecture:

The typical MEMS readout circuit consists of capacitance-to-voltage converter connected to the device. The output of the C2V is the amplified by a controllable gain amplifier and the output of the amplifier is then converted to a digital signal. The commonly used A/D converter is the Sigma-Delta converter. The following figure shows the typical MEMS readout circuit:
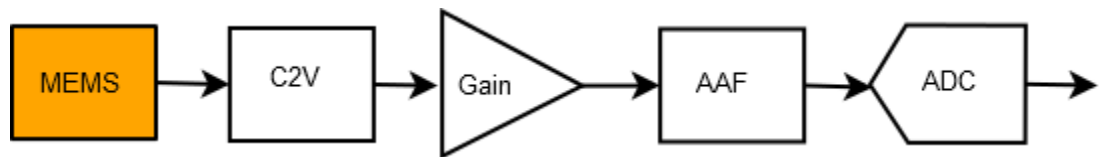
Figure 0-2 Typical MEMS accelerometer readout

The MEMS devices have a large parasitic capacitances and the readout circuitry needs to be insensitive to these capacitances. Many techniques have been developed, such as charge sensitive amplifier (CSA), auto-zeroing technique, correlated double sampling(CDS) and chopper stabilization.

The existing readout circuitry for capacitive sensing can be classified in to three types: Switched-capacitor (SC) charge integration, continuous-time (CT) current readout with trans impedance amplifier (CT) and continuous-time voltage readout (TIA). The switched

capacitor circuitry is commonly used since it robust and has noise reduction techniques that can be designed.

3.3 Proposed Built in Self-Test:

The proposed BIST circuit consists of a DAC to electrically excite the MEMS device, a capacitive C2V converter, a sigma-delta A/D converter to convert the output to a digital signal.
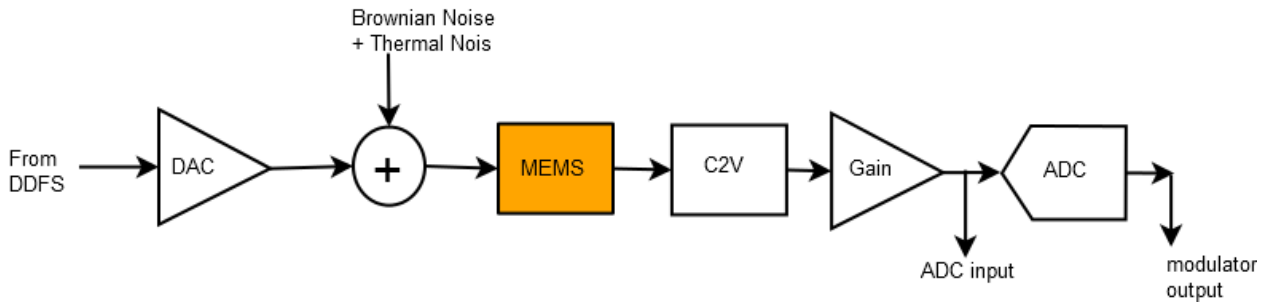
Figure 0-3 Proposed BIST circuit

The DAC generates a stair stepped signal and the output of the DAC is the used to excite the MEMS device. The MEMS device plates are connected to a C2V converter and the output is digitized by an A/D converter and the signal is then saved in a FPGA. The frequency of excitation of the MEMS device is swept from 1 KHz to 6 KHz at 500 Hz resolution and the output of each frequency is saved in an FPGA.

The electrical parameters are extracted from this data and these are used to estimate the calibration coefficient of the MEMS device. The accelerometer we used is a 3-axes accelerometer, comb shaped structure. The same accelerometer will be used in electrical stimulus excitation and the same is used in physical acceleration.

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CHAPTER 4 : ELECTRICAL STIMULUS GENERATION

The cost associated with testing these complex systems have increased and there is a lot of research effort to explore more efficient testing methodologies. Traditional test methodologies required an ATE (Automatic Test Equipment) generating high quality stimuli and high quality digitization and acquisition systems, making the implementation of Test Systems difficult. So in order to overcome the challenges, we have developed BIST (Built-in Self-Test) mechanism to test the MEMS accelerometer.

The Built-in-self-test architecture of the MEMS device consists of a Signal Generation, Capacitance–to-Voltage converter and a Sigma Delta Converter. The MEMS accelerometer is excited using an Electrical Stimuli and the type of the electrical stimuli used for the excitation should be or similar to a Sine Wave. We need an architecture which will allow us to completely characterize the magnitude and phase response of the MEMS device when excited by a Signal generator whose signal frequency is swept across a range.

The Electrical stimuli are applied to a DUT (Device under test) and the output is the characterized and digitized by a Sigma Delta A/D converter. In this line, some interesting work on generation and evaluation of signals for BIST applications has been published in the past [0123456]. Among them, preferred solutions are those with the following attributes:

- Produces Signal whose range is from 1KHz-10KHz
- Output should have a resolution of 10 Hz.

- Output Frequency should change instantaneously depending on input selection

- Should be compact and simple to be used in Built-in-self-test

- Low design efforts

The following section talks about the various techniques used for the generation of sine waves. The Signal generator has been implemented in a 0.35um-3.3V process.

Phase Locked Loops:

 The phase locked loops for decades have been one of the most common ways to generate signals on a chip. The Phase Locked Loops typically consists of a Phase Detector, Charge Pump, Voltage Controlled Oscillator and Frequency Divider. The signal from a Crystal is used as an input to the loop and the output of the PLL is proportional to the Frequency Divider ratio. The PLL is typically used when the frequency required by the circuit is .1 GHz-10 GHz. The following figure shows a typical model of a PLL:
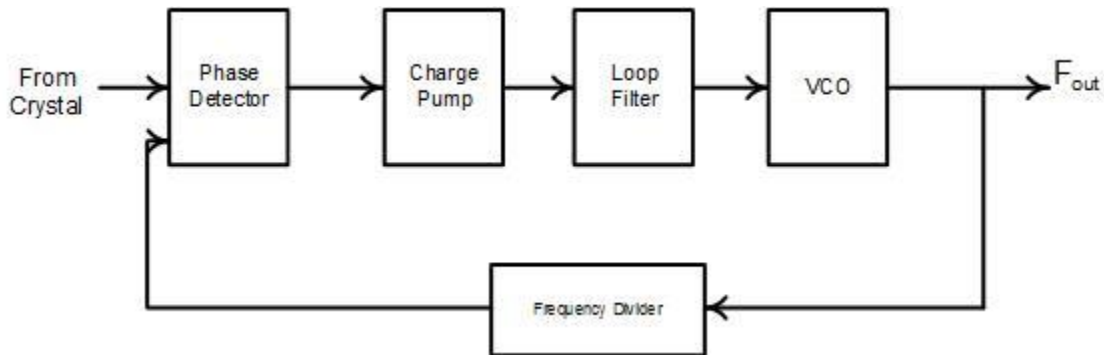

Figure 4-1 Typical phase locked loop strucure

The output frequency of the PLL is controlled by the Frequency Divider. It is very difficult to design a PLL which has 10 Hz resolution. The output of the PLL would

change when the Frequency Divider ratio is changed. The PLL requires Loop-Lock time before which the output of the frequency changes with respect to the change in Frequency Divider ratio. The PLL is a very complex and the area needed by a PLL is larger.

The output of the PLL should then be filtered to get a pure sine-wave with lesser number of harmonics. The circuitry involved in using a PLL as a signal generator is quite large and we would require a simpler circuitry since it will be used in a Built-in-self-test circuitry.

Since generation of pure sine wave using this technique requires a lot of design effort and the complex architecture makes it less suitable to use this in BIST. We have decide on implementing the following technique as part of the BIST methodology considering its simple design and can be easily added to the present circuitry on chip.

Digital Frequency Synthesizer:

Many BIST solution and methodologies have been proposed in the past. These techniques use a DAC interface to generate a stimuli and an ADC for digitizing a response. In two techniques of using $\sum \Delta$ bit stream techniques have been proposed. In RAM based technique, a RAM is used and this requires a large area to implement on Silicon. And the resolution of the output frequency is dependent on the number of bits (N) and the RAM size. In the authors designed a mechanism which uses a DDFS and a Switched capacitor bank to generate a stepped sine wave. The output from the switched capacitor network is then filtered using a Switched capacitor filter. We designed out technique on similar lines to generate the stepped sine wave signal.

In our application the MEMS device is excited by an electrical stimuli and the output is then digitized using a $\sum \Delta$ converter. The output from the MEMS device consists of sine wave whose amplitude and frequency is characterized using the A/D converter. The output of the A/D converter is then stored for post-processing. The frequency of the electrical stimuli is swept and the output magnitude and phase for all the frequencies is stored. Using this data we can retrieve information regarding the MEMS device parameters from post processing. From our observation, the output SNR is around 40dB.The low SNR is due to the MEMS mechanical noise and the Brownian noise. The noise can be reduced be reduced by various techniques . But in the application we don't have the option to reduce the noise and so we are restricted to a SNR of 40dB.Since the SNR is limited by the MEMS noise, the signal used to excite the device need not be a pure sine signal. A stepped sine wave can be used to excite the DUT and the effect of the signal nature does not depreciate the SNR. The SNR is not degraded very much and since the input signal's frequency is known, we can to some extent expect the frequencies at which the harmonics are present. The frequency of output signal is expected and we take into account the spot noise at that frequency for our post processing. The use of Stepped Sine wave served the purpose of excitation in our BIST approach.
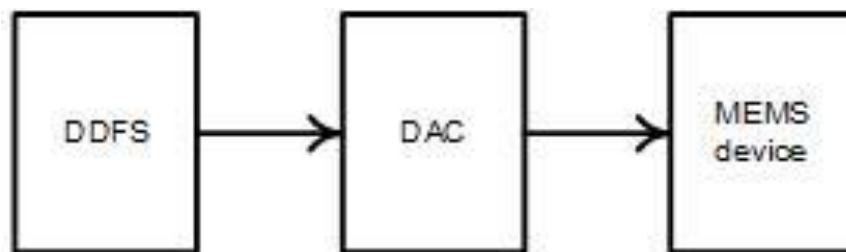

Figure 4-2 Proposed DAC

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The picture shows the methodology followed to generate the signal. The signal generated is a stepped sine wave and the architecture designed consists of a DDFS, DAC. The DDFS is implemented in a DDFS on a FPGA and the signal from the DDFS is then transmitted onto the chip to be fed to the DAC to generate the stepped sine wave. The following section discusses in detail the various parts of the signal generation methodology.

4.1 Direct Digital Frequency Synthesizer:

4.1.1 Theory of operation:

A Digital Frequency synthesizer consists of an overflowing Phase Accumulator, Phase-to-Amplitude converter and D/A converter. The output of the DDFS is controlled by 1) the Tuning word and longer the M word, 2) the frequency of the reference clock [7].
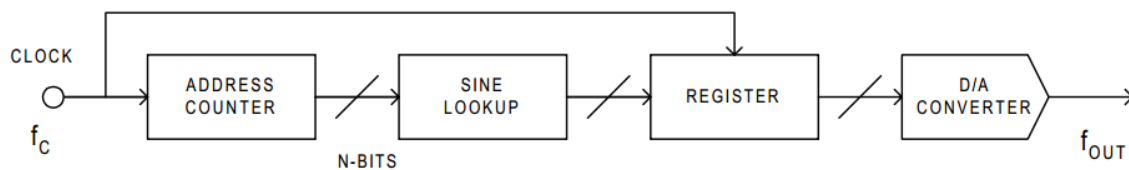

Figure 4-3 Commonly used DDFS

The tuning word is typically 24-48 bits and is fed to the Phase accumulator. The tuning word controls the minimum resolution that can be achieved from the DDFS. The longer the M word better is the accuracy and better is the output frequency resolution.

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The typical DDFS consists of a N-bit variable-modulus counter and Phase register. The Phase accumulator overflows depending on the M word and the carry function allows this function as a "phase wheel" in the DDFS architecture.
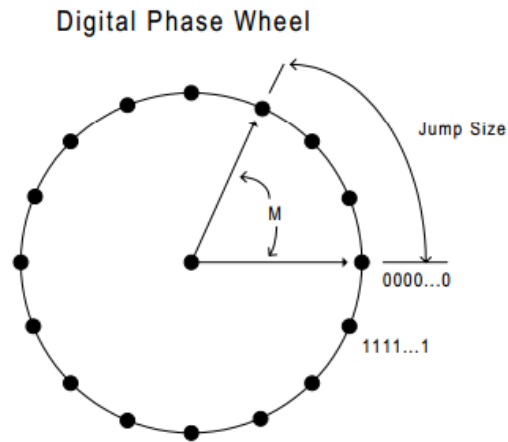
Figure 4-4 Digital Phase wheel

Each point the phase wheel corresponds to an equivalent point of a sine wave. Depending on the M word, the designated points on the phase wheel are hit. As the vector rotates around the wheel, the corresponding output sine wave is being generated. One revolution of the vector around the phase wheel, at a constant speed, results in one complete cycle of output sine wave.

The Phase Accumulator adds the M word to the present value in the Phase Accumulator each time it receives the clock pulse. The M word forms the phase step size between reference clock updates. The M word sets how many points to skip around the phase. This keeps happening until the Phase Accumulator overflows. The larger the jump size, the phase accumulator overflows faster and completed an equivalent cycle. The relationship between the M word, output frequency of the DDFS is given as

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$$F_{out} = \frac{M(REFCLK)}{2^N}$$

Where: F_{out} – Output frequency of the DDFS

M – Binary tuning word/ M word

REFCLK – Reference clock of the system

N – length in bits of the phase accumulator

A set of bits from the Phase Accumulator is fed to the Phase-to-Accumulator converter. The D/A converter generate the analog sine wave in response to the output from the Phase-to-Amplitude converter. The change in the M word results in immediate and phase continuous change in the output frequency. The speed limitation in changing the DDFS output frequency is dependent on the rate at which the buffer register can be loaded to the phase accumulator.

4.2 Implementation of DDFS:

In our methodology, we 1) feed the M word to the phase accumulator on the FPGA; 2) the MSB of the phase accumulator is taken as an input to the chip and used as a clock to the DAC. We use the MSB of the DDFS's 16 bit output as an input to the DAC's digital logic. When the phase accumulator overflows the MSB bit will change its value and this digital signal is transmitted as an input to the BiST chip.
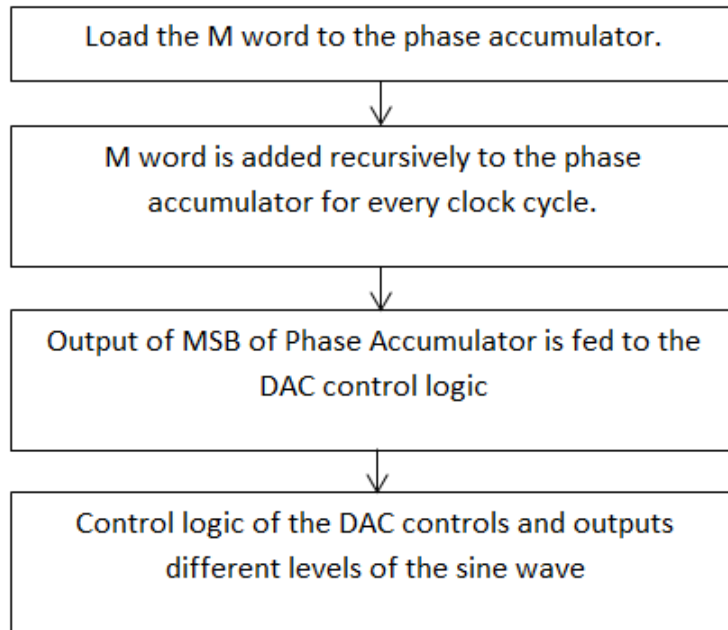
Figure 4-5 DDFS

The Clock frequency for the FPGA is 1MHz and the number of bits for the DDFS is 16 bits. The 16 bits word length of the phase accumulator will provide us resolution of 15Hz. The output required from the DDFS is around 24 KHz-240 KHz. This is can be achieved by using the M word between 1573- 15728. The change in M word from 1573 to 1574 will change the output from 24002 Hz to 24017Hz and giving us a resolution of 15Hz.
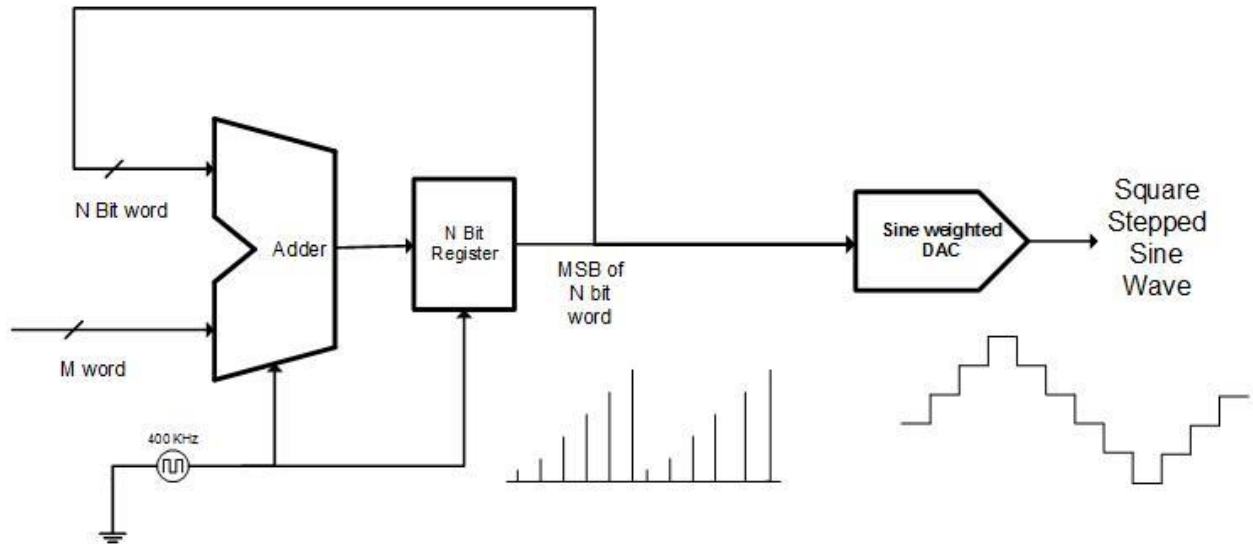
Figure 4-6 Block diagram of DDFS

The output of the DDFS is fed to the DAC's digital logic. The output of the DAC will be 1/24 times the output of the DDFS. The DAC will generate an output of 1 KHz if the 24 KHz digital signal is fed from the DDFS. The minimum resolution that can be achieved from the DDFS is 15Hz and this will convert to a 1Hz resolution at the DAC's output.

In many DDFS applications, the spectral purity of the system is important. But this is affected by the spurs which are produced in the DDFS system. One of the reasons why the spurs are produced is because of the truncation of the phase accumulator's value. The amplitude of these spurs is dependent upon the ratio of the output frequency to the clock frequency. spurs are dependent on these factors - Phase Accumulator Size and M bit tuning word. One way to reduce the spurs is by adding Dither to the Phase accumulator.
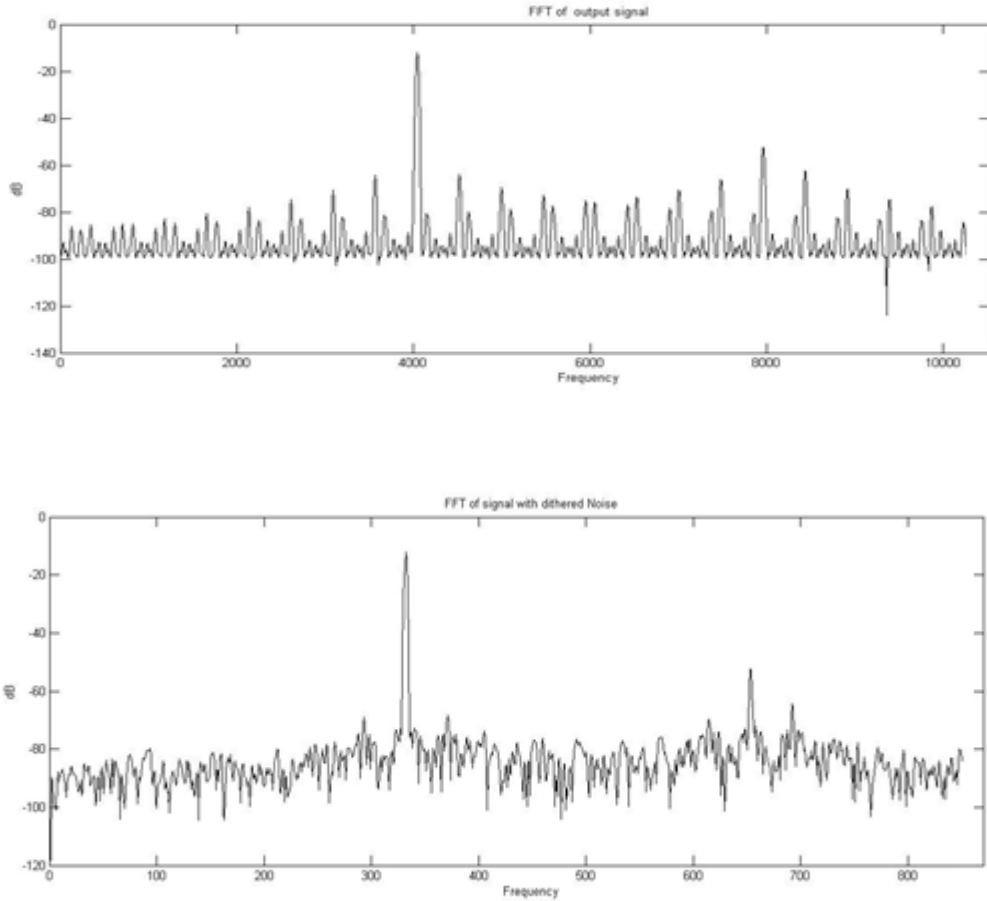
Figure 4-7 FFT of DDFS signal with and without dithering

This will randomize or spread the spurs throughout the available bandwidth. The following is the FFT of a signal with and without dithering.

The addition of dither to M-word in DDFS will reduce the spurs by spreading the energy of the spurs in to successive bands. This might rise the noise floor of the signal but might have lesser spurs and better harmonic distortion. The dithering of M-word can be done using a pseudo-random generator. If the N-bit phase word is truncated, then the resultant signal is mixed with spurs at multiples of frequencies [01234], given by

$$F_{spur} = REFCLK. \frac{GCD (FCW, 2N-P)}{2^{N-P}}$$

During our experiments it is observed that the spurs would be dominant if the output frequency to be generated from the DDFS is more than $1/3^{rd}$ the maximum reference clock frequency. In our case since the maximum frequency needed from the DDFS is 240 KHz, which is less than the 666 KHz, we can expect less spurs to be produced.

Table 4-1 DDFS   specifications requirements

Clock reference Frequency, FPGA	1 MHz
Resolution of DDFS	15Hz
DDFS output range	24KHz – 240 KHz
M word, Binary tuning word range	1573-15728

In our application, to reduce complexity we use a ROM-less DDFS. We don't have a ROM lookup table and instead use the MSB of the phase accumulator as the input to the DAC to produce a sine-weighted signal. Due to this method the maximum frequency that can be achieved from the DDFS is REFCLK/2. However, the output frequency of the DDFS is limited to less than REFCLK/3 in practical implementation to reduce glitches and spurs.

4.3 Digital/Analog converter:

In our application we needed to design a DAC which is

- Less complex

- Output frequency should change with a resolution of 10 Hz.

- Consumes less silicon area

- Can be easily implemented as a part of the BiST circuit.

In our application we need a signal whose frequency can be changed immediately. To meet our design specifications we designed a DAC which outputs a stair-stepped sine wave which has sine weighted amplitude levels. The amplitude levels are sine-weighted to make the output resemble more like a sine wave and reduce the distortion that will be produced due to this type sine wave. The distortion of the sine wave depends on the number of steps used to generate the sinusoidal waveform. The harmonics in output signal are due to the sample and hold nature of the signal, so it is necessary to choose a number of steps that provides a lesser number of harmonics components. We can use 8 points, the signal resembles a sine wave, but the number of harmonics is high. If we used 32 points the signal will be purer, but the amount of logic and the size of the DAC increases considerably. We therefore used 24 steps which provide us lesser number of harmonics and small area.

The DAC output will give rise to odd harmonics due to the nature of the signal and may reduce the SFDR that can be achieved through this method. In our application, the SNDR was limited to be around 50dB. The SNDR limitation is caused by the Brownian Noise and Mechanical Noise of the MEMS device. So the 24 point signal was selected since it gives an SFDR of 55dB and the DAC was designed to produce the 24 point signal. The amplitude levels of the signal were according to sine angles:

Table 4-2 Amplitude levels of stepped sine wave

Level 1	$Sin(0^0)$	0
Level 2	$Sin(15^0)$	.2588
Level 3	$Sin(30^0)$	.5
Level 4	$Sin(45^0)$	.707
Level 5	$Sin(60^0)$	.866
Level 6	$Sin(75^0)$	.9659
Level 7	$Sin(90^0)$	1

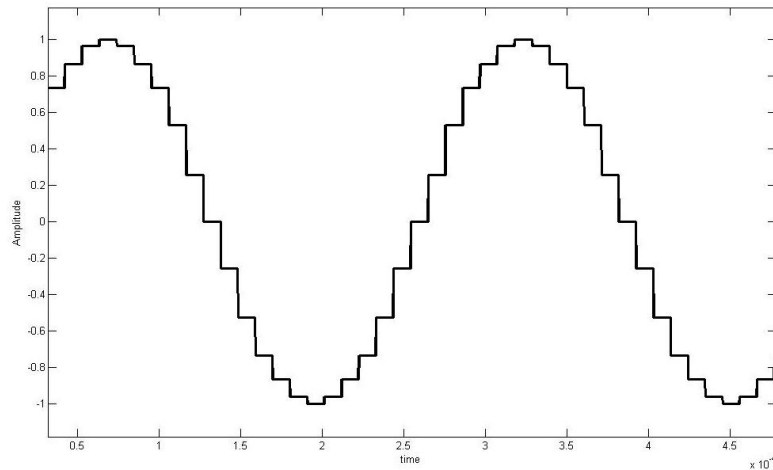The stair steeped sinewave with 24 points would be as follows :

Figure 4-8 Stair stepped sinewave

The DAC generates a signal which is applied as a stimulus to the MEMS device. The stimulus frequency is swept from 1KHz – 6KHz and the MEMS is excited at different

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frequencies and the output from the MEMS device is used to plot the Bode Plot. The device will generate an output which has a first order response.

The specification for which the DAC was designed for was:

Table 4-3 DAC specifications

Signal's Voltage Swing	.3-3 V
Output frequency range	1KHz -10 KHz
Frequency Range	100 Hz
SFDR	<40 dB
Power	400um * 400um

The DAC primarily composes of two parts:

a)Control logic

b) Sinewave Generator.

4.3.1 Control Logic:

The control logic forms an important part of the DAC and generates the logic phases for controlling the switches. It is composed of up-counter followed by a decode logic and digital logic to control the switches in the DAC. The counter used is 6 bit up-counter

which is reset every 24 cycles. The MSB bit of the DDFS's phase accumulator is used as clock for the counter.
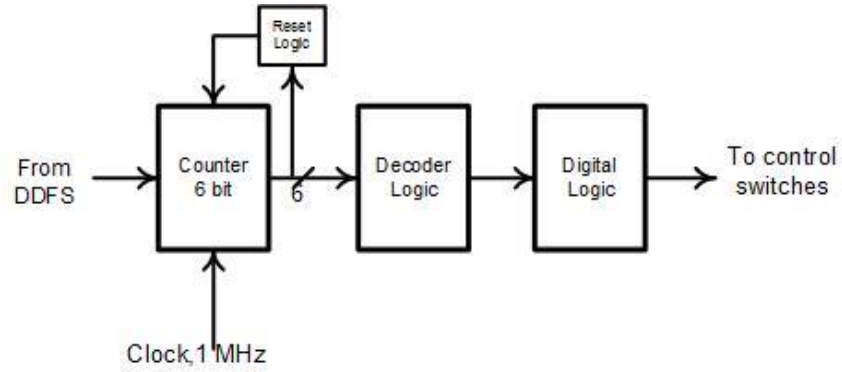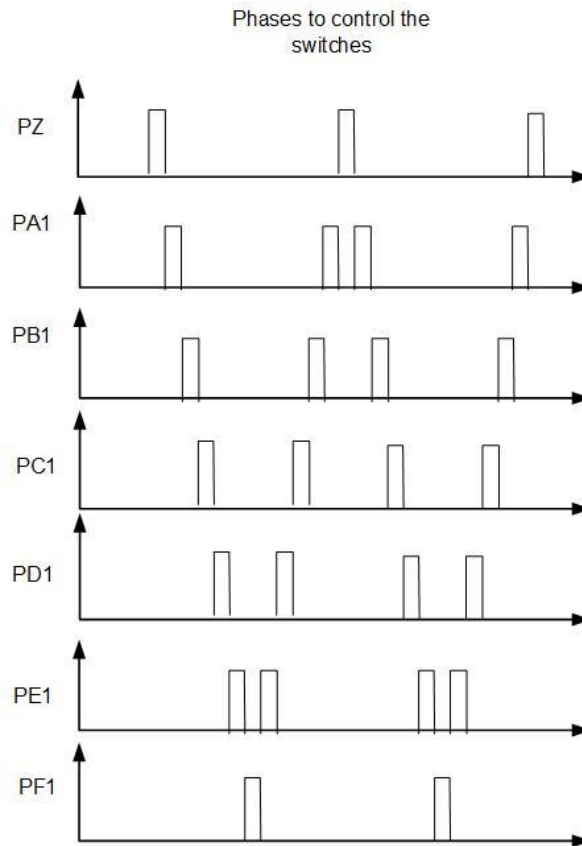

Figure 4-9 Block diagram of DAC

Figure 4-10 Phase signal to control switches

The decode logic then generates the 24 phases which are needed and the digital logic generates the logic to control the switches. The digital logic is set of OR gates which groups the 24 phases together to control the switches.

This implementation has several advantages. The logic is very simple and provides a compact implementation. By changing the clock of the counter, the period for which each amplitude value of the sine wave is held can be controlled. This makes the variation of the output frequency easier. The following are the phases generated from the logic to control the switches:

4.4 Sinewave Generator:

The Sinewave generator can be implemented in three different methods:

1) Current Steering

2) Switched Capacitor

3) Resistor String

We designed all these mechanisms and selected the one which gave us the best result and good accuracy for our application. The following section talks in detail about each of these methods and their advantages and disadvantages of each of the methods.

4.4.1 Current Steering Sinewave Generator:

The Current Steering DAC uses a set of 12 current sources to generate the sine-weighted signal. The current sources whose ratios are sine-weighted either sink or source current to the circuit and this is converted to voltage by a transimpedance amplifier. The current

sources/sinks are turned on/off by the switches that are controlled by the phases from the Control Logic.
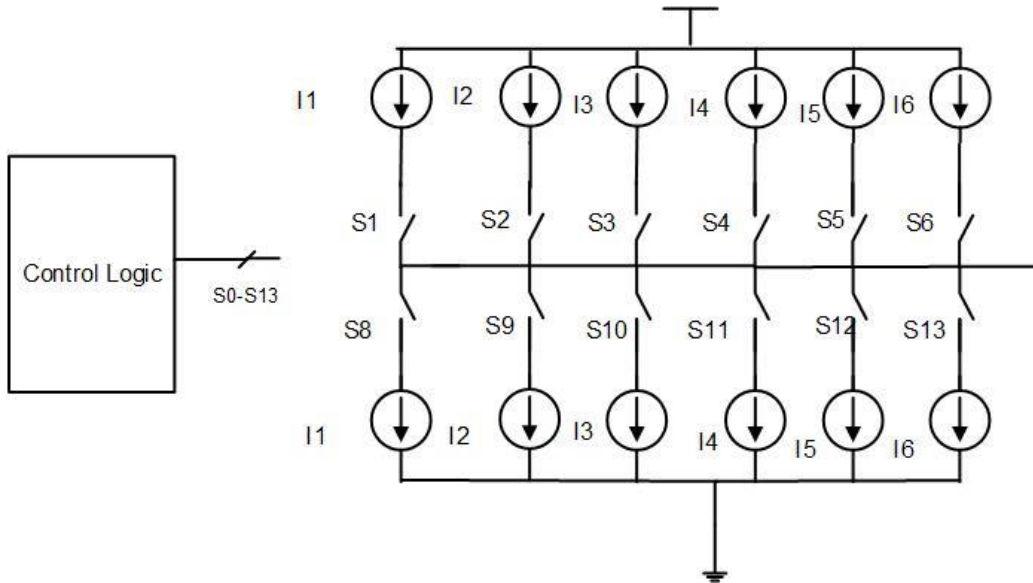
Figure 4-11 Current steering DAC

When all the current sources were on the, the sum of the current that is flowing through the entire network was designed to be around 100 uA. The individual current sources/sink were I1=26uA; I2=24uA; I3=21uA; I4=16uA; I5=10uA; I6=3.3uA. The ratios of current sources were achieved by changing the ratio of the current source replicating transistors. The entire current was converted to voltage at the output by using a Transimpedance amplifier. The transimpedance amplifier was then hooked up to the MEMS device. The following figure shows the implementation of current steering DAC.
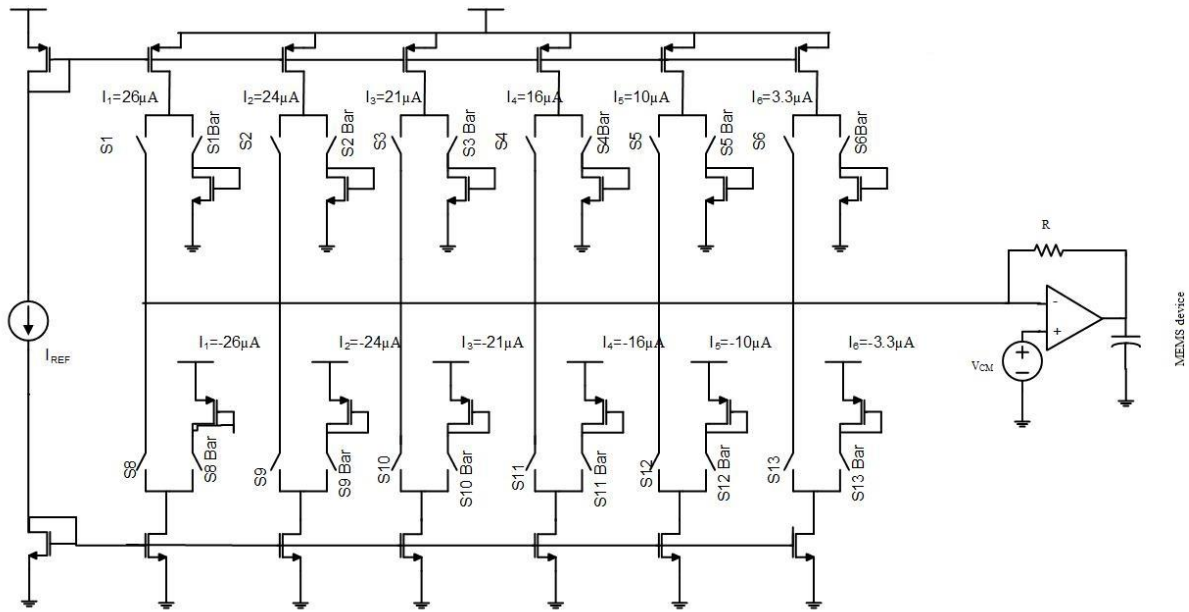
Figure 4-12 Circuit implementation of current steering DAC

The accuracy of the current sources/sinks is very important and the matching of them play a very important role in the signals amplitude value. The mismatch in the current sources will create harmonics and the mismatch error of them varies for different PVT corners.

4.4.2 Switched Capacitor DAC:

The switched capacitor DAC is designed to convert the Phase to Sine weighted amplitude. It is composed of a Switched capacitor array and an integrator. The capacitors in the capacitor array are ratio metrically sized to produce sine weighted signal. There are 24 different clock phases which control the switches of the capacitors in the bank. The clock phases are designed to produce non-overlapping phases. The capacitors are all

hooked up to a voltage source $+V_{ref}$ /- V_{ref} for 23 of the clock phases and at a specific

Figure 4-13 Capacitive DAC

The values of the capacitors in the bank are calculated according to:

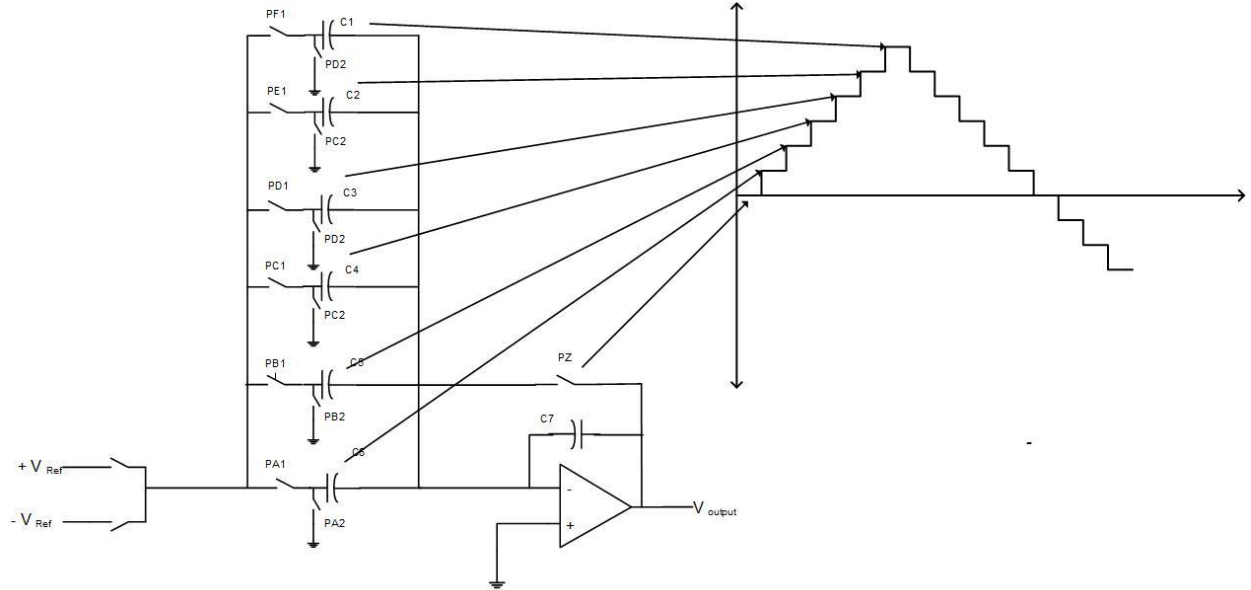Table 4-4 Calculation of capacitors values in array

$$\frac{C_6}{C_0} = sin(15^0) - sin(0^0) \qquad \frac{C_5}{C_0} = sin(30^0) - sin(15^0)$$

$$\frac{C_4}{C_0} = sin(45^0) - sin(30^0) \qquad \frac{C_3}{C_0} = sin(60^0) - sin(45^0)$$

$$\frac{C_2}{C_0} = sin(75^0) - sin(60^0) \qquad \frac{C_1}{C_0} = sin(90^0) - sin(75^0)$$

phase pulse the charge stored on the capacitor is transferred to the integrator capacitor. All of the banks capacitor's charges are transferred to the integrator capacitor. A similar approach has been implemented in [8] .

Once the maximum amplitude value is obtained, the V_{ref} is switched from $+V_{ref}$ to $-V_{ref}$ so that the lower half of the signal is generated. There is a reset switch which produces the zero-crossing two times for the signal. This method is very simple to implement and since it is generated using a digital signal, it makes frequency very precise and easily controllable.

The minimum capacitor was set to 302fF and the final value of the capacitors were as follows:

Table 4-5 Capacitor values used in array

C_1	302fF	C_4	1.867 pF
C_2	898 fF	C_5	2.15 pF
C_3	1.43 pF	C_6	2.34 pF

The capacitor sizes play a major role in signal amplitude levels. If we use a small capacitor we can lose charge from the capacitor due to leakage and the charge that is transferred to the integrator will be an incorrect value. If all the capacitors in the bank lose charge, this charge loss adds up and the output of the sine wave will not have the exact amplitude levels. We can see a droop in the voltage stored in capacitor and this is disadvantageous, since it generates more harmonics.

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4.4.3 Resistor DAC:

This DAC is composed of a resistive string and very simple to implement. A single unit resistor was used to generate the resistor string values. The single unit resistor was combined in set of series and parallel combinations to get the nearly exact values of the chain. The unit resistance that was used was 3.7 KΩ. The resistor string values were:

Table 4-6 Resistor values used in resistive string

R1	47.3 KΩ	R5	51.95 KΩ
R2	8.32 KΩ	R6	60.29 KΩ
R3	24.73 KΩ	R7	64.62 KΩ
R4	39.89 KΩ		

These resistor string is easy to implement and very simple. It also does not have the issues like leakage which were present in the Capacitive DAC. A unit resistor value was selected to reduce any errors that occur due to matching. The resistor unit size was chosen to be 3.7 KΩ so that the effect of contact resistance and the wire resistance is very less and this reduces the voltage drop across these. By selecting large resistor string value we also benefit from the less current flowing through the chain. The output from the resistive string is then filtered using a low pass filter to reduce any glitches and harmonics. The LPF stores the voltage drop across the capacitor and the voltage drop is then buffered through a source follower. This signal is then used as an input stimuli to the MEMS accelerometer. The following figure shows the schematic of the resistive DAC.

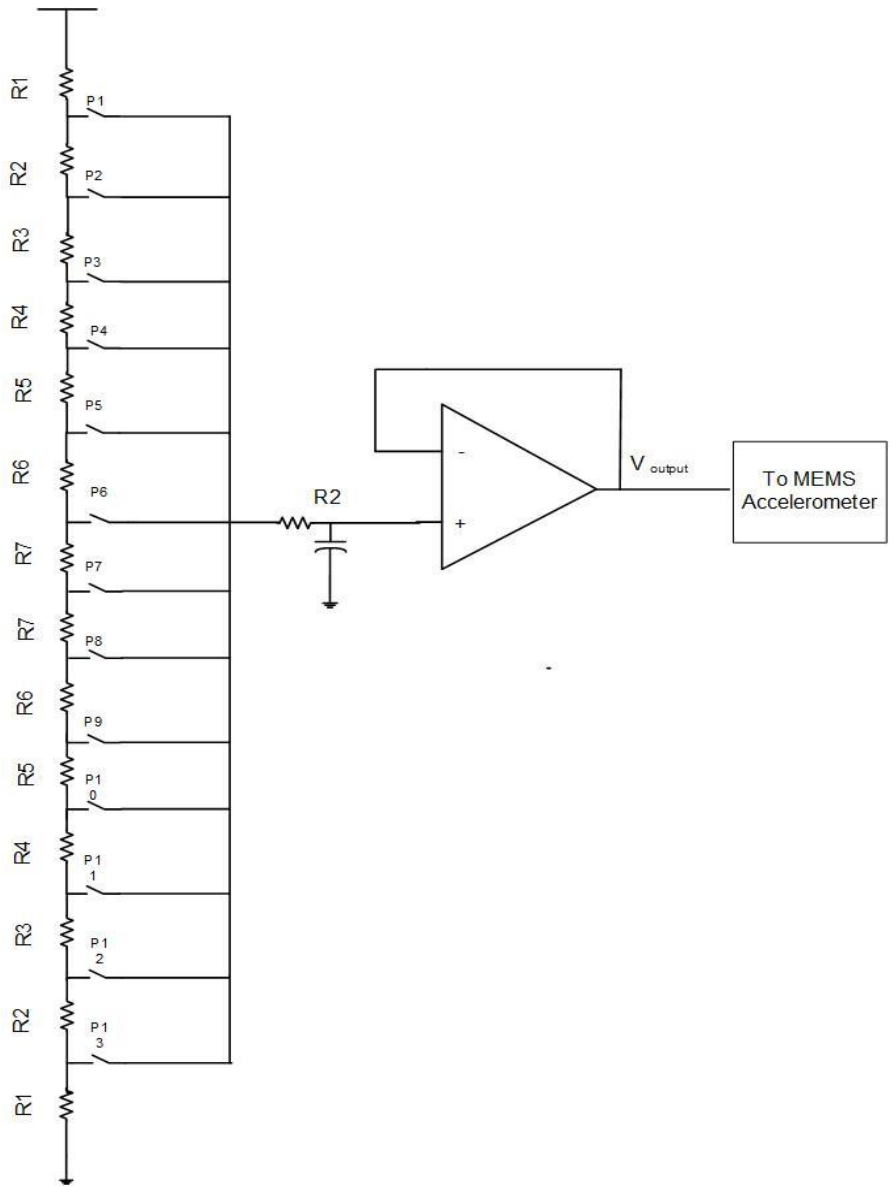**Figure 4-14 Resistive DAC**

The opamp used in the DAC's had to buffer a rail-to-rail output. The opamp designed had to have constant gain across the entire range of common-mode voltage. The following section talks about the opamp in detail.

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4.5 Rail - to - rail Op-amp:

The differential amplifiers can be mostly used as operational amplifiers in a voltage follower. The only disadvantage of using a PMOS/NMOS differential amplifier is that it will only have a limited range of common-mode input of 0.3- 3 V. The better solution to this problem is to use a rail – to –rail amplifier.

4.5.1 Input Stage:

The Rail – to – rail amplifier has a complimentary differential input stage. This op-amp has both n-type and p-type input pairs and both work simultaneously. This technique allows a direct implementation of linear weighted addition of continuous-time signals from the individual differential pairs. Common mode rail –to –rail capability is achieved by using NMOS differential pair with conductance, g_{mN} and PMOS differential pair with transconductance g_{mP} in parallel:

$$g_{mt} = g_{mN} + g_{mP}$$

This op-amp has three operating regions with respect to the input CM voltage range:

1) When the input CM voltage is threshold voltage (V_T) plus a saturation voltage above the negative power supply, only n-channel transistor pair is on. The range extends from $V_{gs} + V_{sat}$ above the negative power supply to positive power supply.

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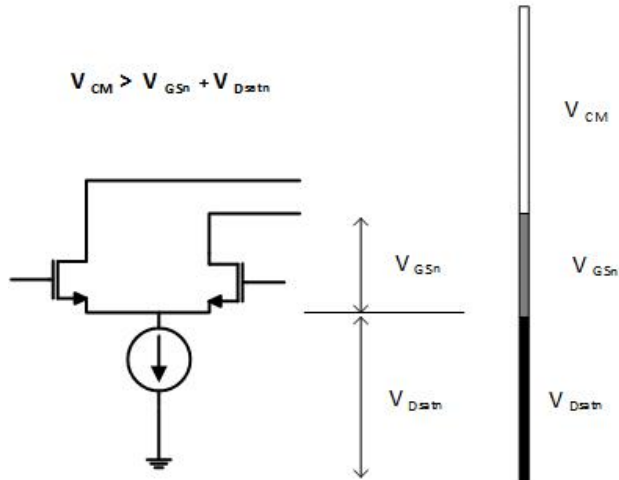
Figure 4-15 NMOS differential pair common mode input range

2) When the input CM voltage is threshold voltage and a saturation voltage below the positive voltage supply, only the n-channel input pair is on. The range extends from negative power supply to $V_{gs} + V_{sat}$ below the positive power supply.
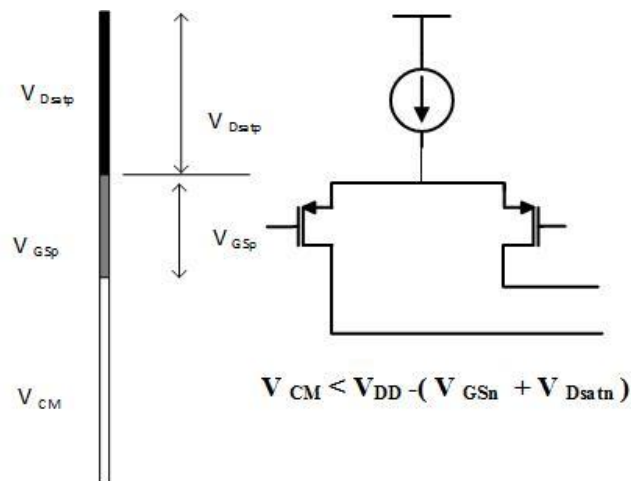
Figure 4-16 PMOS differential pair common mode input range

3) If the CM voltage is between these two limits, both the transistor pairs are on.
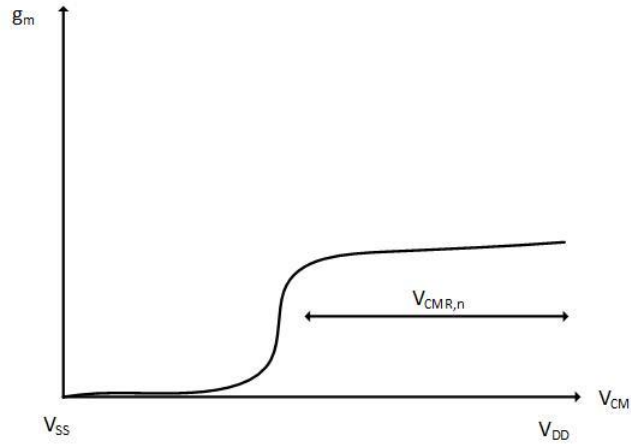
Figure 4-17 NMOS differential pair transcondcutance VS input common mode

Figure 4-18 PMOS differential pair transcondcutance VS input common mode

For a low common mode input, the PMOS differential pair is in saturation and NMOS is off. For high common mode input, the NMOS differential pair is in saturation and PMOS is off. If the common mode is in the middle region bot the pairs are working and the g_{mt} is higher. The following figure shows the transconductance versus NMOS, PMOS input pairs.

Combining these two graphs gives the transconductance versus input common mode of the complimentary pair as follows:

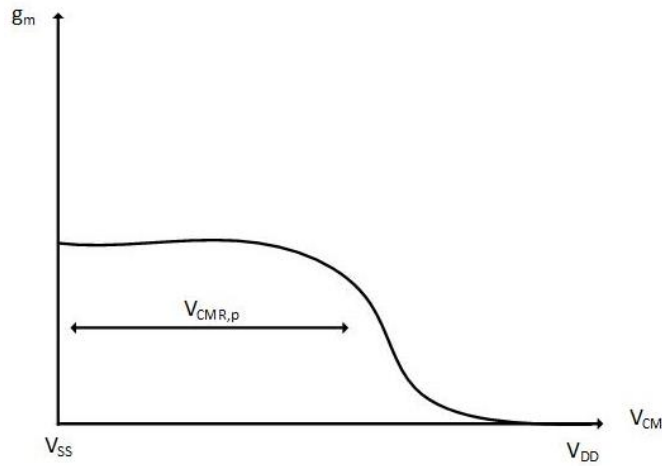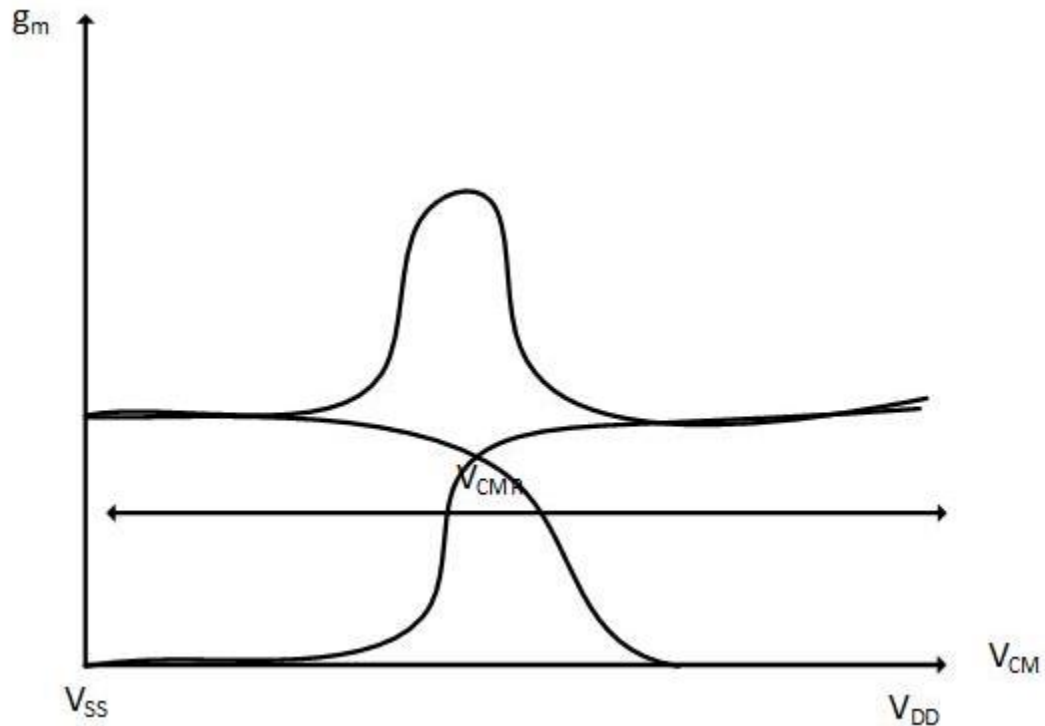**Figure 4-19 Complementary differential pair transconductance VS input common mode voltage**

The transconductance of the complimentary differential pair is almost constant for high or low common mode input when only one of the input pair is active. Both the PMOS and NMOS pair are designed to produce the same g_m. In the middle region, both the pairs are active and the transconductance is twice that of the other regions. In conventional use, this large variation of g_m change is not desirable. But in our application use, we use this op-amp in a voltage follower. The gain of the voltage

follower is around unity because of the negative feedback in the circuit. So the change of the op-amp's gain does not drastically change the outputs accuracy level.

Figure 4-20 Circuit diagram of Rail-to-rail opamp

The figure shows the op-amp and the current that flows through each node. The ouput sage sources or sinks the current. The current from the input pair's tail current is mirrored to the output. The PMOS input pair and the NMOS input pair are sized to provide the same g_m across different input common mode ranges.

4.6 Simulation & Results:

This section explains more about the results, layout, post-layout extracted simulations. We talk in detail about the simulation results of the Switched Capacitive DAC, the Resistive DAC and the op-amp used in these circuits.

Switched Capacitive DAC:

The switched capacitor DAC was designed using a 180nm analog process. The following is plot of the transient signal that is generated. The issues of using this type of DAC was leakage of capacitor array and thus creating droop in the signal.
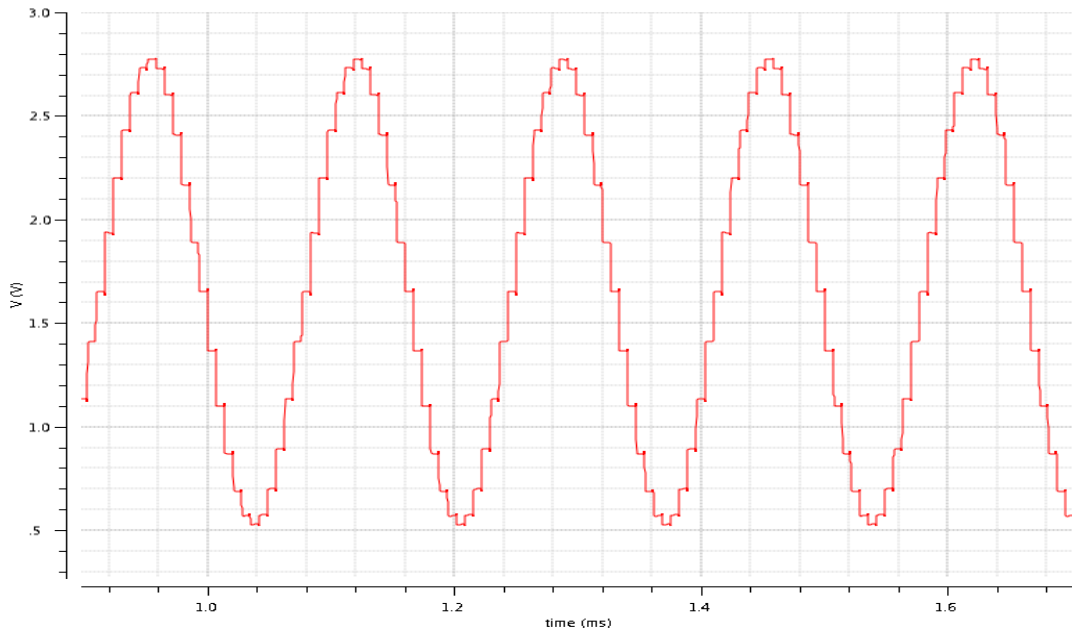

Figure 4-21 SC DAC output

Resistive DAC:

The resistive DAC is the one which was finally fabricated as a part of the chip as it provided better harmonic distortion and easy to implement. The DAC was designed and taped-out in a 180 nm analog process.
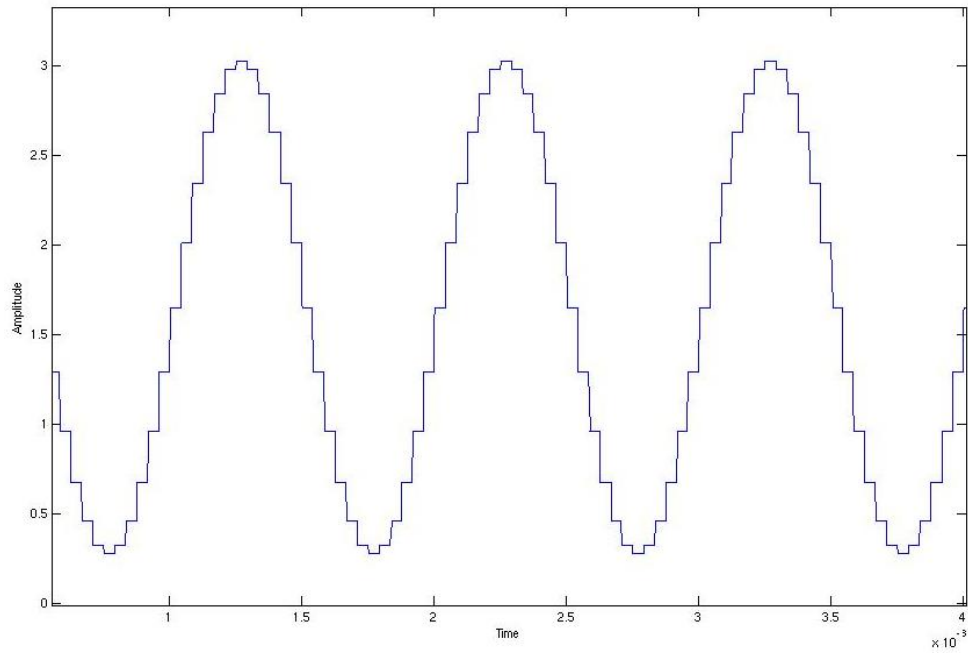
Figure 4-22 Resistive DAC signal generation

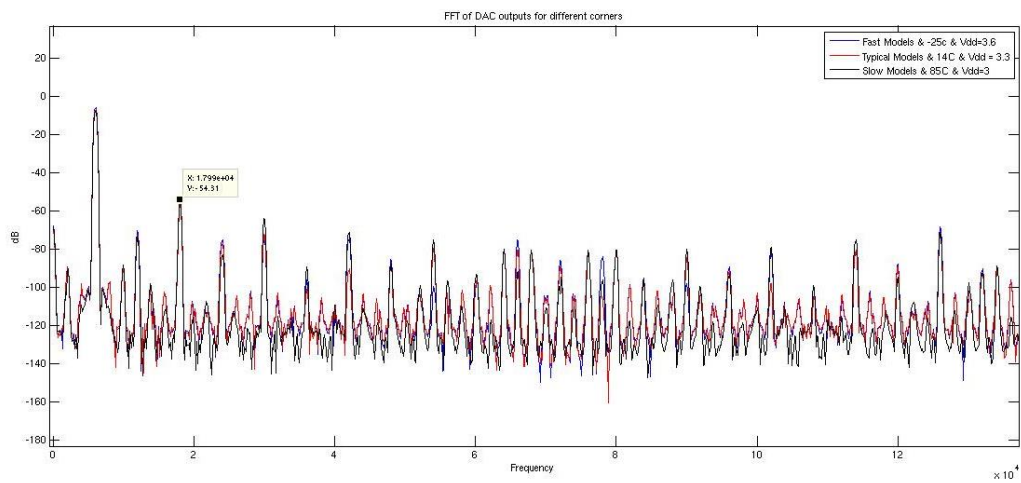The following plot shows the FFT of the DAC signal at different corners of the

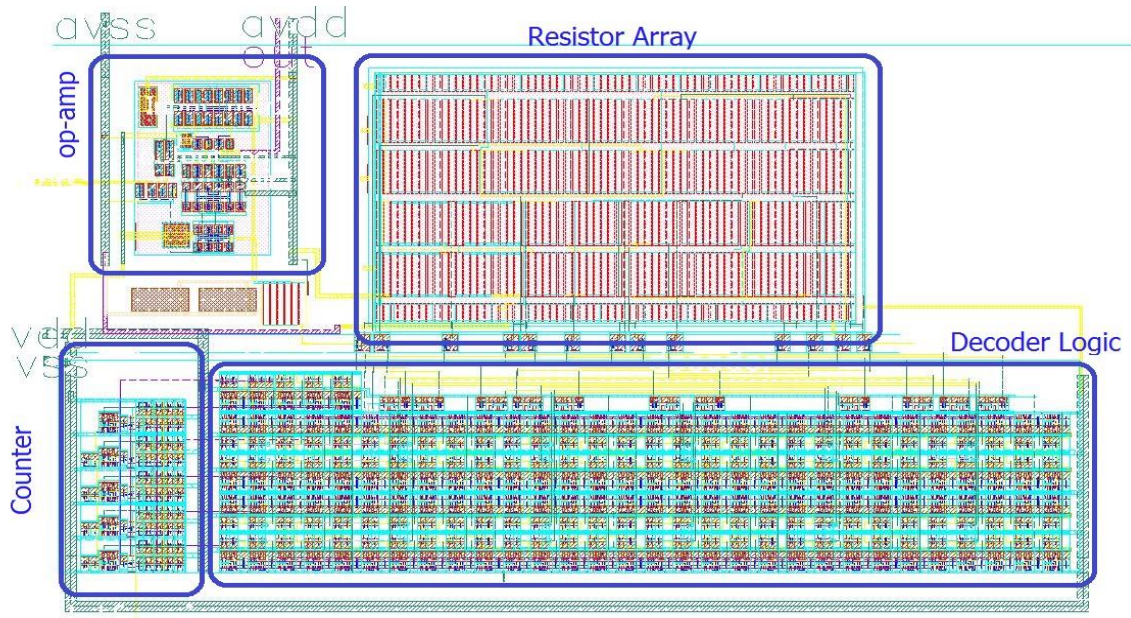**Figure 4-23 FFT of signal at different corners**

Figure 4-24 Layout of DAC

CHAPTER 5 : TESTING AND CALIBRATION MECHANISMS

5.1 Statistical Framework:

The cost of testing the MEMS device contributes to 20-30% of the total cost of the device. The MEMS accelerometers are tested using physical stimulus in an ATE and this testing is necessary to calibrate the MEMS devices. The MEMS testing involves two phases of testing: static measurement tests and dynamic measurements.

Presently in the industry a setup for testing the MEMS devices consists of ATE, handler nest and physical stimulus. The ATE provides a known acceleration into the device creating a mechanical displacement or acceleration from an electro-dynamic shaker through multiple mechanical interfaces into the MEMS device under test. Accelerometer applications usually employ a shaker system to provide the input excitation with typical accelerations ranging from 1G to 15G. Shakers commonly use a sinusoidal or pulse waveforms and the size of the shaker and input excitation waveform is determined by acceleration amplitude and frequency range.

In our approach we use two stages of statistical framework. The first stage consists of MEMS devices being excited using the electrical stimulus and then the same devices excited using the physical stimulus. The output of these electrical responses and mechanical responses are used to train the mapping engine. Once we have trained the mapping network to a certain confidence we can use the Statistical framework in the next stage of our approach. The next stage of the framework consists of exciting the MEMS devices with electrical stimulus and then using the data collected from the electrical response to predict and estimate the calibration coefficient of the device.
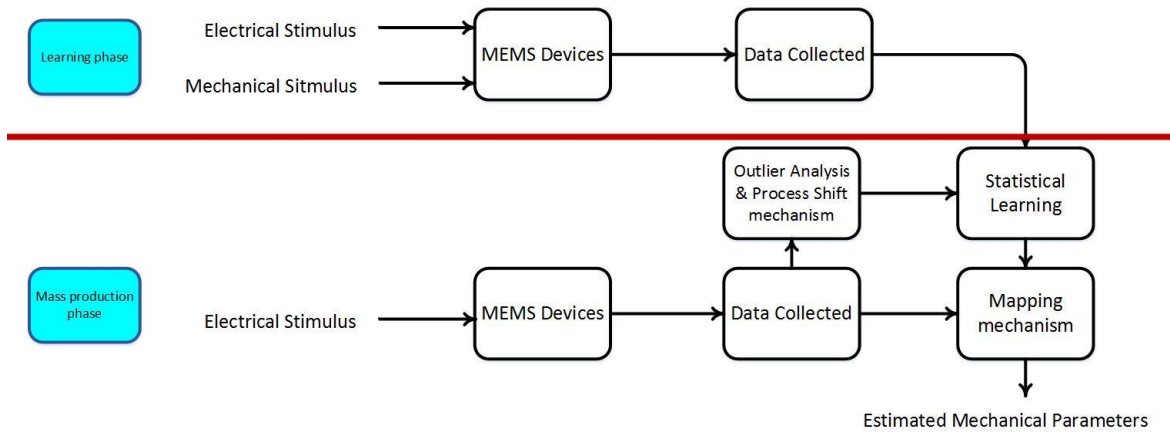
Figure 5-1 Statistical Framework

5.2 Test Set Reduction:

In the process of testing devices on an ATE, many tests conducted are correlated and at times tests conducted are redundant. Using data from individual tests to detect the outliers is not always efficient. Since multiple tests are correlated we need to use a mechanism which takes into account the correlation between tests and reduces the test set. This is becoming more important since the time spent for testing each device on an ATE will contribute to the final cost of the device. The optimized test set will consists of reduced meaningful tests and the time spent for the tests will be lesser.

In our case for a MEMS accelerometer, in the industry many redundant tests are conducted. The test set data from one of the fabrication unit for a 3-axis MEMS accelerometer has been analyzed as a part of this thesis. The number of tests conducted for these devices are around 182 and these have been conducted on all the devices. The data from these tests are highly correlated and show correlation as high as 1. Taking the correlation into account we can reduce the test set to save money and time. After doing

the analysis on the correlation, the test sets can be grouped into different clusters. Following figure shows one such cluster:
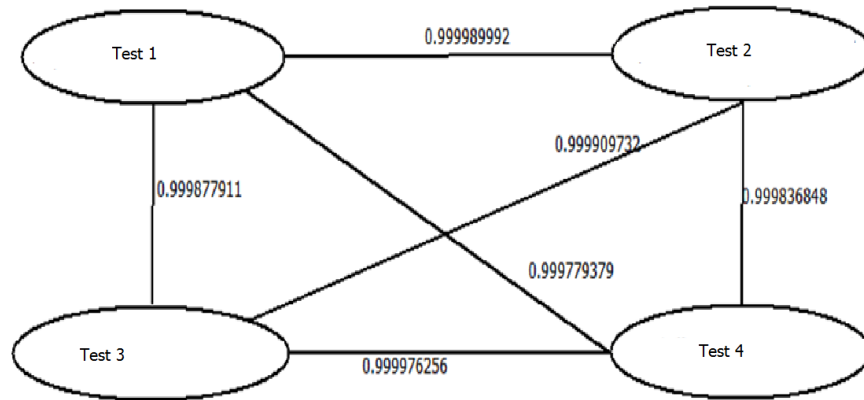

Figure 5-2 Correlation of tests in cluster

The correlations between these tests are above 0.9999. These tests are highly correlated that data from one of these tests in the cluster will suffice to determine if it is defective or faulty device. So taking into account the correlation between these tests and cluster formed, we can reduce by selecting a few tests from each cluster. Thus the test set can be reduced to contain only tests which contribute to outlier detection analysis or fault detection of the devices. In our case the compacted test set was reduced to only 72 tests compared to the original 182.

The test set consists of many tests and data from each test may help in identifying defects. Typically univariate outlier detection analysis is used to detect faulty devices. At times the defects at times pass each of the univariate outlier analysis thus contributing to high DPPM. These defective parts can be detected based on multivariate outlier analysis.

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The data from each of these test variables will be considered while determining pass/fail. If there are P test variables, the data from each of these variables will be taken into consideration during the outlier analysis detection. The metric used in this Multivariate outlier detection analysis is known as Mahalanobis Distance.

5.3 Mahalanobis Distance:

Mahalanobis distance (MD) [9] is a commonly used distance metric in multivariate outlier detection analysis. MD is a distance metric which estimates how far each device is far from the center of variables distribution. MD accounts for different scales and variance of each of the variables in a probabilistic way. It accounts for the variances of the variables, covariance between the variables. MD takes into account the correlation between two variables. In order to measure MD we first apply linear transformation that uncorrelates the data and then calculate the Euclidean distance of the points [10] .

MD is defined as :

$$MD(x_t) = \sqrt{(x - \mu)^T S^{-1}(x - \mu)}$$

Where

μ- Mean of the variable

S^{-1}- Inverse covariance matrix.

The variance-covariance matrix between two variables x_1 and x_2 is:

$$S = \begin{bmatrix} \sigma_1^2 & \rho_{12}\,\sigma_1\sigma_2 \\ \rho_{12}\,\sigma_1\sigma_2 & \sigma_2^2 \end{bmatrix}$$

Where

σ_1^2, σ_2^2 – Variances of the values

$\rho_{12}\,\sigma_1\,\sigma_2$ – covariance between the variables

$$S^{-1} = \begin{bmatrix} \sigma_2^2/\det(S) & -\rho_{12}\sigma_1\sigma_2/\det(S) \\ -\rho_{12}\sigma_1\sigma_2/\det(S) & \sigma_1^2/\det(S) \end{bmatrix}$$

For our analysis we have used 72 tests to determine the outliers. The MD is calculated using the above equation. The threshold used for determining the outliers can be determined from the chi-square plot. The threshold can be determined based on the quantile and the number of test variables used. The threshold should be adaptively computed to take into account the shift in the process variables. The below plot shows the MD of 81000 samples plotted in a sorted order. The samples in the red indicate outliers and the samples in blue are inliers.
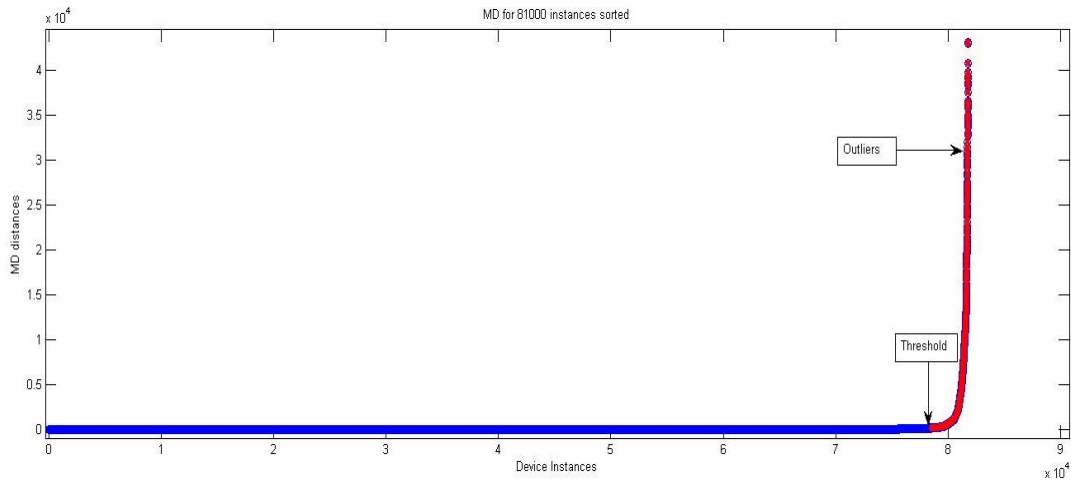
Figure 5-3 MD of 81000 samples sorted

If the threshold set is stringently a few device samples which are outliers are detected as inliers. This causes an increase in DPPM. The reason that the outlier was not detected might be based on the fact that the noise from all the other tests might have masked the outlier. In order to prevent this from happening we have developed an algorithm which detects the outliers more efficiently. The following section highlights the seeding algorithm.

5.4 Seeding Algorithm:

The test variables used to calculate the MD can at times mask some outliers. These outliers/defects may pass through the manufacturing line and might be shipped to a customer. This will cause and increase in DPPM. In order to reduce the DPPM we would have to catch these outliers before being packaged. To detect these defective devices we use a subset of the test variables to detect the outliers. The devices which are inliers are tightly correlated. Those that are not correlated are present away from the ellipsoid

distribution. For example we can use 3 test variables to detect the outliers. The following is the 3D plot of the devices and each of the axes represent an individual test.
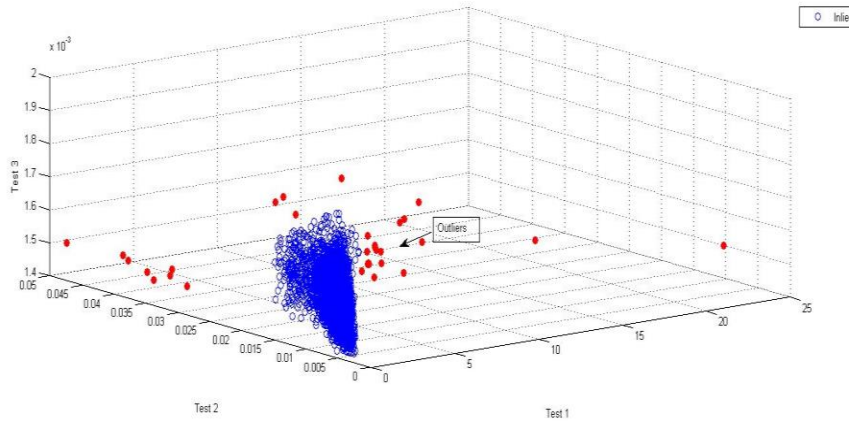

Figure 5-4 3D Scatter plot of devices

The below plot shows that inliers (in blue) are tightly correlated and the outliers (in red) can be easily identified. The following part explains the algorithm which takes into account the subset of the tests and will be used to detect the outliers.

We use a subset of tests to begin with to calculated the MD and identify the outliers based on these subset of tests. We start with seeds of two tests and calculate the number of outliers detected. Then we add one more test each of these seeds and observe the number of outliers that are detected. If the number of outliers detected is less, then the seed has reached a maximum detection capability and the subset has saturated. If there is an increase in the number of outliers detected we use the seeds for the next iteration.
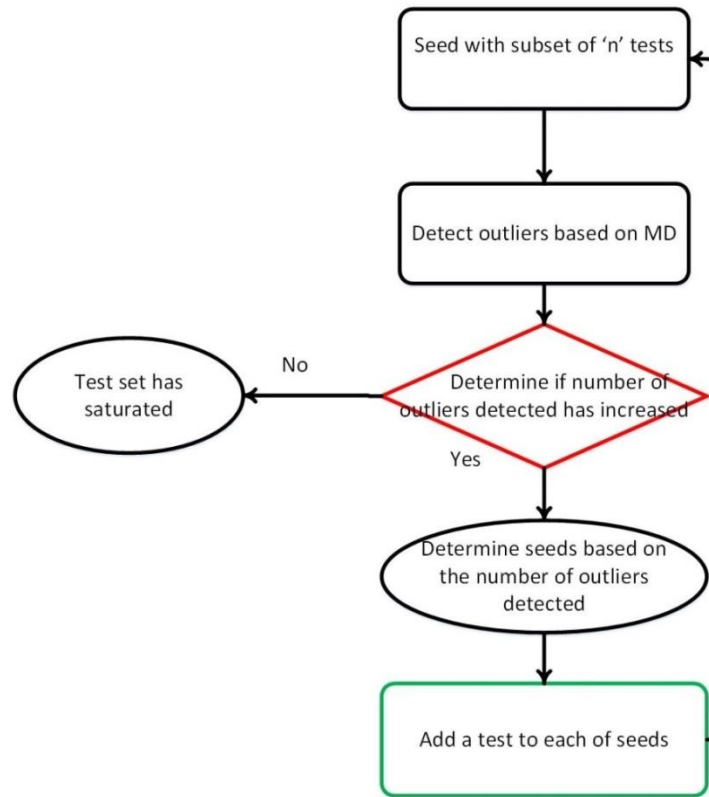
Figure 5-5 Seeding algorithm

We keep on iterating till have enough number of seeds and subset of tests to comfortably detect the outliers. In this analysis we have started with two seeds and grew the seeds till we detected majority of the outliers. We have restricted ourselves to seeds containing 4 tests since we have detected majority of the outliers based in these seeds and also due to large computation time involved in each simulation.

Case study : For example we started with a seed which contains data from test variable-20, 56. The numbers of outliers detected was 252 devices. Then we add an individual test to the seeds and calculate the number outliers detected. The new seed which contains

test- 20, 56, 36 was able to detect the 708 outliers. We again add one more test in the next iteration and we observe that the seed having tests- 20,56,36,38 was able to detect 929 outliers. A similar process is followed for many seeds and the final set of seeds is formed. These seeds will then be used to detect the outliers from the test data and this helps in reducing the DPPM. This is also an efficient mechanism to detect outliers.

5.5 Statistical mapping framework:

We have developed a mechanism to replace the physical stimuli applied by ATE during the testing of MEMS accelerometer with an electrical stimulus. The stimuli we have chosen is an Stair-stepped sine wave and the method of generation of this signal using a DAC was explained in previous section. The MEMS device acts as second-order filter and would not respond after a certain range electrical signal frequency.

When we apply an electrical signal to the MEMS device it moves at twice the frequency since the equivalent Force and voltage are related by square law.

$$F = \frac{\varepsilon_0 A}{2} \left(\frac{V}{d}\right)^2$$

But, $F = m.accel$

Thus, $accel \; \alpha \; V^2$

Thus if we apply a *sin(x)* signal we then see device to move at *1-cos (2x)* frequency.

Thus the output from the MEMS device will be observed at twice the stimulus frequency.

MEMS accelerometer is an inertial sensor whose natural frequency is defined as [11] :

$$\omega_n = \sqrt{\frac{k}{m}}$$

and the mechanical quality factor is defined as:

$$Q = \frac{\sqrt{km}}{b}$$

The accelerometer is said to be underdamped if Q>0.5, critically damped if Q=0.5 and overdamped if Q<0.5. In our case the damping ratio is around 0.7 and the natural frequency is also the resonant frequency. The sensitivity of the accelerometer is given by:

$$\frac{x}{a_{in}} = \frac{m}{k} = \frac{1}{\omega_n^2}$$

The resonance frequency for the accelerometers is typically around few KHz. They have a second order response and the gain/sensitivity of the accelerometer will roll off after the resonance frequency. They would stop reacting to any signals which have frequencies higher than that of the resonance frequency. They typically don't react to signals of high frequency. For example they would not respond to signals with 1MHz frequencies. The

figure 5-6 shows the capacitance change across different frequencies. It rolls off after natural frequency showing a response similar to that of a first order filter.

In a parallel plate capacitor, when an electrical stimulus or acceleration is applied then the proof mass moves and there is change in the distance caps. The capacitance sensitivity to distance changes a gap distance x_0 is given by:

$$\left.\frac{dC}{dx}\right|_{x=x0} = \left.\frac{d}{dx}\left(\frac{C_p}{x}\right)\right|_{x=x0} = \frac{-C_p}{x_o{}^2} = -\frac{C(x_0)}{x_0}$$

The output voltage that will be sensed will be dependent on:

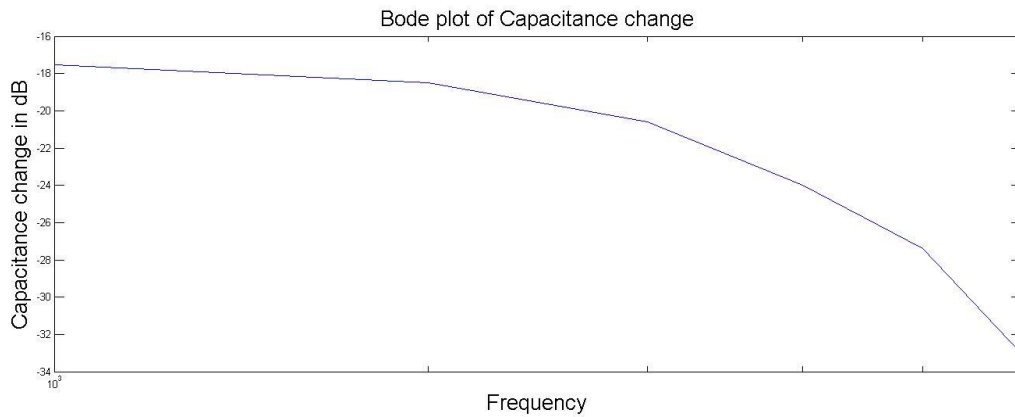$$V_{sense} \; \alpha \; \frac{x}{x_0} V_m$$

Figure 5-6 Bode plot of capacitance change

The following section explains a methodology that is followed to map the electrical stimulus response to that of the mechanical stimulus response. We used a Verilog model of the MEMS device to develop this methodology. We have varied various MEMS

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parameters and used the responses in the mapping network. The parameters that were

varied are

Table 5-1 MEMS capacitor typical values

Parameter	Typical Values
Mass	3.4e-9 (g)
Spring constant	3.5 (N/m)
Damping ratio	.7
Intial Gap	0 (um)

The above parameters were varied in the model. We applied an electrical stimulus to the

model and applied a mechanical stimulus to the same device. The data from the output of

the electrical response was observed. The different outputs that were observed from the

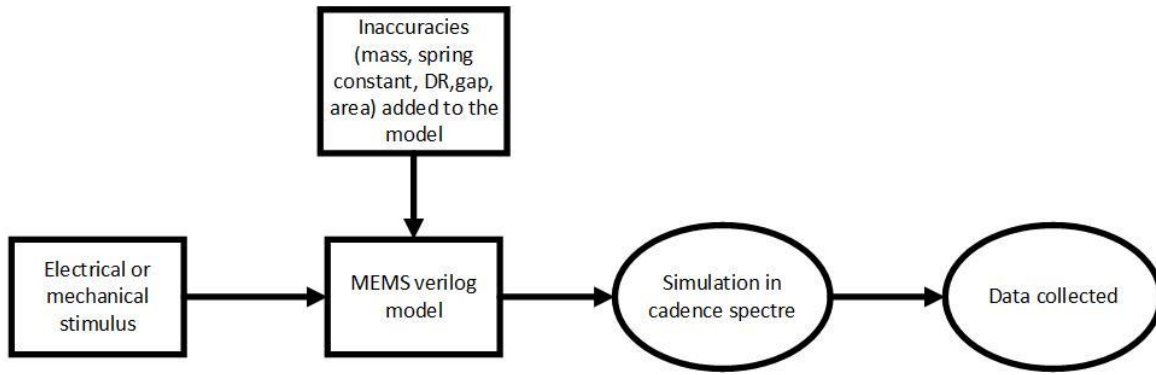model were capacitance change, displacement, voltage change at the plates.

Figure 5-7 Simulation setup

Similarly for the mechanical stimulus we observed similar data. We then used a Neural Network to develop the mapping mechanism. The following figure shows the statistical frame work that was used in this learning process.
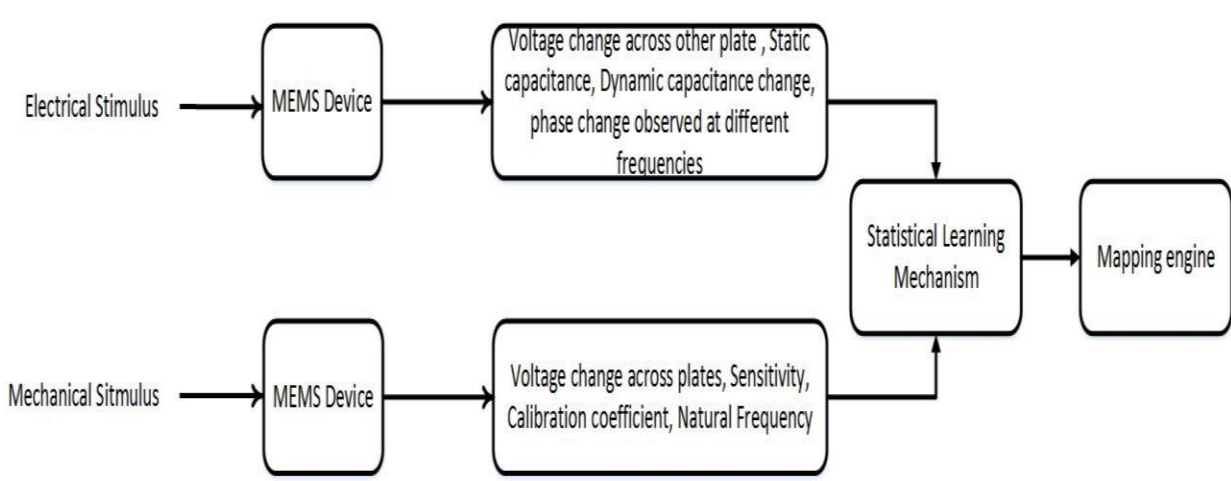

Figure 5-8 Mapping mechanism of Electrical and Mechanical mechanism

Neural Network for statistical mapping:

The neural network tool box provided by Mathworks has been used to train and develop a statistical mapping engine. We would train the neural network with 900 samples and the parameters that would be used to train the neural network would be capacitance change,

the initial gap. The output that would be targeted is the capacitance change when a mechanical stimulus is applied. This mapping network would then be used to train the new electrical response data to estimate the calibration coefficient.

Case Study I: Electrical voltage change to Mechanical Capacitance variation (ideal response):

The data such as capacitance change, displacement change, voltage change and initial gap are collected from these simulations. The data is collected for both the electrical response of MEMS device and mechanical response of MEMS device. Of the information we have from simulations we would give more importance to the capacitance variation since the calibration coefficient is directly related to the capacitance change and is used to trim and calibrate the MEMS device.

The capacitance change from simulation data for all six frequencies will be used for the training the mapping network. The mapping network will try to map the capacitance variation from electrical stimulus response to that capacitive variation of mechanical stimulus response. The following shows the mapping of the electrical capacitance change to that of mechanical capacitance change.

Table 5-2 Neural network training

Inputs to the network	Electrical Capacitance Change (fF) and initial gap (um)
Target to the network	Mechanical capacitance change (fF)

The MSE calculated was 1.7e-22. The number of samples that was used for training was around 900 and number of hidden layers that was used to train in this network is 25. It took 28 iteration/epochs to converge. The trained network was used to predict a 100 samples and the following was the prediction results.

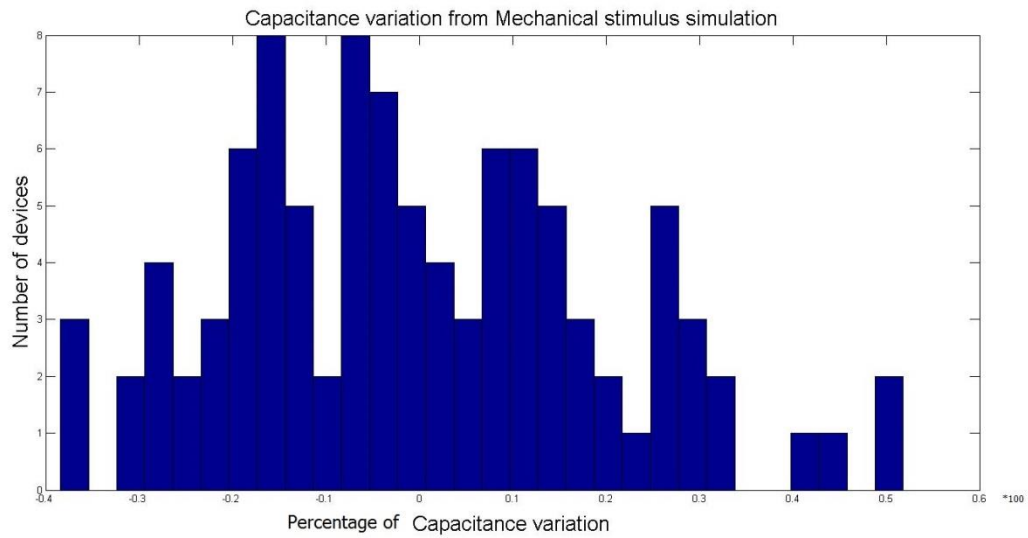Capacitance change from Mechanical response (Histogram):

Figure 5-9 Histogram of capacitance change from Simulation

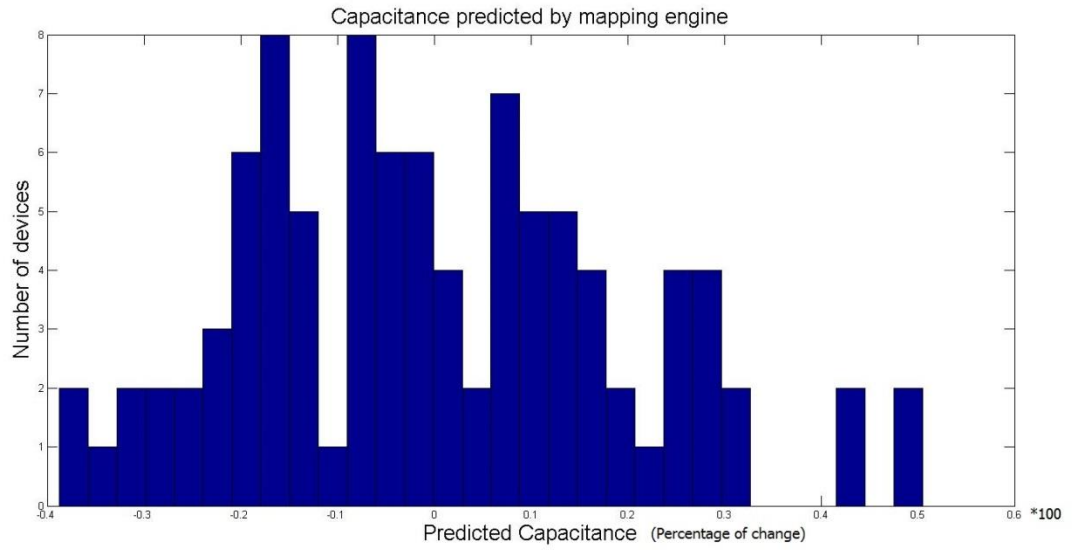Predicted capacitance change (Histogram):

Figure 5-10 Histogram of predicted capacitance change by Neural Network

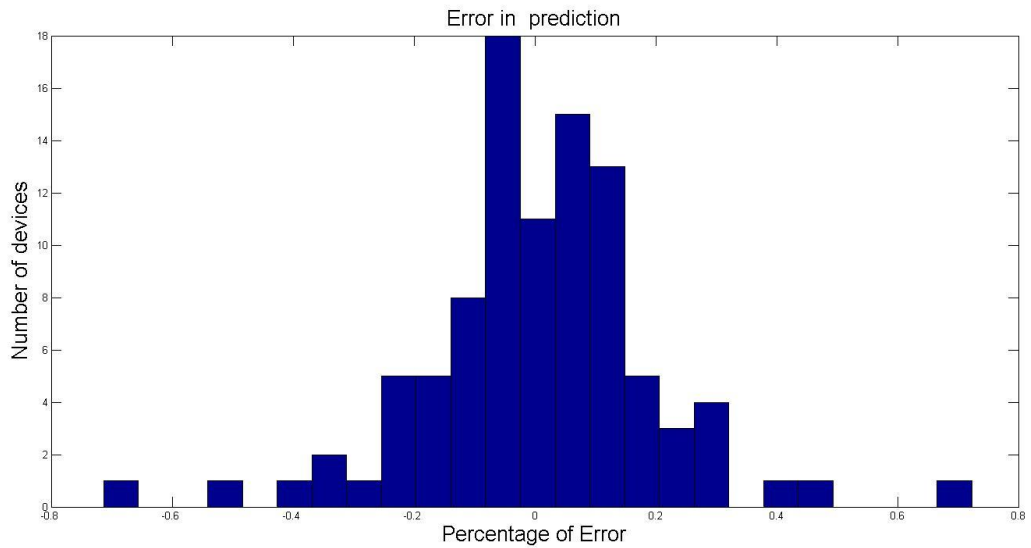Error in prediction (Histogram):

Figure 5-11 Histogram of error in capacitance change prediction

From the mapping mechanism we observe that the mechanical response cap change can be estimated from the corresponding electrical response capacitance change very well with an accuracy of 1%. From our analysis we observed that the accuracy with which the prediction was done was good. If we added BiST non-idealities to it, then the prediction is affected by the non-idealities. The non-idealities of the BiST circuit is the one that contributes to the overall increase in error. Any error is prediction in real world is primarily dominated by the presence of non-idealities in the BiST circuitry.

This approach is very beneficial since it uses the existing readout circuitry and adds very minimal overhead and complexity. This method can be used to substitute the mechanical/physical stimulus presently used in the industry and this saves a lot of cost spent on the specialized automatic testing equipment thus making it cheaper. The approach uses very simple circuitry mechanism which can be applied to other devices like gyroscopes and other inertial sensors.

CHAPTER 6 : CONCLUSION & FUTURE WORK

A new alternative testing technique has been developed which uses an electrical stimulus to test and calibrate the MEMS device. It replaces the physical stimuli presently required for testing the MEMS accelerometer used in presently in the industry. It uses a statistical framework to map the electrical stimulus response to that of the calibration coefficient of the MEMS devices. We have implemented the proposed architecture in 3-axes, comb shaped capacitive MEMS accelerometer. The BIST designed uses a lot of the existing circuitry and DAC adds little overhead to the present circuit. The new electrical stimulus calibration reduces test time and cost.

The statistical framework consists of mapping engine which maps the electrical response data to that of the mechanical calibration coefficient. The data collected from the electrical response would be magnitude response, 90^0 phase shift point and offset capacitance. The data collected from the mechanical response of the same MEMS device would be the magnitude response. These parameters would then be used in a training engine to build a mapping network. This network would then be used to map the electrical response to that of the mechanical calibration coefficient.

This statistical framework if proven efficient might be applied to other MEMS devices like gyroscope. This architecture and statistical framework will save test time and test equipment cost. Defects detected earlier will then discarded thus saving the ASIC cost and packaging cost. Thus we have demonstrated a method by which we can substitute the need for mechanical and physical stimuli thus saving the cost spent on specialized ATE's.

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