# Digital Calibration and Effective Number of Bit Prediction for Pipeline ADC

by

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# ABSTRACT

In thesis, a test time reduction (a low cost test) methodology for digitally-calibrated pipeline analog-to-digital converters (ADCs) is presented. A long calibration time is required in the final test to validate performance of these designs. To reduce total test time, optimized calibration technique and calibrated effective number of bits (ENOB) prediction from calibration coefficient will be presented. With the prediction technique, failed devices can be identified only without actual calibration. This technique reduces significant amount of time for the total test time.

***To My parents***

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# 1. INTRODUCTION

## 1.1 Introduction

Due to the rapid development of digital signal processors (DSP) and communication technology, Analog to Digital Converters (ADCs) became essential parts in various applications. However, in current technology scales, because of the requirement of high sensitivity and accuracy to fabrication and various interferences and noises from the manufacturing environments, calibration process became inevitable to generate reliable data conversion. Especially, digital calibration techniques are most popular considering digital circuits are self-error detectable, and synthesizable. Furthermore, a digitally-assisted design style becomes an increasing trend [1]. Digital calibration techniques have been popularly used in various ADC architectures such as pipeline ADCs [2], successive-approximation register (SAR) ADCs [3], and sigma-delta ADCs [4]. In the last decade, pipeline ADCs are widely employed because it has desirable speed, resolution with relatively low power consumption and small size. The ADC model used in this research is a 14-bit 1MS/s 1.5bit/stage pipeline ADC with 2-bit auxiliary ADC.

## 1.2 Motivation

In order to obtain higher reliability and accuracy in data conversion from ADC, calibration became an essential process. In addition, digital calibration overcomes the analog impairments like finite op-amp gain, op-amp offset, and capacitor mismatch. Several digital calibration techniques for pipeline ADCs [5-8] have proven its superior effect.

Testing the final performance of a digitally-calibrated ADC should be run after calibration. However, device testing and calibration process requires huge amount of time especially ADC testing due to its huge portion of data which has to be acquired to achieve its static and dynamic parameters. Effective number of bits (ENOB), in particular, is generally must be measured which represents the signal to noise ratio and distortion (SINAD). The most widely used method to calculate ENOB of ADCs [9] is to apply a sine wave to input and obtain output, then apply a coherent FFT plot to obtain SNR value. From the SNR value from the sine-wave test, use the formula for the conversion from SNR to ENOB, which is defined as

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{1.1}$$

SNR unit is dB and ENOB is presented in bits. As mentioned above, ENOB calculation needs coherent FFT plotting which takes huge amount of time for calculation compare to obtaining only calibration coefficients. Consequently, I propose a digital calibration technique for pipeline ADC and a test methodology for reducing overall test time by acquiring predicted ENOB value from calibration coefficients in this thesis.

## 1.3 Thesis Outline

This thesis is organized as following. Background knowledge of performance parameters of ADCs are explained in Chapter2. In Chapter 3, the proposed test methodology of ENOB prediction from calibration coefficients is provided. The simulation results are presented in Chapter 4. At last, the conclusion and future work are given in Chapter 5.

# 2. BACKGROUND

The basic knowledge of ADCs and performance of a pipeline ADC and kernel estimation technique will be presented in this chapter. The major parameters used to represent the overall performance of an ADC are explained in Section 2.1. Section 2.2 presents operation and structure of a general pipeline ADC. In Section 2.3, various errors occur in pipeline ADC will be given. Finally, in section 2.4, kernel estimation background will be presented.

## 2.1 ADC Performance Metrics

The most commonly used and one of the most important metrics for measuring the performance of an ADC is the signal-to-noise ratio (SNR). SNR is defined as the power ratio between the signal and the noise. SNR can be calculated easily. First, collect the output codes correspond to sinusoidal input and create a coherent FFT-plot from the output codes. Then, take the power level of the signal and comparing it to the total remaining power (except DC power). The equation for SNR calculation is shown below.

$$\mathrm{SNR}_{dB} = 10log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) = \mathrm{P}_{signal,dB} - \mathrm{P}_{noise,dB} \quad (2.1)$$

Also, SNR describes in terms of effective number of bits (ENOB). ENOB shows the overall accuracy of the ADC. The equation for ENOB is in Eq. (1). If there is quantization noise correlated to the input, a different conversion signal to noise ratio and distortion (SINAD) to ENOB should be considered. The equation for SINAD is shown below.

$$\mathrm{SINAD}_{dB} = 10log_{10}\left(\frac{P_{signal}}{P_{noise} + P_{distortion}}\right) = \mathrm{P}_{signal,dB} - \mathrm{P}_{noise,dB} - \mathrm{P}_{distortion,dB} \quad (2.2)$$

For the conversion from SINAD to ENOB is almost the same as the conversion from SNR to ENOB. Instead of SNR use SINAD in the same equation.

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{2.3}$$

## 2.2 Pipeline ADC

### 2.2.1 Pipeline ADC architecture

The pipeline ADCs are one of the most popular architecture in modern applications in advantage of its high resolution and relatively small size. A general pipeline ADC block diagram is described in Fig. 2.1. The ADC described in the block diagram has K stages and delay logic to synchronize the outputs from the each stage.

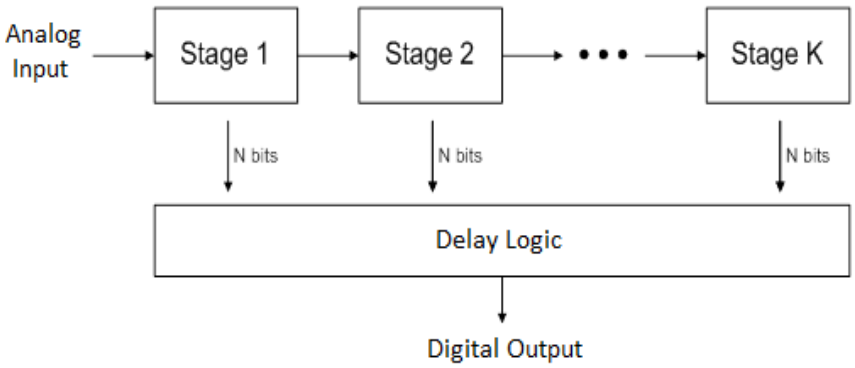


Fig. 2.1 Block Diagram of a Pipeline ADC

Each stage is consist of a low resolution typically 1 to 2.5 bit ADC and multiplying digital to analog converter (MDAC) which operates sample and hold(S/H) process, digital to analog conversion, and subtraction and amplification. One stage of pipeline ADC is shown in Fig. 2.2.

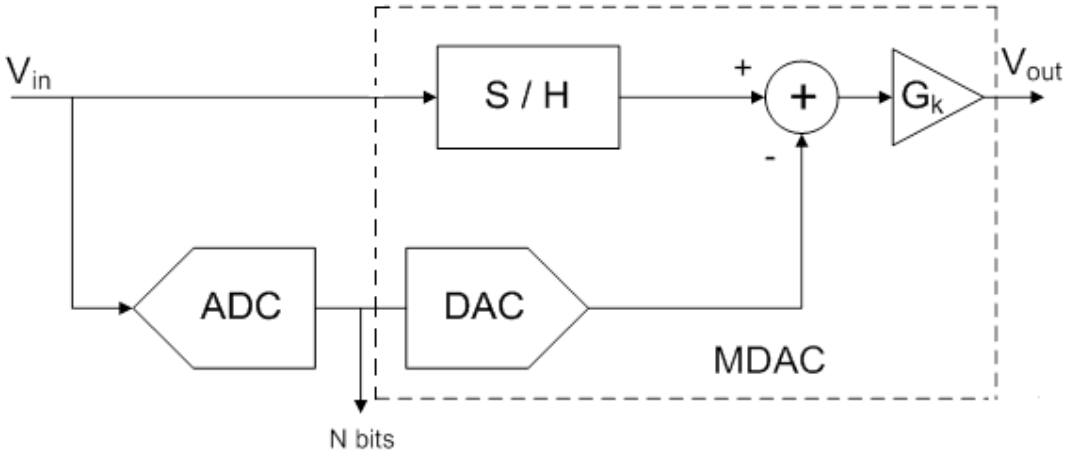


Fig. 2.2 One stage of Pipeline ADC

Each stage has identical structure and very straight forward function. The input voltage from previous stage is sampled and converted by a low resolution ADC to N bit digital code. Then, the converted code is again converted back to analog signal by DAC. The sampled input signal is subtracted by converted analog signal which is generated by the DAC. Finally, the subtracted value is amplified and sent to next stage. The signal sent to the next stage is also called residue signal or voltage. The digital output code of each stage will be added each other to acquire the final digital code of the ADC. All the stages uses the same clock, the same reference voltage, and the same gain.

### 2.2.2 Mathematical Model of Pipeline ADC

In this section, mathematical modeling for a pipeline ADC will be given. As explained in the previous section each stage of pipeline ADC has the same transfer function. Since, differential pipeline ADC is used in this thesis, the transfer function given below is for 1.5bit/stage pipeline ADC. Where $V_{out}$ is output voltage of the stage

and $D_{out}$ is 1.5bit digital output code of the stage. G is the gain of amplifier and in this case it is 2 and g consists of G – 1, so 1 in the ideal case.

$$V_{out} = G * V_{in} + k * g * V_{ref} \tag{2.4}$$

$$k = \begin{cases} -1, & V_{in} > V_{ref} \\ 0, & V_{ref} > V_{in} > -V_{ref} \\ 1, & -V_{ref} > V_{in} \end{cases} \tag{2.5}$$

$$D_{out} = \begin{cases} 10, & V_{in} > V_{ref} \\ 01, & V_{ref} > V_{in} > -V_{ref} \\ 00, & -V_{ref} > V_{in} \end{cases} \tag{2.6}$$

Fig 2.3 shows the transfer curve of each stage with the case of G>2, G=2(ideal), G<2.

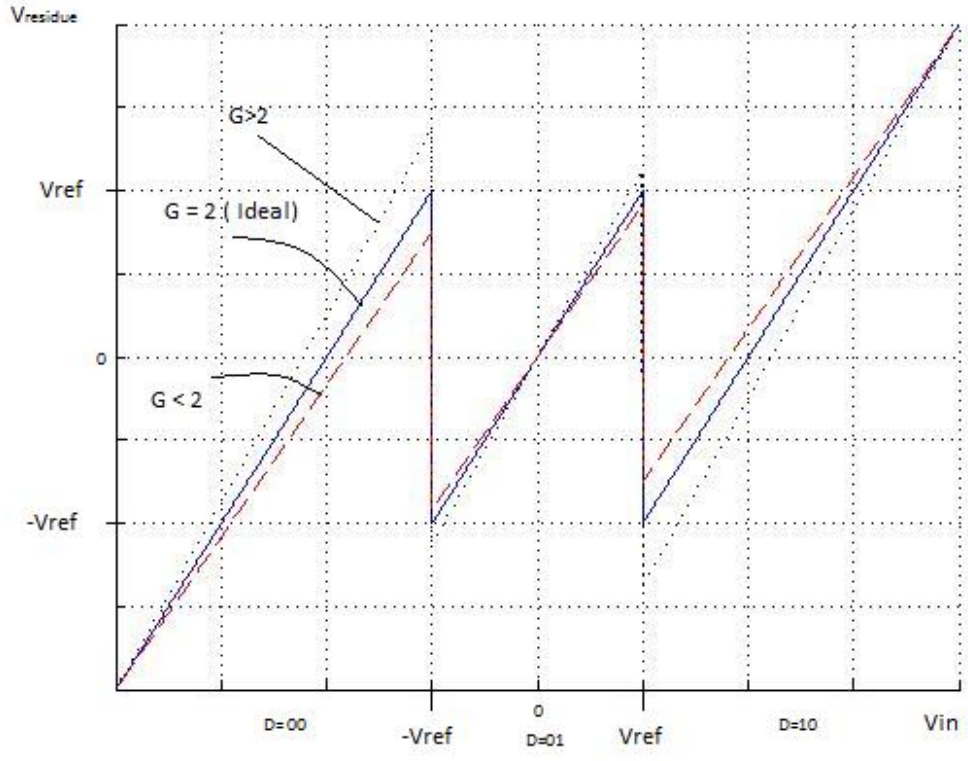


Fig 2.3 Transfer curve of stage residue amplification

## 2.3 Errors in ADC

As the input and the corresponding output are directly related in ADC, errors in the conversion are easily noticeable and measureable as long as we know the input. General errors occur in ADC are offset error, gain error, and nonlinearity errors (INL and DNL).

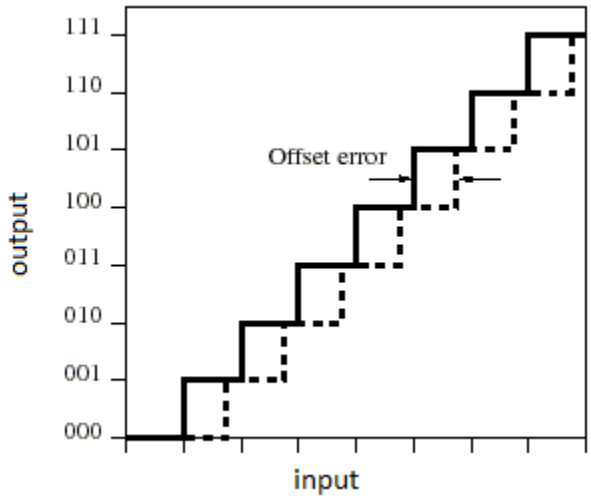


Fig. 2.4 Offset Error in a 3-bit ADC

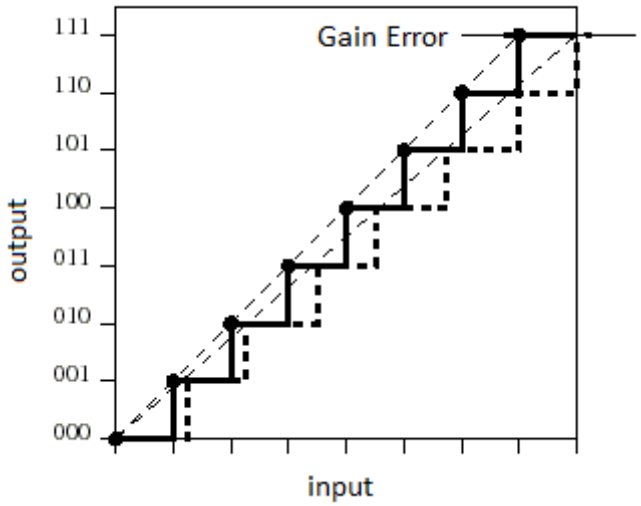


Fig. 2.5 Gain Error in a 3-bit ADC

Fig. 2.4 shown above illustrates the offset error in a 3-bit ADC. The definition of the offset error is a constant difference between the ideal output and the actual output over the whole range of the ADC. Fig. 2.5 shows the gain error in a 3-bit ADC. Gain error is defined as the difference of the slope of the ideal output and the actual output. Offset error is related to a quantization step of the ADC. Gain error is usually expressed in a percentage unit. The expressions of offset error and gain error in N-bit ADC are given below. Where $V_{ti}$ is $i^{th}$ transition voltage, respectively i = 1~$2^N$-1.

$$\text{Offset Error}_{LSB} = \frac{V_{t1,ideal} - V_{t1,actual}}{V_{LSB}} \tag{2.7}$$

$$\text{Gain Error} = \left(\frac{V_{t(2^N-1),ideal} - V_{(2^N-1),ideal}}{V_{t(2^N-1),actual} - V_{(2^N-1),actual}}\right) * 100 \tag{2.8}$$

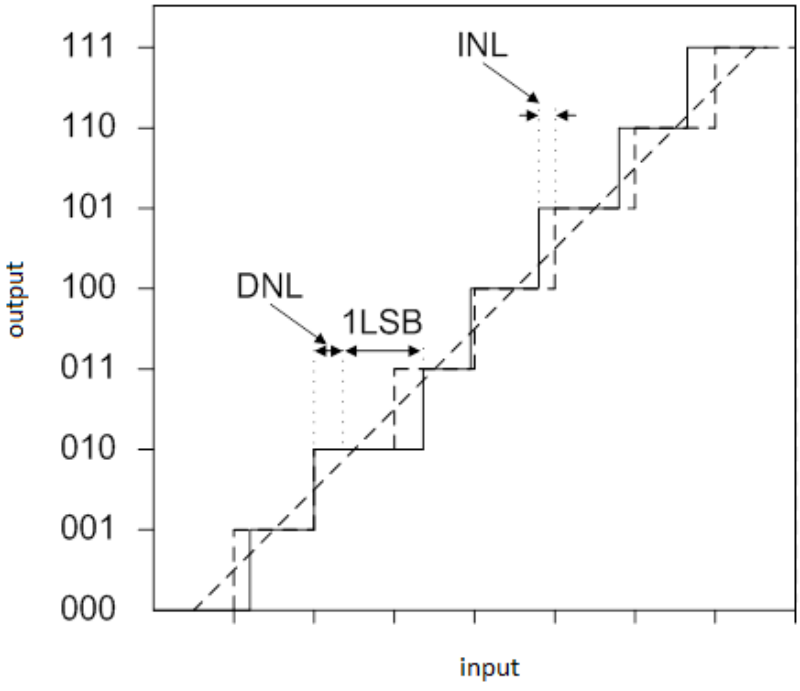


Fig. 2.6 INL and DNL in 3-bit ADC

The most important static parameters in ADCs are integral nonlinearity error (INL) and differential nonlinearity error (DNL). A plot for INL and DNL is given in Fig 2.6. These parameters represent the accuracy and performance of an ADC and contain errors of nonlinearity, quantization, offset, and noise. Differential nonlinearity error (DNL) is the difference between a digital output step size of an ADC and a step size calculated by dividing whole range of the ADC by the digital code numbers. If the maximum DNL error value is smaller than 0.5 LSB, the ADC is guaranteed that is monotonic. Monotonic means the digital output code does not collapse when increasing input signal is given. The mathematical equation of DNL is given below.

$$\mathrm{V}_{LSB} = \frac{V_{t(2^N-1)} - V_{t1}}{2^N - 1} \tag{2.9}$$

$$\mathrm{DNL}_n = \frac{V_{t(n+1)} - V_{t(n)}}{V_{LSB}} - 1 \tag{2.10}$$

$$\mathrm{INL}_n = \sum_{i=1}^{n} DNL_n \tag{2.10}$$

As shown in Eq. 2.10, INL and DNL are directly connected.

## 2.4 Kernel Estimation Method

A kernel estimation method [10], [11] is used for prediction in this research. Assume that $x_i$, $i = 1, \ldots, n$, is an independent and identically distributed random variables with an unknown density f. The basic kernel estimation is written as

$$\tilde{\mathrm{f}}(\mathrm{x}) = \frac{1}{nh}\sum_{i=1}^{n} K\left(\frac{x - x_i}{h}\right) = \frac{1}{n}\sum_{i=1}^{n} K_h(x - x_i) \tag{2.11}$$

Where $K_h(t) = K(t/h)/h$, $h>0$ is a smoothing parameter called bandwidth [12]. Kernel estimation is closely related to histograms. However, kernel estimation can be provided with better smoothness or continuity by employing a appropriate kernel. A range of kernel functions are uniform, triangular, bi-weight, tri-weight, Epanechnikov, normal, and others. Epanechnikov kernel is the most optimal in a minimum variance. The bandwidth of the kernel mentioned above is a parameter which has a strong influence to the estimated results. The most common this bandwidth parameter is termed the mean integrated squared error (MISE) is given as

$$\mathrm{MISE}(\tilde{f}) = \int E\{\tilde{f}(x) - f(x)\}^2 dx \qquad (2.12)$$

With the assumption of f(x) follows a *d*-variate normal distribution.

$$f(x) = \mathrm{PDF}(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}$$

# 3 PROPOSED METHODOLOGY

In chapter 3, the proposed method of digital calibration and prediction of effective number of bits using calibration coefficient for pipeline ADC to reduce the static specification test time will be presented. The calibration technique used in this research is introduced in Section 3.1. Then, in Section 3.2, proposed prediction technique is described.

## 3.1 The Concept of a Foreground Digital Calibration

Foreground calibration scheme is to estimate errors due to component mismatch, finite gain, offset and other non-ideal effects [13]. The foreground calibration stars with the least significant stage and recursively proceeds backwards to the most significant stage. In this research, 14bit pipeline ADC with 2 bit auxiliary is used. Therefore, the 2 bit auxiliary ADC is used to calibrate $14^{th}$ stage first, and the $14^{th}$ stage is calibrated, it joins the 2 bit auxiliary ADC to calibrate the frontend $13^{th}$ stage. This process goes on until $1^{st}$ stage is calibrated. One complete digital calibration for all stage needs to be executed at the initial startup. Fig 3.1 and Table 3.1 illustrate how one stage is calibrated to generate the related calibration coefficient. Each stage calibration needs five trip points, $V_a$, $V_b$, $V_c$, $V_d$, $V_e$, and Table 3.1 shows how the analog input Vin and D need to be set in order to calculate their values. Once these five trip points' values are acquired, we can use the equation in Table 3.2 to get the necessary calibration coefficients for each stage. In the ideal case, all the calibration coefficients $C_{1,n}$, $C_{0,n}$, $C_{-1,n}$ are zero. Where n is stage number, G is gain of each stage, ideally, G = 2.

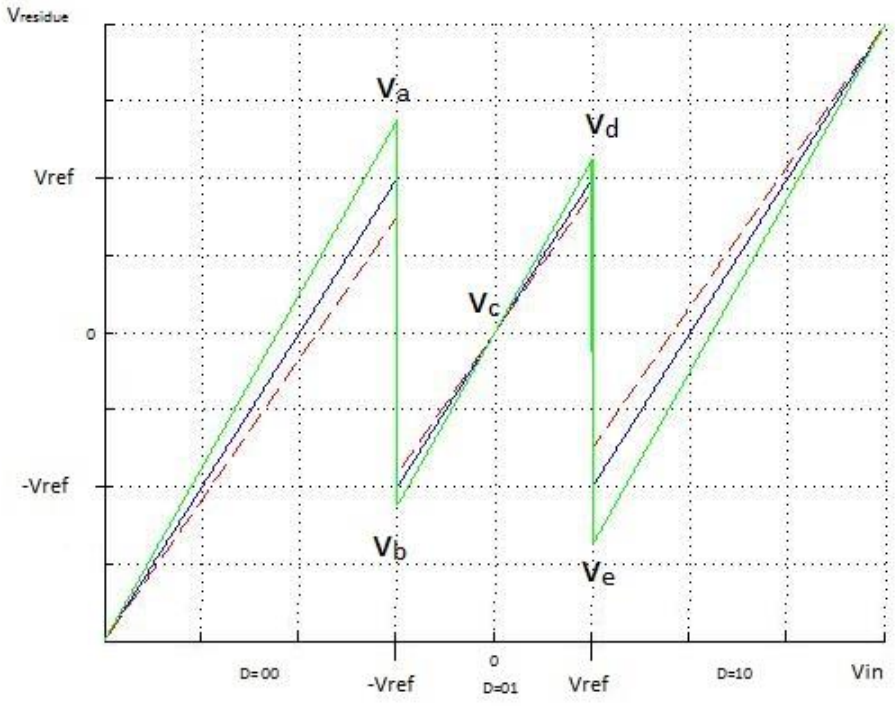


Fig 3.1 Trip points of stage calibration

Table 3.1 Stage calibration trip points setting requirements

| Trip Point | $V_{in}$ | D |
|---|---|---|
| $V_a$ | $-V_{ref}$ | -1 |
| $V_b$ | $-V_{ref}$ | 0 |
| $V_c$ | 0 | 0 |
| $V_d$ | $V_{ref}$ | 0 |
| $V_e$ | $V_{ref}$ | 1 |

Table 3.2 Stage calibration coefficients

| Calibration Coefficients | Equations | Values |
|---|---|---|
| $C_{1, n}$ | $2^{n-1}$-($V_d$ - $V_e$) + $V_c$ | $2^n$ – G * $V_{ref}$ + $V_{os}$ |
| $C_{0, n}$ | Vc | Vos |
| $C_{-1, n}$ | -$2^{n-1}$-($V_a$ – $V_b$) + $V_c$ | -$2^n$ + G * $V_{ref}$ + $V_{os}$ |

## 3.3 The Concept of Kernel Estimation Based Adaptive Prediction

In this research, we used a kernel-based estimation approach [14], [15] for our adaptive prediction technique. Kernel estimation gives us to find the correlations between the Calibration Coefficients and ENOB values and update the joint probability distribution function (JPDF) after running training set. After the training process, the created probability distribution function (PDF) provides the most possible value of the correlated parameter. The kernel function is given in (3.1). Among the number of well-known kernels, we chose the Gaussian distribution as kernel to be used. Using the Gaussian distribution kernel, equation (3.2) is the PDF estimated.

$$\int_{-\infty}^{\infty} K(x)dx = 1 \tag{3.1}$$

$$\widehat{\mathrm{PDF}}(\mathrm{s}) = \frac{1}{n\prod h_j}\sum_{i=1}^{n} w_i \prod_{j}^{M} K\left(\frac{s_j - S_{i,j}}{h_j}\right) \tag{3.2}$$

Where $h$ is the kernel width, $S_i$ is a vector containing parameters of $i^{th}$ device in the training set, $w_i$ is kernel weight, $n$ is the size of training set, and M is the number of

parameters which is number of calibration coefficients of each device. Kernel based PDF estimation basically adds kernels on each data in training set ($S_i$). The kernel width *h* is adjustable to acquire the most suitable value. Equation (3.3) is the optimized width for the Gaussian kernel to minimize MISE.

$$h_j = \left(\frac{4}{d+2}\right)^{\frac{1}{d+4}} \sigma_j n^{-\frac{1}{d+4}} \tag{3.3}$$

Where *d* is number of dimensions and $\sigma_j$ is standard deviation of the estimated parameters of $j^{th}$ specification in this paper the specification is the calibration coefficient.

# 4 RESULTS

We have modeled a pipeline ADC in MATLAB and performed statistical simulations to verify our calibration and prediction methodology and mathematical equations we proposed. The model is considered that has offset error, capacitor mismatch. It is assumed that this pipeline ADC has less than ±30% capacitor mismatches. With the assumption, the variables have random values with normal distributions. A 14-stage, 1.5 bit per stage, 1Mega Sample per second pipeline ADC with 2-bit auxiliary ADC is modeled ADC. Table 4.1 to 4.3 shown below are capacitor mismatch ratios for each running and Fig. 4.1 to 4.3 are output plot of each running comparing actual, calibrated, and ideal output.

Table 4.1 Capacitor mismatch ratio for 1st running

| Stage Number | Stage 1 | Stage 2 | Stage 3 | Stage 4 | Stage 5 | Stage 6 | Stage 7 |
|---|---|---|---|---|---|---|---|
| Mismatch Ratio | 1.180 | 0.785 | 0.953 | 1.249 | 1.175 | 1.276 | 1.093 |
| Stage Number | Stage 8 | Stage 9 | Stage 10 | Stage 11 | Stage 12 | Stage 13 | Stage 14 |
| Mismatch Ratio | 0.721 | 1.209 | 1.260 | 1.107 | 1.155 | 1.146 | 0.935 |

Table 4.2 Capacitor mismatch ratio for 2nd running

| Stage Number | Stage 1 | Stage 2 | Stage 3 | Stage 4 | Stage 5 | Stage 6 | Stage 7 |
|---|---|---|---|---|---|---|---|
| Mismatch Ratio | 0.837 | 1.248 | 0.791 | 1.196 | 1.023 | 1.298 | 0.747 |
| Stage Number | Stage 8 | Stage 9 | Stage 10 | Stage 11 | Stage 12 | Stage 13 | Stage 14 |
| Mismatch Ratio | 0.966 | 0.764 | 1.277 | 0.703 | 1.165 | 1.190 | 1.221 |

Table 4.3 Capacitor mismatch ratio for 3rd running

| Stage Number | Stage 1 | Stage 2 | Stage 3 | Stage 4 | Stage 5 | Stage 6 | Stage 7 |
|---|---|---|---|---|---|---|---|
| Mismatch Ratio | 1.212 | 1.073 | 0.911 | 1.008 | 0.941 | 0.746 | 0.844 |
| Stage Number | Stage 8 | Stage 9 | Stage 10 | Stage 11 | Stage 12 | Stage 13 | Stage 14 |
| Mismatch Ratio | 0.774 | 0.810 | 0.844 | 0.950 | 0.731 | 1.242 | 1.267 |

Table 4.4 shows the SINAD and ENOB results comparing before and after calibration.

This calibration provides approximately 60% to 83% improvements in ENOB.

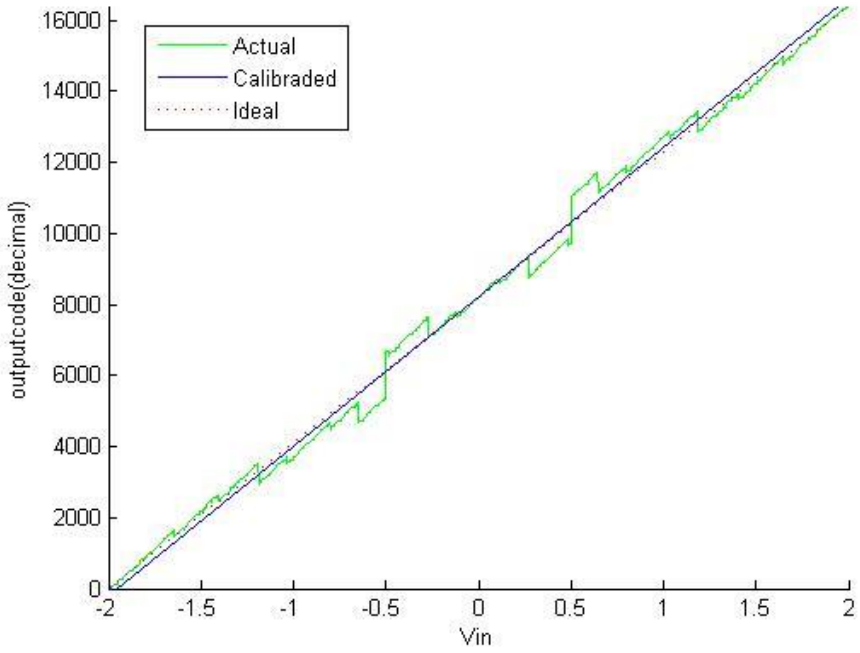


Fig. 4.1 Output of 1st running

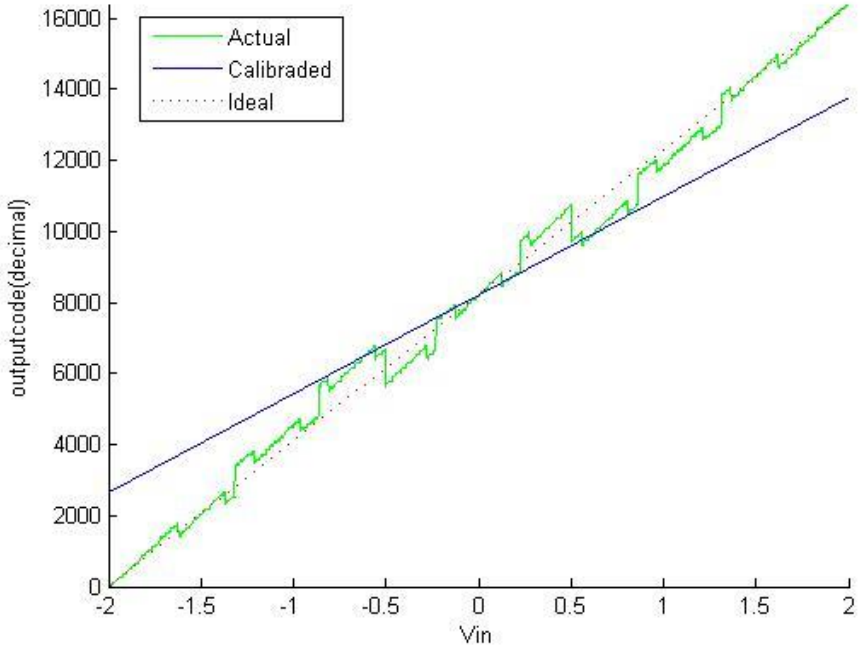


Fig. 4.2 Output of 2nd running

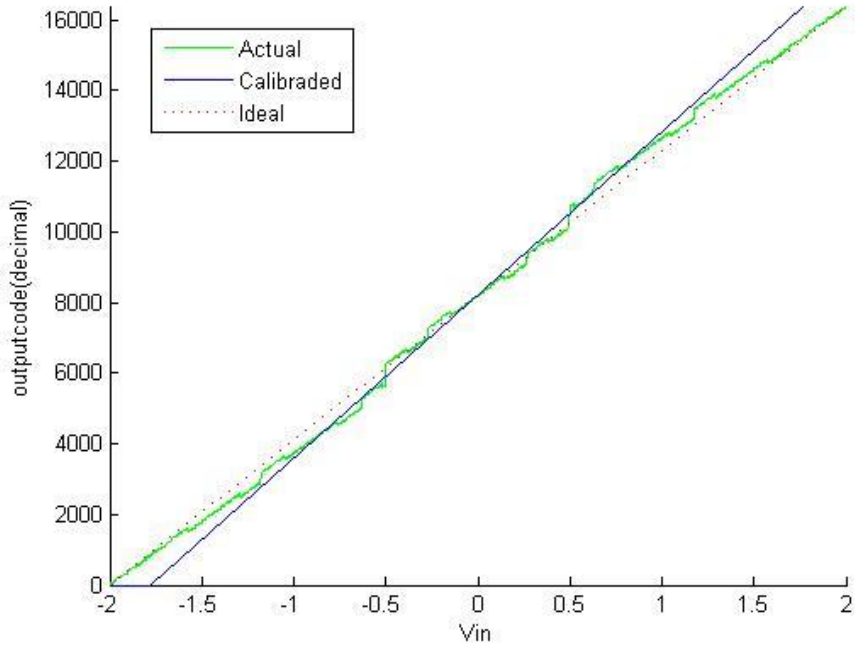


Fig. 4.3 Output of 3rd running

Table 4.4 Actual vs. Calibrated SINAD and ENOB of 14-bit pipeline ADC

| | Actual | | Calibrated | | Improvement (%) |
|---|---|---|---|---|---|
| | SINAD(dB) | ENOB(bits) | SINAD(dB) | ENOB(bits) | |
| 1st | | | | | |
| 2nd | | | | | |
| 3rd | | | | | |

We made 1400 cases of gradually increasing capacitor mismatch training set for the prediction and ran 1000 randomly generated capacitor mismatch cases for comparing actual and predicted ENOB values. Fig 4.4 shows actual (red) and predicted (blue) ENOB values.

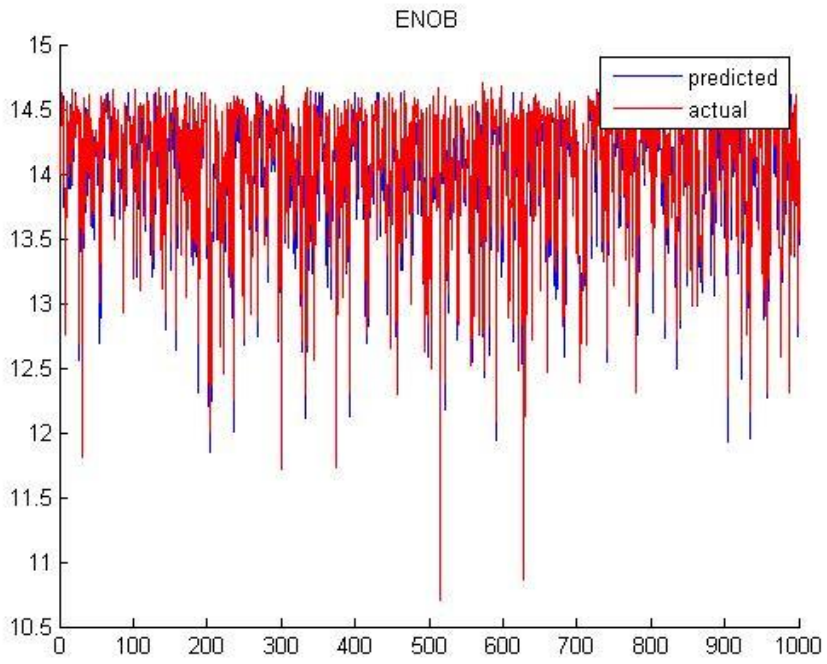


Fig 4.4 Actual and predicted ENOB

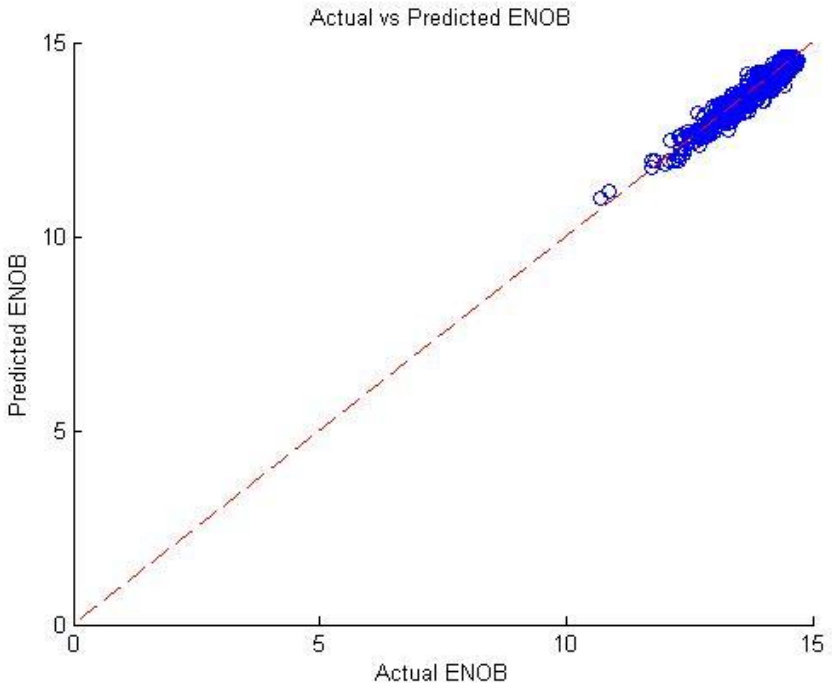


Fig 4.5 Actual vs predicted ENOB

Fig 4.5 illustrates actual (x-axis) versus predicted (y-aixs) ENOB values and Table 4.5 is brief comparison between actual and predicted ENOB values. It has maximum of 4.1156% difference in whole 1000 cases and average difference is less than 0.5%.

Table 4.5 Average and Maximum difference of actual and predicted ENOB values

| | Difference (%) |
|---|---|
| Average | -0.4758 |
| Maximum | 4.1156 |

# 5 CONCLUSION

## 5.1 Summary

In this thesis, a novel methodology for digital calibration and ENOB prediction of pipeline ADC is presented. For the verification of the proposed method, mathematical model of the ADC and equations for kernel based estimation are derived. In the mathematical model, non-ideal parameters such as non-ideal operational amplifier, capacitor mismatch, comparator offset, and random noise are considered. The proposed calibration method is based on foreground digital calibration technique. The calibration method proposed in this thesis significantly reduces initial calibration process time and provides reliable result compare to conventional method. In addition, the kernel based estimation prediction method we proposed also reduces remarkably for post calibration testing time with highly accurate result.

## 5.2 Future work

Most of modern devices are made in mass production and especially ADCs with high speed sampling frequency and high resolution requires huge amount of time for testing. Therefore, the proposed prediction method can be extended to other parameters.

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