

Design of a Twelve Bit, Four Hundred Mega-Samples-per-Second, Interpolating Dual  
Channel Digital to Analog Converter Featuring Digital Modulation

by

Cliff Nixon

A Thesis Presented in Partial Fulfillment  
of the Requirements for the Degree  
Master of Science

Approved November 2013 by the  
Graduate Supervisory Committee:

Bertan Bakkaloglu, Chair  
Bert Vermeire  
Jennifer Kitchen

ARIZONA STATE UNIVERSITY

December 2013

## ABSTRACT

Digital to analog converters (DACs) find widespread use in communications equipment. Most commercially available DAC's which are intended to be used in transmitter applications come in a dual configuration for carrying the in phase (I) and quadrature (Q) data and feature on chip digital mixing. Digital mixing offers many benefits concerning I and Q matching but has one major drawback; the update rate of the DAC must be higher than the intermediate frequency (IF) which is most commonly a factor of 4. This drawback motivates the need for interpolation so that a low update rate can be used for components preceding the DACs.

In this thesis the design of an interpolating DAC integrated circuit (IC) to be used in a transmitter application for generating a 100MHz IF is presented. Many of the transistor level implementations are provided. The tradeoffs in the design are analyzed and various options are discussed. This thesis provides a basic foundation for designing an IC of this nature and will give the reader insight into potential areas of further research.

At the time of this writing the chip is in fabrication therefore this document does not contain test results.

## ACKNOWLEDGEMENTS

I would like to take this opportunity to thank my committee members for their support during this project. Dr. Bertan Bakkaloglu, my thesis advisor, guided me along the way and was always there to help and provide encouragement. Dr. Bert Vermeire provided funding for the project from the private sector and aided with numerous system level details to ensure the products success. Dr. Jennifer Kitchen endured many RFIC questions and was always very helpful.

I would also like to thank my family for putting up with my conquest of becoming a professional student.

## TABLE OF CONTENTS

	Page
LIST OF TABLES .....	v
LIST OF FIGURES .....	vi
LIST OF ABBREVIATIONS.....	viii
INTRODUCTION .....	1
Design Goals.....	1
Thesis Structure .....	2
LVDS .....	3
LVDS Specification.....	3
LVDS Driver .....	4
LVDS Receiver.....	8
INTERPOLATION.....	9
Interpolation Filter Basics.....	9
Half-band Filters .....	10
Half-band Filter Implementation .....	12
DIGITAL MIXING .....	16
Complex Mixing.....	16
Modulator Architectures .....	18
Digital Quadrature Modulation.....	20
IQ Mismatch Considerations .....	21
Double Quadrature Modulation Implementation.....	23
CURRENT STEERING DAC .....	24

	Page
Current Steering DAC Concepts .....	24
DAC Architecture .....	25
Gate Drive Design .....	28
Differential Switch Considerations.....	30
Sizing for Mismatch and Noise .....	31
DAC Performance .....	33
DAC Layout.....	34
FINAL DESIGN .....	36
Top Level.....	36
Pin Configuration and Description .....	37
Floorplan.....	38
Layout .....	39
Conclusion and Future Work.....	41
REFERENCES .....	42

## LIST OF TABLES

Table	Page
2-1 LVDS Specification.....	3
3-1 Filter Properties .....	14
3-2 Filter Multiplier Coefficients.....	15
4-1 Bit Selection Modulation.....	23
6-1 Pin Function Descriptions .....	38

## LIST OF FIGURES

Figure	Page
1-1 Functional Block Diagram.....	1
2-1 Ideal LVDS Driver and Receiver .....	4
2-2 Digital LVDS Driver .....	5
2-3 Analog LVDS Driver.....	6
2-4 LVDS Driver Schematic.....	7
2-5 CMFB Gain and Phase .....	7
3-1 Interpolation Example .....	9
3-2 Return to Zero.....	10
3-3 Sinc Function .....	11
3-4 Non-Symmetrical FIR .....	12
3-5 Symmetrical FIR.....	12
3-6 3rd Interpolation Filter.....	13
3-7 Cascaded Half-band Filters .....	14
3-8 Filter 1 Magnitude Response.....	15
3-9 Filter 2 Magnitude Response.....	16
3-10 Filter 3 Magnitude Response.....	16
4-1 Upconversion.....	17
4-2 Complex Mixing.....	17
4-3 Double Sideband Modulator.....	18
4-4 Quadrature Modulator (SSB).....	19
4-5 Double Quadrature Modulator (Complex) .....	20

Figure	Page
4-6 90°Samples .....	21
4-7 Image Rejection vs. Amplitude Mismatch .....	22
4-8 Image Rejection vs. Phase Mismatch .....	22
4-9 One Bit Mixer .....	23
5-1 Three Bit Current Steering DAC .....	25
5-2 Current Steering DAC Block Diagram.....	27
5-3 Current Array Structure .....	28
5-4 Gate Drive.....	30
5-5 DAC FFT .....	33
5-6 MSB Array .....	35
5-7 ULSB Array.....	35
6-1 Pin Configuration .....	37
6-2 Floorplan.....	39
6-3 Layout.....	40

## LIST OF ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
MSPS	Mega Samples Per Second
RF	Radio Frequency
SNR	Signal to Noise Ratio
SOI	Silicon On Insulator
ULSB	Upper Least Significant Bit

# 1 INTRODUCTION

## 1.1 Design Goals

The goal of this project was to design a 12 bit, 400 MSPS dual channel interpolating digital to analog converter with on chip digital mixing to be used in a transmitter application for the purpose of satellite communications. One of the primary design objectives was to obtain a low static and dynamic mismatch between I and Q channels. Minimum risk design methods were prioritized in order to achieve first pass success. The chip was designed in a  $0.18\mu\text{m}$  SOI CMOS process.

The functional block diagram of the design is shown in Figure 1-1. LVDS is used for the data interface. Cascaded half-band filters provide an interpolation factor of eight. A double quadrature modulator is implemented in digital as  $F_s/4$ . Current steering DACs output the modulated I and Q signals.

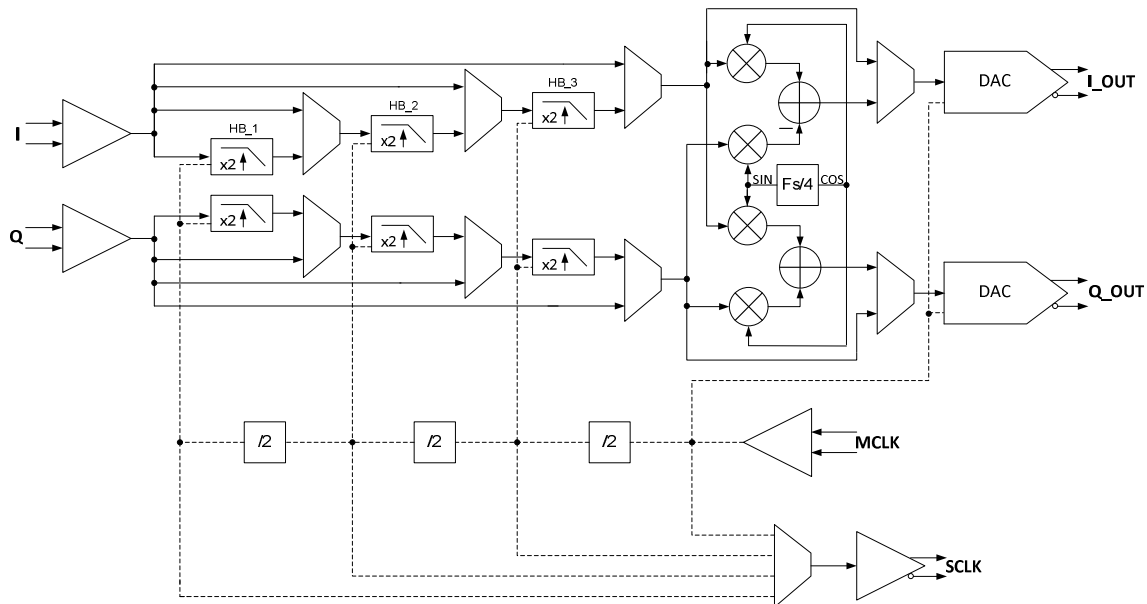


Figure 1-1 Functional Block Diagram

## 1.2 Thesis Structure

This thesis is divided into chapters which correspond to the cells within the functional block diagram of Figure 1-1. The cells which were implemented in the chip are described in each corresponding chapter. Concepts are developed from the ground up and the intention is to provide the reader with the necessary tools to analyze and design a similar cell.

Chapter 2 provides an overview of LVDS communications. The standards and benefits of LVDS are presented. The LVDS output driver cell which was created is described in detail.

Chapter 3 develops the concept of interpolation. The primary system level structure of a half-band filter is provided and its operation is described.

Chapter 4 presents an overview of digital mixing. The concepts of digital mixing are discussed in both the frequency and time domain in an attempt to clarify the material. The design of an  $F_s/4$  bit mixer is provided.

Chapter 5 gives a detailed account of the design of a current steering DAC. The major components and several of the tradeoffs which need to be considered are discussed. DAC layout methodologies are presented along with various common centroid topologies for current arrays.

Chapter 6 concludes with the final design of the chip at the top level. The completed layout of the IC is presented.

## 2 LVDS

### 2.1 LVDS Specification

LVDS is an acronym for low voltage differential signaling and is a popular method for high speed digital communications between chips up to about 3GHz. IEEE Standard 1596.3, developed in 1996, provides a basis for implementing LVDS circuits. Table 2-1 shows the main DC specifications derived from the standard for the driver and receiver cells. Another standard for LVDS, ANSI/TIA/EIA-644, was developed by the Telecommunications Industry Association.

Table 2-1 LVDS Specification

LVDS DC Driver Specifications				
Symbol	Parameter	Min	Max	Units
Vod	Output Voltage Differential	250	400	mV
Voh	Output Voltage High	-	1475	mV
Vol	Output Voltage Low	925	-	mV
LVDS DC Receiver Specifications				
Symbol	Parameter	Min	Max	Units
Vidth	Input Differential Threshold	-100	+100	mV
Rin	Input impedance	90	110	$\Omega$
Vin	Input Voltage Range	0	2400	mV
Vhyst	Input Differential Hysteresis	25	-	mV

LVDS drivers are typically designed to deliver a current of 3.5mA to a 100 ohm load which will generate 350mV. The receiver detects this voltage to determine if the signal is positive or negative depending upon the direction of the current through the resistor. As shown from the table, LVDS was developed when 2.5V was a popular supply voltage which accounts for the high common mode levels of the driver and the wide common mode range of the receiver.

LVDS offers many benefits for chip to chip digital communication. Differential signals provide common mode rejection and help to reduce EMI (electromagnetic interference) providing a robust method of transferring data. With a properly designed driver switching noise will be minimized and EMI will be further reduced, similar to the benefits seen in CML and ECL logic. A low signal level offers the potential for higher speed by reducing the time for charging and discharging large on chip input capacitances which also helps to further reduce noise.

## 2.2 LVDS Driver

An ideal LVDS driver and receiver are shown in Figure 2-1. The switches control the direction of current through the 100 ohm resistor of the receiver making the output signal positive or negative. This circuit would be considered an analog solution because it requires a common mode feedback circuit (not shown) to set the voltage level of the output. The circuit will have low EMI because the current sources are never turned off so no switching transients occur.

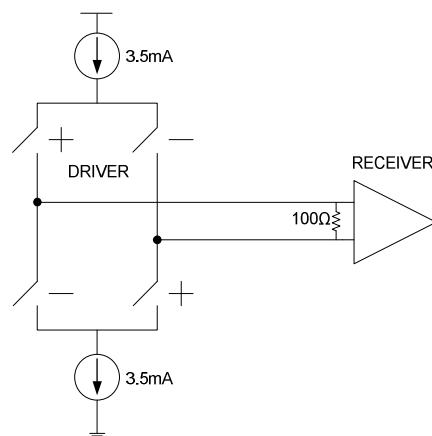


Figure 2-1 Ideal LVDS Driver and Receiver

An alternative implementation which is often seen in FPGA's is shown in Figure 2-2. This is a digital solution which uses external resistors to set the common mode and current levels. The digital implementation is a simple approach that is guaranteed to be stable but has the potential to produce rail to rail transients if output transition times are not matched which will increase noise and degrade EMI performance.

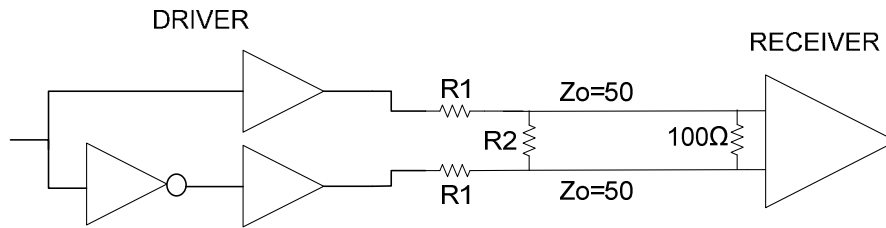


Figure 2-2 Digital LVDS Driver

In the literature [Chen] and [Tajalli], the LVDS drivers presented both operate with a 1.8V supply and resemble the analog implementation of Figure 2-1. Both of the designs utilize voltage CMFB which requires compensation capacitance to prevent instability. The large switching transients required of the driver circuit makes an analog implementation difficult to stabilize with voltage CMFB as mentioned in [Tajalli].

Consider the circuit shown in Figure 2-3. This is an analog LVDS driver implementation which utilizes current common mode feedback. ISOURCE is designed to be slightly larger than ISINK. The common mode feedback circuit sinks ( $I_{SOURCE} - I_{SINK}$ ) to set the common mode to  $V_{CM}$ .

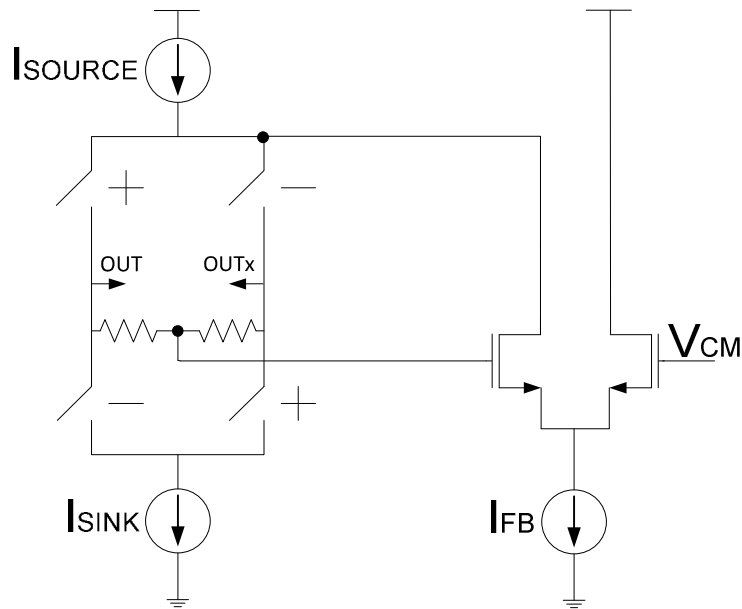


Figure 2-3 Analog LVDS Driver

An original approach to an LVDS driver based on the simplified circuit in Figure 2-3 is shown in Figure 2-4. This circuit is based on a rail to rail input folded cascode and is designed to operate with a 1.8V supply. Standard differential CMOS switching levels are used as an input. Current common mode feedback is used to set the common mode level to  $V_{CM}$  and requires no compensation. A thorough sensitivity analysis was performed on the circuit and it was determined to be very robust. The gain and phase of the common mode feedback circuit for the LVDS driver is shown in Figure 2-5. From the plots it can be seen that there are 3 poles and one left half plane zero in the CMFB loop. With careful sizing the loop can be made stable without adding any additional capacitors. From a half circuit perspective, M10 and M12 are sized with minimum channel lengths but are still fairly large devices due to the high current requirement of 3.5mA. The parasitic capacitances of these devices establish the dominant pole of the loop. The series combination of M12 CSD and the measuring resistor accounts for the

zero. M17 and M18 are responsible for the remaining 2 poles. As long as M17 and M18 are made relatively small with respect to M10 and M12 the remaining poles will be pushed out far enough to keep the circuit stable under all conditions.

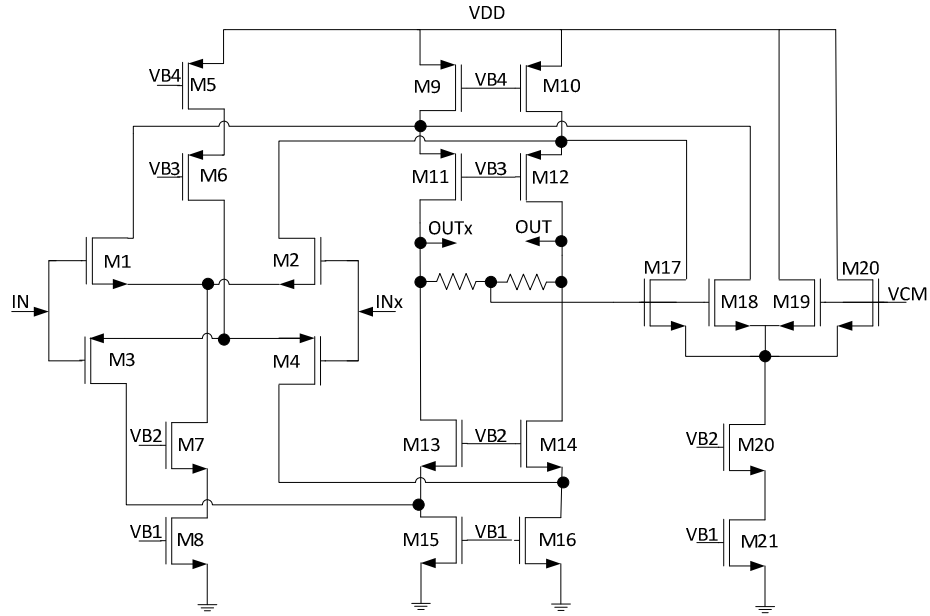


Figure 2-4 LVDS Driver Schematic

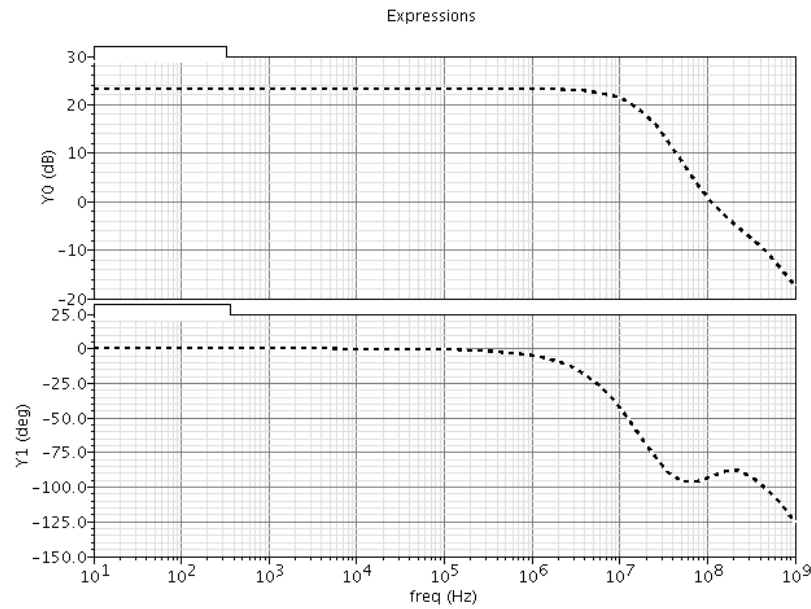


Figure 2-5 CMFB Gain and Phase

For this chip, the LVDS driver circuit will provide the output synchronizing clock for an FPGA which will typically run at 50MHz and will be on the same circuit board. With bypass modes enabled the maximum frequency it will see is 400MHz.

### 2.3 LVDS Receiver

A receiver based on a 1.8V supply is unable to meet the common mode range specification of 0 to 2.4V but does not need to since this will only provide protection against high common mode noise and will not affect normal functionality. Notice that the output driver common mode range specification is from 975mV to 1475mV which will work well with an n-channel comparator used for a receiver. Rail to rail inputs could be used if a wider common mode range was desired. A standard n-channel comparator was used as the receiver cell. The input devices were chosen to have a thicker gate oxide in order to withstand transients up to 3.3V in case an interface circuit is used with a supply voltage higher than 1.8V.

The specification states that the receiver cell should have a minimum hysteresis of 25mV. Hysteresis sets a different threshold for an increasing and decreasing transition which provides a voltage “guard band” and protects against noise in a system. Hysteresis was first proposed by Otto Schmitt, who is responsible for the design of the Schmitt trigger. Some literature states that hysteresis will increase jitter but I have never found anything substantial to back up that statement. Obviously hysteresis will result in an asymmetrical waveform if it is used in a clock circuit, but as long as there is only a small amount; the asymmetry should not pose an issue. Hysteresis should only result in increased jitter if the noise is higher at the transitions than at the zero cross.

### 3 INTERPOLATION

#### 3.1 Interpolation Filter Basics

Digital filters mimic analog filters by convolving an input digital signal with a digital representation of an analog filter. There are two basic types of digital filters, FIR (Finite Impulse Response) and IIR (Infinite Impulse Response). An FIR filter does not have feedback and will settle in a “finite” time. An IIR filter has feedback and will never settle so its settling time is “infinite”. An FIR will require more computations for the same response but will always be stable due to not having feedback and linear phase can easily be achieved.

An interpolation filter is a special application of digital filters which calculates the intermediate value between two consecutive values of a sampled signal. From a black box perspective the output of an interpolation filter should look like the input signal was sampled at a higher rate as shown in Figure 3-1.

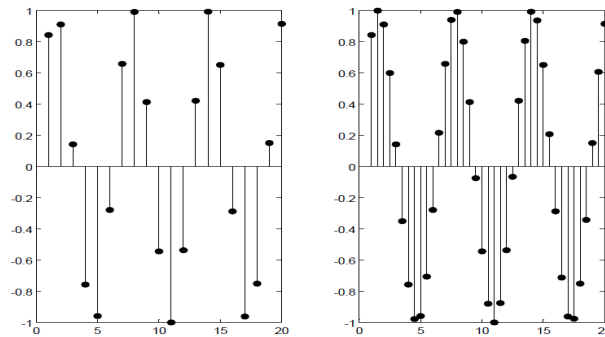


Figure 3-1 Interpolation Example

There are several different types of interpolation methods which produce varying results. Linear interpolation is perhaps the easiest to understand; the midpoint value is just the average of two consecutive values. Curve fitting methods based on polynomials

are also used. The most popular methods involve using FIR filters to obtain the desired result. One way to accomplish this is to “zero stuff” the input and convolve the new signal with a low pass filter. So in order to interpolate by  $2x$ , a zero data word should be placed after every input data word which can then be low pass filtered to produce an interpolated signal. The output amplitude will be one half the value of the original due to the zeros. The “zero stuffing” method is similar to the output of a return to zero DAC as shown in Figure 3-2. Additional zeros can be added to increase the interpolation factor, resulting in further reduction of the output amplitude.

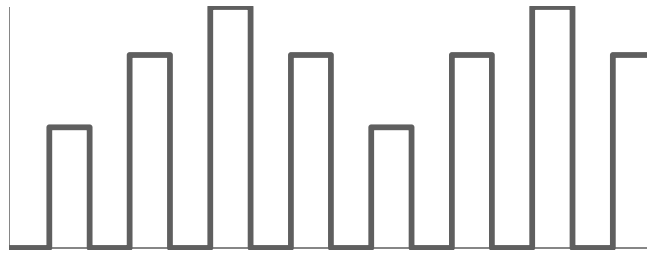


Figure 3-2 Return to Zero

Another method which can be used to interpolate a signal is to low pass filter the input with a special type of FIR filter called a half-band. The output of a half-band filter is alternated with the original signal to produce an interpolated output. This is a popular method of interpolation which has many benefits when compared to the “zero stuffing” method but can only be used for a factor of two.

### 3.2 Half-band Filters

The sinc function shown in Figure 3-3 is a perfect “brick wall” low pass filter if carried out to infinity. If an input signal is convolved with this filter at  $\frac{1}{4}$  intervals of a period, zero amplitude will be applied at every other term except for the origin which will

be 1. A half-band filter performs this function, taking advantage of the zeros by convolving an input signal with a sinc at  $(n\pi)/2$  intervals which is similar to the concept used in  $F_s/4$  digital mixing. This gives a savings of  $1/2$  of the multipliers and is the reason why half band filters are popular. If a filter is made symmetric the multipliers can be used twice to convolve a signal resulting in saving an additional  $1/2$  of the multipliers. Utilizing these two methods provides a significant savings in both power and area reducing the number of multipliers to  $1/4$  of the original value.

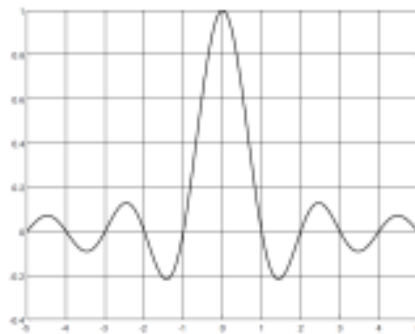


Figure 3-3 Sinc Function

Half-band filters are a subset of Nyquist filters and are characterized by having a cutoff frequency of  $0.5\pi$ . When a sinc is truncated with an appropriate windowing function to make the filter finite, ripples are created in the passband and stopband. In half-band filters the ripples are identical in both bands.

The two filter structures shown below take advantage of the zeros in the sinc function. The longer filter does not take advantage of symmetry, requiring twice as many multipliers as the shorter filter. Notice that the shorter filter requires additional adders for implementation. The additional adders are a small price to pay for the reduction in multipliers.

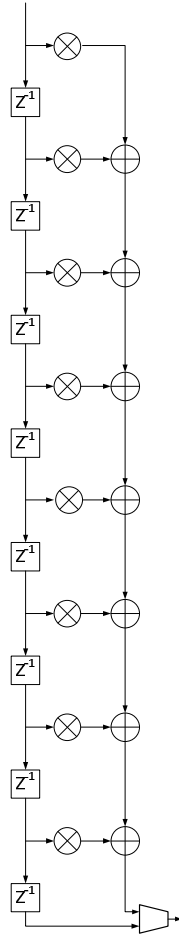


Figure 3-4 Non-Symmetrical FIR

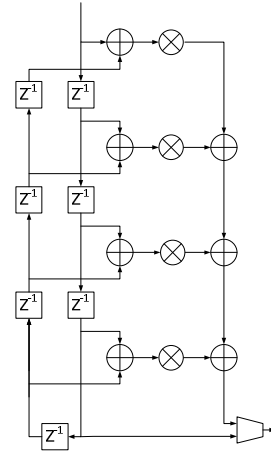


Figure 3-5 Symmetrical FIR

### 3.3 Half-band Filter Implementation

The interpolation filter in this chip is based on 3 cascaded half-band filters which brings the interpolation factor to 8 as shown in Figure 3-7. The 3rd interpolation filter is shown in Figure 3-6. The data coming in is 12 bits. The first adders in the chain are 13 bits, so that no overflow occurs. The multipliers have a 13 bit data input and a 17 bit coefficient with an output of 19 bits. The final adders are 20 bits, so that no overflow occurs. At the input to the clamp the data stream is shifted to the left by 2 (multiplied by 4) to account for the increase in adder bits and truncated to 12 bits.

A digital filter closely resembles its analog counterpart therefore overshoot will occur with large inputs. The filter must recognize these occurrences and clamp the signal to the appropriate rail, which is the purpose of the clamp circuit. The MSB of the last multiplier is compared with the (MSB – 2) bit, which is now the new MSB of the filtered data stream, to see if they are the same. If they are not, the output is clamped to the appropriate rail.

This particular circuit will run at a minimum of 200MHz, and will produce a 400MHz interpolated signal by outputting the delayed signal when the clock is high and the filtered signal when the clock is low.

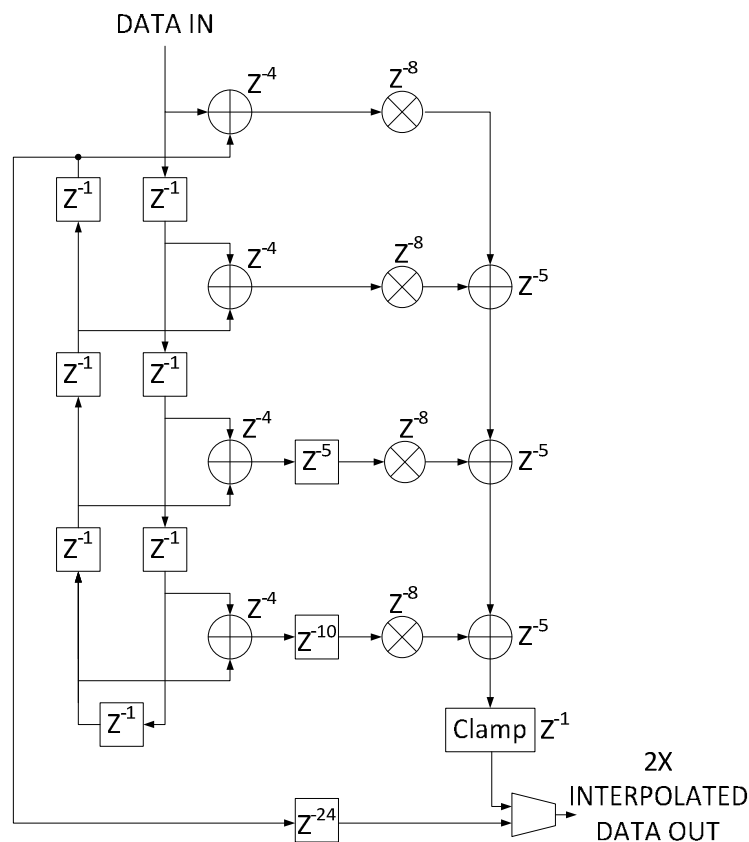


Figure 3-6 3rd Interpolation Filter

Major reductions in computation can be made to the design of a filter by increasing the number of individual cells as opposed to keeping the design modular. For instance, each addition in a multiplier can be analyzed to determine if a carry is possible, if not the logic can be simplified. Since cascaded half-band filters run at different speeds the modularity must be reduced to a certain degree to take full advantage of the power savings. For example, the preceding filter runs at half the speed so it would only require half the pipelining. The primary cost of implementation is additional design time.

The coefficients for the multipliers were determined using MATLAB Filter Builder. 17 bit coefficients were required to meet the minimum SNR of 74dB. The filter properties and multiplier coefficients are shown in Table 3-1 and Table 3-2 respectively. Each subsequent filter runs at twice the rate as the previous one. The transition width can be relaxed and the poles can be decreased in each subsequent filter while maintaining the same SNR target as shown in Table 3-1.

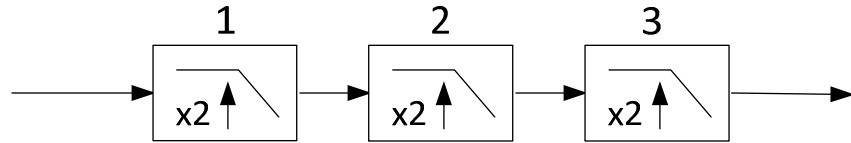


Figure 3-7 Cascaded Half-band Filters

Table 3-1 Filter Properties

	Filter 1	Filter 2	Filter 3
Order	47	23	15
Transition Width	0.2	0.4	0.6
Clock Frequency	MCLK / 8	MCLK / 4	MCLK / 2

Table 3-2 Filter Multiplier Coefficients

Filter 1	Filter 2	Filter 3
-0.000396728515625	-0.001556396484375	-0.00494384765625
0.00115966796875	0.00823974609375	0.033935546875
-0.0027008056640625	-0.026947021484375	-0.1353607177734375
0.005462646484375	0.070220947265625	0.6063385009765625
-0.009979248046875	-0.1721954345703125	
0.016998291015625	0.6221771240234375	
-0.0275726318359375		
0.043426513671875		
-0.067962646484375		
0.1098785400390625		
-0.2013092041015625		
0.6329193115234375		

MATLAB has an HDL Coder program which synthesizes filters with verilog but pipelining within the multiplier and accumulator cells is not an option. Verilog could have been used to synthesize the cells but it was considered to be too much of a risk when they were initially designed. It would be a great exercise to design them with verilog now that they are completed and compare the results. The layout was completed using Cadence Encounter.

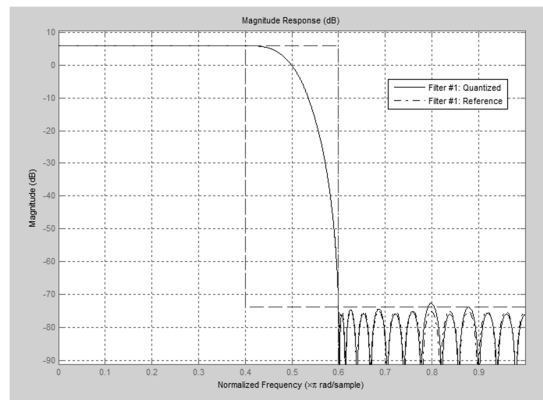


Figure 3-8 Filter 1 Magnitude Response

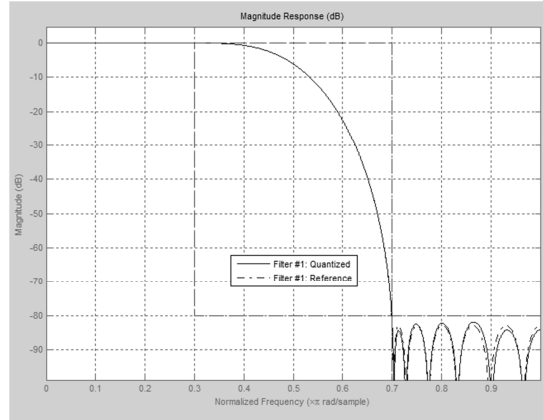


Figure 3-9 Filter 2 Magnitude Response

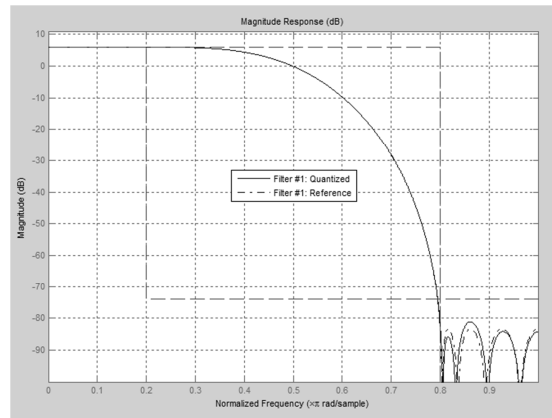


Figure 3-10 Filter 3 Magnitude Response

## 4 DIGITAL MIXING

### 4.1 Complex Mixing

When a baseband signal is upconverted, mixed with a higher frequency carrier, two images are produced with respect to the carrier. In a transmitter the higher frequency image is desired and the lower frequency image is an undesired byproduct which must be filtered out. For the following diagram,  $F_B$  = Baseband Frequency and  $F_C$  = Carrier Frequency.

$$A \cos(2\pi F_B) * B \cos(2\pi F_C) = \frac{AB}{2} \cos(2\pi(F_C - F_B)) + \frac{AB}{2} \cos(2\pi(F_C + F_B))$$

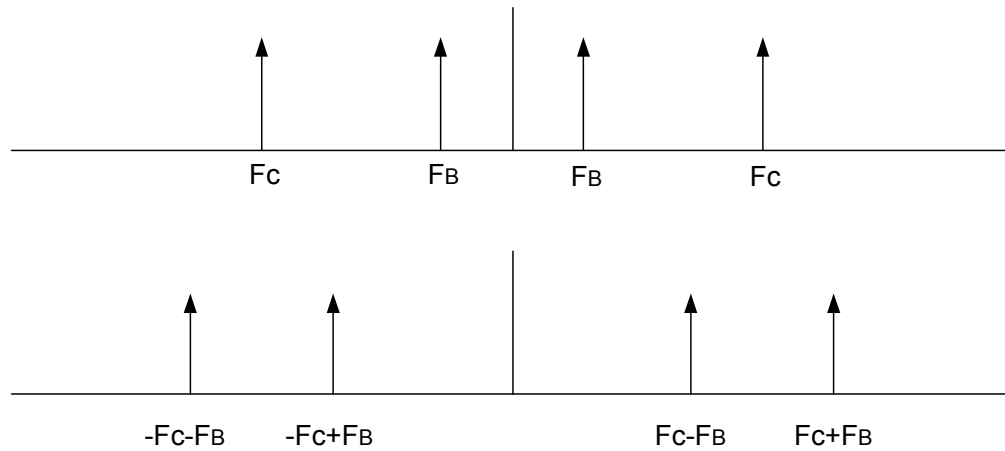


Figure 4-1 Upconversion

The entire premise behind complex mixing comes from combining an in phase signal (I) with its quadrature component (Q), a signal which is delayed by 90 degrees. The signals are combined after upconversion so that the unwanted image is removed as shown below.

$$\cos = \frac{e^{j2\pi ft} + e^{-j2\pi ft}}{2} \quad \sin = \frac{e^{j2\pi ft} - e^{-j2\pi ft}}{2j}$$

$$e^{j2\pi ft} = \cos(2\pi ft) + j\sin(2\pi ft)$$

$$e^{-j2\pi ft} = \cos(2\pi ft) - j\sin(2\pi ft)$$

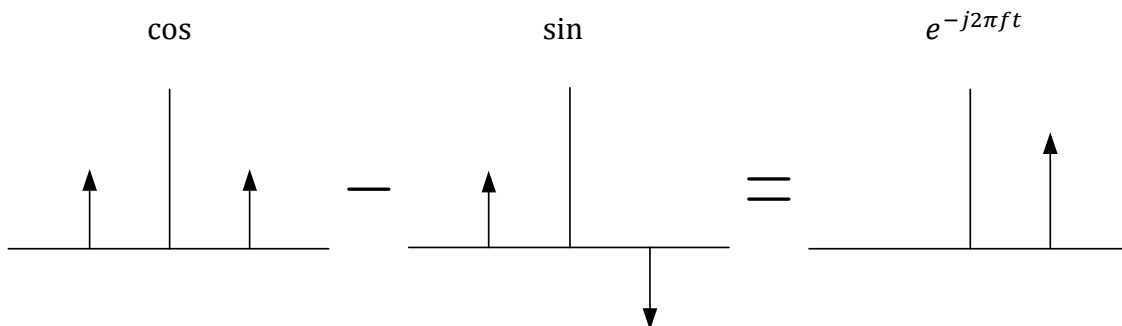


Figure 4-2 Complex Mixing

The time domain equation for adding a sine and cosine of the same frequency is as follows.

$$A\cos(2\pi f) + B\sin(2\pi f) = \sqrt{A^2 + B^2} \cos\left(2\pi f \tan^{-1} \frac{B}{A}\right)$$

If  $A=B=1$ , then this equation reduces to

$$\sqrt{2}\cos\left(2\pi f - \frac{\pi}{4}\right)$$

#### 4.2 Modulator Architectures

Three types of mixers are shown below. The first mixer is a double sideband modulator which means that it produces both images. The second mixer is a quadrature modulator, which is a single sideband mixer that cancels the image by combining the in-phase signal with its quadrature. The third mixer is a double quadrature modulator and is intended to be used in a two stage transmitter (Super Heterodyne) where the first upconversion is to the IF (Intermediate Frequency). Its purpose is to provide a complex output so that the image can be cancelled in the final upconversion to RF.

The following equations describe double sideband modulation which refers to Figure 4-3. (LO stands for Local Oscillator)

$$\cos(2\pi F_B) * \cos(2\pi F_{LO}) = \frac{1}{2}\cos(2\pi(F_{LO} - F_B)) + \frac{1}{2}\cos(2\pi(F_{LO} + F_B))$$



Figure 4-3 Double Sideband Modulator

The following equations describe quadrature modulation which refers to Figure 4-

4.

$$\begin{aligned}
 [\cos(2\pi F_B) * \cos(2\pi F_{LO})] + [\sin(2\pi F_B) * \sin(2\pi F_{LO})] &= \left[ \frac{1}{2} \cos(2\pi(F_{LO} - F_B)) + \right. \\
 &\quad \left. \frac{1}{2} \cos(2\pi(F_{LO} + F_B)) \right] - \left[ \frac{1}{2} \cos(2\pi(F_{LO} - F_B)) - \frac{1}{2} \cos(2\pi(F_{LO} + F_B)) \right] \\
 &= \cos(2\pi(F_{LO} + F_B))
 \end{aligned}$$

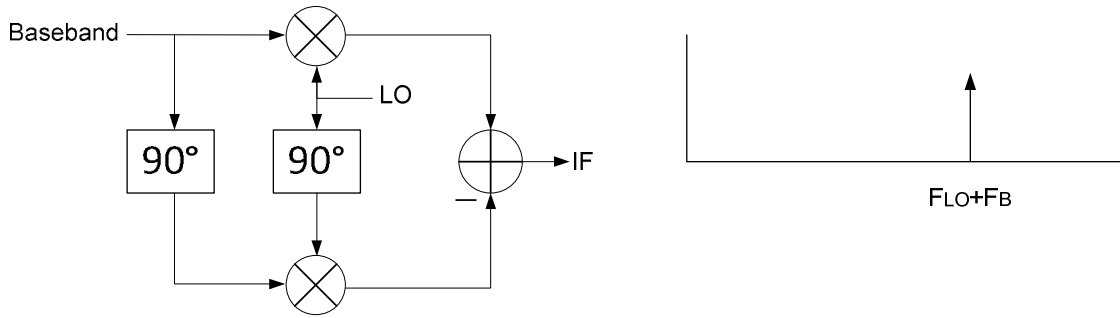


Figure 4-4 Quadrature Modulator (SSB)

The following equations describe double quadrature modulation which refers to Figure 4-5. The Real IF output is the same as the quadrature modulator.

$$\text{Real IF} = \cos(2\pi(F_{LO} + F_B))$$

The Imaginary IF is as follows:

$$\begin{aligned}
 [\cos(2\pi F_B) * \sin(2\pi F_{LO})] + [\sin(2\pi F_B) * \cos(2\pi F_{LO})] &= \left[ \frac{1}{2} \sin(2\pi(F_{LO} + F_B)) + \right. \\
 &\quad \left. \frac{1}{2} \sin(2\pi(F_{LO} - F_B)) \right] + \left[ \frac{1}{2} \sin(2\pi(F_{LO} + F_B)) - \frac{1}{2} \sin(2\pi(F_{LO} - F_B)) \right] \\
 &= \sin(2\pi(F_{LO} + F_B))
 \end{aligned}$$

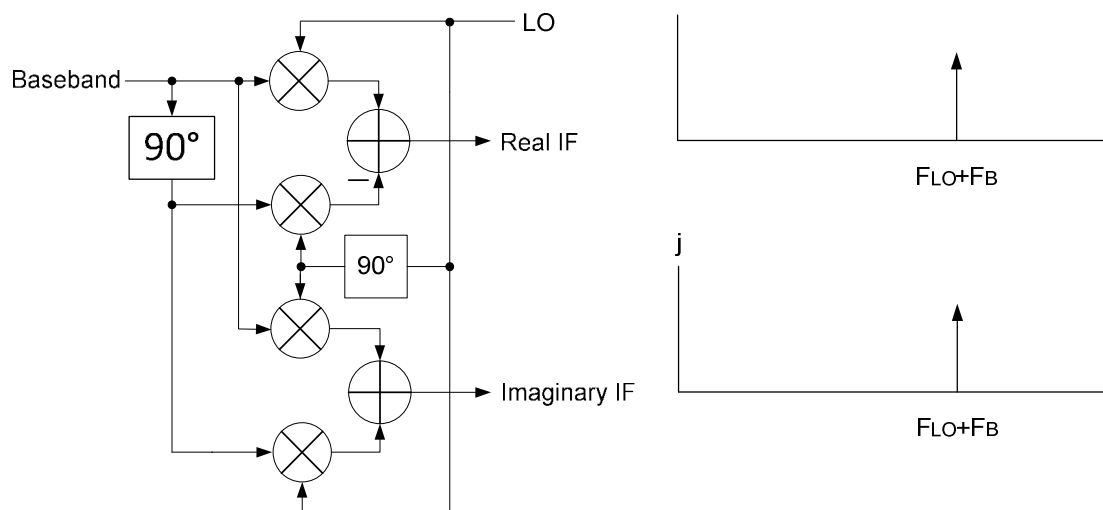


Figure 4-5 Double Quadrature Modulator (Complex)

#### 4.3 Digital Quadrature Modulation

In the analog domain an oscillator is a sine wave and in the digital domain it is a square wave. In order to modulate a signal digitally, the input signal is multiplied by a square wave. To perform quadrature modulation there must be an in phase LO and a quadrature LO, therefore the LO clocks must maintain a specific interval relationship to the  $F_s$  of the input signal. Any oscillator value could be chosen but the cost of implementation is not the same. Consider a cosine wave to be the LO. If samples are taken at  $90^\circ$  intervals the output becomes 1, 0, -1, 0 as shown in Figure 4-6. The quadrature LO will lag  $90^\circ$  behind the in phase LO so it becomes 0, 1, 0, -1 which is also a sine wave sampled at  $90^\circ$  intervals. This is an easy way to implement a quadrature oscillator which requires minimal area and a low level of complexity.

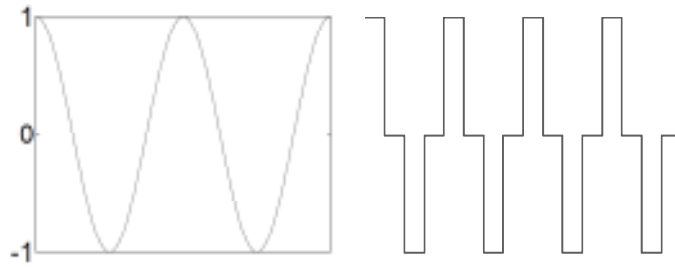


Figure 4-6 90° Samples

#### 4.4 IQ Mismatch Considerations

The purpose of quadrature modulation is to remove the image produced from mixing. A digital modulator will have a perfect IQ match which is impossible for the analog counterpart but at some point the digital signal must become analog in order to be transmitted. It is imperative to understand how mismatch affects the image as this will be of the utmost importance and will dictate the design of the DACs.

Phase and amplitude mismatch will degrade the image cancelling capabilities of a quadrature modulator. Figure 4-7 shows image rejection versus amplitude mismatch and Figure 4-8 shows image rejection versus phase mismatch. Notice that amplitude mismatch is more forgiving than phase mismatch. A mismatch of 1% amplitude will still produce about 47dB of image rejection whereas a 1% phase mismatch will drop the image rejection to 31dB.

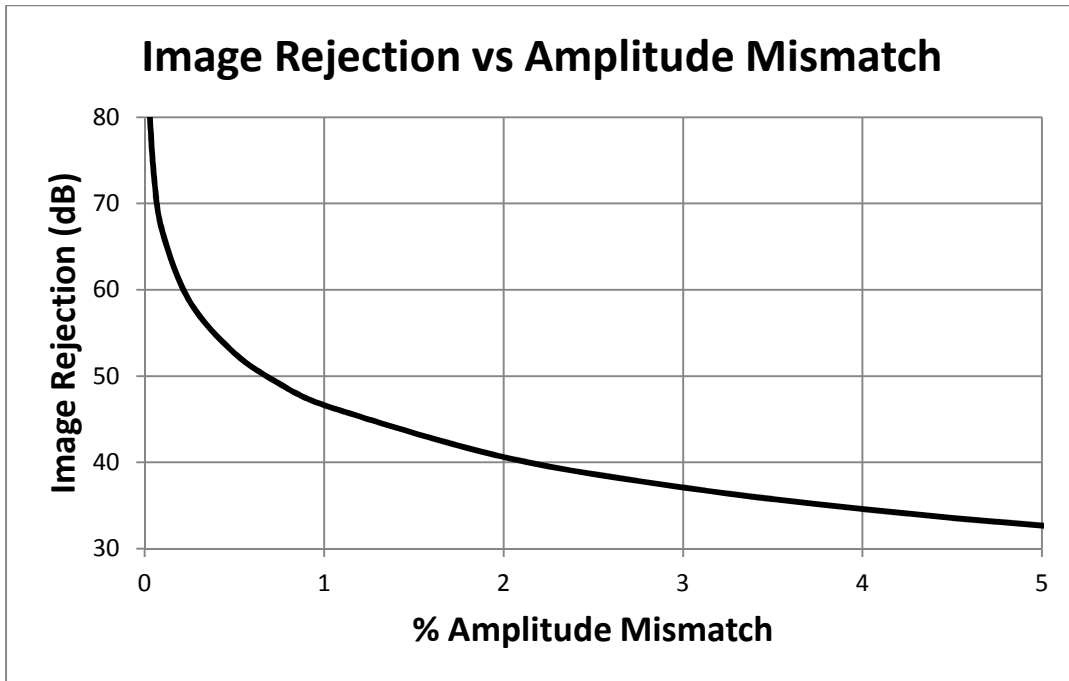


Figure 4-7 Image Rejection vs. Amplitude Mismatch

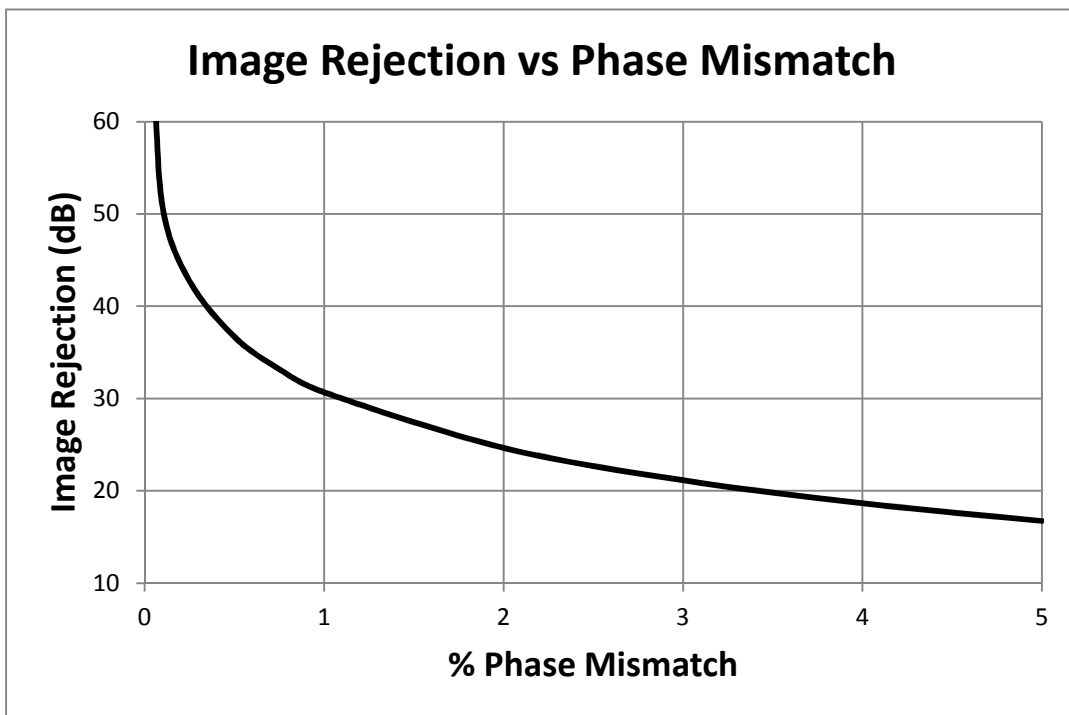


Figure 4-8 Image Rejection vs. Phase Mismatch

#### 4.5 Double Quadrature Modulation Implementation

Shown in Figure 4-9 is a one bit implementation of an  $F_s/4$  mixer which generates the Imaginary IF. The circuit requires the clock to be divided into 4 phases and selects either  $I$ ,  $\bar{I}$ ,  $Q$  or  $\bar{Q}$  for the output depending upon the phase to create the modulated signal. The Real IF is generated with a similar circuit but with different phases as shown in Table 4-1. To create the double quadrature modulator for 12 bit DACs, 24 copies of the circuit in Figure 4-10 are required. As can be seen by the small number of gates, the implementation for digital mixing is very efficient.

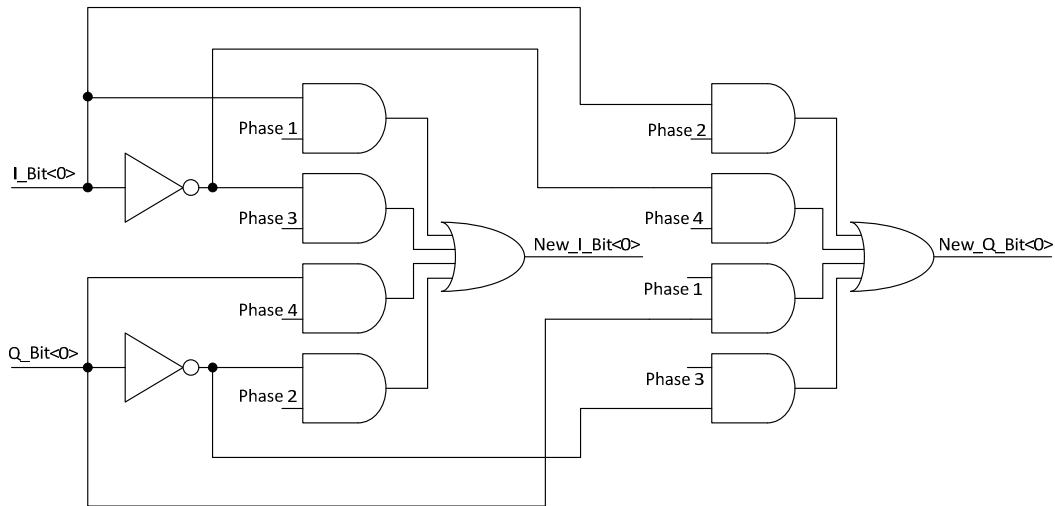


Figure 4-9 One Bit Mixer

Table 4-1 Bit Selection Modulation

Clock Phase	Real IF	Imaginary IF
1	$I$	$Q$
2	$\bar{Q}$	$I$
3	$\bar{I}$	$\bar{Q}$
4	$Q$	$\bar{I}$

## 5 CURRENT STEERING DAC

### 5.1 Current Steering DAC Concepts

A current steering DAC accepts a digital input and “steers” the direction of the current to either the positive or negative output terminal. The output can either be a high side configuration which sources current or a low side configuration which sinks current. The current steering DAC architecture is the preferred choice for obtaining high speed operation. Resistors are generally used to terminate the output of a current steering DAC to perform I-V conversion for further signal processing. 50 ohm termination resistors are the preferred choice for most designs, but 25 – 100 ohms is also quite common. Figure 5-1 depicts an example of a 3 bit low side current steering DAC.

Binary weighted current sources results in the simplest implementation of a current steering DAC but suffers from poor monotonicity, degraded current matching and large switching transients. Thermometer based current sources are monotonic, provide superior matching performance and produce smaller switching transients. A high resolution design based entirely on thermometer code is possible but would be a difficult task from a layout perspective. A segmented approach consisting of both binary and thermometer weighted current sources can provide good performance with reasonable layout requirements. The overwhelming majority of DAC’s in production use a segmented design approach. The upper bits (MSB’s) are thermometer coded since their requirements for matching are more stringent than the lower bits (LSB’s). There are numerous different ways to segment the bits of a DAC. Consider some of the possibilities of segmentation in a twelve bit DAC (6 MSB thermometer + 6 LSB binary),

(6 MSB thermometer + 6 LSB thermometer), (5 MSB thermometer + 4 ULSB thermometer + 3 LSB binary), etc.

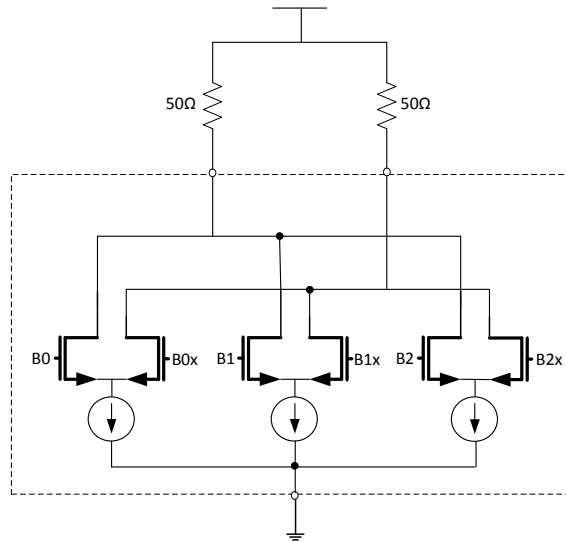


Figure 5-1 Three Bit Current Steering DAC

## 5.2 DAC Architecture

The DACs for this chip are a low side configuration with a segmentation consisting of 4 MSB thermometer, 4 ULSB thermometer and 4 MSB binary. This approach breaks the MSB current sources into 16 unit cells (1 diode connected device and 15 sources).

A dual channel DAC which is to be used in a transmitter application must have a very good match between the I and Q channels in order to achieve reasonable image rejection. Correction circuits are often used to provide a better match both dynamically and statically. A static match can also be achieved with brute force, utilizing area which has the benefit of minimizing risk. Dynamic matching is a real challenge and is an area of active research. The vast majority of the methods described in literature for dynamic correction are not production ready and are based on correction through characterization.

Dual channel DACs currently in production have hooks in the IC for amplitude and phase correction between channels.

The dual channel DAC configuration for this chip was designed as a single DAC rather than two separate entities as shown in Figure 5-2. There is one “golden” current source which sets all of the currents for the DAC’s. The current arrays for each segment are intertwined, i.e. the MSB array contains 16 current sources from each DAC and 1 current setting device. 2 currents leave the MSB and set the ULSB current sources and 1 dummy cell was used for matching. This brings the total number of matching devices to 34 in the MSB array. Internally the DACs will have a good static match due to sharing the same current but the one drawback is that the current can no longer be adjusted to compensate for external resistor mismatch. The primary benefit of using this approach is improvement of the dynamic match. Transients are constantly produced in a DAC from the gate drive of the output switching transients and from the switching of the output itself. Parasitic capacitances allow some of the transients to find their way back to the gate of the current source which sets all of the currents, when this happens the current will change value and require time to recover depending upon the magnitude of the transient. Since both DACs share the same source the error produced becomes common mode thus improving the dynamic match between the channels which increases image rejection. Designing both DAC’s as one promotes better matching from both a design and layout perspective. The output switches that connect to each array are of extreme importance in determining the dynamic match. Both the I and Q DAC switches that control their respective source are in the same schematic cell and are common centroid with respect to the final clock line which actuates them.

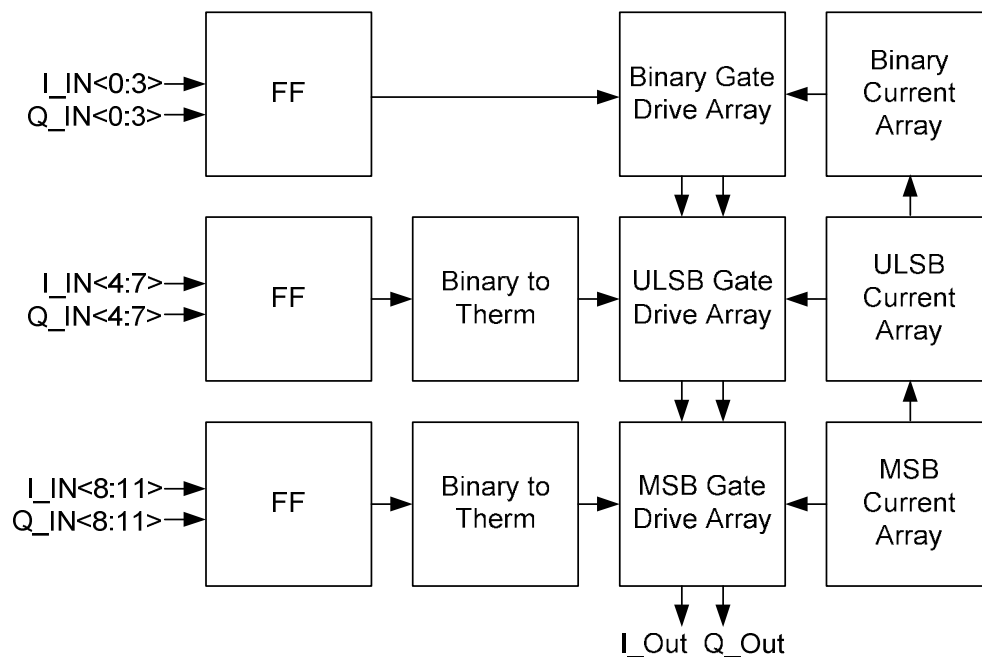


Figure 5-2 Current Steering DAC Block Diagram

Figure 5-3 shows the schematic for the three current arrays. This is a popular technique used by Analog Devices, Inc. which promotes monotonicity by using one bias current to set all of the currents. The amplifiers are implemented as folded cascode OTAs. Notice that the MSB and ULSB devices are double cascoded. With the configuration of the ULSB being fed from the MSB the double cascode is absolutely necessary in order to obtain a high enough output impedance so that current division between the sources of the ULSB is implemented correctly. The second cascode of the MSB was used to increase output impedance and to reduce capacitance by using a small device and placing it close to the switch, thereby reducing settling time for any glitches that might appear at the drain node of the cascode. The output impedance of a DAC changes with each code due to devices being switched in and out of parallel, which is

referred to as code dependent output impedance. Keeping the output impedance high helps to isolate the current sources and minimizes this effect.

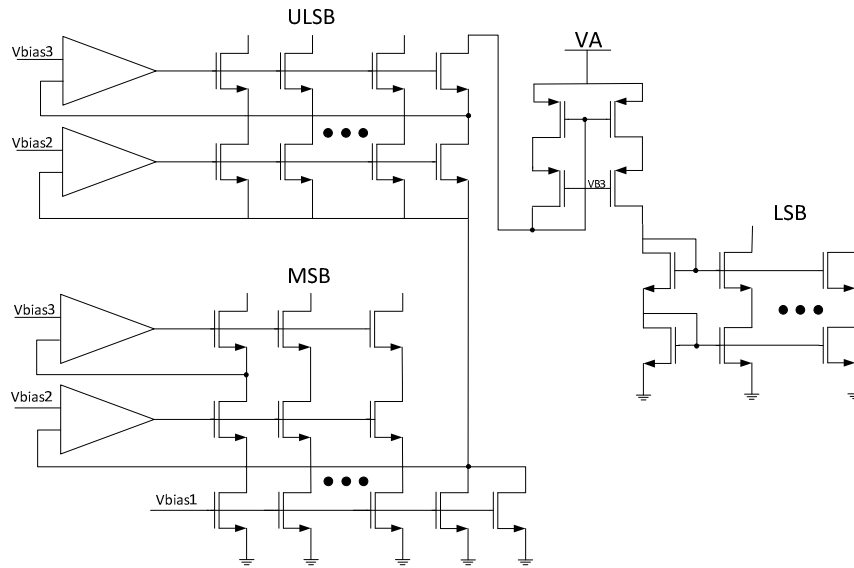


Figure 5-3 Current Array Structure

### 5.3 Gate Drive Design

The goal in designing a gate drive for a differential switch is to try and make the transistors act more like ideal switches. In order to do this the transistors should switch infinitely fast and produce no disturbances.

It is possible to switch a differential pair with a sculpted gate drive which will maintain a constant voltage on the source node. This is non-trivial at fast speeds therefore in general practice a high switch point is chosen to ensure that both devices remain on during the switching transition. This method minimizes source node disturbance and is easily implemented.

This ASIC is intended for one application which targets performance parameters. There were several voltages available (1.8v, 3.3v, 5v) on the customer's system level board implementation which allowed tremendous flexibility in controlling the gate drive

for the differential switch to achieve optimal results. The switching voltage was chosen to be from 1.8v to 3.3v. This is more than the minimum voltage required to switch but switching between power rails has the benefit of being able to source and sink large currents so that the gates of the switching transistors can be charged and discharged quickly. This was shown to have a greater impact on performance than gate feedthrough caused by the larger switching transitions.

The input signal used to determine if the switch will be positive or negative is generated from 1.8V logic and must be level translated to the higher voltage. One way to accomplish this is shown in Figure 5-5. The current source provides a pull-up bias for the gate of M2 when M1 is turned off. The resistor is used to limit the current that will be sourced through M1 when its gate is pulled low by M3. The current can be set to a low value but there is a power trade-off between the value of the resistor and the frequency of operation. The resistor forms a low pass filter with the gate of M2 so the larger the resistor the longer it will take to turn M2 off when M4 is turned on. M4 and M2 were sized to minimize this effect. The lower inverter and buffer have matched delays.

The actuating signal comes from a separate circuit referred to as the High Clock which transitions between 3.3V and 1.8V. In Figure 5-4 the upper flip flop was designed by hand for high frequency operation otherwise all of the basic digital cells were from a standard cell library provided by the foundry. The cross coupled inverter at the output is used to actuate the differential switch and was made popular by [Van den Bosch]. A high switch point can be achieved through proper sizing.

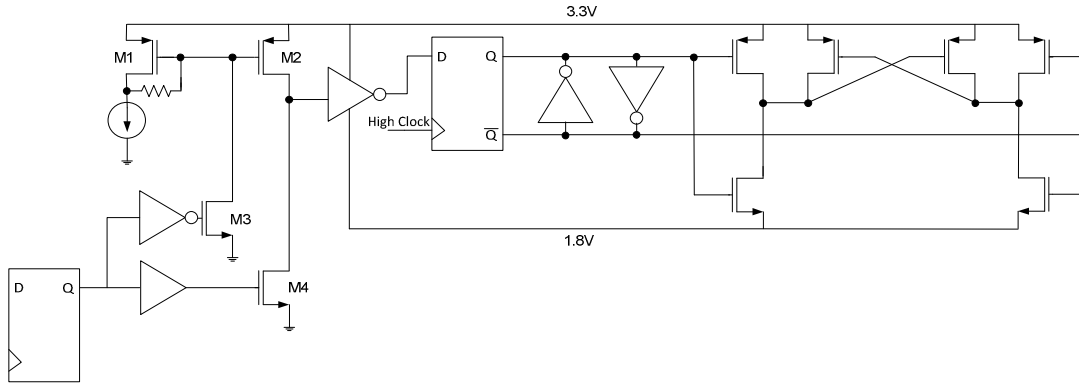


Figure 5-4 Gate Drive

#### 5.4 Differential Switch Considerations

For a high speed design the differential switch must remain in saturation. It is also desirable to use small devices to keep parasitic capacitances low, thereby increasing switching speed and reducing both gate and output feedthrough. Capacitance must also be kept small at the source node so that any disturbance generated on that node can settle quickly to maintain the tail current at the desired level. For this design a simple differential switch was chosen as shown in Figure 5-1. In section 5.3 it was noted that the actuating voltage for the switch is between 1.8V and 3.3V. A 3.3v device was used for the switch. The 50 ohm output resistors are intended to be connected to the available 5V supply. The switch is isolated in a deep trench with bulk connected to source to prevent overvoltage.

During the design process, a cascoded switch implementation was investigated. In theory, cascoding would provide an advantage because the differential switch would be isolated from the switching transients generated at the output plus the switch would remain in a tighter controlled region of operation due to maintaining a constant  $V_{DS}$ . There are 3 problems associated with cascoding the switch. The first obvious problem is

that additional capacitance is added to the output node which significantly hinders high frequency performance at low current levels. Another problem is due to a leakage current which flows from drain to bulk of the cascode device when it is sinking current. For a high resolution design cascoding would require deep n-well or deep trench isolation to prevent SNR degradation. Another potential problem will occur if a cascode device stays off long enough for the source node to float high causing the device to enter the cutoff region. In this case a small glitch may occur when the device turns on as it enters saturation again. This problem is exacerbated at low current levels.

### 5.5 Sizing for Mismatch and Noise

One of the main things to consider in designing a DAC is the size of the current sources that will be required in order to achieve a desired static resolution. In this case 12 bits was the target so a certain amount of tolerable error had to be decided upon. A quarter of an LSB is generally considered to be a reasonable target. This DAC will normally be used at the maximum FSR current of 30mA which gives an LSB current of approximately 7.3uA, so a quarter of an LSB would be about 1.8uA. The MSB sources are divided into 16 unit cells carrying a maximum current of 1.875mA, therefore the required match would be 0.096%.

Referring back to Figure 4-7 Image Rejection vs. Amplitude Mismatch, a mismatch of 0.1% will provide about 67dB of image rejection which is adequate for IQ matching. Consider the extreme codes for a DAC, near maximum and minimum values; there will be many devices in parallel on one terminal but only a few in parallel on the other which would lead to the worst case matching condition. The middle codes will have the best overall match between the two DAC's. Therefore a 0.1% static mismatch

at 1 sigma should correspond to the extreme code conditions and be the worst case between the two channels.

The MSB current sources were designed for a 1 sigma 0.096% mismatch which was verified using a monte carlo simulation with mismatch models provided by the foundry. The ULNB current array is comprised of 16 current cells and requires a 1.5% match for a quarter of an LSB deviation. The binary array requirement is further reduced to the following values for each consecutive bit: 3%, 6%, 12% and 25%.

The cheapest way to improve mismatch is to use a high overdrive if headroom is available.  $V_t$  mismatch effects are considerably reduced with a lower  $g_m$ . After headroom is exhausted, area can be increased to satisfy system requirements. Mosfet mismatch improves with the inverse square root of the area.

$$\% \text{ Desired Mismatch} = \frac{\% \text{ Present Mismatch}}{\sqrt{(\text{Present Area}) * K}}$$

For example, if a device currently has a 10% mismatch and the desired match is 1%, the area would have to be increased by 100. Correction circuits are often used to increase matching without increasing area at the cost of system complexity and are generally a necessity for DAC's greater than 12 bit resolution.

When designing a DAC it is important to take thermal and flicker noise into consideration so that it doesn't interfere with meeting SNR requirements. Thermal noise of a current mirror will reduce with increased area and with increased overdrive voltage. Flicker noise is primarily dependent upon device area. Diode connected devices contribute a lot of noise so it is important to minimize the number of current mirror translations in a design for both noise and mismatch. In this design, headroom was

abundant so overdrive of the MSB current sources was maximized (500mV). The majority of the cascodes were sized to have an overdrive of 250mV.

## 5.6 DAC Performance

The maximum achievable SNR of a data converter is given by  $SNR_{dB} = 6.02 * (\# \text{ of bits}) + 1.76$ . The maximum SNR for a 12 bit DAC is 74dB. A “perfect” zero order hold output signal is needed to achieve this value, which can be approximated fairly close up to a given range of output power and frequency. For a DAC with a large number of devices, an FFT with a reasonable number of cycles requires a long simulation time due to the oversampling needed to capture the majority of the transients. Figure 5-5 shows an output FFT of one DAC at maximum power (FSR=30mA and 50 ohm resistors) with a sampling frequency of 400MHz and an input signal of approximately 73.7 MHz. The output of the DAC was sampled at 4GHz, which was considered to be the minimum value needed to accurately depict performance. The plot is shown up to  $F_s/2$  (200MHz). At this bandwidth the DAC produces 70dB of SNR, which equates to an ENOB of 11.3 bits.

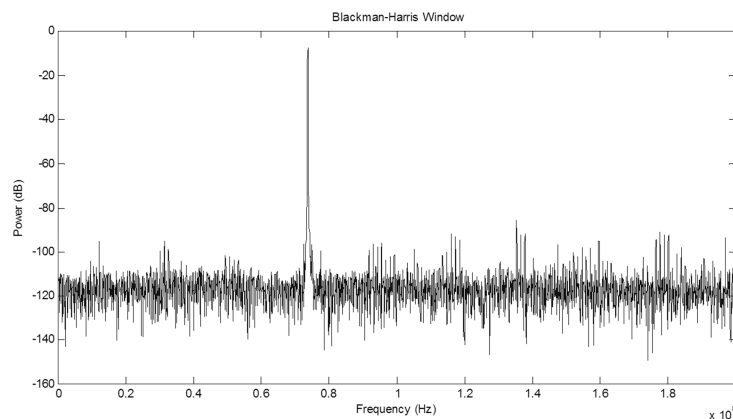


Figure 5-5 DAC FFT

The FFT in Figure 5-5 took about a week to run and still shows spreading at the fundamental. Transient simulation can provide initial feedback into the performance of a DAC within a few minutes which drastically reduces the design time required for meeting performance objectives. Insight is gained by analyzing the overshoot, undershoot and settling time. Transient parameters are code dependent so it is important to establish a specific code transition to determine the SNR for comparison tests.

### 5.7 DAC Layout

Current steering DAC's are heavily dependent upon layout to achieve a good static and dynamic match. From a physical design perspective, the static match is dependent upon the layout of the current arrays whereas the dynamic match is dependent upon the routing and interconnection of the final clock line to the gate drive circuits which actuate the output current signal. The following paragraphs describe a few layout techniques which were used to help achieve the desired SNR that was reflected in simulation.

The MSB current array is shown in Figure 5-6. Each I and Q channel consists of 16 current sources with one current setting device which brings the total number of matched devices to 33. One dummy was added to the array to make it an even 34. The unit cells were further broken down into 32 unit cells. The figure below would be considered a strong common centroid. It was designed in this manner based on its pattern and ease of wiring. The devices form overlapped Xs and Vs which must then be connected horizontally so it requires several layers of metal to implement this centroid. In order to make the layout reasonably compact the source metal must cover the devices

so that the metal runs connecting the devices do not have to match. It is preferable to have the metal which covers the devices to be as high as possible.

A	B	C	D		D	C	B	A
1	2	3	4		4	3	2	1
C	D	A	B		B	A	D	C
3	4	1	2		2	1	4	3
3	4	1	2		2	1	4	3
C	D	A	B		B	A	D	C
1	2	3	4		4	3	2	1
A	B	C	D		D	C	B	A

Figure 5-6 MSB Array

The ULSB current array is shown in Figure 5-7. A standard common centroid was used for this cell since it does not need to match as well as the MSB array.

A	B	C	D		D	C	B	A
1	2	3	4		4	3	2	1
D	C	B	A		A	B	C	D
4	3	2	1		1	2	3	4
4	3	2	1		1	2	3	4
D	C	B	A		A	B	C	D
1	2	4	4		4	3	2	1
A	B	C	D		D	C	B	A

Figure 5-7 ULSB Array

The most important clock line in a DAC is the final clock which actuates the output gate drive. Any mismatch will cause a phase error and degrade the IRR. The final clock line was wired on top layer metal in a symmetrical fashion with an I switch bank on one

side and Q on the other. The incoming clock signal from the clock generator was kelvin connected to the 3 switch arrays to provide a solid dynamic match of the clock line. Parasitic extraction was performed to verify that the clock routing would be sufficient to meet the design requirements.

## 6 FINAL DESIGN

### 6.1 Top Level

The block level diagram of Figure 1-1 is a fairly good representation of the chip but excludes a few primary cells, the bias generator and clock generator.

There are a total of 5 clocks in this system which must work in unison. The digital mixer requires clock division by 2 and 4 to generate the phases necessary for modulation and the interpolation filters require clock division by 2, 4 and 8. A “high” clock is derived from the master clock for improved actuation of the output differential switch. The clocks are retimed and buffered after being divided down. The clock generator circuit supplies these clocks to the chip, controls the bypass modes of operation and signals for the synchronizing output clock.

The bias generator operates as a pseudo bandgap. A voltage input of 1.25V is accepted from a pin on the chip and is buffered to another pin connected to an external resistor which sets the “golden” current for the DACs. The current in the resistor is equivalent to the current in one MSB cell. Another amplifier inside the chip biases a poly resistor which sets the currents for all of the additional internal biasing.

A chip containing this many transistors can be challenging to simulate at the top level due to extremely long time requirements. At the top level functionality was tested

utilizing Ultrasim. Performance simulations were completed at the cell level with Spectre.

## 6.2 Pin Configuration and Description

The pin configuration for the chip is shown in Figure 6-1 and the pin descriptions in Table 6-1. There are 2 separate power supplies, VDD (1.8V digital supply) and VA (3.3V analog supply). VDD draws 500mW and VA draws 100mW at 400 MSPS operation. At the request of the customer the input was made parallel LVDS. The number of input pins could have been reduced by sharing the IQ pins and alternating their input sequence. This alternative method is popular in industry due to the lowered pin count but requires the update rate to be double.

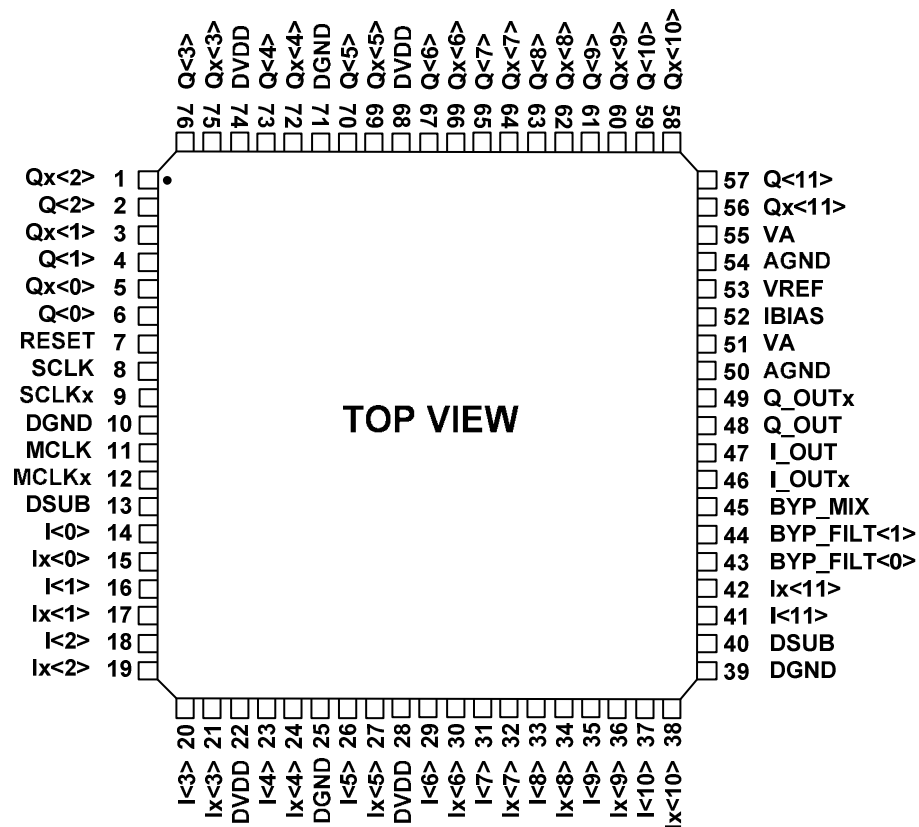


Figure 6-1 Pin Configuration

Table 6-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1,3,5,56,58,60 62,64,66,69,72,75	Qx<0:11>	Q negative input data, twos complement, LVDS
2,4,6,57,59,61 63,65,67,70,73,76	Q<0:11>	Q positive input data, twos complement, LVDS
7	RESET	Logic 0 resets all of the digital latches (1.8V Logic)
8	SCLK	Output synchronizing clock positive, LVDS
9	SCLKx	Output synchronizing clock negative, LVDS
10,25,39,71	DGND	Digital common
11	MCLK	Master clock positive input, LVDS
12	MCLKx	Master clock negative input, LVDS
13,40	DSUB	Digital substrate common
14,16,18,20,23,26 29,31,33,35,37,41	I<0:11>	I positive input data, two's complement, LVDS
15,17,19,21,24,27 30,32,34,36,38,42	Ix<0:11>	I negative input data, two's complement, LVDS
22,28,68,74	DVDD	Digital supply voltage (1.8V)
43	BYP_FILT<0>	Binary input used to bypass filters (1.8V Logic)
44	BYP_FILT<1>	Binary input used to bypass filters (1.8V Logic)
45	BYP_MIX	Logic 1 bypasses digital mixer (1.8V Logic)
46	I_OUTx	Negative I channel current output
47	I_OUT	Positive I channel current output
48	Q_OUT	Positive Q channel current output
49	Q_OUTx	Negative Q channel current output
50,54	AGND	Analog common
51,55	VA	Analog supply voltage (3.3V)
52	IBIAS	Current output, An external resistor placed from the pin to common sets the full scale range current of the DACs
53	VREF	High impedance reference voltage input (1.25V), Replicates a bandgap voltage

### 6.3 Floorplan

The floorplan of the chip is shown in Figure 6-2. It would have been preferred to have the current arrays close to each other but it was done in this manner to make routing of the signal lines more convenient. The currents which are fed from the MSB current

array to the ULSB current array and from the ULSB current array to the binary currents are ran in coax lines to prevent switching noise from affecting the biasing.

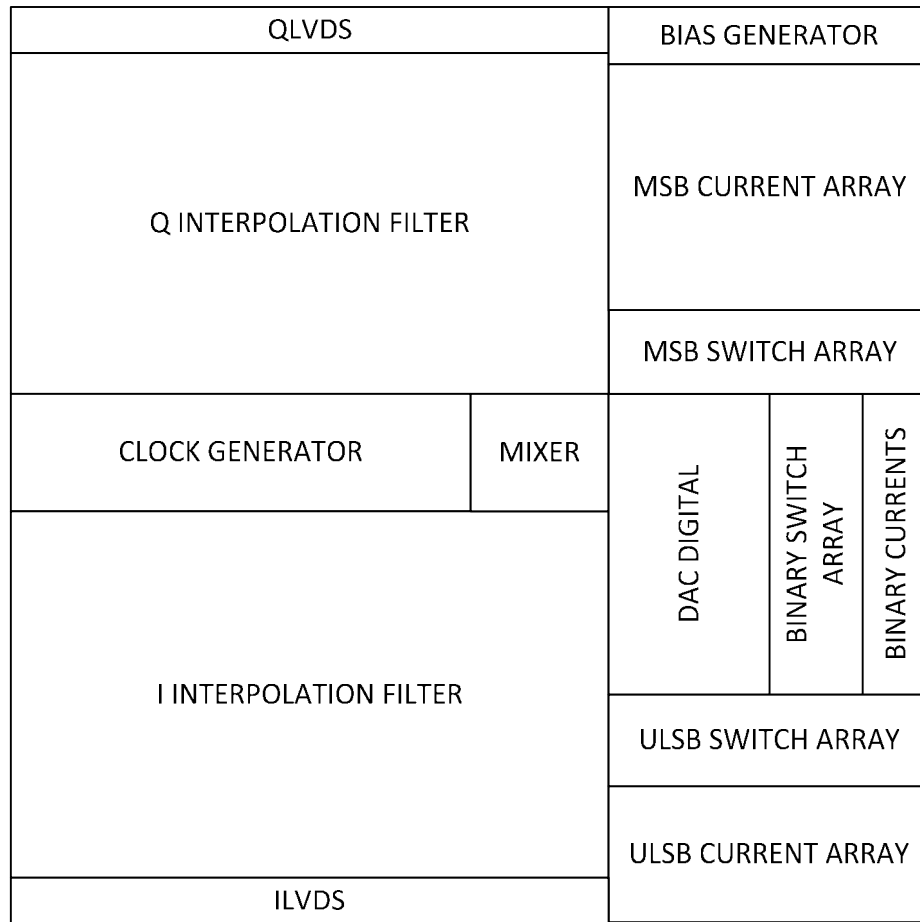


Figure 6-2 Floorplan

#### 6.4 Layout

The final chip layout is shown in Figure 6-4. At the customer's request, a second row of bond pads were added to provide the option for additional power and ground connections. Due to the high current requirement of the digital section large buses of top metal run the length of the chip connected to pins on both sides and branch out in a fingered fashion creating a solid power grid. A few lines had to run behind the bond pads for proper connection. The chip was fabricated on a multi-project wafer run which

delivers 5mm x 5mm tiles independent of active circuit size therefore area was abundant and was not a concern in the design. The active circuit area of the chip is approximately 4.1mm x 4.7mm.

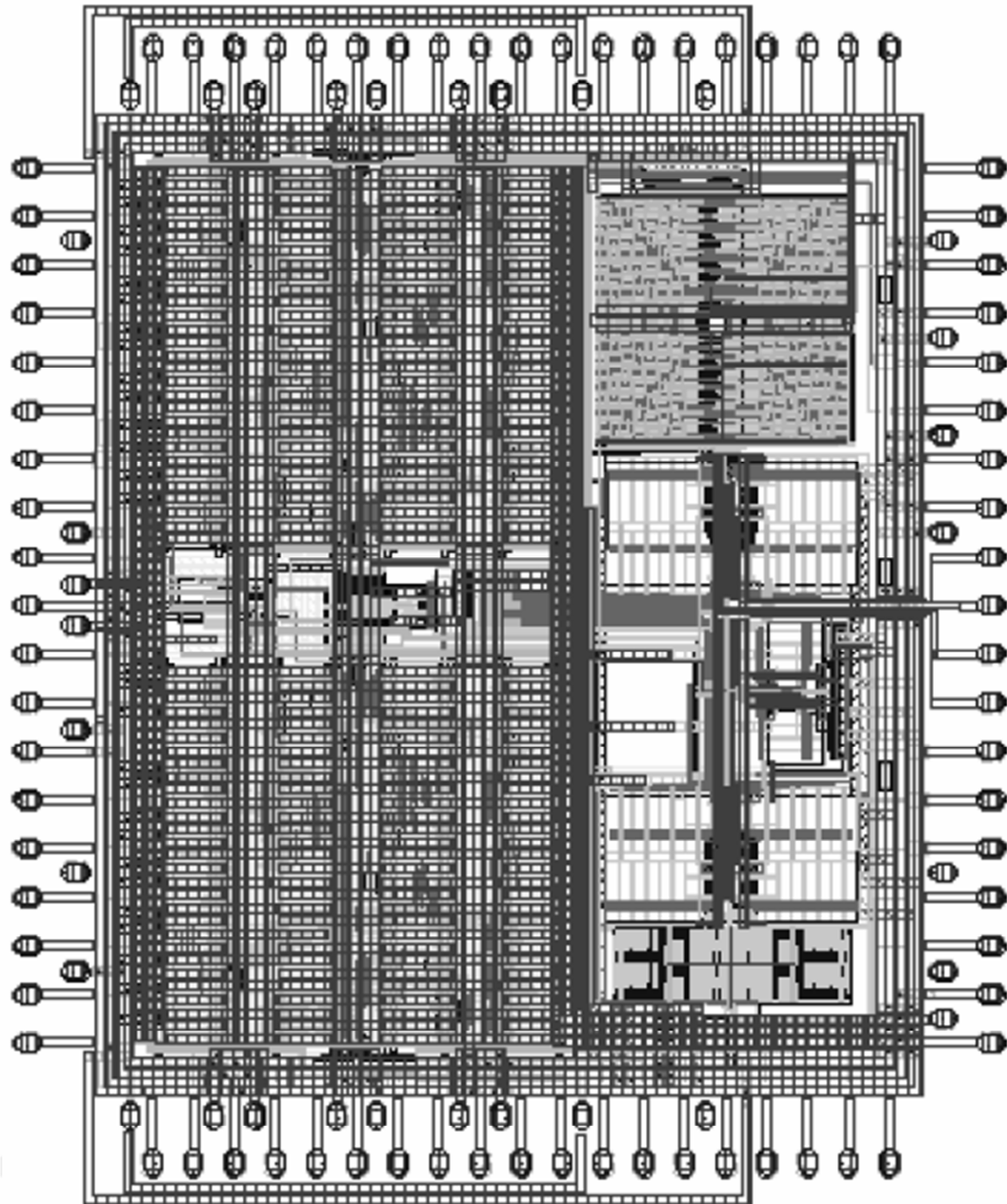


Figure 6-3 Layout

## 6.5 Conclusion and Future Work

The work presented in this thesis was based primarily upon proven methods of implementation. No major risks were taken due to a tight schedule and the customers desire to produce a low risk chip with a high chance of first past success. During the design process, two main areas of interest were investigated, analog FIR implementations and correction circuits. These two areas complement each and are being used for my current and future research.

The motivation for the analog FIR implementation was made keenly aware after viewing the layout area of the digital filters and their corresponding power requirements. A switched current approach has numerous advantages due to wired addition and scalable multiplication. For example, the multipliers could be implemented as current mirrors and the adders could be eliminated by connecting the drains of the output transistors together to sum the currents. From a die area and power standpoint this is a huge savings, but there are many hurdles to overcome.

Correction circuits provide a very attractive area of research offering many possibilities. During the course of this research several correction schemes were analyzed involving static and dynamic methods. Static correction at start up is most interesting because it introduces methods to increase die yield and has numerous applications without the associated risks of continuous and dynamic correction. The mixed-signal FIR filter is just one case which would be applicable, correcting for the multiplier coefficient currents. Applications for correction circuits are literally found everywhere in analog design.

## REFERENCES

- Analog Devices, Inc. 16-Bit, 160 MSPS 2x/4x/8x Interpolating Dual TxDAC+D/A Converter. Datasheet. Norwood: Analog Devices, Inc., 2006.
- Bakkaloglu, Bertan, Hongjiang Song and Syed Roomi Naqvi. "I/Q-Channel Mismatch Transfer and Amplification Effects and Applications to the Measurement and Calibration of Integrated VLIF RF Receivers." IEEE International SOC Conference (2006): 35-38.
- Bastos, Jose, et al. "A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC." Volume 33, No. 12. 1998.
- Chen, Mingdeng, et al. "Low-Voltage Low-Power LVDS Drivers." IEEE Journal of Solid-State Circuits (n.d.): Volume 40, No. 2.
- Crols, Jan, Peter Kinget and Michiel Steyaert. A Double Quadrature Topology for High Accuracy Upconversion in CMOS Transmitters. Academic. Heverlee: Katholieke Universiteit Leuven, n.d.
- Fairchild Semiconductor. "AN-5017 LVDS Fundamentals." Application Note. 2005.
- Harris, Fredrick J. Multirate Signal Processing for Communication Systems. New York: Prentice Hall, 2004.
- Hastings, Alan. The Art of Analog Layout. 2nd. Prentice Hall, 2005.
- Hogenauer, Eugene. "An Economical Class of Digital Filters for Decimation and Interpolation." IEEE Trans. Acoustics, Speech, and Signal Processing (1981): ASSP-29.
- Huq, Syed B. and John Goldie. "An Overview of LVDS Technology." Application Note 971. 1998.
- Kempainen, Stephen. "Low-Voltage Differential Signaling (LVDS)." Application Note. 2002.
- Kester, Walt. The Data Conversion Handbook. Burlington: Newnes, 2005.
- Lattice Semiconductor. "Using Differential I/O (LVDS, Sub-LVDS) in iCE40 Devices." Technical Note TN1253. 2013.
- Losada, Ricardo A. "Digital Filters with MATLAB." Report. 2008.
- Lyons, Richard G. Understanding Digital Signal Processing. 2nd. Upper Saddle River: Prentice Hall, 2004.

Lyons, Richard. "Sum of Two Sinusoids." Report. 2011.

Martin, Ken. Complex Signal Processing is Not-Complex. Academic. Toronto: University of Toronto, n.d.

Martins, R. P., et al. "A Multistandard Transmitter D/A Interface with Embedded Frequency Up-Conversion and Two-Step Channel Selection." IEEJ International (2004): Analog Workshop.

Maxim. 16-Bit, 500Msps, Interpolating and Modulating Dual DAC with Interleaved LVDS Inputs. Datasheet. Sunnyvale: Maxim, 2010.

McClanin, Kevin. Wireless Receiver Design for Digital Communications. 2nd. Raleigh: Scitech Publishing, Inc., 2012.

Mercer, Douglas A. Digital to Analog Converter Design. Presentation. Wilmington: Analog Devices, Inc., 2008.

Palmer, Pieter and Michiel S. Steyaert. "A 10-Bit 1.6-GS/s 27-mW Current-Steering D/A converter with 550-MHz 54-dB SFDR Bandwidth in 130-nm CMOS." IEEE Transactions on Circuits and Systems (2010): Volume 57, No. 11.

Parikh, Viral K., Balsara T. Poras and Oren E. Eliezer. "All Digital-Quadrature-Modulator Based Wideband Wireless Transmitters." IEEE Transactions on Circuits and Systems-I (2009): Volume 56, No. 11.

Pun, Kong-Pang, et al. "Quadrature Sampling Schemes with Improved Image Rejection." IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing (2003): Volume 50, No. 9.

Salomon, O. and J.M., Clare, H. Green. "General Algorithms for a Simplified Addition of 2's complement Numbers." IEEE Journal of Solid State Circuits (1995): Volume 30, No. 7.

Schafer, Ronald W., Rabiner, Lawrence R. "A Digital Signal Processing Approach to Interpolation." Proc. IEEE (1973): Volume 61, Pages 692-702.

Song, Hongjiang. VLSI Analog Signal Processing Circuits. Xilbris Corporation, 2009.

Srinivasan, Venkatesh, Gail Rosen and Paul Hasler. Low-Power Realization of FIR Filters Using Current-Mode Analog Design Techniques. Academic. Atlanta: Georgia Institute of Technology, n.d.

Srinivasan, Venkatesh, Gail Rosen and Paul Hasler. "Low-Power Realization of FIR Filters Using Current-Mode Analog Design Techniques." IEEE (2004): 2223-2227.

Standard. "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits." TIA/EIA-644. 1996.

Standard, IEEE. "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent." Std 1596.3-1996. 1996.

Su, Chao and R.L. Geiger. "Dynamic Calibration of Current-Steering DAC." IEEE (2006): 117-120.

Tajalli, Armin and Yusuf Leblebici. "A Slew Controlled LVDS Output Driver Circuit in 0.18 um CMOS Technology." IEEE Journal of Solid-State Circuits (2009): Volume 44, No. 2.

Texas Instruments. Dual-Channel, 16-Bit, 1.25 GSPS Digital-to-Analog Converter (DAC). Datasheet. Dallas: Texas Instruments, 2012.

—. "LVDS Owner's Manual." Industry Report. 2008.

Vaidyanathan, P.P. and Truong Q. Nguyen. "A "Trick" for the Design of FIR Half-Band Filters." IEEE Transactions on Circuits and Systems (1987): Volume CAS-34, No. 3.

Vaidyanathan, P.P. "Multirate Digital Filters, Filter Banks, Polyphase Networks, and Applications: A Tutorial." Proceedings of the IEEE (1990): Volume 78, No. 1.

Van den Bosch, A., et al. "A 10-Bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter." IEEE Journal of Solid State Circuits (2001): Volume 36, No. 3.

Wiegmann, G. and E.A. Vittoz. Analysis and Improvements of Highly Accurate Dynamic Current Mirrors. Academic. Lausanne: Swiss Federal Institute of Technology, n.d.

Wikner, J. Jacob. Studies on CMOS Digital-to-Analog Converters. Dissertation. Linkoping: Linkopings Universitet, 2001.

Xilinx. "Distributed Arithmetic FIR Filter v9.0." Product Specification. 2005.

Zhang, Yi. "Wireless Transmitter IQ balance and Sideband Suppression." Application Note. 2010.