Hafnium Oxide as an Alternative Barrier to Aluminum Oxide

For Thermally Stable Niobium Tunnel Junctions

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved November 2013 by the
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ARIZONA STATE UNIVERSITY

December 2013

ABSTRACT

In this research, our goal was to fabricate Josephson junctions that can be stably processed at 300°C or higher. With the purpose of integrating Josephson junction fabrication with the current semiconductor circuit fabrication process, back-end process temperatures (>350 °C) will be a key for producing large scale junction circuits reliably, which requires the junctions to be more thermally stable than current Nb/Al-AlO_x/Nb junctions.

Based on thermodynamics, Hf was chosen to produce thermally stable Nb/Hf-HfO_x/Nb superconductor tunnel Josephson junctions that can be grown or processed at elevated temperatures. Also elevated synthesis temperatures improve the structural and electrical properties of Nb electrode layers that could potentially improve junction device performance. The refractory nature of Hf, HfO_2 and Nb allow for the formation of flat, abrupt and thermally-stable interfaces. But the current Al-based barrier will have problems when using with high-temperature grown and high-quality Nb. So our work is aimed at using Nb grown at elevated temperatures to fabricate thermally stable Josephson tunnel junctions.

As a junction barrier metal, Hf was studied and compared with the traditional Al-barrier material. We have proved that Hf-HfO_x is a good barrier candidate for high-temperature synthesized Josephson junction. Hf deposited at 500 °C on Nb forms flat and chemically abrupt interfaces. Nb/Hf-HfO_x/Nb Josephson junctions were synthesized, fabricated and characterized with different oxidizing conditions. The results of materials characterization and junction electrical measurements are reported and analyzed. We have improved the annealing stability of Nb junctions and also used high-quality Nb

grown at 500 °C as the bottom electrode successfully. Adding a buffer layer or multiple oxidation steps improves the annealing stability of Josephson junctions. We also have attempted to use the Atomic Layer Deposition (ALD) method for the growth of Hf oxide as the junction barrier and got tunneling results.

ACKNOWLEDGMENTS

First of all, I would like to express my deepest gratitude towards my thesis advisor, Professor Nathan Newman, for his invaluable guidance, numerous encouragements and generous support throughout these years. I am grateful for the excellent research facilities that he made possible, for the help that he gave me to tackle the challenges, and for the completion of this thesis. Special thanks should also be sent to Professor John Rowell, for his tremendous guidance and valuable support. The days that I spent with them helped me grow up as a mature scientist.

I would like to thank the other committee members, including Professor Rakesh Singh, Professor Ralph Chamberlin and Professor Robert Wang for their constructive criticism to my research. I appreciate all their effort for their detailed suggestions and corrections to my dissertation.

I am deeply indebted to all my colleagues in my research group at Arizona State University for their assistance. Professor Rakesh Singh shared his knowledge about vacuum technology and material characterization techniques. Dr. Lei Yu spent numerous hours of valuable time discussing my thesis work with me. Mr. Richard Hanley and Mr. Kevin Bunish assisted me to solve numerous facility problems in the lab. Dr. Brett Strawbridge and Dr. Yi Shen gave me fruitful advice on thin film growth and device fabrication. Mr. Makram Qader, Mr. Shengke Zhang and Miss Tiantian Zhang shared great ideas and articles in the work. I need to show my gratitude to Mr. You Li and Mr. Cameron Kopas for RBS and XRD characterizations. I want to thank all the other members of the group for the enlightening discussion and vigorous support. These members include: Dr. Lingtao Liu, Dr. Mahmoud Vahidi, Mr. Lei Zhang, Mr. Chris

Traverse, Mr. Patrick Murray, Dr. Zhizhong Tang, Dr. Stephen Lehner, Dr. Subhasish Bandyopadhyay, Mr. Shail Sanghavi, Mr. Nathan Cardinell, Miss Michelle Myers, Mr. Defeng Tao, Miss Sarah Galvin and Mr. Rahul Mitra.

I wish to give my gratitude to all the faculties and staff at the LeRoy Eyring Center for Solid State Science, for informative discussions about research facilities and characterization techniques. I want to thank Professor Ray Carpenter and Dr. John Mardinly for TEM characterization, Mr. Timothy Karcher for XPS measurements and thin film growth, Dr. Klaus Franzreb and Dr. Barry Wilkins for SIMS and RBS measurements, Mr. David Wright for cryogenic temperature measurements, Mr. Kenneth Mossman for AFM measurements and Dr. Zhenquan Liu for SEM measurements. I also wish to thank the faculties and staff at the School of Engineering, for intellectual discussions and selfless help, as well as the staff at Center for Solid State Electronics Research. These people include Professor Terry Alford, Professor Peter Crozier, Professor Dieter Schroder, Professor Van Schilfgaarde and Professor Michael Kozicki.

Getting a Ph. D. degree is a journey that I will never forget with the spiritual and material support from my family. My parents, my mother Ligai Zhang and father Fuwu Huang, I am grateful to you for everything I have achieved here. Special thanks to my girlfriend, Miss Ying Sun, for all the joy she brings to my life. Last but not least, I wish to thank all my close friends, for your support and inspiration, including Mr. Liuxian Zhang, Mr. Xiaofeng Wang, Mr. Liang Huang, Mr. Xiaoli Ma, Dr. Yang Wu, Mr. Hao Wu, Miss Pai Liu, Mr. Dexuan Wang and Mr. Xuan Yang.

DEDICATION

To my parents and my girlfriend

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Chapter 1

MOTIVATION AND INTRODUCTION

In 1962, Brian Josephson predicted that super-current (current existing without voltage, its maximum value is called critical current or I_c) can tunnel through an insulator between two superconductive electrodes [1], as shown in Figure 1.1. This phenomenon is named the Josephson Effect, and the device is called a Josephson junction. The first direct observation of this effect was made by John Rowell and Phillip Anderson in 1963, with a $Sn/SnO_x/Pb$ cross-type junction. [2] The super-current is induced by Cooper pairs, according to the BCS theory. [3, 4] Cooper pairs are formed at low temperature when an electron can attract another electron through interaction with the crystal lattice in superconductors. Formation of Cooper pairs can reduce the energy of electrons near the Fermi level and create an energy gap (Δ) between the ground state and the excited state of a superconductor.

1.1 Overview of Josephson junctions

1.1.1 I-V characteristic of Josephson junctions

I-V characteristic of an ideal Josephson junction at 0 K is shown in Figure 1.2. [5] When V=0, there is only super-current (I_c) induced by Cooper pair tunneling. The maximum value of the I_c is

$$I_c = \pi\Delta(T)\tanh\left(\frac{\Delta(T)}{2k_B T}\right)/2R_n e$$

derived by BCS theory [4], which is close to the normal-state current at ($\pi/4$) of the gap voltage $V_g=2\Delta/e$.

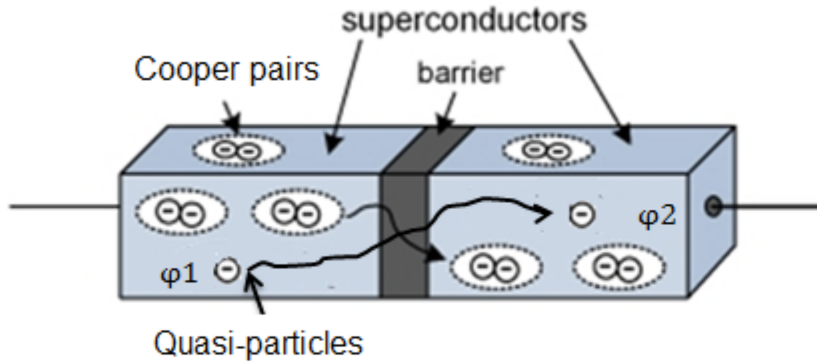


Figure 1.1. Scheme of a Josephson junction

When $0<V<2\Delta$, the subgap current is induced by single electrons (or called quasi-particles) tunneling. In the ideal case (including some practical Nb/Al-AlO_x/Nb junctions with great quality), this subgap current is zero at T=0 K, and only reflects thermal excitation of single electrons at T>0 K (which is very small when $T \ll T_c$); in most of the actual devices, part of the subgap current may also come from defects, nano-shorts in the barrier causing Andreev reflection, etc.. The current rises to $2\Delta(T)/R_n e$ near $V=2\Delta$.

When $V>2\Delta$, the IV curve becomes a straight line, with a normal resistance ($R_n=\frac{dV}{dI}$). R_n depends on the thickness and height of the tunnel barrier.

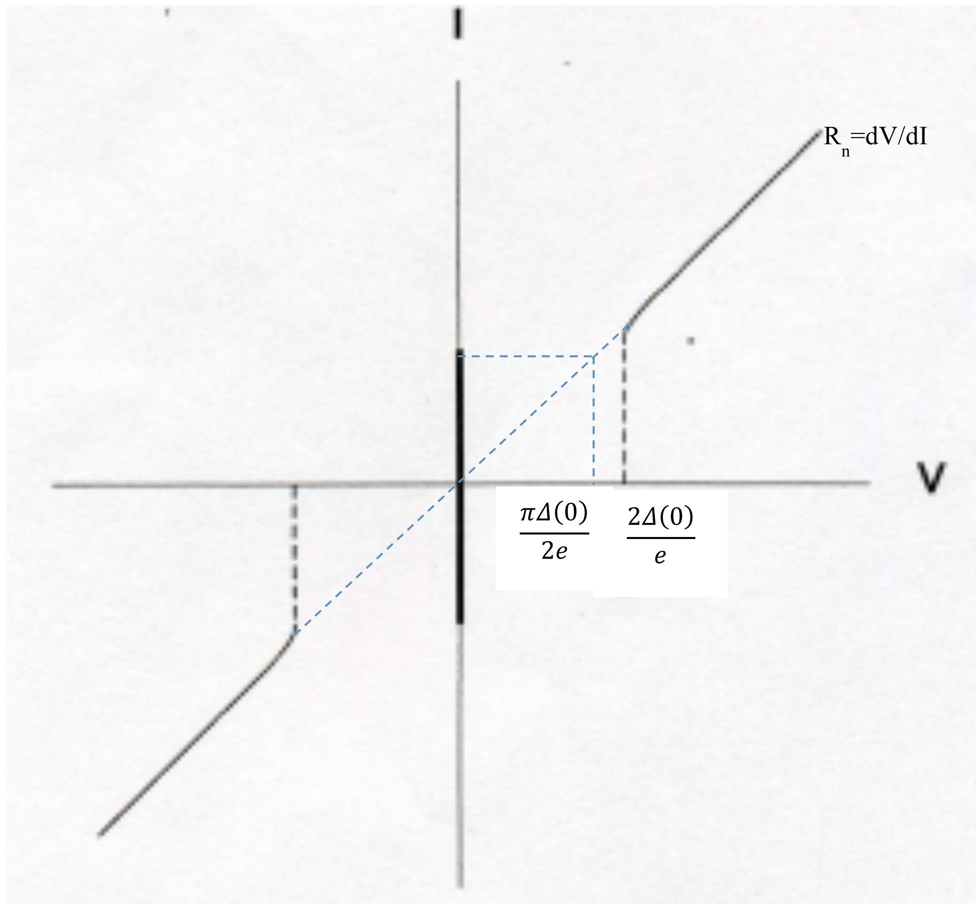


Figure 1.2. I-V characteristic of an ideal SIS junction at T=0 K, reproduced from Supercurrents, Nov. 1988

1.1.2 Magnetic field dependence of critical current

For an ideal square Josephson junction, when there is an external magnetic field applied parallel with one side of the junction, the magnetic field dependence of the critical current will be

$$\mathrm{I}_c(\Phi) = \mathrm{I}_{c0}(\Phi)|\sin\left(\frac{\pi\Phi}{\Phi_0}\right)/\left(\frac{\pi\Phi}{\Phi_0}\right)|$$

where $\Phi = d'LB^0$. Constant Φ_0 is 2.07×10^{-15} V.s. I_{c0} is the critical current without the external magnetic field. $d' = d + 2\lambda$ where d is barrier thickness and λ is the London penetration depth of the material. [5]

L is the size (length of the side) of the junction, the only variable in the case to change the I_c vs B curve. B^0 is the magnetic induction in the insulator region of the junction and the applied magnetic field value is used. A plot of magnetic field dependence of critical current is shown in Figure 1.3.

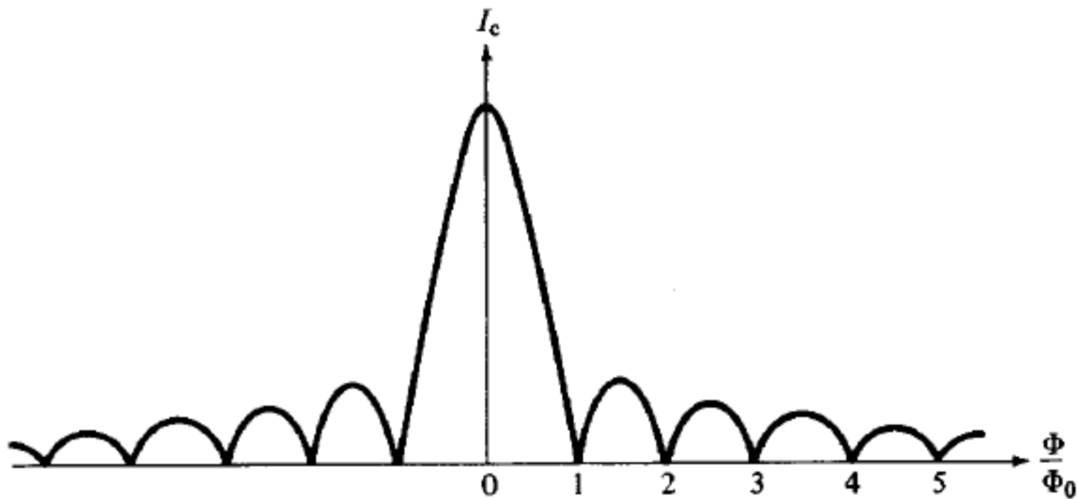


Figure 1.3. Dependence of critical current of Josephson junction on magnetic field when there is magnetic field parallel with one side of the junction, reproduced from [5]

The tunneling current also will induce a magnetic field and affect the junction behavior. This will limit the critical current to a finite value as the size of the junction

increases, and also the maximum point on the field-critical current plot will be offset from 0. People have introduced the Josephson penetration depth, λ_J to characterize the typical length on which an externally-applied magnetic field penetrates into the Josephson junction,

$$\lambda_J = \hbar/2eJ_c\mu_0(2\lambda + d)$$

where J_c is the critical current density, λ is the London penetration depth and d is the thickness of the oxide. The λ_J has a typical order of 5 – 30 μm. If the junction side length w is comparable or smaller than λ_J then the junction could be considered as "small" and the critical current variation along that side can be neglected, and the barrier thickness will be a more important factor affecting the current uniformity. For the field that is parallel with the diagonal of the square junction, the minor peaks in the pattern will be much reduced due to the change in the value of w across the junction.

1.1.3 Proximity effect

Proximity Effect is that a superconductor can induce superconducting properties into a normal metal coupled to it. At the S-N interface, some Cooper pairs can leak into the normal metal while some quasi-particles can diffuse into the superconductor. As a result, the transition temperature of the superconductor could be reduced, and there also could be critical current flow through the normal metal if it is thin enough.

The coherence length of normal metal, the value that represents the exponential decay in density of the Cooper pairs in the normal metal is given in [5]

$$\xi_n = \left(\frac{\hbar D}{2\pi k_B T}\right)^{1/2}$$

where $D = \frac{1}{3}\upsilon_F l_n$ is the diffusion coefficient with the Fermi velocity υ_F and the electron mean free path l_n.

1.2 Application of Josephson Junctions

The special non-linear IV characteristic of Josephson junctions gives potential of various applications. With the effort of the Applied Superconductivity community in the recent decades, Josephson junctions have been adopted in applications such as ultrafast RSFQ (rapid single flux quantum) electronics [6], voltage standards for SI units, SIS receivers and mixers and extremely sensitive SQUID (superconducting quantum interference device) detectors for magnetic field. For example, with the advantages of fast switching speed and low power consumption, the RSFQ logic could be the essential parts for super-computers with clock speed > 50 GHz. Low power dissipation also enables the potential for very dense packing of the electronic units. The superconductive interconnections can be also made to be nearly lossless and form non-dispersive transmission lines, which ensure fast undistorted transmission of signals. Integration of the Josephson relation gives a SFQ (single flux quantum) pulse [5]

$$\int_{t=0}^{\tau} V(t)dt = \Phi_0 = \frac{h}{2e} = 2.07\times10^{-15} V.s$$

The logic is based on manipulating and storing the SFQ pulses. These SFQ pulses can change the state of a gate and the critical current of Josephson junction will be the controlling parameter of the output signal pulse, just like the threshold voltage in the semiconductor CMOS transistors.

1.3 Nb/Al-AlO_x/Nb Josephson junctions

The first Josephson junction was made with Sn and Pb electrodes. [2] Pb has T_c of 7.2K and can be easily grown by thermal evaporation. The superconducting properties of Pb also do not degrade much with impurities in the film. However, due to the quick degradation of Pb in air, Nb was then introduced as another candidate for junction electrodes.

Niobium becomes a superconductor at 9.2K. It has the highest superconducting transition temperature (T_c of 9.2 K) among all the elements at atmosphere pressure. This is very suitable for operating in liquid Helium. Compared with alloys and compound superconductors, Nb is straightforward for material growth and more controllable in uniformity and reproducibility. It is much more stable than other superconducting metals as junction electrodes, with better tensile strength as well. It is non-poisonous, resistant with most acid and alkalis, stable against chemical reagents and relatively easy for machining. Nb also has the largest energy gap ($2\Delta=2.8\sim2.9$ meV at T=0 K) among all the superconducting metals. All these advantages enable Nb as the best candidate for superconductor electronics.

Although there are other alloy or compound superconductors discovered in the later years, such as YBCO-ceramics, MgB_2, Nb-alloys with higher transition temperature, none of them has all the advantages. So Nb is still the best electrode for superconducting electronics operating in liquid Helium.

First all-Nb Josephson junction was made with an insulator layer of natural oxide of Nb. However, the junction characteristics were poor. [7] The insulator was then improved with an RF-oxidation method. [8] Because of high dielectric constant of Nb oxide, the switching speed of the device was be reduced by the junction capacitance. An Al oxide barrier which has lower dielectric constant was first introduced by R. B. Laibowitz in 1972 by thermal oxidation of Al with a 40 to 160 nm thick Al proximity layer [9]. The first Nb/Al-AlO_x/Nb junction with thin Al proximity layer was designed and fabricated by M. Gurvitch et al in 1983 [10], with a new fabrication method using plasma etching. Oxidation condition of Al was studied by R. E. Miller, et al in 1993 [11], and junctions with J_c>100 kA/cm^2 were made with small oxidation exposure (time × pressure). Due to formation of Nb-Al compounds and intermixing, the Al layer requires to be grown at RT, which yields an amorphous AlO_x barrier layer after oxidation.

1.4 Annealing stability of Josephson junctions

We have known that the high temperature synthesis of Nb electrodes could remarkably increase the residual resistivity ratio (RRR) and the crystallinity of Nb thin films.[26, 47] However, the synthesis of the Nb/Al-AlO_x/Nb junction trilayers requires

good substrate cooling and heat sinking during the Al sputtering growth, for smooth and continuous Nb/Al interface, better Nb-Al interface morphology and better junction properties, reportedly because the islanding of Al deposition at elevated temperature and diffusion of Al through Nb grain boundaries. [12] [13][46]

There are still material-related issues and challenges with the fabrication process. The annealing stability of Nb/Al-AlO_x/Nb junction was studied by M. Gurvitch and S. Hasuo's group. [14][33] Junction properties were found to change when exposed to temperatures as low as 100 °C and intermixing starts at the Nb/Al interface through grain boundaries [15] [16], limiting the fabrication conditions. It also may limit the quality and reproducibility [17] [18]. There are factors that may cause problems in the AlO_x barrier: oxygen diffusion from the top electrode surface, reaction between Nb and Al metal, and changes in the barrier itself. Oxygen diffusion could be reduced by annealing in forming gas and coating the top electrode surface with other materials (gold or Nb nitride). For the latter two factors, it is not possible to avoid with using Al. Aluminum also will form compounds with Nb after annealing to 200 °C, according to K. R. Coffey, et al [15]. At low temperatures the compound would be $NbAl_3$ which has T_c of only 0.64K [19], and such low T_c will affect the junction properties.

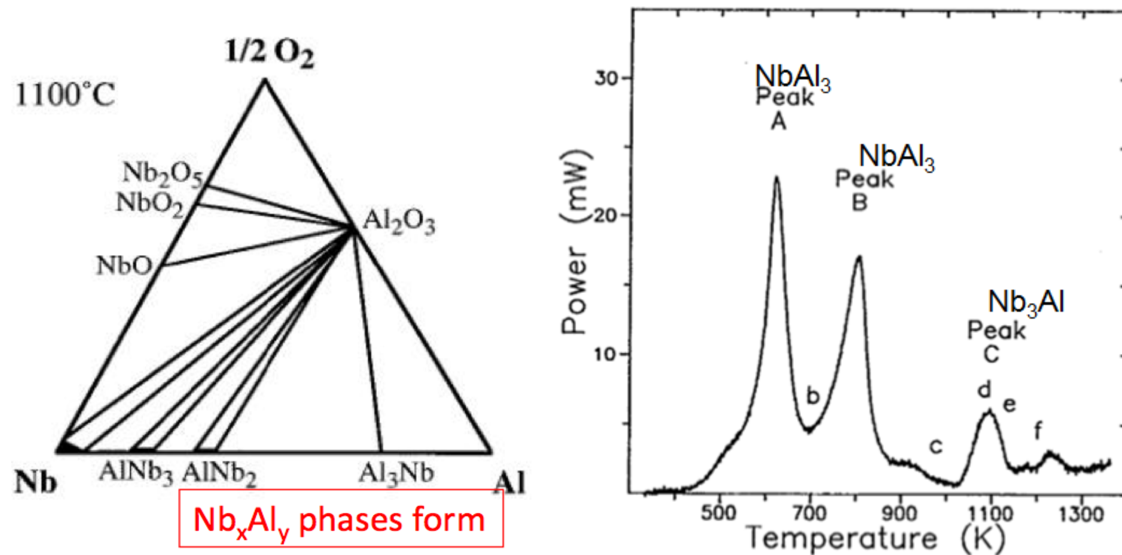


Figure 1.4. (a) Ternary phase diagram of Nb-Al-O at 1100 °C shows Nb_xAl_y compounds forming, reprinted from ref. 20; (b) Scanning calorimetry shows formation of $NbAl_3$ (peak A, B) and Nb_3Al (peak C) compounds after annealing to above ~140 °C, reprinted from ref. 15

On the other hand, in modern IC industry, higher synthesis and back-end process temperatures (up to 300 °C or higher) are usually required for dielectric material deposition and other fabrication processes. Therefore, we are searching for materials that are more compatible than Al with elevated synthesis temperature and fabrication processes.

1.5 Requirements of thermally stable Josephson junctions

To solve the annealing problem of AlO_x, we want to develop a Josephson junction material system that can be stable in growth and post-processing up to 350 °C which is desired for dielectric deposition in IC industry.

To find the best barrier material that suit our purpose, it should

1) Not intermix with Nb at annealing temperatures;
2) Form flat surface with Nb;
3) Wet Nb and preferably be compatible with high-temperature Nb growth for better Nb quality.

After reviewing the common dielectrics used in IC industry, we choose the refractory metal Hf, Zr and Ti have similar properties. Hf oxide was first introduced as barrier material by S. Morohashi, et al in 1992 for its better annealing stability. [21] The good aspects of these refractory metals are summarized below.

1) They do not form compounds that depress the T_c of Nb;

NbHf, NbZr, NbTi alloys a show maximum in T_c vs atom concentration which means even if they have intermixed, the T_c would not drop very much;

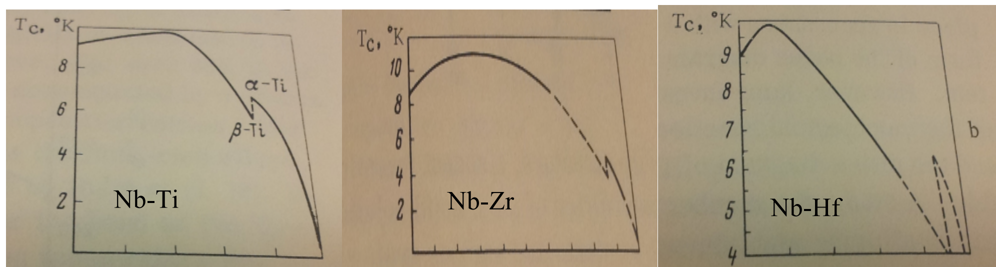


Figure 1.5. Concentration dependence of T_c of Nb-Ti, Nb-Zr and Nb-Hf binary alloys (atomic concentration, from left Nb 100% to right Nb 0%), reprinted from ref. 22

2) Their oxides have smaller band gaps than Al_2O_3

This may allow lower barrier height and thus thicker barriers. The drawbacks of these oxides are their higher dielectric constants and thus higher junction capacity. But their lower band gap comparing to Al_2O_3 may allow lower barrier height and a thicker barrier with the similar critical current density and junction capacity.

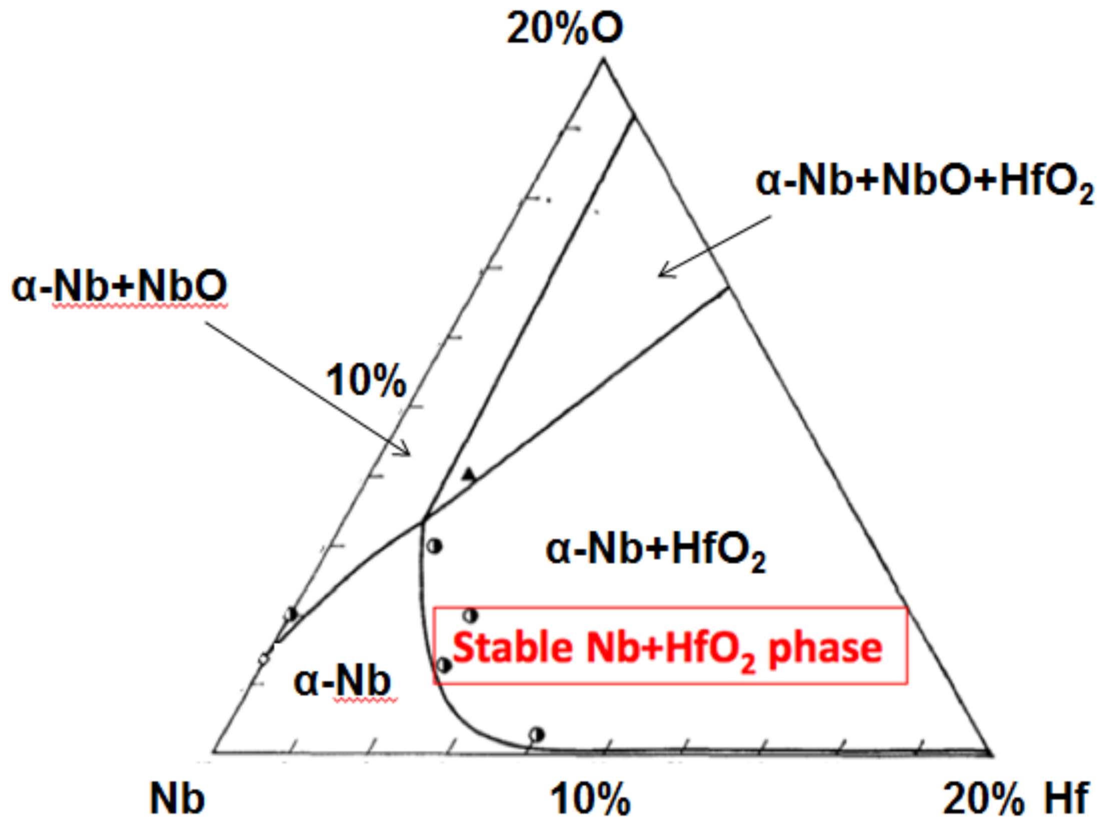


Figure 1.6. Ternary phase diagram of Nb-Hf-O at 1000 °C [23]

Thermodynamics can be used as the first step in the identification of a suitable barrier metal for Josephson junctions. From the phase diagram in Figure 1.6, we know that Nb is stable against HfO_2, and no Nb-Hf compound exists, and NbHf alloys show

maximum in T_c vs atom concentration. However, too much oxidation will oxidize both the Hf and the bottom Nb electrode and degrade the interface, too.

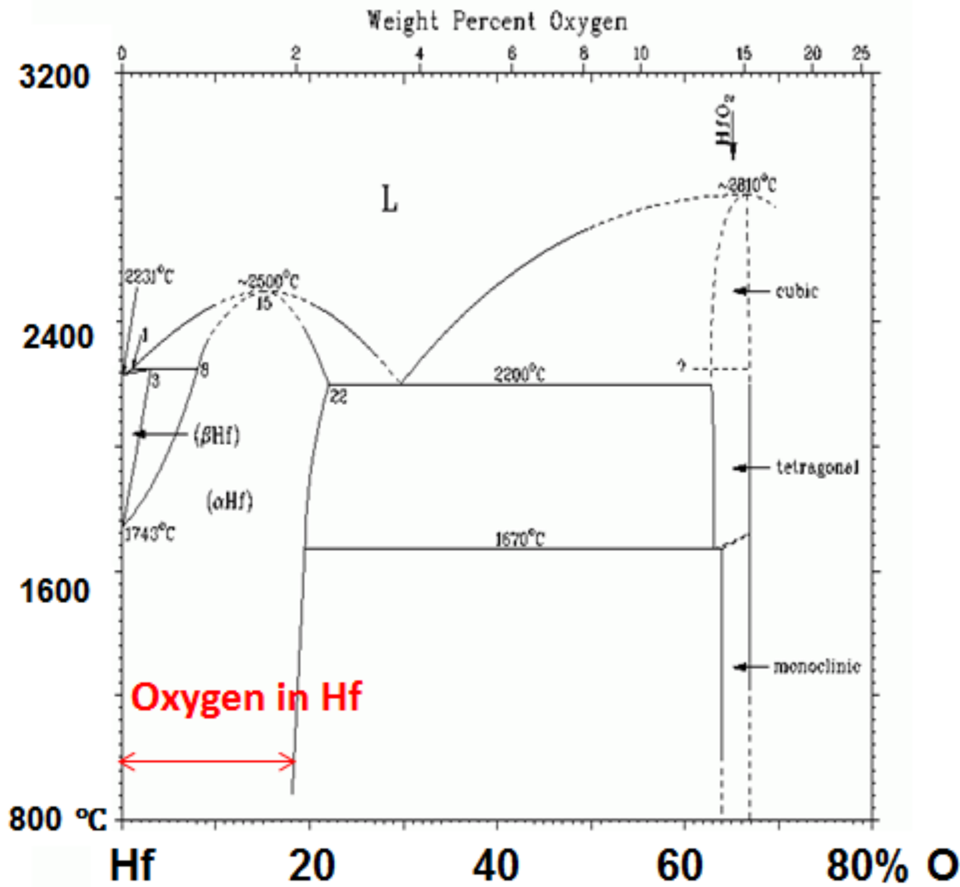


Figure 1.7. Hf-O binary phase diagram indicates oxygen solubility in Hf >10% at RT, reprinted from ref. 24

However, thermodynamics also predict that excess Hf metal will getter oxygen from HfO_2 barrier, as shown in the binary phase diagram in Figure 1.7. Thus, to achieve a thermally stable HfO_2 junction barrier, excess Hf metal should be avoided. For example, ALD method could be used to deposit pure HfO_2 barriers without any excess Hf metal.

1.6. Properties of HfO_x and ideal junction structure

Hafnium is a highly reactive metal. The reaction with air at room temperature is self-limited by the adherent, highly impervious oxide film formed. This film provides oxidation stability at room temperature and resistance to corrosion by aqueous solutions of mineral acids, salts, or caustics. Thicker oxide films are formed at higher temperature.

Two oxides of hafnium, hafnium monoxide, HfO and HfO_2, are known to exist but only the dioxide is stable under ordinary conditions. Gaseous hafnium monoxide can be present at >2000 °C, especially when the partial pressure of oxygen is low. Hafnium monoxide is probably the compound form in which oxygen is evolved when hafnium metal is melted in an electron-beam melting furnace. HfO (gas) is the species observed by mass spectrometry when hafnium dioxide vaporizes. [50]

At lower temperatures, the oxidation following the linear oxidation comprises simultaneous oxide formation and oxygen dissolution in the metal. The solid-solubility of oxygen in the Hf is almost independent of temperature and decreases from 22% (at.) at 2000 °C to 20% (at.) 700°C. As oxygen is dissolved in the Hf metal, oxygen diffusion gradually becomes the rate-controlling step and the rate of reaction decreases with time. Simultaneously, the first traces of HfO_2 are formed on the surface. [51]

During annealing in oxygen gas, the oxygen can diffuse into the HfO_2 film. Atomic oxygen diffusion via oxygen lattice exchange is the predominant diffusion mechanism in Hf oxide. [52]

There is no detailed report on the electrical properties of Hf suboxide. HfO_x (x=1.7) is an insulator and can be used in RRAM (Resistive Random-access memory) as reported recently. [53]

Oxygen in HfO_2 can also be reduced to suboxide when annealing with noble metal at elevated temperature with the presence of hydroxyl groups. [54]

To summarize, during the oxidation process, Hf suboxide can be formed by oxygen diffusion within the Hf layer by diffusion process. The layer is insulator when x is close to 2. There is no detailed report on the electrical properties of Hf suboxide, but at cryogenic temperature, the oxide should be frozen out and become insulating.

The ideal structure of a thermally stable Josephson junction will consist of Nb electrodes and pure Hf oxide barrier, without excess Hf metal. If oxidation is too much, then Nb oxidation will occur, degrading the barrier interface. If oxidation is insufficient, then Hf oxide may not be complete and oxygen diffusion to form a sub-oxide HfO_x layer will occur.

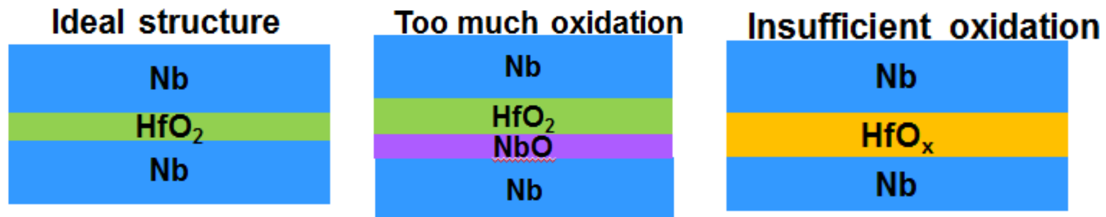


Figure 1.8. Schematics of Nb Josephson junction with HfO_2 as barrier

1.7 Summary

It would be desirable to produce thermally stable junctions that can withstand elevated temperature fabrication and processing steps. Specifically, in the modern industrial microfabrication processes, higher temperatures are used in the synthesis and back-end process (up to 300 °C or higher) for dielectric material deposition and other fabrication processes. Thermal stability of Josephson junctions will clearly be an advantage when scaling to smaller dimensions and higher device counts.

The Nb-Hf-O ternary phase diagram predicts that Nb is thermodynamically stable against HfO_2 below 1000°C. A Nb/HfO_2/Nb junction could be thermally stable.

1.8 Organization of the thesis

In chapter 2, an overview of the thin film growth and analysis techniques used in the research is given. Characterization results for the sample's composition, topology and structural properties are summarized. The I-V characteristic measurement setup is also introduced. The purpose of systematic study with each technique is outlined.

In chapter 3, the process of fabricating Josephson junctions is detailed, including both the shadow mask method and micro-fabrication method. Various tools used during the junction fabrication process are discussed. The preparation process and measurement pre-cautions are discussed.

In chapter 4, thin film characterization results are reported. Growth conditions of the Nb films were optimized for Josephson junction electrodes. Single layer Nb films

were characterized for electrical, topological and structural properties. A bilayer study was also performed to investigate the stability of the Nb-Hf interface. Auger spectroscopy and TEM methods were used to characterize the oxygen diffusion after the annealing process.

In chapter 5, Josephson junction measurement results are summarized. An annealing study performed on each device is also outlined. Different approaches to improve junction thermal stability were attempted and discussed. The proximity effect of the Hf layer was also estimated from experimental data.

In chapter 6, the work is concluded and plans are made for future studies for thin film growth and material characterization.

Chapter 2

THIN FILM GROWTH TECHNIQUES AND ANALYSIS TOOLS

Several characterization techniques were employed to find the electrical, structural and topological properties of the Nb films, as well as the Nb-Hf bilayers and trilayer junction structures. The analytical tools that have been used include: Rutherford backscattering spectroscopy (RBS), atomic force microscopy (AFM), Transmission Electron Microscopy (TEM) and Auger Electron Spectroscopy (AES). Electrical measurements include dipping measurement with spring-loaded contacts and 4-point junction I-V measurement. In this chapter, the scientific background of the growth and analysis techniques is discussed.

2.1 Requirements for thin films in Josephson junction applications

It is desirable to have high-quality in-situ Nb films with high transition temperature (>9 K) for application as Josephson junction electrodes. As electrode layer of Josephson junctions, the superconductive properties of Nb thin film depend on the purity very strongly. High-quality Nb electrode with less than 0.1% impurities should have T_c of 9.2 to 9.3 K and a gap voltage of ~ 1.4 mV at 4.2 K.

Due to the coherence length of around 80 nm, Nb electrodes need to be thick enough to have their full superconductive properties, so they should be at least 80-100 nm thick. A good Nb film with only 50 nm thickness showed an energy gap of 1.3 meV instead of 1.4 meV in a Nb/Al-AlO_x/Nb junction that our group has measured. At the same time, for a Nb film as an electrode, we want the film to be as smooth as possible at

such thickness, so that the electrode can be fully covered with a few Hf monolayers. An surface RMS (root mean square) roughness of the electrode should be no more than 1 nm and as low as possible. However, as the film grows thicker, the surface roughness of the film will also increase, which is not desirable for uniform coverage of the barrier metal. So for practical junctions, the Nb electrode thickness is usually kept at 100 – 200 nm.

Oxygen is the most common impurity in Nb films, due to its easy oxidation from oxygen outgassing and residual water vapor in the growth chamber. So to obtain Nb films with the best quality, high vacuum better than 1×10^{-7} Torr and a higher deposition rate is desired for less oxygen impurities. 1% of oxygen impurity in the bulk of the film will increase the scattering and reduce the Tc by ~1 K. [22] So a good vacuum chamber with low base pressure (1×10^{-7} or lower), low outgassing and rate-of-rise will be required for thin film Josephson junction growth.

Also for a Hf thin film, we want the film to be as smooth as possible, and to wet the Nb base electrode well, preferably at elevated growth temperatures. The Hf layer should not show intermixing with Nb at high temperatures and should form flat interfaces.

To summarize, an ideal Nb electrode for Josephson junction would be 100 – 200nm thick, have T_c of 9.2 K, and AFM surface RMS roughness of ~0.5 nm. The Hf layer should wet Nb at elevated temperatures, should form a flat surface without islanding and should not intermix with the Nb electrode.

2.2 Overview of sputtering

Due to its high melting point at over 2200 °C, a Nb film is usually deposited with the DC sputtering method rather than with thermal evaporation. Hf is also deposited by sputtering.

DC magnetron sputtering is a common thin film deposition method with commercially available equipment. It is achieved by bombarding the source target (which needs to be conductive for DC sputtering) with energetic Ar ions (can also be other noble gas such as Ne) in a vacuum chamber. Atom clusters at the surface of the target are knocked off and dispersed in the vacuum and deposit on the substrate and chamber walls. Ions are generated by applying a few hundred volts between the ground shield and the target which are separated by 1-2 mm at a few mTorr of Ar pressure. A plasma can be seen when the gun is operating, and power is consumed by the ionized Ar current and voltage applied. Rare earth magnets are often used in the sputter guns to create circular field that confine the ions to hit only within the surface of the target. The use of the magnet can greatly improve the growth rate at the same power, and decrease the Ar pressure that is required to maintain the plasma, which will reduce the impurities in the deposited film. Due to the power dissipated when ions bombard the target surface, the gun body can become quite hot, thus cooling is strictly required when operating the sputter gun. If not, the magnet can become hot quickly, exceed its curie temperature, stop forming its magnetic field and thus damage the gun.

A shutter is installed on each sputter gun, so that sputter time could be exactly controlled by opening and closing the shutter. A pre-sputter is also required for each

sputtering deposition, because the sputter target will get some surface oxide or contamination when not used. Pre-sputtering with the shutter closed can clean the target in a few minutes. When a target is freshly installed, a long pre-sputtering (also called target "bake-in") is often needed to remove the thicker surface oxide.

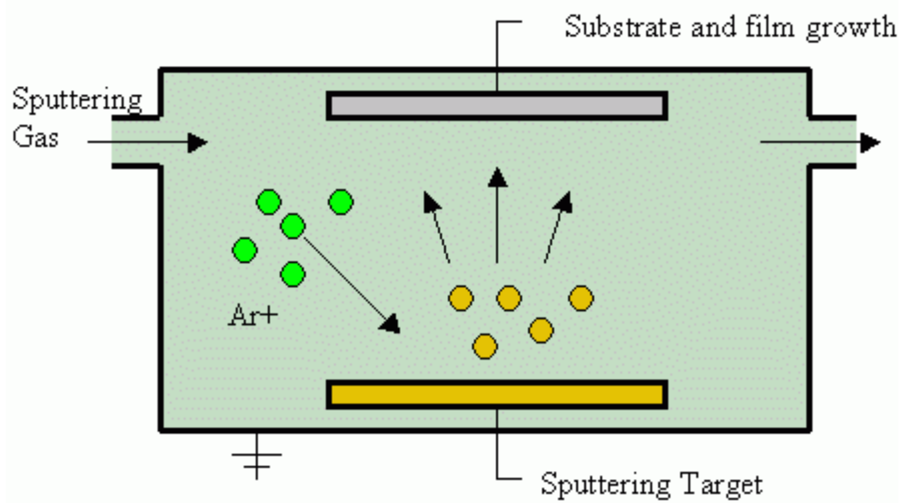


Figure 2.1. Schematics of sputtering, reprinted from wikipedia.org

2.3 Overview of Atomic Layer Deposition (ALD)

To get rid of excess Hf metal, we attempted to use ALD method to synthesize the Hf oxide. Atomic Layer Deposition is a thin film deposition technique that is based on a gas phase chemical process. The reaction in the ALD uses two precursors that react with the surface of the substrate and they are kept separated during the deposition. The reaction is self-limiting. By flashing and keeping the precursors separate throughout the coating process, atomic layer control of film growth can be obtained as fine as ~1 Å per cycle (one monolayer per cycle).

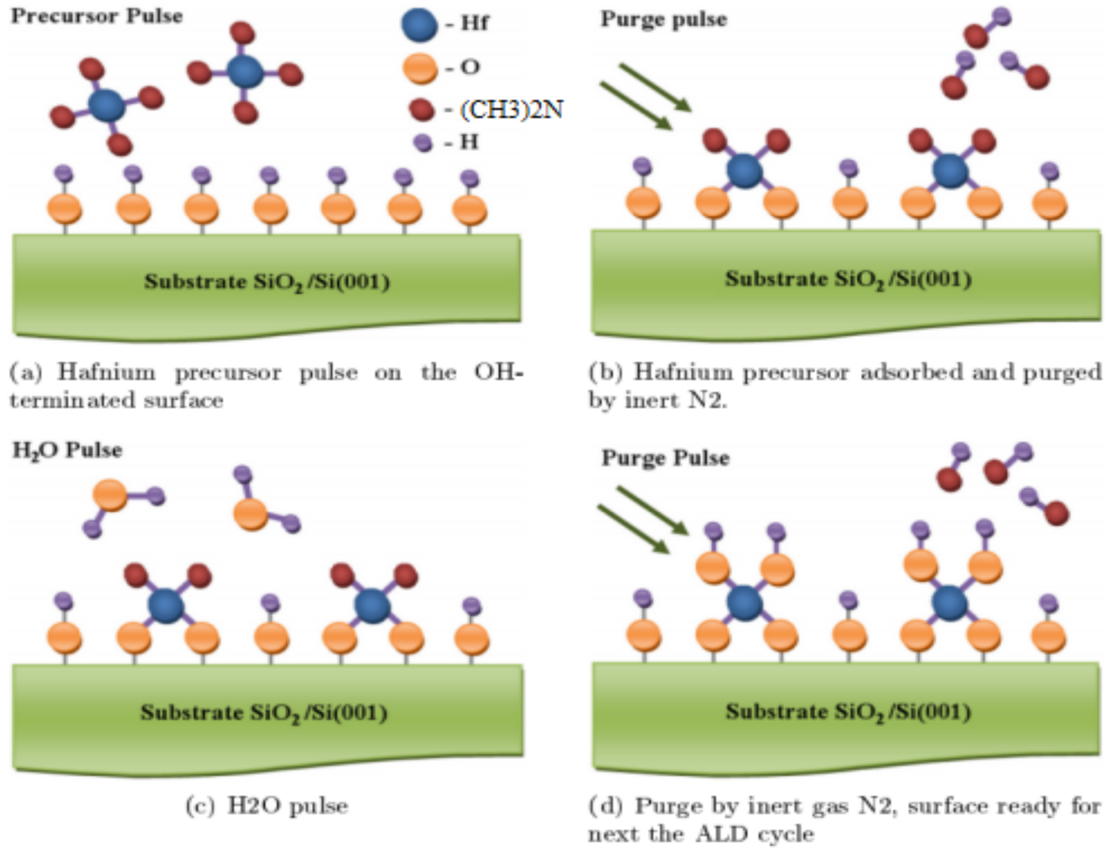


Figure 2.2. ALD growth mechanism of Hf oxide, reprinted from ref. 25

The Cambridge NanoTech Savannah 100 Atomic Layer Deposition System at CSSER was used for HfO_2 deposition. Tetrakis(dimethylamido)hafnium(IV) (TDMA-Hf) was used as the precursor for Hf, which can react with water vapor on substrate surface and form one layer of Hf oxide. The process consists of 15 milliseconds of flashing time from TDMA-Hf and water source alternately followed with 15 seconds of pumping and nitrogen gas purging.

2.4 Experimental Setup

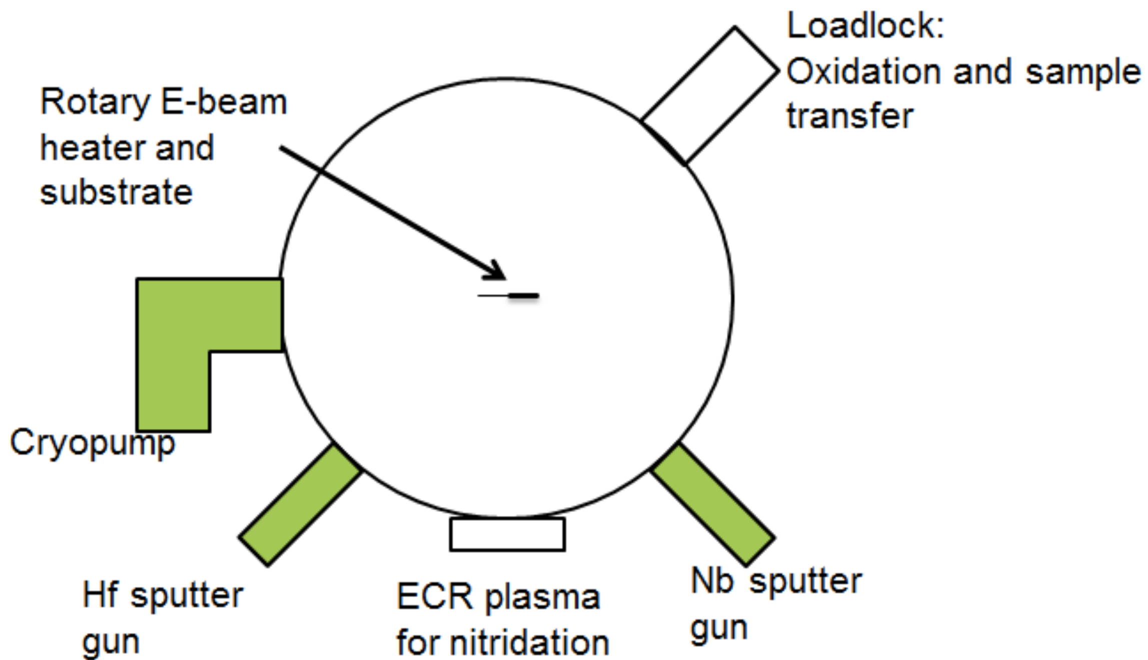


Figure 2.3. Vacuum system for thin film synthesis at ASU

Metals including Nb, Hf and Al were made with DC (direct current) sputtering on 1 cm^2 substrates in a vacuum chamber, shown in Figure 2.3. A 99.95% pure Nb target (1.5 inch diameter for an AJA sputter gun) and 99.9% pure Hf target (1 inch diameter for a Lesker Torus sputter gun) were used. R-plane (1-102) sapphire was used for achieving high-quality Nb epitaxy[26], and C-plane (0001) sapphire and Silicon substrates were also used. The unbaked base pressure of the cryopumped chamber (CTI Model Cryo-8F) is $<5\times10^{-8}$ Torr. The optimum properties of the film were achieved by using an Ar pressure of 6×10^{-3} Torr (measured by the capacitance manometer, 3×10^{-3} Torr by the

convectron gauge which is less accurate) and 230 sccm Argon flow rate for this system. The distance between the substrate and the target was maintained at 6 inch. The sputter deposition rate of Nb, with 180 Watt powered by Advance Energy MDX 500 DC power supply is kept at 0.25 nm/second and Hf (with 50 Watt power) at 0.2 nm/second, calibrated by RBS. The thicknesses of the bottom Nb and top Nb electrodes for the junction are both 100 nm. The substrate temperature was measured with a pyrometer. During a bilayer or a trilayer growth that contains both Nb and Hf, the time duration between the Nb and Hf deposition was kept as short as possible (less than 1 minute) to avoid contamination at the interface, mainly surface oxidation of the Nb film.

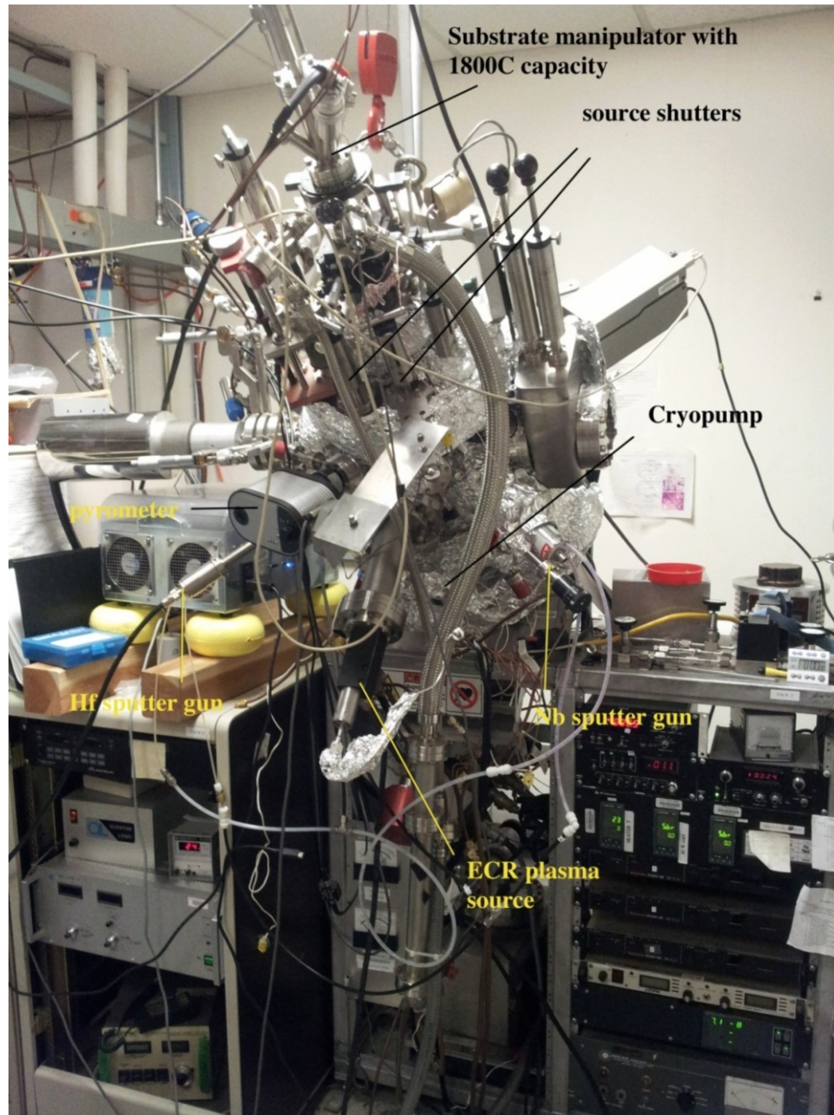


Figure 2.4. Picture of vacuum chamber for thin film growth at ASU

A 1 cm x 1cm square substrate was mounted on a home-made transferrable puck that can be rotating-locked onto the three teeth of electron-beam heater. The sample was clamped with three Ta screws and has good thermal contact with the back of the puck. A load-lock arm can transfer the puck into and out of the chamber without breaking vacuum.

The substrate could be heated by an e-beam heater (by Thermionics) that is capable of heating up to 1500 °C and the substrate temperature was monitored by a pyrometer. The pyrometer can read temperatures above 450 °C and the lower temperatures were calibrated by Brett Strawbridge. [27]

To start heating the substrate, start by ramping up the AC current source to the filament. From 0 to 3A, wait 2-3 minutes every Ampere to reduce thermal shock to the tungsten. An AC current of 9 A with 50mA of emission current can heat the substrate to 500 °C. During metal sputtering process, due to the Ar pressure (~3 mTorr) in the chamber, a higher emission current will be induced with the same setting, and the knob value should be reduced to achieve the same emission current.

The Hf layer was also grown at 500 °C. The period between the growth of the bottom Nb and Hf layer were kept as short as possible to reduce the possibility of oxidation of Nb surface by the residual water vapor and oxygen in the chamber. This period takes about 30 seconds, including changing the direction of the heater, starting the Hf gun and stopping the Nb gun).

2.5 Overview of material characterization tools

The films made by vacuum growth mentioned above were characterized for their compositional, topology and structural properties. The characterization methods used for material studies will be discussed in this section.

2.5.1 Rutherford Backscattering Spectrometry (RBS)

RBS uses a high-energy α-particle beam to characterize the layer composition of thin films. This non-destructive method can detect the amount of different elements in films from the surface down to about 2 microns. The α-particles impinge through the sample surface, and are bounced backwards by the nuclei of the atoms in the film layers. α-particles scattered from different nuclei will have a specific backscattered energy and can be collected by a detector. A software RUMP is used to simulate the elemental information and compared with the actual spectrum by its area concentration. Nuclear resonant scattering $^{16}O(\alpha, \alpha)^{16}O$ was also used for detecting oxygen concentration in the films. RBS channeling can be used to determine the epitaxy of the thin film by comparing the number of reflected particles from a normal crystal structure direction and a random direction.

2.5.2 Atomic Force Microscopy (AFM)

AFM is a technique to map the surface topography of a thin film. A micron size surface area of sample is scanned line by line by a Si nitride cantilever. The cantilever is deflected by the Van Der Waals force when it is a few angstroms from the sample surface atoms. The deflecting movement of the cantilever is measured by a laser beam reflected from the cantilever and can be viewed on the monitor. The resolution can be as good as a few angstroms. Digital Instruments Nanoscope III AFM at LE-CSSS was used to characterize the surface roughness of Nb and trilayer films.

2.5.3 Transmission Electron Microscopy (TEM)

TEM obtains structural information using an electron beam that penetrates the very thin specimen. Diffraction patterns can be observed by elastic scattering between transmit electrons and ion cores. The microstructure and morphology of sample features will be imaged by the inelastic interactions between the electron beam and matrix electrons at defects/grain boundaries. The Nb thin films and junction trilayers were prepared with FIB or ion milling methods into thin specimens and studied with JEOL ARM200F microscope at LE-CSSS. The microstructures and interface roughness were studied with atomic resolution images, and XPS/EELS were used to detect the distribution of oxygen in the barrier.

2.5.4 Auger Electron Spectroscopy (AES)

In the AES system, an electron beam with 3-5 keV is used in UHV to induce Auger electrons from atoms near the sample surface. The emitted Auger electrons only come from the surface and near surface region due to the small escape depth (mean free path), and they are collected by an electron energy detector. By using Ar ion beam sputtering and repeated surface spectroscopy, the depth profile of the sample can also be studied. We used an AES system from LE-CSSS to study the oxygen diffusion in Hf barrier before and after thermal annealing.

2.5.5 X-ray Diffraction (XRD)

X-ray diffraction is a technique that studies crystal structures and atomic spacing based on Bragg's Law ($n\lambda=2d\sin\theta$, λ is the wave length of the X-ray and θ is the incident angle) which shows constructive interference of monochromatic X-rays and a crystalline

sample. In this study, Nb films were studied with XRD for its crystal orientation with theta-2theta scans and crystallinity with rocking curve scans.

2.5.6 Dipping measurements

For superconductive thin films, such as Nb film, a dipping measurement is a way to test its superconducting transition temperature. The measurement was performed with a dipping probe which was inserted into a liquid Helium dewar. The thin film is installed to the bottom part of the probe with four spring loaded contacts, where the outer two contacts source current I and the inner two contacts are used for measuring the voltage V across the two contacts. The sheet resistance of the film (in Ohm) could be thus calculated by

$$R_s = V/I$$

And given the thickness d (in cm) of the film measured by RBS, the resistivity ρ (in μΩ.cm) of the Nb film could be calculated as (shown in D. K. Schroder's Semiconductor Material and Device Characterization)

$$\rho = 4.532 R_s \times 10^6 \times d$$

For Nb, resistivity is usually in the range of 15-25 μΩ.cm at room temperature and <5 μΩ.cm at about 10 K.

Residual resistivity ratio (RRR) is a good judgment of the Nb film quality, which could be measured easily by the dipping measurement easily. It is defined as the ratio of

sheet resistance (or resistivity) of a Nb film at 300 K and at 10 K. A high RRR value indicates fewer impurities in the film. A good Nb film sputtered at RT will have RRR of 3 to 5. Higher growth temperature will largely improve the RRR, as the epitaxy of the film is improved.

2.6 I-V measurement setup of Josephson junctions

Before measurement, the samples were stored in anti-static boxes and transferred into the shielded room for electrical measurement. The wire-bonded chip carrier with the sample was plugged into a home-made dipping probe and inserted in a Liquid Helium dewar. (Wire-bonding process will be mentioned in the next chapter.) The measurement was performed inside a shielded room (Faraday cage) to minimize the noise from the external environment. To avoid damage due to electrostatic discharge, the relative humidity in the shielded room was maintained at around 40% during the experiments and antistatic floor mats were placed under all measurement equipment. Grounding wrist straps were used while people handling the samples. BNC cables were connected through the wall to the measurement system outside the shielded room and RF filters were installed on the feed-through of the cables. The measurement system outside the shielded room consists of a Keithley 220 current source, a HP 34401A multimeter as a voltage meter and a PC recording the data with a C++ program written by Lei Yu. [28] Each measurement plot consists of 400 points of current data points that are equally spaced. The IV characteristics are generated by Excel, and the conductance (G) is calculated by fitting the slope of the closest five data points using the LINEST function.

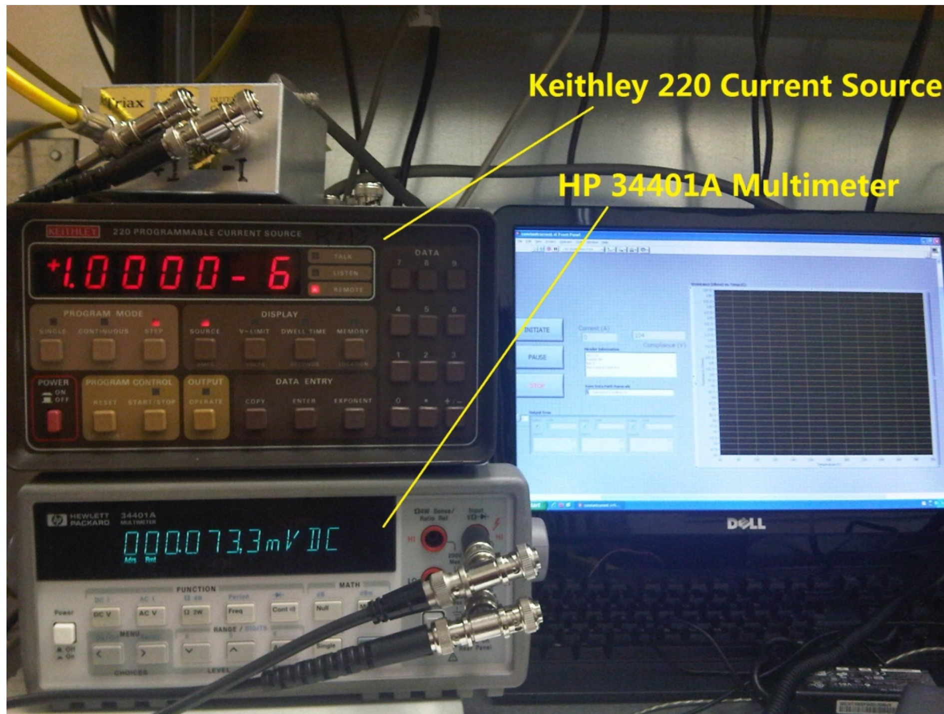


Figure 2.5. Picture of electronics in I-V measurement system

A commercially available measurement system, Mr. Squid box (provided by Star Cryoelectronics) was also used for junctions measurements. By using Mr. Squid, the junction measurement could be done in the Shielded room entirely with less noise. However, the current source of Mr. Squid is capable of measuring up to only 400 µA.

Figure 2.6. Picture of front panel of Mr. Squid box

A home-made copper coil is placed outside the dewar to generate magnetic field and modulate the critical current during measurement. Maximum field is about 40 Gauss powered by a DC power supply kept outside the shielded room. During measurement, the AC power supply into the shield room is stopped to minimize measurement noise, except for the DC power supply for magnet coil.

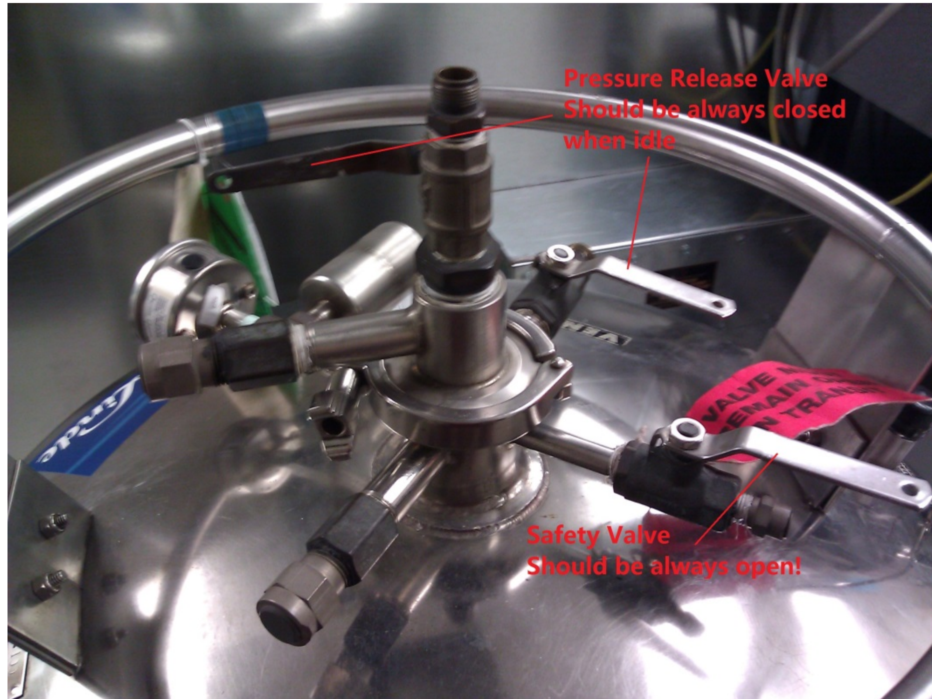


Figure 2.7. The proper way of closing a liquid Helium dewar

As an important safety notice, the Helium dewar should be always used properly with caution, or there will be chance of dewar freezing and explosion. The bottom line is to allow as little air as possible to flow into the dewar. When not being used, the safety valve should always kept open, and the gas releasing valves should both be kept closed.

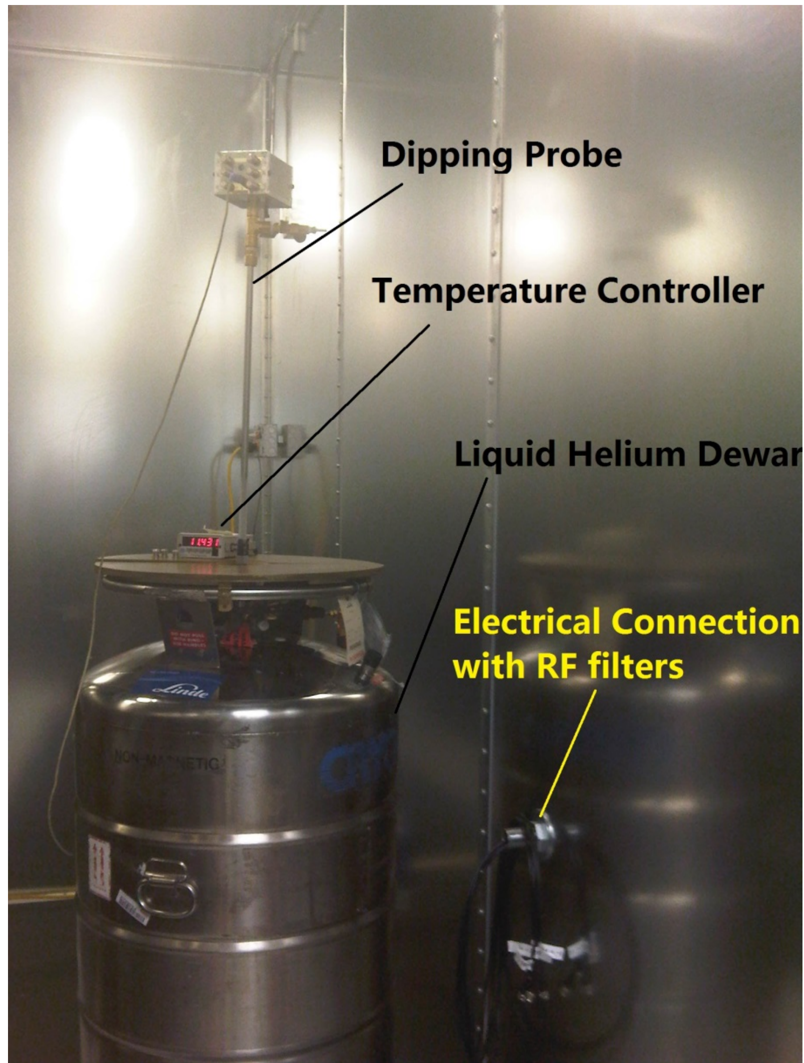


Figure 2.8. Helium Dewar and dipping probe inside the shielded room during junction measurement

Chapter 3

FABRICATION PROCESS OF JOSEPHSON JUNCTIONS

3.1 Overview of fabrication processes

Why do we need to fabricate a junction? First of all, in order to make four-terminal measurement, the junction should have at least two electrodes for electrical contacts. Secondly, the junction area needs to be small enough so that

1) there is less chance that the junction catches a short due to dust or crack
2) junction resistance should be high enough so the I-V measurement doesn't exceed our equipment's limit (100 mA for current source).

According to Miller et al. [11], the critical current of typical Nb/AlO_x/Nb junction can be as high as 1000 A/cm^2 at 4.2 K.

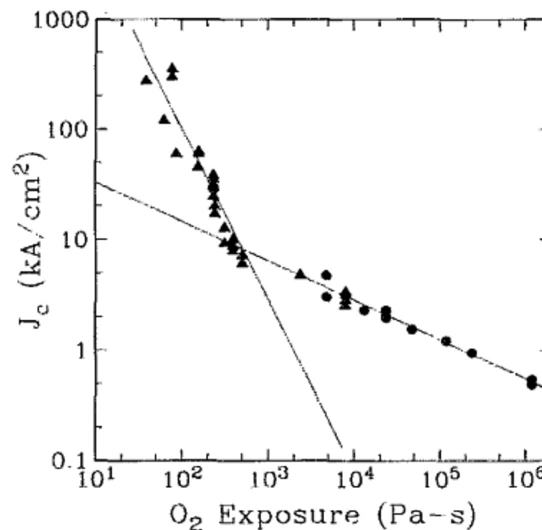


Figure 3.1. Dependence of J_c on oxygen exposure for oxidation times of 10 min (solid triangles) and 30 min (solid circles), reprinted from ref. 11

Assuming we have a 100 A/cm^2 junction, the size of the junction should be at most 0.001 cm^2, or a square size junction with 300 micron on the side. In another word, we want the junction to at least reach its gap voltage of 3 mV at 100 mA, or to have at least 0.03 Ohm of normal resistance. This usually requires the junction size to be less than 500 micron. So the junctions will need to be shaped from thin films into small area of micron-size, which we called "fabrication".

There were two ways of making Josephson junctions during the work of this thesis, shadow mask junctions and micro-fabrication junctions. There are also many forms of weak-link other than a thin barrier layer. A narrow bridge could also form a Josephson junction. But for mass production and circuit integration, a fabricated multilayer structure is the only fabrication method so far. Since the first junction made in 1963, the junction fabrication process has been developed from cross-type junction to a multilayer process after several generation's work. After Nb was chosen as the electrode material, Selective Nb Anodization Process (SNAP) for fabricating with Nb/amorphous-Si/Nb Josephson junctions was first introduced by H. Kroger, et al. in 1981. [29] A Nb surface could be anodized to form a dense, uniform and stable insulating layer of Nb_2O_5, which was used for junction area definition. Selective Nb Etching Process (SNEP) was then adopted by M. Gurvitch, et al. in 1982. [10] In this process, dry etching was used to define the junction area and anodization was also used to form an insulating layer. The anodization process is self-aligned, easy and convenient. However, only one insulation layer will increase the chance of failing of the device. Additional deposition of dielectrics

such as SiO_2 was also used for insulating layers, combined with anodization layers. Method of lift-off of the dielectric was introduced by M. Yuda in 1987. [12] In our fabrication process, we combined both the Nb anodization and dielectric lift-off methods.

A clean Nb film will have a critical current density of 1×10^6 to 1×10^7 A/cm^2 at 4.2 K. Given the wiring layer width of 5 micron and thickness of 100 nm, the Nb wiring layer can carry 5-50 mA of critical current.

3.2 Shadow mask method

The shadow mask method can rather be called a growth method, than a fabrication method, but using shadow mask method is relatively fast, compared with the complete micro-fabrication method. The shadow masks are used during deposition to define the region of the junctions, and are usually made of stainless steel or tantalum. The ASU physics instrument shop can make a slit in Ta sheet that is as thin as 250 micron minimum width.

A shadow mask with a 250 micron slit is used to cover the substrate before growth, to form a strip of the bottom junction electrode. The mask should be as close to the substrate surface as possible to avoid shadowing effect. If the bottom electrode's oxide will be used as the barrier, such as Pb or Al oxides, the wafer should be exposed to air for a certain period. A top electrode shadow mask with a few parallel slits will be installed at normal angle to the bottom electrode for the top electrode deposition. The replacement of masks could be done in-situ with tools in the chamber, but in our group it has been done ex-situ.

If the barrier oxide is not the oxide of bottom electrode, such as Nb-HfO_x or Nb-AlO_x (Nb as bottom electrode and Al/Hf oxide as barrier), then the bottom strip's edge needs to be covered with certain insulators (for example: SiO_2), to prevent the top electrode shorting through the edge of the bottom electrode. In this case, after the bottom electrode deposition, an additional step of depositing an insulator for edge-covering will be needed with another wire-shaped mask. The pros and cons of shadow-mask junctions are listed below.

Pros:

Convenient and fast. Shadow mask cross-junctions are available for measurement after growth.

Cons:

1) Relatively large junction size. It will be difficult to minimize the junction size to less than 50 micron, due to the unavoidable shadow effect.
2) If the mask replacement has to be done ex-situ, then the oxidation of the sample surface will not be controlled. The humidity in air will affect the oxidation, too.
3) When installing/removing shadow masks for growth, the thin film may get scratched or damaged physically by the mask if not done properly.

3.3 Micro-fabrication method

The complete fabrication of junction was done at ASU. It includes several steps: photolithography patterning, reactive ion etching, anodization, dielectric and wiring layer deposition, ion milling and wire-bonding. These steps are detailed below.

3.3.1 Photolithography

Photolithography was done in our lab for defining micron-size patterns on to films followed by reactive ion etching and thus junction lines were made. The pattern was transferred from a soda lime mask with opaque Chromium pattern to the films to be processed. For Josephson junction measurements, a 2-step photolithography was developed and used for our group.

To perform the photolithography, after acetone surface cleaning and 90 °C heating, Hexamethyl disilazane (HMDS) is spin coated on the sample to remove the water vapor. Then a 3 micron thick layer of AZ 4330 photoresist is spin coated at 5000 RPM (ramping up from 2000 to 5000 in a few seconds) on the surface. The sample is subsequently dried on hot plate at 90 °C for 1.5 minutes and transferred to a Quintel Q2001 CT mask aligner, where ultraviolet light is used to expose the photoresist. The exposure time is determined previously because the light intensity in the mercury bulb keeps decreasing over time. The sample is then rinsed in AZ 300 MIF developer to remove the photoresist on the exposed area which takes around 70-90 seconds.

3.3.2 Reactive Ion Etching (RIE)

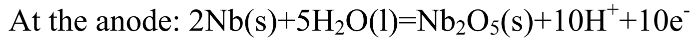
Reactive-ion etching (RIE) is an etching technology used in microfabrication. Chemically reactive plasma is used to remove material deposited on wafers. A typical parallel plate RIE system consists of a cylindrical vacuum chamber, with a wafer platter situated in the bottom portion of the chamber. The wafer platter is electrically isolated from the rest of the chamber. A plasma is initiated in the system by applying a strong RF

(radio frequency) electromagnetic field to the wafer platter. This oscillating electric field ionizes the gas molecules by stripping them of electrons, creating a plasma. The ionized etchant gas reacts with the wafer material and forms volatile chemical which are pumped out by a vacuum pump. In our lab, CF_4 gas was used in the etcher (PlasmaLab µP, Oxford Instruments) for generating fluorine ion plasma to remove Nb layers by forming volatile NbF_3. With 20 sccm CF_4 gas, 50 mTorr, 75 W RF power the etch rate for a clean Nb film is about 10 nm / minute initially and gradually increases to 15-20 nm/minute after extensive etching. The photoresist will also get slowly etched by the plasma so the etching time is limited. For AZ 4330 photoresist, the etch time could be as long as 90 minutes with < 100 W etching power. Ar gas is also used to physically etch other barrier material that is not easily etched by the fluorine plasma.

3.3.3 Anodization

Anodization is used in the process to form an insulation layer to prevent the wiring layer from shorting to the bottom electrode. It was first introduced by Dr. X. Meng at University of California, Berkeley. [30] The anodized layer is grown by passing a direct current through an electrolytic solution (Boric acid formed with 20% ammonia pentaborate and 80% DI water), with the junction wafer serving as the anode (the positive electrode). The current releases hydrogen at the platinum cathode (the negative electrode) and oxygen at the surface of the anode, creating a build-up of Niobium oxide. The Nb surface covered with photoresist will not be anodized. The thickness of the oxide will be

determined by the voltage applied by the current source. According to the experiment, 20 Volt will result in about 50 nm thick Nb oxide. The chemical reaction happened on the two electrodes is shown below in Figure 3.2:



At the anode: $2Nb(s)+5H_2O(l)=Nb_2O_5(s)+10H^++10e^-$

At the cathode: $10H^++10e^-=5H_2(g)$

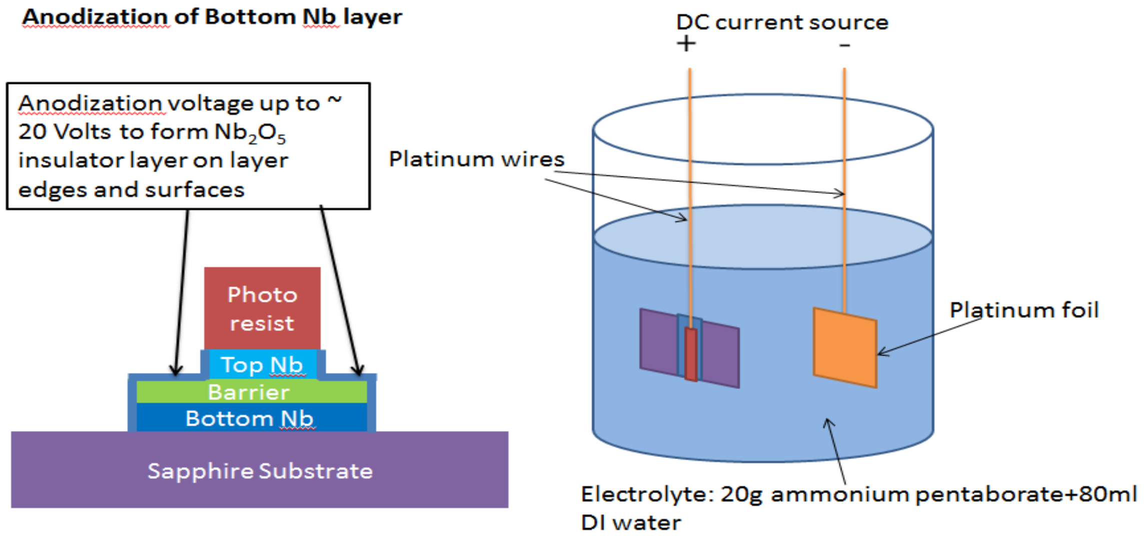


Figure 3.2. Schematics of anodization

3.3.4 Dielectric deposition and lift-off

As shown in Figure 3.3, after anodization, the edge and surface of the barrier are coated with several nanometer thick of oxide. To improve the insulation between the wiring layer and bottom Nb, we deposit another SiO_2 layer by RF sputtering and lift it off. Without removing photoresist, the SiO_2 was loaded into vacuum chamber and sputtered with a 2 inch Torus sputter gun. Due to the low growth rate (~4 nm/minute) of insulating

material by RF sputtering, the growth takes 1 – 1.5 hours to for a 200 – 300 nm thick insulation layer. After deposition, the sample was immersed and rinsed in hot photoresist stripper (around 70 °C) to remove photoresist and thus lift off the SiO_2 over the junction area, where it was coated with photoresist during the SiO_2 deposition process. Then the sample was loaded back to the vacuum chamber for wiring layer deposition.

3.3.5 Ion milling and wiring layer deposition

Before the deposition of the Nb wiring layer, the surface of the top Nb electrodes needs to be cleaned with Argon ion milling to remove the natural oxide that may interfere with the measurement. Commonwealth Scientific IBS-600 Argon milling unit has a 4 inch-diameter ion source and it is 6 inch away from the wafer plate. The milling process is done in a high-vacuum chamber with base pressure $<2\times10^{-7}$ Torr. The sample is adhered to the water-cooled plate using Kapton tape to minimize the heating of the sample. Ar gas is introduced by MFC (mass flow controller) through the rear part of the ion source at a rate of 10 sccm. The Ar gas is ionized and accelerated, bombarding the sample surface and removing atoms from the sample. A low beam current is used (10 to 20 mA) to minimize possible damage to the sample and cross contamination from the stainless steel plate. For Nb, the milling rate at 10 mA beam current is about 5 nm/minute. After the Ar ion milling, a 300 nm thick Nb wiring layer needs to be sputter deposited in-situ.

3.3.6 Overview of micro-fabrication process flow

To summarize, a SiO_2 lift-off process combined with selective Nb anodization is used for cross junction fabrication, similar as previous work [12] [31] [32]. 1 cm × 2 mm Nb-barrier-Nb trilayer strip structure was deposited with physical shadow mask. This step could also be alternatively done by patterning a strip on the fully deposited wafer and etching to form the strip. Then the wafer was patterned and etched with CF_4 gas using an Oxford Plasmalab 80µP reactive ion etcher, and the thin barrier usually works as an etch stop. After that, without removing the photoresist, a self-aligned anodization was performed on the etched area with 20 V. A Platinum (Pt) plate was as cathode and a Pt wire was used to connect the sample to the anode with silver paint. [30] 200 nm SiO_2 was RF sputtered after the anodization process and then lifted off with ultrasonic bath in photoresist stripper (heated on hot plate to 70 °C, AZ 400T Photoresist Stripper). 300nm Nb wiring layer was then deposited by DC sputtering after a brief ion milling surface cleaning. Finally, the Nb wiring layer and the top Nb was patterned and etched to define the top electrode. A series of 50, 20, 10, 5 and 2 µm size of square cross junctions were fabricated as shown in Figure 3.3.

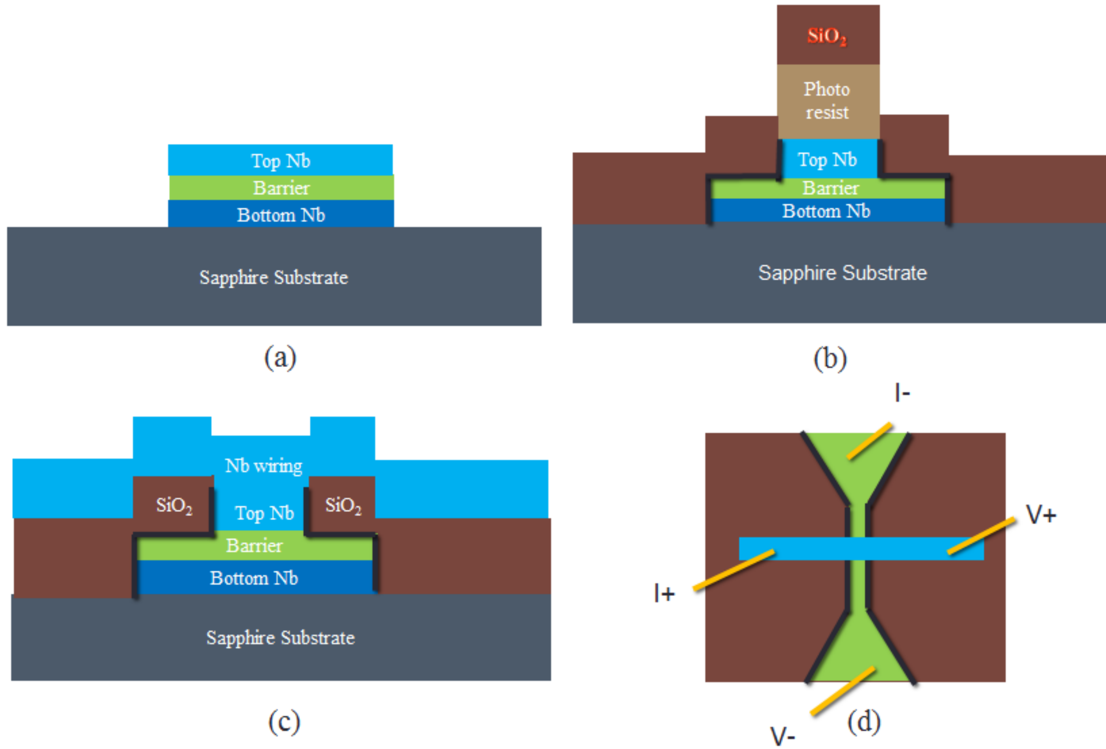


Figure 3.3. Demonstration of junction fabrication process: (a) Junction trilayer strip definition; (b) First etching, anodization and SiO_2 deposition; (c) SiO_2 lift-off, ion milling and wiring layer deposition; (d) Second etching to define junction area and wire bonding

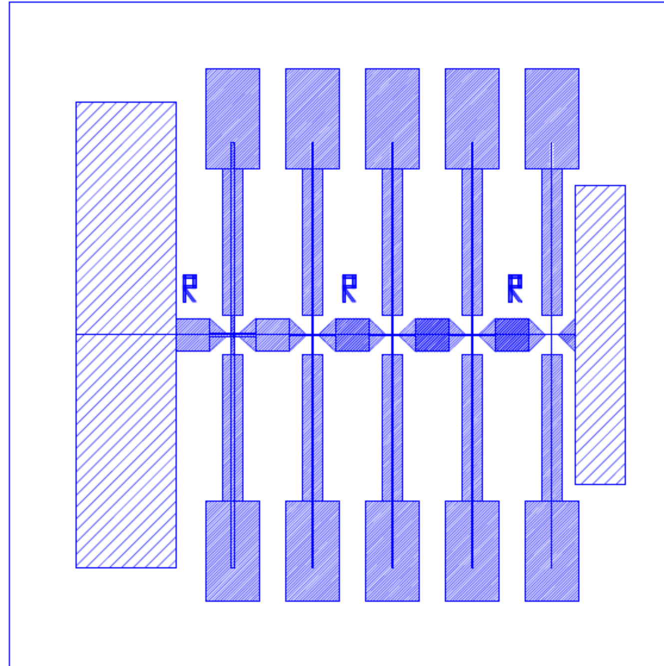


Figure 3.4 Lithography mask lay-out for the fabricated cross junction, designed by Prof. John M. Rowell

3.4 Wire Bonding

In order to electrically contact the junction to the measurement setup, the wire bonding step is required. To avoid any electrostatic discharge damage, the wire bonding station, chip carrier and the operator are all grounded during this process. The wire bonding step is performed in a room with ~40% relative humidity to minimize the chance of electrostatic damage.

The 1 cm × 1 cm size junction wafer was placed in a gold-plated ceramic 44-pin chip carrier, designed to be compatible with our electrical measurement system. The

wafer was attached to the 44-pin chip carrier with silver paint (made by 2SPI) or photoresist. After the adhesion is cured (5 minutes for silver paint and 30 minutes for photoresist), the junction contact pads were connected manually to the electrical connection pins of the chip carrier with thin gold wire (125 mil /31 micron in diameter, made by California Fine Wire) and silver paint. On the wafer, in order to perform four-point measurement, each junction will require two contacts on the top electrode line and two contacts on the bottom electrode line, and the latter two can be shared with all the other junctions. So for a typical 5-junction wafer, 12 connections will be made. After wire-bonding, the wafers with chip carriers were kept in an anti-static box in the room with ~40% relative humidity.

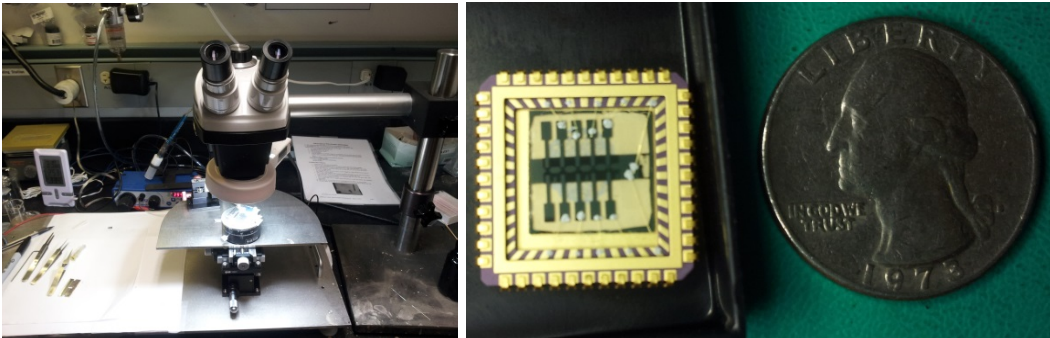


Figure 3.5. Wire bonding station and a wire bonded sample in the lab

CHAPTER 4

GROWTH AND CHARACTERIZATION OF THIN FILMS

In this project, Nb thin films are used as superconductive electrodes in Josephson junctions, as a result of the high critical temperature and large energy gap of films made by a convenient growth method. The T_c of 9.25 K enables the device to operate at liquid Helium temperature (4.2 K). A large energy gap will allow larger Josephson coupling energy and better tunneling.

Nb has been used for the electrode material in Josephson junctions for most practical applications since the 1980s. [34] Nb/Al-AlO_x/Nb junctions have been developed since 1982, and became the favored choice because it is able to produce devices can be made over a wide range of critical currents with excellent reproducibility and uniformity. [10] Nb based processes also have demonstrated possible large scale integration.

There are several articles that describe how to optimize the room temperature growth of the Nb electrode for incorporation into these junctions. [35-37] Achieving a smooth surface topography is crucial for complete coverage by the barrier metal without pin holes or other surface defects. The films must also have low levels of impurities and minimal film stress to adhere and attain a high T_c and corresponding gap value. For the growth part, we want the Nb to have good quality in terms of T_c, resistivity ratio, surface

roughness. We varied the growth condition and characterized films for optimizing the deposition process.

It has been established that Nb films grown at elevated temperatures can have significantly smoother surface topography and improved structural and electrical properties. [26, 38] We want to utilize these advantages for Josephson junctions.

4.1 Characterization of Nb thin films

A set of 400 nm-thick Nb thin films were sputtered at substrate temperatures (T_s) ranging from room temperature to 900 °C. RBS analysis shows that all films are free of oxygen down to the detection limit of <0.1%. For films grown at 400-600 °C, the epitaxy, superconducting transition temperature (T_c), residual resistivity ratio (ρ_{300K}/ρ_{10K}, RRR) and rocking curve FWHM are representative of high quality Nb thin films, shown in Table 4.1. Deposition at above 400 °C on (1-102) sapphire face yields epitaxial (200) Nb measured by an RBS channeling scan. A minimum χ_{min} value of 12% was obtained in Nb grown at 500 °C. For films grown at 500 °C and higher, RBS indicates some Al and oxygen diffuses from the sapphire substrate into Nb near the substrate interface, although this diffusion does not affect RRR or T_c until 700 °C.

Table 4.1. Characterization of Nb grown at different temperatures with dipping measurement and RBS

T_s (°C)	T_c (K)	ρ_{300K} (μΩ.cm)	ρ_{10K} (μΩ.cm)	Δρ (μΩ.cm)	RRR	RBS χ_{min}
25	9.2	24	5.5	18.5	4.3	No
200	9.2	20.4	1.63	18.8	12.5	No
400	9.2	18.8	0.14	18.7	134.3	30.0%
500	9.2	19.3	0.16	19.1	122.8	12.0%
600	9.2	18.5	0.14	18.4	126.0	17.0%
700	9.2	19.9	0.43	19.5	46.3	25.0%
850	9.1	25.7	2.1	23.6	13.3	n/a
900	9.0	20.9	2.43	18.5	8.6	14.0%

Table 4.2. Δρ of Nb films made at room temperature from a few different systems

Made from	T_c (K)	Thickness (nm)	ρ_{300K} (μΩ.cm)	ρ_{10K} (μΩ.cm)	Δρ (μΩ.cm)	RRR
Everspin	9.15	80	25.3	6.3	19.0	4.0
Ion milling	9.25	365	43.8	10.3	33.5	3.2
MBE-4	9.2	338	24	5.5	18.5	4.3
MH84 by Mengchu	9.15	70	26.8	9.6	17.2	2.8
MH21 by Mengchu	9.2	400	94	22.9	71.1	4.3

Nb films are found to have a room temperature resistivity of less than 20 μΩ·cm and a RRR larger than 100 when the film is deposited on a heated substrate at 400-600 °C, similar as reported in ref. 47. The highest RRR value of 134 is obtained in the film grown

at 400 °C, shown in Figure 4.1 and 4.2. Given the room temperature resistivity to be ~20 μm.cm, the corresponding Nb electron mean free path at 10K is $\lambda = 43.3 \times RRR$ (Å) [39], which is comparable with the thickness of the films (400 nm), indicating that the dominant scattering process is from surface scattering.

The characterization results of Nb films made at room temperature in a few different systems are also summarized. The resistivity of these films is in the range of 2.8 to 4.3. The Δρ value is close to 20 μΩ.cm for three of the samples. T_cs are at 9.1-9.2 K and the thinner films have slightly lower Tc. RBS shows all the films are free of oxygen in the bulk down to 0.5%.

There are two films with larger Δρ and ρ_{10K} values than others but with similar Tc. This suggests the effective cross section of the film current path is reduced, and it would increase Δρ but does not affect T_c, similar as in the MgB_2 films reported by J. M. Rowell. [49]This may come from the impurities in the film (presumably oxygen) segregating to the grain boundaries and forming insulating compounds. For example, in MH21, with the ρ_{300K} values 4 times higher than the other films, we can assume that the film is reduced to only 25% of the cross section carrying current effectively, and the Δρ is also about 4 times higher than other films , respectively.

Oxidation process of Nb will transform from a diffuse oxygen structure to a faceted structure as oxidation temperature increases from RT to above 500 °C, which reduces the oxidation significantly. [40] We hypothesize that less oxygen impurities will

be trapped during deposition of Nb at elevated temperature under the same vacuum condition, thus better surface smoothness and less contamination will be obtained than during deposition at room temperature. At the higher temperatures, the kinetic step of trapping the surface oxygen atoms appears to be overcome and lower levels of oxygen, near the solid solubility (<0.5% at 500 °C) in Nb are detected.

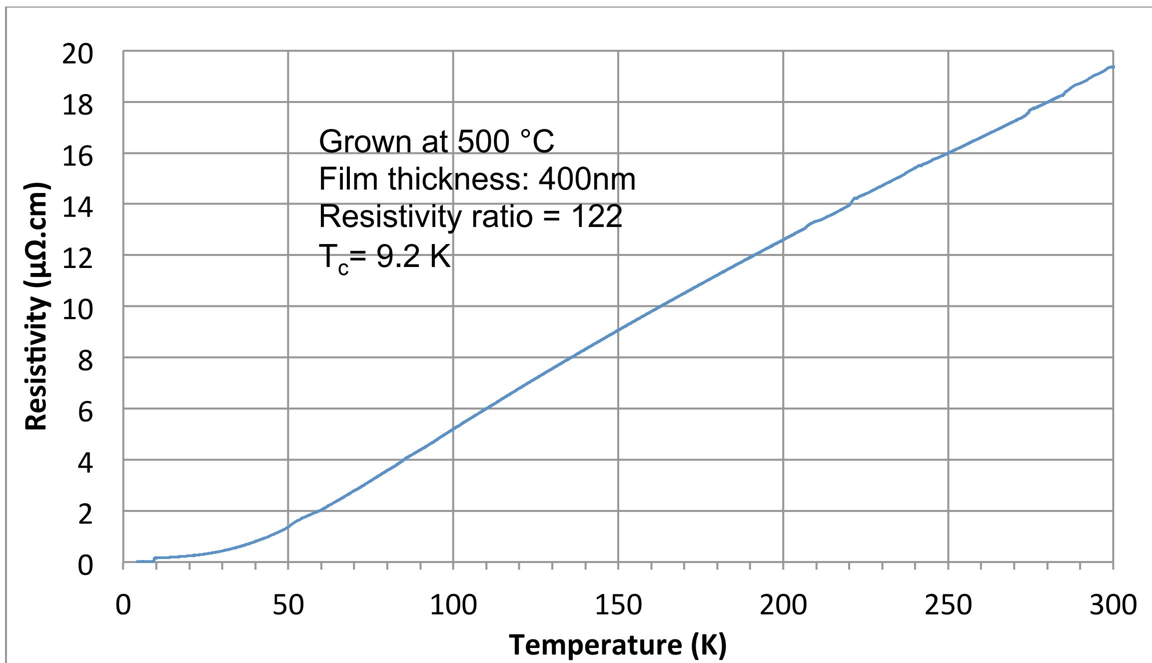


Figure 4.1. Dipping measurement of a 400 nm thick Nb grown at 500 °C with high RRR

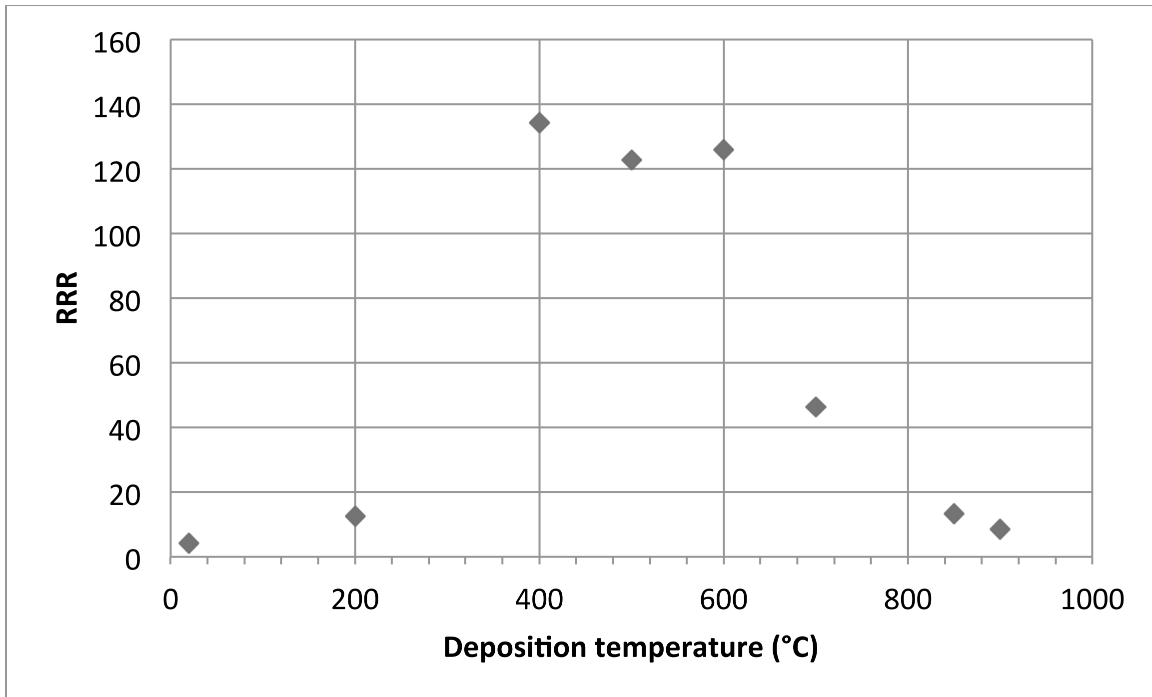


Figure 4.2. Resistivity ratio of Nb films deposited at different temperatures

The superconducting transition temperature (T_c) for films grown below 700 °C is 9.2 K, consistent with that of pure bulk Nb. However, the films grown at and above 850 °C have a reduced T_c. The Secondary Ion Mass Spectroscopy (SIMS) of the Nb films grown at high temperature shows that Al diffused into Nb from the sapphire substrate. (Figure 4.3.) The Nb grown at 850 °C has about 0.5% of Al in the Nb at 100 nm from the sapphire substrate, while the Nb grown at RT has much less Al (~0.01%) at the same distance, with much sharper decline in the Al amount when approaching the film surface. This Al impurity reduces the Nb mean free path; thus the RRR and T_c are reduced.

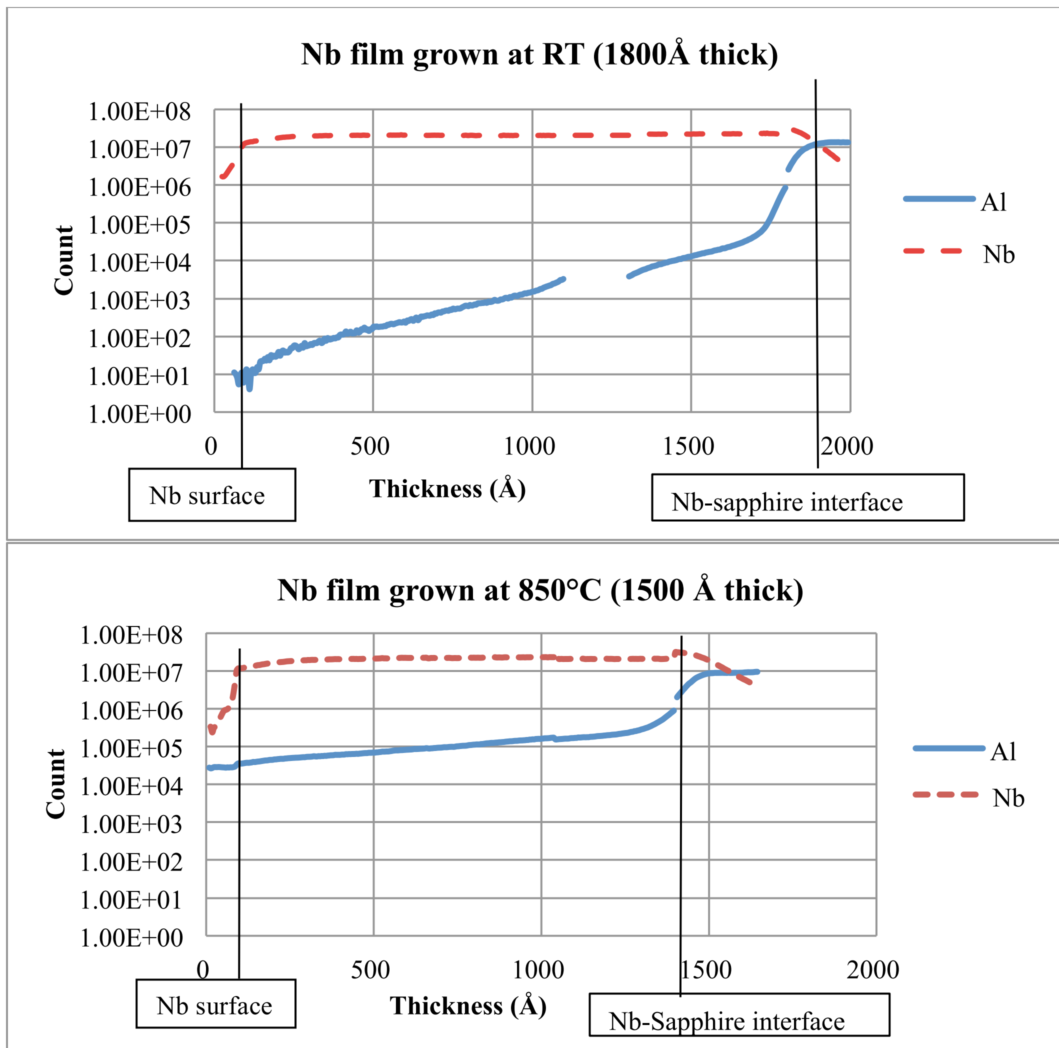


Figure 4.3. SIMS scans of Nb films grown at room temperature and 850 °C showing inter-diffusion between Nb and the sapphire substrate

From the XRD scan, the sample grown at 500°C shows a (110) direction orientation, and the sample grown at 900°C shows (200) growth orientation. The (200) rocking curve of the Nb films grown at 500°C has a FWHM of 0.182°, which indicates the film has good epitaxy. In the 900 °C Nb film, the FWHM for the (200) Nb is as low as 0.111°. The sample is shown to have a few degrees of offset between the Nb film and

the sapphire surface. Phi scan shows four-fold symmetry of the 900 °C Nb film. (Figure 4.4-4.6)

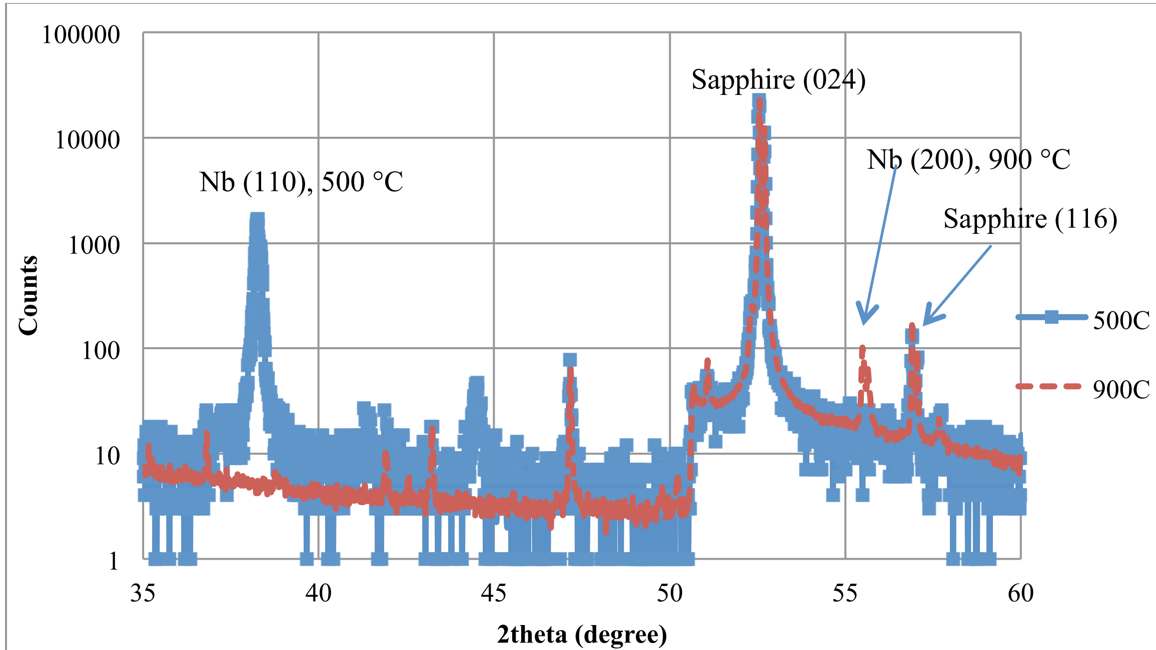


Figure 4.4. XRD Theta-2theta scan (log scale) of Nb films grown at 500 °C and 900 °C shows different growth orientations

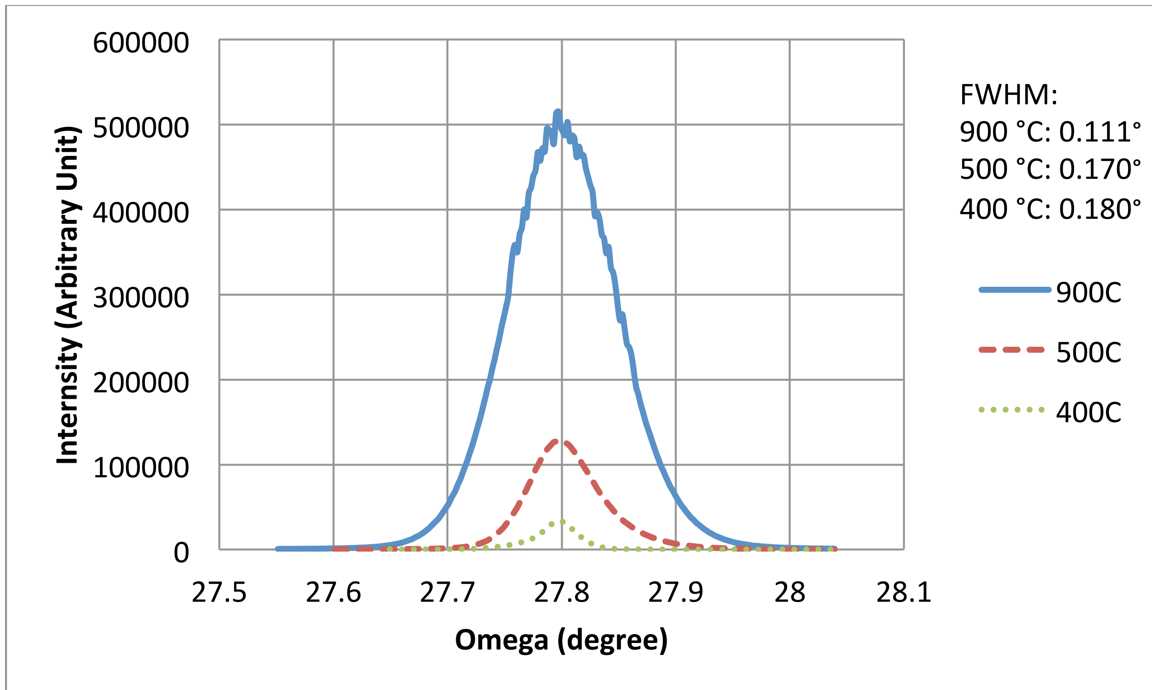


Figure 4.5. XRD Rocking curve of Nb films made at 400 °C, 500 °C and 900 °C

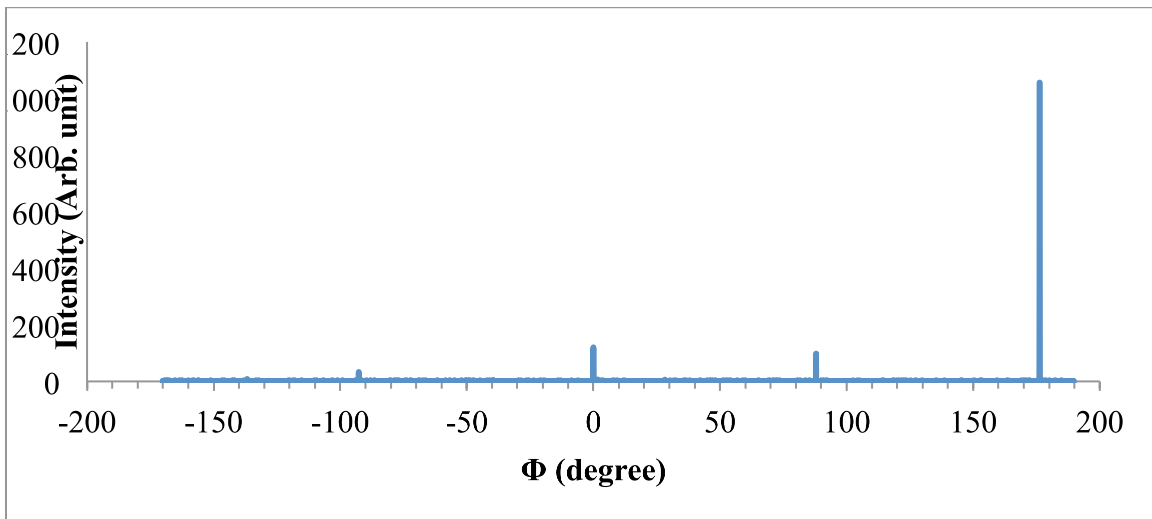


Figure 4.6. XRD Φ scan of (220) reflection of Nb film grown at 900 °C showing four-fold symmetry

Hall mobility measurements were performed on the Nb films grown at RT, 500 °C and 900 °C from 10 K to 300 K using the Van Der Pauw configuration, see Figure 4.7. The Nb film grown at 500 °C has the highest mobility of 750 $cm^2/(V\cdot s)$ at 10 K, which is more than 10 times higher than both the RT sample and the 900 °C sample.

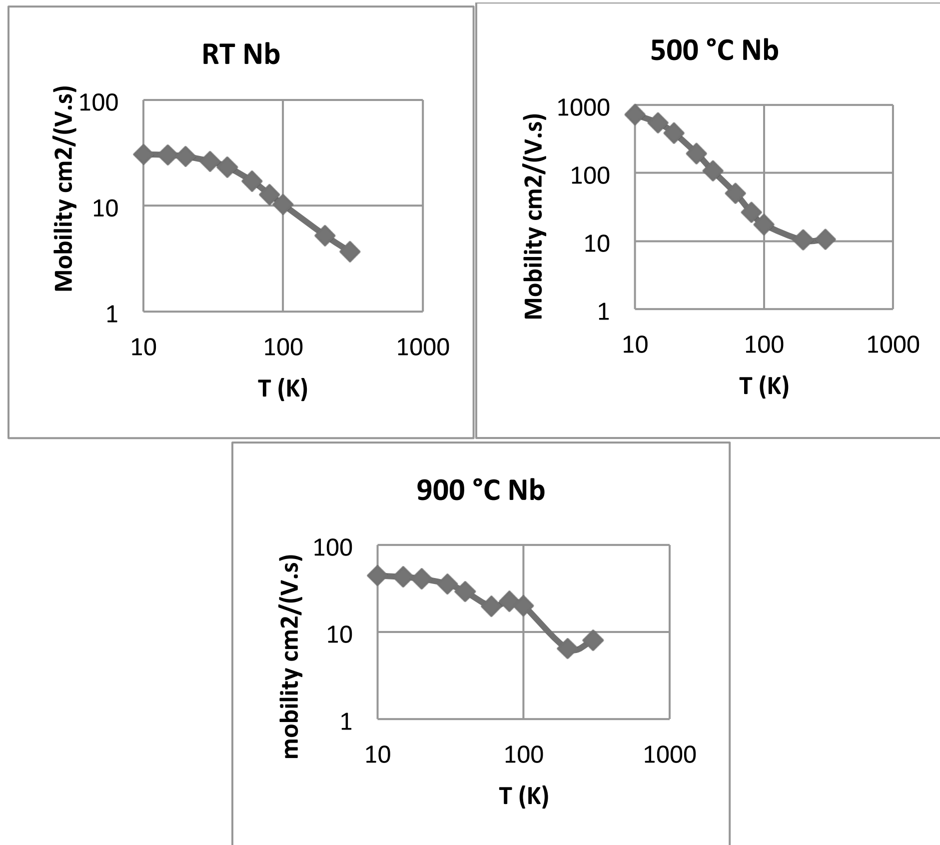


Figure 4.7. Hall mobility of Nb films grown at RT, 500 °C and 900 °C

Transverse magnetoresistance is also observed in the 500 °C sample at low temperarture as shown in Figure 4.8. At 10 K, the [R(H)-R(0)]/R(0) value is about 51% when a magnetic field of 9 T is applied. [39] Fitting the $\mu_B=\sqrt{[R(H)-R(0)]/R(0)}$ gives

a mobility μ=620 $cm^2/V{\cdot}s$, close to the measured Hall mobility. At 100 K and above, magnetoresistance was not observed due to the high residual resistance. The Nb grown at RT and 900 °C has less than 0.5% resistance change at 10 K between 0 T and 9 T.

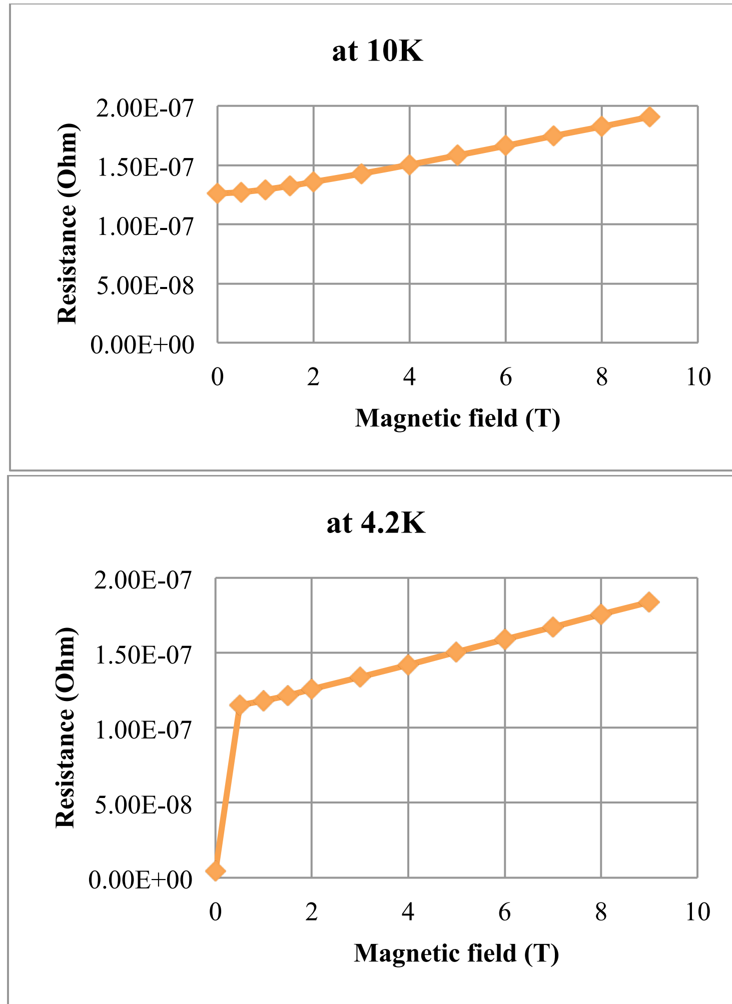


Figure 4.8. Magnetoresistance at 4.2 K and 10 K of 500 °C Nb film

4.2 Growth parameters for achieving smooth Nb at 500 °C

Additional experiments used substrate temperature of 500 °C for Nb growth, to determine the best growth conditions for surface smoothness of Nb thin film. This temperature was chosen because it uses a high enough temperature for the desired structural properties without a significant amount of unwanted Al diffusion from the substrate.

The surface morphology of the base-Nb electrode of the Josephson junctions directly affects the barrier layer coverage on the base-Nb and the quality of the interface. [5] A set of experiments which varied the sputter gun power and growth pressure were performed in order to obtain a relatively smooth Nb film surface. The Nb film thickness was kept at 100 nm. The optimal conditions were found at 180 W sputter gun power and 6×10^{-3} Torr Ar gas pressure. These conditions resulted in a growth rate of 0.25 nm/second.

Table 4.3. The RMS roughness and feature sizes of Nb films grown at 500 °C under varying sputter gun powers and Ar pressures

#	Power (W)	Ar pressure (mTorr)	Average RMS (nm)	Average feature size (nm^2)
a	180	6	0.35	89
b	360	6	0.55	67
c	180	4.5	0.75	191
d	180	3	1.25	289

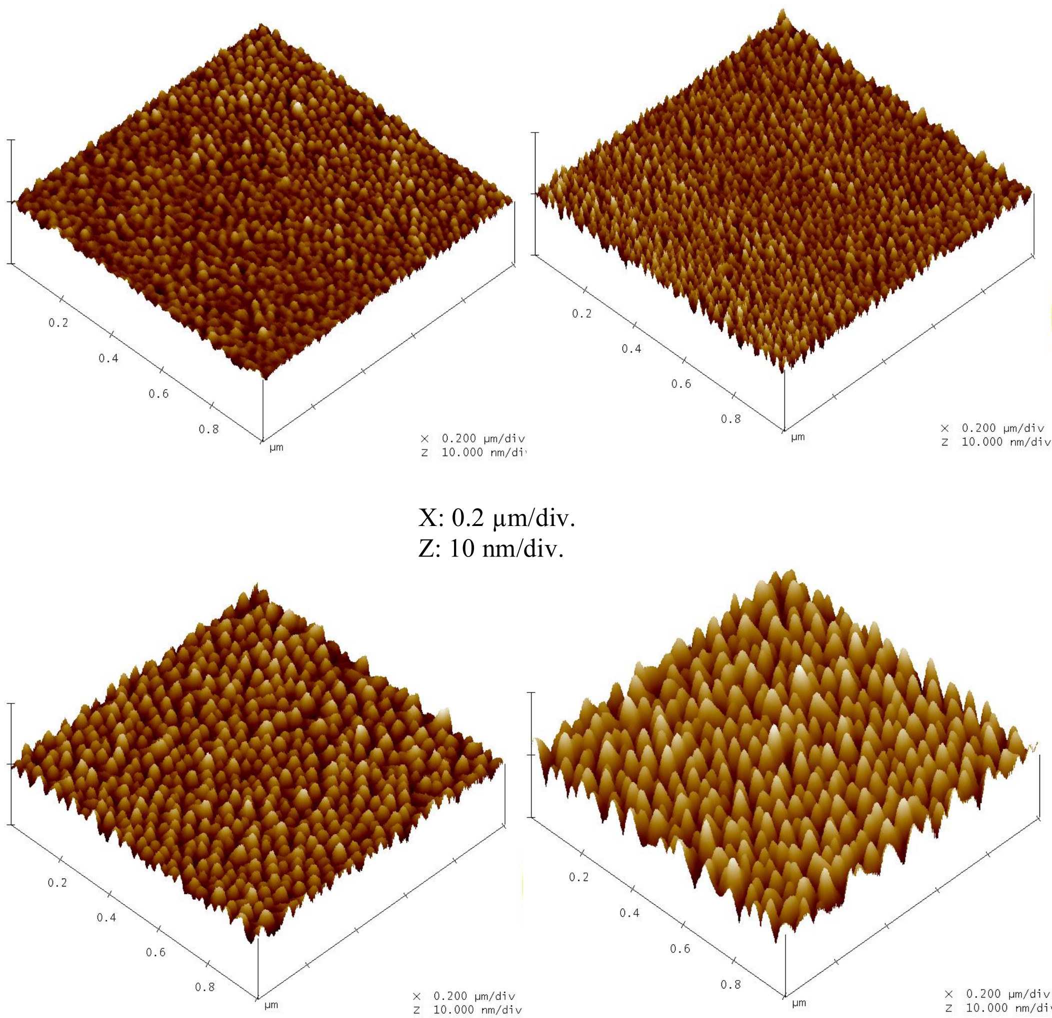


Figure 4.9. AFM images of Nb films grown at 500 °C (Z = 10 nm/div.). (a) Sample grown at 180 W, 6 mTorr (b) Sample grown at 360 W, 6 mTorr (c) Sample grown at 180 W, 4.5 mTorr (d) Sample grown at 180 W, 3 mTorr

The surface roughness and feature size were determined using an Atomic Force Microscope software (Veeco NanoScope) over a 1 µm × 1 µm scan areas. The smoothest film (Figure 4.9) was grown at 180 W and 6×10^{-3} Torr. Films grown at the higher

sputtering power had smaller feature size due to higher surface atom mobility. Films grown at lower pressure have rougher surfaces and larger feature sizes.

4.3 Comparison of surface roughness of Nb-Al and Nb-Hf bilayer films

Nb-Al and Nb-Hf bilayer thin films were deposited in-situ to investigate the surface coverage of the deposited barrier metal layer deposited. 10 nm of Al or Hf was deposited in-situ after the Nb film was deposited at 500 °C.

From the previous reports [13, 41, 42], ambient (or lower) substrate temperature is required to achieve a smooth, complete coverage of thin, say 3 nm of Al on Nb. Because Al will form island at elevated deposition temperatures on Nb, we cooled the substrate down for 30 minutes to about 50 °C before Al deposition. 10 nm Al was evaporated on Nb which was sputtered at 500 °C, after about 30 minutes cooling down. Nb-Hf was deposited at 500 °C for both layers.

The Figure 4.10 indicates that Al does not wet Nb without adequate cooling, and Hf forms smooth surface at elevated temperature with Nb. AFM images clearly show that Al islands are still formed on Nb (RMS roughness = 4.5 nm) due to insufficient substrate cooling, and the Hf surface is still smooth with growth temperature at 500 °C (RMS=0.4 nm), compared with bilayers grown at room temperature.

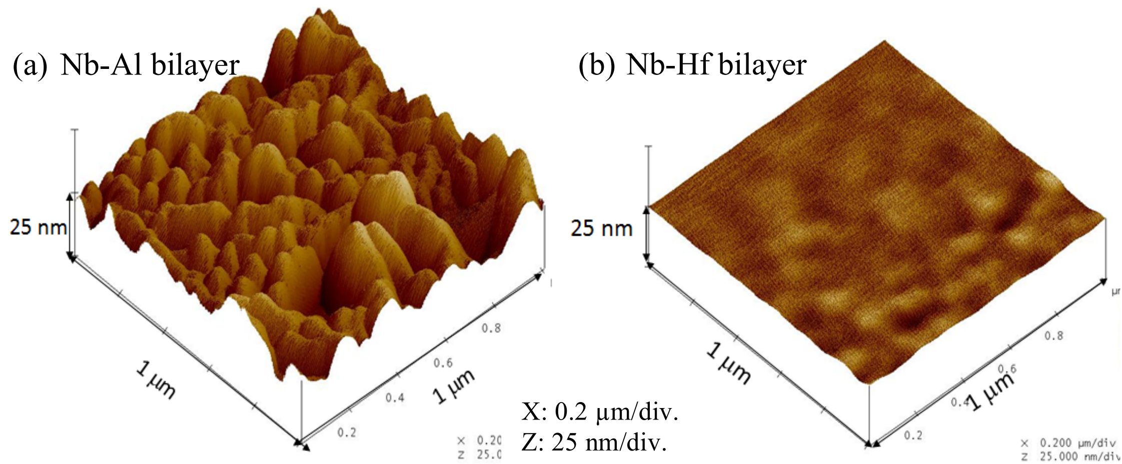


Figure 4.10. AFM images of Nb-Al and Nb-Hf bilayers with bottom Nb layer made at 500 °C. (a) Al deposited at 50 °C, after 30 minutes cooling, surface RMS roughness = 4.5 nm. (b) Hf deposited at 500 °C, surface RMS roughness = 0.4 nm. Z=25 nm/div for both figures.

4.4 Intermixing of Nb-Al and Nb-Hf interface at elevated temperatures

A previous scanning calorimetry study by Coffey, et al. reports that annealing at 140 °C increases the roughness of the Nb-Al interface due to grain boundary diffusion and heterogeneous nucleation of the $NbAl_3$ metallic. [13, 15, 43] We also made a Nb/AlN/Nb trilayer thin film at room temperature and annealed it at 140°C to confirm this. RBS measurements and analysis indicate that the Al barrier is initially 1.5 nm thick after deposition, and about 30% of the Al atoms diffused away after the 140°C anneal. (Figure 4.11) $NbAl_3$ is a superconductor but only has T_c of 0.64 K, along with Nb_2Al of

0.64 K. [19] The Nb_3Al formed at above 1000 K has a high T_c of 18 K, but it does not help the interface degradation at lower temperature that may affect the junction properties.

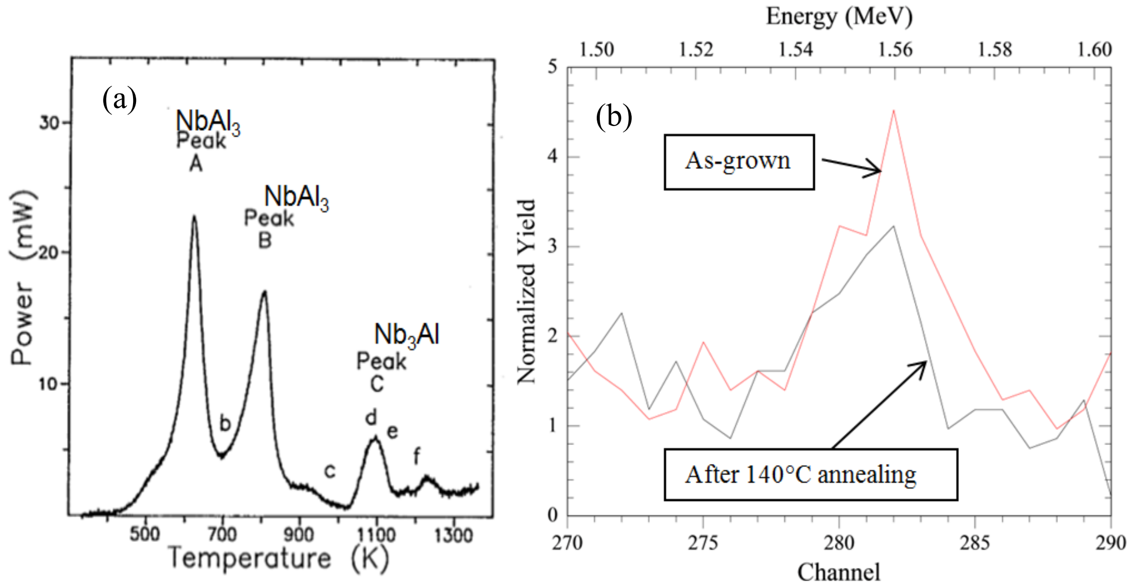
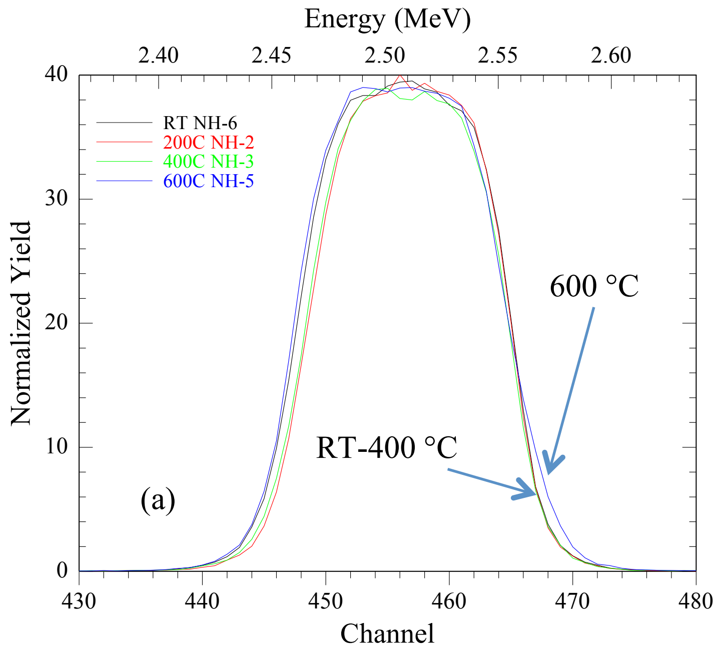


Figure 4.11. (a) Scanning calorimetry shows the formation of $NbAl_3$ (peak A, B) and Nb_3Al (peak C) compounds after annealing to above ~140 °C, reprinted from ref. 15 (b) RBS shows Al in the barrier starts diffusing into the Nb layer after 140 °C annealing.

In contrast, the Nb-Hf interface is not affected by post-annealing up to 400 °C. [43] We also made a set of Nb-Hf bilayers grown on sapphire substrates at RT to 600 °C and found that no mixing between the Nb and Hf is detected up to 400 °C. There is evidence for a small amount of intermixing (about 12 nm with 30% Hf in Nb) for films grown at 600 °C. (Figure 4.12) However, as we mentioned before, Nb-Hf alloys with Hf concentration up to 30% have an elevated T_cs compared to pure Nb, so the tunneling parameters should not be affected with such a small intermixing. [22]



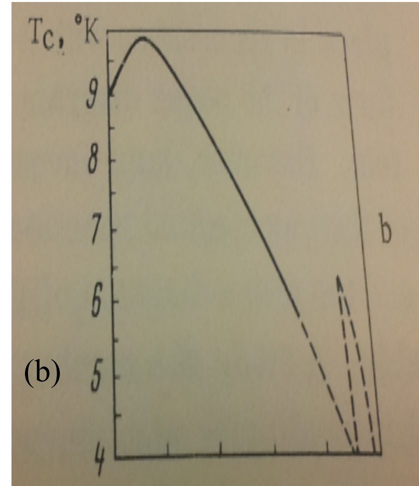


Figure 4.12. (a) Nb peak of RBS scans on Nb-Hf bilayers grown at room temperature to 600 °C, (b) Concentration dependence of T_c of NbHf alloy (atomic concentration, from left Nb 100% to right Nb 0%), reprinted from ref. 22

4.5 Auger Study of Nb/HfO_x/Nb trilayers

A set of Nb/HfO_x/Nb trilayers was grown on sapphire substrates at RT to test the annealing stability of the HfO_x barriers. The op Nb was kept as 20 nm thick for convenience of sputtering during the depth profile process. Hf was sputtered twice for a 1.5 nm thick layer and oxidized twice at 20 Torr for 3 minutes for complete oxidation. AES-1 was scanned by Auger Spectroscopy as-grown, and AES-2 was annealed in forming gas (95% Ar and 5% H_2) for 30 minutes at 300 °C before being taken for measurement. The experiments consist of a series of surface Auger spectroscopy which is

done after each short Ar sputtering steps on the film. Because Auger does not have high enough resolution, especially in the >1500 eV region, it is hard to see a difference between Hf and HfO_x in the depth profile. Nb and Hf peaks also overlap at 1620 eV which makes things more complicated. So instead of using depth profile, we performed AES scans manually after every etch step (2 min) and compared the normalized concentration of element generated from the Nb, Hf and O peak heights. The oxygen concentration becomes more spread out after annealing, and the Hf concentration remains relatively unchanged.

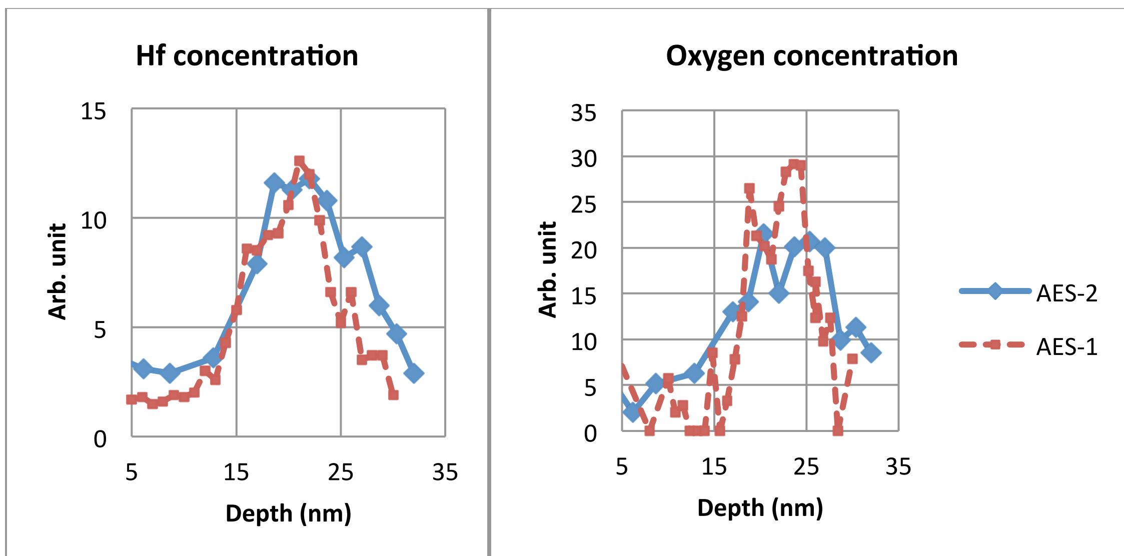


Figure 4.13. Auger Spectroscopy depth profile of oxygen and Hf percentage shows annealing leads to oxygen diffusion: AES-1 (as-grown) and AES-2 (annealed at 300 °C)

4.6 TEM study of junction trilayers

A high resolution TEM scan was done on a Nb-Hf-Nb trilayer structure, to investigate the Nb-Hf interface, as shown in Figure 4.14. The bottom Nb and Hf was grown at 500 °C and annealed for 30 minutes as a bilayer. The top Nb was grown at room temperature. Atomic resolution was achieved in this specimen. Epitaxy growth was found through the 3 nm thick Hf layer, as shown in Figure 4.15 by orientation mapping. It also indicates that the bottom Nb has a columnar growth with large angle grain size of around 50 nm and the epitaxial growth keeps on after the thin Hf layer through the top Nb. The Nb and Hf layers are polycrystalline. The interface of Nb-Hf was abrupt according to the image.

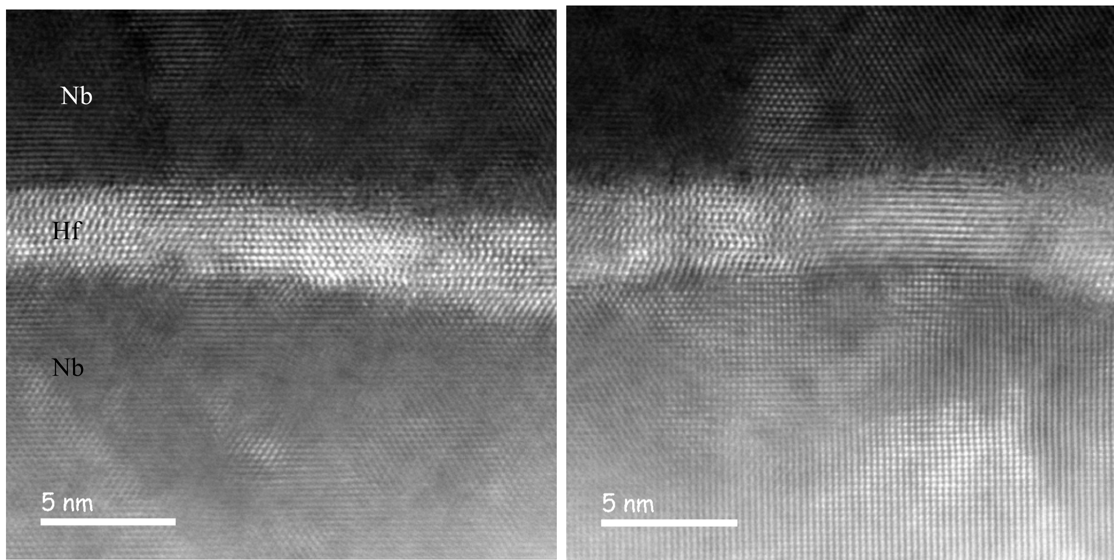
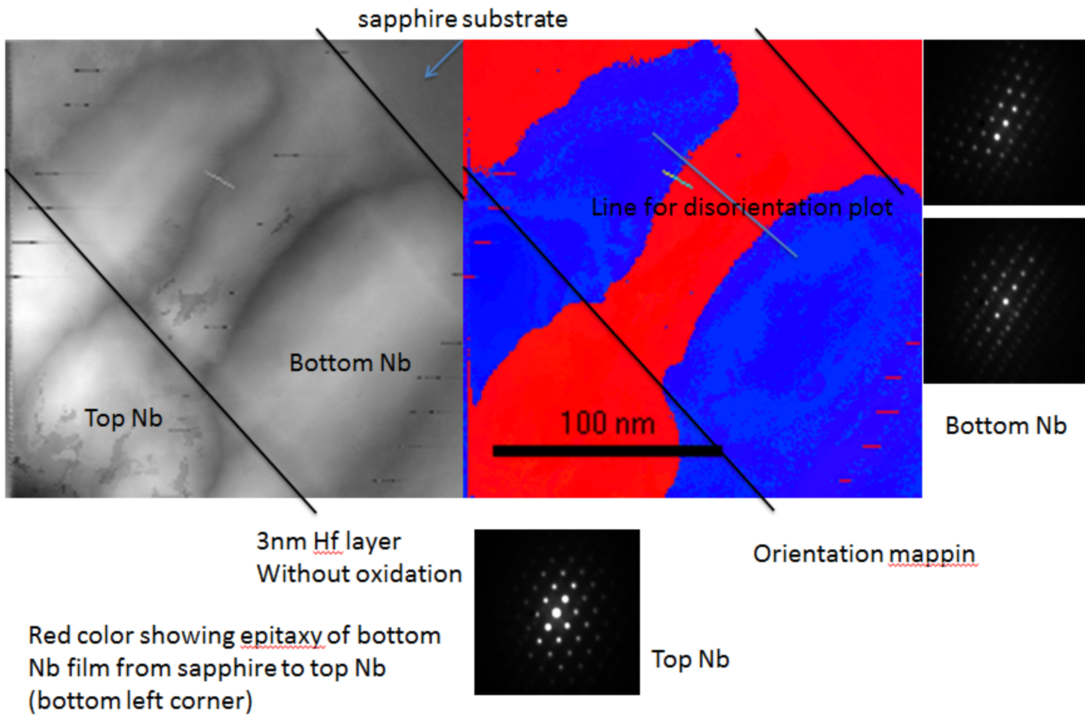


Figure 4.14. High resolution TEM cross-section dark field images of Nb-Hf-Nb trilayer structure, taken by ASU-ARM200F (JEOL) microscope, courtesy of Prof. Ray Carpenter



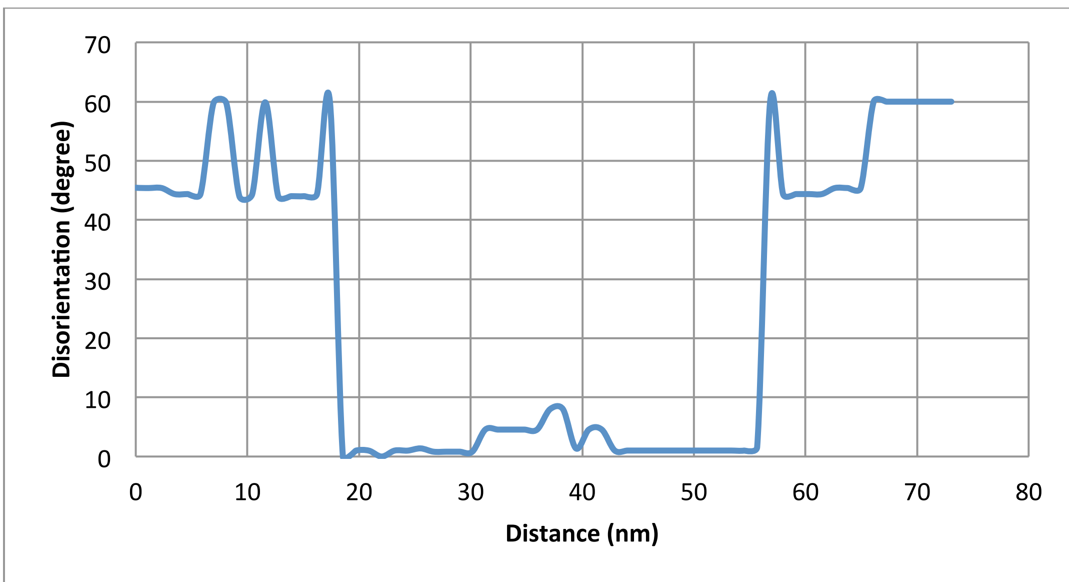


Figure 4.15. Orientation mapping of of Nb-Hf-Nb with 3 nm thick Hf layer, courtesy of

Prof. Ray Carpenter. Line scan of disorientation indicates existing small angle grain boundary.

TEM images of Nb/Al-AlO_x/Nb and Nb/Hf-HfO_x/Nb trilayers also confirm that Hf deposition at elevated temperature is smoother than Al on Nb. Even deposited at room temperature, the Nb/Al-AlO_x/Nb junction that shows an excellent I-V characteristic still has a quite rough bottom Nb-Al interface, as shown in Figure 4.16. The smooth Al layer starts to diffuse into bottom Nb which made the bottom Nb-Al interface rougher than the top Nb-AlO_x interface.

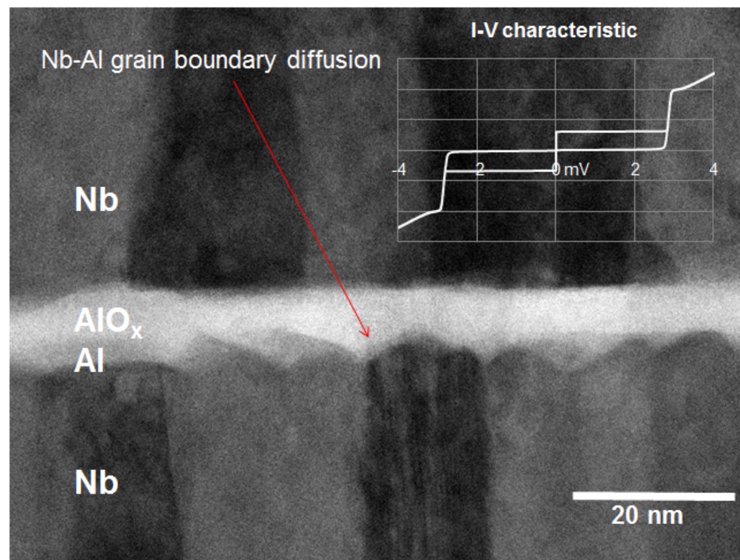


Figure 4.16. TEM bright field image of Star Cryoelectronics commercial Nb/Al-AlO_x/Nb junction synthesized at room temperature with its nice I-V characteristic. Al is about 7 nm thick. Possible Nb-Al diffusion is observed between bottom Nb and Al

At the same time, Nb/Hf-HfO_x/Nb junction grown at elevated temperature shows it has a much smoother Nb-Hf interface as shown in Figure 4.17.

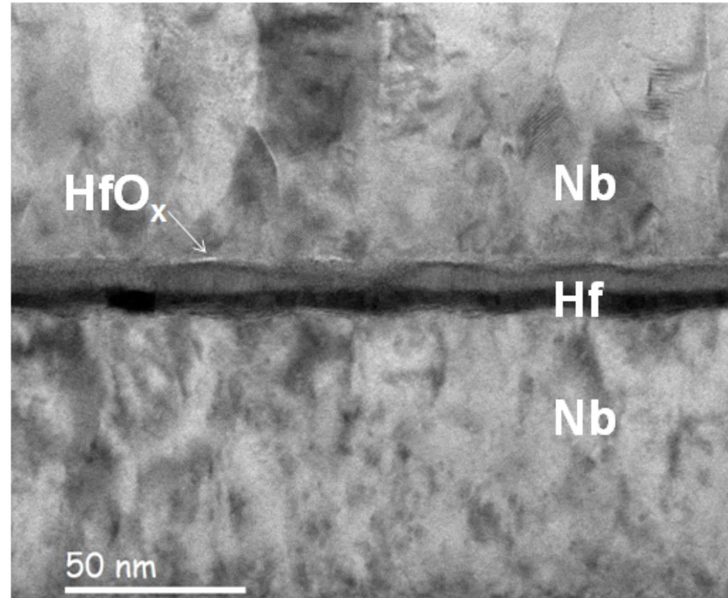


Figure 4.17. TEM bright field image of Nb/Hf-HfO_x/Nb junction structure, bottom Nb and Hf (9 nm thick) grown at 500 °C and top Nb grown at 300 °C

In addition, according to S. Morohashi and S. Hasuo's work [43], after junction growth at room temperature, the bottom Nb-Al interface is rougher than Nb-Hf and Nb-Zr interface. And after annealing at 400 °C, AlO_x barrier is locally damaged. (Figure 4.18)

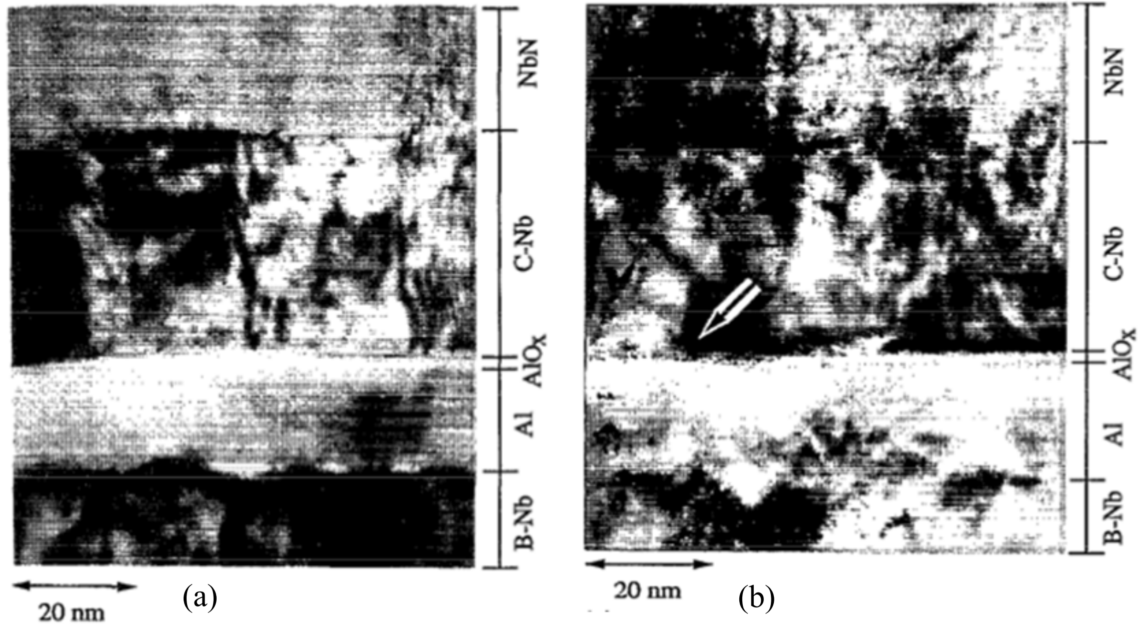


Figure 4.18. Reprinted from S. Hasuo's publication [43] (a) After growth at room temperature, the Nb-Al interface is rough. (b) After annealing at 400 °C, the AlO_x barrier is locally damaged (pointed by arrow).

4.7 Summary and conclusions

Nb thin films have been synthesized at various substrate temperatures and characterized with AFM, RBS and electrical tests. Nb films grown on R-plane sapphire substrates at 400-600 °C show RRR>100 and good epitaxy. These films also have high mobility (750 $cm^2/V{\cdot}s$) at low temperatures. Nb films grown at temperatures >700 °C are found to have contamination from Al diffusion from the sapphire substrate, which reduces the T_c, RRR and Hall mobility of the film. Combination of growth pressure and power were studied for best surface RMS roughness results.

Surface roughness of Nb-Al and Nb-Hf bilayer was measured by AFM, and Nb-Al and Nb-Hf interface intermixing after annealing was characterized. Nb-Hf bilayer structures grown at elevated temperatures have smooth interfaces with good coverage. This work suggests that thermodynamically stable Nb bottom electrodes and Hf layers can be grown at elevated temperatures that will have better thermal stability than current AlO_x barrier junctions.

CHAPTER 5

CHARACTERIZATION OF JOSEPHSON JUNCTIONS

After the fabrication and wire bonding processes as described before, the junctions will be placed on a dipping probe and dipped into the liquid Helium dewar in the shielded room. The measurement system with computer outside the shielded room is connected to the dipping probe the room through the wall of the room with RF filter feedthrough. The dipping process is to cool the sample down to 4.2 K which usually takes about 5-30 minutes depending on the dipping speed that you want.

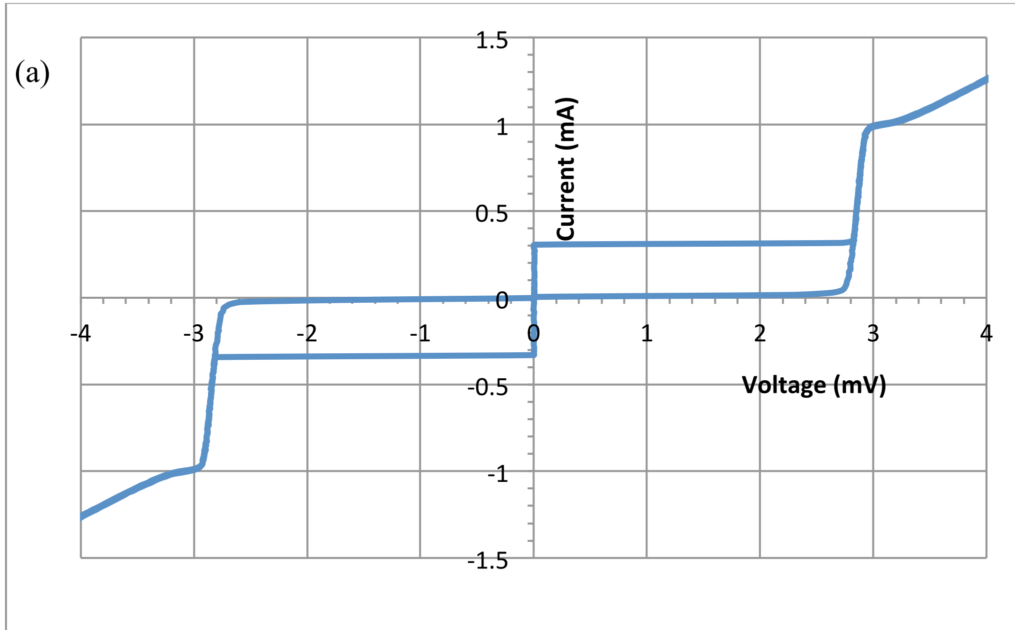
Four-point measurement is done by sourcing current with a Keithley 220 current source, from 0 to a preset maximum value in 100 steps and tracing back to 0. The negative part of current is also measured after the positive part is recorded. I-V measurement is done using C++ software programmed by Dr. Lei Yu, [28] which is used to record the current value and corresponding voltage automatically during the measurement.

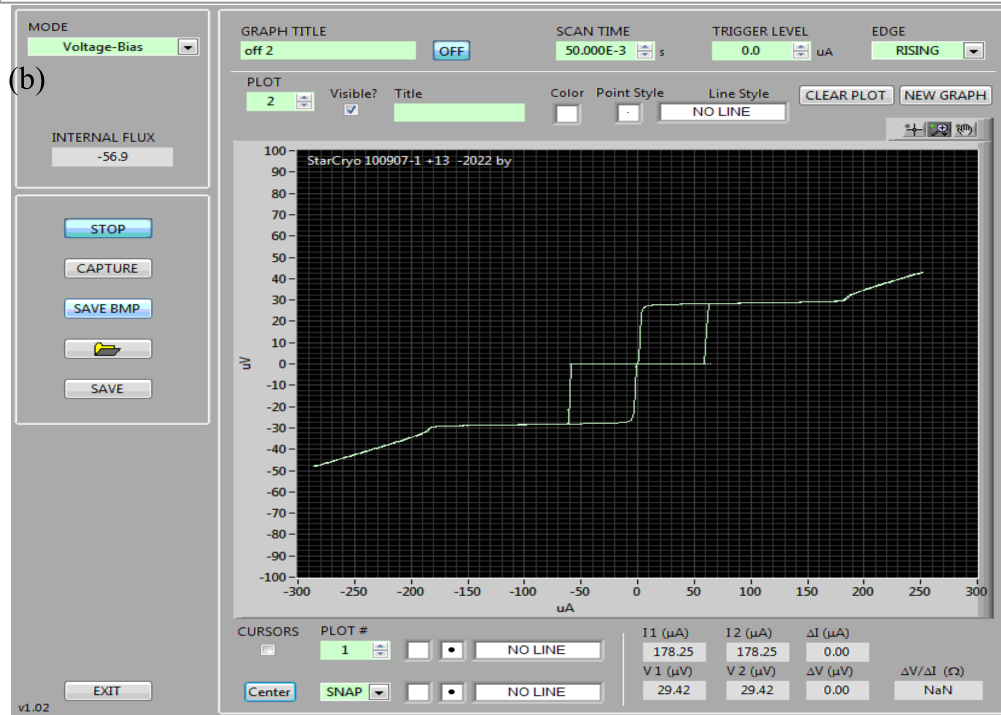
There is also a Mr. Squid system available that can be used inside the shielded room that is based on an oscilloscope and requires a laptop to run its program. The system measures up to 0.4 mA.

5.1 Qualification of I-V measurement system

A commercial Nb/Al-AlO_x/Nb Josephson junction provided by Star Cryoelectronics was characterized by our I-V measurement system, including the

shielded room, wiring feed through and computer with the current source and voltage meter.





(c)

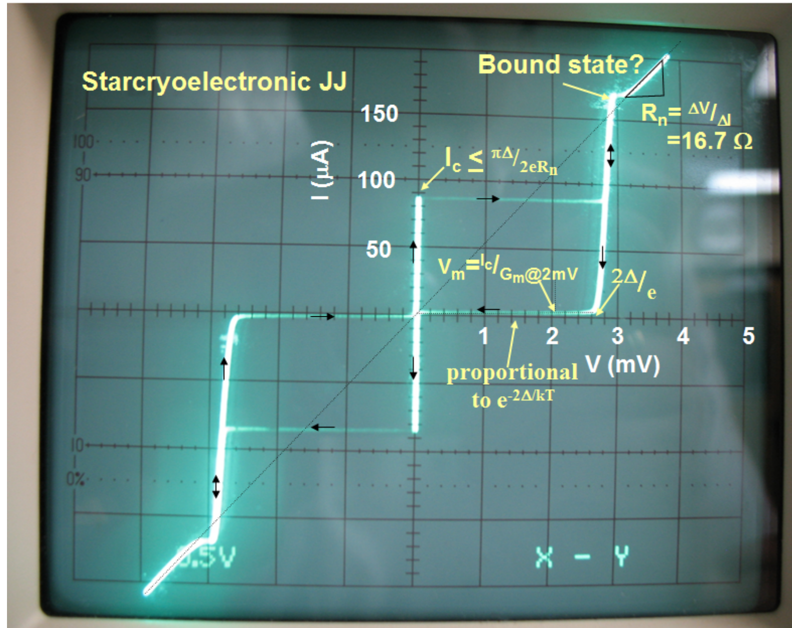


Figure 5.1. I-V characteristic of Nb/Al-AlO_x/Nb junction (Star Cryo. 100907-1) measured in our lab by (a) I-V measurement system (b) Mr. Squid system and (c) oscilloscope measurement

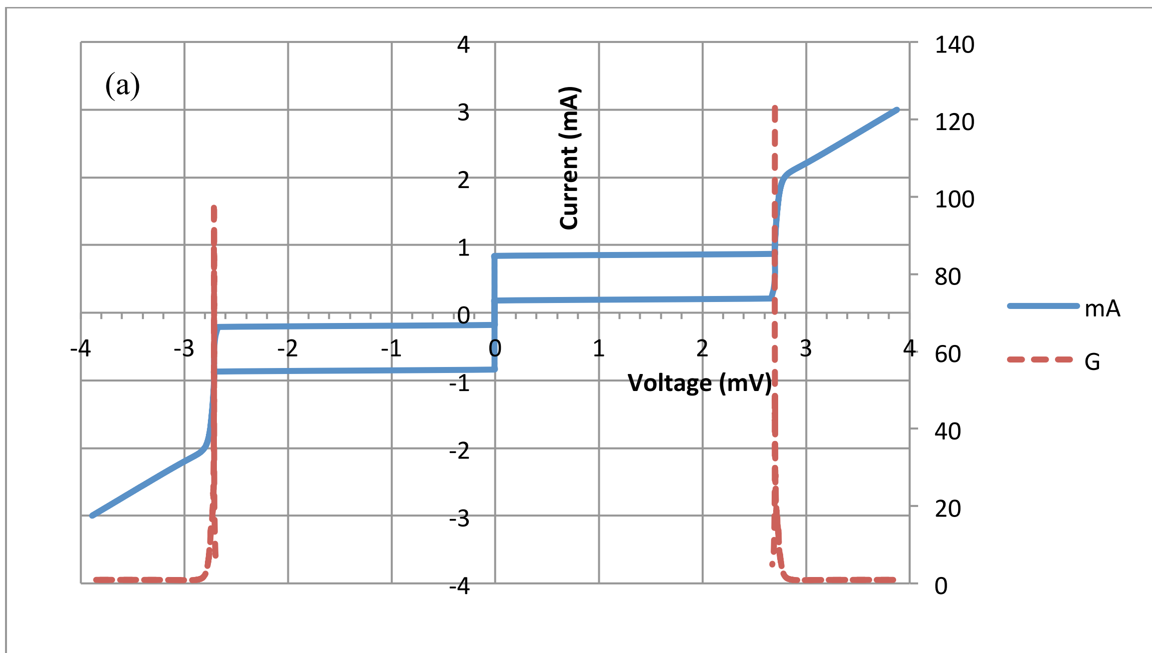
Comparing with the oscilloscope measurement result from Star Cryoelectronics, the critical current of the junction is lower when measured in our lab. We attribute this effect to flux trapping, because the critical current value usually changes after every warming up and dipping process.

5.2 Nb/Al-AlO_x/Nb junction fabrication as process certification

To prove our fabrication process is valid, we obtained a Nb/Al-AlO_x/Nb trilayer wafer from Everspin, Inc. that was grown on an 8-inch Si wafer (thermally oxidized) with 7 nm thick Al, order to test our fabrication process. The wafer was diced to 1 cm × 1 cm

for process before shipment to ASU. The junction was made by the micro-fabrication process in our lab.

In Figure 5.2, the junction is showing a sharp gap and decent critical current. The gap is slightly smaller than 2.8 meV, since the thickness of Nb electrode is only around 40 – 50 nm, which is less than the coherence length of Nb. The magnetic dependence of critical current fits the theoretical calculation pretty well.



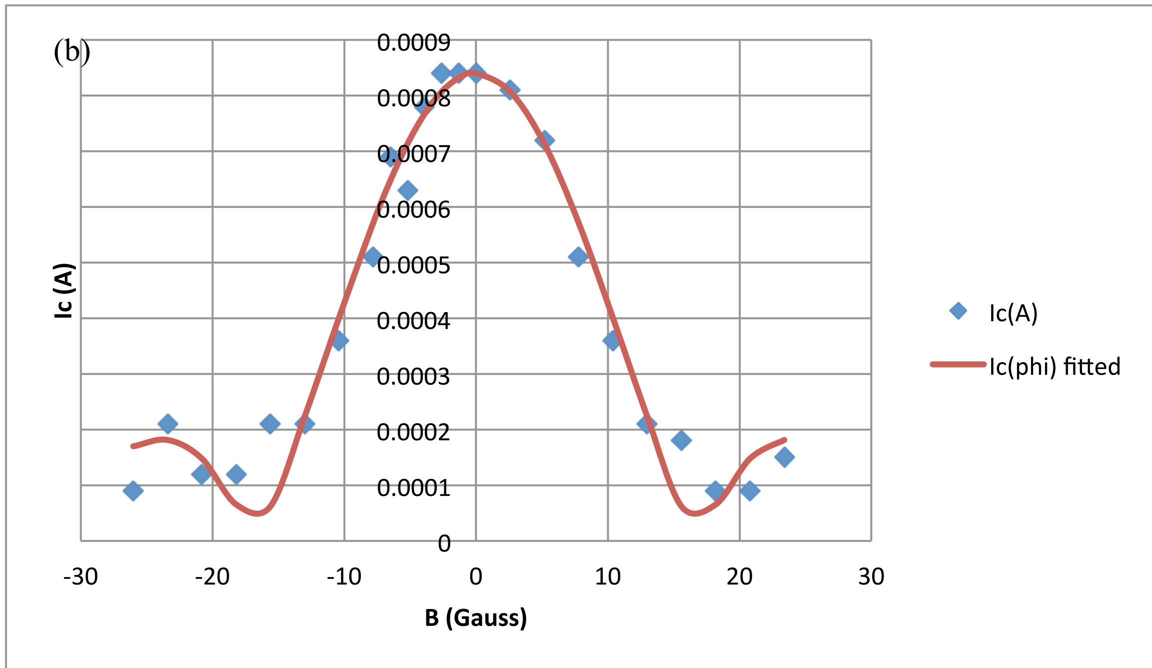
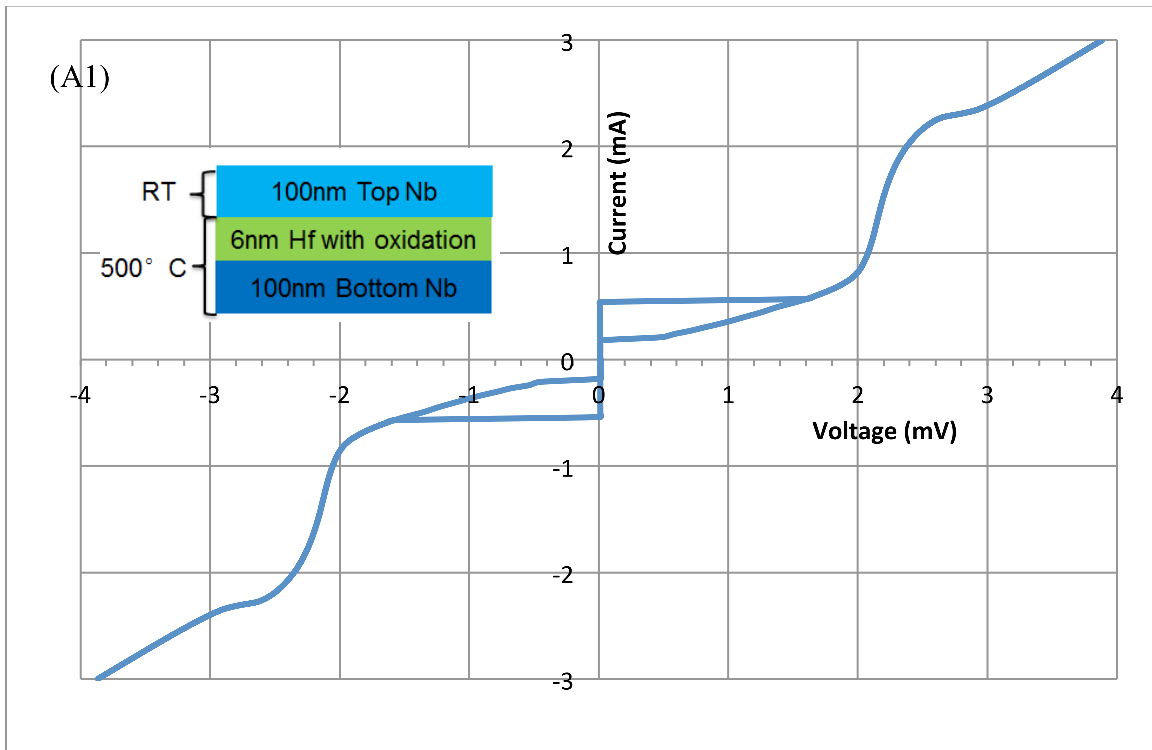


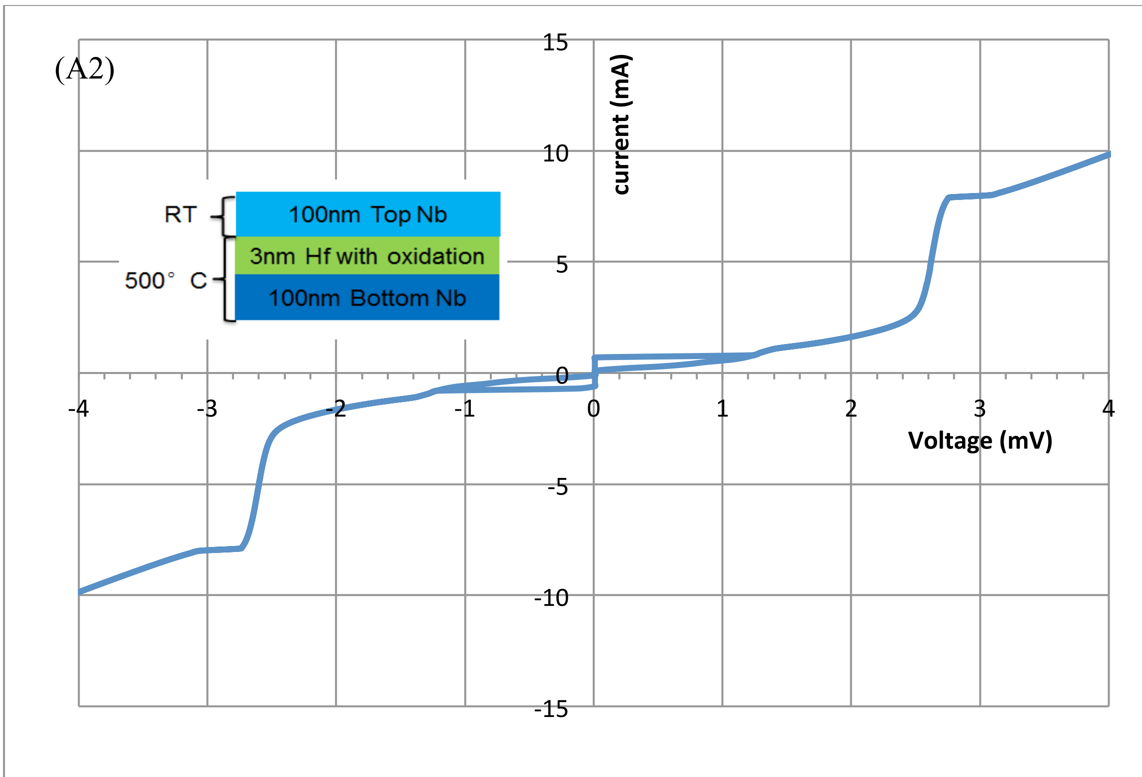
Figure 5.2. 5 µm × 5 µm Everspin Nb/Al-AlO_x/Nb at 4.2 K, Rn=1.1 Ohm, I_cR_n=0.92 mV, J_c=3360 A/cm^2 (a) I-V characteristic (b) magnetic field dependence of I_c

5.3 Junctions with oxidized Hf layer as barrier

We started with Nb/Hf-HfO_x/Nb trilayer structure, similar to the Nb/Al-AlO_x/Nb junctions. Trilayer thin films were synthesized by the growth methods mentioned in chapter 2, and fabricated into Josephson junctions by the process methods mentioned in chapter 3. The bottom Nb electrode and the Hf layer were sputtered at 500 °C, followed by oxidation in the loadlock in 20 Torr pure oxygen at RT for 3 minutes. The top Nb electrode was sputtered at room temperature.

Junction A1 was made with a Hf layer thickness of 6 nm, A2 with 3 nm and A3 with 2 nm. As a normal layer, excess Hf metal suppresses the superconductive gap value of the bottom Nb. The magnetic field dependence of junction A2 indicates the critical current through the junction is quite uniform. Junction A1 with 6 nm of Hf has a smaller gap value than A2 due to proximity effect. Junction A3 with Hf thickness of less than 3 nm shows a less R_nA (normal resistance × area) product and larger leakage current indicates the barrier has pinholes in it, which may be due to the incomplete Hf coverage.




(A2)
RT
500° C
100nm Top Nb
3nm Hf with oxidation
100nm Bottom Nb
current (mA)
Voltage (mV)
15
10
5
0
-5
-10
-15
-4
-3
-2
-1
0
1
2
3
4

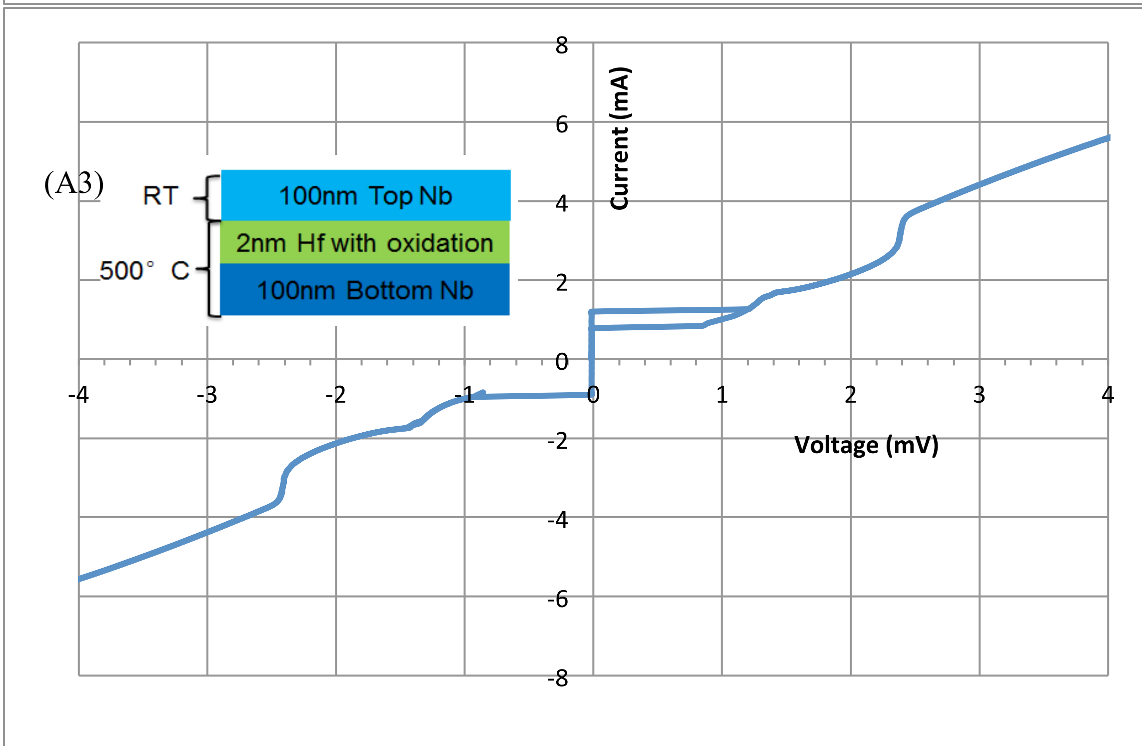

(A3)
RT
500° C
100nm Top Nb
2nm Hf with oxidation
100nm Bottom Nb
Current (mA)
Voltage (mV)
8
6
4
2
0
-2
-4
-6
-8
-4
-3
-2
-1
0
1
2
3
4

Figure 5.3. I-V characteristic of Nb/Hf-HfO_x/Nb junctions A1-A3 at 4.2 K:

(A1) 6 nm thick Hf (#MH114), 30 μm × 30 μm size, gap = 2.14 meV, R_n=1.37 Ohm;

(A2) 3 nm thick Hf (#NHN43), 50 μm × 50 μm, gap = 2.72 meV, R_n = 0.46 Ohm;

(A3) 2 nm thick Hf (#NHN45), 5 μm × 5 μm, with gap = 2.41 meV, R_n = 1.4 Ohm .

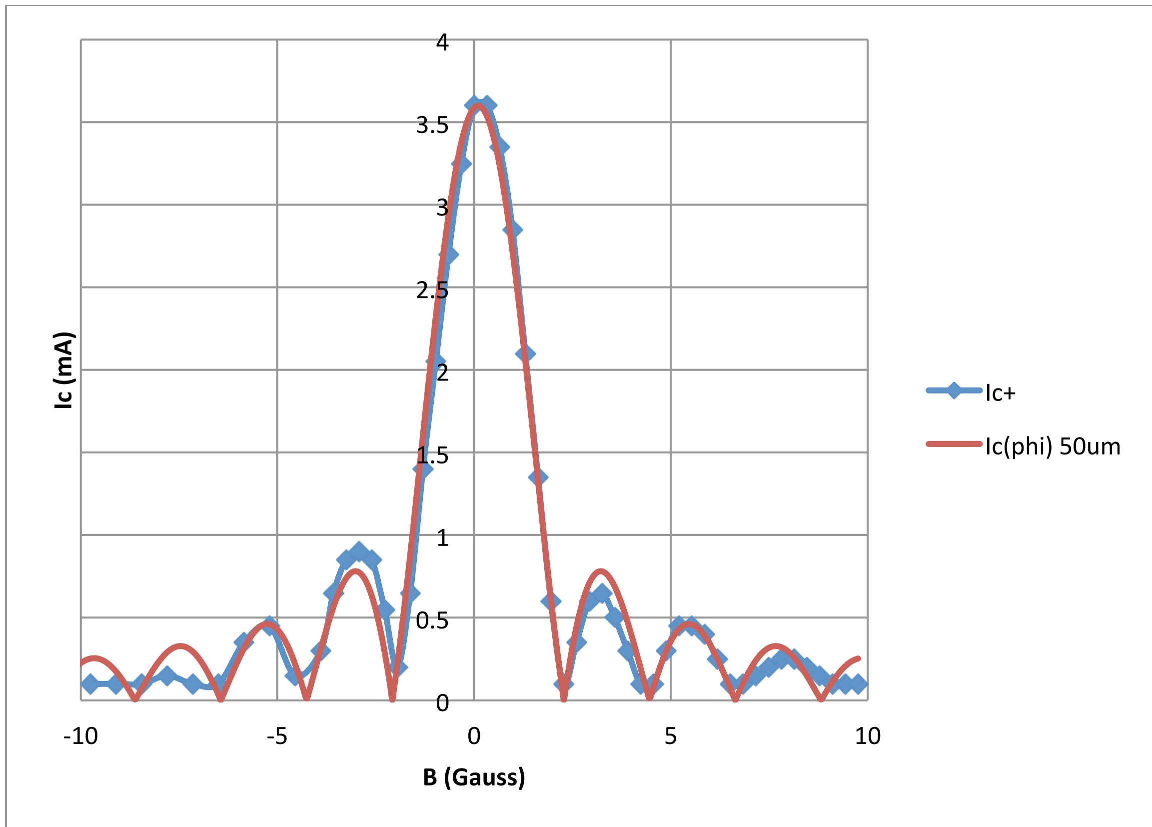


Figure 5.4. Magnetic field dependence of critical current for junction A2 and its theoretical fitting (Penetration depth λ=95 nm was used for fitting)

Annealing these junctions in forming gas up to 250 °C reduces the junction resistance. As discussed before, we attribute this to the diffusion of oxygen within the Hf oxide barrier layer. The increase of junction resistance at 300 °C should be because the oxygen diffusion through the top Nb layer. [14]

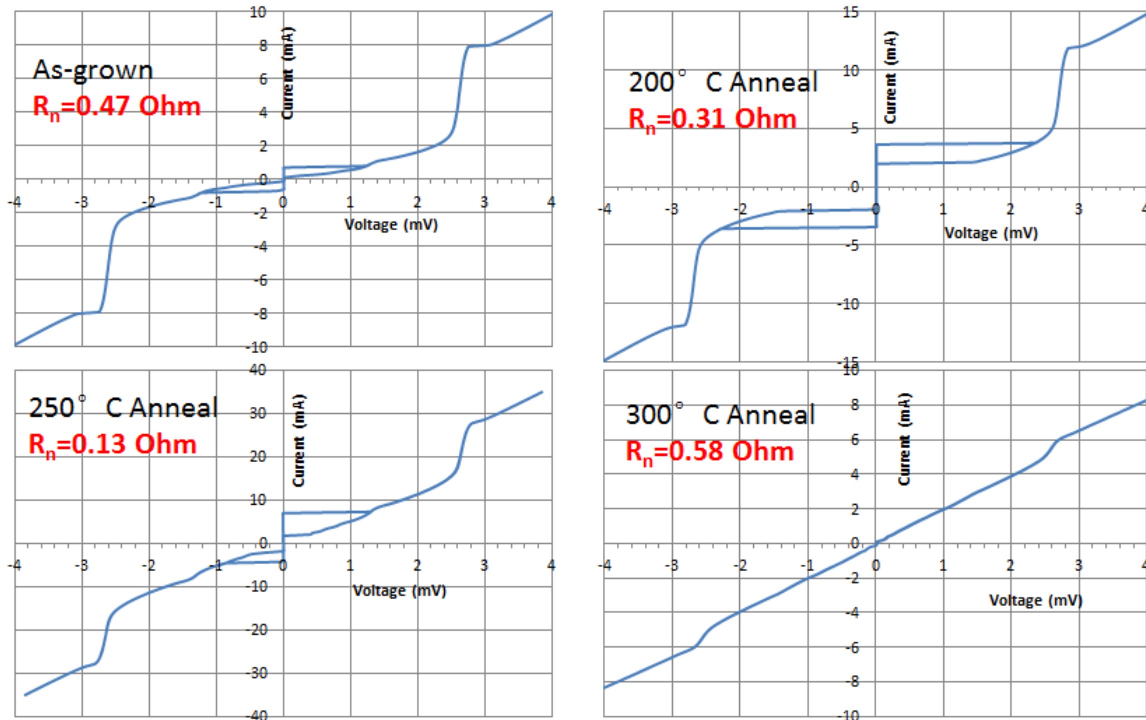


Figure 5.5. I-V characteristics of junction A2 after annealing at different temperatures

According to TEM image, Hf oxide formed with oxidation condition above has about 0.8nm thickness. Junctions with 3nm of Hf metal (minimum for good coverage) show a decrease of junction resistance, i.e. increase of critical current, after 200-250 °C annealing.

The increase of critical current after 200-250 °C annealing was also observed by S. Morohashi, et al. [44] In Figure 5.6, TEM images of trilayer structure show that the oxygen of the Hf oxide barrier diffuses into the excess Hf metal in an annealed sample (during top Nb deposition at 300 °C), comparing with an as-grown room temperature sample. A junction with top Nb deposited at 300 °C was found to be a short.

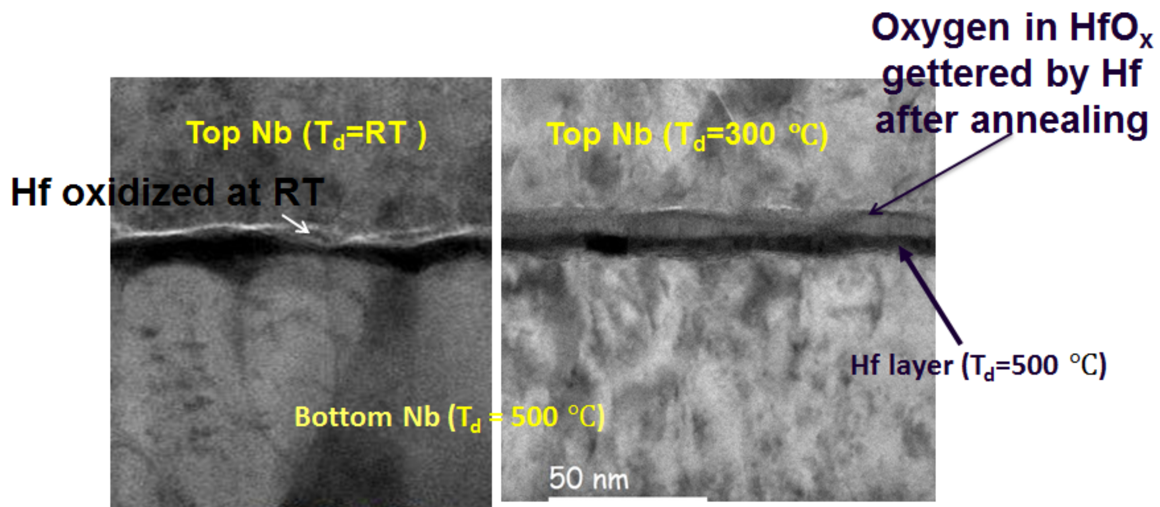


Figure 5.6. TEM images of Nb/Hf-HfO_x/Nb junction structures: left figure: Nb/Hf-HfO_x/Nb structure with 9 nm thick Hf as-grown, and right figure: the same structure was heated to 300 °C during top Nb deposition. The junction in the left figure shows tunneling and junction in the right figure is a short although it has a smoother layer. The grey colored layer below the top Nb should be the HfO_x layer formed by oxygen diffusion.

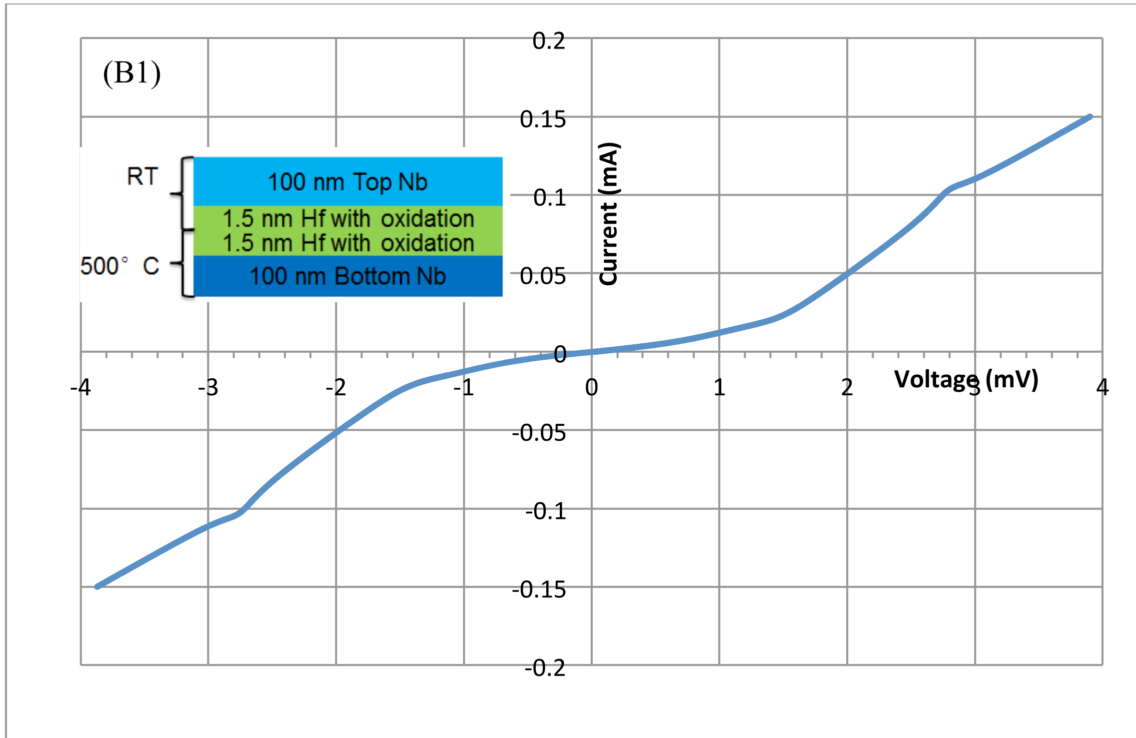
5.4 Junctions with multiple Hf oxide layers as barrier

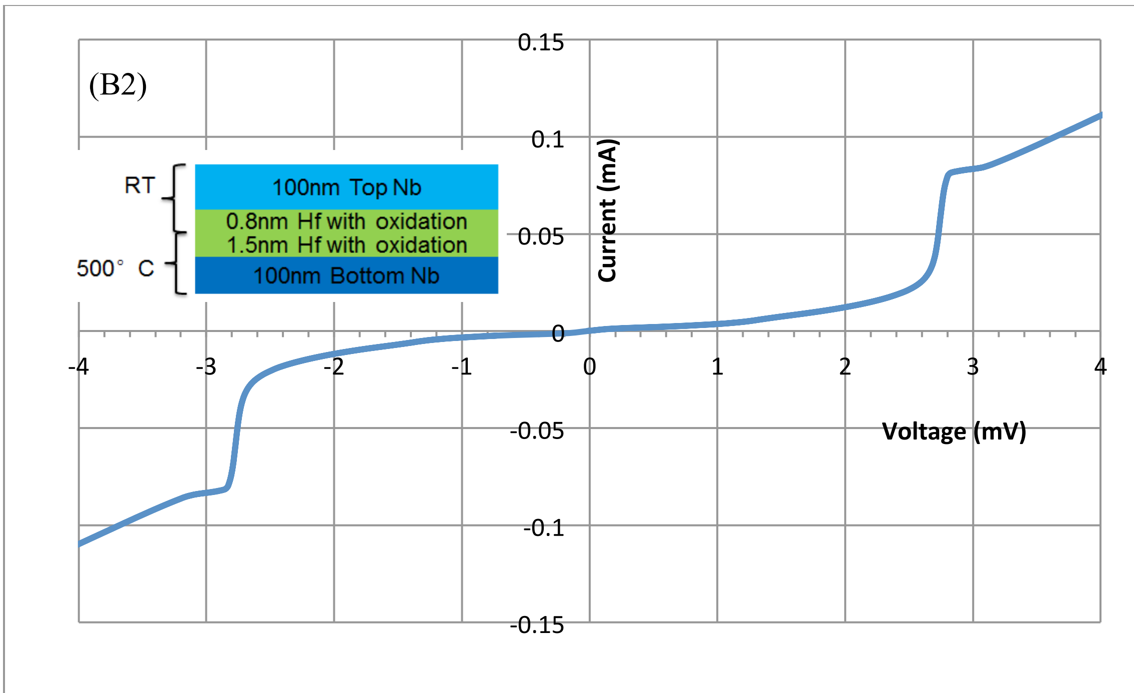
As mentioned in 1.6, the ideal structure of a thermally stable Josephson junction will consist of Nb electrodes and a pure Hf oxide barrier, without excess Hf metal. To solve this problem, we want to minimize the thickness of the excess Hf layer. But according to ref. 48, a Nb electrode will require a certain thickness of metal over layer for full coverage. From previous results, the Hf thickness needs to be more than 2 – 3 nm to cover the 100 nm Nb bottom electrode. However, this is more than the Hf thickness to be naturally oxidized, and excess Hf will cause the problem mentioned before: a suppressed gap by proximity effect, and oxygen gettering from the oxide layer by the excess Hf metal.

So a multiple deposition-oxidation process was employed, to increase the amount of oxidation in the whole Hf layer, and reduce the thickness of excess Hf metal, with the same coverage. The junction B1 has a barrier consisting of two 1.5 nm Hf layers, each oxidized in 20 Torr oxygen for 3 minutes, and junction B2 has one 1.5 nm plus one 0.8 nm Hf layer with the same oxidations. Junction B3 has four 0.6 nm Hf layers with the same oxidation of each.

For junction B1, a double gap-rise feature shows that the junction is separated into two NIS junctions in series to some extent. The resistance of the junction almost does not change after 200 °C and 250 °C annealing, compared to the junction with one 3nm Hf layer and oxide barrier. In junction B2, the reduced Hf layer gives one sharp gap, indicating the thickness of the Hf oxide is around 0.8 nm. Junction B3 has the largest

resistance and highest gap, with almost no "knee" feature, meaning it has very limited proximity layer. The subgap current is also quite large, maybe because a contaminated proximity layer and interface.




(B2)
RT
500° C
100nm Top Nb
0.8nm Hf with oxidation
1.5nm Hf with oxidation
100nm Bottom Nb
Current (mA)
Voltage (mV)
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-4
-3
-2
-1
0
1
2
3
4

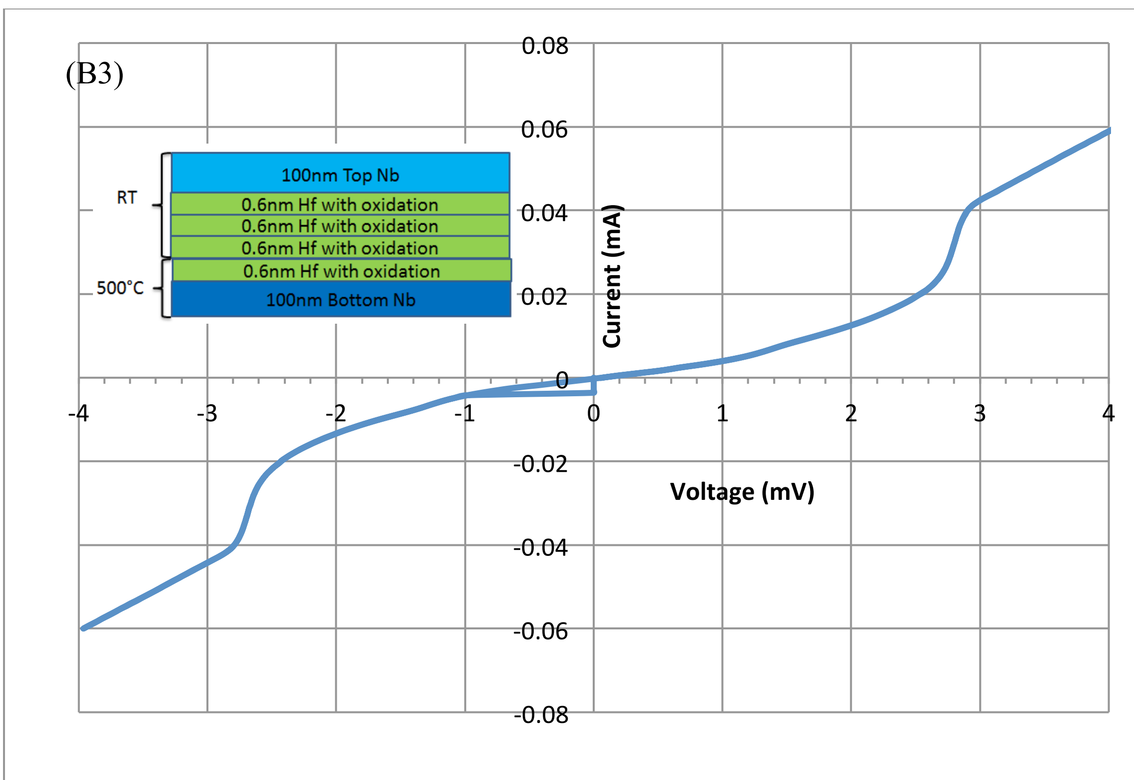

(B3)
RT
500°C
100nm Top Nb
0.6nm Hf with oxidation
0.6nm Hf with oxidation
0.6nm Hf with oxidation
0.6nm Hf with oxidation
100nm Bottom Nb
Current (mA)
Voltage (mV)
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
-4
-3
-2
-1
0
1
2
3
4

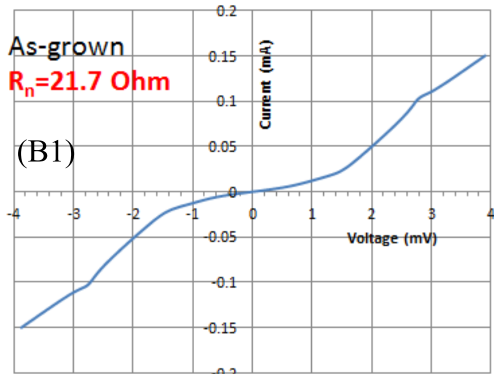
Figure 5.7. I-V characteristic of Nb/Hf-HfO_x/Nb junctions B1 – B3 at 4.2 K:

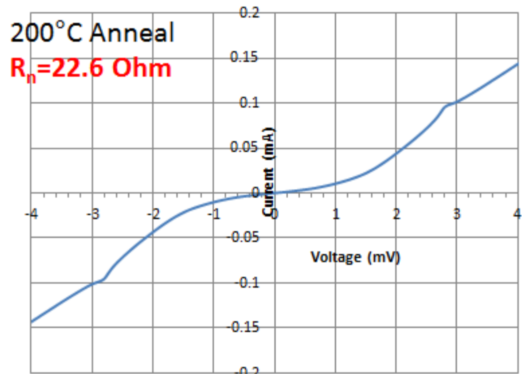
(B1) 1.5 nm thick Hf + 1.5 nm thick Hf (#NHN49), 20 μm × 20 μm size, gap = 2.6 meV, and there is also a rise at 1.4 meV, R_n=21.7 Ohm;

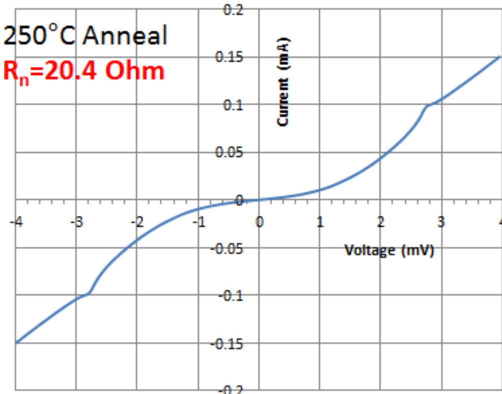
(B2) 1.5 nm thick Hf oxidized + 0.8 nm thick Hf (#NHN51), 20 μm × 20 μm, gap = 2.76 meV, R_n = 32.6 Ohm;

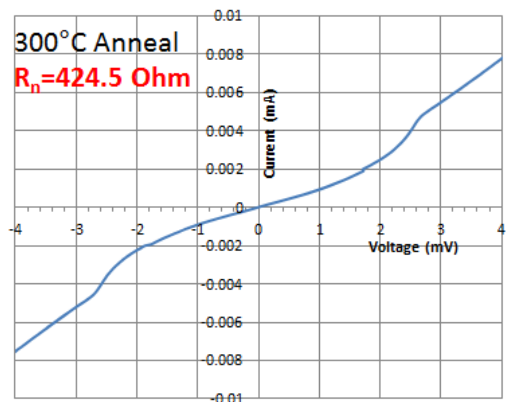
(B3) 0.6 nm thick Hf oxidized × 4 (#NHN53), 20 μm × 20 μm, gap = 2.8 meV, R_n = 61.4 Ohm;

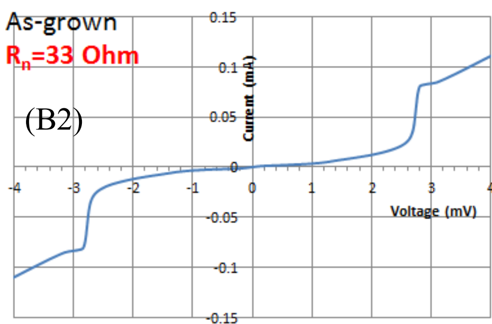
There is no critical current observed in these junctions, due to the weak Josephson coupling between the two electrodes. Both B1 and B2 junctions have their annealing stability improved than the single oxide junctions. Annealing of junction B2 to 250 °C actually increases the junction resistance, which could be from the oxygen diffusion from the surface oxide of top Nb electrode.

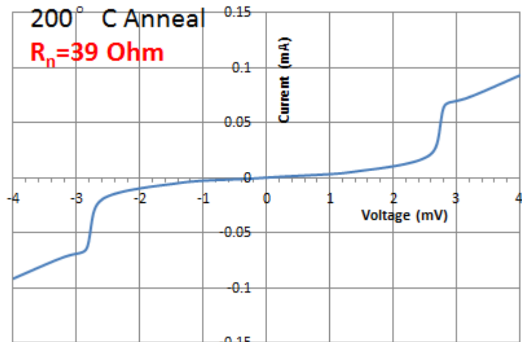

As-grown
Rn=21.7 Ohm
(B1)
Current (mA)
Voltage (mV)

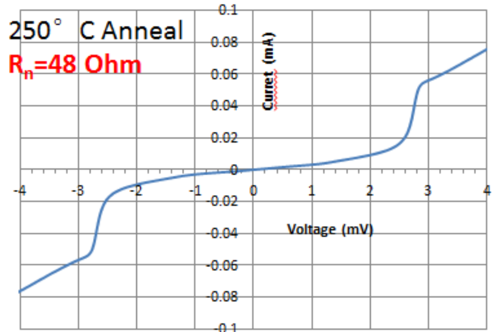

200°C Anneal
Rn=22.6 Ohm
Current (mA)
Voltage (mV)


250°C Anneal
Rn=20.4 Ohm
Current (mA)
Voltage (mV)


300°C Anneal
Rn=424.5 Ohm
Current (mA)
Voltage (mV)


As-grown
Rn=33 Ohm
(B2)
Current (mA)
Voltage (mV)


200° C Anneal
Rn=39 Ohm
Current (mA)
Voltage (mV)


250° C Anneal
Rn=48 Ohm
Curret (mA)
Voltage (mV)

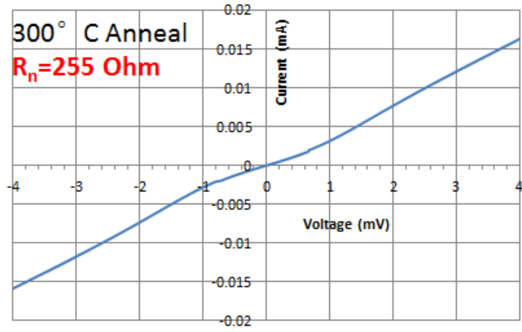
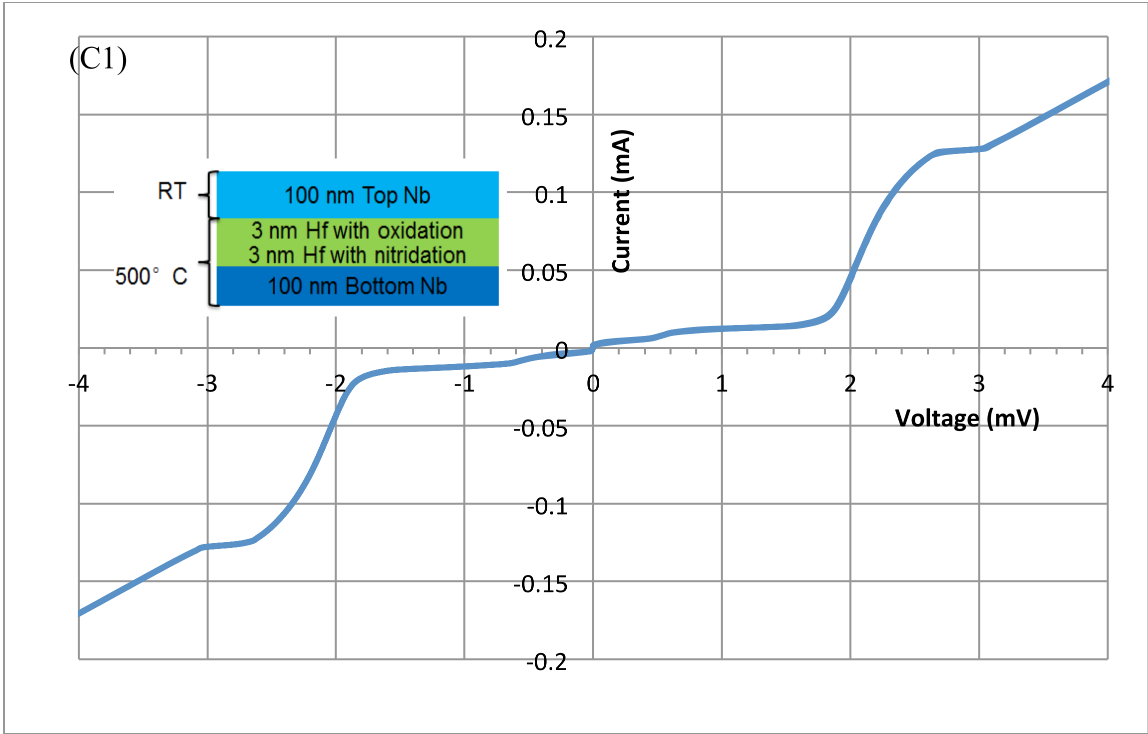

300° C Anneal
Rn=255 Ohm
Current (mA)
Voltage (mV)

Figure 5.8. I-V characteristics of junction B1 and B2 after annealing at different temperatures

5.5 Junctions with Hf oxide barrier and a Hf nitride buffer layer

A Hf nitride buffer layer was introduced as a diffusion barrier by Hasuo. [36] The Hf nitride layer is added to reduce the grain boundary diffusion between the Nb and Hf layers. In this work, a Hf nitride layer is formed by exposing the Hf layer in a nitrogen ECR plasma at 1.5×10^{-4} Torr at elevated temperature. Electrical tests show that the nitride layer is not insulating, but has higher resistance than pure metal. Junctions made with only a Hf nitride layer are shorts, so an oxide layer is necessary for making tunneling junction.

In junction C1 and C2, the Hf nitride buffer layer was kept 3 nm and 1.5 nm thick respectively. Another 3 nm Hf layer was sputtered and oxidized on top of this nitride layer. In these junctions, subgap leakage current is reduced and the gap value is also reduced by this additional Hf nitride barrier.


(C1)
RT
500° C
100 nm Top Nb
3 nm Hf with oxidation
3 nm Hf with nitridation
100 nm Bottom Nb
Current (mA)
Voltage (mV)
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-0.15
-0.2
-4
-3
-2
-1
0
1
2
3
4

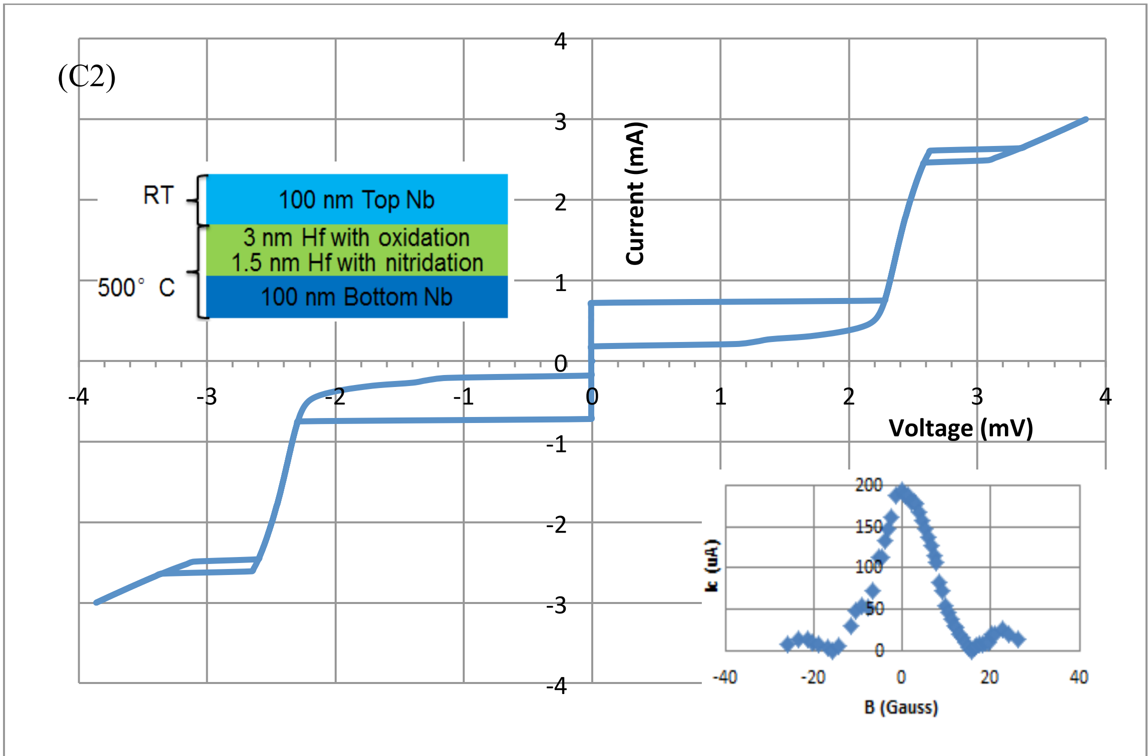
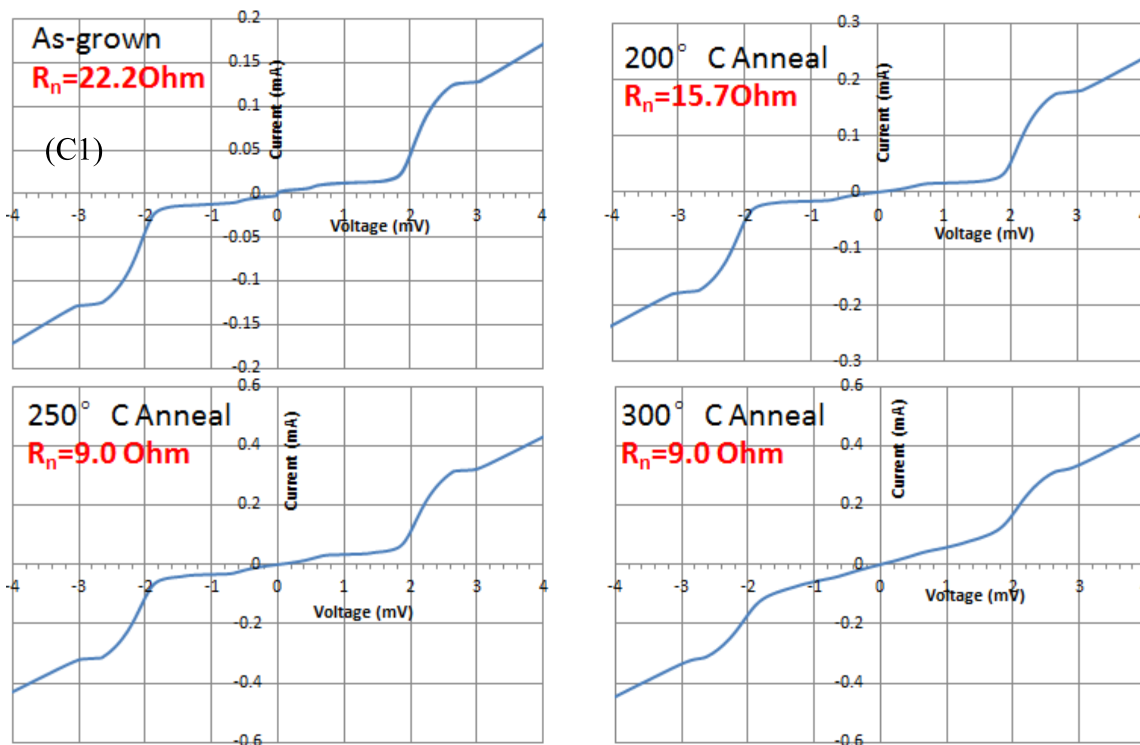

(C2)
RT
500° C
100 nm Top Nb
3 nm Hf with oxidation
1.5 nm Hf with nitridation
100 nm Bottom Nb
Current (mA)
Voltage (mV)
4
3
2
1
0
-1
-2
-3
-4
Ic (uA)
B (Gauss)
200
150
100
50
0
-40
-20
0
20
40

Figure 5.9. I-V characteristic of $Nb/HfN_x/Hf-HfO_x/Nb$ junctions C1 and C2 at 4.2 K:

(C1) 3 nm thick Hf nitride + 3 nm thick Hf oxidized (#NHN46), 10 µm × 10 µm size, gap = 2.0 meV, R_n=22.2 Ohm; Note the onset of gap is reduced but the knee feature is similar to other junctions;

(C2) 1.5 nm thick Hf nitride + 3 nm thick Hf oxidized (#NHN50), 5 µm × 5 µm, gap = 2.4 meV, R_n = 1.4 Ohm, magnetic field dependence of I_c also shows Fraunhofer pattern;



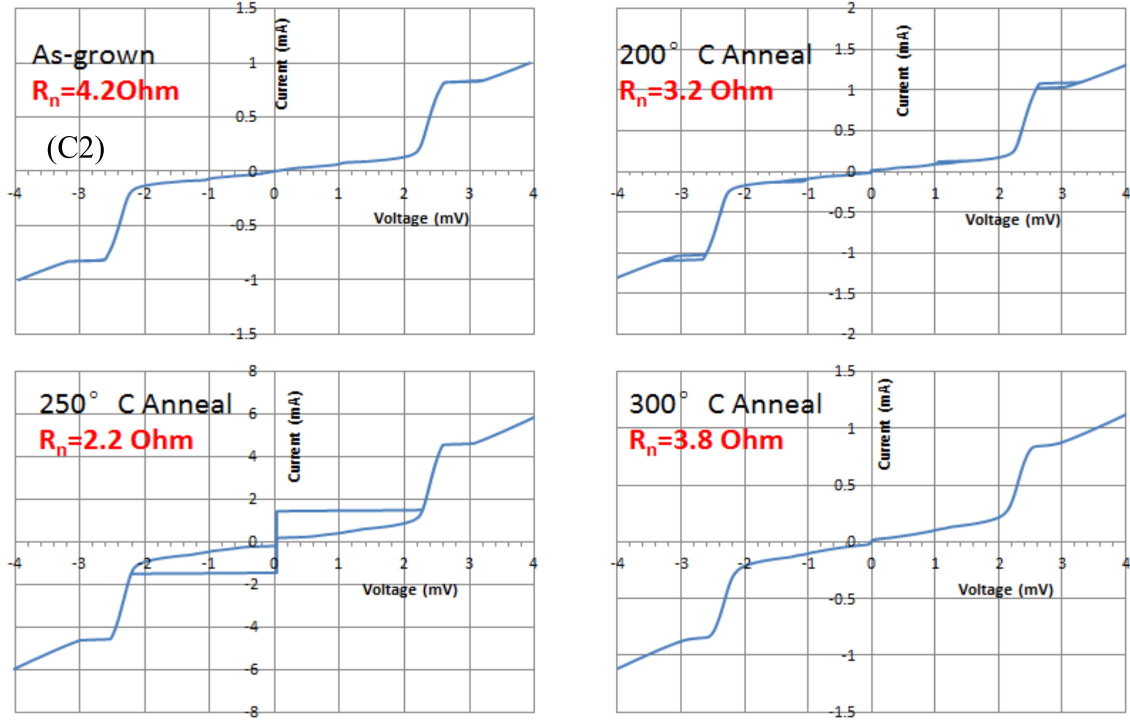


Figure 5.10. I-V characteristics of junction C1 and C2 after annealing at different temperatures

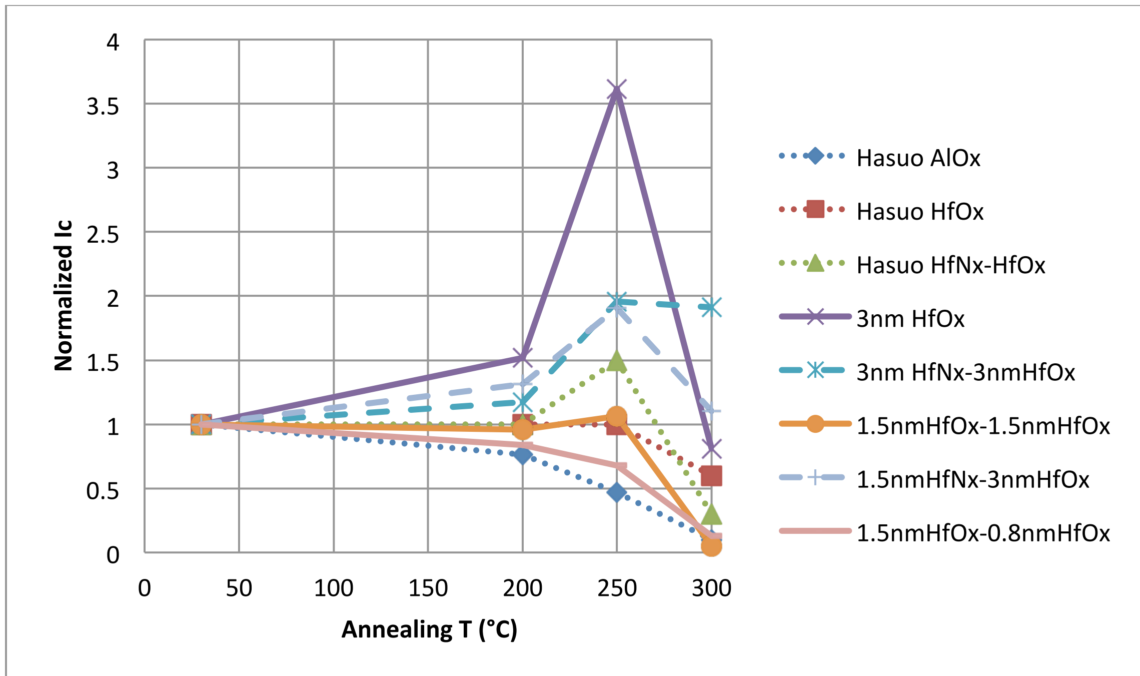


Figure 5.11. Annealing summary of junctions above (I_c =0.7 * $I_{(V=3mV)}$ derived from quasi-particle tunneling)

The results are summarized in Figure 5.11. One of the objectives for this research is to synthesis the whole junction trilayer at elevated temperatures. However, so far when the top Nb is sputtered at 200 °C or above, the junctions are all shorted. And it happens to junctions with both the HfO_x barrier only and the barrier with nitride diffusion layer. This could be caused by oxygen diffusion of the oxide barrier during the deposition process of the top Nb electrode.

5.6 Discussions of oxygen diffusion during annealing process

The increase of the resistance and decrease in I_c after 300°C annealing has been attributed to oxygen contamination in the Nb electrodes diffusing to the barrier, making the barrier thicker. This was first reported by T. Shiota. [18]

Most of the oxygen could be initially in the Nb surface oxide at the top surface of the junction. In our experiments using forming gas anneals, this could explain the increased tunneling resistance observed, even though the thermal treatments were performed in a reducing environment.

To prevent this, an oxygen diffusion barrier could be deposited on the top surface of the junction. For example, a thin layer of gold, or plasma treatment of top Nb to form Nb nitride can serve this purpose, as reported in ref. 18.

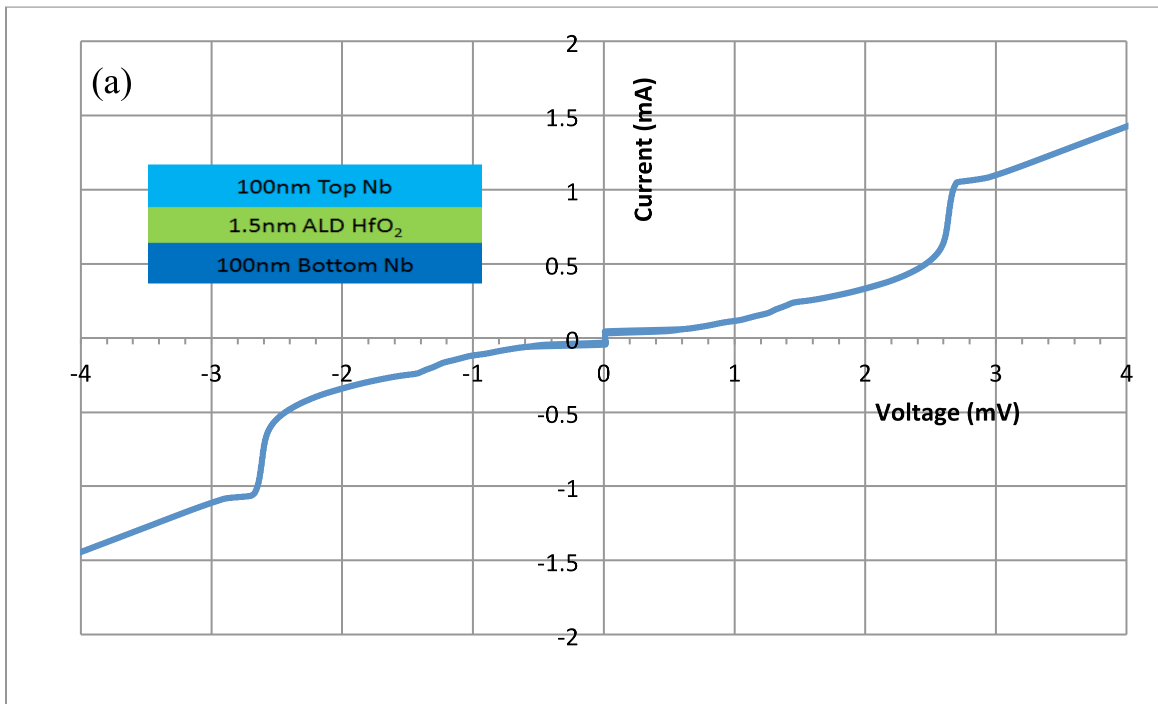
Figure 5.12. Junction structures with and without oxygen diffusion barrier.

The oxygen could also come from the oxygen in the Si or sapphire substrate. As mentioned before in Figure 4.3, SIMS shows that Al in sapphire starts diffusing through bottom Nb when Nb was grown at > 600 °C, but this process could start earlier.

5.7 Junction with ALD HfO_2 as barrier

According to the phase diagram, Nb-based junction with a HfO_2 barrier layer and no excess Hf metal would be thermally stable. So instead of oxidizing Hf, we attempted to grow HfO_2 by the ALD method. Because for now, ALD growth is done in CSSER's cleanroom, we were not able to make in-situ ALD Hf oxide barrier with Nb electrode. In the ALD HfO_2 junctions, the bottom Nb has a surface oxide before the ALD Hf oxide was grown.

Junctions with a barrier of 3 nm HfO_2 have shown high impedance so we reduced the thickness to 1.5 nm with 15 cycles. I-V measurement indicates a tunneling characteristic, but with higher leakage current than in some of the previous junctions.



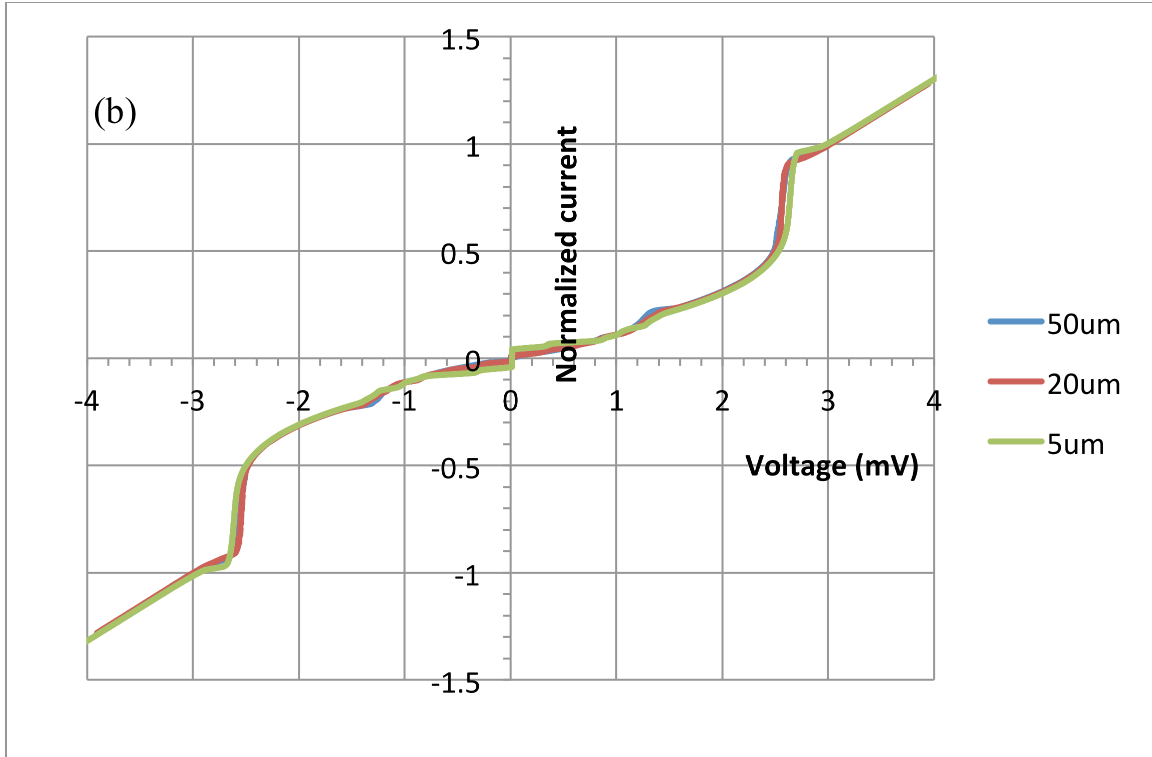


Figure 5.13 (a) I-V characteristic of Nb/ALD-HfO_2/Nb junction (#15Si) at 4.2 K: 5 µm × 5 µm size, gap = 2.61 meV, R_n=3.0 Ohm; (b) Three junctions on the same chip shows the almost same I-V characteristic after normalization, indicating the subgap current is not due to a few shorts, but some dirty density of state or many uniformly distributed nano-shorts.

Annealing was performed to 250 °C and the I-V curve was degraded after annealing as shown in Figure 5.14. The junction resistance dropped from 3 Ohm to 0.36 Ohm and the gap value reduced from 2.61 meV to 2.0 meV. The interesting part is the gap rise also become sharper. The surface oxide of bottom Nb may lead to these effects. The non-stable Nb oxide, which increases junction resistance, diffused after annealing.

On the other hand, the reduction of this interface oxide cleans the interface, so that the gap rise becomes even sharper, although there is more leakage current now. Further annealing up to 300 °C leads to a short in the junction.

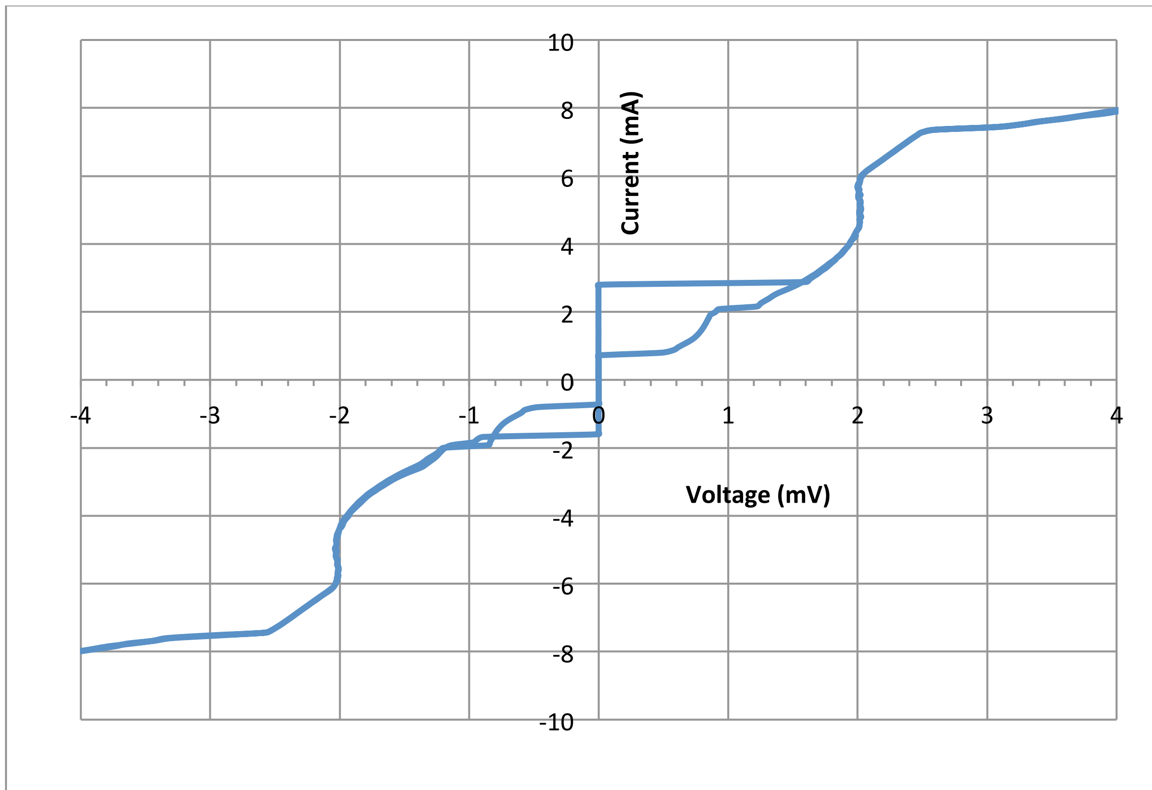


Figure 5.14. I-V characteristic of ALD-1.5nm junction after 250 °C annealing, R_n=0.36 Ohm, gap reduced to 2.0 mV but became sharper

In an RBS study of these trilayer films, we could not fit the Hf and O peak to within experimental error using only those elements in the analysis. This suggests the presence of other contamination, presumably organic impurities. Annealing the wafer in

forming gas was performed after each ALD growth to remove these impurities, although no significant improvement in the junction properties was observed.

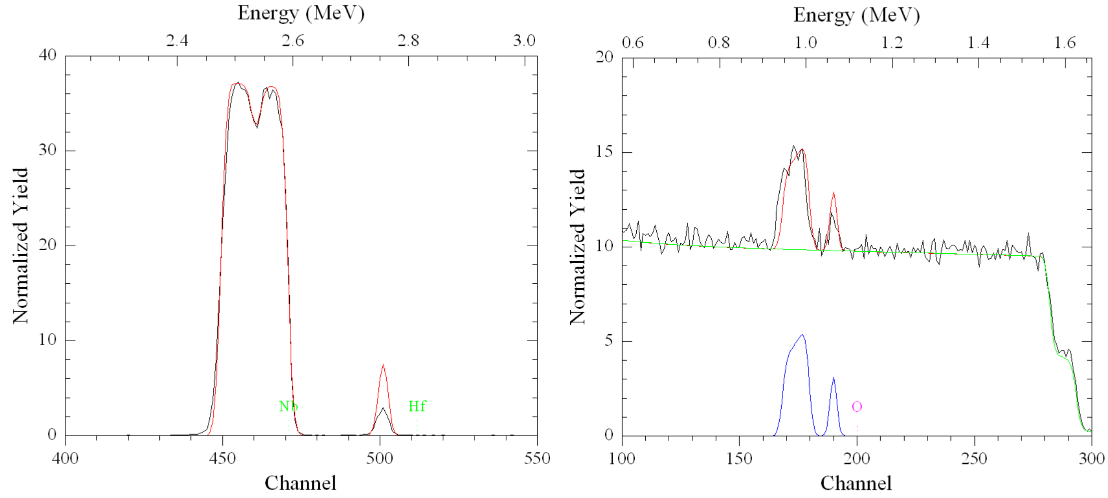


Figure 5.15. Mismatch in Hf and O peak of RBS between experimental data and theoretical fitting in ALD HfO_2 junction layers

5.8 Gap suppression and coherence length calculation

The sumgap of Hf barrier junctions at 4.2K is smaller than theoretical value $2\Delta(\text{Nb}, T=4.2\text{ K}) = 2.9$ meV. When Hf is 6 nm thick (including oxide layer) the sumgap is 2.2 mV. When Hf is 3nm thick, sumgap is 2.6 mV. The gap value is taken where the half gap-rise is. Assuming the Hf surface oxide layer is 0.8 nm thick, we can get the Figure 5.16.

Table 5.1. Gap suppression of junctions with different Hf and Hf nitride thickness

Hf thickness (nm)	Hf nitride thickness (nm)	Sumgap (meV)	Supressed single gap (meV)	Percentage of full gap value Δ/Δ_0
0	0	2.9	1.45	1.00
2.2	0	2.6	1.15	0.79
5.2	0	2.25	0.8	0.55
2.2	3	2.2	0.75	0.52
2.2	1.5	2.4	0.95	0.66

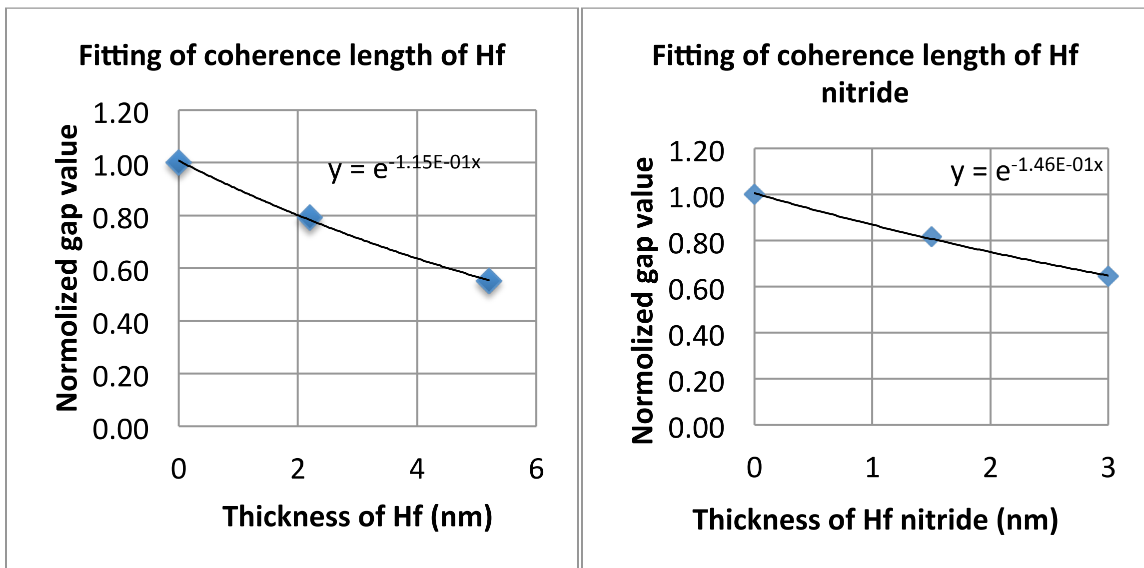


Figure 5.16. Fitting of coherence length of Hf and Hf nitride

According to the fitting equation $\Delta/\Delta_0=e^{-x1/\xi(Hf)-x2/\xi(HfN)}$, where x1 is the thickness of the Hf metal, x2 is the thickness of the Hf nitride layer, Δ is the reduced gap by the Hf proximity layer, and Δ_0 is the energy gap of Nb at 4.2 K, which should be 1.45 meV. [5]

By fitting the data, we can get the coherence length ξ(Hf) is 8.7 nm and ξ(HfN) is 6.8 nm.

To confirm this coherence length value, we measured the resistivity ρ=76 μΩ.cm for the Hf metal film at 4.2 K by four-point dipping measurement; indicating that the mean free path (mfp) is about 0.8nm and coherence length $\xi = \sqrt{\hbar v_F l_n / 6\pi k_B T}$ =11.1 nm [5] [45] This is comparable with the theoretical data from mfp measured by dipping measurement.

Table 5.2. Summary for Hf oxidation and barrier height

Hf thickness	Oxidation (Torr.minute)	Barrier height (eV)
4 nm	6000	0.77
3 nm	60	0.35
3 nm	6000	0.64
3 nm + 3 nm HfN_x	60	0.85
3 nm + 1.5 nm HfN_x	60	0.71

5.9 Discussions about junction barrier height

By fitting the conductance-voltage (G-V) characteristics up to 150 mV using the Simmons-Rowell model, [25] we found that the inferred HfO_x barrier height is 0.85 eV formed in 200 Torr oxygen for 30 minutes. There is some variation of the barrier height with different oxidation exposure and HfN_x diffusion barrier formed by ECR plasma, with similar 2 - 3 nm thickness. The highest barrier fitting (0.85 eV) is shown in Figure

12. Given the long oxygen exposure, this is significantly less than the reported 1.4-1.5 eV barrier found for AlO_x. [26] A smaller barrier height will allow a thicker barrier for the same critical current junction. Since the zero-bias tunneling resistance is proportional to $e^{-\varphi/kT}$ according to the WKB approximation, then the thickness of HfO_x can be ~1.7 times that of AlO_x for a given critical current. Taking into account the additional thickness and almost 3 times higher dielectric constant of HfO_2 over Al_2O_3, we expect about a 20% reduction in the Josephson frequency for a given and J_c, and thus maximum switching speed from that of the AlO_x barrier junction. The thicker barrier may be advantages for insuring better coverage.

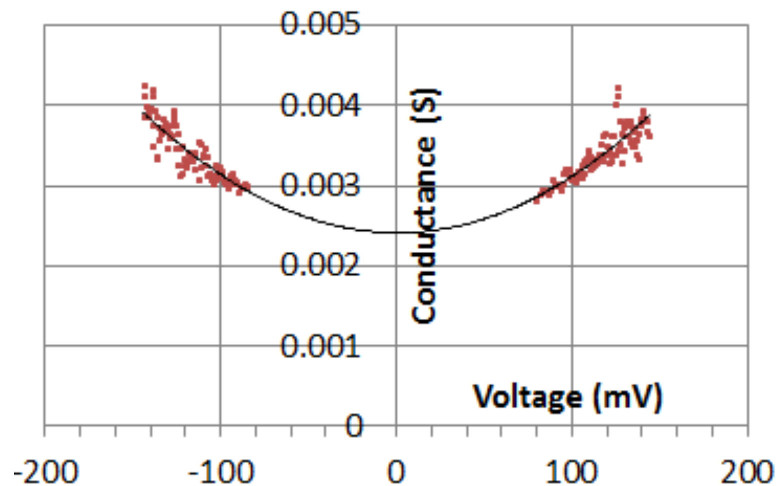


Figure 5.17. A sample of junction barrier height fitting

5.10 Discussions about larger subgap current of HfO_x junctions

In this work, the Nb tunnel junctions with Hf oxide are found to have subgap currents that are much larger than expected from thermal excitations. The commonly-

used and currently-available Nb/Al-AlO_x/Nb trilayer junctions can have properties very near the ideal, even down to relatively low temperature. In our junctions with the smallest subgap current, the characteristics are highly non-linear and there is little current observed at voltages below 1 mV. Furthermore, the critical current can be suppressed to within 5% of the maximum value even to the 3rd minima in the Fraunhofer pattern, indicating relatively good uniformity on the length scale of a fraction of the junction size. This is evidence that there are no large SNS-type shorts between the two electrodes. From this, we conclude that the large subgap current (particularly at > 1mV) is mainly due to a smeared density of states in the superconductor order parameter or within a few coherence lengths from the junction. The subgap (quasi-particle) tunneling current "samples" the gap within a few coherence lengths. Since we consistently observe much lower I_c than expected in these junctions and not to the same extent in other junctions with similar I_c and R_n, we suggest that the reduced I_c is because of the suppression of the order parameter at the barrier interface. Comparing multiple measurements on these and similar junctions is necessary to rule out the effects of flux trapping and environmental noise on the results.

5.11 Summary and conclusions

Our measurement system was qualified with standard commercial samples, and our junction fabrication process was proved to be effective with commercial wafers. Similar to the Nb/Al-AlO_x/Nb junctions, Nb/Hf-HfO_x/Nb junctions with bottom electrode

+ proximity layer grown at 500 °C and the oxidation + top Nb electrode grown at room temperature show good tunneling IV characteristics. After 200-250 °C annealing, the normal junction resistance dropped due to oxygen in the barrier being gettered by excess Hf metal. Multiple oxidation steps reduced the proximity layer and improved annealing stability. The use of HfN_x as a diffusion barrier between the Nb and the Hf proximity layer results in improved annealing stability. The ALD method was used to synthesize HfO_2 barrier as an initial study and we have got tunneling results. Due to the ex-situ growth of the ALD barrier layer, the junction quality was not as good as expected.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

We have initiated a study to explore using Hf as a proximity layer and HfO_2 as a barrier for Nb-based Josephson junction, because of their refractory nature, their demonstrated ability to produce flat and stable interfaces with Nb and to form thermally stable junctions. The Nb-Hf-O ternary phase diagram indicates that Nb is thermodynamically stable against HfO_2 below 1000°C. To synthesize a Josephson junction metal barrier with Nb grown at 500 °C, HfO_2 is a good candidate as the barrier for making thermally stable Josephson junctions for future superconductor digital circuit technology. From the prediction of phase diagram, Nb/HfO_2/Nb junctions without excess Hf are thermodynamically stable.

Nb and Hf thin films were made by DC sputtering. Nb thin films were characterized for the best growth condition for Josephson junction electrodes. The characterizing tools were used, including XRD, RBS, AFM, AES, TEM and dipping measurements for topological, structural and electrical properties of the films. 500 °C substrate temperature, 6 mTorr Ar pressure and 180 Watt of sputtering power were combined to produce the smoothest and best Nb thin film. Hf wets Nb well at 500 °C and Al does not even wet Nb at 50 °C. The Nb-Hf bilayer interface was abrupt up to 400 °C and diffusion of the Nb-Al interface starts above 140 °C. TEM and AES study shows that oxygen in a HfO_x barrier diffuses into excess Hf layer.

A junction fabrication process was successfully developed in our own group and proved to be reliable. Measurement system was also qualified by testing commercial devices. Nb/Hf-HfO_x/Nb Josephson junctions with bottom electrode + proximity layer grown at 500 °C and oxidation + top Nb electrode grown at room temperature show good tunneling IV characteristics, with sharp sumgap up to 2.72 meV and scaling normal resistance across the wafer. After 200-250 °C annealing, the junction resistance dropped due to oxygen in the barrier being gettered by excess Hf metal. Multiple oxidation steps reduced the proximity layer and improved annealing stability. The use of HfN_x as diffusion barrier between the Nb and the Hf proximity layer results in improved annealing stability. The ALD method was used to synthesize HfO_2 barrier as an initial study, and we have got tunneling results. Due to the ex-situ growth of ALD barrier layer, the junction quality was not as good as expected.

In this work, we investigate whether higher temperature growth temperatures can be used to produce HfO_2 barrier Josephson junctions with improved thermal stability and properties. The following experiments can be carried out in the future.

6.1 Material growth

The natural surface oxide of ex-situ grown Nb will degrade the interface between barrier and electrodes. In-situ ALD growth of Hf oxide with Nb electrode could be possibly achieved by collaborating with Prof. Nemanich group's MBE system at ASU Physics Department. The Nb will be deposited by e-beam evaporation and ALD growth

will be plasma assisted. By growing Hf oxide in-situ, the quality of the junction is expected to be improved.

6.2 Fabrication process

The anodization along with sputtered Si oxide has shown they are good for deposition. The current mask design could also be improved so that the wafer area could be utilized more efficiently. Size of junction contact pads could be reduced and more junction lines could be used with different options. E-beam lithography could be used in case sub-micron size junction will be needed.

6.3 Material characterization

Auger Electron Spectroscopy has proven that it is a good way of characterizing oxygen diffusion after the annealing process within trilayer structures. ALD Hf oxide can be studied with the same way and compared to the oxidized Hf layers. The state-of-the-art TEM system at ASU can also provide studies on Hf junction samples with and without annealing to prove oxygen diffusion within the Hf layer with more details.

Cross-section XPS and EELS study in TEM can be adopted to characterize the oxygen distribution on a line or in an area of the sample. Due to the thickness of the specimen being around 30 nm, the transmission signal of the oxygen varies from surface roughness, this result could be used only as a reference.

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BIOGRAPHICAL SKETCH

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