Electromigration in Gold Interconnects

by

Stephen Kilgore

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved November 2013 by the
Graduate Supervisory Committee:

James Adams, Co-chair
Dieter Schroder, Co-chair
Craig Gaw
Stephen Krause

ARIZONA STATE UNIVERSITY

December 2013

ABSTRACT

Electromigration in metal interconnects is the most pernicious failure mechanism in semiconductor integrated circuits (ICs). Early electromigration investigations were primarily focused on aluminum interconnects for silicon-based ICs. An alternative metallization compatible with gallium arsenide (GaAs) was required in the development of high-powered radio frequency (RF) compound semiconductor devices operating at higher current densities and elevated temperatures. Gold-based metallization was implemented on GaAs devices because it uniquely forms a very low resistance ohmic contact and gold interconnects have superior electrical and thermal conductivity properties. Gold (Au) was also believed to have improved resistance to electromigration due to its higher melting temperature, yet electromigration reliability data on passivated Au interconnects is scarce and inadequate in the literature. Therefore, the objective of this research was to characterize the electromigration lifetimes of passivated Au interconnects under precisely controlled stress conditions with statistically relevant quantities to obtain accurate model parameters essential for extrapolation to normal operational conditions.

This research objective was accomplished through measurement of electromigration lifetimes of large quantities of passivated electroplated Au interconnects utilizing high-resolution in-situ resistance monitoring equipment. Application of moderate accelerated stress conditions with a current density limited to 2 MA/cm^2 and oven temperatures in the range of 300°C to 375°C avoided electrical overstress and severe Joule-heated temperature gradients. Temperature coefficients of resistance (TCRs) were measured to determine accurate Joule-heated Au interconnect film temperatures.

A failure criterion of 50% resistance degradation was selected to prevent thermal runaway and catastrophic metal ruptures that are problematic of open circuit failure tests. Test structure design was optimized to reduce resistance variation and facilitate failure analysis. Characterization of the Au microstructure yielded a median grain size of 0.91 μm. All Au lifetime distributions followed log-normal distributions and Black's model was found to be applicable. An activation energy of 0.80 ± 0.05 eV was measured from constant current electromigration tests at multiple temperatures. A current density exponent of 1.91 was extracted from multiple current densities at a constant temperature. Electromigration-induced void morphology along with these model parameters indicated grain boundary diffusion is dominant and the void nucleation mechanism controlled the failure time.

This dissertation is dedicated to Professor Dieter Schroder and Charles Varker for inspiring an inquisitive and disciplined erudition in semiconductor reliability.

ACKNOWLEDGEMENTS

First and foremost, I would like to express my sincerest appreciation for my doctoral advisor Professor Dieter K. Schroder for his guidance, timeless patience, and dedication during my graduate studies at Arizona State University. Dr. Dieter Schroder's work experience in the semiconductor industry and his desire to share his extensive knowledge were immensely important for this research. I want to express my gratitude to Professor James Adams for standing in as chair and providing guidance for completion of this dissertation in my final year. I am also very grateful for the support, guidance, and encouragement of my other doctoral committee members Professor Stephen Krause and Dr. Craig Gaw. Additionally, I would like to thank Professor Fernando Ponce for teaching me materials physics and for extending his kindness.

I express my utmost admiration and gratefulness to my former manager Charles Varker (Dan Noble Fellow) for his mentorship in semiconductor reliability physics while working at Motorola. It is a rare occurrence that a manager selflessly mentors in a hectic business environment, and therefore I am entirely indebted to Charles. It was through many years of technical discussions with Charles that I gained expertise in the field of metallization reliability. This dissertation research topic was inspired by my discussions with Charles Varker.

While working at Freescale Semiconductor (formerly Motorola) there have been several colleagues that have directly helped me and provided insight in the course of this research that deserve recognition. First, I want to recognize Darrell Hill and Haldane Henry for the gold interconnect test structure design support. I am very grateful to Adolfo Reyes for fostering a genuinely helpful attitude in supplying GaAs wafers that were tested in this electromigration study.

I express my gratitude to Phil Williams for teaching me real world statistics and for his persistent guidance with statistical software programs. In the support of the gold film characterization and failure analysis work, I express my thanks to Jake Schaper, Troy Clare, and Jake Hammet. Special thanks are extended to John Euler of QualiTau for his guidance and assistance with the electromigration equipment. I especially appreciate my friend Nick Rivette for his encouragement and diligence in developing data analysis macros. I want to thank Dr. Bishnu Gogoi, Dr. Jerry Nivison, and Dr. Gil Speyer for their friendship and review of this dissertation.

It is very important that I recognize my previous academic graduate mentors at the University of Illinois. I am greatly indebted to Dr. Mike Machesky, my master's advisor, for his exceptional mentorship that developed my scientific foundation upon which this doctoral graduate research was possible. I also want to recognize Dr. Tom Holm for his significant influence and guidance in publishing, especially for introducing me to the reference management software (EndNote) that was a beneficial aid for citing references in this dissertation. During this research, I have had several helpful discussions with Dr. Jim Lloyd on the theory of electromigration, with Professor Rolf Hummel on Au electromigration, and with Professor Paul Kohl on Au electrodeposition.

Most importantly, I sincerely express my love and affection for Lisa who has provided encouragement, patience, and assistance during the arduous time writing this dissertation while working full-time. I want to also thank my parents from whom I have learned self-reliance in my academic endeavors. It should be emphasized that writing this dissertation would have been an entirely lonely venture if not for my furry and steadfast companion Cinder.

TABLE OF CONTENTS

Page

LIST OF TABLES ix

LIST OF FIGURES x

CHAPTER 1 INTRODUCTION 1

1.1 Background and Motivation 1

1.2 Research Objectives 4

CHAPTER 2 ELECTROMIGRATION THEORY AND REVIEW 6

2.1 Electromigration Fundamentals and Theory 6

2.2 Electromigration in Interconnects 11

2.2.1 Microstructure and Geometric Effects 12

2.2.2 Alloying and Metallization Advancements 18

2.2.3 Reliability Measurement Methods 22

2.2.4 Failure Kinetic Models 25

2.3 Properties and Application of Gold Metallization 30

2.3.1 Properties of Gold 30

2.3.2 Application of Gold Metallization 34

2.4 Review of Electromigration in Gold Films 38

2.5 Gold Electromigration Review Summary 54

CHAPTER 3 EXPERIMENTAL METHODS 56

3.1 Test Structure Design 56

3.2 Gold Interconnect Fabrication 63

3.3 Assembly and Packaging 66

3.4 Electromigration Test System 70

3.5 Test Procedures and Methods 74

Page

3.6 Test Structure Cross-Sectional Measurements 81

3.7 Experimental Test Conditions 83

3.8 Statistical Methods and Data Analysis 86

3.9 Summary of Experimental Methods 92

CHAPTER 4 EXPERIMENTAL RESULTS 93

4.1 Interconnect Resistance Measurements 93

4.1.1 Metal 1 Test Structure Resistance 93

4.1.2 Via1 / Metal 1 Test Structure Resistance 99

4.2 Temperature Coefficient of Resistance and Film Temperature . 102

4.3 Resistance Degradation 108

4.4 Electromigration Lifetimes 112

4.4.1 Early Failures 112

4.4.2 Test Structure Lifetimes 116

4.5 Electromigration Activation Energy 119

4.6 Current Density Exponent 128

4.7 Gold Structure Characterization 132

4.7.1 Gold Microstructure Analysis 132

4.7.2 Gold Chemical Analysis 138

4.8 Failure Analysis 139

CHAPTER 5 DISCUSSION AND ANALYSIS 146

5.1 Structure Resistance Variation 146

5.2 Resistance Degradation Characteristics 150

5.3 Electromigration Activation Energy 159

5.4 Electromigration Current Density Exponent 167

Page

CHAPTER 6 CONCLUSIONS AND SUGGESTED FUTURE WORK 172

6.1 Summary of Electromigration in Gold Interconnects 172

6.2 Future Research Suggestions 175

REFERENCES 176

LIST OF TABLES

Table Page

Chapter 2

2.1 Atomic properties and crystal lattice of gold 30

2.2 Physical properties of gold compared to other conductor metals............ 31

2.3 Standard electrode potentials for common metals................................ 33

2.4 Required properties for metallizations in ICs 34

2.5 Summary of the solute effects on the Au film failure site 49

2.6 Au electromigration results for various experimental methods................ 55

Chapter 3

3.1 Experimental stress conditions for Au M1 test structures (phase V)....... 85

3.2 Experimental stress conditions for Au V1M1 test structures (phase V) .. 85

Chapter 4

4.1 Au M1 test structure reference resistances and TCRs 104

4.2 TCRs and film temperatures determined by both methods.................. 106

4.3 Normalized current density median Au electromigration lifetimes......... 131

4.4 ICP-OES analysis for trace elements within electroplated Au film 138

Chapter 5

5.1 Normalized Au M1 structure resistance mean and standard deviation . 148

5.2 Comparison of activation energies for Au electromigration.................. 164

5.3 Observed activation energies for various diffusion mechanisms 166

5.4 Comparison of current density exponents for Au electromigration........ 171

LIST OF FIGURES

Figure Page

Chapter 1

1.1 Operational current density trend for advancing technology nodes 2

1.2 Market revenue growth for GaAs devices 3

Chapter 2

2.1 Electric field forces acting upon metal atoms in a crystal lattice 8

2.2 Flux divergence at grain boundary triple points 12

2.3 Bamboo grained microstructure interconnect 14

2.4 Blech length effect demonstrated on Al thin film segments 15

2.5 Flux divergence at the W via / Al interconnect interface 17

2.6 Huntington and Grone's Au marker motion (*v* / *J*) versus 1 / T graph 39

2.7 Gangulee and d'Heurle's failure times versus inverse temperature 42

2.8 Blech and Kinsbron's Au thin film structure configuration 45

Chapter 3

3.1 NIST electromigration test structure schematic 57

3.2 A two-level metal via electromigration test structure illustration 58

3.3 Dual NIST line (2 µm wide by 800 µm long) test structures 59

3.4 Dual centered via (metal 1 / metal 2) test structures 60

3.5 Metal 1 line (2 µm wide by 450 µm long) test structure design 61

3.6 Via1 / Metal 1 (5 µm wide by 450 µm long) test structure design 61

3.7 Kelvin sensed test structure layout configuration 62

3.8 Semitool Equinox gold plating tool 64

3.9 Processing steps for the Au interconnect test structure formation 65

Figure Page

3.10 Sawn GaAs wafer mounted on UV tape 67

3.11 Ceramic side-brazed 20-pin dual in-line package 68

3.12 Au wirebond configuration diagram 69

3.13 QualiTau MIRA electromigration test systems 70

3.14 Oven socket boards (350°C board above / 400°C board below) 71

3.15 Oven socket boards loaded into oven backplane 72

3.16 QualiTau test system architecture block diagram 73

3.17 Standard method for TCR determination 77

3.18 Standard method for Joule-heated temperature determination 78

3.19 Two-current method for Joule-heated temperature determination 79

3.20 Au M1 test structure line-width and thickness measurements 81

3.21 Au V1M1 test structure line-width and thickness measurements 82

3.22 Log-normal failure distributions with different sigma and $t_{50\%}$ values 88

3.23 Bi-modal failure distribution with intrinsic and extrinsic failure modes 89

3.24 $\ln(t_{50\%})$ versus 1/kT data graph for extracting E_a parameter 90

3.25 $\ln(t_{50\%})$ versus $\ln(J)$ data graph for extracting n parameter 91

Chapter 4

4.1 Initial Au M1 test structure resistance distribution (phase II) 94

4.2 Screened Au M1 test structure resistance distribution (phase II) 95

4.3 Initial Au M1 test structure resistance distribution (phase V) 96

4.4 Illustration of metal interconnect line structure dimensions 97

4.5 Initial Au V1M1 test structure resistance distribution (phase II) 99

4.6 Initial Au V1M1 test structure resistance distribution (phase V) 100

4.7 Au M1 structure resistance versus oven temperature (phase V) 102

Figure Page

4.8 Au M1 (DUTs #1, 10, & 50) structure resistance versus temperature ... 103

4.9 Resistance degradation of Au M1 structures during electromigration ... 109

4.10 Resistance degradation of Au M1 structures with 10% scaled graph ... 111

4.11 Au electromigration lifetimes with a 10% failure criterion ... 113

4.12 Intrinsic failure distributions after removal of early failures ... 114

4.13 Au electromigration lifetimes with a 50% failure criterion ... 115

4.14 Au M1 and V1M1 test structure electromigration lifetimes ... 117

4.15 Electromigration lifetimes for the Au M1 structures (phase III) ... 120

4.16 Arrhenius plot of median Au M1 electromigration lifetimes (phase III) .. 121

4.17 Electromigration lifetimes for the Au M1 structures (phase IV) ... 122

4.18 Arrhenius plot of median Au M1 electromigration lifetimes (phase IV) . 123

4.19 Electromigration lifetimes for the Au M1 structures (phase V) ... 124

4.20 Arrhenius plot of median Au M1 electromigration lifetimes (phase V) ... 125

4.21 Electromigration lifetimes for the Au V1M1 structures (phase V) ... 126

4.22 Arrhenius plot of median V1M1 electromigration lifetimes (phase V) 127

4.23 Electromigration lifetimes for the Au M1 structures at different J ... 129

4.24 ln ($t_{50\%}$) versus ln (J) plot for non-normalized Au M1 median lifetimes .. 130

4.25 ln ($t_{50\%}$) versus ln (J) plot for normalized Au M1 median lifetimes ... 131

4.26 Ion-induced SE image of the electroplated Au microstructure ... 133

4.27 Lineal intercept method applied on the Au microstructure ... 134

4.28 FIB cross-sectional view of the Au test structure microstructure ... 136

4.29 As-deposited voids in the electroplated Au film ... 137

4.30 Electron current flow direction on the Au M1 structures ... 139

4.31 Uncensored failure time data for the Au M1 structures (phase III) ... 140

Figure Page

4.32 Optical image of the early failure void location 141

4.33 SEM cross-sectional view of the early failure void 142

4.34 Optical image of a typical Au M1 electromigration failure void 143

4.35 SEM image of typical Au electromigration-induced voids 144

4.36 SEM image of a large Au hillock formation 145

Chapter 5

5.1 Normalized Au M1 test structure resistance distribution (phase II) 147

5.2 Normalized Au M1 test structure resistance distribution (phase V) 148

5.3 Initial Au M1 structure resistance versus electromigration lifetime 149

5.4 Au electromigration failure distributions with a 10% failure criterion 151

5.5 Au M1 structure resistance traces scaled on a 10% $\Delta R/R_o$ graph 152

5.6 Voltage (resistance) spikes for Al during electromigration testing 154

5.7 Electromigration resistance characteristics of Cu interconnects 155

5.8 As-deposited voids in the electroplated Au film 157

5.9 Au M1 structure early failure void location at the anode end 157

5.10 SEM cross-sectional view of Au M1 structure early failure void 158

5.11 Electromigration lifetimes for the Au M1 structures (phase V) 162

5.12 Arrhenius plot of median Au M1 electromigration lifetimes (phase V)... 163

5.13 Electromigration lifetimes for the Au M1 structures at different *J* 169

5.14 Natural logarithm of Au M1 median lifetimes versus current density..... 170

CHAPTER 1 INTRODUCTION

In this chapter, the background of semiconductor microelectronics and the demand on integrated circuits in terms of performance and current density are reviewed. The significance of electromigration reliability for microelectronic interconnects is discussed along with a brief review of the expanding market for compound semiconductors. This chapter concludes with the defined research objectives for this dissertation.

1.1 Background and Motivation

Ever since the invention of the solid state bipolar transistor by Bardeen, Brattain, and Shockley at Bell Labs in 1947, semiconductor electronics have rapidly advanced in response to the proliferation of modern technology. A continuous increase in microelectronic integrated circuit (IC) complexity and density through miniaturization of device dimensions has enabled integration of over a billion transistors onto a single semiconductor microchip. This miniaturization scaling trend has produced higher performance ICs operating at increased power loads and elevated temperatures, thus posing material reliability challenges. As a result of ICs shrinking, metal interconnects have decreased in both line-width and thickness, causing resistance and current densities of the interconnections to substantially increase. Figure 1.1 exhibits the operational current density increase due to reduced interconnect dimensions, corresponding to the advancing technology generations (nodes).[1] With higher current densities, Joule heating increases metal interconnect film temperatures hastening electromigration failures to be the predominant reliability hazard for ICs.

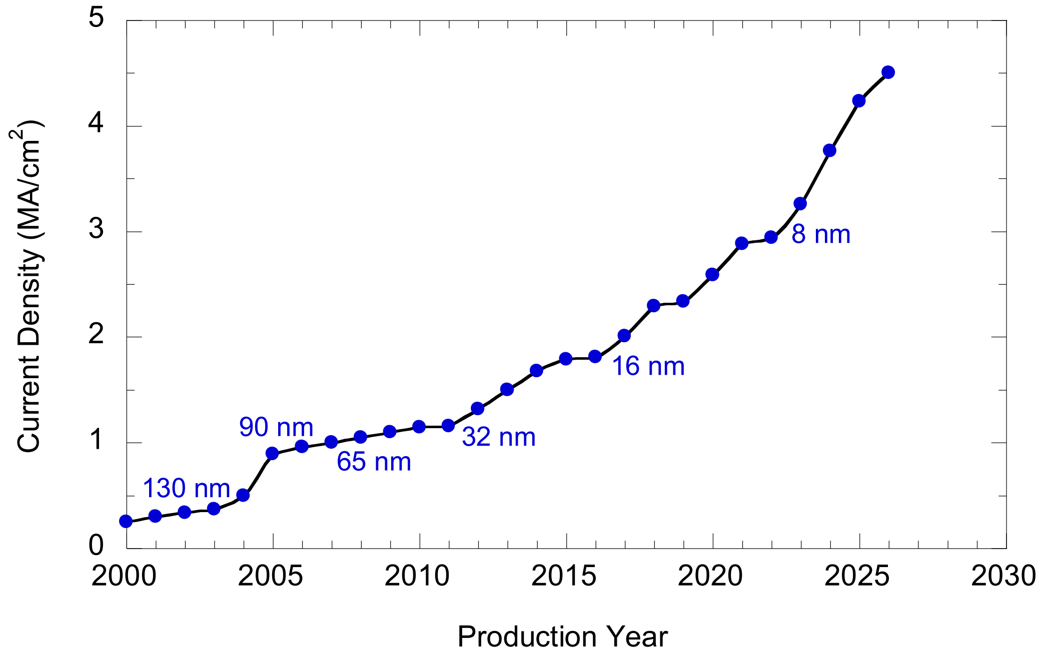


Figure 1.1 Operational current density trend for advancing technology nodes.

Electromigration in metal interconnects is the most pernicious failure mechanism in semiconductor ICs. A notorious example was an interrupted space mission launch at Cape Canaveral caused by the electromigration failure of a microelectronic chip inside the onboard computer, costing taxpayers 1.5 million dollars.[2] All semiconductor companies employ scientists and engineers to evaluate and monitor electromigration reliability of interconnect metallizations. Early electromigration investigations were focused primarily on aluminum interconnects for silicon-based ICs. Development of high-power radio frequency (RF) compound semiconductor devices that operate at higher current densities and elevated metal film temperatures required an alternative metallization that is compatible with GaAs substrates and improved electromigration reliability.

Gold-based metallization was implemented on GaAs devices because it uniquely forms a very low resistance ohmic contact and gold interconnects have superior electrical and thermal conductivity properties. Gold (Au) was also believed to have improved resistance to electromigration due to its higher melting point, yet electromigration reliability results on passivated electroplated Au interconnects are scarce and inadequate in the literature. The impetus for Au-based metallization used for interconnects (transmission-lines) in GaAs devices originated due to the formation of superior ohmic contacts, yet improved electromigration reliability was expected. However, more precisely controlled and statistically rigorous investigations are needed to quantify electromigration lifetimes of Au interconnects. The fast growth of the GaAs device market has motivated obtaining accurate Au electromigration model parameters for lifetime predictions. Figure 1.2 displays the growth of the GaAs market revenue.[3]

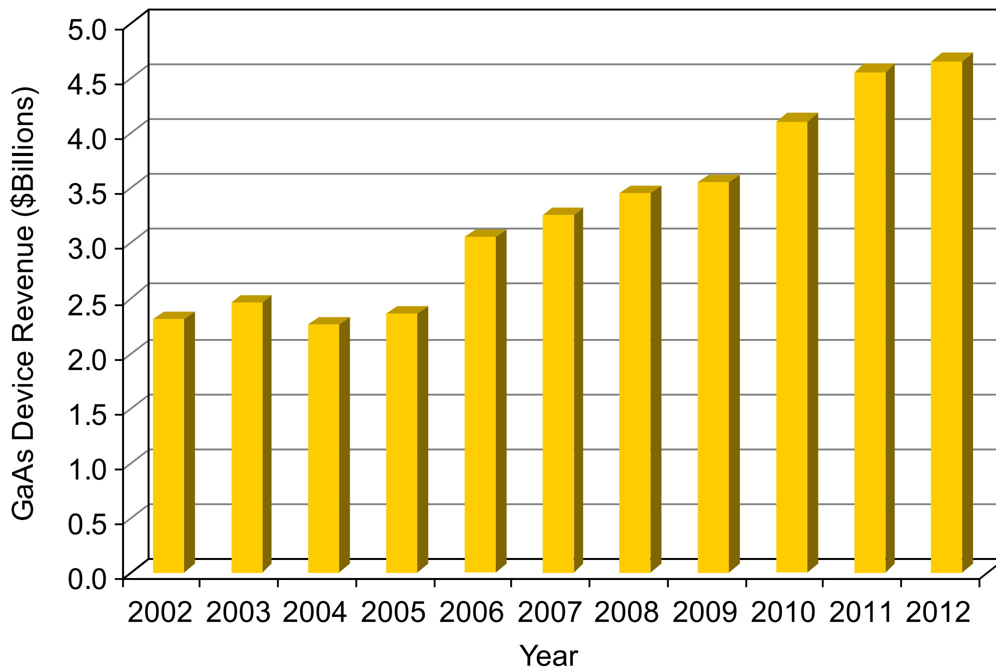


Figure 1.2 Market revenue growth for GaAs devices.

1.2 Research Objectives

The primary objective of this doctoral research was to investigate electromigration reliability of passivated electroplated Au thin film interconnects utilizing high-resolution in-situ resistance monitoring equipment. This research study applied precisely controlled stress conditions and statistically rigorous sample size experiments to determine accurate activation energies and current density exponents for Au interconnects. These electromigration model parameters were derived from log-normal based statistics and extracted from linear regressions of the Arrhenius and inverse relationships on natural log plots. The applicability of Black's empirical model was evaluated through the results of this investigation. Another objective was characterization of the electroplated gold test structure resistance, microstructure, and failure analysis of the electromigration wear-out mechanisms that caused the interconnect failures. In order to accomplish these objectives, successive experimental phases (I – V) were conducted to optimize both test structure design and experimental stress conditions.

This dissertation is organized into six chapters. Chapter 1 provides a brief motivation and background, along with the research objectives for electromigration in gold interconnects. Chapter 2 reviews the fundamental theory of electromigration, and the various effects, measurement methods, and models of electromigration in interconnects. Pertinent properties of gold that are essential to its use in microelectronic applications are succinctly given. This chapter concludes with a comprehensive review and critique of previous research investigations on electromigration in gold films.

Chapter 3 describes the experimental procedures and methods undertaken in this doctoral research. Full details on the test structure design, processing of the film layers, and the package assembly steps are specified. The electromigration test equipment, procedures, and experimental stress conditions as well as the data analysis methods are outlined. Chapter 4 presents the experimental results and data collected in this doctoral research. The measurement data of the resistance, film stress temperature, and degradation of the gold interconnects is presented. The electromigration failure lifetimes of gold interconnects as a function of temperature and current density are presented and used in the determination of the activation energy and current density exponent parameters. Characterization of the microstructure and electromigration-inducted void formation of the gold interconnects are also described. Chapter 5 contains discussion and analysis of the experimental results. Interpretation of early failures and comparison with previous investigations is also discussed. Chapter 6 summarizes and concludes the main results of this doctoral research along with suggestions for future work.

CHAPTER 2 ELECTROMIGRATION THEORY AND REVIEW

In this chapter, the basic theory and fundamental aspects of electromigration in metals are reviewed. The significance of electromigration as it pertains to the reliability of integrated circuit interconnects, as well as the pivotal advancements in the microelectronics manufacturing processes for inhibiting failures and improving metallization lifetimes are discussed. Gold thin film properties and applications in microelectronics are presented. In the final section, a comprehensive review of previous investigations into electromigration in gold thin films is summarized.

2.1 Electromigration Fundamentals and Theory

Electromigration is a phenomenon characterized by mass transport of metal atoms (or ions) under the influence of charge carriers (electrons) when an electric field is applied. This forced mass transport phenomenon was first observed in 1861 by Geradin, who discovered that molten alloys subjected to direct electric current showed segregation of its components. The first attempt to describe electromigration physically is attributed to Skaupy in 1914, who suggested the importance of the interaction between the metal atoms and the moving electrons. It was many years later in 1953, when two German scientists Seith and Wever conducted the first systematic experiments to measure the mass transport of Hume-Rothery alloys. This work was the first evidence for the driving force of electromigration. These marker motion experiments revealed that the driving force for electromigration was not solely influenced by the electrostatic force from the applied electric field, but also strongly depended on

the direction of motion of the electrons.[4] As a result of these empirical observations, Seith conceptualized that flowing electrons transferred momentum to atoms causing mass transport. This prompted a reemergence of the idea originated by Skaupy of "electron wind" as the driving force for electromigration. The idea of the "electron wind" as a momentum transfer driving force causing mass transport in metals subjected to an electric field established the theoretical foundation for electromigration.

Shortly following this theoretical development, mathematical formulations for the electromigration driving forces were derived by Fiks[5] in 1959 and Huntington and Grone[6] in 1961. Their electromigration driving force model was formulated from a semi-classical ballistic approach to explain the collision of the charge carriers with the metal ions to induce mass transport. According to this ballistic model, the electromigration driving force (F_{em}) is composed of two distinct contributions. The first component arises from the interaction of the electric field on the charge of the migrating ion known as the direct electrostatic force (F_{es}). The second component is due to the momentum transfer from flowing conduction electrons colliding with the metal ions, and is called the electron wind force (F_{wd}). Therefore, the total effective electromigration driving force is expressed as

$$F_{em} = F_{es} + F_{wd} = \left(Z_{es} + Z_{wd}\right)eE = Z^{*}_{eff}eE, \tag{2.1}$$

where Z_{es} is the charge number of the metal ion, Z_{wd} the charge number corresponding to the electron wind, e is the electronic charge, and E is the electric field. Combining the charge numbers yields the effective charge number Z^{*}_{eff} which is dimensionless and ranges[7] in value from 10^{-1} to 10^{2}.

Electromigration is basically a diffusion process under a driving force. Viewed microscopically, electromigration is a directed bias on the diffusive motion of metal atoms within a crystal lattice. Metal atoms vibrate within a crystal lattice due to thermal energy that allows atoms to diffuse (jump) out of the equilibrium lattice position to a saddle-point (halfway) position. During the process of an atomic jump out of the lattice equilibrium position under influence of the electromigration driving force, a metal atom in the saddle-point is impacted by a large number of electrons. In this manner, the momentum transfer biases the atomic jump in the direction of the electron flow.[8] Thus, the electromigration driving force generates mass transport of metal atoms and atomic diffusion in the direction of the electron wind. Figure 2.1 depicts the electric field forces that are acting upon metal atoms in a crystal lattice.

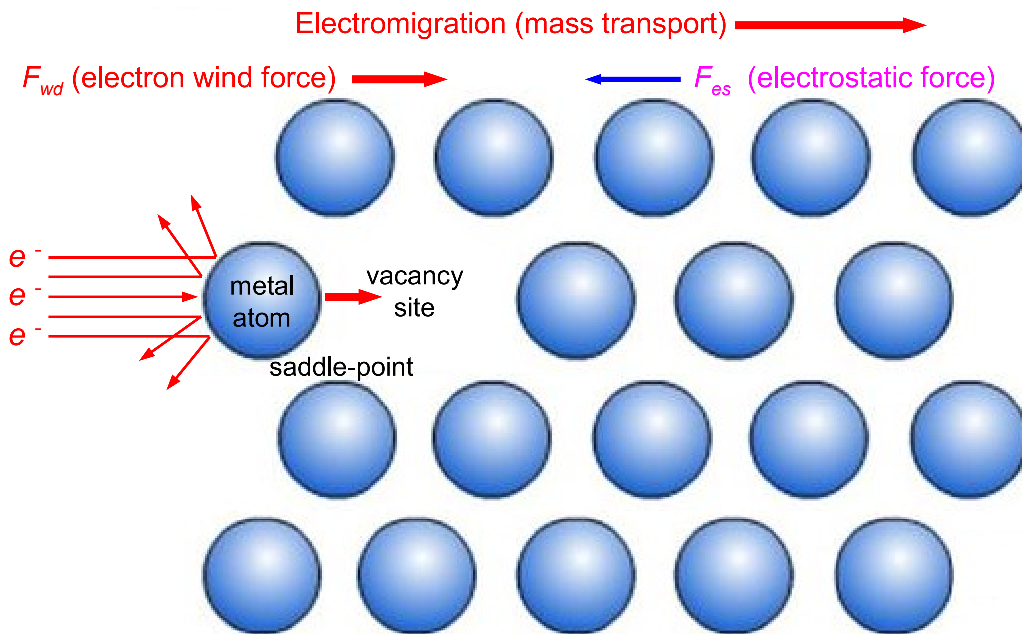


Figure 2.1 Electric field forces acting upon metal atoms in a crystal lattice.

The F_{es} force due to the interaction between the ionic core of the atoms and the electric field is directed toward the negative electrode terminal and is not strongly dependent on the temperature. For most metals, the F_{es} force is negligible in comparison to the F_{wd} force that is acting in the opposite direction toward the positive terminal. This electron wind force has been reported to be an order of magnitude greater than the electrostatic force for gold, copper and aluminum.[9] The portrayal of electromigration in Figure 2.1 is based on vacancy diffusion as the dominant mechanism in a metal lattice. However, it should be noted that similar biased atomic diffusive motion under an electric field occurs more predominantly at grain boundaries and interfaces in thin metal films. More details on these physical mechanisms are discussed later in this chapter.

The electromigration driving force creates an atomic flux (J_a) in the direction of the electron wind described by

$$J_a = N\mu F_{em}, \tag{2.2}$$

where N is the atomic density and μ is the atomic mobility. Substituting the electromigration driving force from Equation (2.1) into Equation (2.2), and expressing the electric field as the product of the current density (J) and the metal resistivity (ρ), yields the following

$$J_a = N\mu Z^*_{eff} eE = N\mu Z^*_{eff} e\rho J. \tag{2.3}$$

According to the Einstein relation, the atomic mobility can be expressed in terms of the diffusion coefficient by

$$\mu = \frac{D}{kT}, \tag{2.4}$$

where D is the diffusion coefficient for metal atoms, k is Boltzmann's constant, and T is the absolute temperature.

Substituting the Einstein relation for the atomic mobility into Equation (2.3), the atomic flux becomes

$$J_a = N\left(\frac{D}{kT}\right)Z^*_{eff}e\rho J. \quad (2.5)$$

Equation (2.5) can be expressed in terms of the metal ion drift velocity (v_d) using the relationship $v_d = \mu F_{em}$. Inserting this relationship into Equation (2.5), and solving for the metal ion drift velocity, the expression converts to

$$v_d = \left(\frac{D}{kT}\right)Z^*_{eff}e\rho J. \quad (2.6)$$

In bulk metals such as metal wires (compared to thin metal films on insulating silicon substrates) applied electrical currents produce significant Joule heating, since thermal dissipation is considerably lower. Even at much lower current densities near 10^4 amps / cm^2, bulk metals generate extremely elevated temperatures where electromigration wear-out is more rapid. Since electromigration is strongly temperature dependent, it is important to examine the diffusion coefficient relationship expressed as

$$D = D_o \exp\left(-\frac{E_a}{kT}\right), \quad (2.7)$$

where D_o is the maximum diffusion coefficient at infinite temperature, and E_a is the activation energy for the diffusion process. Rearranging and substituting into Equation (2.6), the drift velocity equation becomes

$$\left(\frac{v_d}{J}\right) = Z^*_{eff}e\rho\left(\frac{D_o}{kT}\right)\exp\left(-\frac{E_a}{kT}\right). \quad (2.8)$$

By plotting the natural logarithm of (v_d / J) versus the reciprocal of temperature, the electromigration E_a parameter can be obtained from experimental data.

2.2 Electromigration in Interconnects

Early experimentation on the electromigration phenomenon focused on diffusion in bulk metals.[6, 10] It was not until the late 1960's that research efforts abruptly changed focus due to observations that electromigration was the primary metallization wear-out failure mechanism for aluminum interconnects in integrated circuits (ICs).[11, 12] These observed electromigration failures threatened to halt microelectronic IC production and were initially referred to as the "cracked stripe" problem, since void growth extended across the metal lines causing electrical opens. Although the pernicious effect of electromigration was known for several years in bulk metals at higher temperatures, it came as a severe shock that IC thin film metal interconnects were susceptible to electromigration failures at much lower temperatures.

Explanation for this observed discrepancy is attributed to the distinguishing characteristics of thin metal films compared to bulk metals. Because IC thin metal interconnects are deposited on insulating silicon dioxide (SiO_2) layers on silicon (Si) substrates that provide effective thermal conductivity for current-induced heat dissipation, significantly higher current densities can be attained while maintaining much lower film temperatures than allowed in bulk metal wires. Moreover, early IC aluminum interconnects were typically 1 to 2 μm thick and 5 to 10 μm wide, creating a large surface to volume ratio that promotes heat dissipation.[7] Another characteristic of IC thin metal films is the fine grained polycrystalline microstructures that are formed by the evaporation deposition method. As a consequence of subjecting IC thin metal interconnects to current densities above 10^6 amps / cm^2, the electromigration damage phenomena and the preponderant role of grain boundary diffusion became evident.

2.2.1 Microstructure and Geometric Effects

Although electromigration in interconnects occurs as a combination of several different diffusion mechanisms including lattice, grain boundary, and interface, it has been found that grain boundary diffusion is the dominant pathway for mass transport. This is especially true in the case of thin metal interconnects composed of small-grained microstructures, which enables diffusion to occur rapidly along the abundant supply of grain boundaries. Electromigration failures in interconnects are caused either by void formation leading to open circuits or hillock extrusions leading to short circuits. Both of these electromigration failures are due to atomic flux divergence sites where more mass is transported out of a region (void) or where more mass is entering a region (hillock). Grain boundaries are a preferred nucleation site for voids and hillocks because flux divergence occurs in the junction of three grain boundaries. This junction is known as a grain boundary triple point. At these locations, more mass can be migrated along two grain boundaries leaving from a single grain boundary which causes localized mass depletion (voids).[2] Figure 2.2 illustrates a polycrystalline metal interconnect containing grain boundary triple points, where atomic flux divergence occurs leading to void and hillock formation.

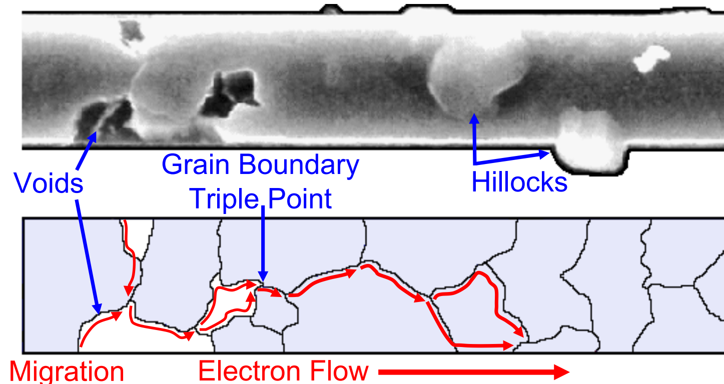


Figure 2.2 Flux divergence at grain boundary triple points.

Numerous studies have carried out experimental work on grain boundary effects and geometric considerations for IC interconnect reliability. The results of the initial studies[13-16] showed that the activation energy of the mass transport for aluminum interconnects was in the range of 0.5 to 0.7 eV. In this activation energy range, the dominant mode of mass transport was determined to be grain boundary diffusion, since lattice diffusion exhibited at higher temperatures yields much larger E_a values[10] on the order of 1.4 eV. The significant influence of grain boundaries on the electromigration mechanism in interconnects necessitates a modification to the atomic flux expression in Equation (2.5). For ideal grain microstructures of equiaxed texture,[4] the atomic flux is represented by

$$J_a = N_{GB}\left(\frac{D_{GB}}{kT}\right)\left(\frac{\delta}{d}\right)Z^*_{GB}e\rho J, \tag{2.9}$$

where δ is the effective boundary width for mass transport, d is the average grain size, and GB subscripted parameters denote grain boundary diffusion.

Since grain boundaries supply rapid pathways for atomic diffusion, efforts were taken to manipulate the grain size and microstructure of interconnects. It has been demonstrated[17] that single crystal aluminum thin film conductors inhibit electromigration damage under current density and temperature conditions that would cause polycrystalline interconnects to fail. However, depositing single crystal interconnects in a high-volume manufacturing environment is not practical, whereas producing large grain microstructures by annealing films is manufacturable. Narrow line-width interconnects with recrystallized large metal grain sizes produce “bamboo-like” microstructures, where almost all grain boundaries are perpendicular to the current flow in the conducting line. Bamboo grained interconnects lack continuous grain boundaries that are parallel to the

electron flow, and therefore mass transport along these rapid diffusion pathways is blocked. A representation of a bamboo grained microstructure interconnect is shown in Figure 2.3. These bamboo grained microstructures have been found to be effective in improving the electromigration lifetimes of interconnects.[18-20] Although bamboo microstructures improve interconnect lifetimes, electromigration failures still occur at the sparsely available grain boundary triple points and edge surfaces.

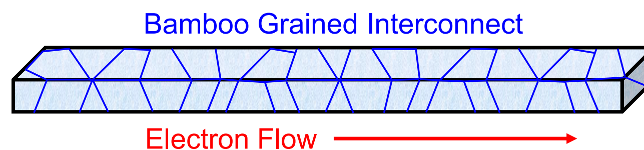


Figure 2.3 Bamboo grained microstructure interconnect.

An added enhancement for improving electromigration lifetimes of Al interconnects was discovered through the use of protective overcoating (passivation) layers. Deposition of SiO_2 or phosphosilicate glass (P_2O_5 - SiO_2) passivation layers over Al interconnects were shown to improve electromigration lifetime by one to two orders of magnitude.[21, 22] Yet the reported high activation energy of 1.2 eV was rationalized as a reduction in surface diffusion. Conversely, another study did not observe this higher activation energy[15] and considered the reduced surface diffusion argument invalid, because grain boundary diffusion at nearly the same activation energy would still be dominant. A more recent explanation for increased lifetimes is that the restraining SiO_2 passivation enables higher compressive stresses on the Al film, which retards electromigration and hillock extrusions.[23]

Another important factor of electromigration in interconnects is the buildup of a mechanical stress gradient within the metal line. During electromigration, atoms are depleted from the cathode end and accumulated on the anode end leading to a slight atomic density imbalance that creates a stress gradient along the Al line segment. Blech conducted electromigration experiments on varying lengths of Al lines deposited onto a refractory layer of titanium nitride (TiN).[24-26] Through passing electrical current in the Blech test structure, electron flow is driven into the much lower resistivity Al film causing Al migration that depends on the current density and the length of the Al line segment. Figure 2.4 depicts the Blech length effect in Al thin film segments.

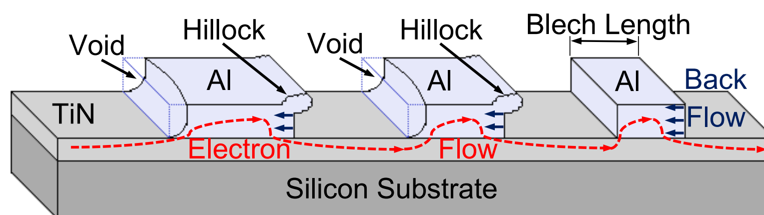


Figure 2.4 Blech length effect demonstrated on Al thin film segments.

It was found that the electromigration-induced stress gradient creates a backflow diffusion flux in the opposite direction to the electron wind atomic flux. If the stress gradient is allowed to increase without stress relief from electromigration damage in the form of voids and hillocks, it reaches a critical limit at which the backflow diffusion flux equals the electron wind atomic flux preventing electromigration. This stress-induced backflow that halts electromigration is known as the Blech effect.

Combining the stress-induced backflow flux with the electron wind atomic flux, the net atomic flux is expressed as

$$J_{net} = N\left(v_d - v_b\right) = N\left(\frac{D}{kT}\right)\left(Z^*_{eff} e\rho J - \Omega\frac{\Delta\sigma}{\Delta x}\right), \tag{2.10}$$

where Ω is atomic volume and $\Delta\sigma / \Delta x$ is stress gradient along the line. Blech established that a critical threshold value exists for which electromigration is averted and determined that it is related to the product of current density and the metal line length. When the electromigration driving force equals the generated backflow stress, a steady state is reached. It is defined as

$$Z^*_{eff} e\rho J = \Omega\frac{\Delta\sigma}{\Delta x}. \tag{2.11}$$

Rearranging this steady state expression to solve for the critical threshold product gives

$$J_c L_{Blech} = \Omega\frac{\Delta\sigma}{Z^*_{eff} e\rho}. \tag{2.12}$$

It is surmised from this relationship that below the critical threshold product of current density J_c and line length L_{Blech}, the atomic mass transport ceases, thereby preventing electromigration damage. Moreover, for a given constant current density J_c there is a specific line length L_{Blech} below which electromigration failure will not occur. This specific line length is known as the Blech length and is typically around 50 μm. It was also found by Blech[24] that Al lines entirely encased in SiN passivation exhibited decreased atomic mass transport and the critical threshold product increased. This threshold effect has very useful implications for the reliability of ICs because designers can lay out interconnect architectures that have significantly reduced electromigration risk by ensuring that the majority of lines are below the critical Blech length.

Despite lifetime improvements achieved with use of large grained bamboo microstructures and passivation encasement of interconnects, electromigration damage persists due to other sources of flux divergence. Electromigration-induced damage in interconnects is the result of sustained atomic or vacancy flux divergence. Other sources of flux divergence to be considered are temperature gradients and terminal material interfaces. High current operation of ICs generates Joule heating accompanied by temperature gradients in regions where interconnect line-widths abruptly change, thus posing a risk for electromigration. Additionally, multi-level metallization IC technology commonly uses refractory metal diffusion barriers and tungsten filled vias. Electron current flowing in the tungsten (W) via into the aluminum-copper (Al-Cu) interconnect creates flux divergence at the interface. A three-dimensional view of the W / Al interface where flux divergence occurs is shown in Figure 2.5. Electron flow causes Al atoms to migrate away from the W via bottom that are not backfilled by the immovable W atoms, thus creating flux divergence at the interface. Therefore, voids nucleate and grow at the via / interconnect interface and lead to electromigration failures.[27]

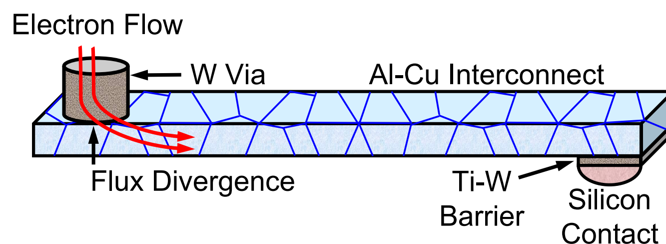


Figure 2.5 Flux divergence at the W via / Al interconnect interface.

2.2.2 Alloying and Metallization Advancements

Pure aluminum was originally the primary metallization used for IC interconnects because of its very low resistivity and compatibility with silicon processing. Al thin films can be deposited by evaporation or sputtering methods and exhibit good adhesion to inter-layer dielectric (ILD) films such as SiO_2. Even though pure Al has several ideal properties for use in IC interconnects, it lacks superior electromigration reliability. Discovery of the beneficial effects of Cu contamination into Al thin films inadvertently occurred while investigating grain boundary mass transport. The addition of 4 wt. % of Cu into Al thin films was found to increase the electromigration lifetimes by a factor of 70 times.[28] It was revealed that failures occurred in Cu depleted areas and that Cu atoms migrate faster than Al atoms. Furthermore, it was suggested that the Cu doped Al films had the same intrinsic grain boundary diffusion mechanism, but the Cu in the grain boundaries retard electromigration. Alloying additions of silver or gold did not show the same increased lifetimes.[29] Also, it is known that the solubility of Cu in Al is only about 0.05 wt. % and that Al_2Cu precipitates are observed to be distributed along grain boundaries. Electromigration lifetime enhancement due to alloying Al with Cu is postulated as a consecutive two step process. The first step consists of the preferential and sacrificial diffusion of Cu atoms occurring along grain boundaries until localized depletion is reached. Next, void formation commences in these Cu free regions of the Al conductor leading to open line failures. Although the activation energy was thought to be similar[30] to pure Al films, it was shown to be 0.2 – 0.3 eV higher[31] for the two-step kinetic failure process of Al(Cu) films. A comprehensive review of electromigration in Al and Al(Cu) interconnects is furnished by C. K. Hu and others.[32]

Additions into Al films of other alloying elements, such as magnesium and chromium, were proven to reduce the rate of electromigration.[33] While additions of magnesium showed substantially better lifetimes compared to Al(Cu) films, the resistivity of Al alloyed with 6 wt. % of Mg increased nearly twofold over pure Al making it less preferable as an electrical conductor. Furthermore, Al alloys containing magnesium are challenged with thermal process limitations because magnesium reacts with SiO_2 at high temperature.[34]

An alternative scheme for improving resistance against electromigration was the implementation of refractory metals for Al(Cu) interconnects. The refractory metal layer is typically deposited underneath the Al(Cu) film as a barrier layer, but also can be on top as a capping layer. One of the most common refractory metal layers used as a barrier layer for Al(Cu) metallization is titanium tungsten (TiW) with a stoichiometry of 10% Ti and 90% W. A TiW / Al(Cu) metallization stack shows median electromigration lifetimes two to ten times longer than Al(Cu) films alone.[35, 36] The TiW layer also acts as a diffusion barrier against junction spiking by being interposed between the Al film and the silicon contact.[37] Another barrier layer observed to enhance electromigration performance is titanium nitride (TiN), which by annealing can increase lifetimes by a factor of 2. Additional electromigration performance improvements were shown with the use of TiN anti-reflection coatings (ARC) deposited on top of the Al(Cu) alloy as a capping layer.[38] Specific refractory metals and silicides including Ti, W, WSi_2, and $MoSi_2$ as capping layers for Al metallization were shown to improve reliability for electromigration.[39] With the selection of metallizations for ICs, it is paramount that superior electrical conductivity and electromigration reliability properties are optimized.

As the trend in IC miniaturization decreased to the low submicron range for ultra large-scale integration (ULSI) devices, a new interconnection metal was sought that would possess higher reliability against electromigration damage. While Al(Cu) metallization served well for decades as an interconnect metal, its continual use in ULSI devices reached performance limitations. These limitations[40] are enumerated by additional interconnect levels necessary for ULSI devices, resistance-capacitance (RC) delays in signal transmission, and insufficient electromigration reliability in Al(Cu) lines with reduced dimensions possessing higher current densities. In addressing these limitations, copper metallization was proposed as a replacement for Al(Cu) in the early 1990's.[41-47]

Given that Cu has a much higher melting point (1083°C vs. 660°C) than Al, its atomic diffusion and thus its electromigration mass transport is expected to be slower at the same device operating temperature. Moreover, the resistivity of Cu compared to Al(Cu) (1.7 μΩ·cm vs. 3.2 μΩ·cm) is significantly lower providing faster signal propagation and shorter switching times, which in turn reduces the RC delay. With these ideal properties, Cu metallization was considered an attractive choice for IC interconnections. However, implementation of Cu as an interconnect material for silicon ICs has been fraught with challenges. These Cu challenges include higher susceptibility to corrosion, rapid diffusion in silicon causing contamination (poisoning) of device regions, difficulty of dry etching, and poor adhesion to silicon oxide dielectric films.[48] A lack of a suitable reactive ion etching (RIE) process for Cu prevented employment of the conventional subtractive etch process used for Al(Cu) interconnects. Thus, an entirely new integration scheme was required and developed for the transition to Cu metallization.

The Cu metallization integration scheme is considered an additive patterning or in-laid process known as the Damascene process. In this process the interconnect trench contour is first patterned into the underlying silicon oxide prior to Cu deposition. A thin layer of barrier metal such as tantalum (Ta) or tantalum nitride (TaN) is then deposited in the trench to surround and prevent Cu diffusion in the silicon device, which would cause deep-level traps. The trenches are overfilled with a thick Cu layer deposited by electrochemical deposition. A thin conductive seed layer is required so that Cu can be electroplated on its surface. Finally, chemical mechanical polishing (CMP) removes the excess Cu and planarizes the Cu metallization with the top of the silicon oxide layer. Further advancement is leveraged with the dual-damascene integration, which combines filling via holes and line trenches into one step, thus reducing the overall processing steps for a multi-level metallization IC.

High performance submicron complementary metal-oxide-semiconductor (CMOS) technology with six levels of planarized Cu interconnects was developed and first announced by Motorola[49] and IBM[50] in 1997. Characterization results of this multi-level Cu interconnect technology showed a significantly lower resistance (45% reduction) potentially translating into a 30% lower RC delay compared to equivalently scaled Al(Cu) technology. Furthermore, dual-damascene Cu metallization has demonstrated superior electromigration reliability allowing higher current density operation. Through direct experimental comparison, electromigration median lifetimes of Cu interconnects are about 100 times longer than that of Al(Cu) metallization.[51] More detailed reviews on Cu metallization reliability are given by Rosenberg,[52] Ogawa,[53] and Tu[40].

2.2.3 Reliability Measurement Methods

Assurance that the electromigration reliability of interconnects at normal operating conditions exceeds the desired IC lifetime of 10 years requires accelerated testing. Accelerated testing involves the application of stresses of temperature and current density significantly above normal operation to expedite the electromigration failure mechanism and shorten tests to a practical timeframe. Stress temperatures from 200°C to 350°C and current densities in the range from 1 to 3 mega amps (MA) / cm^2 are typical for conventional electromigration tests. Electromigration lifetimes under accelerated stress conditions are measured to extract model parameters and to predict normal operating failure lifetimes. To accurately predict operational lifetimes by extrapolation requires that the same failure mechanism operates under both accelerated and normal stress conditions.

Measurement of electromigration-induced failures of interconnects has been approached by an array of different test methods. Conventional package-level tests and highly accelerated wafer-level tests distinguish the two main approaches for electromigration testing. Since conventional package-level tests are time consuming and require expensive ceramic packages, there has been a concerted attempt starting in the early 1980's to use highly accelerated wafer-level tests. The most notable fast electromigration wafer-level test methods include the standardized wafer-level electromigration accelerated test (SWEAT), breakdown energy of metal (BEM), and the wafer-level isothermal Joule-heated electromigration test (WIJET). Unfortunately, these fast wafer-level tests are plagued by substantial overstressing errors causing inaccurate lifetime predictions. These quick tests show merit for reliability monitoring of interconnect processing defectivity, but not for electromigration lifetime prediction.[54]

Conventional package-level electromigration tests with application of a moderate stress acceleration level remain the best approach for accurately extracting model parameters and extrapolating interconnect lifetimes at normal operating conditions. There are three experimental measurement techniques of conventional package-level tests which have had widespread use for electromigration studies of interconnects.[55] The earliest of these three techniques is the median time to failure ($t_{50\%}$) lifetime test. This technique is carried out by stressing several interconnect test structures at known current density and temperature until an electromigration-induced void traverses the entire line-width and ceases current flow, which then gets recorded as the interconnect failure time. All combined failure times yield a statistical spread with the median time to failure defined as the time at which 50% of the interconnect test structures have failed. A major drawback of this technique is that a constant temperature is not maintained because localized Joule heating occurs as the void size grows leading to thermal runaway and catastrophic failures.

Microscopic observation of void formation or edge displacement in metal lines as direct drift velocity measurement techniques have also been utilized for electromigration studies.[56, 57] The void formation technique requires a hole to be etched through the silicon die in order for transmission electron microscopy (TEM) images to be taken of the thin metal film during the test. These TEM images reveal the rate of void formation that determines the electromigration drift velocity. The edge displacement technique measures and relates the velocity of the metal film edge as it migrates to the average drift velocity for electromigration. A disadvantage of these techniques is the laborious test structure preparation and monitoring which prohibits a statistically relevant sample size for tests.

Another key limitation inherent with these techniques is the inability to evaluate interconnect structures with passivation film coatings. Actual IC interconnects are embedded within inter-layer dielectric (ILD) layers with a final passivation overcoat causing enhanced electromigration properties compared to the bare metal films necessary for these direct techniques. Lastly, enormous temperature gradients are generated in the suspended thin metal film samples.

The resistometric method for electromigration experiments has become the most popular technique currently practiced due to its ease of application and lack of major drawbacks. Introduction of the resistance monitoring technique was pioneered early on by Rosenberg[13] at IBM to examine the structural damage of interconnects during accelerated electromigration tests. This technique correlates the change in resistance to structural change caused by accumulation of electromigration-induced voids. The rate of resistance change ($\Delta R/\Delta t\ R_o$) is considered to be proportional to the atomic drift velocity (v_d) as follows

$$\frac{\Delta R}{\Delta t}\left(\frac{1}{R_o}\right) = A\ \exp\left(-\frac{E_a}{kT}\right) = \frac{v_d}{l_v}, \qquad (2.13)$$

where A is a pre-exponential factor and l_v is the metal segment length. Given this implicit relationship, activation energies between 0.5 to 0.7 eV for Al thin films were obtained by the resistometric technique, which are consistent with lifetime measurements.[58] This method is capable of measuring minute resistance change (< 1%) to detect tiny voids not directly observable by microscopic techniques, especially in the case of passivated interconnects. A further advantage is the ability to measure a large number of interconnects inside a constant temperature oven, thus avoiding the Joule heating inherent with other tests. Also, significant test time reduction can be achieved with this method.

2.2.4 Failure Kinetic Models

Accurate prediction of electromigration-induced failures in interconnects under normal operating conditions is of utmost importance for IC manufacturers. Therefore, development of a predictive model that represents the functional relationship between thin film failure kinetics and applied stresses driving the electromigration mechanism has been the central focus of many studies. Early attempts to reconcile theoretical models with experimental electromigration data were insufficient. Upon examination of Equation (2.6), it is ascertained that the electromigration failure time resulting from the drift velocity is proportional to the current density stress. However, actual empirical electromigration data for Al thin films showed an inverse square dependence on current density. Initial theoretical models were not inclusive of several factors such as mechanical stress, chemical composition, and microstructural inhomogeneities which offers explanation for this discrepancy. With the discovery of the electromigration-induced stress gradient as an important contributing factor that opposes the electron wind atomic flux, an advanced understanding of the electromigration mechanism emerged. A more comprehensive model is given in Equation (2.10) with addition of this stress-induced backflow flux that exists with blocking boundaries. Through inclusion of this opposing stress-induced backflow component, general resolution is attained for the earlier disparity between the theoretical model and the empirical results.[59]

Shortly after the electromigration reliability crisis emerged in the electronics industry, Jim Black at Motorola was methodically investigating electromigration failure kinetics. Black's pioneering research developed the first empirical model that predicts the electromigration lifetimes of interconnects under

steady state direct current. Black's empirical model established that electromigration mass transport failure kinetics are dependent on an Arrhenius relationship and are inversely proportional to the square of current density. This relationship has become known as Black's equation[60] which is given by

$$t_{50\%} = \frac{A}{J^n} \exp\left(\frac{E_a}{kT}\right), \qquad (2.14)$$

where $t_{50\%}$ is median time to failure of the tested interconnect population, A is a proportionality constant dependent on the metal, J is the current density, E_a is the activation energy, T is the absolute temperature, k is Boltzmann's constant, and n is the current density exponent equal to 2 according to Black. Black's equation is the most extensively utilized model for interconnect reliability evaluations[61] and has proven to be very instrumental for extrapolating the median time to failure of a group of identical interconnects under electromigration stress conditions to normal operating conditions. According to Black's study, the constant A is composed of factors that involve the cross-sectional area of the thin metal and characteristic material properties. Activation energies E_a were shown to depend upon the microstructure of the thin metal film with higher values for large grained Al films because of a reduction in grain boundaries contained within the line limiting low energy diffusion pathways. For a range of experimental current densities, Black determined a $1/J^2$ relationship, although theoretical formulation for the electromigration driving force has a linear dependence on current density. Black's empirical[14] work was influential in establishing that electromigration failures exhibit an Arrhenius relationship with an inverse square current density dependence and that the failure time data closely follows a log-normal distribution.

More recent electromigration studies on a modern Al alloy metallization[62] scheme incorporating refractory barriers extracted values for the current density exponent between 1 and 2, while for an advanced Cu metallization[63] a current density exponent closer to n = 1 was observed. Higher values ($n > 2$) of the current density exponent are attributed to improper treatment of Joule heating effects.[27] Since many electromigration results did not strictly follow a $1/J^2$ relationship, Black's equation (Equation 2.14) took on a generalized formulation to allow for a variable current density exponent. Nearly two decades later, a few theoretical studies[64-68] have promoted clarification for Black's inverse square dependence on current density and the lack thereof for other metallizations which considerably advanced the understanding of electromigration mechanisms.

A model developed by Shatzkes and Lloyd[64] considers concomitantly the opposing electromigration-induced mass transport and Fickian diffusion due to a concentration gradient. It is based on the condition of a semi-infinite metal line with perfectly blocking boundaries at one end such as in the real situation of a "bamboo" grain boundary. As the vacancy concentration at the blocking boundary reaches a critical concentration, a void can be nucleated. This model expresses the electromigration time to failure (t_f) as

$$t_f = B\frac{T^2}{J^2}\exp\left(\frac{E_a}{kT}\right), \tag{2.15}$$

where B is a constant and E_a is the activation energy for grain boundary diffusion. It is notable this model yields a failure time that accounts for an inverse square dependence on current density and is similar to Black's model with the exception of the T^2 term. Yet this model assumes failures are dominated by the void nucleation stage which is an incomplete portrayal of the entire failure process.

Simple pure Al films without refractory barrier layers as studied by Black are considered to have a significant portion of the electromigration failure time as void nucleation which soon afterward grows to an open circuit.[59] The void nucleation process is strongly influenced by electromigration-induced stresses that build up in the film. Electromigration failure times under a void nucleation dominant process exhibit a current density exponent dependence close to $n = 2$ that confirms Black's observation. Advanced metallizations that incorporate W vias with refractory barrier layers allow current passage to be sustained after the metal is entirely voided. As a result, the void growth process is a larger portion of the electromigration failure time. The void growth process is governed by ion drift velocity factors which translates into a linear $n = 1$ current density exponent dependence. Electromigration failure times are not exclusively nucleation or void growth controlled but considered to be a combination[65] of the two processes supporting fractional current density exponents ($1 < n < 2$).

A modification to Black's equation to delineate the electromigration failure time for the void nucleation and growth kinetics was proposed.[65, 69] This model recognizes two distinct kinetic processes involved in electromigration failures which are no longer a single function of the failure time but instead are the sum of two functions. In this model electromigration median time to failure ($t_{50\%}$) is the sum of these two independent time components as follows

$$t_{50\%} = t_{nuc} + t_g = \left(\frac{AkT}{J} + \frac{B(T)}{J^2} \right) \exp\left(\frac{E_a}{kT} \right), \qquad (2.16)$$

where t_{nuc} is time required for void nucleation and t_g is the time duration for growth of a void to become an open circuit. Constants A and B have geometric factors pertaining to the void size required to reach a line failure. As follows from

this extension to Black's model, the proportion of nucleation and growth is variable depending on the current density. For higher current densities, the growth kinetics proportionately account for more of the time to failure than at lower current densities. It is found that extrapolations to normal operating conditions using this nucleation and growth model under certain cases have roughly similar lifetime prediction to Black's equation. Nonetheless, Black's empirical model parameters (E_a and n) extracted at accelerated test conditions neglect pre-existing thermally induced stresses which are substantially lower under test conditions compared to normal operation conditions. This leads to an increased void nucleation (incubation) time that can produce a significant lifetime prediction inaccuracy. In spite of this error, the nucleation and growth model[69] generally predicts longer lifetimes, so the shorter lifetimes predicted by Black's power law equation are more conservative and therefore ensure a larger reliability margin from an engineering perspective.

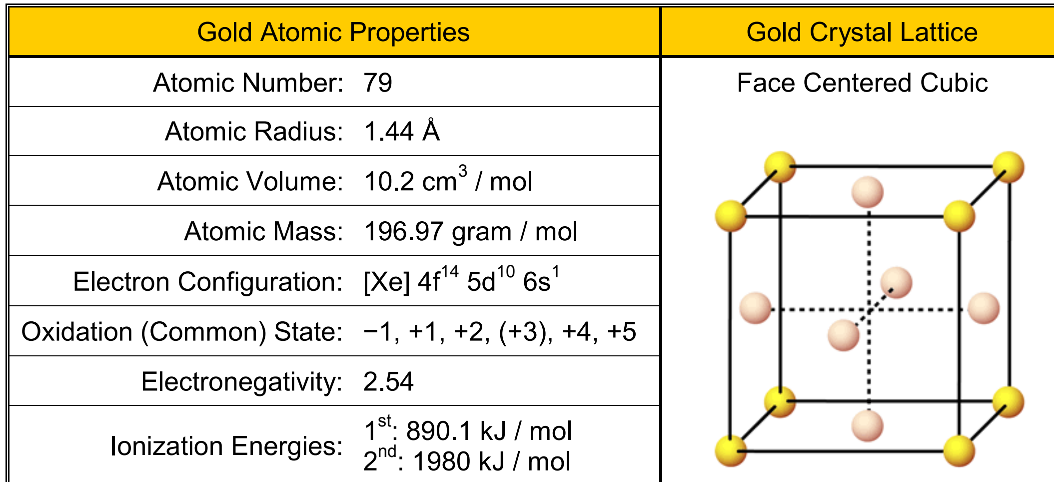
Electromigration failure kinetics display a statistical nature influenced by metallization microstructure, barrier interfaces, and to a lesser extent defectivity. Analysis of electromigration failures has consistently been described by log-normal statistics because the data fit this distribution quite well. Applying log-normal analysis yields two important parameters, the median time to failure ($t_{50\%}$) and the log-normal standard deviation or shape parameter (σ) that characterizes the electromigration failure distribution. Using Black's model and log-normal statistics, the time to failure for an acceptable failure percentage (e.g., 0.01%) under normal operating conditions can be calculated. More details on the log-normal distribution and electromigration data analysis are covered in Chapter 3.

2.3 Properties and Application of Gold Metallization

2.3.1 Properties of Gold

Gold exists naturally in its elemental metallic state as nuggets or in veins of quartz deposits and displays a unique bright reddish yellow color. The chemical symbol for gold is Au derived from its Latin name *aurum*, which means “shining dawn”. Gold has an atomic number of 79 (atomic nucleus has 79 protons) and an atomic mass of 196.97 grams / mol. Table 2.1 lists the atomic properties and lattice structure of gold.[70]

Table 2.1 Atomic properties and crystal lattice of gold.



Gold Atomic Properties		Gold Crystal Lattice
Atomic Number:	79	Face Centered Cubic
Atomic Radius:	1.44 Å	
Atomic Volume:	10.2 cm^3 / mol	
Atomic Mass:	196.97 gram / mol	
Electron Configuration:	[Xe] $4f^{14}$ $5d^{10}$ $6s^1$	
Oxidation (Common) State:	−1, +1, +2, (+3), +4, +5	
Electronegativity:	2.54	
Ionization Energies:	1st: 890.1 kJ / mol 2nd: 1980 kJ / mol	

Gold is a transition metal (d-block) in group 11 and period 6 of the periodic table with a face centered cubic (FCC) crystal lattice. Gold has the highest malleability and ductility of all metals making it suitable for wire bonding in microelectronics. One ounce of gold can be hammered into a thin sheet measuring 300 square feet.[70] This incredible malleability is due to the FCC crystal lattice of gold which is very apt for dislocation movement since it contains 12 possible slip systems that can operate during plastic deformation.[71] The color

of metals is derived from the dependence of its reflectivity upon the wavelength (energy) of incident light. For gold the reflectivity conditions for an intense absorption of light at the energy of 2.3 eV produces its characteristic bright reddish yellow color, fulfilled by electron transitions from the d-band to unoccupied positions in the conduction band.[72] Gold exists primarily in the univalent (+1) and trivalent (+3) oxidation states with the +3 oxidation state being the most common.

Table 2.2 Physical properties of gold compared to other conductor metals.

Properties	Gold	Aluminum	Copper	Silver
Melting Point (°C)	1064	660	1085	961
Boiling Point (°C)	2800	2519	2562	2210
Density (g / cm^3)	19.30	2.7	8.96	10.5
Electrical Resistivity (10^{-8} Ω·m)	2.21	2.65	1.67	1.59
Thermal Conductivity (W / m·K)	318	237	401	429
Thermal Expansion Coefficient (µm·/ m·K)	14.2	23.1	16.5	18.9
Temperature Coefficient of Resistance ($°C^{-1}$)	0.00372	0.00431	0.00404	0.00382
Vicker Hardness (MPa)	216	167	369	251
Modulus of Elasticity (GPa)	78	70	119	83
Heat of Fusion (kJ / mol)	12.55	10.71	13.26	11.28
Molar Heat Capacity (J / mol·K)	25.42	24.20	24.44	25.35

The physical, electrical, and thermal properties of gold in comparison to other conductor metals[73-75] are tabulated in Table 2.2. Gold has a very high density of 19.30 grams / cm^3 at 20°C, which correlates to its atomic mass and crystal structure.[70] A cubic foot of gold weighs over 1,200 pounds. The thermal conductivity of gold is the third highest of all metals. Gold also has the third lowest electrical resistivity behind copper and silver. Therefore, it is no surprise that copper and gold are commonly used for electrical contacts and interconnects.

One key difference is that gold is not susceptible to oxidation under normal processing environments unlike copper, making gold an indispensable choice for the microelectronics industry.

Hardness is the property of a metal that enables it to resist permanent plastic deformation. The hardness of metals is measured by penetrating a diamond indenter into the metal surface. Commercial instrumentation with four scales of hardness (Brinell, Vickers, Knoop, and Rockwell) is available. Most common of these scales for thin films use pyramidal diamond indenters with equal (Vickers) or unequal (Knoop) diagonal sides.[76] Quantitative hardness measurements on thin metal films require a minimum thickness. A Vickers hardness value for gold is 22 HV (216 MPa) in the annealed condition. Gold is a very soft metal compared to iron with a hardness of 62 HV (608 MPa). The modulus of elasticity is a measure of the stiffness of a metal and is defined as the ratio of stress over strain in the linear region where Hooke's Law is observed.[77] The modulus of elasticity of gold is 78 GPa which is close to those of aluminum and silver, but it is much lower than that for copper (119 GPa).

By far the most unique and advantageous property of gold is its excellent corrosion resistance. Corrosion is an electrochemical process composed of two half cell reactions, an oxidation reaction and a reduction reaction. The oxidation reaction involves the release (loss) of electrons, whereas the reduction reaction entails the consumption (gaining) of electrons.[78] When a metal strip (electrode) is immersed into an aqueous solution an electrical potential difference develops. The electrode potential difference is measured in volts. Note that an absolute value of a single electrode potential cannot be measured directly because a half-cell reaction, such as an oxidation reaction, cannot occur independently.

Therefore, the difference between the electrode potentials of two half-cell (oxidation and reduction) reactions is measured. This is typically accomplished by measuring the metal electrode potential with respect to the standard hydrogen electrode (SHE) under standard conditions (1 atmosphere, 1 Molar, and 25°C). By convention SHE is assigned a potential of zero volts and all other standard electrode potentials are compared against this value. Standard electrode ($E°$) potentials are useful for indicating the tendency of a metal to oxidize. Table 2.3 lists standard electrode potentials[79] for common metals.

Table 2.3 Standard electrode potentials for common metals.

Reduction Half-Reaction	$E°$ (volts)	Reduction Half-Reaction	$E°$ (volts)
$Al^{3+}_{(aq)} + 3e^- \rightarrow Al_{(s)}$	-1.67	$Cu^{2+}_{(aq)} + 2e^- \rightarrow Cu_{(s)}$	0.340
$Cr^{3+}_{(aq)} + 3e^- \rightarrow Cr_{(s)}$	-0.74	$Cu^{+}_{(aq)} + e^- \rightarrow Cu_{(s)}$	0.520
$Fe^{2+}_{(aq)} + 2e^- \rightarrow Fe_{(s)}$	-0.44	$Ag^{+}_{(aq)} + e^- \rightarrow Ag_{(s)}$	0.799
$Co^{2+}_{(aq)} + 2e^- \rightarrow Co_{(s)}$	-0.277	$Pt^{2+}_{(aq)} + 2e^- \rightarrow Pt_{(s)}$	1.188
$Ni^{2+}_{(aq)} + 2e^- \rightarrow Ni_{(s)}$	-0.257	$Au^{3+}_{(aq)} + 3e^- \rightarrow Au_{(s)}$	1.52
$H_{2(g)} \rightarrow 2H^{+}_{(aq)} + 2e^-$	0	$Au^{+}_{(aq)} + e^- \rightarrow Au_{(s)}$	1.83

Resistance to corrosion is increased for metals with more positive standard electrode potentials. As expected, gold has the highest positive standard electrode potential of all metals correlating to its excellent corrosion resistance. Due to its superior oxidation resistance, gold is classified as a noble metal along with palladium, platinum, and silver. Most chemicals will not react with gold, but it can be attacked by chlorine, fluorine, aqua regia and cyanide solutions.[70] The inertness of gold prevents the formation of insulating surface oxides, making gold indispensable for electronic circuit applications because contact resistance and reliability problems from corrosion are averted.

2.3.2 Application of Gold Metallization

In the selection of a metallization for semiconductor devices, several required properties need to be considered with respect to metal thin films for delivering IC performance, reliability, and ease of fabrication. Table 2.4 outlines the required properties for metallizations in ICs. The properties in Table 2.4 are so varied that finding a single metallization to entirely satisfy all requirements is a monumental challenge.

Table 2.4 Required properties for metallizations in ICs.

Required Properties	Benefits
High conductivity	Shorter RC time delay and high Q factor
Electromigration resistant	Reliability for long interconnect lifetimes
Corrosion resistant	No degradation from process chemistries
Low ohmic contact capable	Linear and low resistance
Good adhesion to semiconductor materials	Coherent interfaces / resist delamination
Stability from degrading intermetallic films	No resistance or detrimental reactions
Practical deposition and delineation	Reduced process complexity

The most common metallization for contacts and interconnects in ICs is aluminum because it satisfies most of the required properties. However, because of demand for interconnect miniaturization with higher current densities, it became evident that aluminum was vulnerable to electromigration failures as well as spiking of the silicon contact. Alternative metallizations with higher conductivity were sought that could satisfy the required properties and replace aluminum.[80] The higher conductivity metals gold, silver, and copper all have poor adhesion to SiO_2, which prevents a single-layer metallization solution. Both silver and copper oxidize readily in normal processing environments[81] due to the absence of a self-passivating oxide layer as is the case in aluminum thin films.

Refractory metals with better adhesion and diffusion barrier properties in conjunction with high conductivity Au were investigated as a two or three layer metallization stack. The TiW / Au metallization[80-84] showed the most promise for high temperature resistance stability, corrosion resistance, and good adhesion / diffusion barrier properties along with superior electromigration reliability compared to aluminum. A thin titanium layer provides good adhesion to SiO_2, tungsten serves as a barrier against gold diffusion into the Si active region, and a thick gold film offers a highly conductive and reliable interconnect. There are two main problems that must be overcome when utilizing gold composite layered metallization for Si devices. The first problem is the creation of deep-level traps with Au penetration into the Si active region and the formation of Au-Si eutectic at 377°C. For this reason, it is imperative that Au diffusion is prevented from entering the Si active region during high temperature processing through use of an effective diffusion barrier layer. Another problem area is the formation of intermetallics during high temperature processing that causes a resistance increase in the overall Au metallization stack. Although the TiW / Au metallization was proven to avoid these problems, early complexity and the cost of this composite layer metallization limited its implementation on Si devices.

Industrial demand for reliable high-temperature and high-frequency electronics for communications, aerospace, and military applications has driven the development of GaAs device technology. Due to the higher energy band gap (1.4 eV) of GaAs compared to silicon (1.1 eV), GaAs devices operate stably at ambient temperatures significantly above 300°C.[85] Moreover, GaAs has higher electron mobility (6 times) and saturated drift velocity (2 times) compared to Si, which facilitates device operation at microwave frequencies.

Other major advantages are that GaAs substrates can be semi-insulating with resistivity up to 10^8 ohms-cm that results in low parasitic capacitances and minimizes device isolation problems. Additionally, GaAs is a direct band gap semiconductor enabling efficient light emission for optoelectronic devices.[86] All these advantageous electrical properties have led to advancement of several GaAs devices which include: metal semiconductor field-effect transistors (MESFETs), monolithic integrated microwave circuits (MMICs), high electron mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs), and photonic devices such as laser diodes and light emitting diodes (LEDs).

Since the initial development of high-frequency GaAs devices designed for elevated temperatures and high current density operation, Au has been the exclusive metallization for interconnects and contacts in GaAs ICs. Of importance to device performance is the ohmic contact formation at the GaAs semiconductor-metal conductor interface. Approximately half of the total (parasitic) source resistance in a GaAs FET may be due to the metal contact.[86] At the metal-semiconductor interface, a potential barrier height to electron flow exists, which in theory can be lowered by matching the work function of the metal to that of the semiconductor. Yet it is found that compound semiconductors such as GaAs have a barrier height essentially independent of the work function of the metal due to the large density of surface states.[87] In practice, an ohmic contact is achieved when the GaAs surface layer is highly doped by diffusing in a dopant supplied from the alloyed contact metal, thus forming a very narrow depletion region that allows electrons to tunnel through the barrier. In the search for a low resistance, linear and thermally stable ohmic contact for n-type GaAs devices, it was found that an eutectic alloy of gold-germanium (AuGe) along with nickel (Ni)

was successful.[88] The AuGe-Ni alloy uniquely remains as the superior ohmic contact material for n-type GaAs devices while optimization of film thicknesses and process improvements offered additional increases to device performance.

In addition to its vital role in GaAs ohmic contacts, Au metallization provides several attractive properties for high-powered radio frequency (RF) ICs. At high temperatures, Au does not oxidize like Al and Cu films, thereby permitting electrical current flow on the top surface as is perpetuated by the alternating current skin effect in RFICs. Furthermore, implementing an all Au metallization avoids the thermally unstable $AuAl_2$ intermetallic (purple plague) formation that occurs when Au wires are connected to Al bond pads. The higher electrical (~20% better than Al) and thermal (~25% better than Al) conductivity properties of Au are much more desirable for interconnects because of reduced power losses. Moreover, the thermal expansion coefficient of Au (~63% lower than Al) is the lowest of all conductor metals, providing significantly less expansion and therefore stable interfaces with dielectric films during thermal processing. Au films clad with a thin TiWN barrier layer provide good adhesion and diffusion barrier properties for embedding within Si dielectric films. Also, the TiWN barrier layer resists intermetallic formation at high temperatures preventing degradation of the low resistivity Au film. Additional benefits of Au are that thick films can be deposited by electroplating because of the rapid deposition rate, and recovery of excess Au is recycled from within the plating bath. Of most significance, Au interconnects exhibit superior resistance to electromigration compared to Al, making them desirable for high current and high temperature microelectronic applications. Specific studies on electromigration in passivated electroplated Au films are absent in the literature, and therefore are the subject of this research.

2.4 Review of Electromigration in Gold Films

Although an abundance of thin film electromigration studies since the mid 1960's have improved our understanding of this failure mechanism, most of these studies were focused on Al and AlCu interconnects on silicon ICs. More recent electromigration research beginning in the 1990's concentrated on Cu thin film reliability because Cu replaced Al for interconnections on advanced silicon CMOS ICs. The study of electromigration in Au thin films emerged in the late 1960's, but its scope was primarily limited to non-passivated and evaporated films. Research on actual passivated electroplated Au interconnects in GaAs semiconductor devices is still lacking in published literature, even though it is critical to understand the electromigration reliability of these devices. This section provides a review in chronological order of the experimental methods and results of previous investigators in the study of electromigration in Au thin films.

One of the earliest experimental methods for studying electromigration in bulk pure metals was marker motion under high electric currents. Huntington and Grone[6] were the first to carry out experiments on bulk pure Au wires using the marker motion method. Originally these researchers[6] examined Cu wires, but were frustrated by the lack of reproducibility in the results, suggesting that inadequate protection of the samples led to Cu oxidation. As a result, Huntington and Grone's[6] efforts naturally transitioned to Au wires because of the superior oxidation resistance of Au. In these experiments, Au wires within a chamber (under a positive Argon atmosphere) were affixed to avoid any mechanical stresses that arose from thermal expansion and contraction. Transverse scratches (markers) made with a razor blade on the Au wire surface were optically monitored while being subjected to electrical currents of 30 and 60 amps.

At these high currents on bulk Au wires, elevated film temperatures of 850°C to 1000°C were generated and measured by an optical pyrometer. Throughout the experiments, markers were measured with a Hilger linear comparator microscope and recorded daily. For each marker measurement, the ratio of velocity to current density was logarithmically graphed against the reciprocal of the absolute temperature. Huntington and Grone's[6] data graph is reproduced in Figure 2.6.

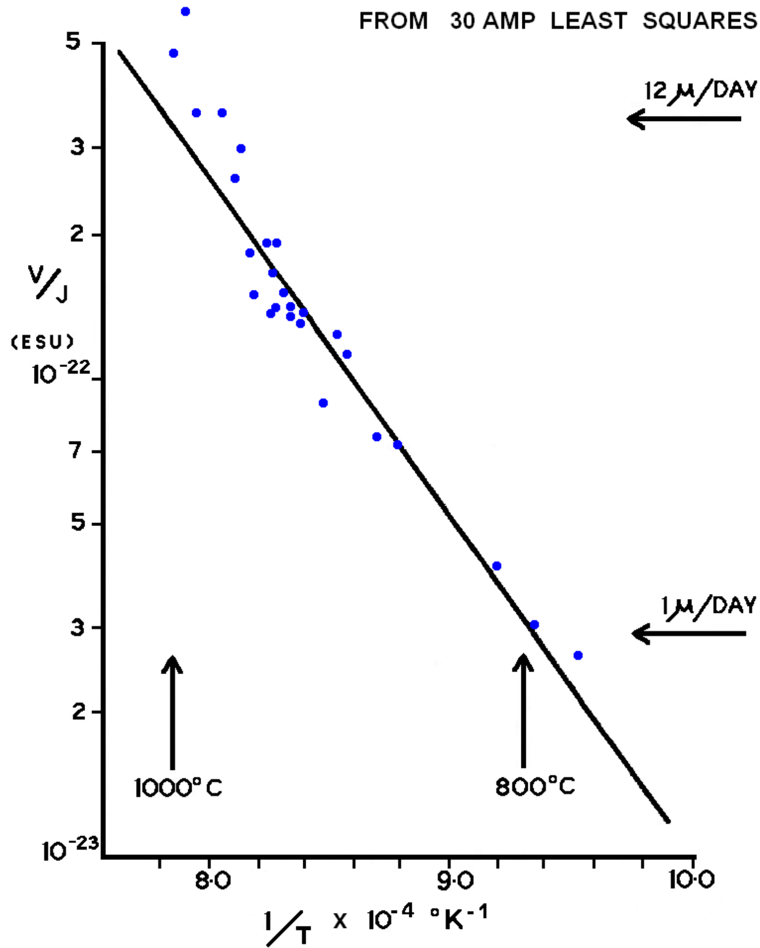


Figure 2.6 Huntington and Grone's[6] Au marker motion (*v* / *J*) versus 1 / T graph.

The activation energy of 35 kcal / mol (20% of self-diffusion in gold) was obtained by a least squares regression of the two data sets graphed. Converting to units of electron volts, it is equivalent to 1.52 eV, which is considered very high for grain boundary or surface electromigration, but closer to bulk lattice diffusion. Admittedly, inaccuracies associated with the indirect optical temperature measurements could explain the discrepancies. Nevertheless, the pioneering measurements of Huntington and Grone established that the direction of mass transport is consistent with the theory of momentum exchange from electrons, causing electromigration of metal ions in the direction of the electron flow.

Since bulk Au wire studies induce vastly higher temperatures than experiments involving Au thin films deposited on insulating materials, it follows that diffusion pathways and electromigration properties are measurably different. Therefore, experiments conducted on Au thin film layers that closely match actual IC interconnects yield more accurate electromigration information for determining metallization reliability. In review of the following studies, emphasis will be on the experimental stress conditions and Au film properties that are not characteristic of Au interconnections in IC devices. In one of the first electromigration studies involving Au thin films on silicon substrates, Hartman and Blair[89] conjectured that temperature gradients along the test structures may be more important than structural properties. Their study also observed that Au grain boundary erosion and mass depletion occurs on the negative (cathode) end of the test structure, which is consistent with the electron wind theory. In another study, using an in-situ SEM technique[90] to characterize the Au film surface during electromigration, voids formed at the cathode and hillocks formed near the positive (anode) end. Neither of these studies measured activation energy.

In 1971 Hummel and Breitling[91] published results, contradicting previous observations by finding that applied currents in Au thin films caused ion migration towards the cathode, which is opposite to the electron wind direction. Hummel's Au test structures were vapor deposited onto glass microscope slides under vacuum and tested with a current density of 0.7 MA/cm^2. Three techniques were used to observe the Au mass transport; (1) resistance changes measured in five sections, (2) displacement of radioactive ^{198}Au atoms, and (3) SEM micrographs taken of the cathode and anode regions. These three methods led University of Florida investigators to conclude that ion movement occurs towards the cathode because voiding was found on the anode end. This contrary result was rationalized by the argument of higher concentrations of electrons in the grain boundaries raises the Fermi energy, which in turn changes the type of conduction. In effect, the drag force due to electron holes becomes larger than the electron wind force, causing a reversal in the direction of electromigration. A great controversy ensued with researchers in industry over Hummel's reported findings.

Blair and co-workers[92] at Texas Instruments provided experimental data on the electromigration lifetime of sputtered Au films. A TiW and Au metallization stack with good adhesion to SiO_2 and better compatibility with silicon device processing was evaluated. Au films of 0.8 μm thick with a 0.1 μm TiW underlayer were sputter deposited onto silicon substrates. These Au films were subjected to current densities from 2.0 to 3.5 MA/cm^2 with a 150°C ambient temperature. A lifetime test method yielded mean time to failure data that showed an order of magnitude longer lifetime than Al films. Activation energy of 0.9 eV was estimated for these Au films by comparison with Al films. Additionally, all

sputtered Au film structures failed near the cathode end in disagreement with Hummel's observation. Yet subsequent studies by Hummel[93] and Breitling[94] continued to observe failures near the anode for Au, as did Cu and Ag thin films deposited on glass microscope slides.

Gangulee and d'Heurle,[95] researchers at IBM, were among the first to examine electroplated Au films using silicon substrates covered with a thin Ni / Fe underlayer base alloy. In this study, these researchers applied an extremely high current density of 6 MA/cm^2 generating significant Joule-heated film temperatures between 202°C and 293°C, potentially causing overstressed failure mechanisms. Also, the Au films were not covered with dielectric passivation and the Ni / Fe underlayer is known to form intermetallic alloys with Au. Still a realistic activation energy of 0.88 ± 0.06 eV was obtained by the fitted slope of the mean failure time data graphed against the inverse of temperature, which is shown in Figure 2.7.

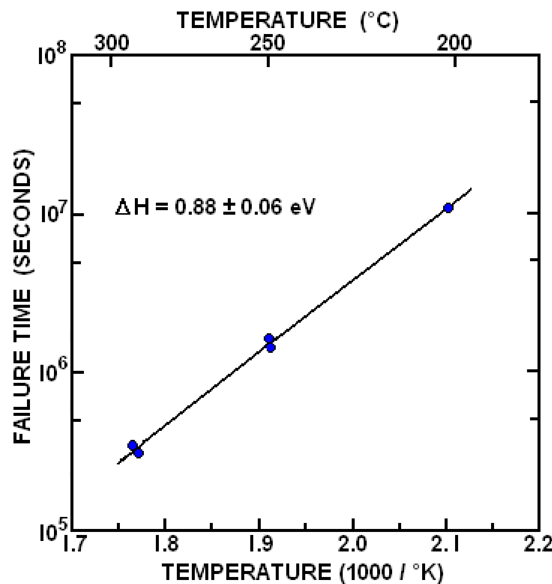


Figure 2.7 Gangulee and d'Heurle's[95] failure times versus inverse temperature.

Another study by Klein[96] employed an in-situ TEM technique to measure the void formation rate in evaporated Au films by taking micrographs over time. Au films were stressed at current densities from 1.8 to 2.5 MA/cm^2 corresponding to Joule-heated temperatures of 210°C to 350°C, which are considered reasonable conditions. Based on this void growth method, Klein calculated average metal ion drift velocity (v) from the fitted slope of the void surface area versus elapsed time divided by line-width. Thus, according to the Huntington and Grone[6] theory, graphing the ln(v / J) versus inverse temperature results in a straight line slope equal to -E_a / k. The activation energy obtained by this method was 0.8 ± 0.2 eV which is in fair agreement to both Blair[92] and Gangulee[95]. It is proposed within this activation energy range (nearly half of the 1.81 eV Au self-diffusion value) that grain boundary diffusion is the dominant mechanism. Further, Klein observed that the void formation always occurred on the cathode region with hillocks forming on the anode region. Although this study used a thin underlayer of Cr for better adhesion to substrate, Cr impurities within the Au increased the film resistivity and potentially changed the electromigration properties.

Up until this time, electromigration studies on Au thin films consisted of very small sample size experiments upon which statistical conclusions were derived. A study by English and co-workers[97] at Bell Laboratories had a relatively large sample size of 50 Au film structures tested in series with the resistance monitoring method. Extremely high current densities ranging from 2 to 8 MA/cm^2 with an ambient temperature of 180°C were applied to shorten test times. All Au film structures were tested to open circuit that caused excessive Joule heating and failure time distributions were observed to have considerably

wide variation. A key finding of this study was the initial slopes of the resistance versus time measurements were linear and inversely correlated to Au film lifetime. While English's investigation concluded that Au film lifetime is dependent on current density to the inverse fourth power, this is considered highly questionable because of the enormous scatter in the data and the extensive Joule heating not accounted for in the measurements. Experimentally extracted current density exponents (*n*) above 2 have to be scrutinized as not correcting for excessive Joule heating that elevates the actual metal film temperatures.

Given that direct experimental methods to evaluate electromigration in Au thin films entail inspection of the films' surface for void formation, these direct observation tests prohibit examining the effect of passivation overlayers on Au films. It has been shown that the electromigration lifetimes of Al thin films was improved significantly with SiO_2 passivation covering the films' surface.[21, 22] It is presumed that lifetime improvement also applies to Au thin films with passivation overlayers, but in order to evaluate this postulation requires indirect experimental methods such as the resistometric technique. Since surface electromigration may operate to a great extent in non-passivated thin films, it is important to examine conductor films with dielectric overlayers as is typical of ICs. Breitling and Hummel[94] employed the resistometric technique where resistance was monitored within five segments of a Ag thin film structure to reveal that silicon oxide overlayers prolonged lifetimes by about 30%. Agarwala[98] at IBM examined sputtered Au thin films that were 0.8 μm thick with underlayers and overlayers of inert molybdenum (Mo) and tantalum (Ta) thin films. Mo films are preferred due to the very low solid solubility in Au which prevents intermetallic formation and subsequent resistivity decay. Both these overlayers were found to substantially

improve Au film lifetimes as the degree of surface coverage increased. Agarwala reported a lower activation energy for the covered Au films, but stated high stress currents caused thermal runaway. Still surface diffusion was suggested as the dominant mechanism for electromigration in Au thin films. In this study, a current density exponent of 3.3 clearly indicates severe thermal gradients existed and Au film temperatures were inaccurately measured, thus an invalid current density exponent was obtained. Even so the importance of this study was that passivated Au thin films had improved lifetimes warranting further investigation.

Based on the same experimental method that discovered the electromigration induced backflow force in Al films, Blech and Kinsbron[57] evaluated sputtered Au thin films. Current densities from 0.1 to 1.0 MA/cm^2 were passed through Mo thin films that divert into a much higher conductivity Au layer with test temperatures between 260°C to 500°C. The premise of this experimental method is that observations of a more rapidly transported conductive Au layer on top of a relatively inert Mo base metal are measurable. A glass window in the vacuum chamber allowed microscopic measurements of the edge displacement in the Au film. Figure 2.8 illustrates the Au thin film structure configuration tested by Blech and Kinsbron.

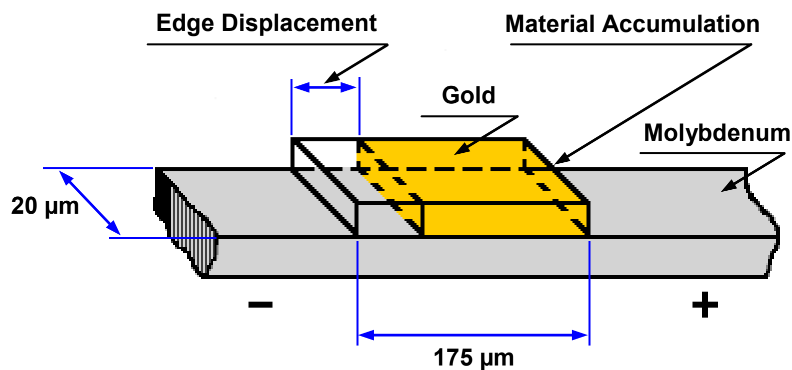


Figure 2.8 Blech and Kinsbron's[57] Au thin film structure configuration.

The Au edge displacement was assumed to be equivalent to the average drift velocity that depends exponentially on temperature and directly proportional to current density. A wide range of activation energies (0.6 to 0.9 eV) were obtained suggesting difficulty in making exact measurements with this drift velocity method. Mass transport of Au was always observed in the direction of electron flow, contrary to Hummel's earlier results.

In another study by Blech and Rosenberg[99] to provide clarification on the controversial topic related to direction of electromigration, evaporated Au films were examined with different substrates. Indeed, Hummel's results of voids forming at the anode region were reproduced, but only for Au thin films deposited directly on glass slides. In contrast, all other Au thin films with Mo underlayers deposited on silicon substrates failed at the cathode end in agreement with the direction of the electron-wind theory. Blech suggested Au films deposited on cold glass slides are structurally unstable at test temperatures as low as 250°C, and that the existence of non-equilibrium grain boundary structures during powering undergo transformation causing precipitous void formation in the anode region. A further investigation by Blech and colleagues[100] of a 1 μm thick Au film with adhesion underlayers of 20% Cr / 80% Ni on sapphire substrates showed that failures occurred at the cathode, in accordance with ion migration assisted by electron flow.

In an attempt to address Blech's experimental conclusions, Hummel and DeHoff[101] examined Au films deposited on glass substrates with Mo or Cr underlayers that subsequently received high-temperature anneals. Assuming that grain boundary growth was the rationale as pointed out by Blech[99] for the reversal of ion migration against the electron flow, these high-temperature

anneals were aimed at promoting Au film microstructure stability during testing. Hummel's results from the Au film specimens with Cr underlayers showed failures at the cathode region in agreement with Blech. However, it was suggested that Cr impurities detected by Auger analysis throughout the Au film somehow causes Au ion flow in the direction of electrons. It was demonstrated again by Hummel[101] that "pure Au" films fail at the anode indicating Au ion flow against the electron flow. An additional study by Hummel and Geier[102] employing the resistometric method measured abrupt resistance increases that were attributed to Au film void formations in the anode region. These experiments had non-extreme practical stress conditions of 0.63 MA/cm^2 and temperatures in the range of 250°C to 390°C. In this temperature range, Hummel measured 0.98 eV for activation energy residing on the high end of reported values.

In an extension of Blech and Kinsbron's earlier investigation[57] employing edge displacement measurements in Au films, the researchers reported[103] two new significant findings. Specimens were prepared with a 0.1 μm thin sputtered Au film with an equivalent thickness Mo underlayer deposited on top of silicon substrates. The average Au drift velocity was measured as a function of temperature (250°C to 430°C), current density (0.1 to 2.0 MA/cm^2), and specimen length. Empirical results showed that a current density threshold exists for electromigration in Au films and its value was found to be inversely proportional to the Au film length. Secondly, Au film edge displacement was found to be linearly proportional to time at any given current density and temperature, suggesting an incubation time may exist before electromigration damage occurs. But it is highly questionable whether edge displacement measurements are capable of monitoring microscopic changes within the Au

films. A much more perplexing result of this study was on specimens that were deliberately co-sputtered with Au and 10% volume of Mo. Since Mo is almost entirely immiscible within Au it should segregate at experimental temperatures and perhaps hinder electromigration. Indeed, the rate of electromigration was reduced with addition of Mo but a confounding reversal in drift direction was noticed.

Deemed as the first direct measurement of grain boundary ion drift velocity, Tai and Ohring[104] embedded a radioisotope of ^{195}Au tracer into Au thin films. The ^{195}Au tracer transport was measured by an autoradiography technique using a SEM over a temperature test range of 120°C to 250°C. As a result of this tracer method, Au ion transport was found to be predominately through grain boundaries as indicated by the derived activation energy of 0.80 ± 0.03 eV. It was also shown that Au ion transport is directed from the cathode to anode which refutes Hummel’s findings that were in opposition to the electron-wind theory. Yet a study by Lloyd[105] repeated Hummel’s results of void formations at the anode region, but used the same microscope glass as substrates on which the Au films were deposited. A more noteworthy observation of Lloyd’s research was the pre-existence of nanoscale voids in the as-deposited pure Au thin films. It was observed by TEM that these nanoscale voids do not coalesce to contribute as a vacancy source for the electromigration-induced larger voids that grow in the grain boundaries ultimately causing Au film failures. Miller and Gangulee[106] explored various underlayers to improve electromigration lifetimes in Au films. Lifetime increased with niobium (Nb), hafnium (Hf), and zirconium (Zr), with Nb being the most effective underlayer. However, diffusion of these elements increased Au film electrical resistivity, thus any lifetime benefit is outweighed.

Revisiting the controversial debate on the direction of Au ion transport and location of electromigration-induced void formations, Hummel, DeHoff, and their students published a number of reports.[107-110] These reports provided critical information in resolving the conflicting empirical observations on Au films. Upon discovering that pure Au films deposited on quartz (nearly pure SiO_2) glass substrates failed on the cathode side of the stripe, Hummel focused research on minor constituents potentially affecting the Au ion transport and failure site. As it turns out, microscope glass slides used as substrates for depositing Au films are composed of soda-lime silicate glass. Auger electron spectroscopy of Joule-heated samples revealed that the sodium constituent in microscope glass substrates diffuses through the Au film and results in reversal of the failure site. Several other minor solute elements were evaluated for influence over the failure site in Au films. Table 2.5 summarizes the Auger analysis and failure site results obtained by Hummel.[107]

Table 2.5 Summary of the solute effects on the Au film failure site.[107]

Substrate	Deposited Solute	Heat Treatment	Auger results for the Au films	Failure Site
Quartz	Sodium (Na)	1.5 hours at 350°C plus Joule heating	Na on surface and in Au film; mostly on surface near center	Anode (+)
Quartz	Indium (In)	2 hours at 350°C plus Joule heating	Only small amounts of In; no Na	Anode (+)
Soda-lime Glass	None (Na in glass)	100 hours of Joule heating at 150°C	Na on surface	Anode (+)
Soda-lime Glass	None (Na in glass)	No heat treatment	Virtually no Na on surface; none in film	Not tested
Soda-lime Glass	None (Na in glass)	72 hours at 100°C in furnace	Na on surface; virtually none in Au film	Not tested
Soda-lime Glass	None (Na in glass)	5 hours at 300°C	Most Na near surface; virtually none in Au film	Not tested
Soda-lime Glass	Chromium (Cr)	Joule heating	Cr and traces of Na in Au film	Cathode (-)
Soda-lime Glass	Molybdenum (Mo)	24 hours at 400°C	No Mo in Au but traces of Na on surface	Cathode (-)

Based on the Auger analysis of the Au films and the failure site results, Hummel reported that solute elements (Na and In) with ionization energies approximately less than 6 eV cause reversal of the Au film failure site. No reversal of the failure site was observed for solute elements (Mo and Cr) possessing ionization energies above 6 eV. At this time, a proposed mechanism for the reversal effect was not given.

Examination of grain boundary grooving, thermal migration, and electromigration mechanisms to determine which are responsible for void formation in doped and undoped Au films was undertaken by Hummel.[108] Upon isothermal anneals of pure Au films, voids formed without temperature gradients or current flow indicating grain boundary grooving effects. Still, thermally annealed Na doped Au films showed greatly enhanced grain boundary grooving, but this cannot explain void formations in the anode for current stressed Au films. Alkali metals such as potassium were discovered to accumulate in the anode and to accelerate grain boundary grooving and void formations in the anode for alkali doped Au films under current flow.[109] Hummel proposed some explanations for the role of Na on the failure site reversal. It was speculated that Na reduces the electron-wind magnitude allowing Coulomb forces to migrate Au ions toward the cathode which should improve Au film lifetime, but instead Na solutes were found to sharply decrease lifetime. Another supposition was that rapidly diffused Na in Au is transported by the electrostatic force causing a "Na^+ wind" to migrate Au toward the cathode. However, electron-wind forces not only migrate Au ions but rapidly transport alkali impurities to the anode in Au films.[110] A final explanation is that Na changes the electronic structure within the grain boundaries allowing positive charge carriers (holes) to cause net flow of Au ions toward the cathode.

Early implementation of Au-based metallization originated due to its superior low resistance ohmic contacts on GaAs devices, yet extensive reliability data for Au interconnects proven to handle higher current densities and elevated operating temperatures was forthcoming. A study by Eden[111] compared electroplated Au lines versus evaporated Al lines and found that Au lines projected longer operational lifetimes (10^4 times). Superior reliability has been demonstrated with Au films; however, an intermediate layer is essential to serve as a diffusion barrier and adhesion layer for dielectric films in ICs. Kim and Hummel[112] looked at various barrier underlayers for Au thin film stability during thermal annealing. Both oxidation tendency and stress induced by thermal expansion of the underlayers were seen as important factors. Based on these factors, tin (Sn), indium (In), and titanium (Ti) underlayers provided better stability for Au films than copper (Cu), nickel (Ni), and vanadium (V). As a matter of practicality, the microelectronic industry selected Ti and TiW underlayers for ease in processing and providing micro-structural and electrical stability for Au films.

One of the first studies on electromigration in Au films on GaAs substrates was reported by Tang.[113] Au films of thickness 0.26 μm were thermally deposited on semi-insulating GaAs substrates without the use of barrier underlayers. The resistometric method was used to characterize the electromigration process with a rather high current density stress of 3 MA/cm^2 and temperatures between 221°C to 258°C. In the early stages of electromigration the relative resistance change increased linearly with time as previously reported by English[97] and Hummel[102] for Au thin films. For constant time and current density, the resistance change exponentially increases with higher temperatures yielding an activation energy of 0.73 eV.

Scanning probe microscopy techniques (scanning tunneling and atomic force microscopes) emerged in the 1980's to characterize material surfaces. These new experimental techniques were expected to provide insight into thin film electromigration phenomena. Many researchers[114-117] sought to capitalize on these advanced techniques for characterizing electromigration in Au thin films. Indeed, these techniques proved feasible in monitoring electromigration in thin films.[114] The main results obtained center on observations that Au surface morphology rearranges under stress currents and relieves film strain in forming electromigration-induced voids.[115, 116] While this work provides high-resolution images on surface changes during electromigration, it is deficient in measuring internal grain boundary diffusion and evaluation of passivated Au film lifetimes.

A more recent investigation employing the resistometric method to evaluate the early stages of electromigration in evaporated Au films was published by Bai and Roenker.[118] Carefully designed Au test structures with varying line lengths and a 0.08 μm film thickness were created by e-beam evaporation and standard photolithography liftoff procedures. Au films were deposited on top of a coated polyimide layer on silicon substrates. Bai and Roenker's results concurred with previous findings that initial resistance change tracks linearly, but the resistance data also showed a saturation tendency in the early (< 4 hours) stages. A model was devised that described the saturation effect in relation to the physical parameters. This model predicted a linear dependence on current density, yet the experimental data yielded a current density exponent of 1.5. This study deviated from actual Au interconnects produced in industry because of the use of uncharacteristically very thin Au films (< 0.1 μm) without passivation and underlayers of non-inert polyimide films.

A more relevant study on 1.4 μm thick electroplated Au films with a Si_3N_4 passivation was reported by Croes.[119] High-resolution resistometric equipment was employed to examine the electromigration in the electroplated Au films at low percentage (~ 0.1%) changes in resistance. A wide range of stress conditions (0.2 – 6.0 MA/cm^2 and 160°C – 300°C) were evaluated to determine the applicability and validity of Black's equation under these conditions. Black's equation was found to apply over a wide stress range for Au films. Croes estimated an activation energy of 0.68 ± 0.09 and a current density exponent of 2.0 ± 0.51. This study followed a two-step procedure wherein a reduced sample size and test time reduction was achieved. However, some major inadequacies of this investigation were the non-disclosure of the underlayer and substrates and the lack of a statistically significant sample size for determining the median failure time and the failure distribution spread (sigma).

Whitman[120] published the latest investigation on electromigration in passivated electroplated Au films. This experimental investigation also employed the resistometric method and included a sufficient population of 300 Au test structures on which the activation energy of 1 eV and a current density exponent in the range of 2 to 4 was reported. A major drawback of this study was the application of extremely high current densities from 5 to 7 MA/cm^2. As a result, the current density exponent extracted was much greater than 2, indicating Joule-heated film temperatures were not appropriately measured. Application of such excessively high currents causes overstressing with massive Joule heating and failure wear-out mechanisms not representative of the failure modes observed under normal operational conditions.

2.5 Gold Electromigration Review Summary

In this review of past investigations, it was shown that a multitude of experimental methods, stress conditions, and film layer preparations yielded varied electromigration model parameters for Au films. Table 2.6 summarizes the electromigration studies in Au films for various experimental methods, stress conditions, and film layers. Unfortunately, most of these past studies employed experimental methods with inherent control problems, test structure limitations, and measurement inaccuracies. This is exemplified by the open circuit lifetime experimental method that allows current densities to increase as large voids form in Au interconnects leading to thermal runaway and catastrophic failures. Furthermore, the experimental methods (void growth and edge displacement) purported to be direct observation techniques are limited to Au interconnect test structures without passivation allowing surface diffusion, which is irrelevant on actual passivated Au interconnects in ICs. Even the most recent studies utilizing the high-resolution resistometric experimental method were regrettably stressed with excessively high current densities that resulted in significant Joule heating and current density exponents above the physically valid range of 1 to 2.

Because these previous studies inherently lacked control over the electromigration stress conditions, the accuracy of the extracted electromigration model parameters are in question. Almost all of these past studies were limited to non-passivated Au films which are not representative of Au interconnects embedded in microelectronic devices. Therefore, the motivation of this doctoral research investigation was to obtain accurate electromigration model parameters on electroplated passivated Au interconnects in order to understand the electromigration reliability of high-powered GaAs RF microelectronic devices.

Table 2.6 Au electromigration results for various experimental methods.

Authors	Experimental Method	Stress Conditions	Deposition Method	Underlayer / Substrate	Passivation	Activation Energy	Current Density Exponent
Huntington and Grone[6]	Marker Motion	0.01 MA/cm^2 850°C – 1000°C	Au bulk wire	None	No	~1.52 eV (35 kcals/mol)	Not obtained
Blair et al.[92]	Lifetime	2 – 3.5 MA/cm^2 150° + Joule-heat	Sputtered 0.8 µm Au	0.1µm TiW / Silicon	No	0.9 eV	Not obtained
Gangulee and d'Heurle[95]	Lifetime	6 MA/cm^2 202°C – 293°C	Electroplated 1.3 µm Au	0.02 µm NiFe / Silicon	No	0.88 ± 0.06 eV	Not obtained
Klein[96]	Void Growth (in-situ TEM)	1.8 – 2.5 MA/cm^2 210°C – 350°C	Evaporated 0.05 µm Au	0.01 µm Cr / Silicon	No	0.8 ± 0.2 eV	Not obtained
Agarwala[98]	Resistometric	1.7 – 5.5 MA/cm^2 254°C – 354°C	Sputtered 0.8 µm Au	0.05 µm Mo / Silicon	SiO_2 / Mo	0.75 ± 0.05 eV	3.3 ± 0.49
Blech and Kinsbron[57]	Edge Displacement	1 MA/cm^2 260°C – 500°C	Sputtered 0.1 µm Au	0.1 µm Mo / Silicon	No	0.6 ± 0.3 eV	Not obtained
Etzion et al.[100]	Lifetime (Optical/SEM)	0.8 – 1.15 MA/cm^2 200°C – 500°C	Evaporated 1 µm Au	0.02 µm CrNi / Glazed Alumina	No	0.42 ±0.02 eV	Not obtained
Hummel and Geier[102]	Resistometric	0.63 MA/cm^2 250°C – 430°C	Evaporated 0.17 µm Au	None / Soda-lime glass	No	0.98 eV	Not obtained
Kinsbron et al.[103]	Edge Displacement	0.1 – 2 MA/cm^2 250°C – 430°C	Evaporated 0.1 µm Au	0.1 µm Mo / Silicon	No	0.7 ± 0.03 eV	Not obtained
Tai and Ohring[104]	^{195}Au Tracer SEM	0.8 – 2 MA/cm^2 120°C – 250°C	Evaporated 0.5 µm Au	0.05 µm Mo / Sapphire	No	0.80 ± 0.03 eV	Not obtained
Tang et al.[113]	Resistometric	3 MA/cm^2 221°C – 258°C	Evaporated 0.26 µm Au	None / GaAs	No	0.73 ± 0.1 eV	Not obtained
Croes et al.[119]	Resistometric	4.3 MA/cm^2 265°C	Electroplated 1.4 µm Au	Not reported	Si_3N_4	0.68 ± 0.09 eV	2.0 ± 0.51
Whitman[120]	Resistometric	5 – 7 MA/cm^2 75°C – 160°C	Electroplated 1.0 µm Au	TiPt / GaAs	SiO_2	1 eV	~ 2 – 4

CHAPTER 3 EXPERIMENTAL METHODS

In this chapter, the experimental procedures and methods undertaken in this research are described. This encompasses test structure design, fabrication of the Au interconnects, and the packaging assembly procedures. An overview of the experimental electromigration test equipment, test methods, and stress conditions are provided. Fundamental aspects of the experimental methods along with the statistical data analysis methods are given. It is emphasized throughout this chapter that this research was carried out in five sequential experimental phases (I – V) composed of incremental improvements in test structure design and stress condition optimization.

3.1 Test Structure Design

Investigation of the electromigration phenomena in thin metal film interconnects has been facilitated by the use of optimized metal test structures that were designed and processed in semiconductor fabs. Metal test structures have evolved over the years to study the electromigration failure mechanism. These test structures were developed to measure electromigration lifetimes and intended to represent typical interconnect circuit elements found in ICs. The earliest electromigration test structures studied were thin Al lines that were not covered with dielectric passivation films.[11, 12] Afterward the encapsulation of Al thin films with silica glass (SiO_2) passivation prolonged electromigration lifetimes by an order of magnitude.[21, 22] Another common passivation overlayer on metal interconnects is silicon nitride (SiN) which was shown to inhibit the growth of hillock formations (metal extrusions) and decreased the electromigration rate.[24]

Dimensional considerations for interconnect test structures are very important in order to conduct proper electromigration studies. A critical line length effect was observed by Blech[24] (known as Blech Length). It was attributed to the mechanical stress buildup in the metal line causing a back flow that opposes the electromigration induced mass flow. Test structures have been designed to be much longer than 100 microns (μm) to avoid the Blech Length effect. Because there were many differently designed test structures used in the early days of studying electromigration, an effort to obtain accurate and reproducible electromigration results within the semiconductor industry emerged. A standardized electromigration test structure known as the NIST (National Institute of Standards and Technology) test structure was designed and recommended[121] for reproducible electromigration results. Figure 3.1 provides the basic design elements of the NIST electromigration test structure.

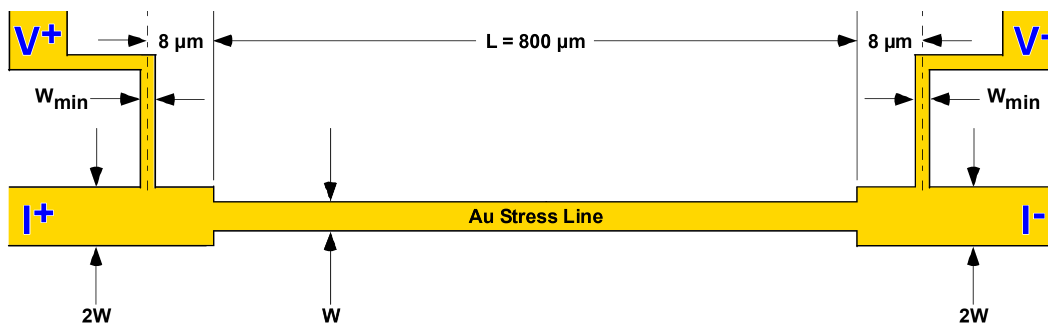


Figure 3.1 NIST electromigration test structure schematic.

The NIST test structure uses a four-terminal Kelvin-sensed layout to prevent measurement interference from contact resistance. The length (L) of the stress line is recommended to be 800 μm. The recommended line-width (W) is dependent on the minimal technology dimensions and metallization grain size. The structure ends (current taps) have a recommended (2W) increased width to

confine wear-out in the stress line portion. Since almost all semiconductor devices are composed of multi-level metallization interconnects, single-level metallization structures (NIST test structures) do not provide a realistic representation of the current flowing in multi-level metallization ICs. It was discovered that electromigration lifetimes of two-level metal test structures where current is flowing through tungsten (W) filled vias were less than half that of NIST test structures.[122-124] As a consequence of measuring electromigration lifetimes on NIST test structures, the worst case reliability of the IC metal interconnections are not accurately predicted and the operational lifetime is overestimated. Therefore, electromigration test structures evolved to incorporate metal stress lines that terminate with W-filled vias. Barrier (Ti, TiN, and TiW) layers are employed for multi-level metallizations for adhesion and to prevent metal ion diffusion within the surrounding dielectric layers. Figure 3.2 illustrates a two-level electromigration test structure with W-filled vias.

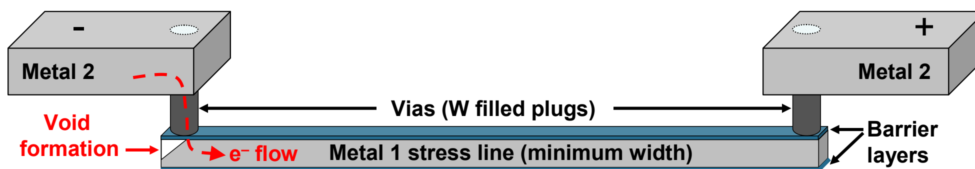


Figure 3.2 A two-level metal via electromigration test structure illustration.

The shorter electromigration lifetime observed in two-level via test structures compared to NIST test structures reflects the effect of current crowding at the W-filled via. Increased current density and the associated localized Joule heating at the interface between the W-filled via and metal stress line are the driving forces causing metal ions to migrate away from the interface.

These via test structures develop void formations that are considered drift velocity electromigration failures and resemble a more realistic interconnect wear-out mechanism for a typical IC layout.

The electromigration test structures designed and examined in this investigation of gold electromigration incorporated features of the standard NIST test structure. The first test structures evaluated in phase I of this study were 800 μm long electroplated gold lines with voltage and current taps connected to bond pads. A design improvement with the current taps being tapered was implemented on this Au test structure. This modification eliminates abrupt current density transitions, thus reducing current crowding at the corners entering the stress line and thereby minimizing localized Joule heating. In addition, a via test structure containing two-level electroplated gold lines was also examined.

In experimental phase II, dual Au test structures were designed and incorporated in a photo mask set to double the samples of the experiment. The experimental sample size was increased from 30 devices under test (DUTs) to 60 DUTs. Figures 3.3 and 3.4 show optical images of the dual NIST line and via test structures examined in phase II.

Figure 3.3 Dual NIST line (2 μm wide by 800 μm long) test structures.

Figure 3.4 Dual centered via (metal 1 / metal 2) test structures.

Another feature of the dual NIST line test structures was the addition of unconnected extrusion monitor lines (not distinctly visible in Figure 3.3) on adjacent sides of the stress line. These unconnected extrusion monitor lines promote uniformity during the gold electroplating deposition, photolithography, and etching processes. The centered via test structure shown in Figure 3.4 was designed to include both metal 1 and metal 2 line segments. Both metal line segments were 5 µm wide and 400 µm long, making the entire test structure 800 µm long. These metal (metal 1 / metal 2) line segments terminated at a centered via, permitting current to be forced in either direction to evaluate electromigration wear-out at the via 1 / metal 1 (V1M1) or the via 1 / metal 2 (V1M2) interfaces.

In experimental phases (III – V), redesigned electromigration Au test structures were implemented. Several improvements were included on this final test structure design. The most significant modification was shortening the stress line length from 800 µm to 450 µm in order to reduce resistance variation due to film thickness non-uniformity from the electroplating process. This line length is still significantly longer than the critical Blech length. Another benefit of the shorter stress line design was aiding the identification of the failure location. The final test structure layout contained bond pads for current force, voltage sense, and extrusion sense connections that were linearly configured.

Complexity of the wire bond routing was reduced with this linear bond pad configuration. The adjacent extrusion monitoring lines were electrically connected to designated bond pads but these extrusion lines were not monitored in this study. The via test structure length was also shortened to 450 μm and has the same linear bond pad configuration. However, the design was modified to include symmetrical terminating vias on opposite ends of the stress line. Optical images of the final metal 1 (M1) line and via 1 / metal 1 (V1M1) test structures designed for this investigation are displayed in Figures 3.5 and 3.6.

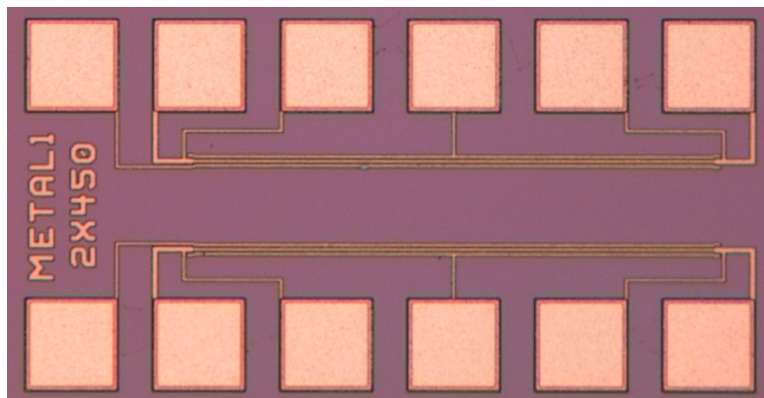


Figure 3.5 Metal 1 line (2 μm wide by 450 μm long) test structure design.

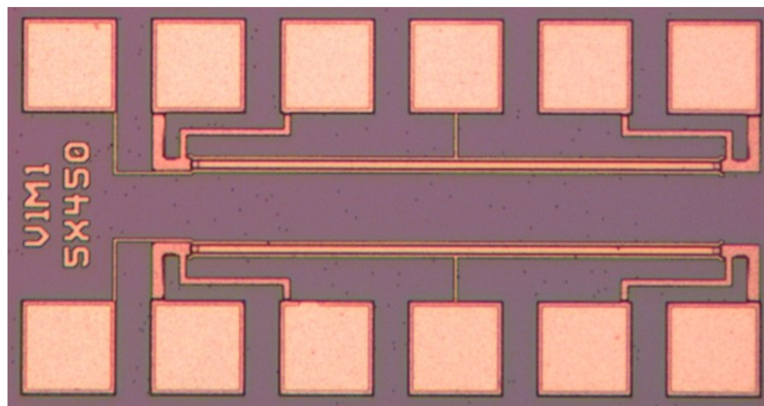


Figure 3.6 Via1 / Metal 1 (5 μm wide by 450 μm long) test structure design.

The V1M1 test structure design is intended to stress and cause wear-out at the via 1 / metal 1 interface whether the current is forced through either end of the structure. This wear-out and void formation at the V1M1 interface is illustrated in Figure 3.2. Current is fed from twice as wide metal 2 lines with much lower current density before entering the V1M1 interface. Both of these test structures were designed to permit four-terminal Kelvin sensing with isolated current and voltage bond pads to eliminate the impedance contribution of the wiring and contact resistance measurement problems. Figure 3.7 demonstrates the four-terminal Kelvin sense bond pad configuration used on the Au metal 1 electromigration test structure.

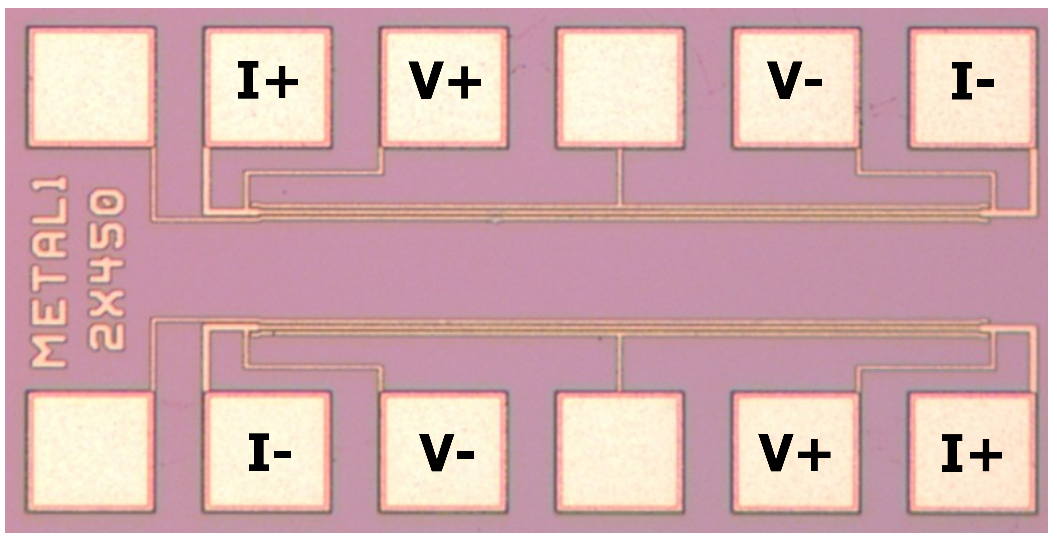


Figure 3.7 Kelvin sensed test structure layout configuration.

3.2 Gold Interconnect Fabrication

Modern gallium arsenide heterojunction bipolar transistors (HBT) technologies are integrated with up to three levels of metal interconnects. The HBT interconnect metallization studied in this investigation consisted of two-levels of metallization on gallium arsenide (GaAs) substrates. All interconnect test structures furnished were processed by Motorola's compound semiconductor manufacturing facility. Several photo mask sets were prepared to fabricate the test structure design and layout as discussed in the previous section. Materials and processing steps for the GaAs HBT differ from both Al(Cu) and Cu metallization technologies. Proprietary device features and process information for the HBT technology is not covered. However, this section does provide a detailed description of the back end of line (BEOL) process layers involved in fabrication of the gold interconnects.

The substrate material used was a GaAs (6-inch diameter) wafer with a thickness of 650 μm. GaAs wafers are much more brittle than silicon wafers so careful handling was necessary during manufacturing. The first step (1) of the BEOL process is the plasma enhanced chemical vapor deposition (PECVD) of the SiN film. This SiN layer is approximately 1,000 angstroms (Å) thick and is the inter-layer dielectric (ILD0) on top of the GaAs substrate. The PECVD SiN film is the most common dielectric material used for GaAs processing since it offers a better diffusion barrier for ions than SiO_2 and has excellent moisture barrier characteristics. The main purposes of SiN films are to serve as an insulating layer and planarize the surface for subsequent interconnect metallization layers. Step (2) is the physical vapor deposition (PVD) of 1,000 Å of TiW followed by 300 Å of Au seed. The TiW film acts as a diffusion barrier and adhesion layer for the

Au metallization. The thin 300 Å Au film functions as a conductive seed layer for the subsequent patterned electroplated thick Au interconnect film. Photo-resist is coated, masked, UV exposed, and then the exposed region is developed in step (3) of the BEOL process. Low power oxygen (O_2) plasma ash is used to remove potential resist "scum" in the areas to be plated. A 1 μm thick Au film is electrodeposited in step (4) using a non-cyanide gold bath solution in a Semitool Equinox plating tool. Figure 3.8 is a photograph of the Semitool Equinox plating tool utilized in the plating of the Au interconnects.

Figure 3.8 Semitool Equinox gold plating tool.

Step (5) strips the photo-resist and employs reverse plating to remove the Au seed layer in the field areas. In the last step (6), the TiW layer removal in the field area is achieved by a spray acid tool using a 30% H_2O_2 wet etchant solution. At this processing stage the Au interconnect test structure line feature is formed. Subsequently, the Au interconnect (metal 1) test structure is encapsulated by a second 1 kÅ SiN (ILD1) film and a final thick passivation layer of 8 kÅ of SiN.

Figure 3.9 depicts these individual processing steps in the formation of the patterned electroplated Au interconnect test structures.

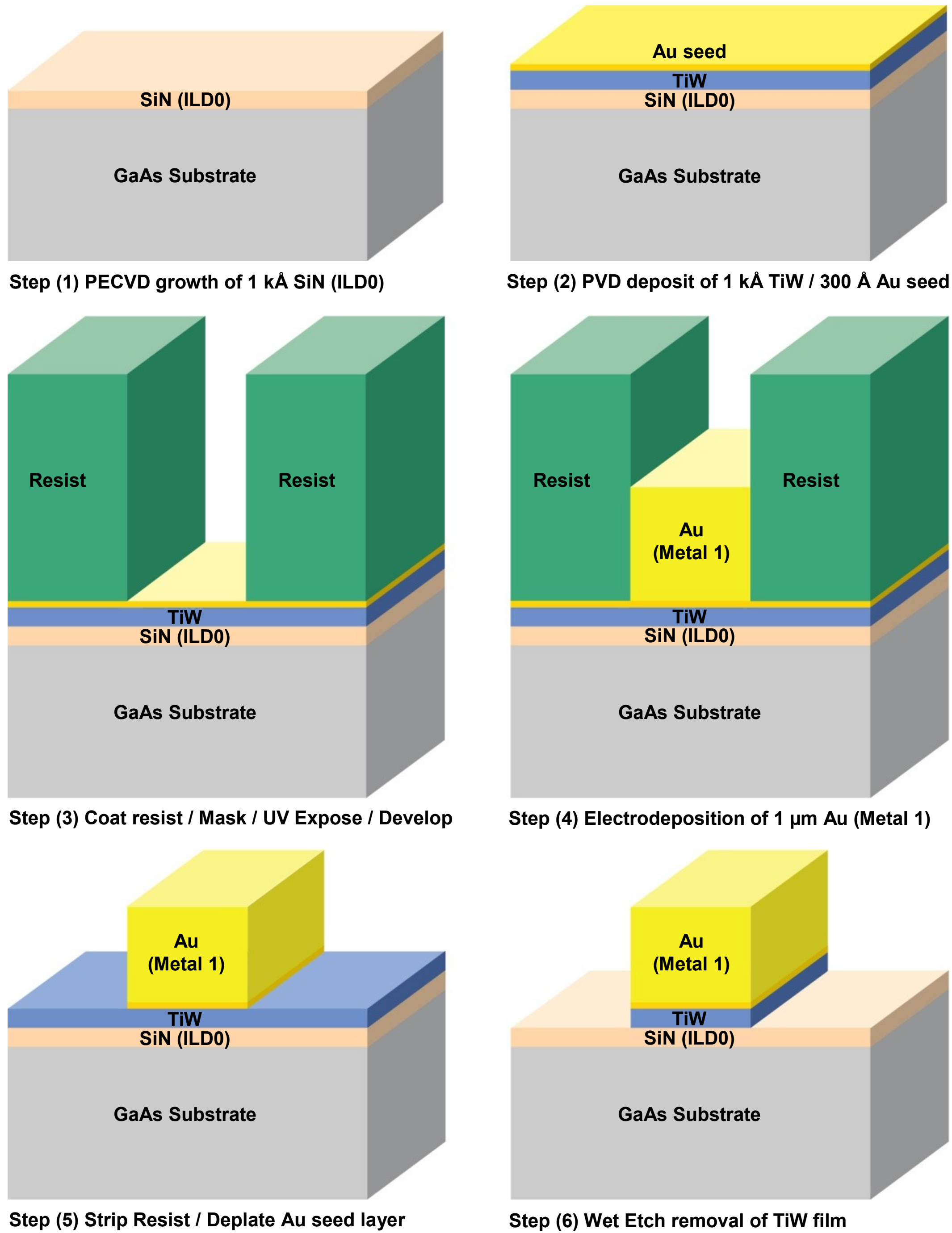


Figure 3.9 Processing steps for the Au interconnect test structure formation.

3.3 Assembly and Packaging

All electromigration testing of Au interconnect test structures in this investigation were conducted by the conventional package-level method. Package-level method has several advantages over the highly accelerated wafer-level test method. A key benefit of package-level method is the testing and stressing of a relatively large number of test structures at the same time. Through simultaneous testing of interconnect lines reasonable stress level conditions are permitted for accelerating the electromigration failure mechanism. Stress level conditions with this approach are optimized to minimize Joule heating and avoid thermal runaway of the interconnect line while targeting practical experimental test times. Current and temperature stress values are typically constant and accounted as independent of each other provided Joule heating is not a significant factor. Another important benefit of the package-level method compared to wafer-level tests is that electromigration model parameter extraction and the extrapolated lifetime predictions are feasible and accurate. Accurate results are attained by maintaining control and monitoring of the current, resistance, and temperature of the test structure during the entire electromigration test. The main disadvantages of package-level method testing include capital expenditure of the specialized electromigration test equipment, the cost of packaging, and extended test times that vary from hours to months.

In the assembly process for the package-level test method, GaAs wafers were thinned to 100 µm (4 mils) thick using backgrind processing to reduce die height for subsequent microelectronic packaged applications. For this backgrind operation, wafers are mounted on sapphire substrates because thinned GaAs wafers are extremely difficult to handle. Backside metallization is then deposited

on the thinned GaAs wafers. A backmetal of 1 kÅ titanium (Ti) and 8 kÅ Au multi-layer film is deposited by PVD. Subsequently, the GaAs wafers were mounted on UV tape and sawn using a diamond saw blade to singulate the die containing the Au interconnect test structures. Figure 3.10 shows an image of a GaAs (6-inch) wafer mounted on UV tape after singulation of the Au interconnect test structures by the saw operation. The UV tape mounted to the GaAs wafer receives UV irradiation to reduce tape adhesion, thus allowing the individual die to be picked. Next, the backside of the individual GaAs die is pushed up by a needle so that the die can be picked and placed into wafer compacts for temporary storage before packaging.

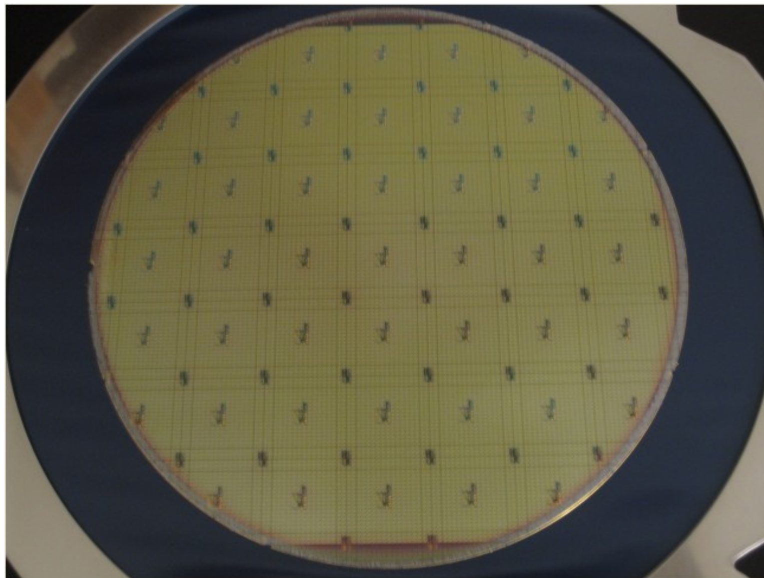


Figure 3.10 Sawn GaAs wafer mounted on UV tape.

GaAs die were packaged in ceramic side-brazed 20-pin dual in-line packages (DIPs) for all electromigration tests in this study. These packages consist of two parallel rows of 10 pins with each pin (lead) corresponding to a lead frame bond pad that surrounds the package cavity. The package has a

notch on one end in order to provide a reference for the top orientation of the package and to aid lead number identification. Leads are numbered consecutively counter-clockwise from pin 1 starting at the top of the package just left of the notch as demonstrated in Figure 3.12. The standard inter-lead spaces (lead pitch) are 0.1 inch (2.54 mm) to guarantee that the packages fit into standardized socket boards. Ceramic DIPs can withstand much higher temperatures (> 300°C) than plastic DIPs and were necessary for these high temperature electromigration tests. Ceramic side-brazed 20-pin DIPs are relatively expensive costing above $3 per package. Several thousand ceramic side-brazed 20-pin DIPs were utilized during this research study. Figure 3.11 provides an image of a ceramic side-brazed 20-pin DIP containing a GaAs die with the Au interconnect test structure.

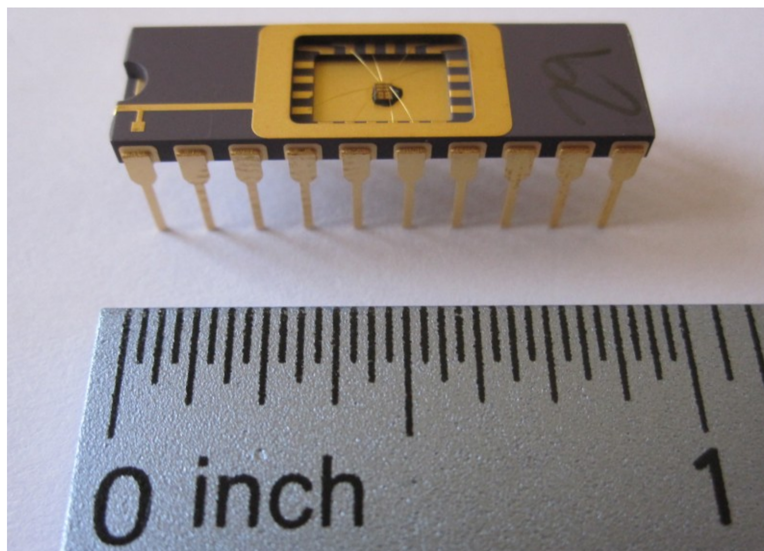


Figure 3.11 Ceramic side-brazed 20-pin dual in-line package.

Openings (cavities) of these packages are 0.26 inches by 0.175 inches with a gold plated surface. Individual GaAs die were bonded to the package

cavity bottom using a silver-glass diebond material that was applied and then reflowed at 390°C for 20 minutes. The silver-glass diebond paste provided excellent thermal dissipation to reduce die temperature and ensured that die adhesion to the package was maintained during the high temperature testing. Next, one mil (25.4 μm) Au wires were ball bonded onto Au bond pads to connect the Au interconnect test structures to the package leads. Au wire was utilized to eliminate any potential of intermetallic formation on the Au bond pads during high temperature testing. Figure 3.12 illustrates the Au wirebond configuration between the Au interconnect test structure and the package bond pad leads. Wirebonded packages were loaded into oven socket boards which subsequently were positioned into the electromigration ovens.

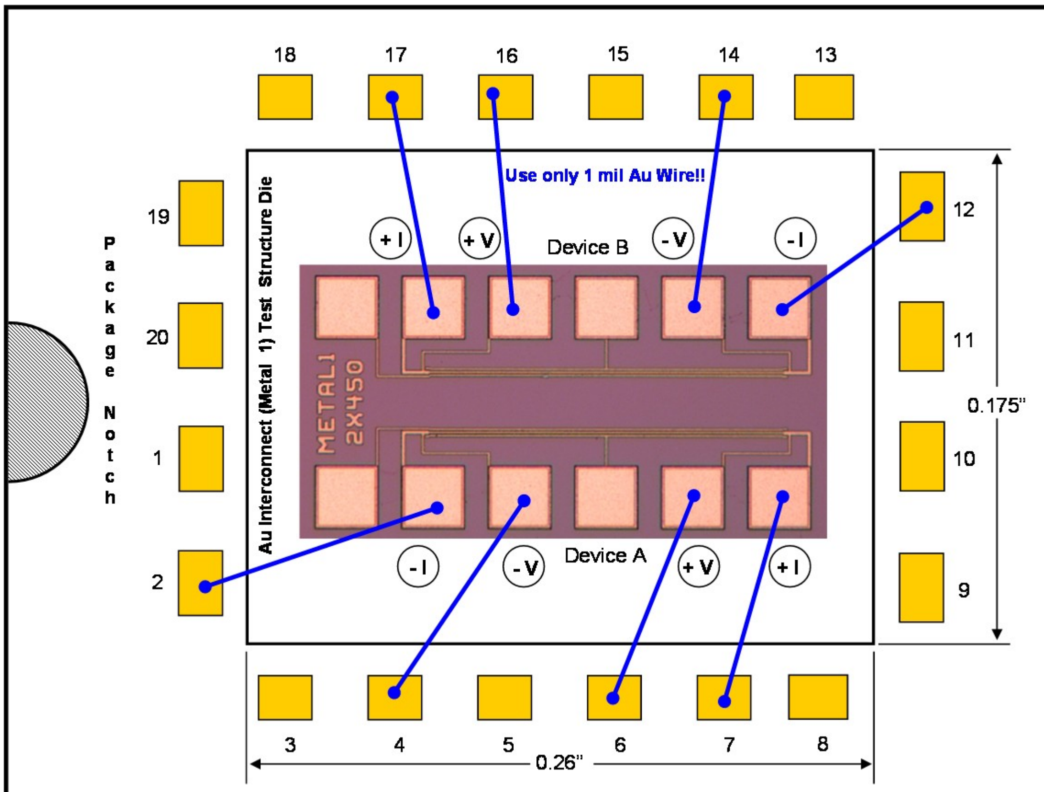


Figure 3.12 Au wirebond configuration diagram.

3.4 Electromigration Test System

QualiTau modular integrated reliability analyzer (MIRA) test systems were utilized for all electromigration tests. The QualiTau MIRA electromigration test systems are composed of up to 4 modules per equipment rack. These test systems are configured with multiple oven chambers for parallel tests at different temperatures. Large ovens are connected to 2 MIRA modules that accommodate 10 oven socket boards with a DUT capacity of 120 test structures. Mini-ovens are connected to only 1 MIRA module allowing up to 5 oven socket boards with a DUT capacity of 60 test structures. Large ovens were designed to test up to 350°C and mini-ovens have a maximum temperature of 450°C. These mini-ovens were essential because higher temperature tests are required to induce electromigration failures in Au films. Due to much less volume and better air flow design, mini-ovens have a tighter temperature uniformity advantage. Figure 3.13 displays a photograph of the QualiTau MIRA reliability test systems utilized for this Au electromigration investigation.

Figure 3.13 QualiTau MIRA electromigration test systems.

The large oven MIRA modules source a maximum stress current of 80 milliamps (mA). Higher current source MIRA modules with a maximum stress current of 500 mA were operated with the two mini-ovens with one oven door open as shown in Figure 3.13. The 80 mA MIRA module has a current resolution of 0.13 mA while the 500 mA MIRA module has a current resolution of 0.12 mA for the stress currents applied. MIRA modules provide a true current source dedicated for each DUT.

Two types of oven socket boards were necessary for this work. The standard oven socket boards are made of steel with an insulating coating designed for maximum testing capability up to 350°C. A higher temperature oven socket board with ceramic zero insertion force (ZIF) sockets were designed for testing up to 400°C. Figure 3.14 presents a photograph of both of these oven socket boards.

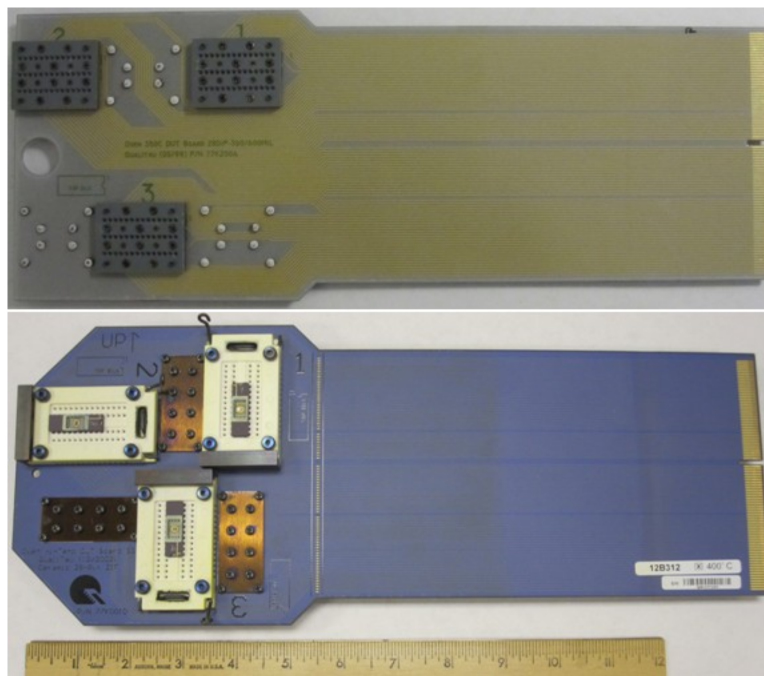


Figure 3.14 Oven socket boards (350°C board above / 400°C board below).

Oven socket boards function as an electrical connection between the packaged Au test structures and the electronics of the QualiTau MIRA test system. Each oven socket board holds up to 6 packages and 12 DUTs with double density packaging that permits two Au test structures per package. Oven socket boards are easily loaded through gasketed slots on the inside oven door allowing connection to the backplane. Figure 3.15 shows an image of the socket boards loaded into the oven door backplane.

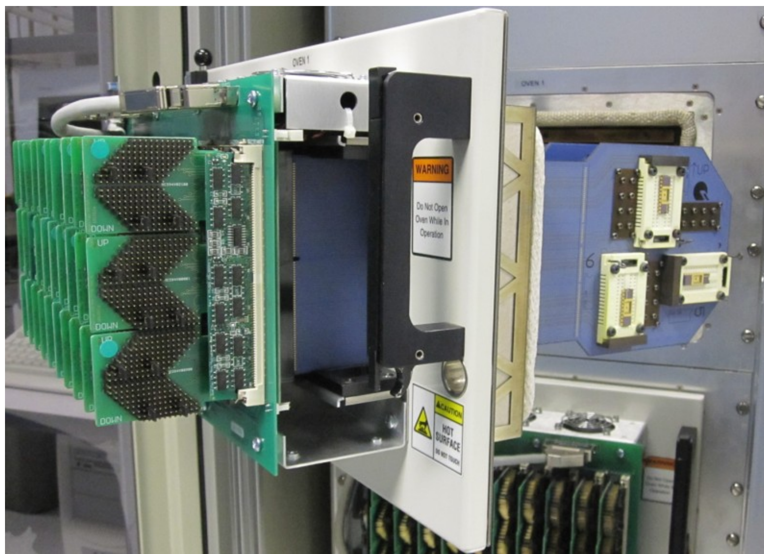


Figure 3.15 Oven socket boards loaded into oven backplane.

The oven door backplane serves multiple purposes. It provides a means of connecting the current sources to the packaged Au test structures, measures the DUTs continuously with a multiplexing measurement system, and patented jumper cards inserted into the backplane enable the user to select pin functions on the package. Oven temperature is controlled by a proportional integral derivative (PID) controller that optimally adjusts the amount of heating power the oven receives to maintain the set-point temperature.

Experimental measurements were made with a high precision HP 34970A data acquisition meter located on the bottom of the equipment rack. The QualiTau test system utilizes two computers so that test program set-up and data review tasks are separated from the tasks of experimental control and data acquisition. This two-computer arrangement is advantageous since the MIRA mainframe computer will not be inadvertently interrupted by data analysis and review on the workstation computer. Proprietary software facilitates automatic control and monitors experimental stress conditions, data acquisition frequency, and the resistance failure criterion threshold on all DUTs resides on the MIRA mainframe computer. Figure 3.16 represents a block diagram of the QualiTau test system architecture, control and measurement paths.

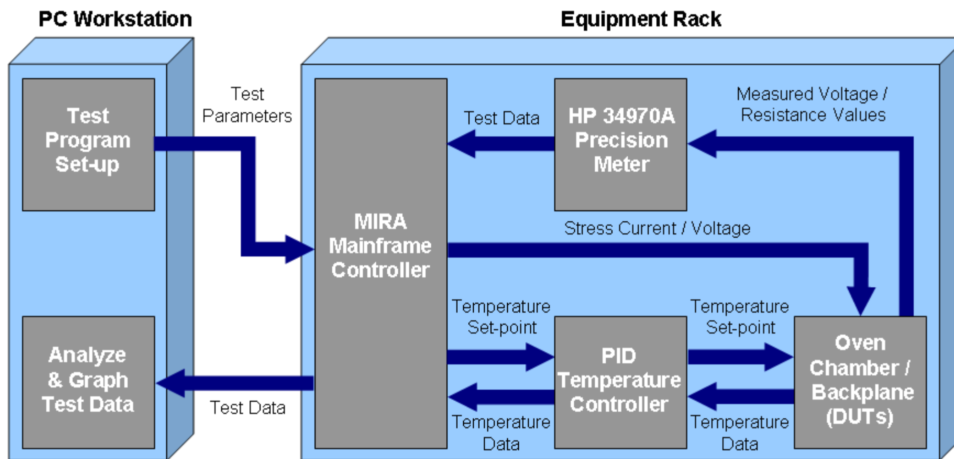


Figure 3.16 QualiTau test system architecture block diagram.

Since electromigration experiments required several weeks or months it was crucial that no power loss was experienced. A large capacity battery uninterruptable power supply (UPS) unit was stationed between the incoming facility power source and the QualiTau test system ensuring no power disruptions.

3.5 Test Procedures and Methods

All packaged Au interconnect test structures had a four-terminal Kelvin resistance measurement initially taken with a Keithley (Model 197A) 5½ digit multimeter connected to a zero insertion force (ZIF) socket box to ensure Au wire bond continuity prior to testing. These initial room-temperature resistance values were recorded and evaluated for their standard deviation providing insight on the Au test structure uniformity and process control. Packaged Au test structures were numbered and loaded into the oven socket boards. The exposed contact leads on the end of the oven socket boards were then carefully inserted into the oven backplane. A new program file was created with the QualiTau electromigration software for every electromigration experiment. These test programs contained all the stress conditions and criteria for the electromigration experiments. Also, the package type and wirebond lead configuration for current and voltage sourcing were entered. Assignment of the jumper card pins for the given packaged test structure wirebond lead configuration is provided in the test program. Before closing an oven door with the loaded boards and inserted DUTs, a quick check software function allowed a lower current to be applied in order to verify electrical continuity of all the DUTs so that packages, boards, and jumper cards could be reseated if necessary.

Since electromigration lifetimes are exponentially dependent on the reciprocal of the metallization temperature it was critical to characterize the Joule-heated metal film temperature caused by higher stress currents. High current densities can generate significant temperature gradients across the metal test line depending on structure design and the thermal conductivity and thickness of the surrounding dielectric layers. Design features recommended by

NIST[125] to minimize Joule heating effects and severe temperature gradients were implemented on the Au interconnect test structures. In addition, a distinctive feature of this Au electromigration investigation was the thick overlayer of SiN passivation that encapsulated all Au interconnect test structures providing improved thermal dissipation.

Given that the electrical resistivity in metal films is caused by electron scattering phenomena, it is expected that metal line resistance increases with rising temperature due to more electron collisions. A metal test structure line resistance has a linear relationship with temperature over an extended range of temperatures. The resistance (R) of a metal test structure as a function of temperature (T), is expressed in Equation (3.1)

$$R = R_0\left[1+\alpha_0\left(T-T_0\right)\right], \tag{3.1}$$

where (R_0) is metal test structure resistance at a reference temperature (T_0) usually specified as 20°C. The temperature coefficient of resistance (TCR) for a metal line is symbolized by alpha (α_0) and is defined as the fractional change in resistance per unit change in temperature. Equation (3.1) can be rearranged to solve for the TCR (α_0).

$$\alpha_0 = \frac{1}{R_0}\frac{\left(R-R_0\right)}{\left(T-T_0\right)} = \frac{1}{R_0}\frac{\Delta R}{\Delta T}. \tag{3.2}$$

Equation (3.2) demonstrates that the TCR value decreases with increasing temperature since the metallization resistance increases with temperature while the slope remains constant. Therefore, the TCR value is not a constant and must always be referenced to a specific temperature. To determine accurate TCR values for metal test structures it is vital that repeatable and consistent resistance measurements are obtainable over the specified temperature range.

Resistance measurements can be affected by changes in the metallization when exposure to high temperature causes annealing of the metal grain microstructure. Another irreversible change to the resistance of a metal test structure is experienced when it is subjected to high current stress for durations long enough to induce electromigration voids. Precautions should be taken to ensure that the metallization resistivity is stable so an accurate TCR value can be obtained for the metal interconnect test structure.

A standard method for determining the TCR is described by Schafft.[126] The resistance of the test structure line is measured at four or more ambient oven temperatures that are uniformly distributed over a selected range. The TCR current applied in measuring the resistance must be low enough not to induce any Joule heating in the metal test structure line. A graph of the measured resistance versus temperature is generated and an unweighted least squares fitting method is used to obtain a straight-line fit of the data. The slope of the fitted straight line is now determined along with the measured reference resistance (R_0). Finally, the TCR (α_0) value is calculated at a reference temperature (T_0) with the following expression

$$\alpha_0 = \frac{1}{R_0}\frac{\Delta R}{\Delta T} = \frac{1}{R_0}(\text{Slope}). \tag{3.3}$$

TCR values are frequently reported for a standard reference temperature usually specified as 20°C, which is approximately room temperature. However, TCR values can be calculated using Equation (3.3) for other temperatures by knowing the resistance at that temperature and the line slope of the fitted data. Figure 3.17 demonstrates a graphical representation of the standard method for determining the TCR of a metal test structure line.

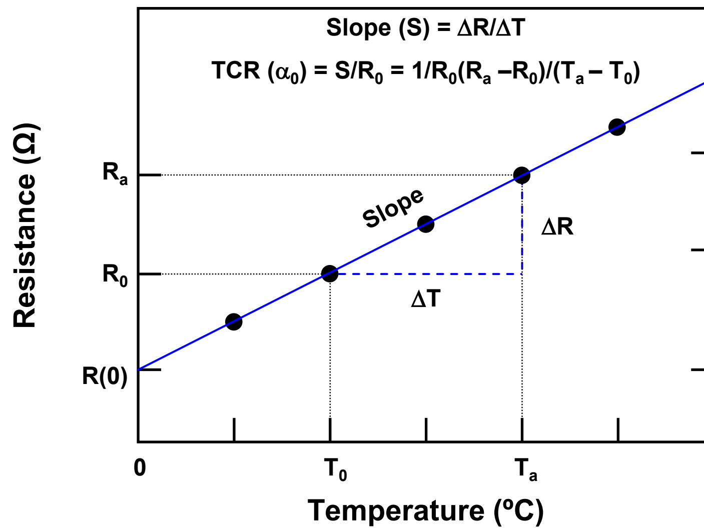


Figure 3.17 Standard method for TCR determination.

Once an accurate TCR value has been calculated for the metallization, its practical application can be exploited. Electromigration reliability tests are accelerated by high currents that under certain circumstances induce significant Joule heating in metal interconnect test structures. In cases where Joule heating is significant, it is imperative that the metal test structure temperature is accurately determined.

Joule-heated film temperatures of metal interconnect test structures are determined through the following standard method. The previously acquired TCR (α_0) at the reference temperature (T_0) along with measured reference resistance (R_0) will be utilized in the film temperature calculation. At the selected stress ambient oven temperature (T_a) of the electromigration test, which is the last TCR temperature, the desired higher stress current is applied to the metal interconnect test structure. After only a few minutes elapse to allow the Joule-heated temperature to reach equilibrium, the resistance (R_s) of the metal

interconnect test structure is measured. Rearranging equation (3.1) to solve for the Joule-heated temperature (T_s) with the predefined subscript notation, the following expression in Equation (3.4) is derived.

$$T_s = T_0 + \frac{(R_s - R_0)}{(R_0)(\alpha_0)} \quad (3.4)$$

Figure 3.18 demonstrates the graphical representation of the low current standard method for Joule-heated temperature determination.

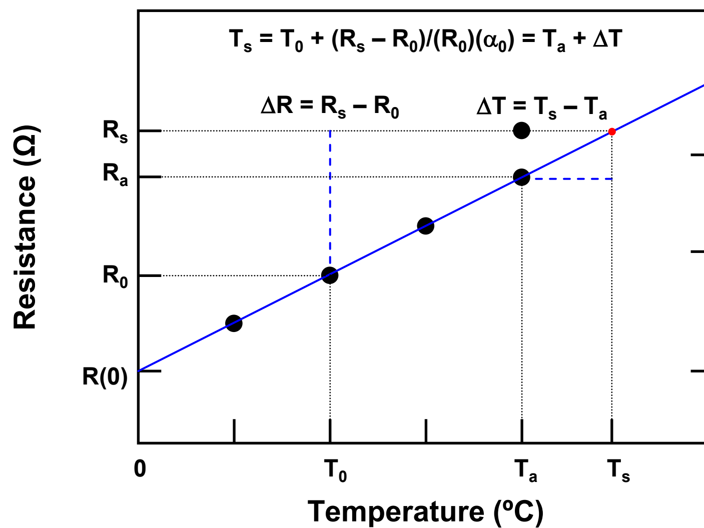


Figure 3.18 Standard method for Joule-heated temperature determination.

In this investigation, the Au interconnect test structures were annealed during the process formation steps producing a stable metallization resistivity. All TCR measurements were made prior to the extended elevated stress current stage of the electromigration experiment to avoid resistance change due to electromigration-induced voids. A two-current measurement technique is automated within the proprietary software of the QualiTau test system. This technique involves measuring the resistance of the Au test structure while

applying a low current as in the standard method as well as an additional higher stress current. Resistance measurements are taken as the oven ramps to multiple preselected oven temperatures evenly distributed up to the actual stress temperature of the electromigration test. A least squares fitting method on both the low and high current resistance data generates linear curves. Figure 3.19 depicts a graph of the two-current method for determining the Joule-heated film temperature. Advantages of the two-current method are that potential Joule heating at low currents is not neglected and that the measurement resolution problem at very low current is avoided.

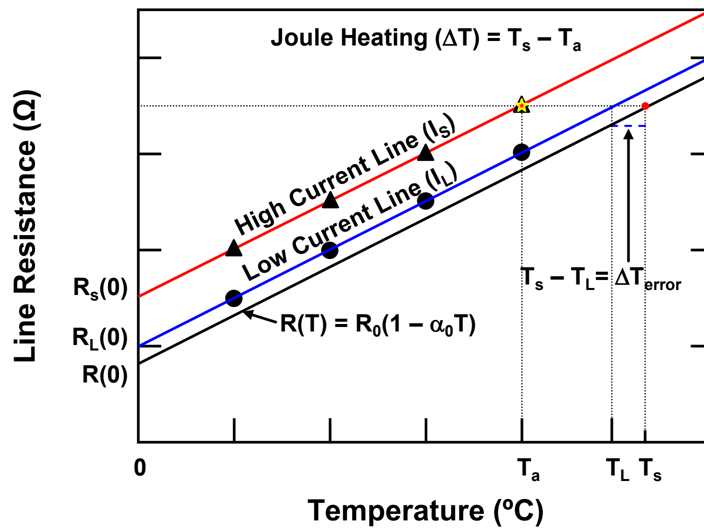


Figure 3.19 Two-current method for Joule-heated temperature determination.

The TCR measurements in this study were at four to five uniformly distributed oven temperatures to supply sufficient data for accurate linear curve fits. Extracted TCR values obtained for the Au interconnect test structures were compared to standard reference values found in the literature. Current densities for the initial electromigration tests in this investigation were as high as 3 MA/cm^2.

In order to apply these current densities on large cross-sectional area Au interconnect test structures, high currents are needed which induce significant Joule heating. Therefore, Joule-heated film temperatures of the Au interconnect test structures were accounted for and determined using the two-current method previously discussed.

Immediately after TCR measurement and Joule-heated film temperature determination, the constant stress current for the electromigration test was applied. Oven temperature remained constant during the entire electromigration test. Voltage measurements across all Au interconnect test structures were taken over time. Under constant current (I) tests, the resistance (R) for each DUT is directly obtained from the measured voltage (V) calculated by Ohm's law

$$V = I\,R \;\Rightarrow\; R = \frac{V}{I}. \tag{3.5}$$

All electromigration tests utilized the resistometric method wherein the resistance increase of the Au interconnect was measured as a function of time. The principle of this method is that resistance change is very sensitive to microstructural changes occurring in the Au interconnect. A key benefit is that the early stages of electromigration are monitored so that as soon as a small void is formed in the Au interconnect it is detected. Electromigration tests continued until the preselected resistance percent change criterion was reached. Typically, electromigration tests have a specified resistance degradation change failure criterion of 10% $\Delta R/R_0$. Utilization of this method and failure criterion avoids catastrophic open circuit failures that are emblematic of electromigration lifetime tests where current density and Joule heating excessively increase.

3.6 Test Structure Cross-Sectional Measurements

In order to ensure appropriate current density stress levels were applied on the Au test structures, cross-sectional measurements were taken with the focus ion beam (FIB) instrument. Several different wafers were sampled for the line-width and thickness cross-sectional measurements to obtain an average that incorporates process variability. A FIB cross-section displaying line-width and thickness measurements of the Au M1 test structure in experimental phase V is displayed in Figure 3.20. An average line-width of 1.95 μm and a thickness of 1.02 μm were calculated for all Au M1 test structures measured. Based on these average Au M1 test structure dimensions an exact stress current of 39.84 mA was applied to achieve a current density of 2.0 MA/cm^2.

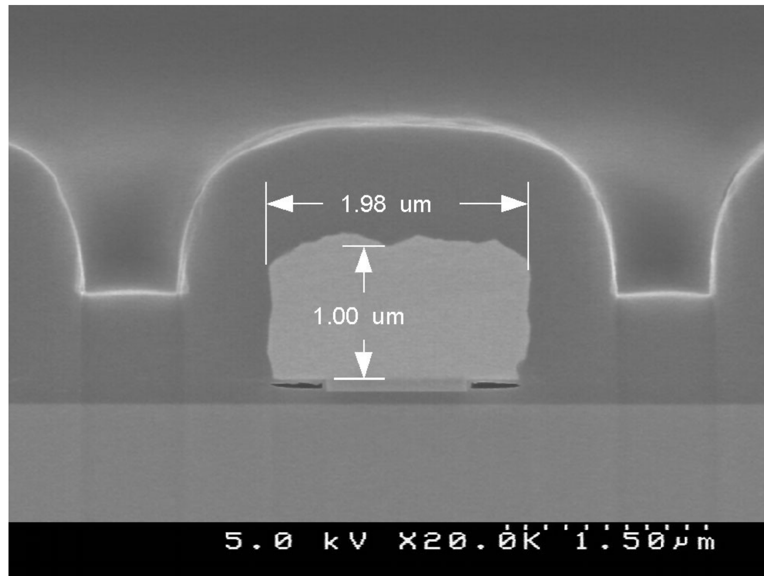


Figure 3.20 Au M1 test structure line-width and thickness measurements.

Cross-sections using the FIB were also obtained for the Au V1M1 test structures. Line-width and thickness measurements were taken approximately in the middle of the stress line. The cross-section of the Au V1M1 test structure in experimental phase V is shown in Figure 3.21. An average line-width of 4.99 μm and a thickness of 1.13 μm were calculated for all Au V1M1 test structure cross-sectional measurements. The line-width was very close to the process target of 5 μm, but the Au film thickness was thicker than its process target of 1 μm. A slightly lower current density of 1.4 MA/cm^2 was chosen for the Au V1M1 test structure in experimental phase V, because the thicker Au film would have exceeded the maximum current of 80 mA on the large oven mainframe controllers in order to target a 1.5 MA/cm^2 current density.

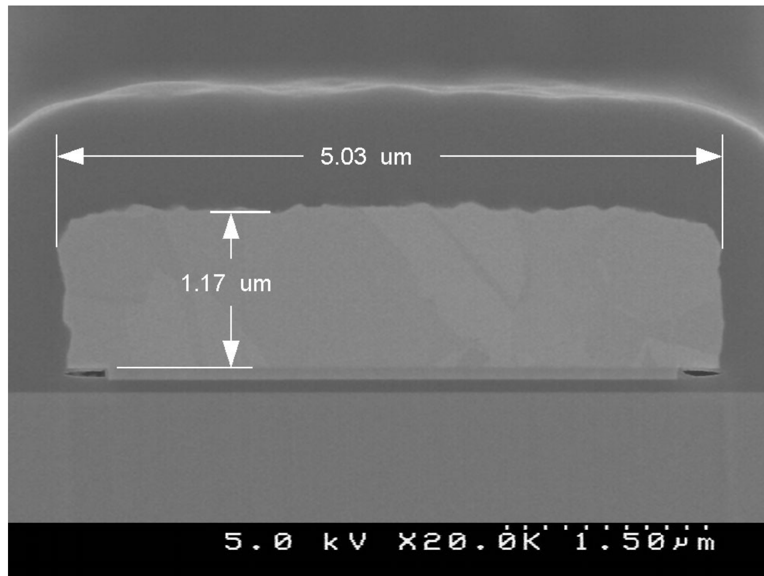


Figure 3.21 Au V1M1 test structure line-width and thickness measurements.

3.7 Experimental Test Conditions

Over the five phases (I – V) of this investigation, test structure design, sample size, and test stress conditions evolved and were optimized to obtain accurate and comprehensive Au electromigration results. The initial experimental phase I applied a considerably high current density of 3 MA/cm^2 on a very limited sample size of 20 Au interconnect (metal 1) test structures. Also, via centered test structures were stressed with a current density of 1.5 MA/cm^2. Oven stress temperatures were 300°C, 325°C and 350°C. The electromigration failure criterion was selected as a 10% resistance change. In experimental phase II, it was deemed necessary to institute dual Au interconnect test structures to double the sample size to 60 in order to increase statistical confidence with the same electromigration stress conditions.

Subsequently, in an effort to decrease the initial test structure resistance variation due to process variability, a redesigned shorter four-terminal Au interconnect test structure was developed in phase III. In order to shorten electromigration test times exceeding 4000 hours at the lowest temperature, oven stress temperatures were incrementally increased to 325°C, 350° and 375°C. In phase III, current density was lowered to 2 MA/cm^2 on the Au interconnect (metal 1) test structures to reduce Joule heating. A key adjustment in phase III was that the electromigration failure criterion was increased to a 50% resistance change to allow for healing recovery of resistance spikes caused by coalescence of pre-existing voids. This criterion still avoids thermal runaway that occurs with open circuit failures. In addition, this higher resistance change criterion facilitated easier optical detection of voids, because electromigration voids grew slightly larger than with a resistance change failure criterion of 10%.

In experimental phase IV, the same three temperatures of 325°C, 350°C, and 375°C were examined for Au electromigration. However, the current density was lowered to 1.5 MA/cm^2 to further minimize Joule heating and thereby more closely approach the oven stress temperature to ensure accuracy of the extraction of the Au film stress temperature.

In the final phase V of this research, both the activation energy and current density exponent parameters for Au electromigration were determined. A fourth intermediate oven stress temperature of 360°C was added to improve statistical confidence in the activation energy extraction accuracy for only the Au M1 test structure. However, the 325°C oven stress temperature was eliminated due to the repeated bi-modal failure distribution observed. The current density was optimized at 2.0 MA/cm^2 to expedite test duration times while not generating significantly more Joule heating on the Au interconnect M1 test structures. The current density for the Au via 1 / metal 1 (V1M1) interface test structures was adjusted lower to 1.4 MA/cm^2 due to the slightly increased Au film thickness of 1.13 μm.

In determining a current density exponent parameter for Black's model, electromigration tests were conducted at a constant oven temperature, while varying the current density (J_{stress}) stress. Current densities of 1.25, 1.5, 1.75, and 2.0 MA/cm^2 were applied on the Au M1 test structures. Due to higher Joule heating at these higher current densities, film temperatures must be normalized for accurate current density exponent extraction. The 50% $\Delta R/R_o$ failure criterion was considered optimal because resistance spikes observed on a few Au interconnect structures are permitted to recover, and thus have prolonged lifetimes before the critical void size is reached.

Table 3.1 displays all the experimental stress test conditions, sample size, and failure criterion for the Au M1 test structure in phase V. Table 3.2 lists all the experimental stress test conditions, sample size, and failure criterion for the Au Via 1 / Metal 1 (V1M1) test structure in phase V. All Au interconnect test structure dimensions and stress current values listed in Tables 3.1 and 3.2 were rounded for illustrative simplification.

Table 3.1 Experimental stress conditions for Au M1 test structures (phase V).

Test Structure	Line Width (μm)	Line Thickness (μm)	Line Length (μm)	Oven Temperature (°C)	J_{stress} (MA/cm^2)	I (mA)	Sample Size	Failure Criterion (% $\Delta R/R_o$)
M1	2	1	450	375	2.0	40	60	50% $\Delta R/R_o$
M1	2	1	450	360	2.0	40	60	50% $\Delta R/R_o$
M1	2	1	450	350	2.0	40	60	50% $\Delta R/R_o$
M1	2	1	450	300	2.0	40	60	50% $\Delta R/R_o$
M1	2	1	450	375	1.75	35	60	50% $\Delta R/R_o$
M1	2	1	450	375	1.50	30	60	50% $\Delta R/R_o$
M1	2	1	450	375	1.25	25	60	50% $\Delta R/R_o$

Table 3.2 Experimental stress conditions for Au V1M1 test structures (phase V).

Test Structure	Line Width (μm)	Line Thickness (μm)	Line Length (μm)	Oven Temperature (°C)	J_{stress} (MA/cm^2)	I (mA)	Sample Size	Failure Criterion (% $\Delta R/R_o$)
V1M1	5	1.1	450	375	1.4	79	60	50% $\Delta R/R_o$
V1M1	5	1.1	450	350	1.4	79	60	50% $\Delta R/R_o$
V1M1	5	1.1	450	300	1.4	79	60	50% $\Delta R/R_o$

3.8 Statistical Methods and Data Analysis

Electromigration lifetime failure data sets have been traditionally fitted using a log-normal distribution. The rationale for the log-normal distribution has been that a nearly straight line fit is consistently obtained when the logarithms of the electromigration failure times are graphed on a cumulative failure probability plot.[127] Identification of specific fundamental mechanisms behind the log-normal appearance of electromigration failure times is yet to be entirely comprehended.[66] However, one plausible suggestion is that the log-normal statistics of electromigration failure times are a consequence of microstructural thin film factors. A strong argument for the log-normal behavior of electromigration failures is that the diffusion pathways are influenced by the microstructural grain size distribution which is also observed to follow log-normal statistics.[128] Regardless of the exact fundamental mechanism for the correlation, the log-normal distribution function has been repetitively demonstrated and proven to provide the best overall fit for electromigration failure time data. Therefore, all the Au electromigration data in this research study were analyzed with log-normal statistics.

The probability density function (PDF) for the log-normal distribution is defined by

$$\mathrm{PDF}(t) = \frac{1}{\sigma t\sqrt{2\pi}}\exp\left[-\frac{1}{2}\left(\frac{\ln(t)-\ln(t_{50\%})}{\sigma}\right)^2\right], \tag{3.6}$$

where (t) is the time, (σ) is the standard deviation in logarithmic time, and ($t_{50\%}$) is the median time to failure. The σ factor is also considered the shape parameter and defines the shape of the log-normal distribution. The cumulative distribution function (CDF) describes the accumulated percentage of failed interconnects

from time 0 until time t. The CDF is obtained by taking the integral of the PDF from time 0 to t and is expressed using a Gaussian integral as

$$\mathrm{CDF}(t) = \int_0^t \mathrm{PDF}(t)\,dt = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{Z(t)} \exp\left(\frac{-z^2}{2}\right) dz, \tag{3.7}$$

where $Z(t) = \ln(t) - \ln(t_{50\%})/\sigma$ and $t > 0$. A convenient alternative expression is in terms of the standard normal CDF (Φ) as follows

$$\mathrm{CDF}(t) = \Phi\left[\frac{\ln(t/t_{50\%})}{\sigma}\right]. \tag{3.8}$$

Values obtained from the standard normal CDF table are selected to evaluate failure probabilities for the log-normal distribution.[129] Fortunately, powerful statistical computer software programs such as Minitab automate CDF graphing and therefore Minitab was utilized in the analysis of electromigration failure time data for Au interconnects. Electromigration failure times are customarily displayed in a log-normal CDF graph with percentages on the y axis and time on the x axis. The CDF graph provides an intuitive examination of the shape parameter (σ) of the distribution as well as the log-normal fit to the failure data.

Semiconductor manufacturing companies routinely acquire experimental electromigration data on thin film metallizations for the primary purpose of determining the interconnect lifetimes under operating conditions. Operational lifetimes are determined by extrapolating the electromigration failure data using a ratio of Black's equation from accelerated stress conditions to normal operating conditions. Operational lifetimes extrapolated from stress conditions depend linearly on the measured median time to failure ($t_{50\%}$), and exponentially on the electromigration activation energy (E_a) and the log-normal standard deviation (σ).

Improving electromigration lifetimes for interconnects relies on increasing the activation energy and decreasing the log-normal standard deviation. The log-normal standard deviation (σ) can be a more significant parameter in the electromigration lifetime extrapolation than the median time to failure ($t_{50\%}$). Figure 3.22 shows two example electromigration failure distributions on a cumulative probability graph with different log-normal standard deviation (σ) and median time to failure ($t_{50\%}$) values. It can be clearly seen in Figure 3.22 that when extrapolating to the time below 0.1% cumulative failures, the failure distribution with the lower sigma value produces a longer lifetime despite having a lower median to time to failure. Therefore, manufacturing metallizations possessing electromigration failure lifetime distributions with tight sigma (< 0.3) values are advantageous.

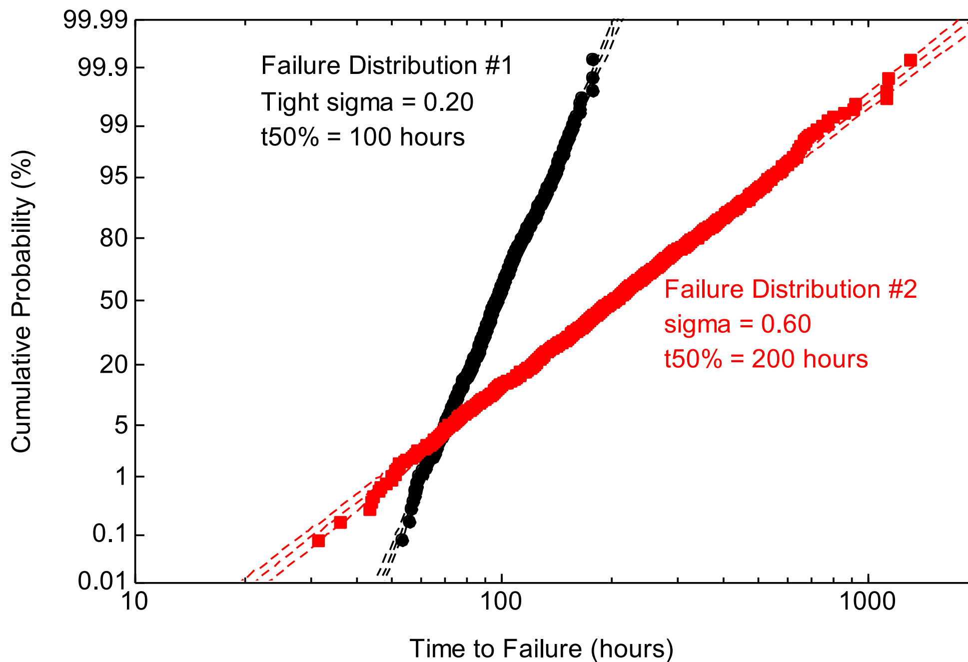


Figure 3.22 Log-normal failure distributions with different sigma and $t_{50\%}$ values.

In some instances experimental electromigration distribution data can exhibit multiple failure modes that are clearly observed when displayed on a cumulative failure probability graph. Extrinsic failure modes that are caused by early failures such as process defects will deviate from the intrinsic electromigration failure mode and should be distinguished from the intrinsic log-normal distribution. The extrinsic (early) failure mode will generally have much shorter median lifetimes and encompass wider (larger sigma values) failure distributions. Figure 3.23 depicts a cumulative probability failure graph with intrinsic and extrinsic failure modes that constitute a bi-modal distribution. It should be recognized that cumulative failure distributions can contain bi-modal or multi-modal failure populations that stem from different intrinsic modes (different diffusion mechanisms) or caused by extrinsic modes (defectivity).

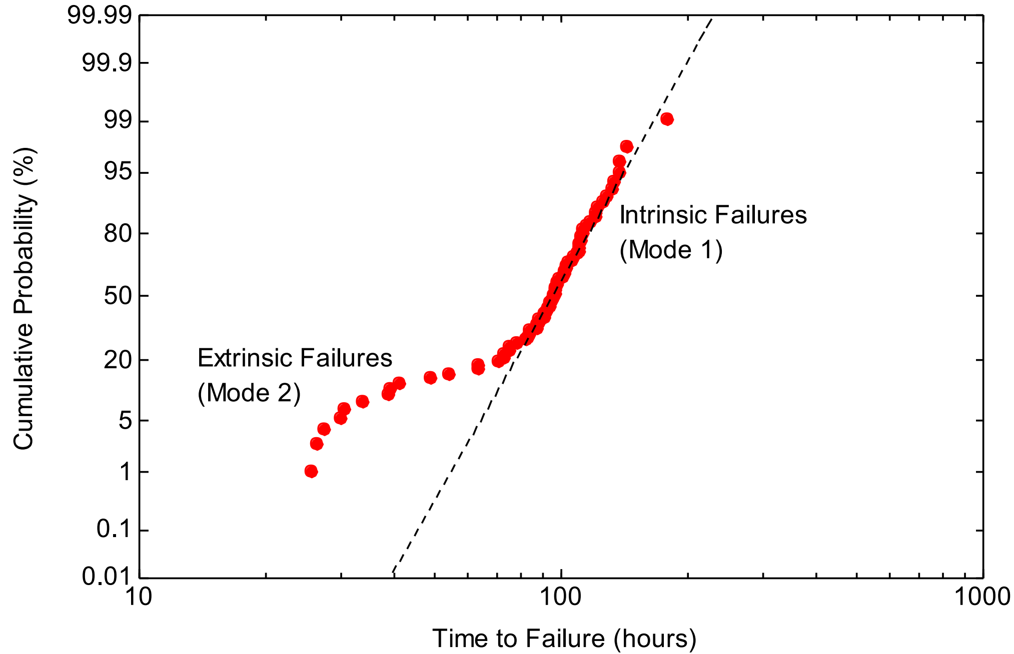


Figure 3.23 Bi-modal failure distribution with intrinsic and extrinsic failure modes.

The Au electromigration lifetimes in this study were extracted from resistance versus time curves and determined by the selected resistance degradation change percentage criteria. These resistance monitored electromigration experiments had the stress current shut off automatically when a particular Au interconnect test structure reached the specified resistance change criterion such as 10% or 50%. Electromigration lifetime data obtained from different stress temperature experiments at the same current density display the acceleration due to temperature, and this permits the activation energy to be determined. The natural logarithmic median time to failure ($t_{50\%}$) data versus the inverse temperature (in Kelvin) is graphed and fitted linearly to extract the activation energy (E_a). An illustrative example of a ln($t_{50\%}$) versus 1/kT data graph for extracting activation energy (E_a) is shown in Figure 3.24. To improve the statistical confidence for extracting accurate activation energy it is imperative to measure at least three or more median electromigration lifetimes at different temperatures.

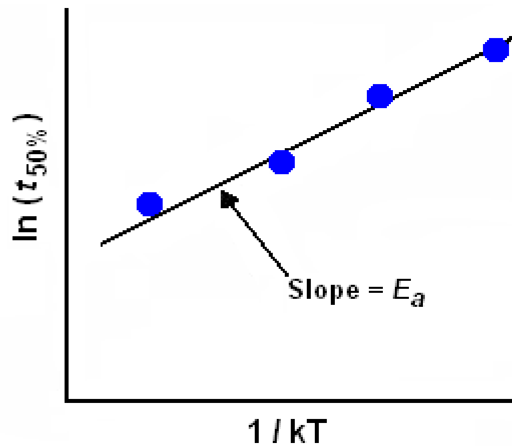


Figure 3.24 ln($t_{50\%}$) versus 1/kT data graph for extracting E_a parameter.

The current density exponent (n) parameter of Black's model is extracted from experiments at different current densities at the same temperature. The current density exponent (n) is extracted by linearly fitting the data plotted in the ln($t_{50\%}$) versus ln(J) graph. An illustrative example of a ln($t_{50\%}$) versus ln(J) data graph is displayed in Figure 3.25. The slope of the fitted line is negative but the current density exponent is taken as a positive value. It is important to note that electromigration experiments with current densities ≥1.0 MA/cm^2 induce Joule heating that cause metal film temperatures to be above the oven temperature. Therefore, it is required to normalize the $t_{50\%}$ data to a constant temperature to obtain an accurate current density exponent.

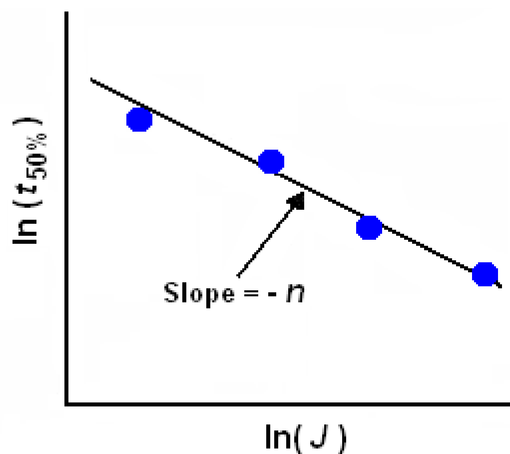


Figure 3.25 ln($t_{50\%}$) versus ln(J) data graph for extracting n parameter.

3.9 Summary of Experimental Methods

In summary of the experimental methods undertaken in this investigation, gold test structure designs were improved over the experimental phases (I – V) along with optimized electromigration stress conditions. The QualiTau MIRA test system permitted package-level double density (60 DUTs) electromigration tests at the high temperatures and stress currents needed to induce electromigration in Au interconnect structures. A high precision data acquisition meter incorporated in the test system enhanced resistance monitoring for the electromigration resistometric technique. The individual TCRs for the Au test structures were determined by low current resistance measurements at four or more temperatures, increasing the accuracy of the determined film temperatures. SEM cross-sectional measurements of the gold test structure dimensions ensured that stress currents were applied to achieve the targeted current densities. Log-normal statistics applied on a very large experimental sample size increased overall confidence in extracting accurate Black's electromigration model parameters.

In this research, a high-resolution in-situ resistometric technique measured the initial stages of the electromigration in passivated electroplated Au films. This technique maintained a constant current and temperature within the Au interconnects, thus avoiding thermal runaway and catastrophic failures inherent with lifetime methods. High-resolution resistance measurements are sensitive in detecting initial electromigration-induced void formations in Au films. In conclusion, meticulous application of the methods and techniques in this research facilitated accurate electromigration lifetime measurements of realistic passivated electroplated Au interconnects on GaAs substrates.

CHAPTER 4 EXPERIMENTAL RESULTS

In this chapter, the electromigration experimental results for the Au interconnect test structures are presented. First, the initial resistance of the Au interconnect test structures are statistically examined. Next, the resistance characteristics during electromigration tests are discussed as well as the electromigration lifetime comparison of the Au interconnect test structures. Imperative to this investigation, the extracted activation energy and current density exponent parameters for electromigration in passivated electroplated Au films are presented. Physical and chemical characterization of the Au thin film microstructure and the electromigration-induced void morphology concludes this chapter.

4.1 Interconnect Resistance Measurements

4.1.1 Metal 1 Test Structure Resistance

The initial resistance of all packaged Au interconnect test structures was measured at room temperature on a Keithley 197A multimeter to verify electrical continuity to ensure integrity of the Au wire bonding process. These initial resistance measurements were also necessary in screening Au interconnect test structures with resistances noticeably outside the standard deviation from the mean. Any packaged Au interconnect test structures that measured as opens (infinite resistance) indicated that either Au wire bonds did not make good electrical connection to the test structure bond pads or Au wires were bonded to incorrect bond pads and thus were excluded from the electromigration tests. Furthermore, packaged Au interconnect test structures with measured

resistances significantly outside the standard deviation of the distribution were screened and replaced with DUTs within one standard deviation from the mean. Screening DUTs was especially necessary for the Au interconnect metal 1 (M1) test structures in experimental phases (I and II). Figure 4.1 displays the initial resistance distribution for the Au M1 test structures in phase II.

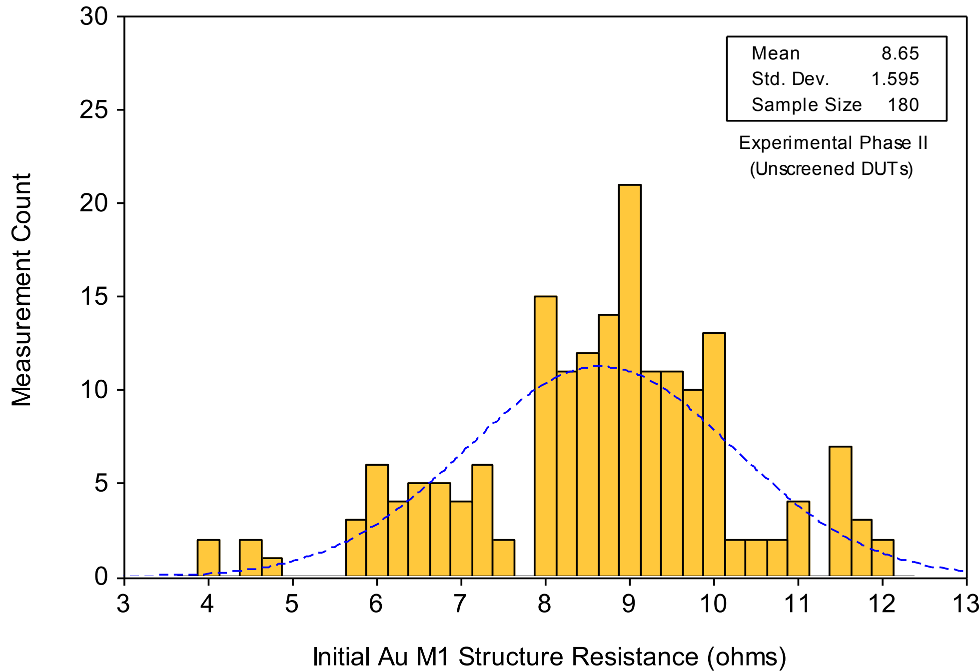


Figure 4.1 Initial Au M1 test structure resistance distribution (phase II).

In experimental phases (I and II), the Au interconnect M1 test structures were 800 μm long with line-width of 2 μm and film thickness of 1 μm. These long electroplated Au interconnects showed a very broad variation in resistance. Standard deviation was 1.6 ohms with an overall resistance range from 4 to 12 ohms. Since the film thickness uniformity is inherently variable with the Au electroplating process, it is unfortunate, but not surprising that these longer Au interconnect test structures exhibited a wide resistance range.

With the same stress current applied to all Au test structures, higher resistance DUTs could potentially exhibit higher Joule-heated film temperatures, causing earlier failures. Conversely, lower resistance Au test structures would be at lower film temperatures promoting longer electromigration lifetimes. Therefore, it was deemed necessary to screen these Au M1 test structures to within approximately ± 1 standard deviation of the mean to avoid test stress condition deviations and potential multi-modal failure mechanisms. Figure 4.2 presents the screened resistance distribution for the Au M1 test structures in phase II.

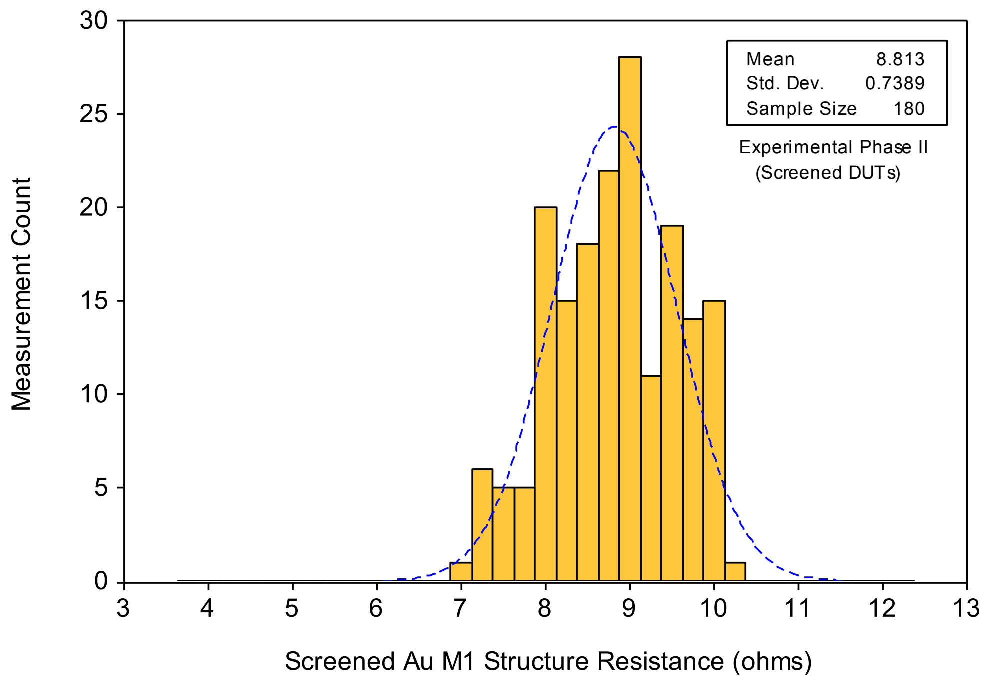


Figure 4.2 Screened Au M1 test structure resistance distribution (phase II).

After screening and exclusion of the initial widely varying resistance DUTs, the resistance distribution of the Au M1 test structures tightened to a standard deviation of 0.74 ohms. The resistance standard deviation decreased by more than a factor of 2 for the Au M1 test structures.

The desire to conduct electromigration experiments on Au interconnect test structures with a lower resistance standard deviation without the need to artificially screen DUTs necessitated the redesign of the Au interconnect test structure in subsequent experimental phases. In experimental phases (III – V), a redesigned Au interconnect test structure was implemented with a shorter length to minimize resistance variation due to plating film thickness uniformity. The length of the redesigned Au interconnect test structures was reduced by almost half to 450 μm long with the same line-width of 2 μm and film thickness of 1 μm. Indeed, these shorter Au interconnect M1 test structures had a tighter resistance distribution spread with a substantially lower standard deviation. Figure 4.3 shows the resistance distribution for the Au M1 test structures in phase V.

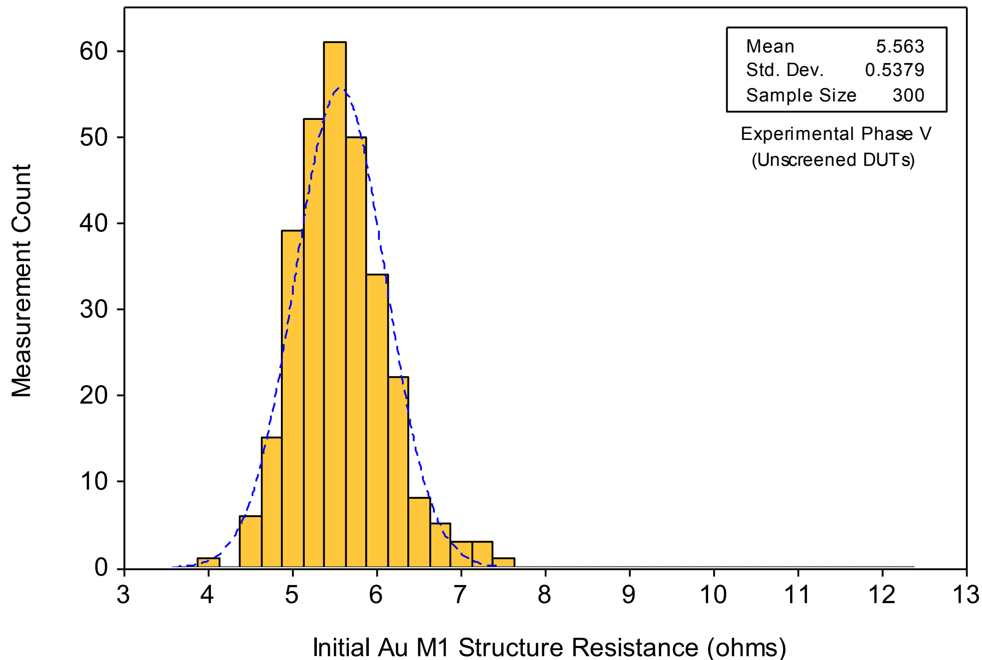


Figure 4.3 Initial Au M1 test structure resistance distribution (phase V).

The redesigned Au interconnect M1 test structures demonstrated a substantial reduction in resistance variability. The standard deviation decreased to 0.54 ohms with an overall resistance range from 4 to 7.4 ohms. Additional reduction in resistance variability is possible with even shorter test structures. However, a shorter test structure would increase the Joule-heated temperature gradient due to a greater percentage of the overall stress line segment that is closer to the much wider and thus cooler current taps.

Resistance measurements of metal interconnect test structures is a practical and rapid parametric test in manufacturing for monitoring process control of the metallization deposition uniformity. In addition, process defects such as non-conducting particles and voids embedded in metal interconnects can be detected. A metal line with a uniform cross-section has a resistance proportional to the resistivity of the metal and the line length but is inversely proportional to the metal line cross-sectional area. Figure 4.4 illustrates the dimensions of a metal interconnect line structure. In reality, plated metal interconnect line structures are not perfectly rectangular in shape and possess more rounded edges due to the etching process. The line-width and thickness of metal interconnect line structures can be determined through FIB cross-sectioning and measuring the dimensions with a calibrated scanning electron microscope (SEM). Section 3.6 provides a comprehensive review of the Au interconnect test structure cross-section measurements.

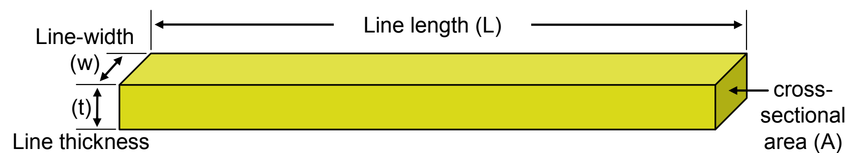


Figure 4.4 Illustration of metal interconnect line structure dimensions.

To confirm that the resistance measurements match the calculated resistances, the average line-width of 1.95 μm and film thickness of 1.02 μm for the Au interconnect M1 test structure was used. A uniform metal interconnect line resistance (R) is calculated by

$$R = \rho\left(\frac{L}{A}\right) = \rho\left[\frac{L}{w \times t}\right], \tag{4.1}$$

where L is the line length in meters (m), A is the cross-sectional area in square meters (m^2) and ρ (rho) is the electrical resistivity of the metal given in ohm-meters (Ω·m). Electrical resistivities for metals are not constant and increase linearly with temperature in a limited range. Thus, reported metal resistivities are provided at a standard reference temperature of 20°C which is approximately room temperature for practical purposes. Published gold film resistivities differ slightly but a commonly reported value[130] is 2.44×10^{-8} Ω·m at 20°C. Inserting the Au resistivity reference value along with the measured Au interconnect M1 structure dimensions into Equation (4.1) gives a calculated resistance of

$$R = 2.44 \times 10^{-8}\,\Omega\text{m}\left[\frac{450 \times 10^{-6}\,\text{m}}{\left(1.95 \times 10^{-6}\,\text{m}\right)\left(1.02 \times 10^{-6}\,\text{m}\right)}\right] = 5.52\ \Omega.$$

The measured resistance statistical mean obtained for the Au M1 test structures shown in Figure 4.3 is 5.56 Ω. The measured Au M1 test structure resistance mean in comparison with the calculated resistance value shows remarkable congruence and garners confidence in the resistance measurements.

4.1.2 Via1 / Metal 1 Test Structure Resistance

In experimental phases (I and II), the Au interconnect via test structure was a two-level metal structure containing both a metal 1 and metal 2 line segment. Each metal line segment was 5 μm wide and 400 μm long with an overall test structure length of 800 μm. Au film thicknesses for metal 1 and metal 2 were 1 μm and 2.6 μm, respectively. These via test structures were wire bonded to force current flow from metal 2 through the centered via into metal 1 to induce failure at the via1 / metal 1 (V1M1) interface. Initial room temperature resistances were measured on the Au V1M1 test structures prior to electromigration testing. Figure 4.5 provides the initial resistance distribution for the Au V1M1 test structures in phase II.

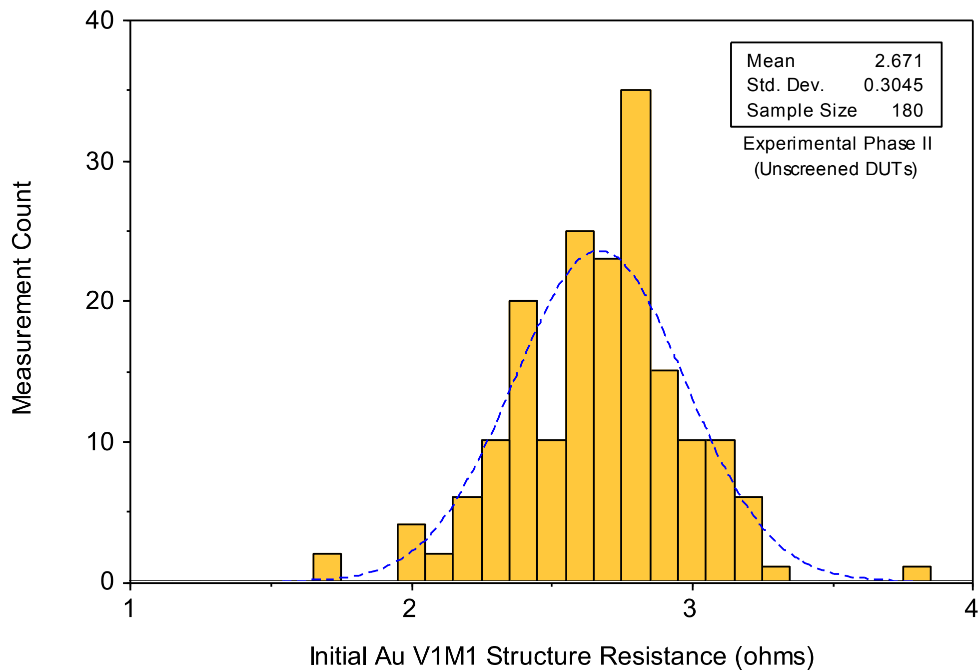


Figure 4.5 Initial Au V1M1 test structure resistance distribution (phase II).

In experimental phase II, the Au V1M1 test structures had a resistance distribution mean of 2.67 Ω with a standard deviation of 0.30 Ω and a resistance range of 1.7 Ω to 3.8 Ω. Although the Au V1M1 test structures were the same length as the phase II Au M1 test structures, the standard deviation of the Au V1M1 test structures was less than half that of the Au M1 test structures. It is expected that the much wider line-width of the Au V1M1 test structures would be less sensitive to the impact of Au electroplating non-uniformity.

In experimental phases (III – V), the Au V1M1 test structure was also shortened to 450 μm. However, the redesigned V1M1 test structure had only one metal 1 line segment that terminated into via 1 on both ends. This test structure design ensures that the via 1 / metal 1 interface is stressed regardless of the direction of forced current. Figure 4.6 displays the initial resistance distribution for the Au V1M1 test structures tested in phase V.

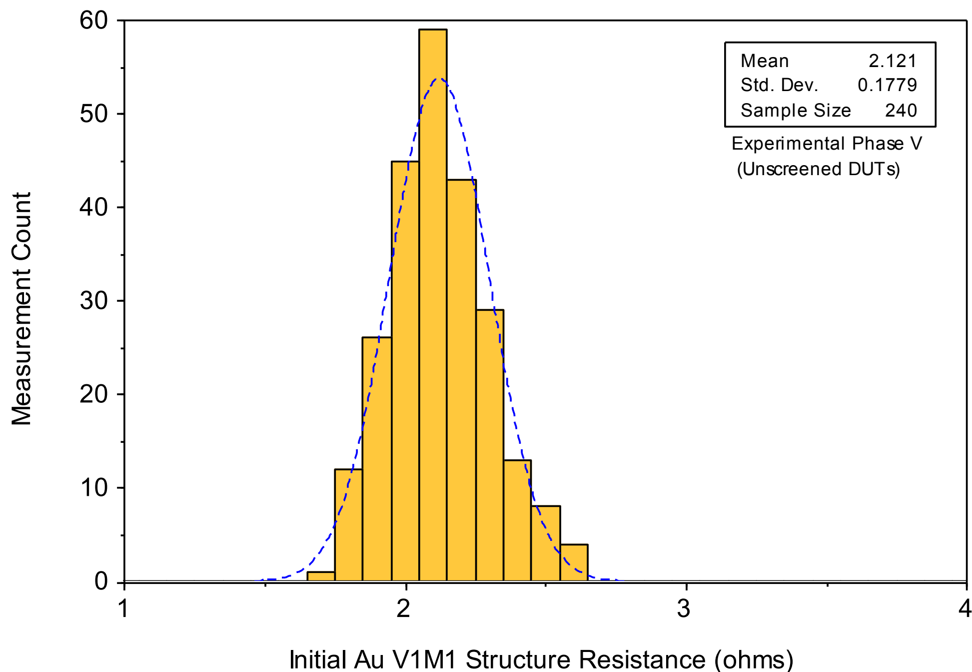


Figure 4.6 Initial Au V1M1 test structure resistance distribution (phase V).

Phase V consisted of a larger sample size of Au interconnect M1 and V1M1 test structures because more temperature electromigration experiments containing 60 DUTs each were carried out. Standard deviation of this resistance distribution was very low at 0.18 Ω with a mean value of 2.12 Ω. The resistance range was from 1.74 Ω to 2.61 Ω. Comparing the Au V1M1 test structures in phase II and phase V, it is discerned that the standard deviation decreased from 0.30 Ω to 0.18 Ω, which is a 40% reduction. Analogous to the Au M1 test structure, the shorter Au V1M1 test structure had a lower resistance standard deviation due to being less impacted by Au electroplating film uniformity variation.

To compute the resistance of the phase II Au V1M1 test structure, Equation (4.1) is expanded for the metal 1 and metal 2 line segments.

$$\mathrm{R} = \rho\left[\left(\frac{L_1}{w_1 \times t_1}\right)+\left(\frac{L_2}{w_2 \times t_2}\right)\right]. \tag{4.2}$$

Entering the phase II Au V1M1 test structure dimensions with the Au resistivity into Equation (4.2) yields a calculated resistance,

$$\mathrm{R} = 2.44\times10^{-8}\,\Omega\mathrm{m}\left[\left(\frac{400\times10^{-6}\mathrm{m}}{\left(5\times10^{-6}\mathrm{m}\right)\times\left(1\times10^{-6}\mathrm{m}\right)}\right)+\left(\frac{400\times10^{-6}\mathrm{m}}{\left(5\times10^{-6}\mathrm{m}\right)\times\left(2.6\times10^{-6}\mathrm{m}\right)}\right)\right]$$

of 2.70 Ω. Comparing the measured resistance mean of 2.67 Ω with the calculated resistance of 2.70 Ω, a very close match is found. Note that the centered via resistance of the V1M1 test structure (~ 0.02 Ω) was not included in the resistance calculation since its contribution is relatively insignificant.

Now, calculating the resistance of the phase V Au V1M1 test structure a resistance of 2.20 Ω is obtained. Close equivalence is also demonstrated between the measured mean of 2.12 Ω with the calculated resistance of 2.20 Ω.

4.2 Temperature Coefficient of Resistance and Film Temperature

Obtaining precise temperature coefficients of resistance (TCRs) were essential for determining accurate Joule-heated film temperatures for the Au interconnect test structure. All Au interconnect test structures had a TCR test before electromigration testing commenced. TCR tests were composed of resistance measurements collected at 4 to 5 uniformly spaced oven temperatures including the electromigration stress temperature. Resistance measurements were taken using a low current to avoid inducing any Joule heating. Additionally, a predefined higher stress current was used to measure resistance as described previously in the two-current method. Figure 4.7 displays the resistance data of a group of 60 Au M1 test structures versus the ramped oven temperature for TCR determination in experimental phase V.

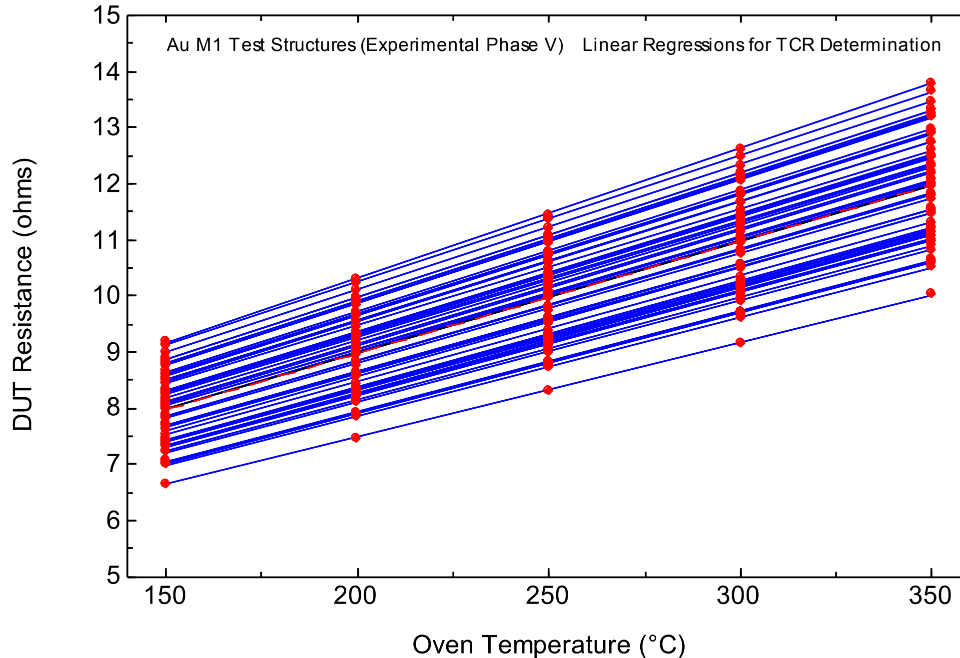


Figure 4.7 Au M1 structure resistance versus oven temperature (phase V).

The resistance of each individual Au M1 test structure was measured during the ramped TCR temperature test. All individual resistances were fitted with a least squares linear regression to compute the line slopes. In this manner, line slope and y-intercept values were obtained for each independent Au interconnect test structure. The y-intercepts were extrapolated as the reference resistance at 0°C. Furthermore, TCRs were determined for each Au interconnect test structure based on its line slope and reference resistance.

Since all 60 linear regressions fitted to the Au M1 test structure resistance data in Figure 4.7 are cluttered and overlap, a simplified example is illustrated by graphing only three DUTs in determining the TCR. Figure 4.8 shows the Au M1 (DUTs #1, 10, & 50) test structure resistance versus TCR oven temperature. Linear regressions were fitted to the resistance measurements versus TCR oven temperature for these three Au M1 structures.

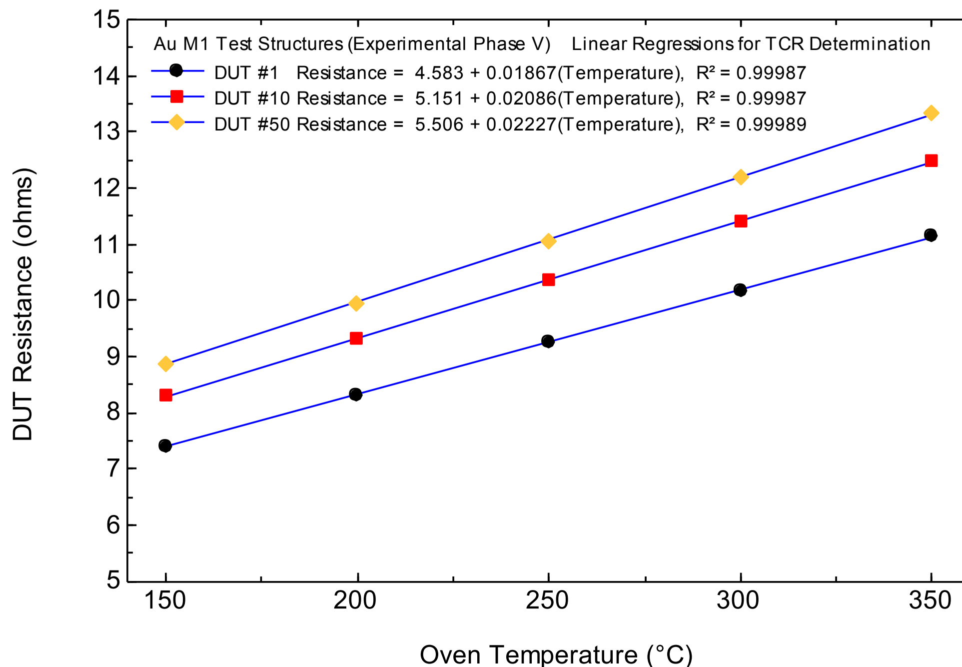


Figure 4.8 Au M1 (DUTs #1, 10, & 50) structure resistance versus temperature.

Linear regressions for the three TCR Au M1 test structure resistance measurements yielded a goodness of fit (R^2) of nearly 1 signifying a strong linear dependence within this temperature range. The line equations with the reference resistance at 0°C (y-intercept) and line slopes are shown in Figure 4.8. These particular Au M1 test structures were chosen to exemplify the relative range of reference resistances of 4.58 ohms to 5.51 ohms. The line slope values also had an approximate range of 0.00187 to 0.00222 ohms / °C. Using Equation (4.3) the TCR can be calculated.

$$\alpha_0 = \frac{1}{R_0}\left(\frac{\Delta R}{\Delta T}\right) = \frac{1}{R_0}(\text{Slope}). \qquad (4.3)$$

In doing so a TCR of 0.004074 per °C is determined for the Au M1 test structure (DUT #1).

Given that TCRs are usually specified at 20°C a reference resistance ($R_{ref.}$) at 20°C can be determined by Equation (4.4).

$$R_{ref.} = R_0 + \left(\frac{\Delta R}{\Delta T}\right)(T_{ref.}) = R_0 + (\text{Slope})(T_{ref.}). \qquad (4.4)$$

For the Au M1 test structure (DUT #1) the reference resistance at 20°C is 4.956 ohms. Recalculating using Equation (4.3), a TCR of 0.003767 per °C at 20°C is determined for the Au M1 test structure (DUT #1). Table 4.1 lists reference resistances and TCRs at both 0°C and 20°C.

Table 4.1 Au M1 test structure reference resistances and TCRs.

DUT #	$R_{ref.}$ at 0°C (ohms)	TCR at 0°C (per °C)	$R_{ref.}$ at 20°C (ohms)	TCR at 20°C (per °C)
1	4.583	0.004074	4.956	0.003767
10	5.151	0.004051	5.568	0.003746
50	5.506	0.004045	5.951	0.003742

Even though the reference resistance and line slope values varied among the Au M1 test structures, the extracted TCRs are very similar. A TCR of 0.003753 per °C at 20°C derived from the CRC Handbook[131] closely matches the measured TCRs in Table 4.1.

Practical use of the TCR is realized through determining the Joule-heated film temperatures of the Au interconnect test structures induced by the stress currents during electromigration testing. As mentioned, all independent Au interconnect test structures are measured for resistance during the TCR temperature ramp test permitting individual TCRs to be extracted. Thus, an individual film temperature is derived for each Au interconnect test structure. The standard (low current) and two-current methods for obtaining Joule-heated film temperatures were described thoroughly in the experimental methods section. For sake of discussion, the TCRs and film temperatures obtained from both methods for all 60 Au M1 test structures in phase V tested at 350°C oven temperature are outlined in Table 4.2. An inconsequential difference is noticed in the TCRs obtained by the standard (low current) and two-current methods. Averaging the 60 Au M1 test structure film temperatures shows a diminutive difference of 0.3°C. The small disparity in TCRs and film temperatures between the standard (low current) and two-current methods is negligible because the selected low current was too low to induce Joule heating yet well above the measurement resolution limitations. The two-current method becomes more beneficial when the chosen low current induces Joule heating or is near the measurement resolution limit. Nevertheless, all TCRs and film temperatures quoted will be referenced from the two-current method.

Table 4.2 TCRs and film temperatures determined by both methods.

DUT #	Standard (Low Current) Method		Two-Current Method	
	TCR at 0°C (per °C)	Film Temperature (°C)	TCR at 0°C (per °C)	Film Temperature (°C)
1	0.004074	359.0	0.004103	358.7
2	0.004146	359.6	0.004180	359.4
3	0.004036	359.7	0.004068	359.4
4	0.004137	358.9	0.004165	358.7
5	0.004105	358.4	0.004130	358.2
6	0.004065	358.6	0.004091	358.4
7	0.004113	359.6	0.004143	359.4
8	0.004073	359.0	0.004102	358.7
9	0.004027	358.4	0.004056	358.2
10	0.004051	359.2	0.004083	358.9
11	0.004085	360.7	0.004116	360.5
12	0.004021	359.7	0.004060	359.4
13	0.004130	359.0	0.004159	358.7
14	0.004078	360.5	0.004111	360.3
15	0.004037	359.5	0.004067	359.2
16	0.004120	358.3	0.004146	358.1
17	0.004069	358.9	0.004099	358.7
18	0.004018	358.8	0.004045	358.6
19	0.004026	360.1	0.004059	359.8
20	0.004093	359.2	0.004123	359.0
21	0.004026	359.3	0.004057	359.0
22	0.004034	358.1	0.004062	357.8
23	DUT #23 did not register a resistance measurement during the continuity check			
24	0.003986	358.7	0.004014	358.5
25	0.004051	358.1	0.004076	357.9
26	0.004098	358.2	0.004125	358.0
27	0.004006	358.3	0.004034	358.0
28	0.004019	358.6	0.004048	358.4
29	0.003954	359.4	0.003986	359.2
30	0.003968	359.0	0.003998	358.7

Table 4.2 Continued.

DUT #	Standard (Low Current) Method		Two-Current Method	
	TCR at 0°C (per °C)	Film Temperature (°C)	TCR at 0°C (per °C)	Film Temperature (°C)
31	0.004076	359.4	0.004105	359.2
32	0.004141	358.8	0.004171	358.6
33	0.004057	359.3	0.004088	359.0
34	0.004157	358.6	0.004184	358.4
35	0.004107	359.1	0.004137	358.9
36	0.004037	359.2	0.004064	359.0
37	0.004121	360.2	0.004153	360.0
38	0.004069	359.6	0.004098	359.3
39	0.003988	359.0	0.004018	358.8
40	DUT #40 did not register a resistance measurement during the continuity check			
41	0.004102	360.3	0.004132	360.1
42	0.004031	359.5	0.004069	359.1
43	0.004155	359.0	0.004186	358.7
44	0.004087	360.1	0.004118	359.9
45	0.004034	359.6	0.004065	359.3
46	0.004117	358.0	0.004142	357.8
47	0.004016	359.4	0.004047	359.2
48	0.004053	358.7	0.004081	358.5
49	0.004049	360.4	0.004084	360.1
50	0.004045	359.9	0.004075	359.7
51	0.003974	359.8	0.004008	359.6
52	0.004036	358.6	0.004068	358.4
53	0.003970	359.9	0.004002	359.7
54	0.004007	359.3	0.004036	359.1
55	0.004048	358.9	0.004075	358.7
56	0.004096	358.5	0.004122	358.3
57	0.003967	359.0	0.003997	358.7
58	0.003993	358.9	0.004022	358.6
59	0.003953	359.5	0.003984	359.3
60	0.003936	358.8	0.003962	358.6
Avg.	0.004053	359.2	0.004083	358.9

4.3 Resistance Degradation

The resistometric method was utilized to determine the electromigration lifetimes of the Au interconnect test structures. Continuous high-resolution resistance measurements monitored the formation and growth of voids in the Au interconnect test structures during accelerated electromigration testing. A specific resistance degradation ($\Delta R/R_0$ %) as a percentage from the initial Au structure resistance was selected and defined as the failure criterion.

The earliest experimental phases (I and II) utilized a resistance degradation failure criterion of 10%. However, this lower resistance degradation failure criterion produced noticeable bi-modal electromigration failure lifetime distributions. An extensive early lifetime failure population was pronounced and separated from a longer electromigration lifetime distribution. In addition, identification of the electromigration voids location within the Au interconnect test structures was challenging at this lower resistance degradation failure criterion. It became apparent that a 10% failure criterion was inadequate to completely characterize the resistance traces and electromigration lifetimes of the Au interconnect test structures. Therefore, in experimental phases (III – V) an increased resistance degradation failure criterion of 50% was utilized. As will be shown later, this was a key adjustment that helped mitigate the majority of the bi-modal electromigration failure lifetime distributions and promoted easier void location detection. It is important to emphasize that this higher resistance degradation failure criterion of 50% still avoids the uncontrolled thermal runaway condition associated with electromigration tests run until the interconnect line is catastrophically voided open.

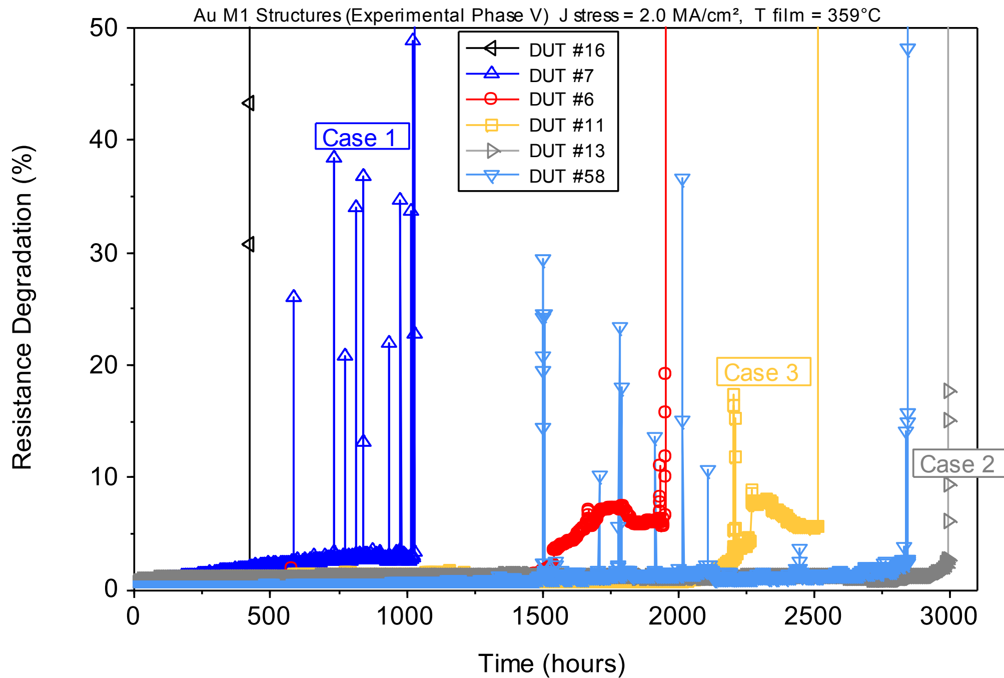


Figure 4.9 Resistance degradation of Au M1 structures during electromigration.

The electromigration resistance degradation characteristics of selected Au M1 test structures with a 50% failure criterion are shown in Figure 4.9. These Au M1 structures were stressed with a 40 mA current corresponding to a current density of 2 MA/cm^2. This specific electromigration test had a 350°C oven temperature with a calculated Au M1 structure film temperature of 359°C. Under these electromigration stress conditions, striking and varied Au M1 structure resistance characteristics are observed over time. Most striking are the multiple abrupt resistance spikes that return to a gradual resistance drift in a very short timeframe. This limited resistance characteristic is defined as case 1. Case 2 is the typical resistance characteristic as exhibited by Au M1 structures with a mostly flat resistance trace that eventually terminates with an abrupt increase in resistance to the 50% failure criterion. For the last resistance characteristic

defined as case 3, the resistance jumps up to near an 8% change and fluctuates back down to 6% over several hundred hours before abruptly spiking to reach the failure criterion of 50%.

Case 1 resistance characteristic exhibits several resistance spikes which are exemplified by DUT #7 and DUT #58. It should be noted that the case 1 resistance characteristic is not limited to Au M1 test structures with shorter electromigration lifetimes as exemplified by DUT #58 that survived to 2844 hours. Likewise, under identical electromigration conditions, case 2 resistance traces contained both short lifetimes (DUT #16 = 425 hours) and very long lifetimes (DUT #13 = 2991 hours) for the Au M1 structures. Case 3 characteristics are interesting since the resistance rises to a resistance peak of near 8% where it decreases followed by an abrupt resistance spike to the 50% failure criterion.

As previously mentioned, the selection of the resistance degradation failure criterion of 10% causes a more pronounced early failure population due to the case 1 resistance spikes. Figure 4.10 represents the electromigration resistance traces of the same six Au M1 test structures but now the cumulative probability graph is scaled to 10% resistance degradation. This graph clearly demonstrates that DUT #7 would have had a premature lifetime of 589 hours instead of 1031 hours if a 10% $\Delta R/R_0$ criterion was imposed. Similarly, DUT #58 would have failed earlier around 1505 hours as opposed to the 2844 hours where it reached with a 50% $\Delta R/R_0$ failure criterion. Therefore, selection of the resistance degradation failure criterion ($\Delta R/R_0$ %) was an extremely important parameter that was adjusted and optimized to enhance the understanding of the statistical Au electromigration failure distributions in this investigation.

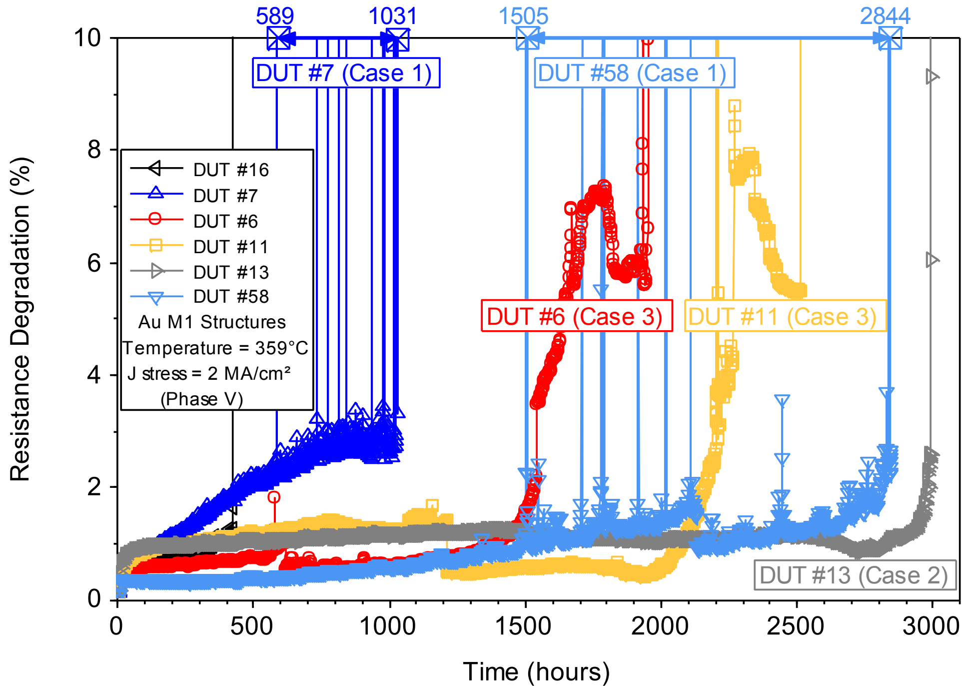


Figure 4.10 Resistance degradation of Au M1 structures with 10% scaled graph.

It is speculated that the resistance spike characteristic (case 1) in the Au M1 test structures was caused by a pre-existing void coalescence that rapidly heals returning to a steady-state resistance drift. A more in-depth analysis and physical evidence for this resistance characteristic is provided later. Another feature worth pointing out with case 3 resistance traces (DUT #6 and DUT #11) is a gradual resistance increase to approximately 1% that abruptly drops to 0.5%. It is possible a slight temperature decrease of a few degrees could cause this drop when the neighboring Au M1 structure finishes testing, thus reducing the Joule-heated die temperature. These six specific Au M1 test structures were showcased to provide an overview of the different resistance traces observed in this investigation. Postulation of the physical mechanisms responsible for these resistance characteristic cases is elaborated in Chapter 5.

4.4 Electromigration Lifetimes

4.4.1 Early Failures

Electromigration lifetimes of metal interconnects are dependent on experimental stress conditions, but fabrication process factors are also important. Electromigration lifetimes significantly improved with advanced interconnect metallizations, specifically electroplated Cu replacing Al(Cu) alloy thin films. Unfortunately, during the initial development of electroplated Cu interconnects, immature processes caused early failures to drastically reduce electromigration lifetimes. Similarly, electroplated Au interconnect electromigration lifetimes are reduced due to immature processes that impact the continuity and thin film thickness uniformity. Any pre-existing defects within the Au interconnects can provide void nucleation locations that profoundly reduce lifetimes. Pre-existing defects (especially those at critical locations) normally cause early failures that stand out from the electromigration failure distribution.

The selection of a lower resistance degradation change failure criterion can cause metallization with pre-existing defects to have lower electromigration lifetimes. A lower resistance degradation percent change failure criterion will enlarge the early failure population and amplify the bi-modal failure distribution. An example of extensive early failure population and distinctive bi-modal failure distribution was discovered for the Au M1 test structures when a 10% resistance degradation change failure criterion was selected. As discussed, some Au M1 test structures exhibited resistance spikes that rapidly recovered. A resistance degradation change failure criterion of 10% recorded Au M1 test structures with resistance spikes as failing much earlier, thereby preventing Au structures the possibility of recovering and surviving to a longer electromigration lifetime.

Figure 4.11 shows a cumulative failure probability graph for the Au M1 structure electromigration lifetimes with a 10% failure criterion in phase II. A current density of 3 MA/cm^2 on the Au M1 structures induced Joule-heated film temperatures of 342°C (325°C oven) and 374°C (350°C oven), respectively. These electromigration failure distributions display early failures that overlap between 10 to 100 hours. Using a 10% $\Delta R/R_o$ failure criterion, a distinct bi-modal characteristic is evident with the early failures deviating from the log-normal intrinsic failure distributions in Figure 4.11. Sigma values are a measure of the failure spread over time and for these distributions with sigma values as high as 1.76 and 1.03 are clearly indicative of multi-modal failure distributions.

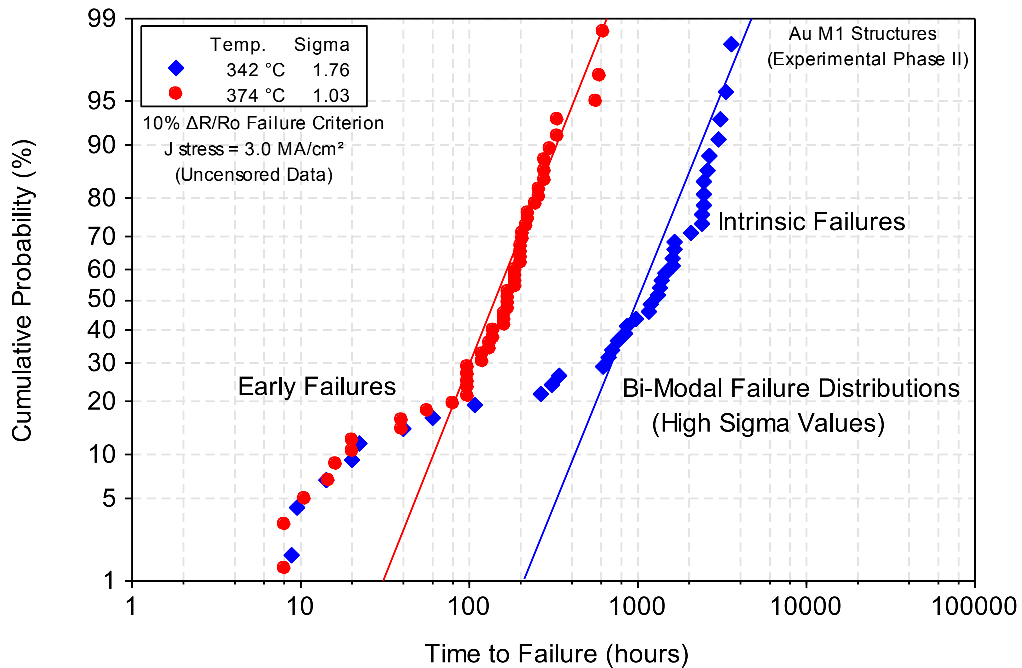


Figure 4.11 Au electromigration lifetimes with a 10% failure criterion.

Early (extrinsic) failures are normally caused by pre-existing defects such as voids or misprocessed interfaces within the metal interconnect. Foreign particles embedded within the metal thin films can also cause early failures. Most defects in metallization are at extremely low levels and thus are not usually detectable with the limited sample size of electromigration tests. Physical confirmation of a specific defect as a primary root cause for the early failures permits censoring or removing data leaving only the intrinsic failure population. In doing so a single intrinsic failure mode distribution is obtained possessing a lower sigma value and significantly longer extrapolated lifetimes.

Figure 4.12 exhibits only the intrinsic failure distributions for the Au M1 structures in phase II. After removal of the early failures, the intrinsic failure data fit log-normal distributions better and thus tighter sigma values of 0.513 and 0.412 were yielded.

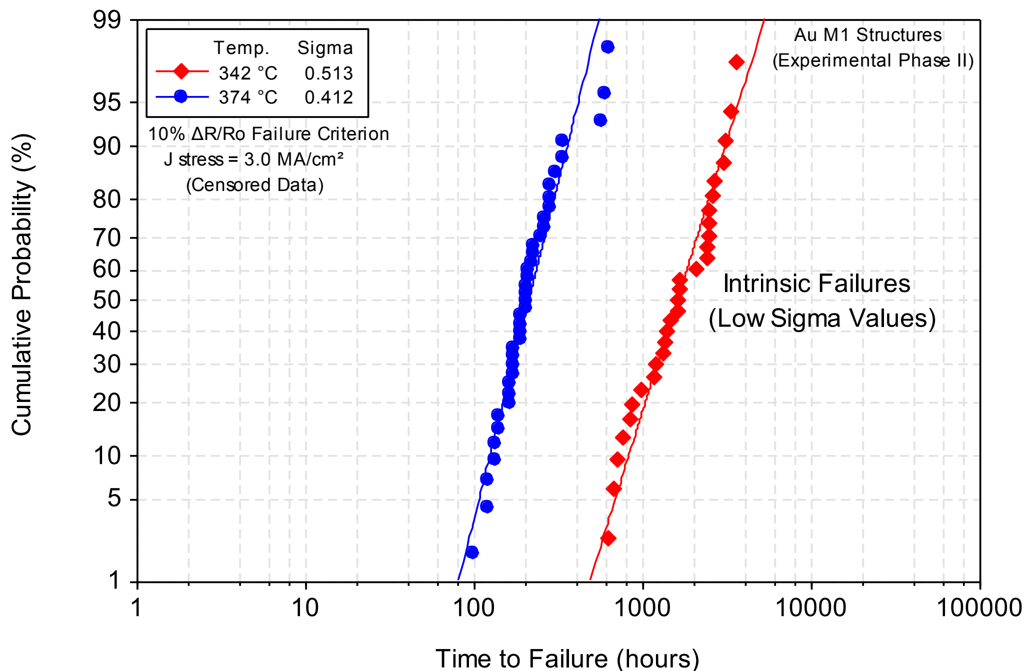


Figure 4.12 Intrinsic failure distributions after removal of early failures.

Although comprehensive physical verification of the root cause for the early failures was not yet conducted, examination of the electromigration resistance traces of some Au test structures with resistance spikes were found to cause early failures with the 10% failure criterion. The physical mechanism responsible for the resistance spikes and corresponding early failures is discussed later.

It was established that simply by selecting a higher resistance degradation change failure criterion percentage, the early failure population diminishes. In essence the higher failure criterion percentage allows the Au test structures with resistance spikes to recover and then fail at a later time among the intrinsic failure distribution. Figure 4.13 shows the electromigration lifetimes of Au M1 structures with a 50% failure criterion in phase III.

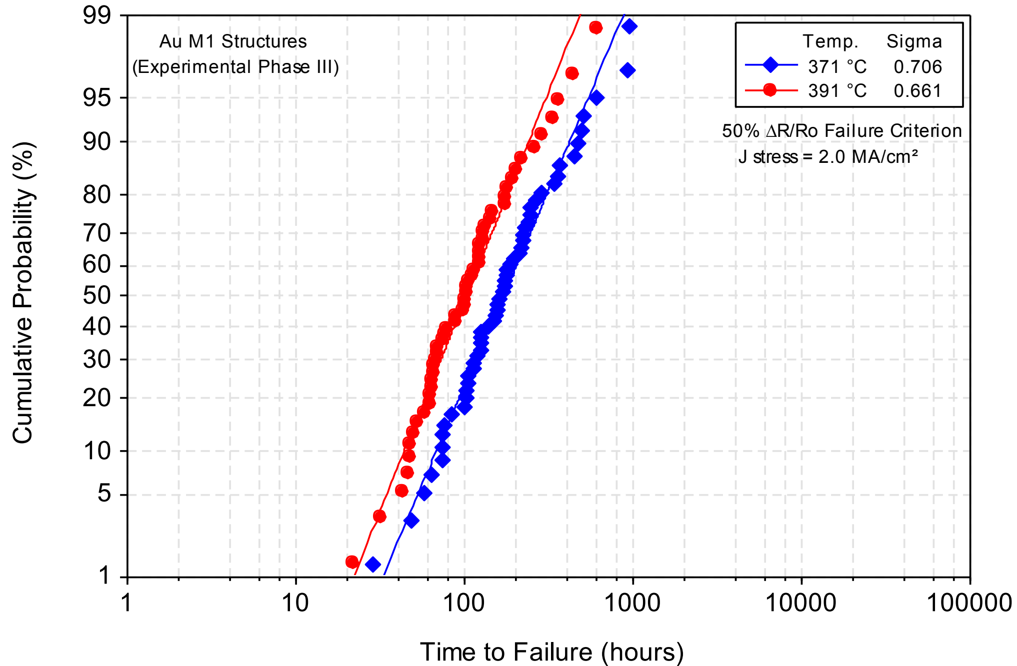


Figure 4.13 Au electromigration lifetimes with a 50% failure criterion.

Electromigration lifetime distributions based on a 50% failure criterion demonstrated a diminished early failure population eliminating bi-modality. Failure distributions with significantly tighter (lower) sigma values of 0.706 and 0.661 were achieved. Additionally, these electromigration lifetimes exhibit excellent fits to the log-normal distribution with lower bounded 90% confidence intervals shown in Figure 4.13. Another contributing factor in aiding the elimination of early failures was the redesigned shorter Au test structure implemented in phase III experiments. All subsequent electromigration lifetime results at these temperatures benefited from the 50% failure criterion and the redesigned shorter Au test structure.

4.4.2 Test Structure Lifetimes

As introduced in the test structure design section, electromigration lifetimes are dependent on the physical layout of the metal interconnect test structure. A single-level metal test structure where the stress current is forced and flows laminar through a flat metal line has a dramatically longer electromigration lifetime compared to a two-level metal test structure where a fixed interface causes flux divergence. Flux divergence at metal grain boundary triple points acts as a catalyst for the electromigration voiding mechanism in flat metal line test structures possessing polycrystalline microstructures. Two-level metal test structures force the stress current through a wider metal tap line and then down through a via into a narrower metal line. Flux divergence at the fixed via / narrower metal line interface causes electromigration wear-out to occur. In addition, the increased current crowding and localized Joule heating at the fixed via / metal line interface significantly accelerates electromigration.

A well-designed Au via 1 / metal 1 (V1M1) interface test structure was also evaluated in comparable electromigration experiments. Since the Au V1M1 test structure was wider than the Au M1 test structure, the same stress conditions could not be exactly matched. Specifically, applying the same stress current on both structures would translate into different current densities. Likewise, applying the same current density on both structures would lead to dissimilar film temperatures because of the varied Joule heating transfer rates associated with the surface area differences. Nevertheless, the metal film temperatures on both test structure types were closely matched but only through the use of different current densities. Figure 4.14 provides a relative comparison of the Au M1 and V1M1 test structure electromigration lifetimes.

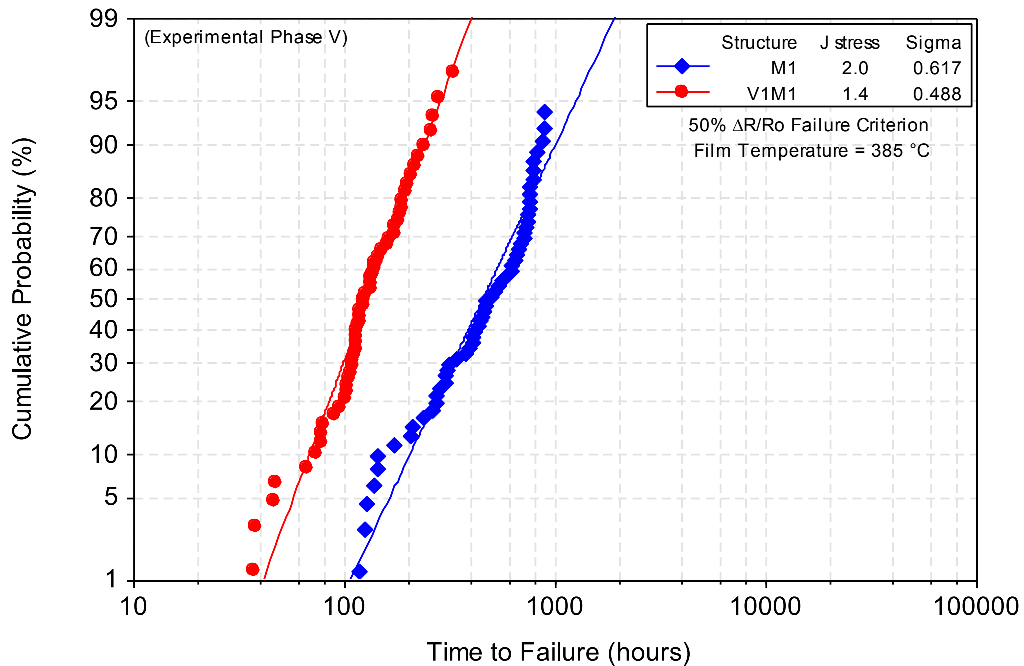


Figure 4.14 Au M1 and V1M1 test structure electromigration lifetimes.

A Joule-heated film temperature of 385°C was identical on both structure types although stress current densities were different for the Au M1 and V1M1 test structures. Joule heating of 10°C was generated on both Au test structures with an oven temperature of 375°C. The V1M1 structure had a higher stress current of 79.23 mA compared with 39.84 mA for the M1 structure but its cross-sectional area was 2.8 times larger yielding a lower current density. The median ($t_{50\%}$) electromigration lifetimes for the M1 and V1M1 structures were 452 hours and 120 hours, respectively. Even though the stress current was 2 times higher on the Au V1M1 structure, its electromigration lifetime was nearly 4 times shorter. In all experimental phases (I – V), lower electromigration lifetimes for the V1M1 structures compared to the M1 structures were reproducible. The lower V1M1 structure electromigration lifetimes were expected because of the factors of flux divergence, current crowding, and localized Joule heating at the via 1 / metal 1 interface. Due to these factors, two-level via interface test structures are considered the limiting electromigration reliability circuit element, and therefore are the standard test structures evaluated in most electromigration experiments.

In this original electromigration investigation on passivated electroplated Au metallization, the focus was primarily on the less complicated Au M1 test structure in order to gain better insight on the grain boundary diffusion and failure mechanisms as well as to obtain accurate parameters for Black's fundamental electromigration model. Nevertheless, the activation energy was also extracted from electromigration lifetimes of the V1M1 test structure at different temperatures with the same current density.

4.5 Electromigration Activation Energy

Since electromigration lifetimes are exponentially dependent on temperature, it is extremely critical to extract an accurate activation energy at accelerated stress conditions. Determination of activation energies can vary due to several reasons including inaccuracies in the measurement method, the deposited metallization microstructure, the quality of the encapsulated passivation film, and various operating diffusion mechanisms. Through use of the high-resolution resistometric method, precise times were determined for the Au electromigration lifetimes, surpassing other technique capabilities. An established quality SiN passivation film encapsulated all the Au test structures permitting evaluation of a realistic compound semiconductor interconnect device. The combined sputtered Au seed layer and electroplated Au film was subsequently annealed to produce a homogenous microstructure that is a thermally stable thin film in terms of resistance. All feasible efforts were taken to mass manufacture a realistic and stable Au thin film for extracting accurate activation energies.

Multiple stress temperatures were selected with an approximate temperature range of 100°C for extracting the Au electromigration activation energy. Experimental current densities were confined to minimize Joule heating to ensure obtaining accurate film temperatures. In each experimental phase, stress conditions were altered and subsequently optimized to improve the extraction of the passivated electroplated Au electromigration activation energy. Censoring of the data was necessary in cases where early failures produced extensive bi-modal distributions and in order to account for DUTs that did not reach failure before terminating a long-term experiment.

In experimental phase III, Au electromigration tests had a stress current density of 2.0 MA/cm^2 with three oven stress temperatures of 325°C, 350°C, and 375°C. At this current density stress, an average Joule-heated film temperature of 16°C above the ambient oven temperature was induced on the Au M1 structures. Figure 4.15 displays the electromigration lifetime distributions for the Au M1 structures with the determined film temperatures in phase III.

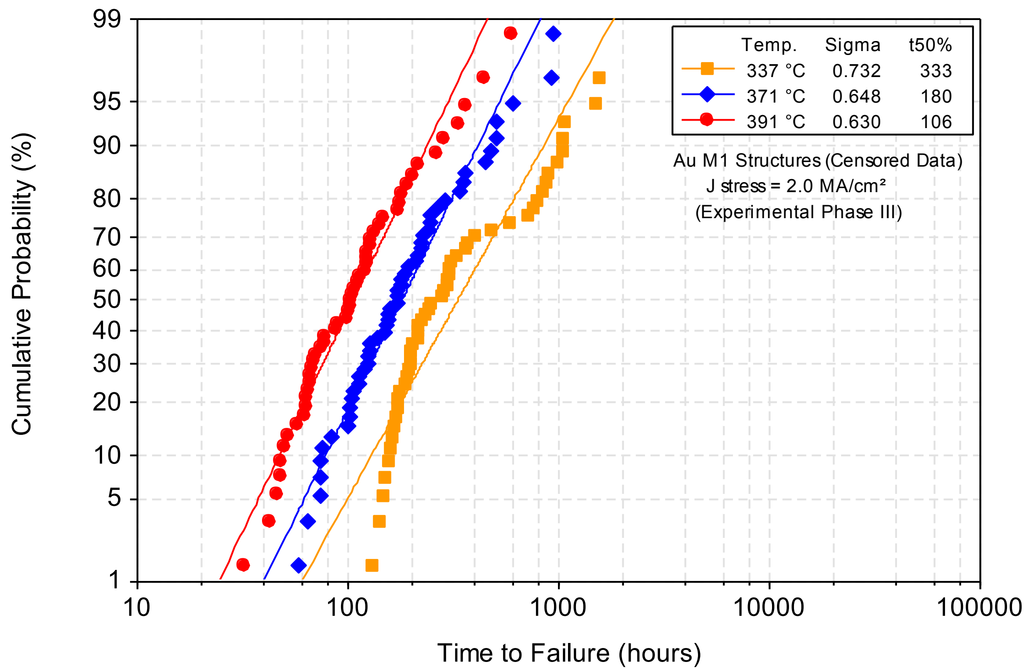


Figure 4.15 Electromigration lifetimes for the Au M1 structures (phase III).

The median electromigration lifetimes ($t_{50\%}$) ranged from 106 hours to 333 hours for Au M1 film temperatures of 391°C to 337°C. Failure distribution spread increased with sigma values of 0.63, 0.65, and 0.73 for decreasing film temperatures. Log-normal distributions were well fitted at both the 371°C and 391°C temperatures. However, a distinct inflection in the failure data is observed at 337°C causing a poor log-normal fit with an associated sigma value of 0.73.

At the 337°C temperature a clear bi-modality was present with 70% of the distribution under one failure mechanism and the remaining 30% of failures under a potentially different failure mechanism. Nevertheless, the 337°C failure distribution was included in the activation energy calculation. Figure 4.16 shows the Arrhenius plot of the median Au M1 electromigration lifetimes versus 1/*kT*.

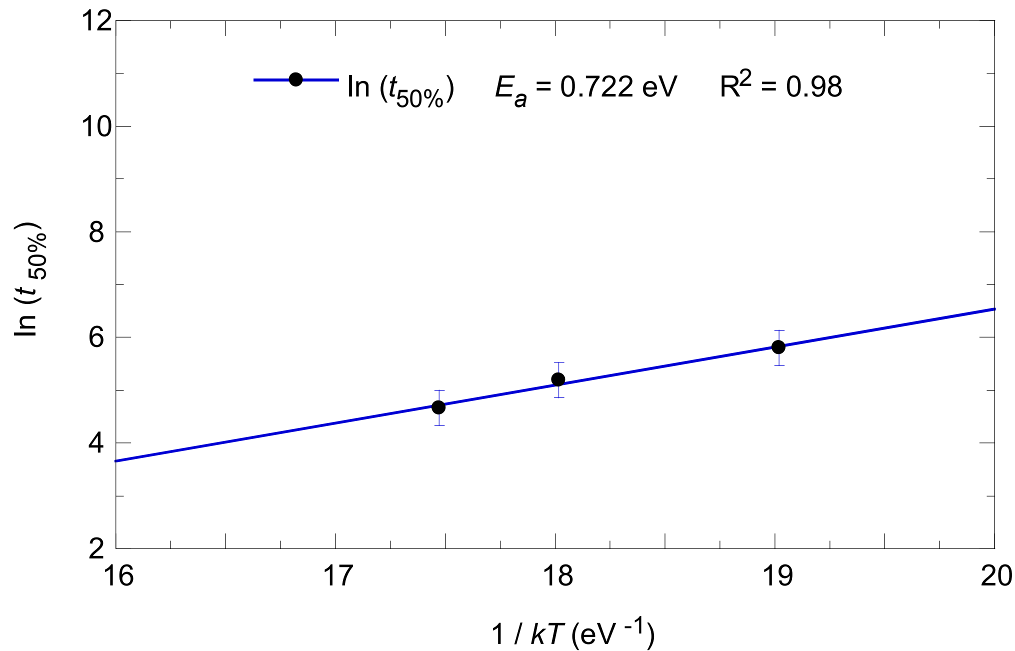


Figure 4.16 Arrhenius plot of median Au M1 electromigration lifetimes (phase III).

The data were fitted to a least squares linear regression with a corresponding coefficient of determination (R^2) value of 0.98. The slope of the fitted line yields an activation energy (E_a) of 0.72 eV. This E_a is considered on the low end of the reported values for Au electromigration but still within the range. When the 337°C data set is excluded, the extracted activation energy is 0.97 eV which is on the high end of the range reported by other investigators shown in Table 2.6.

In experimental phase IV, the current density was lowered to 1.5 MA/cm^2 to reduce Joule heating on the Au M1 structures to better understand the extensive bi-modality noticed at the lowest temperature. The same three oven stress temperatures of 325°C, 350°C, and 375°C were used. The electromigration lifetime distributions of the Au M1 structures in experimental phase IV are presented in Figure 4.17.

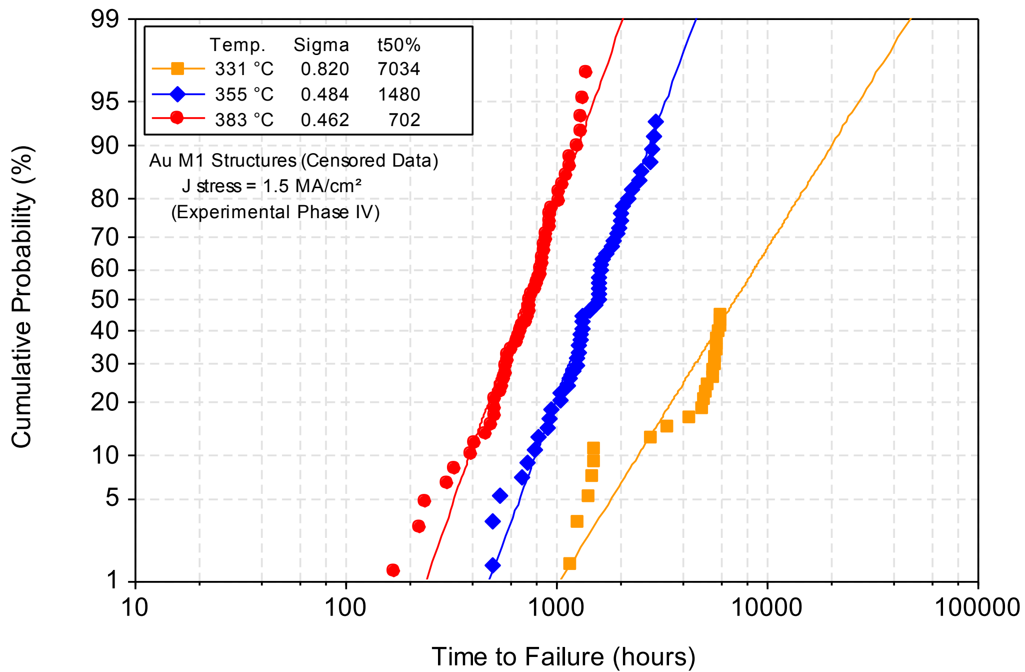


Figure 4.17 Electromigration lifetimes for the Au M1 structures (phase IV).

The lower current density reduced the average Joule heating on the Au M1 structures to 6°C from 16°C. However, electromigration test times increased significantly to the extent that the lowest temperature test of 331°C was not finished after 7000 hours. The median electromigration lifetimes ($t_{50\%}$) ranged from 702 hours to beyond 7000 hours. The spread in the failure distribution slightly improved with sigma values of 0.46 and 0.48 but the lowest temperature

had a higher sigma of 0.82. A distinct multi-modal failure distribution is again observed at the lowest temperature of 331°C. The large sigma value for this distribution indicates that different failure mechanisms exist and are triggered near 330°C. An unrealistic value of 1.51 eV is attained for activation energy when including the lowest temperature median lifetime data. Figure 4.18 shows the Arrhenius plot of the three median Au electromigration lifetimes versus 1/*kT*.

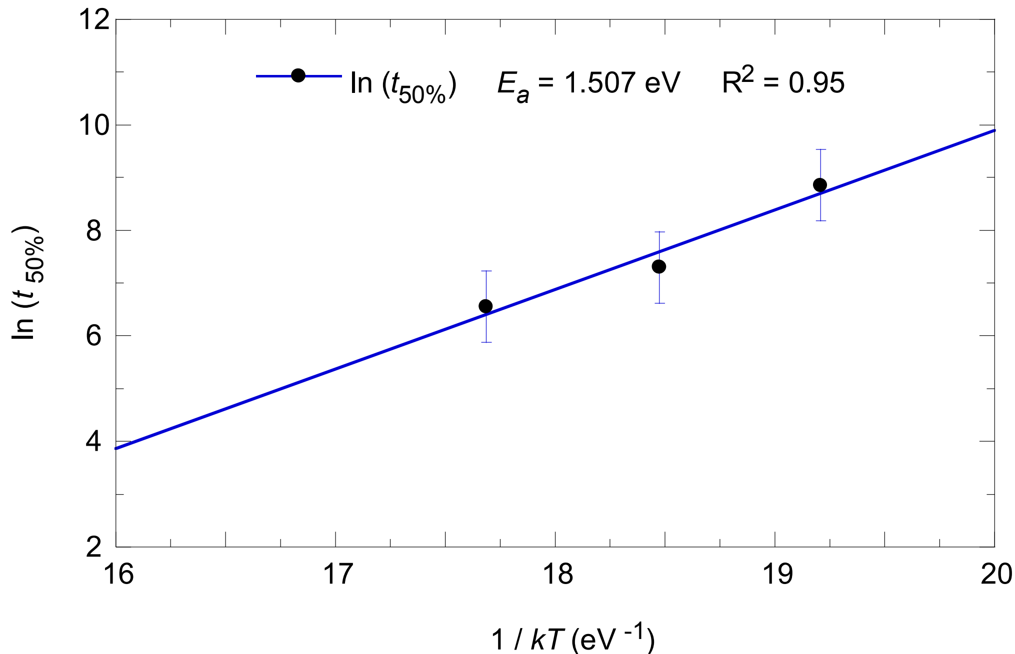


Figure 4.18 Arrhenius plot of median Au M1 electromigration lifetimes (phase IV).

This high activation energy is close to the value for bulk Au lattice self-diffusion which is highly unlikely to be an accurate value given the multitude of grain boundaries in this polycrystalline Au thin film. Thus, the validity of 1.51 eV for Au electromigration is doubtful. Exclusion of the multi-modal distribution median lifetime at 331°C results in an activation energy of 0.95 eV, which is nearly the same value obtained in phase III for the two highest temperatures.

Additional stress temperatures were implemented in the final experimental phase V to extend the temperature range and to improve the statistical confidence with the extracted activation energy for Au electromigration. The current density of 2.0 MA/cm^2 was reselected to ensure all electromigration tests would be completed in a practical timeframe (< 10,000 hours). The four chosen oven stress temperatures were 300°C, 350°C, 360°C, and 375°C but excluded 325°C due to the dominant multi-modal failure mechanisms observed at that temperature. A cumulative probability plot of the Au M1 structure electromigration lifetimes in phase V are shown in Figure 4.19.

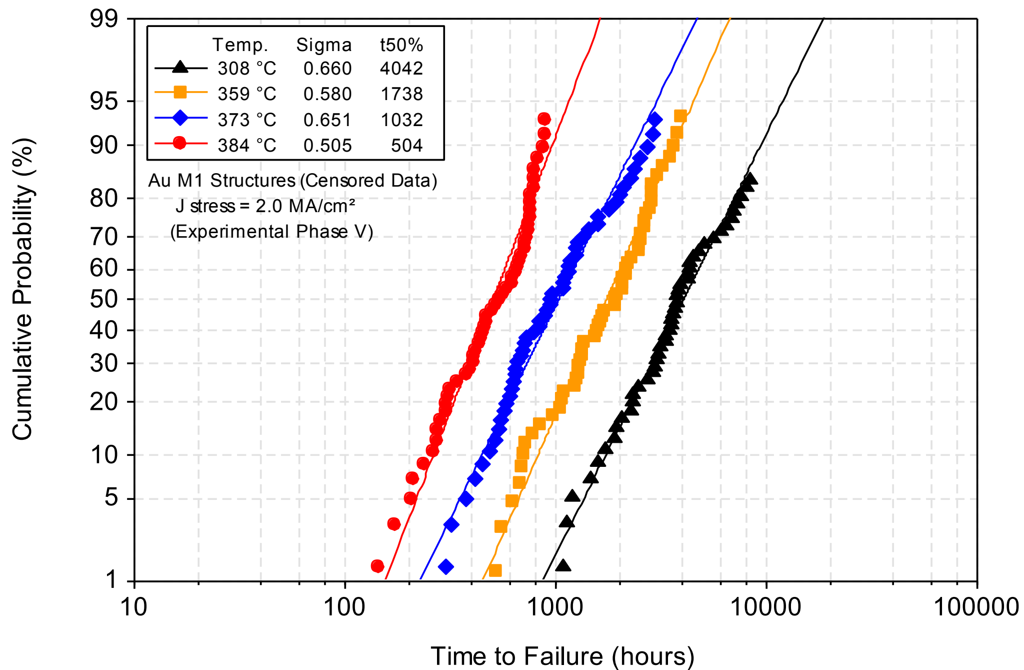


Figure 4.19 Electromigration lifetimes for the Au M1 structures (phase V).

The current density of 2.0 MA/cm^2 induced an average Joule heating of 10°C on the Au M1 structures. The median electromigration lifetimes ($t_{50\%}$) ranged from 504 hours to 4042 hours. The average sigma value for all

electromigration failure distributions was 0.60 which is a reasonable indication that a mono-modal failure mechanism is present. The log-normal model fits the electromigration failure distributions noticeably well in Figure 4.19. It is significant that the lowest temperature test at 308°C showed no failure distribution shifts, indicating a mono-modal failure mechanism unlike that shown with the 331°C failure distribution in phase IV. Another noteworthy factor was the duration of 8400 hours (350 days) for the electromigration test at 308°C facilitated by the uninterrupted power and excellent equipment reliability.

Figure 4.20 displays the Arrhenius plot of the Au M1 structure median electromigration lifetimes versus 1/*kT* in phase V. An activation energy (E_a) of 0.80 eV was determined from the slope of the fitted line to the four median electromigration lifetimes. The R^2 of 0.90 signifies a strong linear relationship.

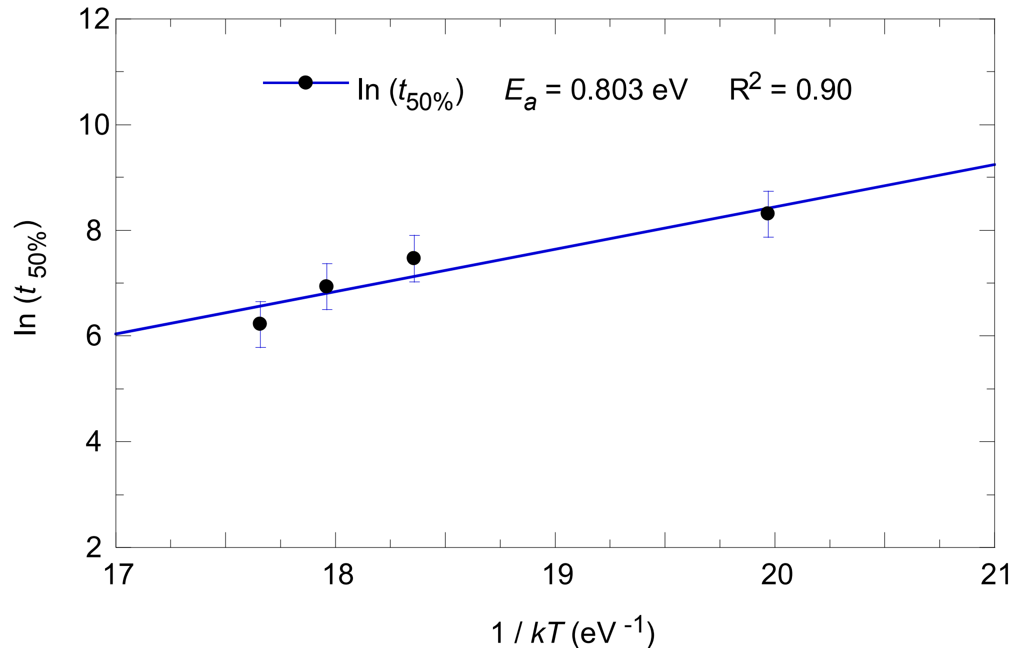


Figure 4.20 Arrhenius plot of median Au M1 electromigration lifetimes (phase V).

This extracted E_a is in the middle of the reported literature values for a variety of different Au film types shown in Table 2.6. This activation energy is the first reported value for passivated electroplated Au films stressed with minimal Joule heating.

The Au V1M1 test structures were also evaluated in similar electromigration experiments to determine activation energy. Because the V1M1 structures are wider, a higher stress current than was applied to the Au M1 structures is necessary to match a current density of 2.0 MA/cm^2. However, this higher current would induce much higher Joule heating. Thus, a lower current density of 1.5 MA/cm^2 was chosen to maintain Joule heating near 10°C. The three oven stress temperatures were 300°C, 350°C, and 375°C. Figure 4.21 shows the cumulative probability graph of the Au V1M1 structure electromigration lifetimes in phase V. The V1M1 structure sigma values ranged from 0.38 to 0.57.

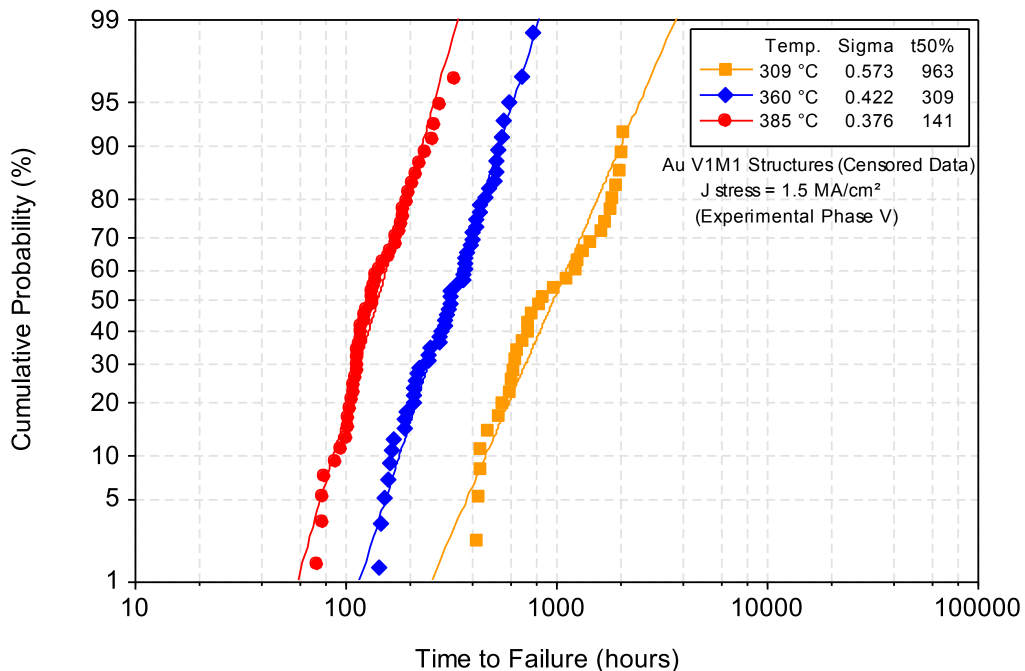


Figure 4.21 Electromigration lifetimes for the Au V1M1 structures (phase V).

A general trend is that the V1M1 test structures have lower sigma values compared to the M1 test structures because failures are forced at the via / metal interface as compared to broader potential wear-out along the polycrystalline line. A similar trend of increasing sigma values with lower temperature is observed. An Arrhenius plot of the Au V1M1 structure median electromigration lifetimes versus 1/*kT* is shown in Figure 4.22.

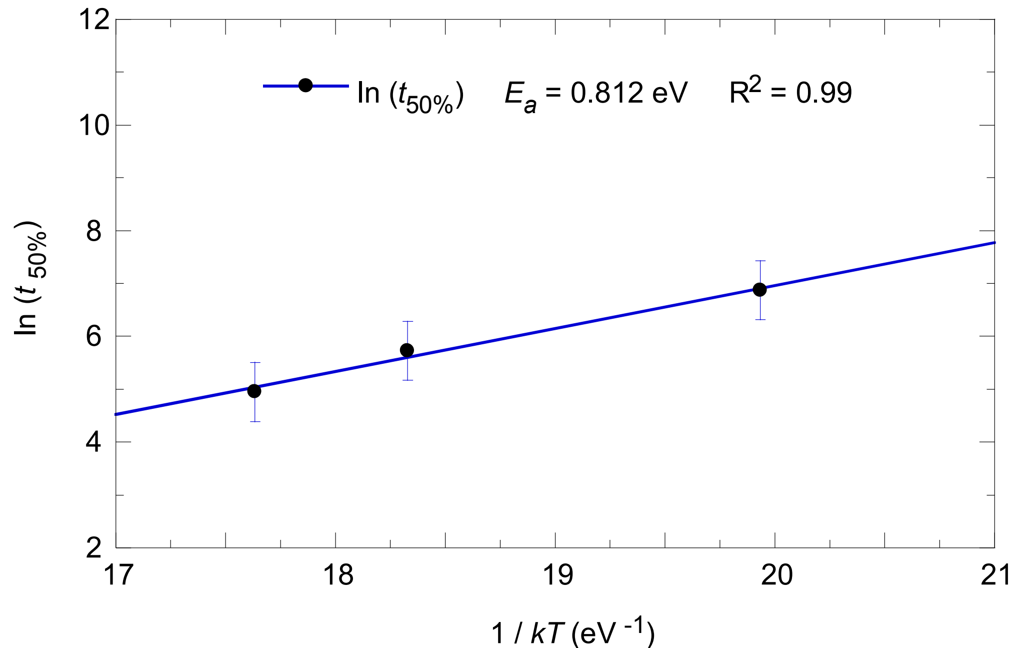


Figure 4.22 Arrhenius plot of median V1M1 electromigration lifetimes (phase V).

An activation energy of 0.81 eV was extracted from the slope of the line fitted to these three median electromigration lifetimes. A very strong linear relationship is demonstrated with a R^2 of 0.99. This extracted E_a is nearly the same as the activation energy obtained for the Au M1 structures. This repeated measurement on a different test structure confirms the validity of this activation energy for passivated electroplated Au films.

4.6 Current Density Exponent

The current density exponent (n) in Black's empirical model is assumed to be 2 based on historical electromigration data for Al interconnects. However, in other cases the reported measurement of the current density exponent has been found to range from 1 to 6 with the majority of values around 2. An extracted current density exponent close to 2 is found to be the result of the time it takes to nucleate a void within the line and corresponds to lifetimes controlled by void nucleation.[64] In contrast, measured current density exponents closer to 1 are controlled by the time it takes to grow a void to a certain size and is indicative of lifetimes that are limited by void growth.[132, 133] Current density exponents much above 2 are caused by either improper treatment of Joule heating from highly accelerated current density electromigration experiments or because of failures inhibited by the Blech length effect. Extraction of accurate current density exponents are important since inaccurately determined higher values of n increase the sensitivity of current density on the resulting extrapolated operational lifetimes.

In this investigation of passivated electroplated Au interconnects, four different current densities were used to stress the Au M1 structures at a constant oven temperature of 375°C. These current densities were 1.25, 1.5, 1.75, and 2.0 MA/cm^2 in order to restrict Joule heating. Figure 4.23 displays the cumulative probability graph of the Au M1 structure electromigration lifetimes at four different current densities. The measured Joule-heated temperatures ranged from 4°C for a current density of 1.0 MA/cm^2 to 9°C for a current density of 2.0 MA/cm^2. The median electromigration lifetimes ranged from 480 to 1318 hours. Sigma values were below 0.6 for all failure distributions suggestive of typical mono-modal

distributions. The expected trend of shorter electromigration lifetimes with increased current density was observed for the Au M1 structure lifetimes shown in Figure 4.23.

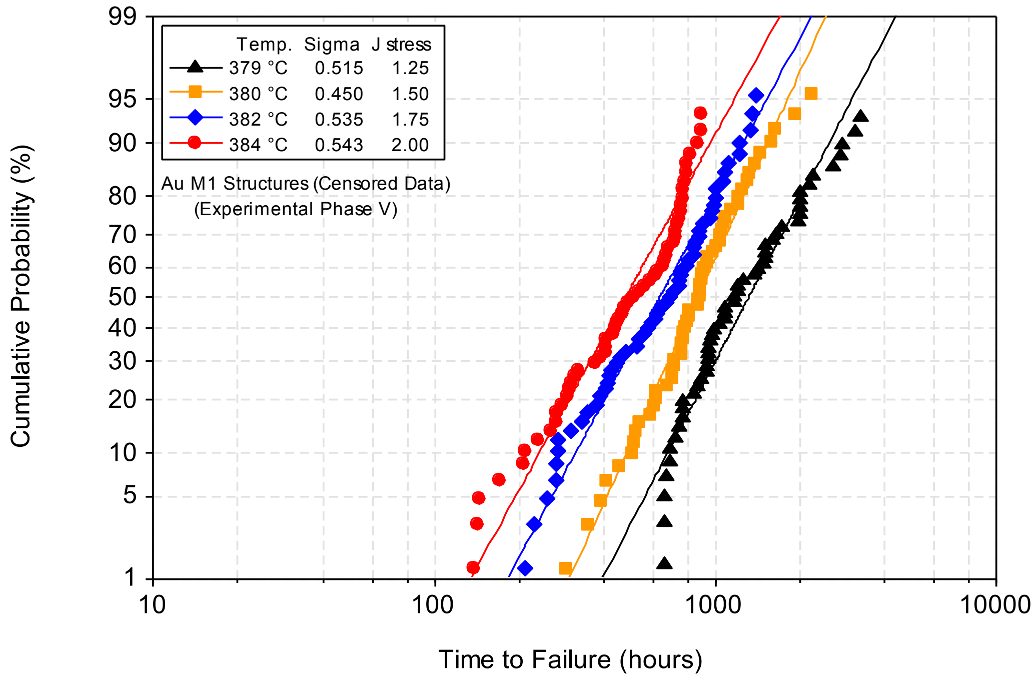


Figure 4.23 Electromigration lifetimes for the Au M1 structures at different *J*.

The current density exponent is determined from the slope of the fitted line of the data in the ln ($t_{50\%}$) versus ln (J) plot. The non-normalized Au M1 median electromigration lifetimes were plotted in the ln ($t_{50\%}$) versus ln (J) graph as shown in Figure 4.24. A strong linear correlation to the data is substantiated by the high R^2 of 0.99. This current density exponent of n = 2.14 is erroneous because the median lifetime data needs to be normalized to a single constant Au film temperature.

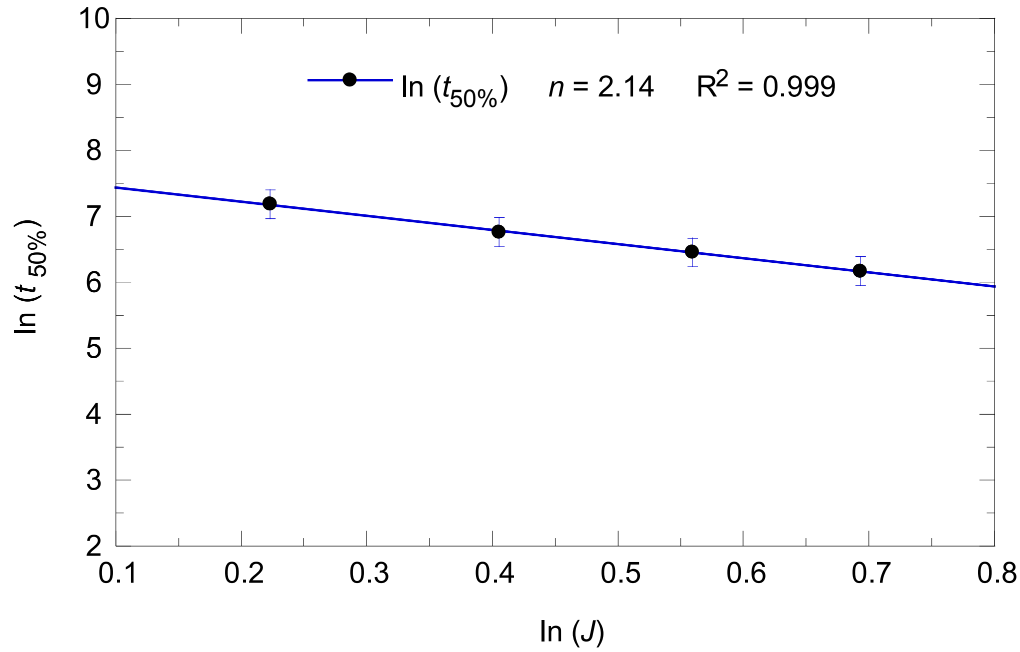


Figure 4.24 ln ($t_{50\%}$) versus ln (J) plot for non-normalized Au M1 median lifetimes.

The Au M1 structure median electromigration lifetimes were normalized through extrapolation to a single constant temperature using Equation (4.5).

$$t_{50\%\ (\text{normalized})} = t_{50\%\ (\text{stress})} \frac{e^{\left(\frac{E_a}{kT_{(\text{normalized})}}\right)}}{e^{\left(\frac{E_a}{kT_{(\text{stress})}}\right)}}. \tag{4.5}$$

The film temperature of 379°C was selected as the temperature that the median electromigration lifetimes were normalized to since it was the lowest film temperature induced by the lowest current density at 1.25 MA/cm^2. The predetermined activation energy of 0.803 eV and Boltzmann constant were used for the lifetime extrapolation. Table 4.3 displays the normalized median electromigration lifetimes at 379°C for all current density experiments.

Table 4.3 Normalized current density median Au electromigration lifetimes.

J_{stress} (MA/cm^2)	Stress Temperature (°C)	Median Lifetime (hours)	Normalized Temperature (°C)	Normalized Lifetime (hours)
1.25	379	1317.6	379	1317.6
1.50	380	886.4	379	885.6
1.75	382	635.7	379	678.6
2.00	384	480.0	379	535.1

Figure 4.25 shows the normalized Au M1 median electromigration lifetimes plotted in the ln ($t_{50\%}$) versus ln (J) graph. A current density exponent of n = 1.91 was extracted from the slope of the fitted line to the normalized data. This value aligns well with the void nucleation stage indicating that these electroplated Au interconnect electromigration lifetimes are mainly controlled by void nucleation as opposed to void growth kinetics.

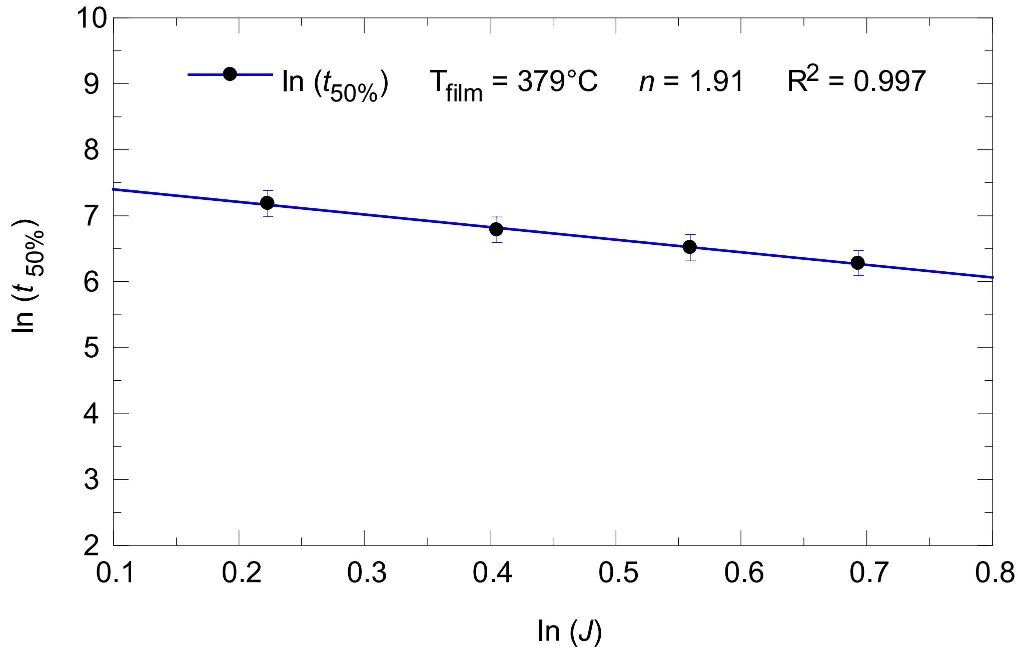


Figure 4.25 ln ($t_{50\%}$) versus ln (J) plot for normalized Au M1 median lifetimes.

4.7 Gold Structure Characterization

4.7.1 Gold Microstructure Analysis

The microstructure of a metal thin film has been well established to strongly influence electromigration failures and thus is a key factor to evaluate in reliability studies. In order to gain insight into electromigration in Au films and its statistical lifetime distributions, the microstructure of the electroplated Au film was characterized. The Au grain size distribution within the test structure lines was contrasted and imaged by a FEI Nova 600 DualBeam SEM / FIB instrument using the ion channeling technique. This SEM / FIB instrument consists of both an ion beam column (gallium ion source) and an electron beam column in a vacuum chamber enabling material samples to be milled and imaged simultaneously. Another significant benefit of this instrument is that the ion channeling effect produces higher contrast images in crystallographic materials than images obtained from the electron beam.[134]

Under high accelerating voltages, the incident Ga^{+} ions of a FIB penetrate into the crystallographic planes of the sample at various depths depending on the atomic spacing and alignment to the ion beam. An ion beam directly aligned down the crystallographic plane of a crystal (grain) allows ions to penetrate (channel) deeper that reduces secondary electron emissions and results in a darker grain appearance. Conversely, an ion beam obliquely aligned to the crystallographic plane of a sample limits ion penetration to the near surface that produces higher secondary electron emissions and as a result has a brighter grain appearance.[135] Therefore, the FIB ion channeling effect produces images with higher contrast among individual grains (crystals), enabling delineation of grain boundaries and subsequent grain size measurement.

Utilizing the ion channeling effect in the FIB, a planar surface view of the Au test structure microstructure was delineated. Figure 4.26 displays the ion-induced secondary electron (SE) image of the electroplated Au grains within the electromigration test structure. The image shows high contrast between Au grains possessing different crystal orientations and thereby enables the grain boundaries to be visibly delineated. At first observation the electroplated Au grains appear to be smaller than the 2 μm line-width of the test structure, which means this Au M1 test structure is not a bamboo-like microstructure. Manual image processing of this planar Au microstructure was performed in order to further enhance the grain boundaries to measure the average Au grain size.

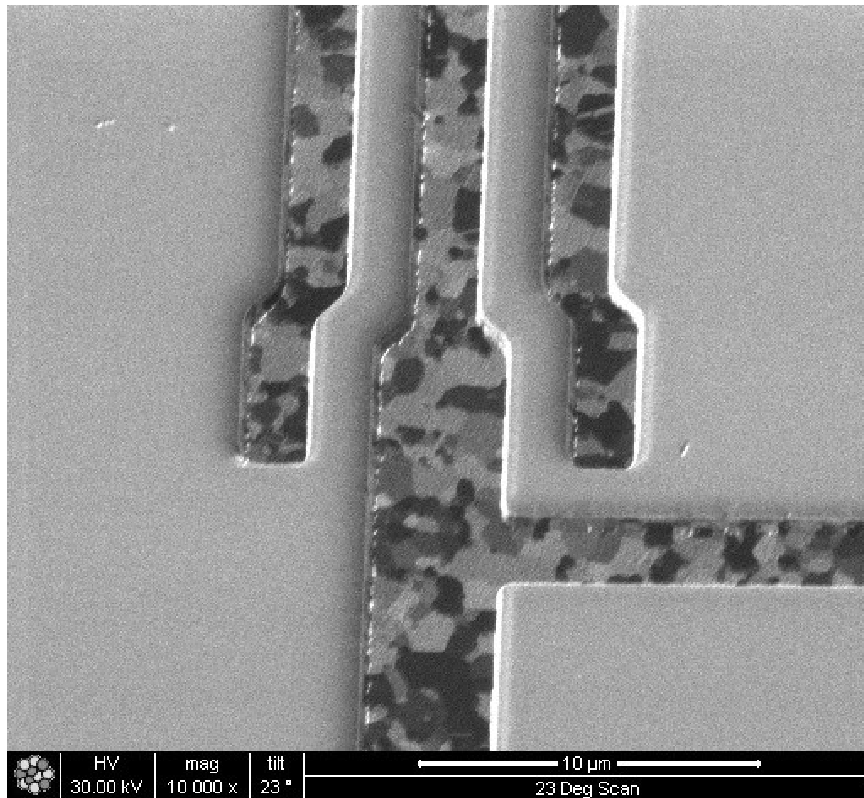


Figure 4.26 Ion-induced SE image of the electroplated Au microstructure.

A lineal intercept method was employed to measure and calculate the average Au grain size following the ASTM Standard E112-10 that outlines standard test methods for determining average grain size.[136] The lineal intercept method is proposed for microstructures that are non-equiaxed grain microstructures such as the Au grains shown in Figure 4.26. This method involves superimposing drawn lines across a micrograph image and performing an actual count of grain boundaries intersecting these drawn test lines to compute the number of intersections per unit length. For acceptable precision, this method recommends that more than 50 intercepts are counted so multiple test lines may be required. Figure 4.27 illustrates the lineal intercept method applied on the planar view of the Au microstructure.

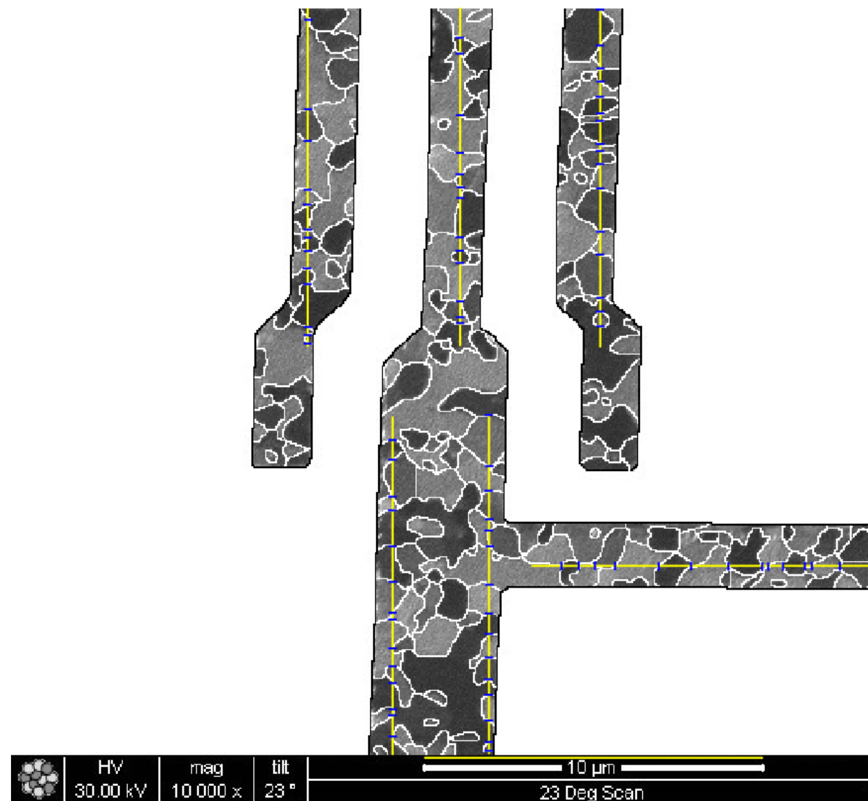


Figure 4.27 Lineal intercept method applied on the Au microstructure.

A total of 6 test lines (five vertical lines measuring 10 μm long and one horizontal line corrected for tilt angle being 10.86 μm long) were drawn on the Au microstructure image shown in Figure 4.27. For each of these test lines the number of grain boundary point intersections (P_i) was counted according to the rules outlined in the ASTM E112-10 standard. Calculation of the number of point intersections per unit length (P_L) is determined by

$$P_L = \frac{\sum P_i}{L_T}, \tag{4.6}$$

where L_T is the true total test line length. Summing up the number of point intersections measured in Figure 4.27, the P_L was determined to be

$$P_L = \frac{96}{60.86\ \mu\text{m}} = 1.58\ \mu\text{m}^{-1} \text{ or } 158\ \text{mm}^{-1}.$$

A grain boundary surface area to volume ratio (S_V) for a single phase is given by

$$S_V = \frac{1}{2}\frac{(\text{Surface Area})}{(\text{Volume})} = \frac{1}{2}\frac{\left(4\pi r^2\right)}{\left(4/3\,\pi r^3\right)} = \frac{3}{(2r)} = 2(P_L). \tag{4.7}$$

Assuming the Au microstructure has an approximately spherical-shaped grain the average grain diameter (D) was calculated as follows

$$D = \frac{3}{S_V} = \frac{3}{2(P_L)} = \frac{3}{2(1.58\ \mu\text{m})} = 0.95\ \mu\text{m}. \tag{4.8}$$

The average Au grain diameter of 0.95 μm is a reasonable value given that the stress line-width is 2 μm and most grains fall within that line-width. Thus, these Au M1 structures do not possess a bamboo microstructure that would prohibit grain boundary diffusion as the predominant electromigration mechanism.

A cross-sectional view of the Au test structure microstructure was prepared with the dual-beam FIB. Figure 4.28 provides a FIB cross-sectional view of the Au test structure microstructure. This image shows that the Au microstructure was not particularly aligned in a strict columnar fashion insofar as most individual grains do not extend the entire thickness of the film. The existence of Au twins sparsely dispersed within the microstructure is noticeable by the straight narrow parallel twin boundaries. Another notable film feature is the slight rolling unevenness of the Au thickness that possesses a very bumpy surface roughness that is mirrored on the surface of the covering silicon nitride passivation.

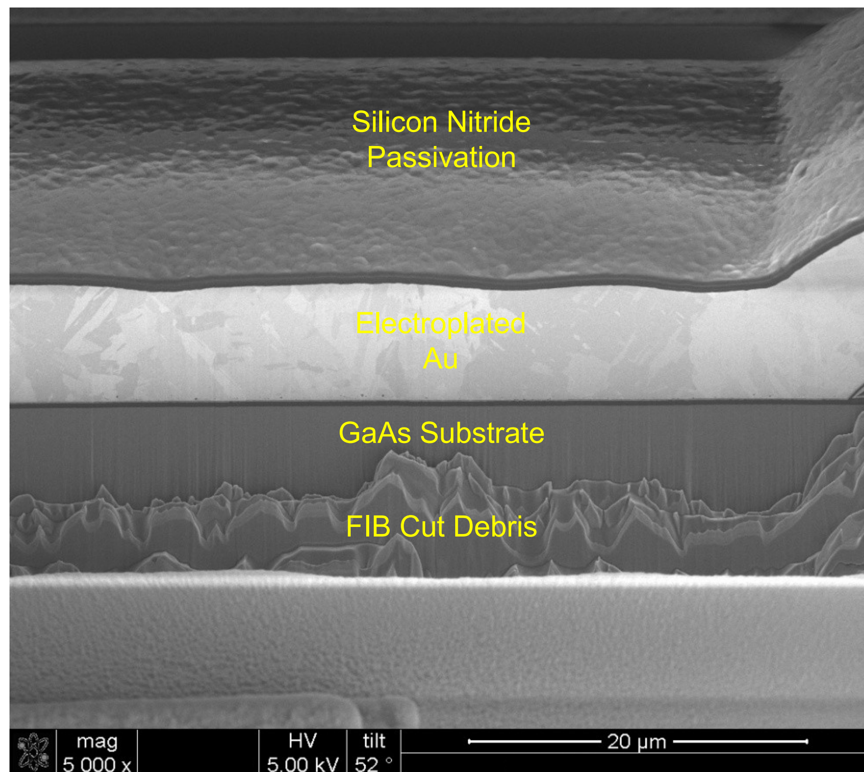


Figure 4.28 FIB cross-sectional view of the Au test structure microstructure.

Upon closer examination of the cross-sectional view of the Au test structure microstructure, it was detected that very small voids were present near the bottom interface of the Au film. A higher magnification FIB image displaying these pre-existing (as-deposited) small voids is shown in Figure 4.29. These microscopic voids were mainly found distributed near the Au seed / electroplated Au interface, but in some cases voids were also isolated in the middle of the film. Void diameters varied widely from approximately 100 Å to 1000 Å. Creation of microscopic voids arises from an array of mechanisms, but gas bubble entrapment has been known to occur in electroplated films.[137] Impurity inclusions such as polymer residue from the photo-resist have also caused some of the voids observed in these electroplated Au films.

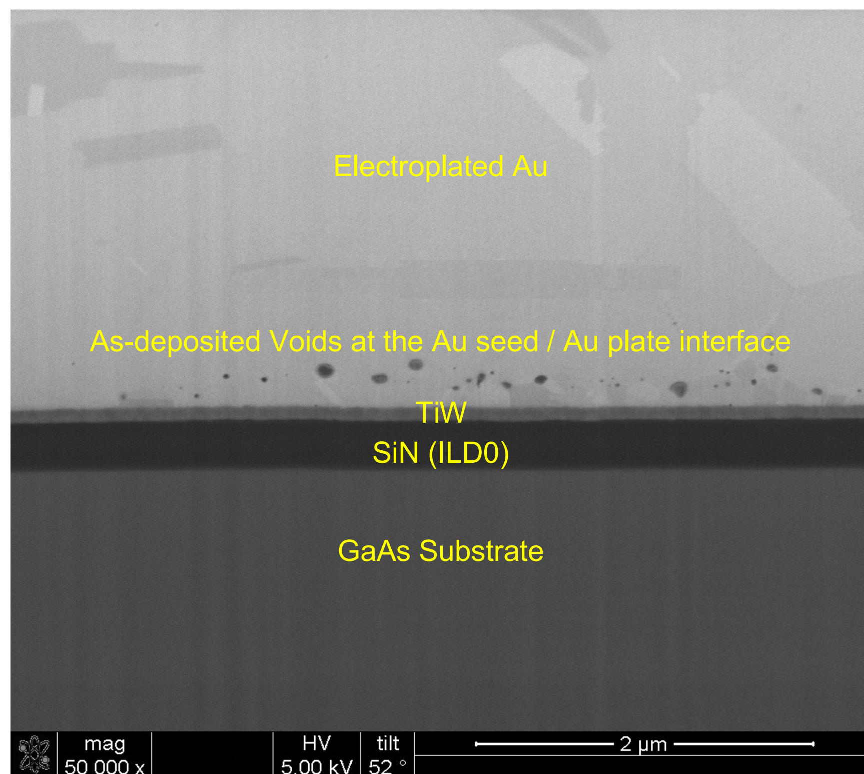


Figure 4.29 As-deposited voids in the electroplated Au film.

4.7.2 Gold Chemical Analysis

Chemical analysis of the electroplated Au films in this study was conducted to characterize the purity of the deposited Au layer. Commercial Au electrodeposition utilizes gold (I) sulfite plating baths that contain thallium (Tl) brightener complexing additives to decrease film stress and hardness as well as reduce sulfur (S) content in the deposit.[138, 139] A few analytical techniques have detection limits below 100 parts-per-million (ppm) that are suitable to accurately measure the trace amounts of co-deposited ions in these electroplated Au films. Inductively Coupled Plasma Optical Emission Spectroscopy (ICP-OES) can quantitatively measure very low elemental concentrations within a thin film.

A section of an electroplated Au film on a GaAs wafer measuring 211 cm^2 in area with a Au thickness of 1.9 μm was dissolved in a mixture of hydrochloric acid and nitric acid ($HCl + HNO_3$). The dissolved gold solution was analyzed by ICP-OES for trace sulfur and thallium ions but neither element was detected. Detection limits of 50 ppm for Tl and 5 ppm for S ions were calculated based on a gold density of 19.3 g/cm^3. Table 4.4 lists the ICP-OES analysis results on the electroplated Au film content. Since the trace elements commonly found in electroplated Au are below the ICP-OES detection limits, this high purity Au film eliminates the possibility of any confounding ionic electromigration effects.

Table 4.4 ICP-OES analysis for trace elements within electroplated Au film.

Element	Concentration	Detection Limit
Thallium	Not detected	< 50 ppm
Sulfur	Not detected	< 5 ppm

4.8 Failure Analysis

Failure analysis was pursued to characterize the electromigration-induced void morphology within the Au interconnect test structures. In addition, determining failure site locations provides insight into the direction of atomic mass transport. For this study, the Au M1 test structure had the applied electrical current configuration shown in Figure 4.30, wherein the electron current flows from the cathode (negative) towards the anode (positive).

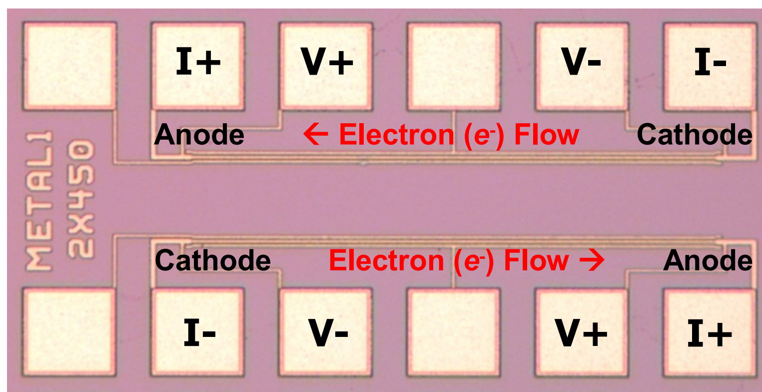


Figure 4.30 Electron current flow direction on the Au M1 structures.

Based on this configuration, it is expected that electromigration-induced voids will develop near the cathode end of the Au structure in accordance with the electron wind force. A few exceptions to this specific void location could be possible if there were pre-existing voids in the Au line structure or if the microstructure varied from bamboo to polycrystalline away from the cathode region. This first scenario is much more plausible given that pre-existing voids have been detected in these electroplated Au test structures. However, the diffusion of Au atoms occurring in the pre-existing void region should still be in the direction of the electron flow that is directed from the cathode to the anode.

After completion of an electromigration test, all DUTs were carefully inserted into electro-static discharge (ESD) protective foam within a sealed case for archival purposes. The considerable cost and labor intensive nature of failure analysis process techniques permitted only a select few DUTs to be evaluated. DUT selection was based on electromigration failure times identified as either early, middle, or late times from within the failure distribution. Samples for failure analysis were initially examined by a Nikon confocal optical microscope to pinpoint potential failure locations for subsequent FIB cross-sectioning.

Failure analysis was first carried out on the Au M1 test structure that failed early to determine the underlying root cause. In experimental phase III, the Au M1 structure (DUT #35) had the earliest failure time of 45.85 hours from within the 337°C electromigration lifetime distribution shown in Figure 4.31.

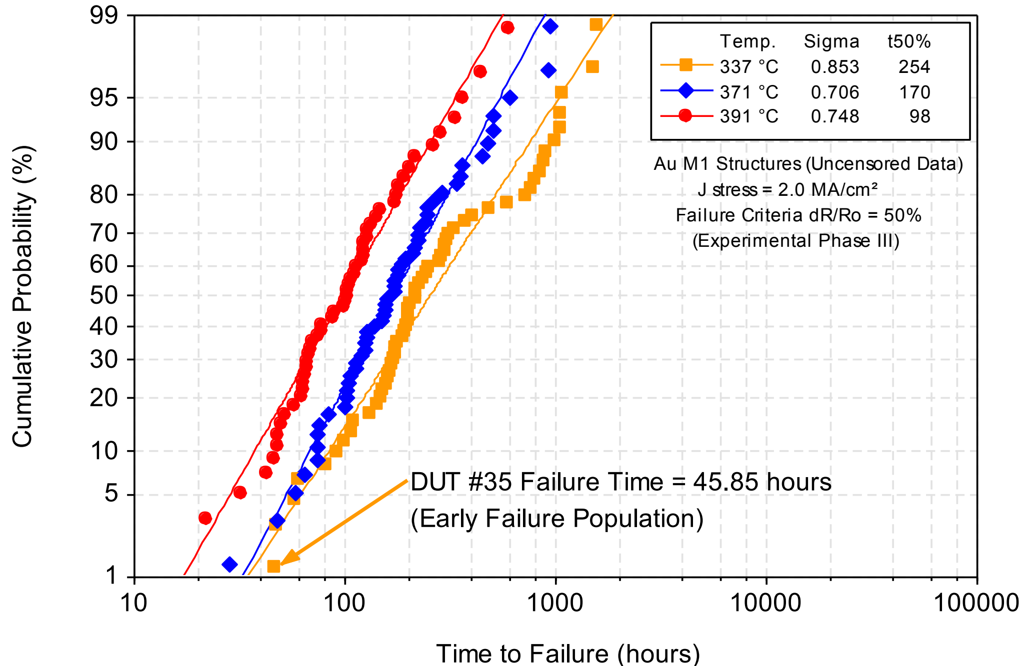


Figure 4.31 Uncensored failure time data for the Au M1 structures (phase III).

The uncensored data in Figure 4.31 distinctly shows the early electromigration failure time populations (about 10%) that are overlapping one another irrespective of the acceleration due to the temperatures at 337°C and 371°C. Since the silicon nitride passivation coating is optically transparent, the Au M1 structure is clearly visible for immediate optical inspection of electromigration-induced damage locations. Optical inspection of DUT #35 detected a half-circle darkened area near the anode end of the Au M1 structure. Figure 4.32 is the optical image showing the half-circle shaped void location near the anode end of the early failure Au M1 structure.

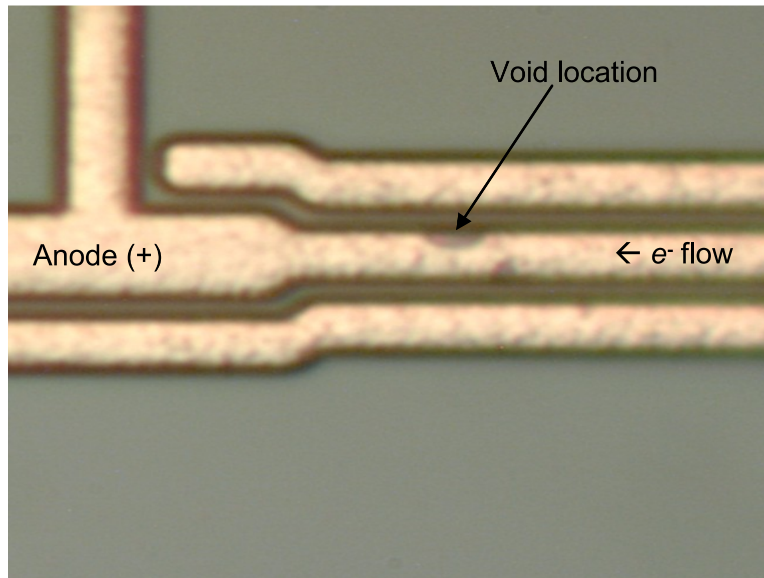


Figure 4.32 Optical image of the early failure void location.

A void nucleating near the anode end is highly improbable since the funneled electron flow entering near the cathode would generate voids in that Au polycrystalline region. In addition, the Au M1 structure length of 450 μm is sufficient for the Au polycrystalline microstructure to have grain boundary triple points much closer to the cathode for void nucleation.

It is for these ascribed reasons and the early failure time of the Au M1 structure (DUT #35) that its void location warranted further failure analysis. A parallel cut along the Au line and into the void location was made by the FIB. Figure 4.33 displays the cross-sectional SEM micrograph of the void cavity found on the Au M1 structure that failed early at 337°C in experimental phase III. Upon examination, the volume of the void was found to be too extensive for the measured resistance change of 50%. As designed, the monitoring equipment prevented the void cavity from breaching the entire Au structure line-width wherein catastrophic failure damage impedes accurate failure analysis of electromigration-induced void evolution. Morphology of the void also suggests void growth evolved from the bottom interface of the Au film where as-deposited voids have been noticed. Based on these observations, it is highly probable that pre-existing voids in the electroplated Au film near the anode accelerated this oversized void formation producing the early failure time of the Au M1 structure.

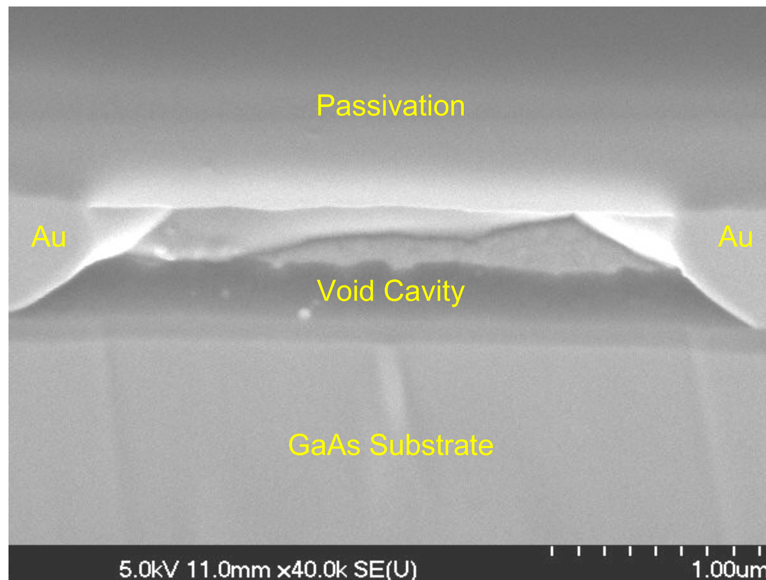


Figure 4.33 SEM cross-sectional view of the early failure void.

When distinct early failure populations (extrinsic failures) are physically verified as pre-existing defects, then it is permissible to censor them from the intrinsic failure population. In doing so, the cumulative failure distribution transforms from a bi-modal to a mono-modal statistical distribution with a much tighter standard deviation. Thus, the early failure populations in Figure 4.31 were subsequently censored based on the detected anomalous failure location and physical characterization highlighting an enormous void that signifies pre-existing voids were the root cause of the premature failures.

Failure analysis of a typical electromigration failure observed on the Au M1 structure (DUT #22) with an intermediate failure time of 491 hours in experimental phase V was conducted. This Au M1 structure (DUT #22) was positioned within the intrinsic electromigration failure distribution. An optical micrograph taken at 200X magnification identifies a darkened region on the Au M1 structure where both a void and hillock formation (Au extrusion) are located near the cathode end shown in Figure 4.34.

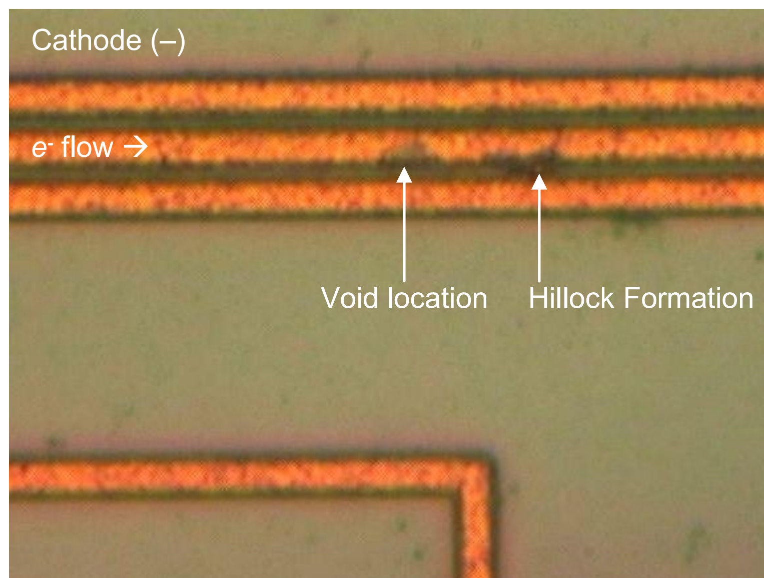


Figure 4.34 Optical image of a typical Au M1 electromigration failure void.

Void formation occurring near the cathode end of the Au M1 structure is the expected electromigration failure mode that is consistent with the electron wind funneling out of the cathode current tap. Figure 4.35 is a SEM image of a FIB cut into the void region of this typical Au M1 electromigration failure.

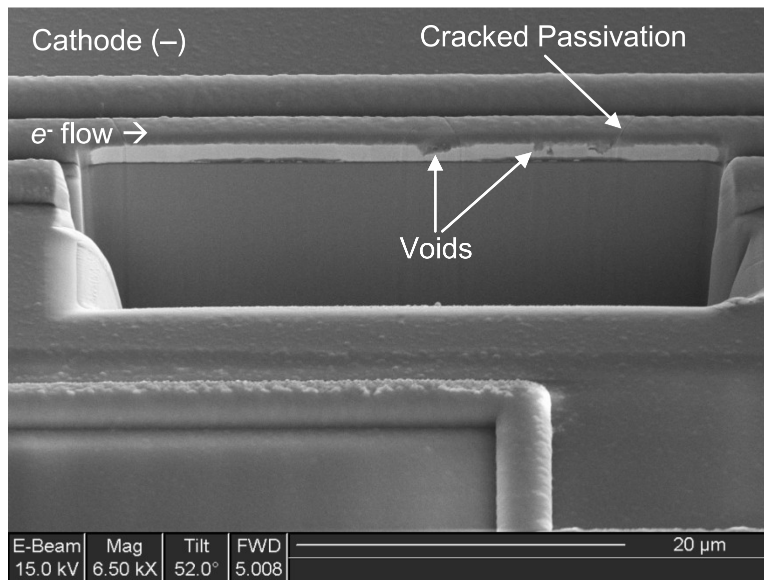


Figure 4.35 SEM image of typical Au electromigration-induced voids.

This SEM micrograph shows smaller size voids that are not breaching the entire Au line thickness as was discerned with the void displayed in Figure 4.33. Another significant characteristic is that these voids formed near the top of the Au film layer where pre-existing voids have not been found. With the absence of pre-existing void defectivity in the Au film, it is concluded that the nucleation of these voids initiated at grain boundary triple points due to flux divergence. This corresponds to the normal diffusion wear-out mechanism for electromigration of polycrystalline metal films. Moreover, the Au mass transfer is shown to be in the electron flow direction since Au hillocks were noticed downstream of these voids.

Hillocks form as a result of Au mass transfer convergence that builds up pressure which causes fractures in the glass passivation whereby Au extrusions are deposited. Figure 4.36 displays a FIB cross-section of a large Au hillock that is located several microns away from the previously described electromigration-induced voids.

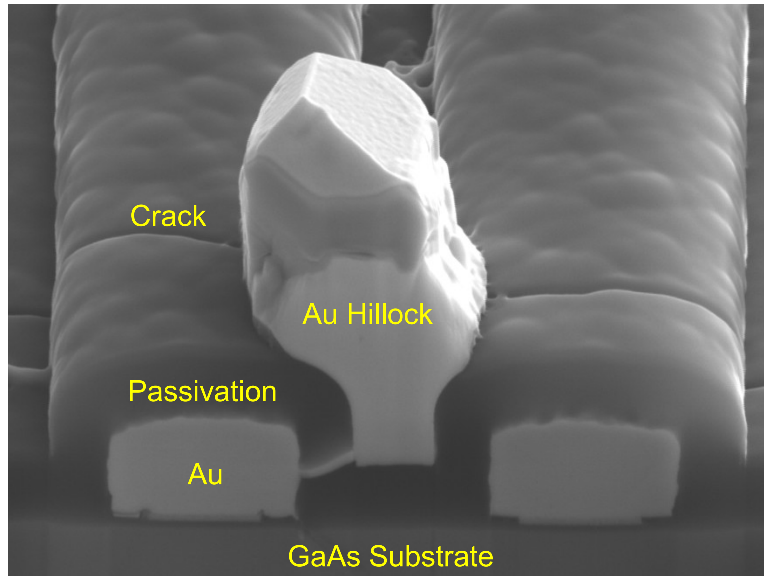


Figure 4.36 SEM image of a large Au hillock formation.

The thick silicon nitride passivation acts to confine hillock formation and hence inhibit electromigration process. However, once the electromigration-induced film stresses build up enough to cause the passivation to fracture, hillocks can readily be extruded forming a lower stress mass transfer pathway for the electromigration process. The Au mass from several tiny voids is migrated along grain boundaries to a region of flux convergence into one large hillock as shown above. It should be noted that the law of conservation of mass is maintained with these electromigration-induced voids and hillock formations.

CHAPTER 5 DISCUSSION AND ANALYSIS

In this chapter, discussion and analysis of the main experimental results in this research are expounded. Analysis of resistance variation among the Au test structures are examined in connection with different test structure designs. Resistance degradation characteristics during electromigration testing are discussed in regard to the resistance change failure criterion percentage and its associated electromigration lifetimes. A physical mechanism linked to process induced defects is proposed for early lifetime failures. The electromigration activation energy extracted for Au interconnects is assessed in relation to relevant literature values as well as the underlying diffusion mechanism. In the final section, the predominant electromigration failure mechanism responsible for the measured current density exponent for the Au structures is evaluated.

5.1 Structure Resistance Variation

In experimental phases (I and II), the Au interconnect M1 test structures were designed based on NIST recommendations to be 800 μm long. These long Au structures measured a very broad resistance range (4 to 12 ohms) with a standard deviation of 1.6 ohms. The variability in the Au structure resistance is due to poor film thickness uniformity along the structure length that is inherent to Au electroplating. All Au structures with outlier resistances were screened to avoid structures with measurably different film temperatures causing adverse spreads in the electromigration lifetime distributions. In experimental phase II, the resistance standard deviation was reduced to 0.74 ohms by screening Au M1 structures to ± 1 standard deviation of the initial resistance mean.

In experimental phases (III – V), a desire to conduct electromigration experiments on Au test structures with even lower resistance variability and to eliminate artificial screening of Au structures prompted a redesign for a shorter Au test structure. This redesigned Au test structure had the same line-width and film thickness, but the line-length was shortened to 450 μm from 800 μm to reduce resistance variation. Phase V Au M1 test structures had a significantly lower resistance standard deviation of 0.54 ohms compared with the phase II Au M1 test structure resistance standard deviation of 1.6 ohms. The higher standard deviation for phase II Au M1 structures may be a result of the higher resistance mean of 8.65 ohms. Thus, for a direct comparison of both Au M1 structures, the resistances need to be normalized per unit length. Dividing the phase II Au M1 structure resistances by the 800 μm (0.08 cm) length yields the normalized resistance distribution shown in Figure 5.1.

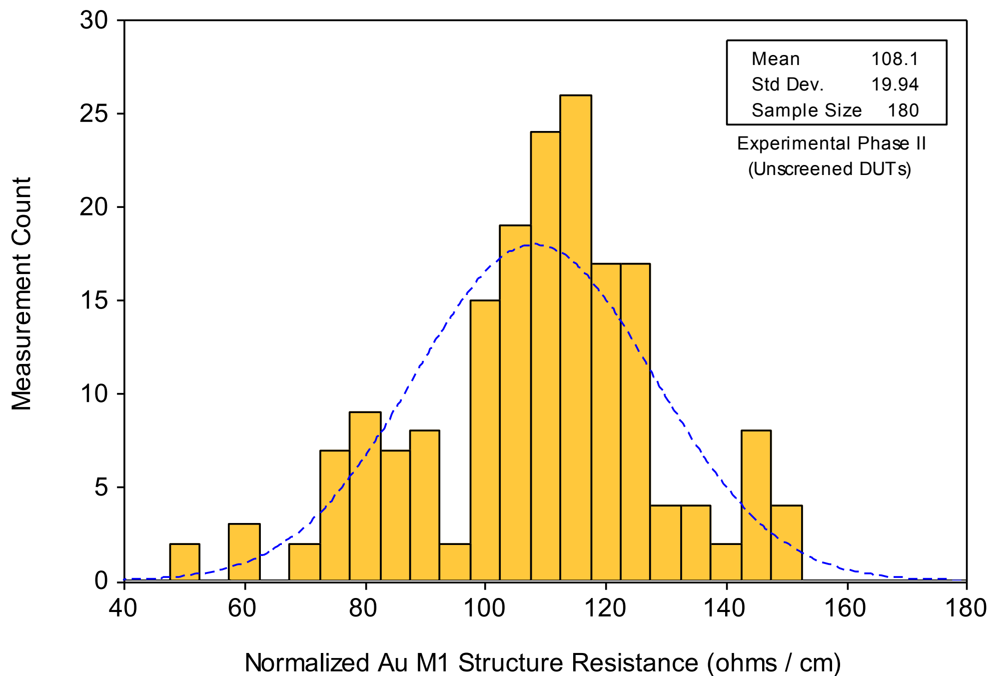


Figure 5.1 Normalized Au M1 test structure resistance distribution (phase II).

Figure 5.2 displays the normalized (per length) resistance distribution for the phase V Au M1 structures. Table 5.1 compares the mean and standard deviation for initial and normalized resistances for the Au M1 test structures in experimental phase II and phase V. The normalized resistance standard deviation is still lower for phase V Au M1 structures by 40% even with a higher normalized mean, perhaps indicating that the electroplating Au thickness uniformity was improved for these test structures.

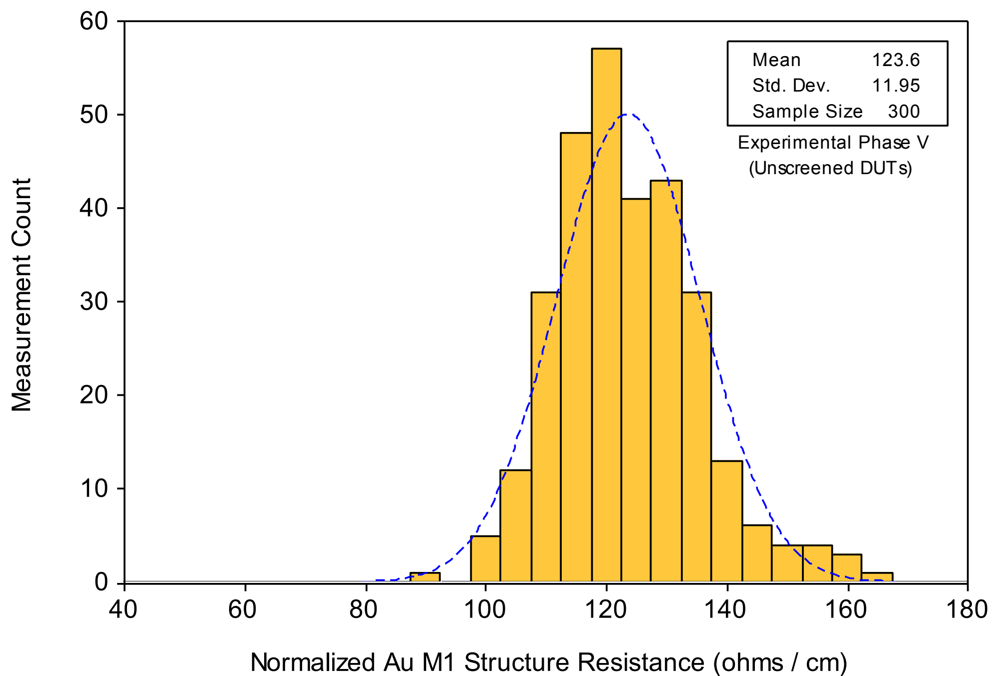


Figure 5.2 Normalized Au M1 test structure resistance distribution (phase V).

Table 5.1 Normalized Au M1 structure resistance mean and standard deviation.

Test Structure (Phase #)	Initial Resistance		Normalized Resistance	
	Mean (ohms)	Standard Deviation (ohms)	Mean (ohms / cm)	Standard Deviation (ohms / cm)
Au M1 (Phase II)	8.65	1.60	108.1	19.94
Au M1 (Phase V)	5.56	0.74	123.6	11.95

Even with the considerable improvement in resistance standard deviation for phase V Au M1 structures, the potential influence of resistance variability on the electromigration lifetimes of these Au structures was examined. A scatter plot of the initial Au M1 structure resistance versus the electromigration lifetime in experimental phase V is shown in Figure 5.3.

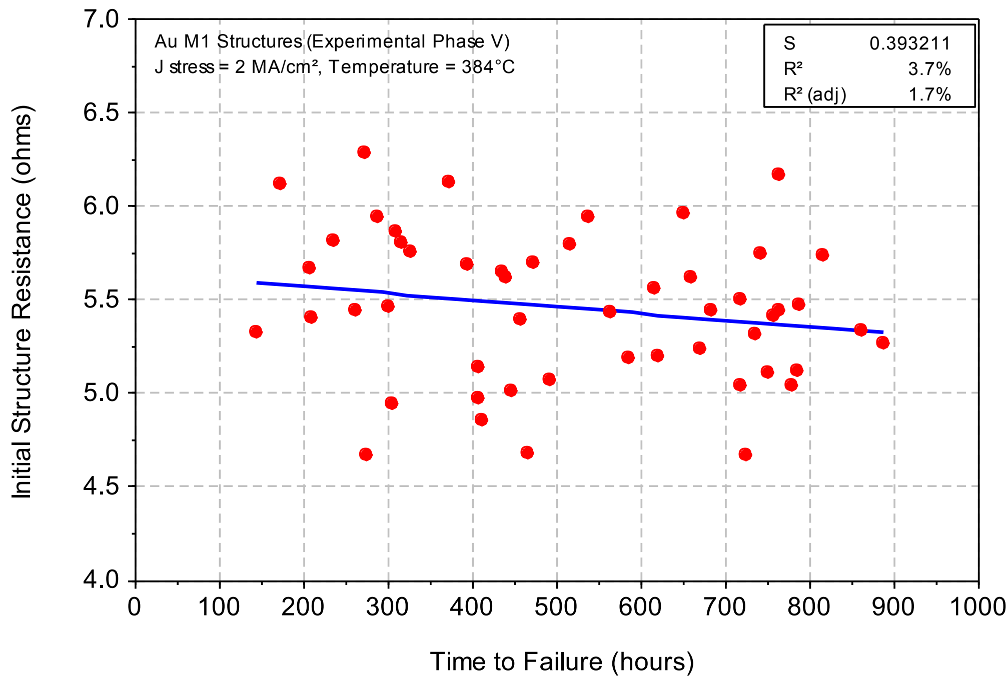


Figure 5.3 Initial Au M1 structure resistance versus electromigration lifetime.

A linear regression fit of the data produced a very low R^2 of 3.7% indicating essentially a non-correlation between initial structure resistance and electromigration lifetime. Thus, it is concluded that initial structure resistance variation does not influence electromigration lifetime. This is an important conclusion because electromigration lifetimes are strongly dependent on stress conditions and microstructural features, not initial structure resistance variability.

5.2 Resistance Degradation Characteristics

Electromigration reliability studies currently employ the resistometric method as the industry standard in the assessment of the operational lifetime of embedded metal interconnects. The resistometric method is advantageous for examining the initial stages of the electromigration where current density and temperature are roughly constant in the metal interconnect test structures. These high-resolution resistance measurements are very sensitive in detecting initial void formation and growth during electromigration testing. Most importantly, the resistometric method facilitates evaluation of actual passivated covered metal interconnects, the same as those embedded in IC devices.

A high-resolution resistometric method was utilized in this investigation for all electromigration tests, where the resistance of the Au interconnect test structures were continuously measured as a function of time. In this method, selection of a low resistance degradation percentage failure criterion ($\Delta R/R_o$) avoids catastrophic open circuit failures that are problematic in electromigration lifetime tests, where runaway current density and Joule heating are allowed. A resistance degradation failure criterion ($\Delta R/R_o$) of 10% for electromigration tests is a conservative guideline designated in the semiconductor industry. For most operational conditions, a 10% resistance increase in a given metal interconnect is tolerable in that the overall IC device is still functional. As interconnect resistance increases beyond a 100% $\Delta R/R_o$ degradation, the functional performance of most ICs is substantially diminished. Beyond this degradation level, the electromigration-induced void rapidly grows as the current density and Joule heating exponentially increase, leading to a catastrophic open interconnect circuit failure.

In the first two experimental phases (I and II), the conventional resistance degradation failure criterion ($\Delta R/R_o$) of 10% was explored for electromigration in Au interconnects. This failure criterion resulted in a pronounced bi-modal electromigration failure distribution with a significant early failure population. Figure 5.4 displays a cumulative probability graph containing bi-modal electromigration failure distributions with a 10% failure criterion.

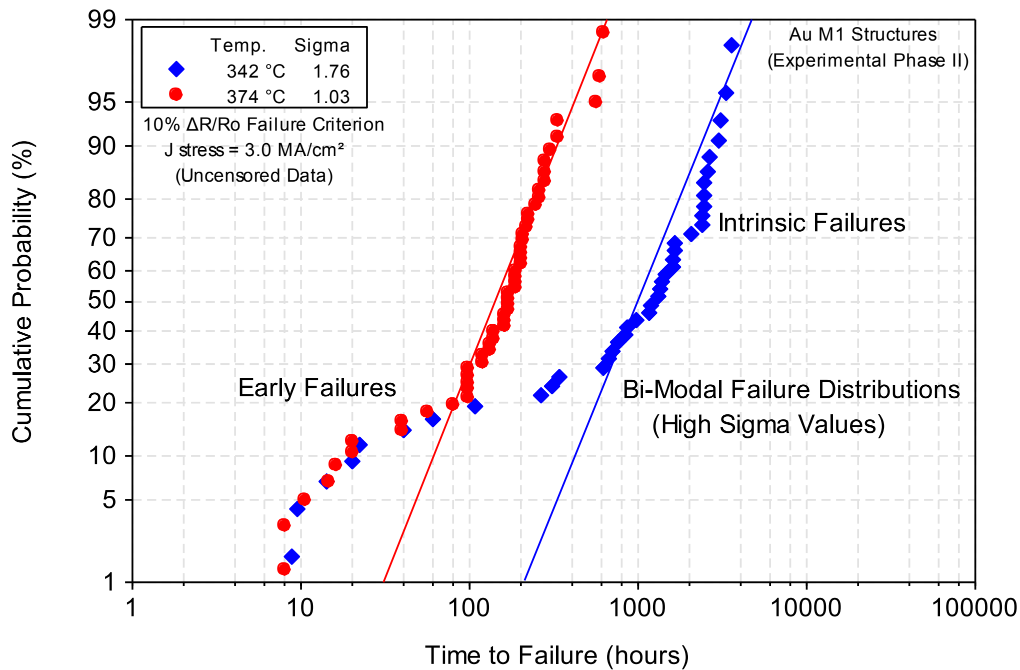


Figure 5.4 Au electromigration failure distributions with a 10% failure criterion.

Because these electromigration failure distributions possess high sigma values, it was evident the Au M1 structures exhibited two distinct failure modes with early failures deviating from the log-normal fit. It was initially assumed that the broad resistance variability of these longer Au M1 structures in experimental phases (I and II) was responsible for the bi-modal failure distributions. However, no statistical correlation with initial resistance was found as shown in Figure 5.3.

In examination of the Au M1 structure resistance traces under electromigration stress test conditions, unusual characteristics were observed. Figure 5.5 displays a few Au M1 structure resistance traces for an electromigration test at a temperature of 359°C and current density of 2 MA/cm^2.

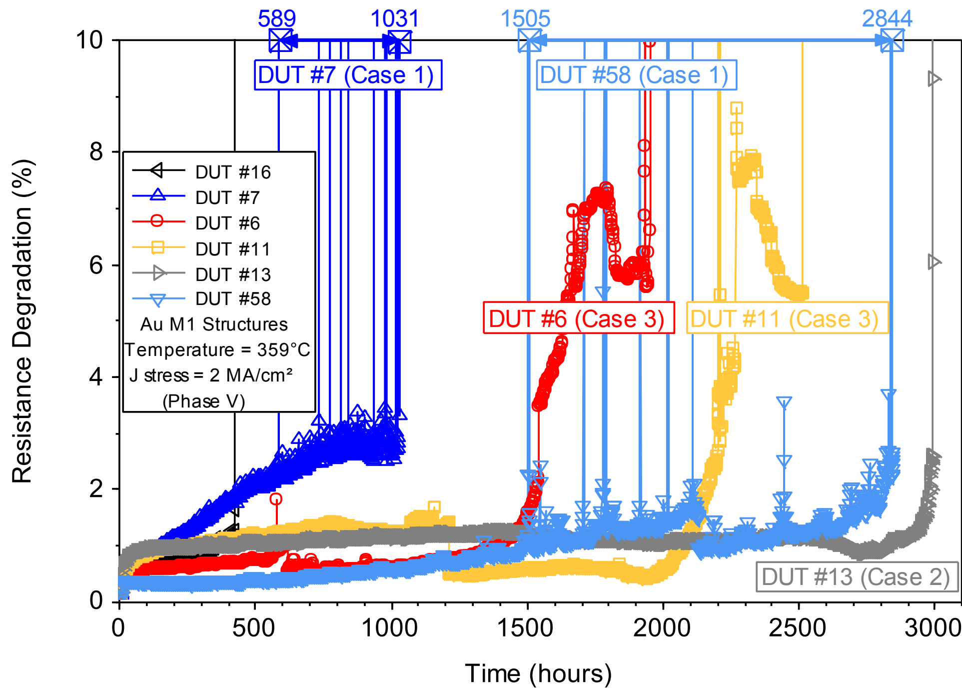


Figure 5.5 Au M1 structure resistance traces scaled on a 10% $\Delta R/R_o$ graph.

Most peculiar are resistance traces that possess multiple resistance spikes as observed with DUT #7 and DUT #58, which are denoted as case 1 characteristic. For a resistance degradation failure criterion of 10%, these resistance spikes result in much earlier failure times. For DUT #7, a premature failure time of 589 hours is encountered with a 10% failure criterion instead of an extended lifetime of 1031 hours with a 50% failure criterion. This translates into a lifetime difference of 442 hours. Thus, imposing a 10% failure criterion culminates these resistance spikes as early failures and produces bi-modal failure distributions.

In order to effectively characterize the resistance traces and electromigration lifetimes of Au interconnects, it was necessary to increase the resistance degradation criterion to 50% $\Delta R/R_o$. This increased resistance degradation of 50% was utilized in the last three experimental phases (III – V). Two key benefits resulted from this adjustment. First and most importantly, the early failure population of the Au electromigration failure distributions almost entirely disappeared, leaving an intrinsic log-normal failure distribution with much lower sigma values. The rationale for this diminished early failure population is explained by the Au M1 structure (DUT #7) resistance spikes recovering several times from a greater than 10% resistance change before ultimately reaching an extended lifetime with a 50% failure criterion. Secondly, the benefit of the 50% failure criterion was realized in the optical detection of void formations within the Au interconnect structures. These electromigration-induced voids grow marginally larger with this increased failure criterion and thus are easier to locate along the Au interconnect structures.

Although the 50% failure criterion diminished the early failure population, investigation into the underlying physical mechanism for the Au structure resistance spikes (case 1 characteristic) is of great importance. Resistance degradation (increase) during electromigration testing is known to be caused by geometrical changes in the interconnect microstructure. The onset of gradual resistance degradation coincides with the nucleation and formation of voids, whereas a rapid resistance increase indicates exponential growth of a single void or possibly a sudden coalescence of existing voids. At first, the Au resistance spikes were puzzling[140] but through ruling out measurement errors it was recognized these resistance spikes were related to microstructural changes.

Resistance spikes are rarely reported in the literature, but after widespread use of the resistometric method a few cases of resistance spikes during electromigration testing have been reported. Short duration resistance spikes during electromigration stressing were previously observed for sputter deposited Al alloyed thin film interconnects.[141, 142] These Al resistance spikes varied randomly in time and magnitude, with the overall interconnect lifetime primarily dependent on the ability to heal from the spikes. Figure 5.6 is the reproduced voltage versus time chart during electromigration testing wherein voltage ($\propto$ resistance) spikes were detected for an Al-Si(1%) interconnect.[141]

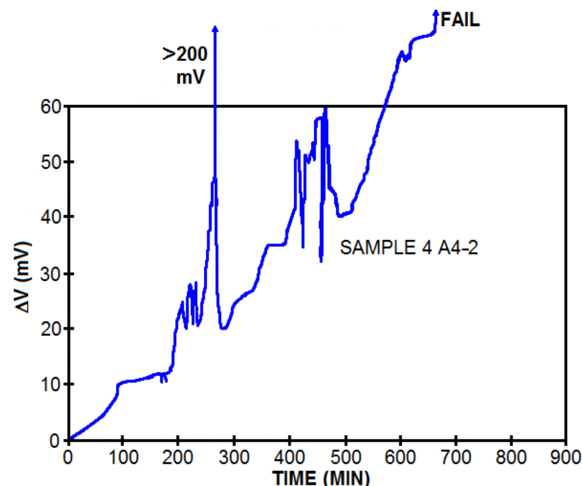


Figure 5.6 Voltage (resistance) spikes for Al during electromigration testing.[141]

These resistance spikes were explained as a sudden narrow void formation nearly breaching the Al stripe that caused the localized temperature to increase. This in turn may cause metal expansion to re-seal (heal) the void and as a result the resistance decreased. Direct evidence of a physical mechanism for Al resistance spikes was sought by electromigration tests inside a high voltage SEM.[142] These in-situ periodic SEM images revealed that voids nearly

breaching the Al stripe dynamically changed shape or healed and were responsible for the resistance spike characteristic. It was also concluded that abrupt resistance change depends more critically on void shape than on void volume.

Electromigration in dual-damascene electroplated Cu interconnects shows similar resistance spike characteristics.[143-145] For Cu interconnects a gradual linear increase in resistance is observed as electromigration commences with the formation of tiny voids. As electromigration progresses, the gradual increase in resistance is followed either by an abrupt terminating resistance change (final failure) or proceeds with recovery of several temporary resistance spikes that ultimately terminate into final failure. Figure 5.7 shows the two types of resistance characteristics (A and B) displayed during electromigration testing of dual-damascene Cu interconnects.[145]

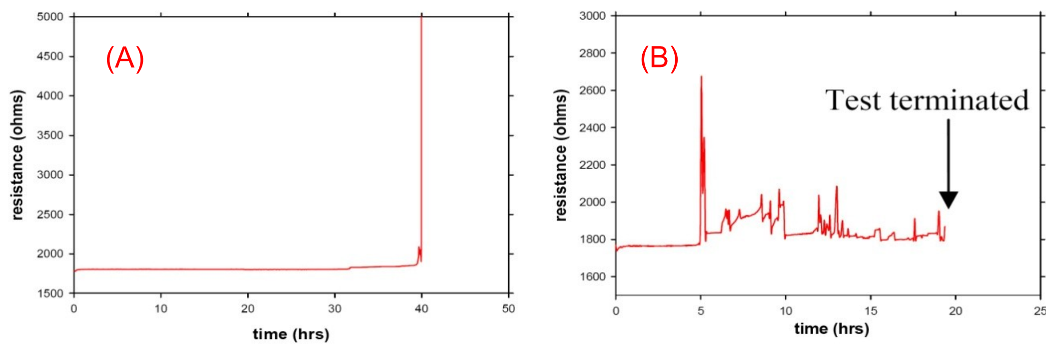


Figure 5.7 Electromigration resistance characteristics of Cu interconnects.[145]

Failure analysis of type (A) resistance trace found a critical sized void in the Cu line between the via top and dielectric cap layer. In contrast, for type (B) resistance trace the void growth initiated in the Cu via bottom, where resistance fluctuation and recovery stemmed from voiding and healing processes.[145]

In summation, both the Al and Cu interconnect resistance spike characteristics resemble the resistance spikes detected for the electroplated Au interconnects in this investigation. Overall, this resistance spike characteristic is limited to a relatively small percentage (< 10%) of the total Au interconnects tested. As revealed by in-situ SEM imaging, the recovery (healing) of resistance spikes is due to voids nearly breaching the interconnect and then rapidly changing shape to be more conducive to electron flow. Yet the exact origin of the precipitous resistance spike characteristic is not fully comprehended. The limited occurrence suggests that process-induced defects are the underlying cause for resistance spikes culminating in early electromigration failures. Defects impacting the integrity of the TaN barrier liner in dual-damascene Cu may hasten voids originating in the via bottom. As for critically sized voids found in the interconnect line, coalescence of as-deposited voids in the electroplated Cu accelerates resistance increase leading to early electromigration failures.

In this study on Au interconnects, it was substantiated that as-deposited voids (approximately 0.1 μm diameter) were dispersed along the sputtered seed and electroplated Au interface shown in Figure 5.8. Furthermore, examination of Au M1 structure (DUT #35) in experimental phase III with an early failure time of 46 hours revealed a large void on the anode end of the Au M1 structure shown in Figure 5.9. This early void is located on the opposite end from where electromigration-induced voids are expected to form, due to the increased electron wind funneled at the cathode end. Examination of other Au M1 structures with intermediate electromigration failure times showed the void location near the expected cathode end. A parallel FIB cut into this early void location found an extensive void cavity volume as displayed in Figure 5.10.

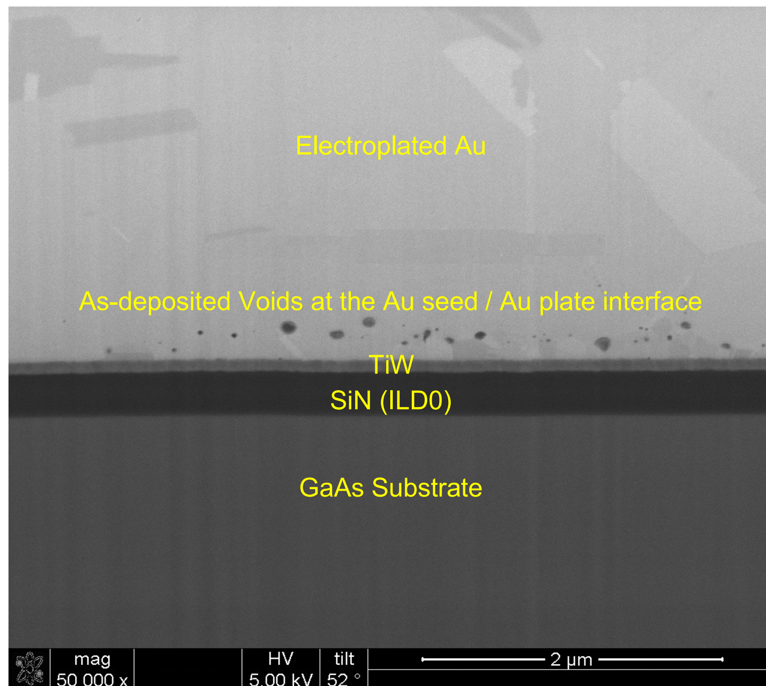


Figure 5.8 As-deposited voids in the electroplated Au film.

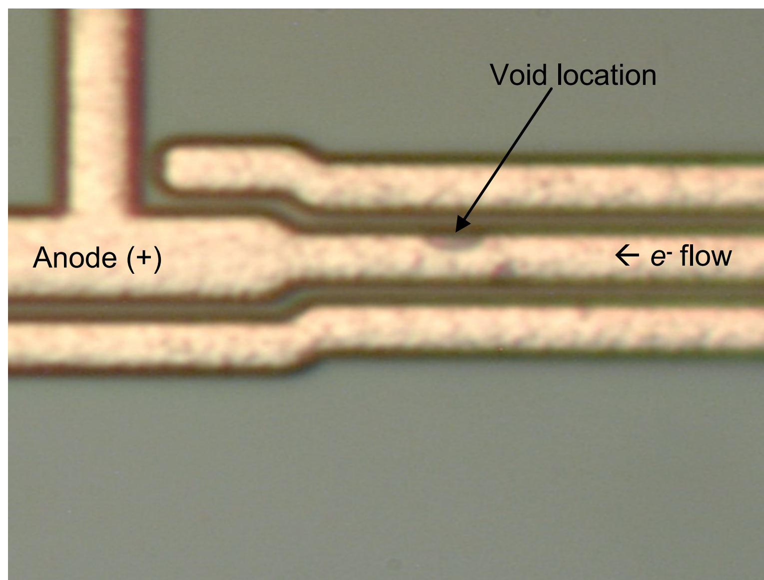


Figure 5.9 Au M1 structure early failure void location at the anode end.

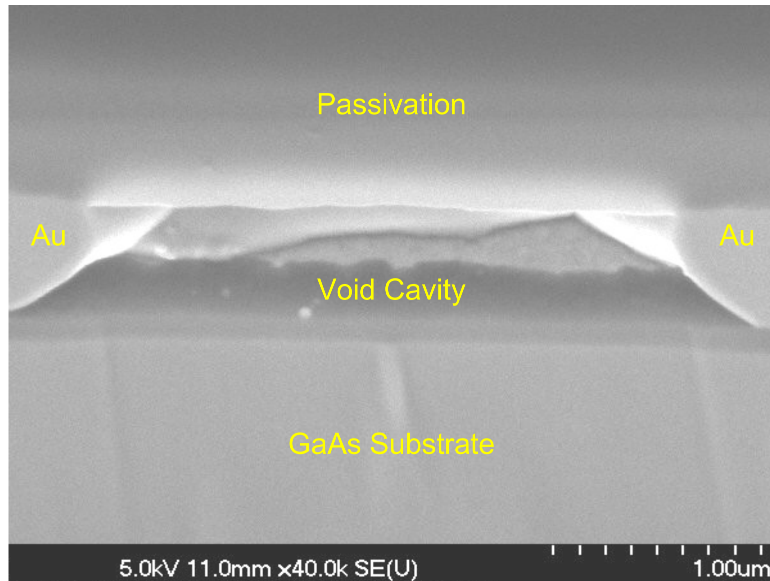


Figure 5.10 SEM cross-sectional view of Au M1 structure early failure void.

On close inspection of this micrograph, it is confirmed that the void cavity volume is larger than expected for the measured resistance change of 50%, especially if voids were not initially present prior to testing. For Au M1 structures that did not experience early failure times, the electromigration-induced voids were located at the cathode end and were considerably smaller, not depleting the entire thickness of the film as shown in Figure 5.10. Additionally, the void morphology of early failure indicates that the void formation evolved along the bottom Au interface where the pre-existing voids were detected. Based on all these void features (location, size, and morphology), it is concluded that pre-existing voids coalesced near the anode to accelerate this early electromigration failure. In conclusion, coalescence of as-deposited voids is considered to be the physical mechanism responsible for the precipitous resistance spike characteristic and the resulting early electromigration failures.

5.3 Electromigration Activation Energy

Electromigration experiments are accelerated by stress conditions to obtain failure time data in practical timeframes (< 6 weeks) necessary to extract Black's model parameters (E_a and n) for prediction of metal interconnect lifetimes. Since electromigration wear-out of interconnects follows this Arrhenius based model, the lifetime of interconnects is exponentially dependent on metal film temperature. Thus, electromigration experiments are conducted at elevated temperatures, wherein temperature is the main accelerating stress condition. The acceleration factor due to temperature (AF_T) is determined by

$$AF_T = \frac{\exp\left(E_a / kT_{\text{use}}\right)}{\exp\left(E_a / kT_{\text{stress}}\right)} = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{stress}}}\right)\right], \qquad (5.1)$$

where T_{use} is the operational use temperature and T_{stress} is the electromigration test temperature. Most IC interconnects operate at ambient temperatures between 85°C and 130°C depending on product applications. Consumer products operate under lower temperatures, whereas automotive products are exposed to higher use temperatures since these ICs are mounted near engines.

In this study on passivated electroplated Au interconnects, it was necessary to elevate the stress temperature above 300°C with an average stress temperature of 350°C. A temperature acceleration factor on the order of 10^5 for these Au electromigration experiments was calculated based on an operational temperature of 85°C and the average stress temperature with assumed activation energy of 0.8 eV. Since electromigration lifetimes are exponentially dependent on activation energy, it is extremely important to determine accurate model parameters for extrapolation. Hence, a major focus was on accurate extraction of activation energy and Au film temperatures under stress conditions.

Electromigration experiments are also accelerated by high currents that induce Joule heating, thereby increasing the metal interconnect film temperature above oven stress temperature. Unfortunately, too often several electromigration studies employed current densities in excess of 3 MA/cm^2 that led to inaccurate accounting of the Joule-heated film temperatures. Significant error in both activation energy extraction and predicted electromigration lifetime results when Au film temperature has not been precisely determined. To make matters worse, electromigration studies on non-passivated Au films with these high current densities experience much higher Joule heating due to less thermal dissipation. In addition, the exposed Au film surface in these studies provides a lower energy pathway for electromigration that is not realistic of actual passivated interconnects embedded in ICs.

In this investigation, the previously ascribed undesirable conditions were eliminated by application of a lower current density ($\leq$ 2MA/cm^2) on thick silicon nitride passivated Au interconnects. The silicon nitride passivation overcoating the Au film promotes thermal conduction and temperature uniformity compared to non-passivated Au films. Moreover, Au film temperatures for each independent interconnect structure were calculated using accurately extracted temperature coefficient of resistance (TCR) values measured at four or more temperatures, including the electromigration stress oven temperature. Furthermore, confinement of the current density to 2 MA/cm^2 prevented Au film temperatures from exceeding more than 10°C above the oven temperature. This very low Joule heating enhances overall accuracy of the Au interconnect film temperature determination because excessive temperature gradients are not present and accounting for them would be much more difficult.

Another source of inaccuracy in the extraction of activation energy stems from the method used for electromigration lifetime measurements. For example, the lifetime method measures the failure time when the open circuit condition is reached where a catastrophic void ruptures the entire metal interconnect. As a metal interconnect approaches open circuit, the metal film temperature rapidly rises to the melting point where the metal line fuses. As a result, metal film temperatures are not kept constant and the rate of electromigration varies, making the extraction of activation energy highly questionable. The best method to avoid the thermal runaway problem is to monitor and measure the initial void growth stages of electromigration long before reaching an open circuit failure. A key benefit of this method is that the interconnect film temperature is essentially constant during the initial stages of electromigration.

Therefore, in this study a high-resolution resistometric method was utilized to precisely measure electromigration lifetimes of Au M1 interconnect structures for a 50% resistance change failure criterion. The Au M1 structures were stressed over the widest possible temperature range with four oven temperatures to improve the statistics for activation energy extraction. A deficiency in sample size (< 30) for individual stress temperatures is noticed for other industry reliability studies on Au interconnects. Thus, in this study a total of 60 Au M1 structures for each temperature were stressed to increase statistical confidence in the median failure time ($t_{50\%}$). Another major advantage over these previous studies is that the primary stress acceleration was provided by the oven temperature with a moderately low current density of 2 MA/cm^2 in which the exact metal film temperature is accurately calculated. As stated, the Au film temperatures were on average only 10°C above the oven temperature.

Figure 5.11 displays a cumulative probability graph of the Au M1 structure electromigration lifetimes. Median electromigration lifetimes ranged from 504 hours at 384°C to 4042 hours at 308°C. The Au electromigration failure distributions follow the log-normal model extremely well as shown in Figure 5.11.

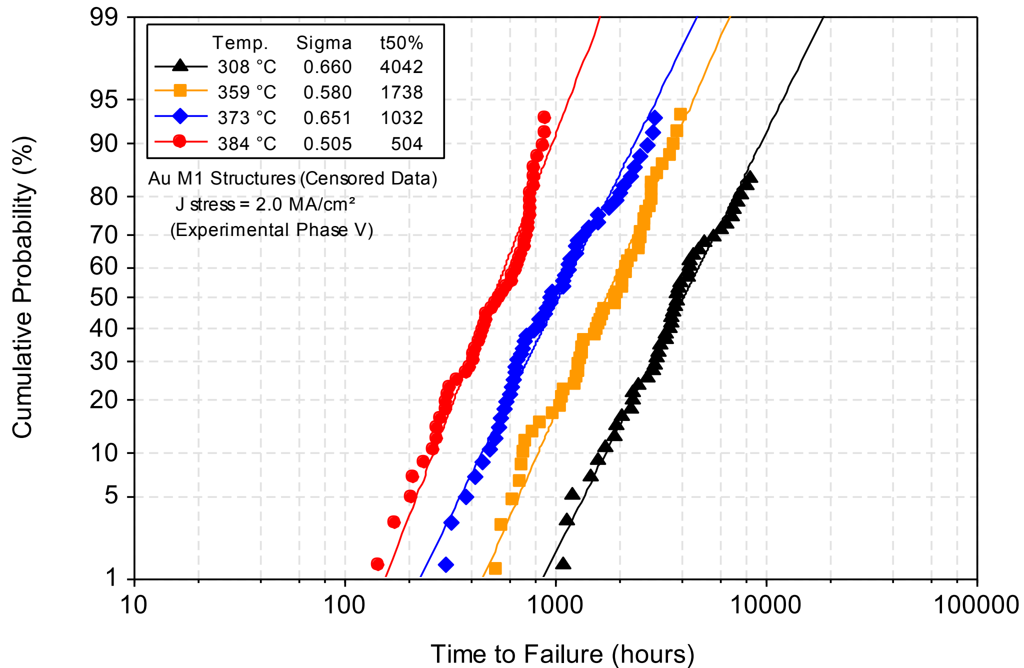


Figure 5.11 Electromigration lifetimes for the Au M1 structures (phase V).

The spread in electromigration lifetimes is reasonably tight with an average sigma value of 0.6 which is consistent with a mono-modal (single) failure mechanism. Also, it should be fully appreciated that the longest electromigration test at 308°C lasted 8400 hours (350 days) demonstrating the moderately accelerated and precisely controlled stress conditions. This careful and patient application of stress averts the undesirable multi-modal failure mechanisms and thermal fluctuation problems inherent with overstressed experimental conditions that are profoundly evident in many past Au electromigration studies.

The median electromigration lifetimes and the Joule-heated film temperatures of the Au M1 structures are fundamental in the extraction of electromigration activation energy. An Arrhenius plot of the Au M1 median electromigration lifetimes versus $1/kT$ in phase V is presented in Figure 5.12.

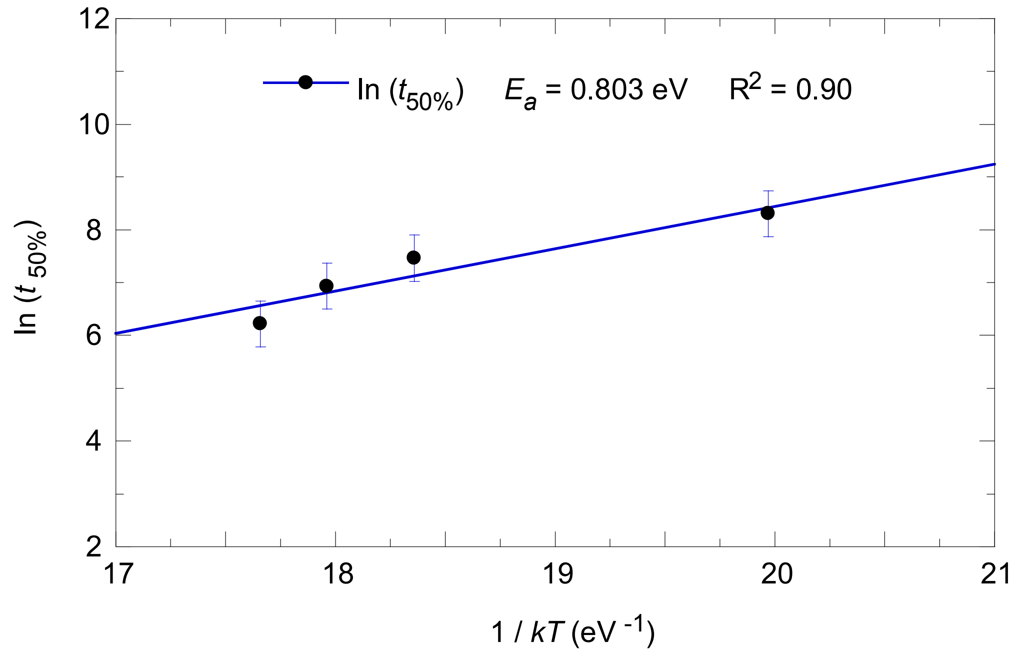


Figure 5.12 Arrhenius plot of median Au M1 electromigration lifetimes (phase V).

The activation energy of 0.80 eV was extracted from the slope of the line fitted to the Au median electromigration lifetimes. The R^2 of 0.9 indicates a strong linear relationship as exemplified by the fitted line transecting the standard error bars. This Au electromigration activation energy of 0.80 eV is in the mid-range of reported values (0.68 – 1.0 eV) for the resistometric method studies. Table 5.2 provides a comparison of different studies' experimental stress conditions, deposition methods, and extracted activation energies for Au electromigration.

Table 5.2 Comparison of activation energies for Au electromigration.

Authors	Stress Conditions	Deposition Method	Passivation	Activation Energy
Gangulee and d'Heurle[95]	6 MA/cm^2 202°C – 293°C	Electroplated 1.3 µm Au	No	0.88 ± 0.06 eV
Klein[96]	1.8 – 2.5 MA/cm^2 210°C – 350°C	Evaporated 0.05 µm Au	No	0.8 ± 0.2 eV
Agarwala[98]	1.7 – 5.5 MA/cm^2 254°C – 354°C	Sputtered 0.8 µm Au	SiO_2 / Mo	0.75 ± 0.05 eV
Hummel and Geier[102]	0.63 MA/cm^2 250°C – 430°C	Evaporated 0.17 µm Au	No	0.98 eV
Tai and Ohring[104]	0.8 – 2 MA/cm^2 120°C – 250°C	Evaporated 0.5 µm Au	No	0.80 ± 0.03 eV
Tang et al.[113]	3 MA/cm^2 221°C – 258°C	Evaporated 0.26 µm Au	No	0.73 ± 0.1 eV
Croes et al.[119]	4.3 MA/cm^2 265°C	Electroplated 1.4 µm Au	Si_3N_4	0.68 ± 0.09 eV
Whitman[120]	5 – 7 MA/cm^2 75°C – 160°C	Electroplated 1.0 µm Au	SiO_2	1 eV
This study	2 MA/cm^2 308°C – 384°C	Electroplated 1.0 µm Au	Si_3N_4	0.80 ± 0.05 eV

The previously published studies that evaluated Au films with passivation used higher current densities (> 3 MA/cm^2), where it is critical to account for Joule heating. It is suspected that Au film temperatures were not accurately determined. As a result, the activation energies (0.68 eV – 1.0 eV) varied widely in these studies. Notably, two independent studies by Klein[96] and Tai[104] with low current density (0.8 – 2.5 MA/cm^2) stress conditions extracted the same activation energy of 0.8 eV. It is important to note these studies used in-situ TEM observation of void growth and ^{195}Au radioactive isotope tracer techniques which are vastly different than the experimental resistometric method in this study. The fact that two other methods extracted the same activation energy of 0.8 eV is a strong validation of this investigation. It is especially noteworthy that accurate ^{195}Au tracer measurements attained the same activation energy, though this technique is not practical for industry reliability tests.

Mass transport in polycrystalline metals occurs by way of several contributing diffusion mechanisms that includes lattice (bulk), grain boundary, and surface or interfacial diffusion. A combination of these diffusion mechanisms can operate, but usually a single diffusion mechanism dominates depending on the temperature range, metallization, and the microstructure. Activation energies for self-diffusion in face-centered-cubic metals are found to correspond to the melting temperature (T_m),[146, 147] yet accurate measurement of diffusion activation energies remains a challenge.

Self-diffusion of Au in the medium to high temperature range (> 0.5 T_m) is predominantly lattice diffusion via the mono-vacancy mechanism, but contributions from di-vacancies are important at these high temperatures.[148] Within the temperature range (704°C to 1048°C) where Au lattice diffusion is dominant, a measured activation energy of 1.81 eV was determined by ^{198}Au radioactive tracer.[149] The dominant diffusion mechanism and the corresponding activation energy in the lower temperature range (< 0.5 T_m) is a sensitive function of the microstructure (grain size) and the geometric shape of the metal interconnect. A grain boundary diffusion mechanism was stated as dominant with an activation energy of 0.88 eV for polycrystalline Au in the temperature range of 367°C to 444°C.[150] For non-passivated Au films at much lower temperatures below 0°C, the surface diffusion mechanism is dominant possessing a lower activation energy of 0.32 eV.[151]

This strong dependence of activation energy on the mass transport pathway provides an indication of which diffusion pathway is dominant. Activation energy ranges observed for the main diffusion pathways for the common metal interconnects are tabulated in Table 5.3.

Table 5.3 Observed activation energies for various diffusion mechanisms.[59]

Metal Interconnect	Lattice (Bulk) E_a	Grain Boundary E_a	Interfacial E_a	Surface E_a
Al	1.4 eV	0.4 – 0.5 eV	—	0.28 eV[152]
Al(Cu)	1.2 eV	0.6 – 0.7 eV	0.8 – 1.0 eV	—
Cu	2.3 eV	0.8 – 1.0 eV[153]	0.7 – 1.0 eV	—
Au	1.8 eV[149]	0.7 – 0.98 eV (see Table 5.2)	—	0.32 eV[151]

These Au diffusion activation energies clearly show the trend: lattice E_a > grain boundary E_a (~ ½ bulk E_a) > surface E_a. It must be noted that Al surface diffusion is limited due to the native oxide layer that forms on exposed surfaces, thus shutting-off this diffusion pathway. In contrast, exposed Au surfaces do not oxidize so this investigation evaluated passivated Au interconnects to eliminate any surface diffusion pathways. A probable explanation for the widespread range of activation energies (0.42 – 1.0 eV) reported for Au is that the majority of these studies were carried out on non-passivated Au films. Activation energies attained close to the lowest value of 0.42 eV could have been influenced by a combination of surface and grain boundary diffusion.

Grain boundary diffusion is the predominant mechanism for electromigration in polycrystalline metal films at low temperatures (< 0.5 T_m). The activation energy of 0.8 eV obtained in this study for passivated Au interconnects is within activation energies dominated by the grain boundary diffusion mechanism. Physical evidence in support of grain boundary diffusion is provided by the void morphology (shown in Figure 4.35), in which voids were eroded out of Au grains near grain boundary triple points. Hence, it is concluded that grain boundary diffusion is the dominant mechanism found in this study.

5.4 Electromigration Current Density Exponent

Demands for higher performance ICs have driven the shrinkage of metal interconnect dimensions that have led to significantly higher current densities as depicted in Figure 1.1. At these higher operational current densities, there is increasingly higher risk of electromigration failures in interconnects and is the limiting design factor in achieving the desired practical lifetimes for ICs. According to Black's empirical model, the median electromigration lifetime ($t_{50\%}$) is proportional to the inverse square of current density ($1/J^2$) expressed as

$$t_{50\%} = \frac{A}{J^2} \exp\left(\frac{E_a}{kT}\right). \tag{5.2}$$

Still the earlier derived solid state theoretical model for the electromigration driving force (F_{em}) corresponds to a linear dependence on current density (J) given by

$$F_{em} = Z^*_{eff} \, e\rho J, \tag{5.3}$$

where Z^*_{eff} is the effective charge, e is electronic charge, and ρ is the resistivity. This disparity in current density dependence was reconciled by inclusion of the electromigration-induced backflow stress gradient.[64] More recent insight on the current density dependence is revealed by the failure kinetics of void nucleation and growth processes in a particular metallization. A modified expansion to Black's empirical model was proposed[69] that recognizes the two distinct kinetic processes of void nucleation and void growth involved in electromigration failures of metal interconnects.

In this modified Black's model, the electromigration median time to failure ($t_{50\%}$) is the sum of these two independent time components expressed as

$$t_{50\%} = t_{nuc} + t_g = \left(\frac{AkT}{J} + \frac{B(T)}{J^2}\right)\exp\left(\frac{E_a}{kT}\right), \qquad (5.4)$$

where t_{nuc} is time required for void nucleation and t_g is the time duration for growth of a void to become an open circuit. Constants A and B have geometric factors that pertain to the void size required to reach a line failure. Ascertained from this modified model by Lloyd[65] is that the current density dependence is determined by which process stage (void nucleation or void growth) dominates the overall electromigration failure times. Electromigration lifetime is dependent on the inverse square of current density ($1/J^2$) when the failure time is dominated by the void nucleation stage. Conversely, the electromigration lifetime is inversely dependent on current density ($1/J$) when failure time is primarily composed of the void growth stage. In cases where the current density exponent exceeds a square dependence ($n > 2$), the electromigration failure data is most likely confounded by Joule heating effects that cause severe temperature gradients.[59] Clearly, it is essential to eliminate any confounding effects such as temperature gradients to accurately extract the current density exponent.

Accordingly, the current density stress levels applied in this electromigration study on passivated Au interconnects were minimized to avoid significant Joule heating. In this approach, four current densities 1.25, 1.5, 1.75, and 2.0 MA/cm^2 were selected that restricted Joule heating to a maximum of 9°C. All experiments on current densities for the Au M1 structures were carried out at a constant oven temperature of 375°C. The Au M1 structure electromigration lifetime distribution at the four current densities is shown in Figure 5.13.

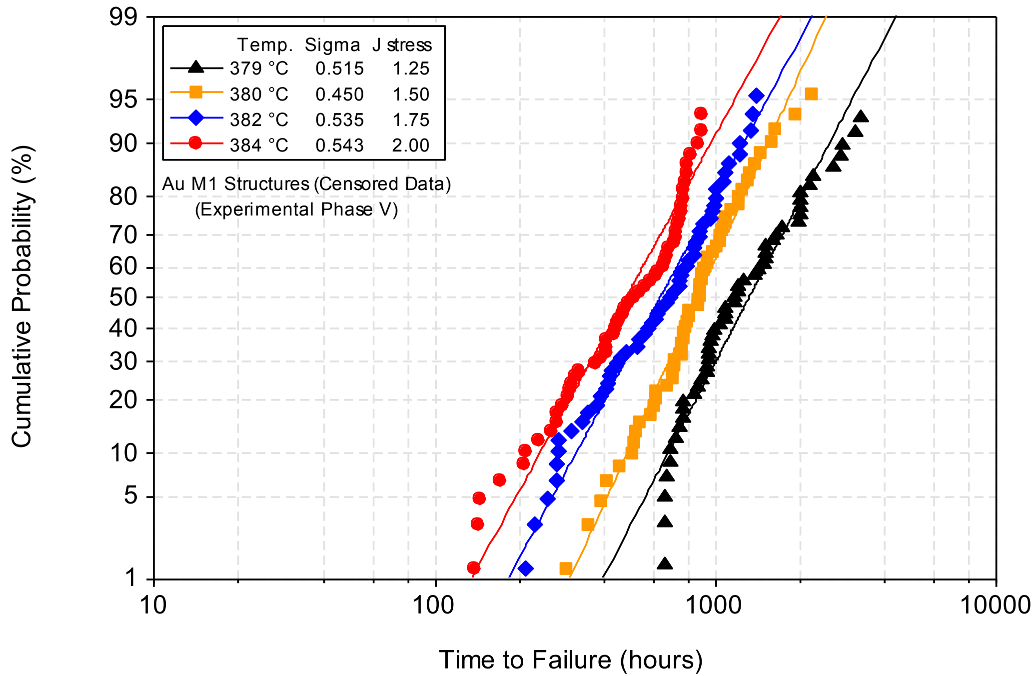


Figure 5.13 Electromigration lifetimes for the Au M1 structures at different *J*.

These results clearly show the median Au M1 structure electromigration lifetimes decreased with increased current densities at nearly constant temperature as anticipated. The median electromigration lifetime was 480 hours for highest current density of 2.0 MA/cm^2 and 1318 hours for the lowest current density of 1.25 MA/cm^2. A relatively tight log-normal sigma of less than 0.6 was found for all the electromigration failure distributions.

The increase in current density induced an incremental rise in the Joule-heated film temperature. Although the maximum increase in film temperature was slight (ΔT = 5°C), accurate current density exponent extraction requires median electromigration lifetimes from a constant single film temperature. Thus, the median Au M1 electromigration lifetimes were extrapolated using Equation (4.5) to the lowest experimental temperature of 379°C and are listed in Table 4.3.

The natural logarithm of the normalized median Au M1 structure electromigration lifetimes and current densities are plotted in Figure 5.14.

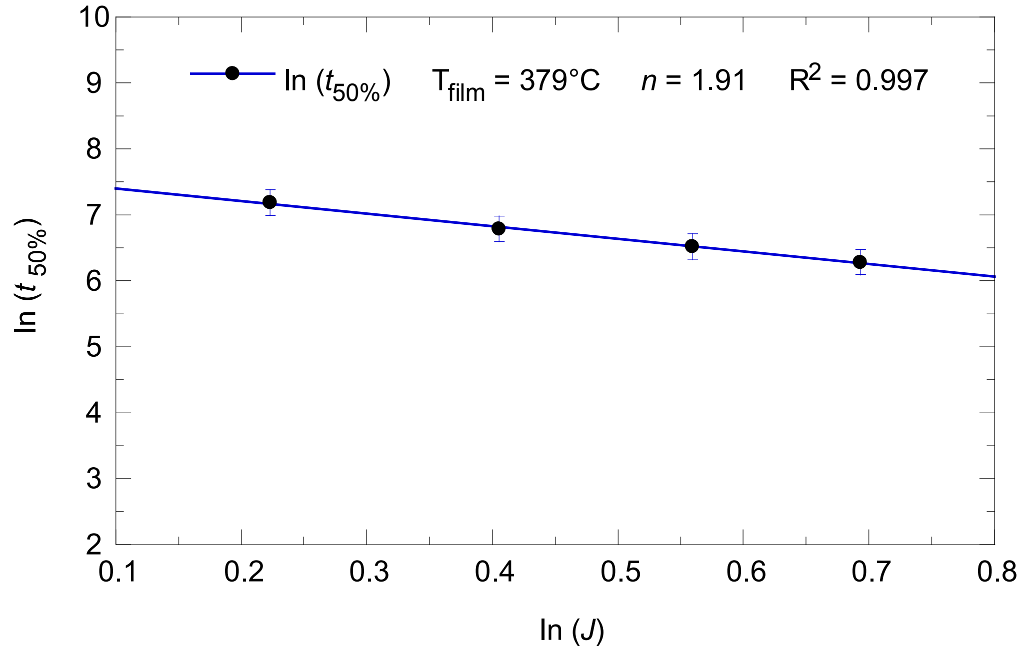


Figure 5.14 Natural logarithm of Au M1 median lifetimes versus current density.

A current density exponent of 1.91 was extracted from the slope of the fitted linear regression of the normalized Au M1 structure electromigration lifetimes versus current density. The coefficient of determination R^2 of 0.99 indicates that the data very closely fits the linear regression function. Even with the moderately low current densities in this investigation, there was no sign that electromigration was retarded by reaching Blech's critical threshold current density. In fact, electromigration in Au films was experimentally observed[104] at a current density as low as 0.6 MA/cm^2, which is less than half the lowest current density applied in this study.

In this study, the extracted current density exponent is the first reported value within the valid range of 1 to 2. Table 5.4 lists current density exponents for Au electromigration from the few studies that reported values.

Table 5.4 Comparison of current density exponents for Au electromigration.

Authors	Stress Conditions	Deposition Method	Passivation	*n*
Agarwala[98]	1.7 – 5.5 MA/cm^2 254°C – 354°C	Sputtered 0.8 μm Au	SiO_2 / Mo	3.3 ± 0.49
Croes et al.[119]	4.3 MA/cm^2 265°C	Electroplated 1.4 μm Au	Si_3N_4	2.0 ± 0.51
Whitman[120]	5 – 7 MA/cm^2 75°C – 160°C	Electroplated 1.0 μm Au	SiO_2	2.0 – 4.0
This study	1.25 – 2 MA/cm^2 379°C – 384°C	Electroplated 1.0 μm Au	Si_3N_4	1.91 ± 0.03

Most of the comparable studies investigated electroplated Au films (roughly the same thickness) with passivation layers but overly accelerated electromigration tests with current densities greater than 2.0 MA/cm^2. At higher current densities, severe temperature gradients form along the metal thin film stripe that affects accuracy of the film temperature measurement. Thus, it is suggested that these other studies with extracted current density exponents above 2 were impacted by significant Joule heating variations. This study's lower current density stresses avoided temperature gradients and as a result obtained an exponent of 1.91. Based on a model proposed by Lloyd,[69] fractional current density exponents near 2 indicate failure kinetics dominated by void nucleation. In conclusion, electromigration of electroplated Au interconnects under moderate current densities are primarily void nucleation controlled. Lastly, accurate current density exponents are imperative for extrapolation to operational conditions.

CHAPTER 6 CONCLUSIONS AND SUGGESTED FUTURE WORK

This brief chapter provides a summary of the overall experimental results and observations in this research. It concludes with future research suggestions.

6.1 Summary of Electromigration in Gold Interconnects

This research characterized the electromigration lifetimes of very large quantities of passivated electroplated Au interconnects fabricated on GaAs substrates in a 6-inch wafer fab using conventional lift-off process methods. High-resolution in-situ resistance monitoring equipment was utilized to measure Au electromigration lifetimes. Over the course of the five successive experimental phases (I – V) in this research, Au interconnect test structure design was significantly improved. The first design improvement was a dual Au interconnect test structure that doubled the number of devices under test (DUTs) to be stressed in parallel, thereby increasing statistical confidence in extracted electromigration model parameters. The second design improvement shortened the Au interconnect test structure length from 800 μm to 450 μm to reduce the standard deviation in resistance from 1.6 ohms to 0.54 ohms. Two different Au interconnect test structure types were examined, a standard NIST (M1) line structure and a via 1 / metal 1 interface (V1M1) test structure. As expected, the Au M1 structures had a median electromigration lifetime that was nearly 4 times longer in comparison to the Au V1M1 structures due to the current crowding, localized Joule heating, and flux divergence at the via interface.

The Au interconnect test structures were measured at multiple temperatures to determine the temperature coefficients of resistance (TCRs). Resistance versus temperature was very linear in the range of 150° to 350°C. A measured Au TCR value of 0.003752 per °C at 20°C was obtained. This Au TCR value is in extremely close agreement with the CRC Handbook derived value of 0.003753 per °C at 20°C. Thus, accurate Joule-heated Au interconnect film temperatures were calculated with this Au TCR value.

Application of a moderate current stress condition limited to a current density of 2.0 MA/cm^2 constrained the Joule heating of the Au interconnects to no more than 10°C above oven stress temperatures. A failure criterion of 50% resistance degradation ($\Delta R/R_o$) prevented thermal runaway and catastrophic metal ruptures as observed by many other studies on electromigration in Au films that performed open circuit failure tests. The 50% $\Delta R/R_o$ failure criterion enabled Au structures exhibiting resistance spikes to survive to longer lifetimes, diminishing the small early failure population. Failure analysis of the Au M1 structure that failed early revealed a void on the anode end. This early failure showed an extensive void cavity for only a 50% $\Delta R/R_o$ in which the Au along the bottom TiW interface was completely removed. FIB cross-sections on untested Au structures detected pre-existing small voids on the order of 100 Å to 1000 Å in the electroplated Au film. Based on all these void features (location, size, and morphology), it is suggested that pre-existing voids coalesced near the anode to accelerate this early electromigration failure. It is also proposed that the physical mechanism responsible for the precipitous resistance spike characteristic on a small percentage (< 10%) of Au structures is the coalescence of pre-existing voids and healing (recovery) through void annihilation.

Analysis of the initial Au structure resistance found no significant statistical correlation to electromigration lifetime. This is an important conclusion because electromigration lifetimes were found to be strongly dependent on stress conditions and not on the initial structure resistance variability. A median grain size of 0.91 μm was measured for the Au microstructure. This grain size is sufficiently polycrystalline within the Au line-width of 2 μm to avoid a bamboo-like structure that would inhibit grain boundary diffusion. The electroplated Au film was dissolved and analyzed by inductively coupled plasma optical emission spectroscopy (ICP-OES). No trace impurities of thallium and sulfur were found with the ICP-OES detection limits of 50 ppm and 5 ppm, respectively. Therefore, the electroplated Au films in this study were essentially 'pure Au'.

In this investigation on passivated electroplated Au interconnects, it was necessary to elevate the oven stress temperature above 300°C because electromigration tests at 308°C exceeded 8400 hours (350 days). The highest oven stress temperature of 375°C avoided over acceleration, yet reasonable test times of approximately 1000 hours were achieved. Median electromigration lifetimes ($t_{50\%}$) for the Au M1 structures ranged from 504 hours at 384°C to 4042 hours at 308°C. Electromigration lifetimes were relatively tight with an average log-normal sigma value of 0.6, which is consistent with a mono-modal (single) failure mechanism. An activation energy of 0.80 ± 0.05 eV was measured from constant current electromigration tests at multiple temperatures. A current density exponent of 1.91 was extracted from multiple current densities at a constant temperature. Electromigration-induced void morphology along with these model parameters indicated grain boundary diffusion is dominant and void nucleation mechanism controlled the failure time.

Overall, this research was successful in the development of test procedures and test structures for passivated gold interconnects that resulted in improved electromigration reliability test results and yielded very reasonable activation energies and current density exponents. Therefore, these accurately determined electromigration model parameters provide a good prediction of electromigration lifetimes under normal device operating temperatures.

6.2 Future Research Suggestions

A future characterization effort needs to focus on the entrapment mechanism that creates as-deposited voids in the electroplated Au films. Producing electroplated Au films without these as-deposited voids (defects) will eliminate defect related early failures, thus improving metallization performance and reliability. Additionally, investigation into the mechanistic details that caused the multi-modal failure distributions repeatedly observed near the temperature of 330°C is needed. One possible theory to be evaluated is that the dielectric films that encapsulate the electroplated Au deposited at 330°C by plasma enhanced chemical vapor deposition (PECVD) somehow induce mechanical stress that would cause Au migration.

Application of these same experimental methods to measure passivated evaporated Au films on gallium nitride (GaN) substrates to extract electromigration model parameters (E_a and n) for comparison with this study is also proposed. It is important to understand the current carrying capability and electromigration reliability of light emitting diodes (LEDs) that are fabricated by evaporated Au films on GaN. The growth in a wide variety of LED applications and its commercial use in indoor lighting have ramped-up mass production.

REFERENCES

1 "International Technology Roadmap for Semiconductors." [Online]. Available at: http://www.itrs.net/. (accessed: Dec. 15, 2012).

2 R. E. Hummel, "Electromigration and related failure mechanisms in integrated circuit interconnects," *International Materials Reviews,* vol. 39, pp. 97-111, (1994).

3 E. Higham and A. Anwar, "GaAs Industry overview and forecast: 2009 - 2014," in *CS ManTech Digest*, (2011).

4 P. S. Ho and T. Kwok, "Electromigration in metals," *Reports on Progress in Physics,* vol. 52, pp. 301-348, (1989).

5 V. B. Fiks, "On the mechanism of the mobility of ions in metals," *Soviet Physics - Solid State,* vol. 1, pp. 14-28, (1959).

6 H. B. Huntington and A. R. Grone, "Current-induced marker motion in gold wires," *Journal of Physics and Chemistry of Solids,* vol. 20, pp. 76-87, (1961).

7 H. B. Huntington, "Electromigration in metals," In *Diffusion in Solids: Recent Developments*, edited by A. S. Nowick and J. J. Burton, pp. 303-352, (Academic Press, New York, 1975).

8 J. R. Lloyd, "Electromigration in thin film conductors," *Semiconductor Science and Technology,* vol. 12, pp. 1177-1185, (1997).

9 F. M. d'Heurle, "Electromigration and failure in electronics: An introduction," *Proceedings of the IEEE,* vol. 59, pp. 1409-1418, (1971).

10 R. V. Penney, "Current-induced mass transport in aluminum," *Journal of Physics and Chemistry of Solids,* vol. 25, pp. 335-345, (1964).

11 I. A. Blech and H. Sello, "The failure of thin aluminum current-carrying strips on oxidized silicon," in *Physics of Failure in Electronics, 5th Annual Symposium on the*, pp. 496-505, (1966).

12 I. A. Blech and E. S. Meieran, "Direct transmission electron microscope observation of electrotransport in aluminum thin films," *Applied Physics Letters,* vol. 11, pp. 263-266, (1967).

13 R. Rosenberg and L. Berenbaum, "Resistance monitoring and effects of nonadhesion during electromigration in aluminum films," *Applied Physics Letters,* vol. 12, pp. 201-204, (1968).

14 J. R. Black, "Electromigration - A brief survey and some recent results," *Electron Devices, IEEE Transactions on,* vol. 16, pp. 338-347, (1969).

15 M. J. Attardo and R. Rosenberg, "Electromigration damage in aluminum film conductors," *Journal of Applied Physics,* vol. 41, pp. 2381-2386, (1970).

16 R. Rosenberg, "Value D_0Z^* for grain boundary electromigration in aluminum films," *Applied Physics Letters,* vol. 16, pp. 27-29, (1970).

17 F. d'Heurle and I. Ames, "Electromigration in single-crystal aluminum films," *Applied Physics Letters,* vol. 16, pp. 80-81, (1970).

18 T. Kwok, "Effect of metal line geometry on electromigration lifetime in Al-Cu submicron interconnects," in *Reliability Physics Symposium Proceedings, 26th Annual IEEE International*, pp. 185-191, (1988).

19 J. M. Pierce and M. E. Thomas, "Electromigration in aluminum conductors which are chains of single crystals," *Applied Physics Letters,* vol. 39, pp. 165-168, (1981).

20 S. Vaidya et al., "Linewidth dependence of electromigration in evaporated Al-0.5%Cu," *Applied Physics Letters,* vol. 36, pp. 464-466, (1980).

21 J. R. Black, "Electromigration failure modes in aluminum metallization for semiconductor devices," *Proceedings of the IEEE,* vol. 57, pp. 1587-1594, (1969).

22 S. M. Spitzer and S. Schwartz, "The effects of dielectric overcoating on electromigration in aluminum interconnections," *Electron Devices, IEEE Transactions on,* vol. 16, pp. 348-350, (1969).

23 J. R. Lloyd et al., "The role of metal and passivation defects in electromigration-induced damage in thin film conductors," *Thin Solid Films,* vol. 93, pp. 385-395, (1982).

24 I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *Journal of Applied Physics,* vol. 47, pp. 1203-1208, (1976).

25 I. A. Blech and C. Herring, "Stress generation by electromigration," *Applied Physics Letters,* vol. 29, pp. 131-133, (1976).

26 I. A. Blech and K. L. Tai, "Measurement of stress gradients generated by electromigration," *Applied Physics Letters,* vol. 30, pp. 387-389, (1977).

27 D. G. Pierce and P. G. Brusius, "Electromigration: A review," *Microelectronics and Reliability,* vol. 37, pp. 1053-1072, (1997).

28 I. Ames et al., "Reduction of electromigration in aluminum films by copper doping," *IBM Journal of Research and Development,* vol. 14, pp. 461-463, (1970).

29 F. M. d'Heurle, "The effect of copper additions on electromigration in aluminum thin films," *Metallurgical transactions,* vol. 2, pp. 681-689, (1971).

30 M. C. Shine and F. M. d'Heurle, "Activation energy for electromigration in aluminum films alloyed with copper," *IBM Journal of Research and Development,* vol. 15, pp. 378-383, (1971).

31 F. M. d'Heurle et al., "Activation energy for electromigration failure in aluminum films containing copper," *Journal of Vacuum Science and Technology,* vol. 9, pp. 289-293, (1972).

32 C. K. Hu et al., "Electromigration and stress-induced voiding in fine Al and Al-alloy thin-film lines," *IBM Journal of Research and Development,* vol. 39, pp. 465-497, (1995).

33 A. Gangulee and F. M. d'Heurle, "Effect of alloy additions on electromigration failures in thin aluminum films," *Applied Physics Letters,* vol. 19, pp. 76-77, (1971).

34 F. M. d'Heurle and A. Gangulee, "Effects of complex alloy additions on electromigration in aluminum thin films," in *Reliability Physics Symposium Proceedings, 10th Annual IEEE International*, pp. 165-170, (1972).

35 H. H. Hoang and J. M. McDavid, "Electromigration in multilayer metallization systems," *Solid State Technology,* vol. 30, pp. 121-6, (1987).

36 N. P. Armstrong, "Evaluation of TiW+Al/Cu electromigration performance," *Quality and Reliability Engineering International,* vol. 7, pp. 281-6, (1991).

37 P. B. Ghate and J. C. Blair, "Electromigration testing of Ti: W/Al and Ti: W/Al-Cu film conductors," *Thin Solid Films,* vol. 55, pp. 113-123, (1978).

38 J. O. Olowolafe et al., "Effect of TiN anneal ambient on the microstructure and electromigration performance of Al-based alloys," in *Materials Research Society Symposium Proceedings*, vol. 309, pp. 95-100, (1993).

39 T. Kikkawa et al., "Comparison of refractory metal and silicide capping effects on aluminum metallizations," in *VLSI Multilevel Interconnection Conference Proceedings, 6th Annual IEEE International*, pp. 463-469, (1989).

40 K. N. Tu, "Recent advances on electromigration in very-large-scale-integration of interconnects," *Journal of Applied Physics,* vol. 94, pp. 5451-5473, (2003).

41 P. L. Pai and C. H. Ting, "Selective electroless copper for VLSI interconnection," *Electron Device Letters, IEEE,* vol. 10, pp. 423-425, (1989).

42 C. W. Park and R. W. Vook, "The kinetics of electromigration damage in copper films studied by isothermal resistance change analysis," in *Materials Research Society Symposium Proceedings*, vol. 225, pp. 119-124, (1991).

43 C. W. Park and R. W. Vook, "Activation energy for electromigration in Cu films," *Applied Physics Letters,* vol. 59, pp. 175-177, (1991).

44 C.-K. Hu et al., "Electromigration in Cu/W structure," in *Materials Research Society Symposium Proceedings*, vol. 265, pp. 171-176, (1992).

45 C. W. Park and R. W. Vook, "Electromigration in vacuum evaporated Cu films," *Applied Surface Science,* vol. 70–71, Part 2, pp. 639-643, (1993).

46 J. Tao et al., "Electromigration characteristics of copper interconnects," *Electron Device Letters, IEEE,* vol. 14, pp. 249-251, (1993).

47 D. Gupta, "Comparative Cu diffusion studies in advanced metallizations of Cu and Al-Cu based thin films," in *Materials Research Society Symposium Proceedings*, vol. 337, pp. 209-215, (1994).

48 J. R. Lloyd and J. J. Clement, "Electromigration in copper conductors," *Thin Solid Films,* vol. 262, pp. 135-141, (1995).

49 S. Venkatesan et al., "A high performance 1.8 V, 0.20 μm CMOS technology with copper metallization," in *Electron Devices Meeting (IEDM), IEEE International*, pp. 769-772, (1997).

50 D. Edelstein et al., "Full copper wiring in a sub-0.25 μm CMOS ULSI technology," in *Electron Devices Meeting (IEDM), IEEE International*, pp. 773-776, (1997).

51 C. K. Hu et al., "Comparison of electromigration in submicron Al(Cu) and Cu thin film lines," *AIP Conference Proceedings,* vol. 373, pp. 153-168, (1996).

52 R. Rosenberg et al., "Copper metallization for high performance silicon technology," *Annual Review of Materials Science,* vol. 30, pp. 229-262, (2000).

53 E. T. Ogawa et al., "Electromigration reliability issues in dual-damascene Cu interconnections," *Reliability, IEEE Transactions on,* vol. 51, pp. 403-419, (2002).

54 J. R. Lloyd, "Quick tests for electromigration: useful but not without danger," in *Materials Research Society Symposium Proceedings*, vol. 265, pp. 177-186, (1992).

55 I. A. Blech, "Electromigration and crevice formation in thin metallic films," *Thin Solid Films,* vol. 13, pp. 117-129, (1972).

56 I. A. Blech and E. S. Meieran, "Electromigration in thin Al films," *Journal of Applied Physics,* vol. 40, pp. 485-491, (1969).

57 I. A. Blech and E. Kinsbron, "Electromigration in thin gold films on molybdenum surfaces," *Thin Solid Films,* vol. 25, pp. 327-334, (1975).

58 R. E. Hummel et al., "Activation energy for electrotransport in thin aluminum films by resistance measurements," *Journal of Physics and Chemistry of Solids,* vol. 37, pp. 73-80, (1976).

59 J. R. Lloyd, "Electromigration in integrated circuit conductors," *Journal of Physics D: Applied Physics,* vol. 32, pp. 109-18, (1999).

60 J. R. Black, "Mass transport of aluminum by momentum exchange with conducting electrons," in *Reliability Physics Symposium Proceedings, 6th Annual IEEE International*, pp. 148-159, (1967).

61 J. R. Lloyd, "30 years of electromigration research: A grand masters' perspective," in *Materials Research Society Symposium Proceedings*, vol. 428, pp. 3-14, (1996).

62 A. S. Oates, "Current density dependence of electromigration failure of submicron width, multilayer Al alloy conductors," *Applied Physics Letters,* vol. 66, pp. 1475-1477, (1995).

63 C. K. Hu et al., "Copper interconnection integration and reliability," *Thin Solid Films,* vol. 262, pp. 84-92, (1995).

64 M. Shatzkes and J. R. Lloyd, "A model for conductor failure considering diffusion concurrently with electromigration resulting in a current exponent of 2," *Journal of Applied Physics,* vol. 59, pp. 3890-3, (1986).

65 J. R. Lloyd, "Electromigration failure," *Journal of Applied Physics,* vol. 69, pp. 7601-7604, (1991).

66 J. R. Lloyd and J. Kitchin, "The electromigration failure distribution: The fine-line case," *Journal of Applied Physics,* vol. 69, pp. 2117-2127, (1991).

67 M. A. Korhonen et al., "Stress evolution due to electromigration in confined metal lines," *Journal of Applied Physics,* vol. 73, pp. 3790-3799, (1993).

68 J. J. Clement and C. V. Thompson, "Modeling electromigration-induced stress evolution in confined metal lines," *Journal of Applied Physics,* vol. 78, pp. 900-904, (1995).

69 J. R. Lloyd, "Black's law revisited—Nucleation and growth in electromigration failure," *Microelectronics Reliability,* vol. 47, pp. 1468-1472, (2007).

70 "Gold." *Wikipedia, The Free Encyclopedia*, [Online]. Available at: http://en.wikipedia.org/w/index.php?title=Gold&oldid=526175716. (accessed: Dec. 8, 2012).

71 M. Grimwade, "The metallurgy of gold," *Interdisciplinary Science Reviews,* vol. 17, pp. 371-381, (1992).

72 K. E. Saeger and J. Rodies, "The colour of gold and its alloys," *Gold Bulletin,* vol. 10, pp. 10-14, (1977).

73 "Aluminium." *Wikipedia, The Free Encyclopedia*, [Online]. Available at: http://en.wikipedia.org/w/index.php?title=Aluminium&oldid=527826460. (accessed: Dec. 8, 2012).

74 "Copper." *Wikipedia, The Free Encyclopedia*, [Online]. Available at: http://en.wikipedia.org/w/index.php?title=Copper&oldid=528138593 (accessed: Dec. 8, 2012).

75 "Silver." *Wikipedia, The Free Encyclopedia*, [Online]. Available at: http://en.wikipedia.org/w/index.php?title=Silver&oldid=525772411 (accessed: Dec. 8, 2012).

76 P. A. Kohl, "Electrodeposition of gold," In *Modern Electroplating*, pp. 201-225, (John Wiley & Sons, Inc., 2000).

77 G. E. Dieter, *Mechanical Metallurgy*, 3rd ed., McGraw-Hill, 1986.

78 W. F. Smith, *Principles of Materials Science and Engineering*, 2nd ed., McGraw-Hill, 1990.

79 A. J. Bard et al., *Standard Potentials in Aqueous Solution*, Marcel Dekker, 1985.

80 L. E. Terry and R. W. Wilson, "Metallization systems for silicon integrated circuits," *Proceedings of the IEEE,* vol. 57, pp. 1580-1586, (1969).

81 L. W. Danley, "A metallization system for microwave and UHF power transistors," *Solid State Technology,* vol. 18, pp. 35-9, (1975).

82 J. A. Cunningham et al., "Corrosion resistance of several integrated-circuit metallization systems," *Reliability, IEEE Transactions on,* vol. R-19, pp. 182-187, (1970).

83 R. W. Wilson and L. E. Terry, "Metallization systems for integrated circuits," *Journal of Vacuum Science and Technology,* vol. 7, pp. 142-142, (1970).

84 D. C. Dening et al., "Reliability of high temperature I^2L integrated circuits," in *Reliability Physics Symposium Proceedings, 22nd Annual IEEE International*, pp. 30-36, (1984).

85 K. Fricke et al., "A new GaAs technology for stable FETs at 300 degrees C," *Electron Device Letters, IEEE,* vol. 10, pp. 577-579, (1989).

86 R. Williams, *Modern GaAs Processing Methods*, Norwood, MA, USA: Artech House, 1990.

87 D. V. Morgan, "Interdiffusion of metal films on gallium arsenide and indium phosphide," In *Reliability and Degradation - Semiconductor Devices and Circuits*, pp. 151-189, (Wiley, Chichester, UK, 1981).

88 N. Braslau et al., "Metal-semiconductor contacts for GaAs bulk effect devices," *Solid-State Electronics,* vol. 10, pp. 381-383, (1967).

89 T. E. Hartman and J. C. Blair, "Electromigration in thin gold films," *Electron Devices, IEEE Transactions on,* vol. ED16, pp. 407-410, (1969).

90 J. R. Devaney, "Investigation of current-induced mass transport in thin metal conducting stripes," in *Reliability Physics Symposium Proceedings, 8th Annual IEEE International*, pp. 127-132, (1970).

91 R. E. Hummel and H. M. Breitling, "On the direction of electromigration in thin silver, gold, and copper films," *Applied Physics Letters,* vol. 18, pp. 373-375, (1971).

92 J. C. Blair et al., "Electromigration-induced failures in, and microstructure and resistivity of, sputtered gold films," *Journal of Applied Physics,* vol. 43, pp. 307-311, (1972).

93 R. E. Hummel, "Observations on the electromigration in various thin films of group I-IV," *Thin Solid Films,* vol. 13, pp. 175-178, (1972).

94 H. M. Breitling and R. E. Hummel, "Electromigration in thin silver, copper, gold, indium, tin, lead and magnesium films," *Journal of Physics and Chemistry of Solids,* vol. 33, pp. 845-848, IN1-IN2, 849-852, (1972).

95 A. Gangulee and F. M. d'Heurle, "The activation energy for electromigration and grain-boundary self-diffusion in gold," *Scripta Metallurgica,* vol. 7, pp. 1027-1030, (1973).

96 B. J. Klein, "Electromigration in thin gold films," *Journal of Physics F: Metal Physics,* vol. 3, pp. 691-696, (1973).

97 A. T. English et al., "Electromigration of Ti-Au thin-film conductors at 180°C," *Journal of Applied Physics,* vol. 45, pp. 3757-3767, (1974).

98 B. N. Agarwala, "Electromigration failure in Au thin-film conductors," in *Reliability Physics Symposium Proceedings, 13th Annual IEEE International*, pp. 107-112, (1975).

99 I. A. Blech and R. Rosenberg, "On the direction of electromigration in gold thin films," *Journal of Applied Physics,* vol. 46, pp. 579-583, (1975).

100 M. Etzion et al., "Study of conductive gold film lifetime under high current densities," *Journal of Applied Physics,* vol. 46, pp. 1455-1458, (1975).

101 R. E. Hummel and R. T. DeHoff, "On the controversy about the direction of electrotransport in thin gold films," *Applied Physics Letters,* vol. 27, pp. 64-66, (1975).

102 R. E. Hummel and H. J. Geier, "Activation energy for electrotransport in thin silver and gold films," *Thin Solid Films,* vol. 25, pp. 335-342, (1975).

103 E. Kinsbron et al., "The threshold current density and incubation time to electromigration in gold films," *Thin Solid Films,* vol. 46, pp. 139-150, (1977).

104 K. L. Tai and M. Ohring, "Grain-boundary electromigration in thin films II. Tracer measurements in pure Au," *Journal of Applied Physics,* vol. 48, pp. 36-45, (1977).

105 J. R. Lloyd and S. Nakahara, "The effect of high d.c. density stressing on pre-existing voids in thin gold films," *Thin Solid Films,* vol. 64, pp. 163-169, (1979).

106 R. J. Miller and A. Gangulee, "Electromigration in gold and copper thin film conductors," *Thin Solid Films,* vol. 69, pp. 379-386, (1980).

107 R. E. Hummel et al., "The effect of minor constituents on the electrotransport-induced failure site in thin gold films," *Applied Physics Letters,* vol. 33, pp. 960-962, (1978).

108 R. E. Hummel et al., "Thermal grooving, thermotransport and electrotransport in doped and undoped thin gold films," *Thin Solid Films,* vol. 78, pp. 1-14, (1981).

109 R. E. Hummel et al., "New insights on the reversal of the site of electromigration failure in gold films doped with alkali," *Journal of Applied Physics,* vol. 54, pp. 2855-2856, (1983).

110 R. E. Hummel et al., "The role of thermal grooving, thermotransport and electrotransport on the failure of thin film metallizations," in *Reliability*

Physics Symposium Proceedings, 22nd Annual IEEE International, pp. 234-241, (1984).

111 K. Eden et al., "Electromigration in fine-line conductors (0.45-2 μm)," *Microelectronic Engineering,* vol. 1, pp. 263-268, (1983).

112 J. Y. Kim and R. E. Hummel, "Hole and hillock formation in gold metallizations at elevated temperatures deposited on titanium, vanadium, and other barrier layers," *Physica Status Solidi (a),* vol. 122, pp. 255-273, (1990).

113 P. F. Tang et al., "Electromigration in thin films of Au on GaAs," in *Advanced Electronic Packaging Materials, Materials Research Society Symposium on*, vol. 167, Pittsburgh, PA, USA, pp. 341-5, (1990).

114 M. Paniccia et al., "Scanning probe microscopy studies of electromigration in electroplated Au wires," *Journal of Applied Physics,* vol. 73, pp. 8189-8197, (1993).

115 M. Aguilar et al., "The effect of electrical current (DC) on gold thin films," *Surface Science,* vol. 409, pp. 501-511, (1998).

116 M. Aguilar et al., "Electromigration in gold thin films," *Thin Solid Films,* vol. 317, pp. 189-192, (1998).

117 A. Panin and A. Shugurov, "Electromigration-induced damage of Au conductor lines," in *Science and Technology, Proceedings of the 5th Russian-Korean International Symposium on*, vol. 1, pp. 182-186 vol.1, (2001).

118 S. Bai and K. P. Roenker, "Early stage electromigration in gold thin films," *Journal of Applied Physics,* vol. 84, pp. 4248-4254, (1998).

119 K. Croes et al., "High-resolution in-situ of gold electromigration: test time reduction," *Microelectronics Reliability,* vol. 41, pp. 1439-1442, (2001).

120 C. S. Whitman, "Prediction of transmission line lifetimes over temperature and current density," *Microelectronics Reliability,* vol. 49, pp. 488-494, (2009).

121 H. A. Schafft et al., "Reproducibility of electromigration measurements," *Electron Devices, IEEE Transactions on,* vol. 34, pp. 673-681, (1987).

122 T. Kwok et al., "Electromigration in a two-level Al-Cu interconnection with W studs," in *VLSI Multilevel Interconnection Conference Proceedings, 7th Annual IEEE International*, pp. 106-112, (1990).

123 H. Kahn and C. V. Thompson, "A statistical characterization of electromigration-induced open failures in 2-level metal structures," in

Materials Research Society Symposium Proceedings, vol. 225, pp. 15-20, (1991).

124 J. J. Estabil et al., "Electromigration improvements with titanium underlay and overlay in Al(Cu) metallurgy," in *VLSI Multilevel Interconnection Conference Proceedings, 8th Annual IEEE International*, pp. 242-248, (1991).

125 H. A. Schafft, "Thermal-analysis of electromigration test structures," *Electron Devices, IEEE Transactions on,* vol. 34, pp. 664-672, (1987).

126 H. A. Schafft and J. S. Suehle, "The measurement, use and interpretation of the temperature-coefficient of resistance of metallizations," *Solid-State Electronics,* vol. 35, pp. 403-410, (1992).

127 F. M. d'Heurle and P. S. Ho, "Electromigration in thin films," In *Thin Films - Interdiffusion and Reactions*, edited by J. Poate, K. N. Tu and J. W. Mayer, pp. 243-303, (Wiley, Chichester, UK, 1978).

128 M. Gall et al., "Statistical analysis of early failures in electromigration," *Journal of Applied Physics,* vol. 90, pp. 732-740, (2001).

129 P. A. Tobias and D. C. Trindade, *Applied Reliability*, 2nd ed., Van Nostrand Reinhold, 1995.

130 R. A. Serway, *Physics for Scientists & Engineers with Modern Physics*, 3rd ed., Saunders College Pub., 1990.

131 D. R. Lide, *CRC Handbook of Chemistry and Physics: A Ready-Reference Book of Chemical and Physical Data*, 78th ed., CRC Press, 1997.

132 R. G. Filippi et al., "The effect of a threshold failure time and bimodal behavior on the electromigration lifetime of copper interconnects," in *Reliability Physics Symposium Proceedings, 47th Annual IEEE International*, pp. 444-451, (2009).

133 R. G. Filippi et al., "Implications of a threshold failure time and void nucleation on electromigration of copper interconnects," *Journal of Applied Physics,* vol. 107, pp. 103709-7, (2010).

134 X. Meng-Burany, "Analysis of electroplated films using dual-beam FIB / SEM and TEM techniques," In *Modern Electroplating*, pp. 637-663, (John Wiley & Sons, Inc., 2010).

135 L. A. Giannuzzi and J. R. Michael, "Comparison of channeling contrast between ion and electron images," *Microscopy and Microanalysis,* vol. 19, pp. 344-349, (2013).

136 ASTM Standard E112-10, "Standard test methods for determining average grain size," ASTM International, West Conshohocken, PA, (2010).

137 R. C. Sanwald, "The characteristics of small gas-filled voids in electrodeposited gold," *Metallography,* vol. 4, pp. 503-13, (1971).

138 W. J. Dauksher et al., "A new operating regime for electroplating the gold absorber on x-ray masks," *Microelectronic Engineering,* vol. 23, pp. 235-238, (1994).

139 T. Osaka et al., "Electrodeposition of soft gold from a thiosulfate-sulfite bath for electronics applications," *Journal of the Electrochemical Society,* vol. 144, pp. 3462-9, (1997).

140 S. Kilgore et al., "Electromigration of Electroplated Gold Interconnects," *Materials Research Society Symposium Proceedings,* vol. 863, (2005).

141 D. J. LaCombe and E. Parks, "A Study of Resistance Variations During Electromigration," in *Reliability Physics Symposium Proceedings, 23th Annual IEEE International*, pp. 74-80, (1985).

142 J. C. Doan et al., "The relationship between resistance changes and void volume changes in passivated aluminum interconnects," in *Reliability Physics Symposium Proceedings, 37th Annual IEEE International*, pp. 206-212, (1999).

143 L. Arnaud et al., "Microstructure and electromigration in copper damascene lines," *Microelectronics Reliability,* vol. 40, pp. 77-86, (2000).

144 L. Arnaud, "Electromigration threshold length effect in dual damascene copper-oxide interconnects," in *Reliability Physics Symposium Proceedings, 40th Annual IEEE International*, pp. 433-434, (2002).

145 X. Lu et al., "Statistical study of electromigration line-width dependence in Cu/low-k interconnects," *AIP Conference Proceedings,* vol. 741, pp. 188-195, (2004).

146 K. Mukherjee, "Correlation between the energy of motion of monovacancies and the melting temperature of metals," *Journal of Physics and Chemistry of Solids,* vol. 25, p. 517, (1964).

147 K. Mukherjee, "Correlation between the absolute melting temperatures and the activation energy of formation of monovancies in fcc metals," *Physics Letters,* vol. 8, pp. 17-18, (1964).

148 J. B. Adams et al., "Self-diffusion and impurity diffusion of fcc metals using the five-frequency model and the Embedded Atom Method," *Journal of Materials Research,* vol. 4, pp. 102-112, (1989).

149 S. M. Makin et al., "Self-diffusion in gold," *Proceedings of the Physical Society. Section B,* vol. 70, pp. 545-552, (1957).

150 D. Gupta, "Grain-boundary self-diffusion in Au by Ar sputtering technique," *Journal of Applied Physics,* vol. 44, pp. 4455-4458, (1973).

151 A. Trembulowicz et al., "Surface diffusion of gold on quasihexagonal-reconstructed Au(100)," *Physical Review B,* vol. 84, p. 245445 (5 pp.), (2011).

152 G. L. Baldini et al., "Electromigration in thin-films for microelectronics," *Microelectronics Reliability,* vol. 33, pp. 1779-1805, (1993).

153 C. S. Hau-Riege, "An introduction to Cu electromigration," *Microelectronics Reliability,* vol. 44, pp. 195-205, (2004).