Large Area Ultrapassivated Silicon Solar Cells

Using Heterojunction Carrier Collectors

by

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ABSTRACT

Silicon solar cells with heterojunction carrier collectors based on a-Si/c-Si heterojunction (SHJ) have a potential to overcome the limitations of the conventional diffused junction solar cells and become the next industry standard manufacturing technology of solar cells. A brand feature of SHJ technology is ultrapassivated surfaces with already demonstrated 750 mV open circuit voltages (V_{OC}) and 24.7% efficiency on large area solar cell.

Despite very good results achieved in research and development, large volume manufacturing of high efficiency SHJ cells remains a fundamental challenge. The main objectives of this work were to develop a SHJ solar cell fabrication flow using industry compatible tools and processes in a pilot production environment, study the interactions between the used fabrication steps, identify the minimum set of optimization parameters and characterization techniques needed to achieve 20% baseline efficiency, and analyze the losses of power in fabricated SHJ cells by numerical and analytical modeling.

This manuscript presents a detailed description of a SHJ solar cell fabrication flow developed at ASU Solar Power Laboratory (SPL) which allows large area solar cells with >750 mV V_{OC}. SHJ cells on 135 μm thick 153 cm^2 area wafers with 19.5% efficiency were fabricated. Passivation quality of (i)a-Si:H film, bulk conductivity of doped a-Si films, bulk conductivity of ITO, transmission of ITO and the thickness of all films were identified as the minimum set of optimization parameters necessary to set up a baseline high efficiency SHJ fabrication flow. The preparation of randomly textured wafers to minimize the concentration of surface impurities and to avoid epitaxial growth of a-Si films was found to be a key challenge in achieving a repeatable and uniform

passivation. This work resolved this issue by using a multi-step cleaning process based on sequential oxidation in nitric/acetic acids, Piranha and RCA-b solutions. The developed process allowed state of the art surface passivation with perfect repeatability and negligible reflectance losses.

Two additional studies demonstrated 750 mV local V_{OC} on 50 micron thick SHJ solar cell and < 1 cm/s effective surface recombination velocity on n-type wafers passivated by a-Si/SiO_2/SiN_x stack.

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Chapter 1
INTRODUCTION

1.1 Status of PV Industry in 2013

The first experimental solid state devices that convert sunlight directly into electricity were created in 1930s. these devices were based on such materials as Cu_2O[1], Se[2] and Tl_2S[3]. The potential of photovoltaic technology was quickly recognized by a number of scientists who offered to cover the roofs with photovoltaic elements in late 1930s[4]. However, the first real economic application of solar cells took place in space, where they were used to supply energy for spacecrafts and satellites. The cells sent to space were based on crystalline silicon (c-Si) technology which emerged in 1950s and continued to boom for the next several decades. In 1958, Chapin et al. reported using silicon p-n junction for converting light into electricity for the first time[5]. The efficiency of the first c-Si solar cell was about 5%. By the 1970s, Si solar cells reached 17% efficiency[6] which was followed by the first terrestrial applications for powering remote electrical devices. Wider utilization of photovoltaic devices, however, required further technological improvements for cost reduction.

Major development in Si photovoltaics occurred during late 1980s and early 1990s with most notable results from the University of New South Wales (UNSW) and Stanford University. A PV industry as a sector of economic manufacturing PV modules and installing PV systems to produce electricity emerged in the middle 2000s with the introduction of the feed-in-tariff in Germany. At the same time, the industry introduced several key manufacturing processes with a good relation between production cost and

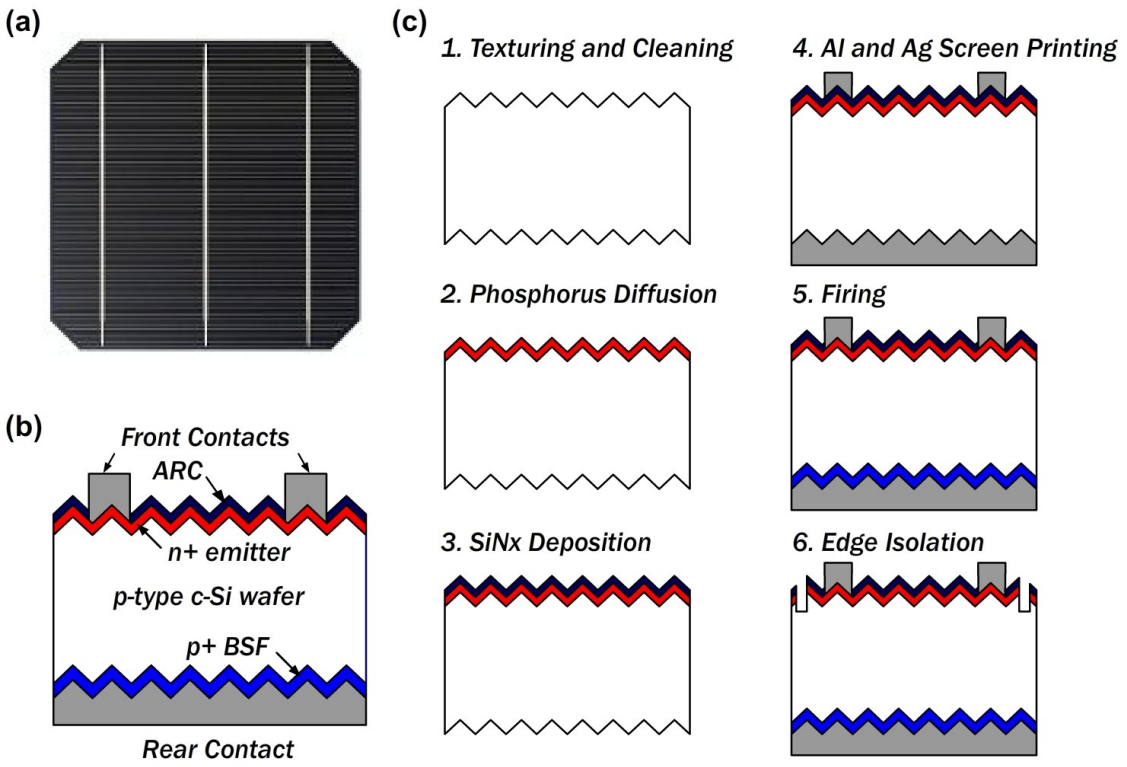


Fig.1-1. A structure and fabrication flow for a conventional screen printed solar cell. (a) A photo of a typical solar cell on 6" monocrystalline Si wafer. (b) Schematic diagram of the cross section of screen printed solar cell. (c) 6 core process flow steps which are used in manufacturing of basic screen printed cells with 17-18% efficiency. For more detailed description of screen printing technology see the review papers by Aberle [7] and Neuhaus [8].

device performance. Presently, more than 90% of the solar cells generating electricity in the field are based on wafer Si technology with the device schematic and main fabrication steps shown in Fig.1-1. For the last 10 years, the PV industry has demonstrated more than 40% cumulative annual growth rate with more than three times cost reduction that quickly approaches grid parity. In fact, today, PV electricity is cost competitive in locations with high solar irradiation and high electricity prices, where it can compete with conventional power generation technologies without additional state subsidies. Fig.1-2 shows world and US totals installed PV capacity as it compared to the cumulative

electrical generation capacity. Fig.1-2 also shows the average PV module selling price (ASP)which has experienced a significant drop in the last five years after poly-Si shortage peaked in 2008. Presently, the cost of PV modules can be as low as \$0.5/W_p to constitute between only20% and 30% of the total PV system cost.

PV has become a major contributor to the newly installed electricity generation capacity in Europe—with about 16.6 GW_p installed in 2012[9].Wind turbines were second to PV with 11.8 GW_p installed capacity followed by natural gas power plants with

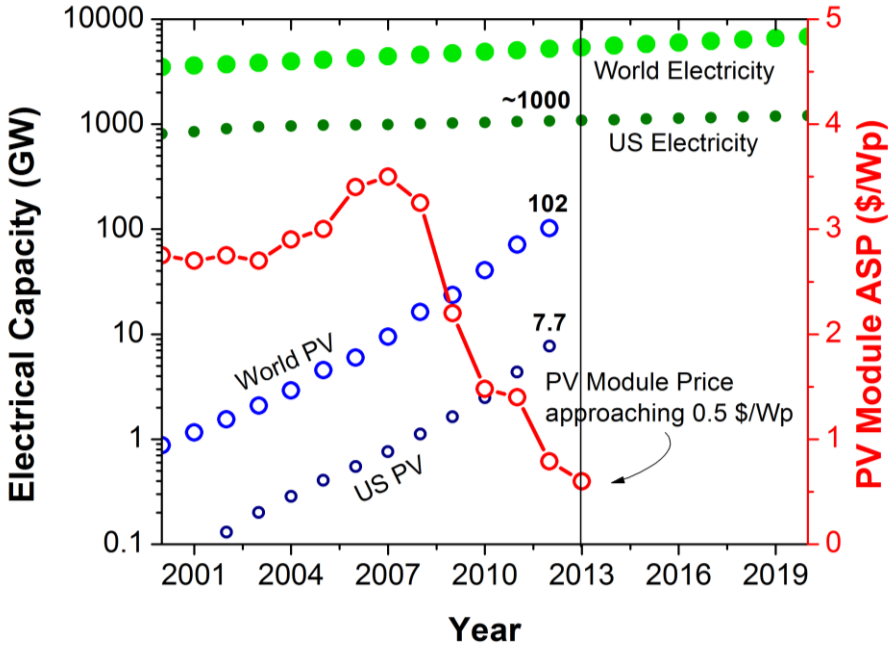


Fig.1-2. The growth of installed PV capacity and the reduction of PV module average selling price in 2000-2012. The graph also shows total electricity generation capacity for comparison. Note that PV has a lower capacity factor (annual kWhr produced for each kWp installed) compared to other electricity generation technologies. Capacity factor will also strongly depend on the location and PV system setup. For example, 1 kWp installed in Germany will generate about 800 kWhr of electricity during the year while it could generate 1600 kWhr in Arizona. Comparatively, 1 kWp nuclear power produces approximately 4000 kWhr of electricity annually. Also note that total energy consumption also includes heating/cooling and transportation which constitutes about 2/3 of the entire amount.

10.5 GW installed and 5.5 GW decommissioned. In 2012, PV generated approximately 6.5% of the total electricity in Italy and 5.5% in Germany[9]. The U.S. still lags behind Europe as PV installations only took off significantly in 2012 when 3.3 GW_p PV was installed to reach total 7.7 GW_p [10].

The growth within the last decade is based primarily on the state subsidies initially put into PV demand in a number of European countries and later put into PV supply mainly in China. In order to achieve a sustainable growth in the next ten years without relying on state stimuli, the PV industry will need to meet grid parity in most electricity markets(i.e. further reduce the cost of PV systems). Since the cost consists of multiple components, the reduction can come from many areas, e.g. raw materials, large volume manufacturing, system installation, or even financing. It turns out, for example, that rapid reduction of PV module costs for the last three years was mainly driven by declining poly-Si prices. Improvements in solar cell technology, however, were falling behind the learning curve[11]. On the solar cell side, cost reduction can be achieved by switching to higher efficiency technologies. These technologies can reduce the cost of balance of system (BOS) components as discussed later in Section 1.4. Introduction of high efficiency cell designs into mass production, however, is always a tradeoff between increased conversion efficiency and additional cost. High efficiency approaches usually require larger number of fabrication steps often using specialized expensive equipment. Alternatively, for low efficiency technologies, the tradeoff is between the reduced efficiency and the reduction of manufacturing or materials cost. Switching to high efficiency cells in order to compete with mainstream screen printing technology also poses a challenge as the manufacturers are forced to ramp up manufacturing capacity in

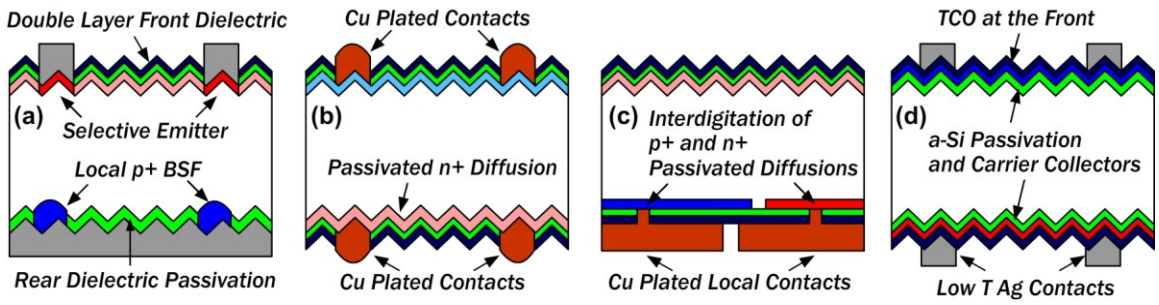


Fig.1-3.Structure of the solar cells representing four main high efficiency technologies.(a) PERC/PERL solar cell, (b) bifacial cell with passivated diffusion at the rear (PASHA cell), (c) interdigitated back contact (IBC) solar cell, (d) silicon heterojunction (SHJ) solar cell.

Table 1-1. A table comparing main high efficiency solar cell technologies

	PERC/PERL	(b) Bifacial	(c) IBC	(d) SHJ
Small area efficiency	25	n/a	n/a	n/a
Large area efficiency	20-21	20-21	24.2	24.7
Mean efficiency in production	19.5-20.5	19.5-20.5	23-24	22-23
Wafer type	p	n/p	n	n
Surface passivation	SiO_2/SiNx Al_2O_3/SiNx	SiO_2/SiN_x Al_2O_3/SiN_x	SiO2/SiNx Al2O3/SiNx	a-Si
Main manufacturers	Suntech, Suniva, Trina	Yingli, TetraSun, bSolar, Nexolon	SunPower	Panasonic, Silevo

order to use the advantages of the economy of scale which is related to high financial risks. Nonetheless, the industry is on the verge of shifting from conventional screen printing technology towards technologies which will ideally provide both higher efficiency and lower manufacturing cost.

1.2 High Efficiency Solar Cell Technologies

In this section, high efficiency solar cell technologies that can replace screen printed cells in large volume manufacturing in the next 5-10 years are reviewed. Fig.1-3 shows the structures of four main high efficiency c-Si solar cell technologies while Table

1-1 compares several of their important characteristics. The considered technologies include Passivated Emitter and Rear Cell (PERC) developed at the University of New South Wales (UNSW), bifacial solar cells with planar diffused passivated carrier collectors developed by ECN in the Netherlands, Interdigitated Back Contact (IBC) solar cells developed by Stanford group and further commercialized by SunPower, and SHJ solar cells developed by Sanyo in Japan. The chart is missing Metal Wrap Through and Emitter Wrap Through technologies which also have high efficiency potential, but started to get to 20% efficiency only recently[12].

It should be noted that each technology has many variations. For example, one modification of PERC design is Passivated Emitter and Rear Locally diffused (PERL) cell where rear local contacts are additionally passivated by p+ boron diffusion. Industrial PERC cells instead have Al/Si local contacts which are formed by either laser firing or ~400 ^{o}C annealing of printed or evaporated Al. Alternatively, the entire rear surface may have additional boron doping formed either by diffusion or implantation which may or may not be passivated by dielectric. In their turn, bifacial cells may have metallization formed by screen printing of Ag and Ag/Al pastes instead of Cu plating.

In PERC cells (device a), efficiency improvement is primarily due to the increase of V_{OC} which is achieved by replacing a continuous Al BSF with dielectric passivation having local Al BSF[13]. In addition, the front surface usually has a higher sheet resistance emitter, with or without higher doping underneath metal contacts, which is usually passivated by thermal SiO_2 or AlO_x.

Three other cell technologies rely on n-type wafers which are free from B-O degradation and can potentially achieve higher efficiency[14]. It should be noted here

that there have been several reports recently describing p-type CZ material with very low oxygen concentration grown byeither continuous CZ[15]or magnetic CZ[16]. Providing such material can be produced on a scale, there will appear to be more high efficiency industrial solar cells on p-type wafers.

Bifacial cells (device b) with passivated diffused carrier collectors and either Al/Ag printed grid or Cu plated grid from both sides of the device are being developed by ECN[17] and TetraSun[18]. The cells from TetraSun are notable for achieving 700 mV V_{OC} by using n-type wafers which is not available for the cells on p-type wafer with similar design. An additional advantage of this approach is the use of Cu plated metallization which can achieve very thin fingers (down to 30 μm) with low resistance increasing both J_{SC} and FF. Plating, however, is currently rarely used in high volume manufacturing due to a number of technological issues[19].

Another class of solar cell technologies is IBC cells (device c) where both carrier collectors are formed at the rear side of the cell[20][21]. This design avoids front metal shading losses and allows the use of thick plated Cu metallization which reduces resistance losses. A manufacturer of IBC solar cells, SunPower, currently holds PV module efficiency record. Their X-series modules using Gen III IBC cells with >24% efficiency[22] were reported to have 21.5% efficiency[23]. The main drawback of IBC technology is a high number of manufacturing steps and the use of specialized equipment. This can be one of the reasons for SunPower modules to be the most expensive on the market.

The last technology in the list is SHJ cells (also known as HIT cells which is a brand name by Panasonic). In SHJ cells, carrier collectors are formed by depositing thin

a-Si layers on both sides of the cell. A transparent conductive oxide (TCO) layer at the front surface (usually Indium Tin Oxide (ITO)) serves as an antireflection coating, a contacting layer between a-Si and metal electrodes and a lateral conductivity layer. A TCO at the rear surface is usually used for making good ohmic contact and ensuring good internal reflectance of IR light. Panasonic currently holds the efficiency record among large area c-Si solar cells with 24.7% efficiency[24]. The distinguishing feature of SHJ solar cells is the almost perfect surface passivation by (i)a-Si allowing very high V_{OC} (higher than 730 mV in commercial devices). Silicon heterojunction cells are the main topic of this dissertation.

1.3 Approaches to Ultra-thin Solar Cells

Silicon heterojunction technology is particularly important in order to achieve high efficiency on thin wafer. Making solar cells on ultra-thin wafers is another direction of R&D efforts which can change PV industry. Thinning the wafer can be beneficial for two reasons: first, it may reduce the consumption of expensive c-Si. Second, the cells made on thin wafer can potentially have higher efficiency since thinner cells may have higher V_{OC}.

Two critical requirements in achieving high efficiency on thin wafer are advance IR light trapping and very good surface passivation[25]. Light trapping in thin c-Si cells is important since optical path length of IR photons may reach several hundreds of microns. These photons, therefore, may escape the device after multiple internal reflections through the front surface reducing generation current. Very good surface passivation is important since in thin cells the contribution of surface recombination in

Table 1-2. Review of various approaches to the manufacturing of thin kerfless Si wafers. Two main technologies are ion implantation followed by cleaving and epitaxial growth followed by a lift off.

	AstroWatt [30][31]	Solexel [32]	Crystal Solar [34]	SiGEN [33]	Twin Creeks	Ampulse [38]	ISFH [29]
Technology	Plating and cleaving	Epi on porous	Epi on porous	H^+ implant and cleave	Implant and cleave	Epi	Make pores and cleave
Thickness	20-40	40-60	40-80	20-120	n/a	n/a	20-40 μm
Bulk quality	CZ	Epi	Epi	CZ	CZ	Epi	Porous
Bulk lifetime (us)	n/a	>300	100-200	~200	n/a	n/a	1-3
Best cell efficiency	14.9	20.1	16.7	16	n/a	n/a	19.1
Area (cm^2)	80-100	243	156	239	n/a	n/a	4
Development state by 2013	Closed	R&D	R&D	R&D	Closed	Closed	R&D

overall recombination losses increases, and moderately passivated surfaces may pull the efficiency down.

Table 1-2 summarizes the most notable results achieved by various R&D teams developing thin wafer technologies. Several groups have also attempted to integrate SHJ technology with their thin wafer process[26][27]. The performance of the reported devices, however, is not high. The record 20% efficiency cell on very thin wafer is made by Solexel which relies on IBC approach and epitaxial growth of the substrate[28]. 19.1% efficiency was also reported by ISFH where they integrated PERC design with their porous silicon process[29]. Despite moderate performance of the reported solar cells, silicon heterojunction technology is probably the best choice for making a cell on a thin wafer since it provides the best device level surface passivation which is sufficient to

achieve higher V_{OC} with thinning the wafer. Two other important advantages related to using thin wafers are low temperature and low stress processing. Both may relax the requirements of the material used for bonding thin wafers to the carrier.

Similar to other modifications of the standard screen printing technology, the benefit of using ultra-thin substrates will be a tradeoff between manufacturing cost and performance.

Back in 2008, the work on ultra-thin substrates was stimulated by the very high price of poly Si. At that time,the cost of Si wafer accounted for more than 30% of the PV module cost with approximately 2/3 of the wafer cost coming from ingot growth and wafering. In addition, Si wafer manufacturing consumed the major fraction of energy used to make PV modules increase energy payback time. Instead of wire sawing, lifting off thin wafers from a crystalline substrate could potentially reduce c-Si material cost lost to kerf, which is usually between 120 and 180 μm thick depending on the sawing technology. Epitaxial growth could also potentially provide cost reduction since in this approach the substrates are obtained directly from silane bypassing the growth of poly Si and pulling CZ ingots.

In 2010, however, with the expansion of poly-Si manufacturing capacity primarily in China and Korea, the price of poly-Si has been reduced from $400/kg in 2008 to as low as $30/kg in 2013. As a result, the advantages of kerfless approaches were leveled to a big extent while most manufacturers have failed to scale their technologies and compete with the substrates based on ingot casting and wire sawing. Presently, the use of thinner substrates in order to reduce the consumption of expensive c-Si is of interest for the manufacturers of high efficiency solar cells based on high quality n-type CZ material

which can be up to three times more expensive than p-type material. In the future, however, the cost of n-type wafers may also drop as the industry shifts towards n-type technology. With more players and increased competition in the field, advanced ingot growing technologies such as continuous CZ and magnetic CZ will become available to a larger number of manufacturers.

1.4 High Efficiency for Lowering the Cost of PV

Silicon heterojunction cells, similar to other high efficiency technologies, may require using more expensive specialized equipment. This necessity will increase capital cost and, hence, the cost of PV modules. This section compares high and low efficiency approaches to cost reduction. In low efficiency approaches, the performance is compromised in favor to using less expensive materials or simplified cell designs or less expensive manufacturing processes.

Presently, the PV module market is divided between three main technologies: the modules using high efficiency cells on mono c-Si wafers (18-22%), the modules using cells on multi c-Si wafers with moderate efficiency (15-18%),and thin films modules with relatively low efficiency (10-13%). For most PV installations, the technology that provides the lowest cost of generated electricity is chosen. In order to estimate the cost of PV electricity and compare it to the cost of electricity generated by other technologies, a parameter called Levelized Cost of Electricity (LCOE) can be used. LCOE is calculated using the following equation:

$$LCOE = \frac{(\$/\mathrm{m}^2{}_{PV} + \$/m^2{}_{BOS})}{\eta \times S} \times FinancingCost \tag{1}$$

whereη is module efficiency and S is the annual incident solar radiation.

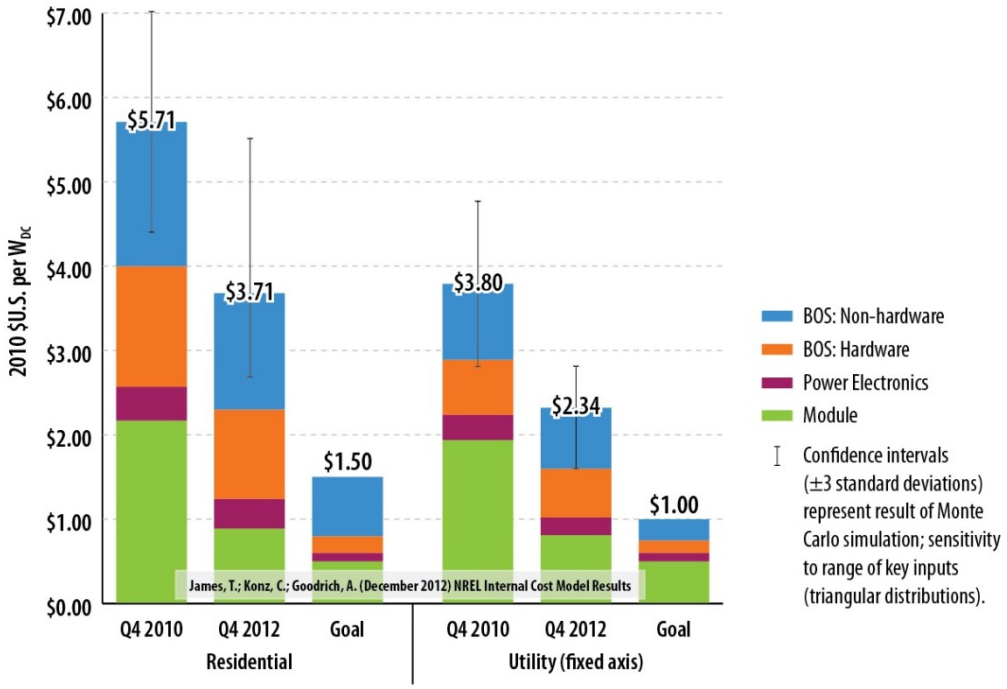


Fig.1-4. A comparison of PV system cost components in 2010 and 2012 [35]. The cost of the system dropped primarily due to the reduced cost of the PV module.

As follows from the equation, LCOE can be reduced by either reducing the cost of PV modules and Balance of System (BOS) components, or by increasing the efficiency of energy conversion. As was mentioned before, reaching higher efficiency is usually associated with more expensive materials and/or increased number of fabrication steps which add to the capital cost, equipment ownership, and factory space. Therefore, surplus energy output due to higher cell efficiency can often be leveled by the increased manufacturing cost, making it useless to implement higher efficiency technologies. However, recently, the cost structure of PV system has significantly changed due mainly to the reduced price of the PV modules which is in the \$0.5-\$1/W_p range for c-Si modules depending on the technology and manufacturer. The cost breakdown of a typical

utility scale PV system in 2012 is shown in Fig.1-4. Note that for smaller scale residential and commercial systems the relation between PV module and other non-hardware components can differ since smaller scale installations usually have more expensive system design and installation procedure. It follows that 60-75% of the PV system cost in 2012 is composed of several area dependent components such as the cost of land ownership, installation labor, wiring, etc. This fact makes high efficiency PV modules more competitive due to the higher power per square meter they can deliver. The choice between higher versus lower efficiency PV modules will depend on the area dependent components of the PV system which will depend on a particular installation project. The general trend is, however, towards higher efficiency technologies which can reduce area dependent non-hardware system costs.

1.5 History and Status of SHJ Technology

In the next two sections, the structure of SHJ cells is discussed and the recent developments in the area of SHJ cells are summarized. Then, in Section 1.7 different types of SHJ cells are reviewed.

The name “Silicon Heterojunction” is typically used to designate a wafer silicon solar cell where both carrier collectors are created by the deposition of thin doped a-Si films. Due to a high resistivity of a-Si, the wafer is then coated by a transparent conductive oxide (TCO) film which provides lateral transport of the collected carriers to the metal electrode grid. TCO also serves as an antireflection. Although the devices similar to SHJ cells have been reported previously[36][37], the first SHJ cell with the presently used design was invented and published in 1992 by Sanyo[39], where they

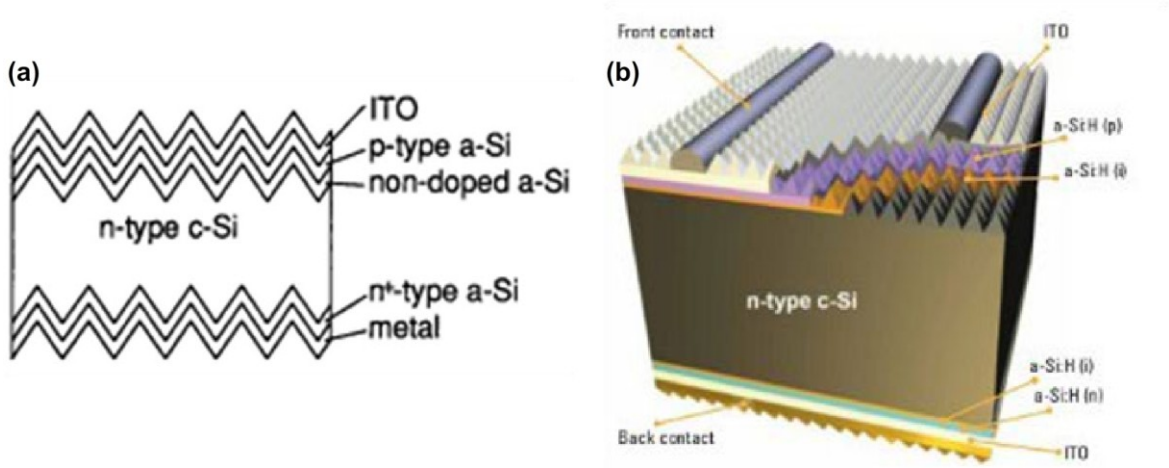


Fig.1-5. Schematic diagrams of SHJ cells from the literature. (a) The first published HIT cell by Sanyo [39]. (b) A contemporary SHJ cell by Roth & Rau [40]. The development in SHJ cells was primarily in the improvement of the properties of thin films and front metal grid. The structure of the device remained essentially unchanged.

found that using a thin layer of intrinsic hydrogenated amorphous silicon ((i)a-Si:H) in between c-Si wafers and doped a-Si carrier collectors provides a superior surface passivation and increases V_{OC}.

The structure of the first Sanyo cell, which achieved 614 mV V_{OC} and 18% efficiency, is shown in Fig.1-5 with the structure of a contemporary SHJ cell from Roth & Rau[40]. Since the first publication in 1992, the design and fabrication methods have not changed significantly. However, each fabrication step and the interactions between all steps have been heavily optimized to minimize recombination, optical, and series resistance losses. Two key improvements that allowed high efficiency SHJ cells in mass production were the ultra-passivation of the c-Si surface by (i)a-Si:H to allow V_{OC} up to 730 mV in commercial devices and the introduction of polymer based Ag pastes that ensure sufficient conductivity at low curing temperatures. The main advantage of SHJ technology over other high efficiency approaches is that the entire surface of the wafer is

passivated by (i)a-Si:H, while the junction is induced inside the wafer due to band bending. SHJ structure avoids the diffusion of dopants into the wafer and shields metal electrodes from the surface of the wafer by a-Si/ITO stack. Thus, very low overall recombination can be achieved. In addition to low recombination, the following features are usually claimed to be the advantages of SHJ technology over high efficiency cells based on diffused carrier collectors: (1) low temperature processing (< 250 ^{o}C thermal budget), (2) the lowest number of processing steps, (3) planar structure (except front metal grid), (4) natural bifacialism, and (5) low temperature coefficient (degradation of V_{OC} and efficiency per degree temperature increase).

Presently, over ten laboratories around the world have reported SHJ cells with >20% efficiency on either small or large area substrates[41]. Sanyo (which was recently acquired by Panasonic) now holds the efficiency record with the following independently confirmed parameters of 10x10 cm^2 solar cell : 24.7% efficiency, 750 mV V_{OC}, 39.5 mA/cm^2 J_{SC} and 83.2% FF[24].

1.6 The Structure of an SHJ Solar Cell

The structure of a conventional SHJ solar cell and a standard fabrication flow are shown in Fig.1-6. A standard SHJ cell is preferably made on n-type c-Si wafers with a bulk lifetime greater than 1 ms in order not to limit the performance by the bulk SRH recombination. The wafers are textured, cleaned, and a-Si films are deposited by plasma enhanced chemical vapor deposition (PECVD). TCO films, for example ITO, are then deposited by reactive magnetron sputtering from both sides of the wafer. Finally, Ag

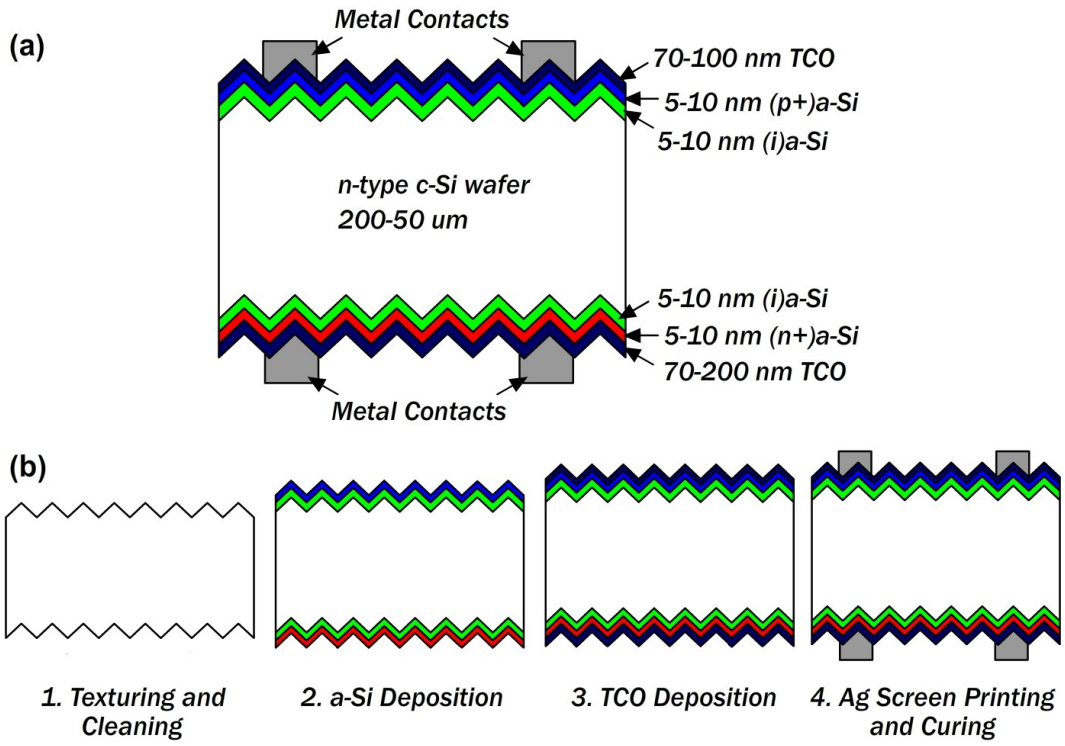


Fig.1-6. (a) The structure of a conventional SHJ solar cell using a-Si layers, TCO and screen printed Ag contacts. (b) A process flow showing three main fabrication steps. Note that a single step is usually defined as the process sequence using similar type of equipment. For example, cleaning step may consist of multiple cycles of wet chemical treatment. Also note that edge isolation can be done either by using the shadow mask during TCO deposition or by a wet or plasma treatment following TCO deposition.

paste is printed from both sides, which is followed by low temperature curing of the paste, usually below 250 ^{o}C.

The structure and fabrication of SHJ cells may have several variations the most notable of which are summarized in Table 1-3. One important option in fabrication of SHJ cells is using tunnel oxides, such as $SiO_2$and Al_2O_3 for surface passivation[42][43]. Using tunnel oxides may have two advantages: the absence of parasitic absorption compared to (i)a-Si and more reliable deposition process. The main disadvantage of tunnel oxides is that their thickness should be very carefully controlled since tunneling

Table 1-3. A comparison of the classical SHJ structure with a-Si carrier collectors, ITO transparent conductive layer and screen printed Ag metallization to various alternative designs reported in the literature.

	Sanyo HIT	Alternative	Developers
Passivation	Intrinsic	Tunnel oxides Al_2O_3, SiO_2	Silevo [42], ISE [43]
Junction	(p+)a-Si	(p+)μc-Si, a-SiC, GaP, etc.	IBM [59], ISE [45]
Meal	Printed Ag	Plated Cu	Kaneka[50], Silevo, EPFL [51]
TCO	ITO	ZnO, ITO:H, IO	Most of the labs
Wafer	n-type	p-type	EPLF [57], IBM [59]
Geometry	Front grid	IBC	IEC[60], INES[63], LG[62], ISFH[61]

probability is a strong function of the oxide thickness. Another option for the cell structure is the use of minority carrier collectors different from (p+)a-Si and (n+)a-Si. As in the case of using tunnel oxides, the motivation is to reduce parasitic absorption. Therefore, higher band gap films such as SiC_x and a-SiO_x:H are sometimes attempted as carrier collectors in SHJ cells[44][45][46]. A hybridization between SiO_2 and (i)a-Si:H is also possible. A-SiO_x:H layers were reported as passivating layers used in order to prevent epitaxial growth of a-Si on textured c-Si wafers[47][44].

One interesting opportunity in replacing (p+)a-Si emitters is growing III-V semiconducting films directly on a Si wafer[48]. In this case the surface can be strongly inverted suppressing recombination by the field effect without additional chemical passivation. A recent theoretical work predicted up to 710 mV V_{OC} on a solar cell with GaP emitter[49].

An important step towards lower cost and higher efficiency SHJ cells is the replacement of screen printing of the front Ag electrodes with high resolution Cu plating[50][51] or alternative Cu metallization technologies. Cu plating usually requires the formation of the barrier/seed layer on the TCO which can be done by using a patterning process followed by sputtering. Both will, however, increase the cost of a solar cell. The overall metallization cost will still be lower since Cu is 140 times less expensive than Ag. Additional advantages of Cu plating are higher conductivity and smaller finger width (down to 30 microns) compared to screen printed Ag fingers, which are usually limited by 90 microns in mass production. The advantage of Cu plating over screen printing of Ag is demonstrated in Table 1-4 by comparing 23.5% plated SHJ cells made by Kaneka[50] and 20% screen printed SHJ cell made by Roth & Rau[52]. Due to a low conductivity of Ag paste, Roth & Rau has to use the grid with five busbars to reach a reasonable value of fill factor which also increases optical losses.

A popular topic of research in the field of SHJ solar cells is the replacement of ITO with indium free TCO since several studies indicated that indium has a limited

Fig.1-7.5 busbar cell from Roth & Rau limited by high shading and series resistance.

Table 1-4. A comparison of Cu plated cell from Kaneka and Ag screen printed cell from Roth & Rau

	Eff (%)	Voc (mV)	Jsc (mA/cm^2)	FF (%)
Kaneka	23.5	737	**39.9**	**79.7**
Roth & Rau	20	730	35-36	77-78

availability and can potentially limit the scaling of SHJ technology[53]. Good results have been obtained with ZnO doped by either Al[54]or B[55]and with hydrogen doped indium oxide films[56]. These films can also be used in stacks with various ITO films in order to provide the best combination of electrical and optical performance. For example, a thin layer of ITO with high carrier density can be used as a contacting layer, while another low carrier density, low index, thicker TCO layer can be used for light trapping.

Several groups reported SHJ cells on p-type wafers[57][58][59]. Industrial p-type CZ material is, however, limited by boron-oxygen degradation[14]. Unless p-type material with very low oxygen density is available, mass production of p-type SHJ cells seems less attractive compared to n-type.

Finally, SHJ technology was combined with interdigitation of p- and n-type carrier collectors at the rear surface in order to integrate the advantages of SHJ and IBC solar cells. After the pioneering work by Lu et al.[60], SHJ-IBC cells have been reported by several groups with most notable results from ISFH[61], LG[62] and INES[63].

1.7 Recent Developments in SHJ Solar Cells

In this section the most notable results in the field of SHJ cells published in 2012-2013 are summarized. For earlier development see, a review paper by De Wolf[41]. The most notable results in 2013 came from Japan where Panasonic presented a 100 cm^2 SHJ cell with 24.7% efficiency which has become the highest efficiency large area c-Si solar cell[24]. The Panasonic cell had very high FF which implies that their device achieved very low surface recombination in the wide range of minority carriers density. As a result Auger mechanism dominated recombination not only at V_{OC} where carrier density is high

but also at maximum power point. This, together with very low series resistance, allowed 83.5% fill factor on large area SHJ cell (see the discussion in Section 6.5). Very impressive results were recently achieved by the collaborative group between Japanese Kaneka and Belgian IMEC which is developing SHJ cells with Cu plated metallization. Kaneka reported 24.2% SHJ cell on 156x156 mm^2 wafer which is notable not only for very high V_{OC} but also for >40 mA/cm^2 J_{SC}[64]. Compare, for example, with the record cell from Panasonic, which has achieved 39.5% $mA/cm^2$$J_{SC}$. The improvement in J_{SC} is most probably associated with using very thin Cu fingers, possibly <30 μm wide, which allowed reduction of shading losses. Several companies such as CIC and AU Optronics have recently reported rear planar junction SHJ cells with minority carrier collector located at the rear side of the cells. The cells from CIC and AU Optronics achieved >22% efficiency[65][66]. An important achievement was a demonstration of SHJ interdigitated back contact solar cell with 24% efficiency by LG[62] which was a significant breakthrough compared to the previous record cell made by Helmholtz Zentrum Berlin and ISFH[61]. The cell from LG, however, is a small area device using photolithographical processing. Note also that 24% efficiency was not yet confirmed by external entities. Silevo is another company that reached 22% efficiency[42]. Silevo is developing SHJ cells with tunnel SiO_2 and Cu metallization. Passivating the entire surface with a thin SiO_2 film allowed Silevo to achieve 730 mV V_{OC} which is comparable to the best devices based on (i)a-Si:H passivation. An interesting result was reported by EPFL, which published SHJ cell on p-type wafer with >21% efficiency[57]. The process developed at EPFL also allows n-type SHJ cells with 22%. They attributed lower performance of p-type SHJ cell to lower pFF caused by the difference in the capture cross

sections of minority electrons and holes in p-type and n-type devices. Aiming to reduce metallization cost and resistance losses caused by using resistive low temperature polymer Ag pastes, Meyer Burger is developing wire mesh metallization technique for SHJ cells. This technology is designed to replace 5 busbar metallization scheme Meyer Burger is currently using (see Fig.1-7). Very good results were achieved both on the cell level (21% efficiency) and on the module level (1% cell to module efficiency loss versus conventional 2-3%)[67]. Another company developing wire mesh metallization for SHJ cells is CIC. CIC recently demonstrated SHJ modules with 79% FF and 90% reduction of Ag usage[69]. Finally, Roth & Rau reported achieving 21% mean efficiency in their pilot production line where they are developing high throughput PECVD and sputtering equipment for SHJ manufacturing[68].

1.8 Thesis Objectives, Novelty and Structure

1.8.1 Introduction

As was previously discussed in Section 1.4, the PV industry needs to further improve the efficiency of solar cells in order to increase the power delivered per unit area occupied by the PV system. Higher power density will reduce the cost of area related components of the balance of system which is presently the most efficient way to further reduce the cost of PV electricity.

SHJ solar cell is a very promising technology in the achievement of high efficiency in mass production. However, presently Panasonic is the only manufacturer of SHJ solar cells while other players are still at small scale R&D stage. Moreover, although the record efficiency of SHJ solar cells in R&D is quickly approaching 25 %, the cells in

Panasonic's large scale manufacturing lines are usually between 20% and 21.5% with the module efficiency being at 18-19% level (see Table 1-5)[70]. Panasonic, for example, still does not have >20% module on the market while the efficiency of their R&D cells reached 22% back in 2008.

Table 1-5. The performance of selected PV modules made by Panasonic using SHJ cells demonstrating the difference between record R&D HIT cells and HIT cells produced on a scale [70]. All modules are made of 72 125x125 cm^2 cells.

	Module		Cell	
Module ID	V_{OC} (V)	I_{SC} (A)	V_{OC} (mV)	J_{SC} (mA/cm^2)
HIT-215N	51.6	5.61	716.7	36.67
HIT-220A	52.3	5.65	726.4	36.93
HIT-225A	53	5.66	736.1	36.99
HIT 235S	51.8	5.84	719.4	38.17
HIT-N235SE	51.8	5.84	719.4	38.17
HIT-240S	52.4	5.85	727.8	38.24

One of the reasons for relatively low performance of industrial SHJ cells may be a low electrical yield due to the variability of a-Si passivation quality. For example, the typical performance of several Panasonic modules shows that even the technology leader may have V_{OC} variation between 716 and 736 mV in its commercial process (see Table 1-5). At the same time, the majority of laboratories around the world are struggling to achieve high quality a-Si passivation of randomly textured c-Si wafers since the exact details of a-Si passivation process has never been reported. Additionally, it turned out to be an extreme challenge to transfer a heterojunction solar cell process to mass production tools since the interaction between different components of the cell is not clearly understood.

1.8.2 Objectives

The main objectives of this work are to develop a SHJ solar cells fabrication flow at the ASU Solar Power Laboratory pilot production line and use it as a workhorse 1) to study the interaction between different industry compatible fabrication processes, which can be used in the large volume manufacturing of SHJ solar cells, and their influence on the performance of the solar cell, 2) to identify a minimum set of optimization parameters and corresponding characterization techniques needed for quick and efficient optimization of SHJ manufacturing flow in a pilot production environment, 3) to understand power loss mechanisms the reduce the performance of a large area industrial SHJ solar cells and identify the foreground directions of further efficiency improvements.

1.8.3 Novelty

This dissertation developed the entire SHJ fabrication flow on large area 140 um and 50 um thick wafers which allowed solar cells> 730 mV and >750 mV V_{OC} respectively. It was demonstrated that state of the art a-Si process can be developed by using a design of experimental approach with only five optimization parameters: (i)a-Si:H passivation quality on polished wafers, bulk resistivity of doped a-Si films, transmission and conductivity of ITO films, and thicknesses of all films. This work also developed a wet cleaning process to allow ultra-passivation of randomly textured surfaces which was based on a sequence of nitric/acetic, piranha, and RCA-b oxidations. An in-depth study was done on the influence of textured surface morphology on the quality of a-Si passivation. Various surface features and different types of particles were identified as sources of poor passivation performance. A better understanding was

developed on the interaction of various process components along the fabrication flow. This includes reoxidation of H-terminated surface in air, the choice of the carriers for the deposition, the optimization of a-Si and ITO thicknesses on textured wafers, the use of various handling equipment, curing the passivation damage produced by sputtering of TCO and metal contacts, and the effect of low temperature Ag pastes curing on passivation. This work also developed an affordable photoluminescence tool using low pressure sodium bulbs as an excitation source which was used as an ultimate quality control tool to understand the uniformity of surface passivation at each process step. Finally, a comprehensive analytical model, based on a set of key measured material and device parameters, was built. The model was used to analyze power losses in large area industrial SHJ cells and propose the structure of SHJ cell which can further achieve 22% efficiency.

1.8.4 Structure

The thesis is structured in the following way: Chapter 3 goes through experimental setup to include the list of characterization techniques and the list of processing tools used to fabricate SHJ solar cells with the discussion of their basic theory and application to SHJ research. Chapter 4 is devoted to the optimization of a-Si deposition, which was done by using a design of experiment approach. The results of optimization study together with optical and electrical characterization of the films are presented. Chapter 5 describes a novel approach to the preparation of randomly textured Si surfaces to achieve uniform and repeatable passivation with ultralow recombination rate. Chapter 6 summarizes the electrical and optical performance of SHJ cells. Chapter 7

introduces a solar cell model based on the measured recombination and optical parameters. Further, the model is used to analyze the loss mechanisms in SHJ solar cell and discuss a roadmap to 22% and 25% efficiency devices. In Chapter 8, the performance of SHJ cells on ultra-thin substrates is discussed. Chapter 9 presents the passivation quality of a-Si/SiO_2/SiN_x stack which can be used at the front surface of IBC solar cells serving both as a passivating and antireflection layer.

Chapter 2
PROCESSING AND CHARACTERIZATION

Chapter 2 describes the characterization techniques and processing equipment used in this work. The three characterization techniques that were used most frequently for developing thin film deposition and surface passivation were: photoconductance decay to measure effective minority carrier lifetime of passivated wafers, spatial band to band photoluminescence imaging to measure the uniformity of passivation, and spectroscopic ellipsometry to measure the thickness of thin films. Complete solar cells were characterized by measuring light current-voltage characteristics, Suns-V_{OC} curve, quantum efficiency (QE),and spatial forward current electroluminescence. Textured surfaces were routinely characterized using SEM imaging and reflectance measurements. This work also used the standard characterization tools which can be found in many electronic labs: a four point probe, a probe station, optical microscopes, reflectometers, and profilometers.

Solar cell fabrication was done at the ASU Solar Power Laboratory pilot production line. The tools and equipment available for this work included wet benches with dedicated bathes, Applied Materials P-5000 cluster PECVD system, a KDF sputter tool and an AMI screen printer.

2.1 Characterization tools

2.1.1 Photoconductance Decay

Photoconductance decay (PCD) is a relatively simple, yet very powerful technique to characterize recombination properties of crystalline silicon material. PCD is the most often used characterization technique in this dissertation. The basic modern PCD setup with transient illumination by a flash lamp and eddy current detection of the change in photoconductance was developed in 1980s at Stanford[71]. Its first application was measuring emitter dark saturation current densities in high resistivity wafers with diffused carrier collectors. Later in 1990s a method using quasi-steady-state (QSS) illumination was introduced to measure low minority carrier lifetimes[72]. Finally, photoconductance was generalized for both short and long flash durations[73]. Presently, PCD is routinely used in almost every photovoltaic lab working with c-Si material. Unlike other characterization techniques, almost all PCD tools based on inductive coupling are supplied by a single company—Sinton Instruments. Therefore, PCD testers using inductive coupling are often interchangeably called "Sinton testers" or simply "lifetime testers."The basic operation of a Sinton tester is shown in Fig.2-1. In PCD, the wafer is exposed to a flash of light produced by a xenon bulb usually filtered using a 700 nm long pass filter to get more uniform excitation across the thickness of the wafer. During the flash, minority carriers are generated in the wafer increasing its conductivity. The change in conductivity is sensed by the RF coil located underneath the wafer. The intensity of light is also sensed by the reference solar cell. The measured temporal decay of photoconductivity ($\Delta\sigma(t)$) and light intensity are used to calculate effective minority

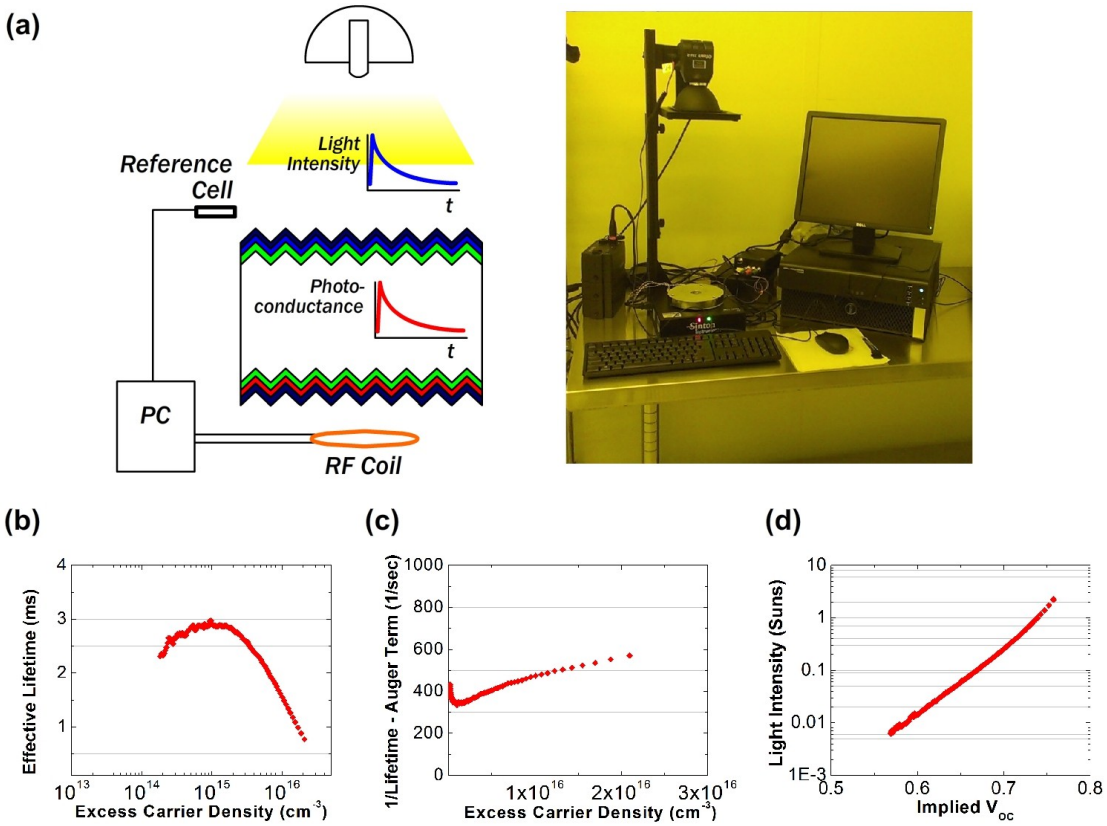


Fig.2-1. (a) Schematic diagram and a photo of a Sinton lifetime tester. (b) $\tau_{eff}(\Delta n)$ as measured by the Sinton tester. (c) A graph yielding J_0 of the samples with potential barriers. (d) Light intensity versus implied V_{OC} calculated from Δn data. From this graph implied V_{OC} at 1 Sun and implied pFF of the solar cell are obtained.

carrier lifetime (τ_{eff}) versus excess minority carrier density (Δn) which can further be used to extract various recombination parameters, such as the dark saturation current density (J_0) and bulk SRH lifetime (τ_{SRH}).

Detailed material properties can be measured by fitting $\tau_{eff}(\Delta n)$ curves with the simulated $\tau_{eff}(\Delta n)$ curves. For example, one can calculate the concentration of various impurities (Fe, Cr and O) in the bulk of the wafer[74][75] or different parameters of surface recombination, e.g. surface recombination velocity[76].

The effective minority carrier lifetime can be derived from the continuity equation assuming no current flow:

$$\frac{dn}{dt} = G(t) - U(t), \tag{2}$$

where recombination rate is expressed in terms of τ_{eff}: $U(t) = \Delta n(t) / \tau_{eff}$ and $dn(t) = n_0 + \Delta n(t)$. Thus,

$$\tau_{eff} = \frac{\Delta n(t)}{G(t) - d\Delta n(t)/dt}, \tag{3}$$

where $\Delta n(t)$ is calculated from the measured $\Delta\sigma(t)$ and G(t) is calculated from the light intensity measured by a reference cell.

Most measurements in this work were done in transient mode, where the flash duration (~0.2 ms) is much shorter than the excess carrier decay lifetime (~ 2-10 ms). Therefore, the generation term in equation (3) can be neglected. The method, however, is only suited for high lifetime samples (with $\tau_{eff} > 0.5$ ms). Therefore, several samples with low τ_{eff} were measured in a quasi-steady-state mode with slow flash intensity decay which allows the measurement of samples with short τ_{eff}.

With the known Δn and $\tau_{eff}(\Delta n)$, two additional recombination parameters can be calculated. One is surface saturation current density (J_0) which is a standard parameter used to evaluate the recombination properties of the device regions having potential barriers with exponential forward current, e.g. p-n junction, p-p+ junctions or the barrier induced by the charges built into dielectric films[77][78][79]. J_0 can be calculated from equation (4) by finding a linear fit to the function $f(\Delta n)$ at the injection level close to V_{OC}, where $\Delta n >> N_D$.

$$f(\Delta n) = \frac{1}{\tau_{eff}} - \frac{1}{\tau_{Auger}} = \frac{1}{\tau_{SRH}} + \frac{2J_0}{qn_i^2 W}(N_D + \Delta n) \quad (4)$$

Note that an accurate estimation of J_0 will require using an effective intrinsic carrier density, $n_{i,eff}$, which is a function of band gap narrowing and therefore depends on the carrier density in the device. The Schenk band gap narrowing model is usually used to calculate $n_{i,eff}$[80].

Another two important parameters obtained from photoconductance decay measurement are implied V_{OC} (iV_{OC}) and implied pFF (ipFF). iV_{OC} is determined by the separation of the quasi Fermi levels written in terms of carrier densities:

$$iV_{OC} = \frac{k_B T}{q} \ln\left(\frac{(n_0 + \Delta n)(p_0 + \Delta n)}{n_0 p_0}\right) \quad (5)$$

ipFF can be found from the implied IV curve which in its turn is calculated from the Suns-iV_{OC} curve using a superposition principle[81]. In order to get an accurate estimation of both iV_{OC} and ipFF the generation current (which gives the generation rate at 1 Sun light intensity) representing the light trapping of the actual solar cell should be used. In addition, a precise measurement of wafer thickness and bulk resistivity will be required.

The symmetrical structure of SHJ solar cells is ideally suited for in-line characterization by PCD where a RF coil and a flash light source can be conveniently located underneath the conveyer belt. τ_{eff} can be measured after a-Si deposition as well as after ITO deposition giving the recombination properties of the solar cell at multiple steps during the manufacturing sequence. These measurements can be used as one of the quality control methods. An example of the measured $\tau_{eff}(\Delta n)$ data is shown in Fig.2-1 a.

2.1.2 Suns-V_{OC}

Once the junction separating the carriers is created, the device can generate a potential difference, which can be probed. Providing metal probes can make an ohmic contact with the terminals of the solar cell. Similar to the effective minority carrier lifetime, the voltage measured at open circuit for different light intensities provides information about recombination properties of the solar cell[82][83]. Thus, V_{OC} at 1 Sun, pseudo fill factor and also the injection dependence of the ideality factor can be obtained.

In a conventional diffused junction solar cell the Suns-V_{OC} curve can be measured once an Al BSF is formed at the rear side of the wafer. On the front surface a sharp probe can punch through the layer of SiN_x and achieve good contact with a phosphorus emitter. In the case of SHJ cells, Suns-V_{OC} is measured after ITO deposition. A junction is

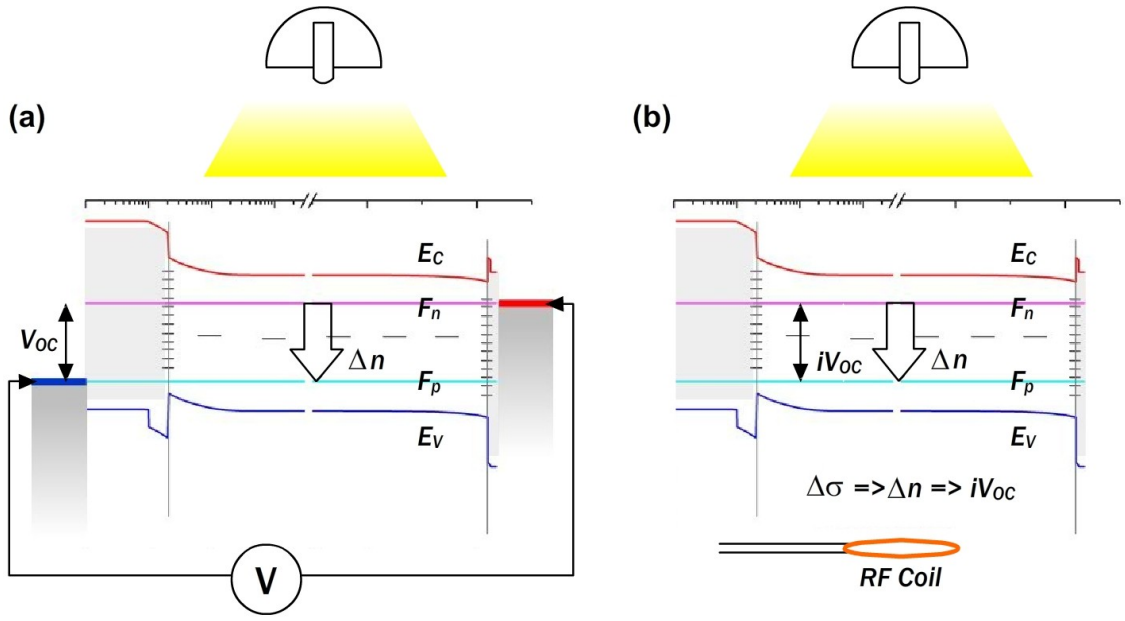


Fig.2-2. Band diagrams of SHJ solar cell at V_{OC} illustrating the relation between (a) Suns-V_{OC} measurement and (b) lifetime measurement. In both cases an excess minority carrier density generated by light is sensed. It is done either by measuring potential difference between the carriers separated by the junction (in Suns-V_{OC}) or by measuring the excess conductivity due to the excess carrier density.

formed during the deposition of the doped amorphous layers but the high resistivity of the amorphous layers makes reliable probing challenging. Both lifetime and Suns-V_{OC} measurements are sensitive to the recombination that takes place in the device and both measure the separation between the quasi Fermi levels. The difference between two techniques is that V_{OC} is measured when the carriers are separated, while excess photoconductivity can be measured without carrier separation. The interrelation between two techniques is illustrated in Fig.2-2.

Note that in lifetime tester the measured carrier density is averaged over the area of the RF coil. Note also that local measurement of V_{OC} will depend on regional isolation by series resistance. For example, after metallization, the voltage may be the same

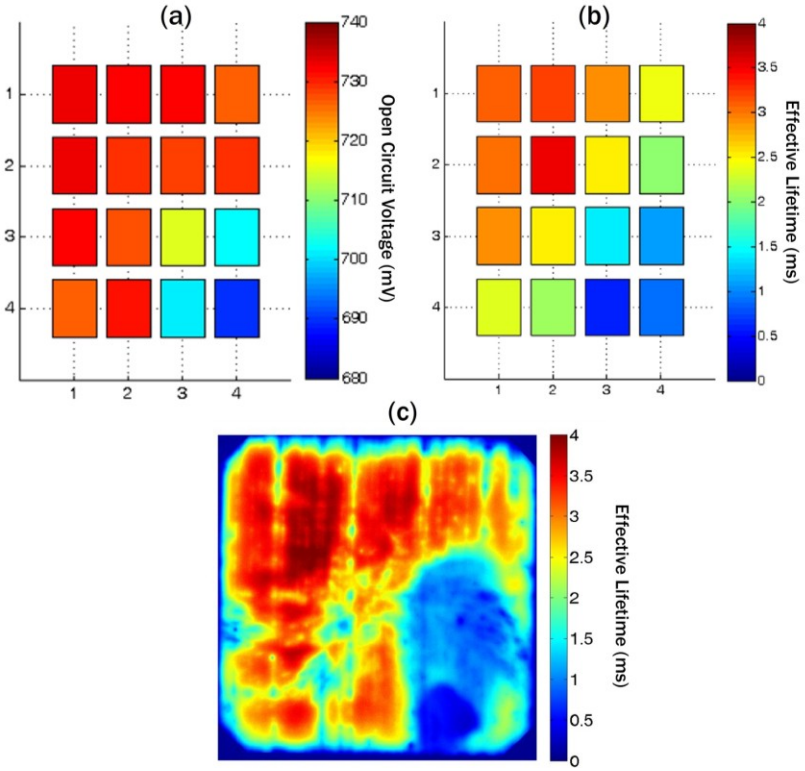


Fig.2-3. A comparison of uniformity maps measured by (a) Suns-V_{OC}, (b) Sinton tester and (c) PL. The V_{OC} of the complete solar cell was 719 mV.

everywhere on the cell. So the lateral resolution of voltage depends on the lateral resistance of the diode with higher resolution possible before metallization and with high lateral sheet resistance. For a more detailed discussion about reciprocity between lifetime, Suns-V_{OC} and implied IV curves the reader is referred to PhD dissertation by Kerr[84].

One challenge in using Suns-V_{OC} curves to evaluate the V_{OC} of the final SHJ cell is a nonuniformity of passivation, which can be responsible for 5-10 mV difference in the local V_{OC} across the wafer. The map of the local V_{OC} measured by the Suns-V_{OC} compared to the PL and lifetime maps and a corresponding final V_{OC} of one of the defected SHJ solar cell prepared during this work are shown in Fig.2-3.

2.1.3 Light IV curves

In this work, all light IV curves of SHJ cells were measured using a flash solar cell tester by Sinton Instruments. The tester is using a xenon flash bulb that produces a spectrum very close to the AM1.5G. A set of filters and diffusers are used in order to achieve Class A spectrum and uniformity at the solar cell plane. The tester was calibrated by using full area screen printed solar cells measured at Sinton Instruments. Later in this work, a screen printed cell measured at NREL was used for intensity calibration.

The probing bars used in the tester are 3 mm wide therefore providing significant shading of the active cell area. In order to compensate for the shading caused by the probing bars, the J_{SC} of a solar cell was first measured using multiple probes contacting the edges of the busbars without any shading as shown in Fig.2-4. Then, the cell was contacted by the probing bars and the light intensity was increased above 1 Sun to get the J_{SC} measured without shading. Note that narrow probing bars which are, for example,

used at NREL can provide only 0.3 mA/cm^2 so that screen printed cells could be measured without adjusting light intensity.

One important advantage of using flash IV testers from Sinton Instruments is that they are designed to compensate for the capacitance effects known to occur when measuring devices with V_{OC} > 700 mV using flash light sources[85]. The testers are therefore suited to measure large area high voltage SHJ cells.

Besides the basic characteristics of a solar cell, such as J_{SC}, V_{OC}, FF, and efficiency, the tester also measures a pseudo IV curve, which is obtained from the Suns-V_{OC} measurement. The pseudo IV data can be used to conveniently obtain shunt and series resistances of a solar cell. The slope of the pseudo IV curve at low voltages (0.3-0.4 V) provides the shunt resistance. The series resistance is extracted by comparing the pseudo IV curve with the actual IV curve[86][87]. There exist other methods to measure series resistance. In one method series resistance is obtained from the IV curves measured at two different light intensities[88]. In another method series resistance is measured by

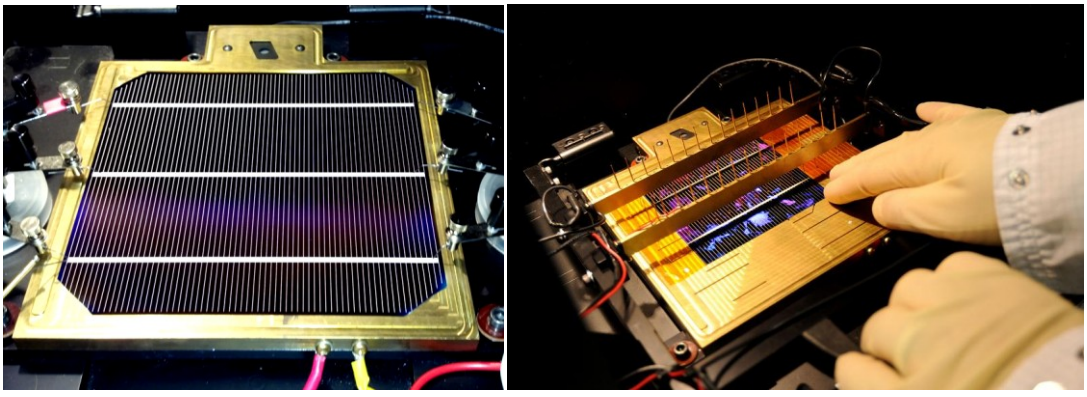


Fig.2-4. Left – measuring J_{SC} of a solar cell with screen printed grid using 6 current probes. Right – measuring IV curve of a solar cell with 3 mm wide probing bars.

comparing the actual IV curve to the J_{SC}-V_{OC} curve[86]. For the comparison between different methods, the reader is referred to the study by Pysch et al.[89]. The pseudo IV curve also yields a pseudo FF, which is a FF of a pseudo IV curve at its maximum power point. pFF is a direct indicator of the ideality of the dominant recombination mechanism at the maximum power point injection level (see the discussion in Section 6.5). In this work, the solar cells were evaluated by comparing the maximum theoretical FF based on the intrinsic recombination in the solar cell (Auger and radiative) with the pFF from the Suns-V_{OC} and with the actual FF.

2.1.4 Quantum Efficiency

By definition, the quantum efficiency (QE) of a solar cell is the ratio of the number of the incident photons to the number of the collected electron-hole pairs. It is therefore a measure of both the optical properties of the solar cell and the collection probability of the generated electron-hole pairs. QE is frequently measured using a white bias light, which provides constant illumination of the solar cell during the sweeping of the wavelength of the excitation beam. The bias light brings the operation point of the solar cell during QE measurement can be brought close to its actual operation point under one sun illumination. In other words, light bias will increase average carrier density in the solar cell to the values similar to those experienced during solar illumination. Biasing a cell may be important in case the dominant recombination mechanism changes at maximum power and open circuit as compared to the short circuit (in other words, from higher injections at V_{OC} towards lower injections at J_{SC}).

One usually distinguishes between internal and external QE, however for the internal QE only the photons absorbed in the cell are considered an input (i.e. the reflected photons are subtracted). For the detailed QE analysis of SHJ cells made in this work the reader is referred to Section 6.4.

The QE of a complete solar cell can be measured either by focusing the beam in between the fingers (usually having 1.5-2.5 mm spacing), or by using a large area beam which will interact with the screen printed grid which may cause undesired effects associated with the scattering of light by metal fingers. Since the current generated by the monochromatic light is weak, the QE of an SHJ solar cell can be measured prior to metallization but after the TCO layer is deposited. Sheet resistance of the TCO is usually between 50 and 90 Ohm/□, which is low enough to collect the photogenerated current by the probe positioned near the illuminated area. All QE curves reported in this manuscript were obtained after metallization with the light beam focused in between the fingers. Although QE curves of non-metallized SHJ cells are not reported here, they were frequently used to optimize the thickness of a-Si films. In this thesis, QE was used primarily to evaluate parasitic absorption of visible light in the front a-Si and ITO films and to analyze the losses in IR part of the spectrum. For the review of the capabilities of QE analysis the reader is referred to the publications by Brendel[90].

2.1.5 Electroluminescence and Photoluminescence

Fig.2-5 shows band diagrams of a solar cell demonstrating the principles of spatial band to band photoluminescence (PL) and electroluminescence (EL). EL of silicon solar cells was first reported by Fuyuki[91] in 2005 and was intensively studied by

several groups. EL was applied to generate spatial maps of the diffusion lengths[92][93], local shunts[94], surface dark saturation currents[95]and series resistances[96][97].

In an electroluminescence setup, the solar cell is forward biased to obtain the forward current equal to the maximum power point current. Recombination of the minority carriers in conventional c-Si solar cells is dominated by the bulk and surface SRH recombination with a small contribution of Auger and even smaller contribution of radiative recombination. However, radiative recombination produces sufficient number of photons to be detected by a photo camera using a cooled Si CCD detector within the reasonable acquisition time.

EL uses the fact that radiative recombination is proportional to the local

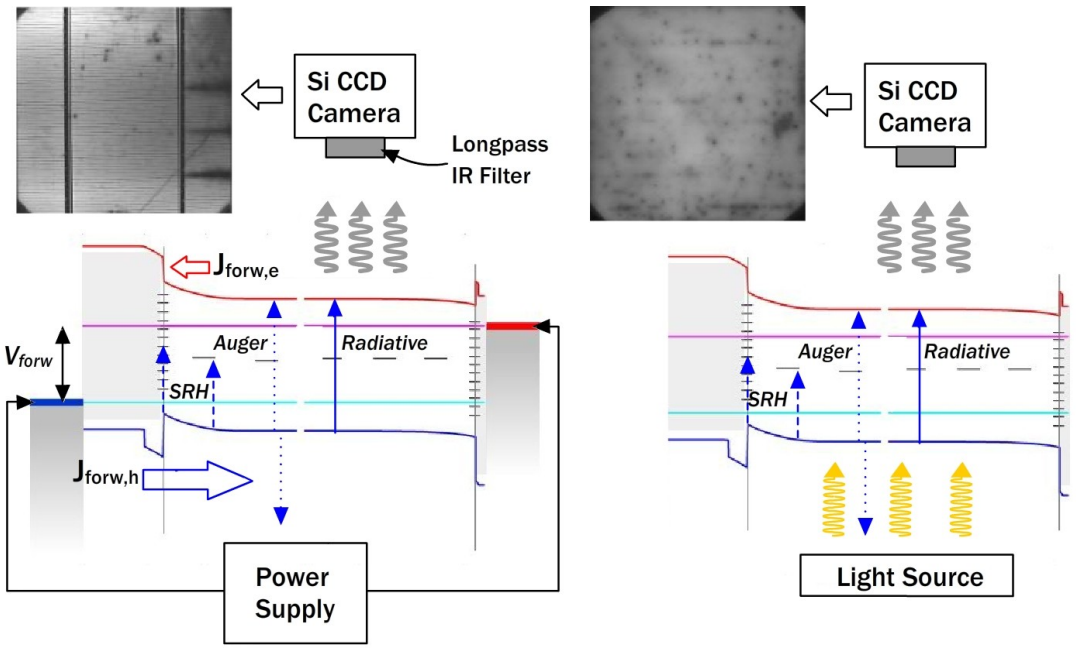


Fig.2-5. Schematic diagrams showing the principles of electroluminescence (left) and photoluminescence (right) operation. Blue arrows symbolize recombination processes taking place in the device. In EL excess carriers are injected into the bulk from the external power supply, while in PL excess carriers are generated by light.

concentration of the minority carriers which in its turn is proportional to the local SRH recombination and local junction bias determined by the local series resistance. Thus, the contrast on EL images is due to either local series resistance or local recombination. One additional source of contrast can be the various optical effects locally changing the emission of IR light, for example, shading or surface texture. As stated above, a number of methods have been developed to decouple resistance and recombination on EL images[96][97]. In this work, however, a simple approach was used, where EL images obtained at very low forward currents (0.7mA/cm^2) and longer acquisition times (~60 sec versus 0.5 sec for 36 mA/cm^2 current) were considered to be free of series resistance effects. The main drawback of this approach is that recombination mechanisms at lower injections may differ from the recombination at maximum power and open circuit. Therefore the difference between high current and low current EL maps may not only be due to R_S.

In photoluminescence the minority carriers are excited by an additional light source instead of being injected from the external circuit through the junction. A pioneering work in using spatial PL for silicon solar cells was done by Trupke et al.[98] and was mastered by other groups as well[99][100]. In fact, both EL and PL have become standard characterization tools in Si solar cell R&D and production with turnkey tools available from multiple manufacturers.

An in-house PL tool was developed specially for the work described in this dissertation[100]. PL systems usually use laser diodes with homogenizing optics or high power LED arrays as an excitation source. In this work, an experimental setup with three low pressure sodium lamps was used as a light source. In order to reduce parasitic IR

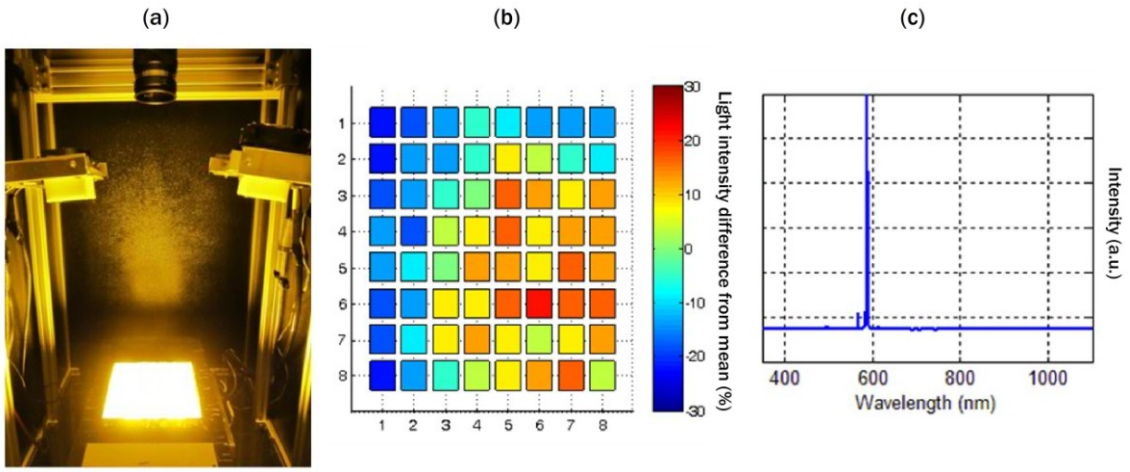


Fig.2-6. Photoluminescence system used in this work. (a) photo of the system showing IR camera, an enclosure with 3 low pressure sodium bulbs and 2 diode lasers. The lasers, however, were not used in this work; (b) uniformity of light produced by the sodium lamps at the location of the wafer; (c) spectrum of low pressure sodium light; note that undesired IR produced by the bulbs was filtered by a 4 mm thick Schott KG5 filter.

produced by the sodium lamp, a 4 mm thick Schott KG5 filter was positioned between the lamps and the wafers to filter light greater than 850 nm. The intensity of light after filtering was approximately 0.2 Suns. The camera used conventional long pass filters to cut the visible light. Light intensity uniformity and spectrum of the PL setup used in this work are shown in Fig.2-6. PL was measured after a-Si and ITO depositions and served as a tool to evaluate spatial uniformity of a-Si passivation and various processing imperfections.

2.1.6 Ellipsometry

Ellipsometry is a characterization technique where the change of polarization of the reflected light beam is used to evaluate optical and structural properties of the material[102]. A common application of ellipsometry in the semiconductor industry is the

measurement of the thickness of dielectric and semiconducting films or their stacks[103]. Ellipsometry provides measurement accuracy of film thickness down to 0.1 nm with short data acquisition times, which make it a perfect technique for developing new thin film deposition processes. Another application of ellipsometry is the measurement of optical properties of the films, usually in the form of the complex dielectric function (n,k) which is further used in optical models and ray tracers to evaluate the optical properties of a particular solar cell structure.

This work used ellipsometry to determine the thickness and optical constants of a-Si, μc-Si, SiO_2 and SiN_x films. A variable angle spectroscopic ellipsometer from J.A. Woollam was used[104]. The raw ellipsometric data, Ψand Δ, was measured in 300-1100 nm range at three incident angles: 70, 75 and 80 degrees. The data was fitted by building the optical models using the CompleteEASE program developed by J.A. Woollam.

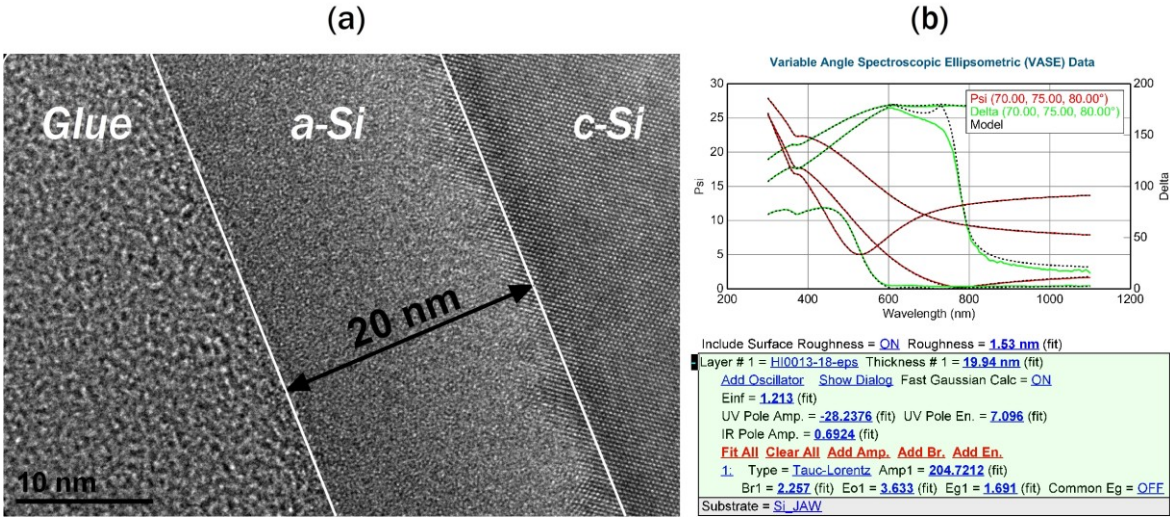


Fig.2-7.Calibration of Tauc Lorentz model for a-Si film. (a) TEM image of a-Si film on c-Si wafer, (b) the measured ellipsometric data and optical model with fitted parameters; the model yielded the thickness equal to 19.94 nm with 1.53 nm roughness. Mean square error (MSE) was equal to 0.7.

Optically transparent films were fitted using a Cauchy layer. Homogeneous a-Si films were fitted by using Tauc-Lorentz and Cody-Lorentz oscillators[105]. The fits with mean square error (MSE) below 1 could be obtained for most a-Si films.

Optical models were additionally calibrated by correlating the thickness measured by VASE and TEM. An example for (n+)a-Si film is shown in

Fig.2-7.

Fitting μc-Si films required using more complicated models due to their non-uniform structure[107]. A typical model used to fit μc-Si films as well as the fitted ellipsometric data are shown in Fig.2-8. The model consisted of a layer of Effective Media Approximation (EMA) composed of a-Si, μc-Si and voids with the percentage volume fraction of three media and the parameters of the oscillators were the fitting

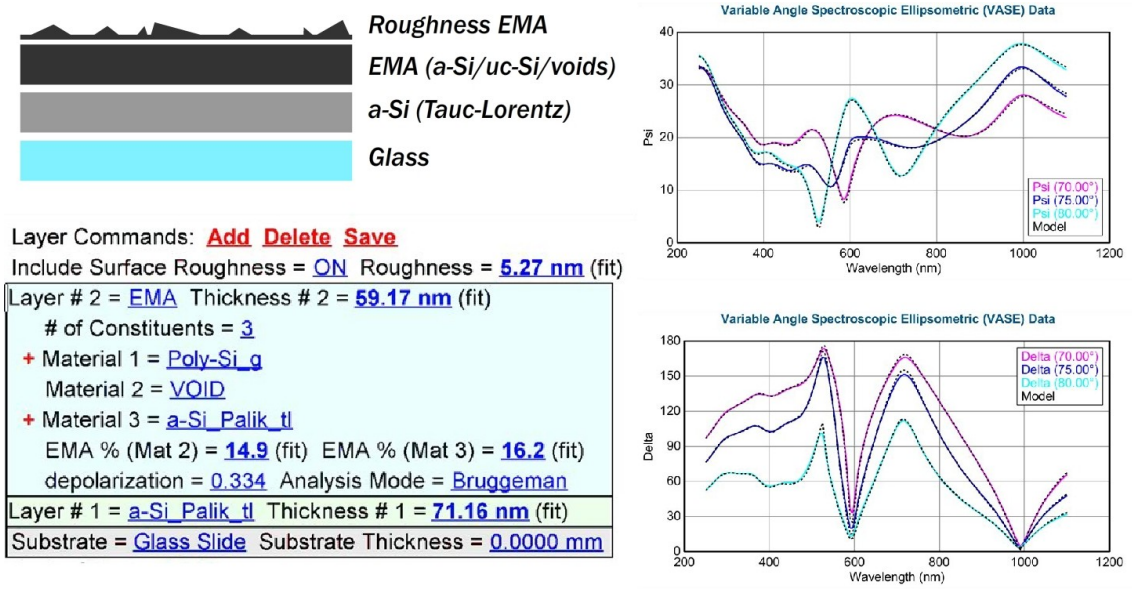


Fig.2-8. Ellipsometric model applied to fit the data measured on microcrystalline films. Note that microcrystalline films were deposited on (i)a-Si/glass substrates.

parameters. The fits with MSE below 3 were considered acceptable for most μc-Si films.

Several films, however, required more complicated modeling. In those cases the optical model introduced by Filonovich et al. was used[106]. The model consisted of two layers: a thin porous a-Si layer in the upper part of the μc-Si film followed by a thick crystalline layer which were simulated by the EMA layers. The cumulative thickness of the two layers and half thickness of the rough layer was considered as a total thickness of μc-Si film.

2.1.7 Raman Spectroscopy

Raman spectroscopy measures the spectrum of inelastically scattered monochromatic light interacting with different atomic vibrations. One of the applications of Raman spectroscopy is the measurement of the degree of crystallinity in a-Si/uc-Si

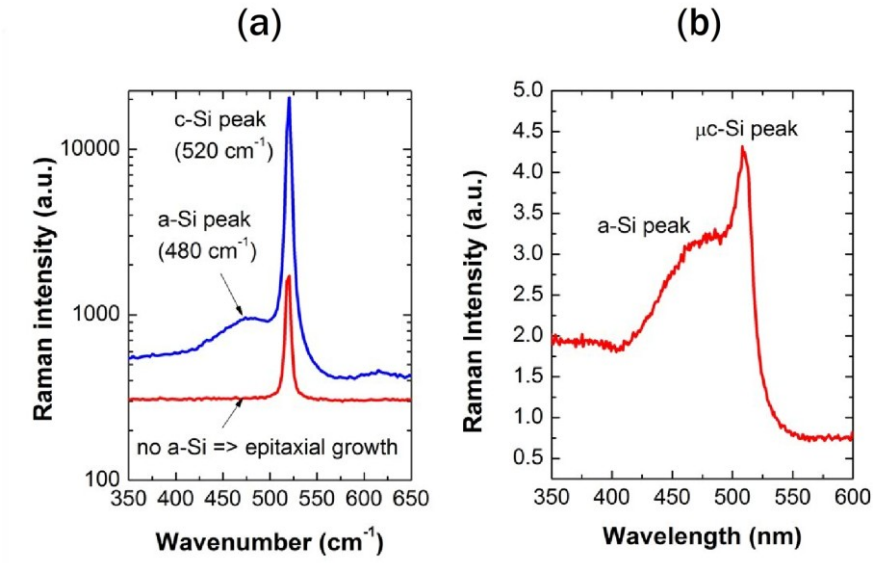


Fig.2-9. The intensity of Raman scattering showing characteristic a-Si, μc-Si and c-Si peaks. (a) Raman scattering can be used to identify epitaxial growth on textured wafers passivated with a-Si film; (b) an example of Raman signal measured on μc-Si film deposited on glass.

films[108]. a-Si and c-Si produce characteristic peaks at approximately 480 and 520 cm^{-1} respectively due to transverse optical vibration modes in a-Si and c-Si. A rather small additional peak at 510 cm^{-1} is due to the interaction of light with the boundaries of Si nanocrystals. The integrated intensity of the peaks can be used to calculate the fraction of crystalline phase in the film. In this dissertation, crystallinity fraction was calculated according to equation (6):

$$X_{c-Si} = \frac{I_{c-Si} + I_{GB}}{I_{c-Si} + I_{GB} + 0.8I_{a-Si}}, \tag{6}$$

where I are integrated intensities of the Raman shift and 0.8 is the ratio of the cross sections of a-Si and c-Si phases[109].

This work used Raman spectroscopy to determine crystallinity of thin Si films deposited on glass and also to detect epitaxial growth of a-Si on c-Si wafer. An example of Raman data for both cases is shown in Fig.2-9.

2.2 Processing

All processing steps except ITO sputtering were done in Class 10,000 clean room at the ASU Solar Power Laboratory. ITO was deposited in Class 10 clean room operated by the ASU Flexible Display Center. The clean room provided the ambient with 19 ^{o}C temperature and constant humidity. Maintaining constant humidity throughout the year was especially important in order to slow down reoxidation of H-terminated wafers and allow a convenient time gap between rinsing and drying the wafers after BOE etch and moving them into the deposition chamber.

2.2.1 Wet Chemistry

Wet chemical treatments used in this work are summarized in Table 2-1. This work also followed a particular set of rules to maintain the cleanliness of wet baths and prevent contamination of the wafers:

- All chemical hoods with the baths were decontaminated prior to being used at Solar Power Lab.
- Only semiconductor grade chemicals were used. The chemicals were routinely refreshed with the following periodicity: every week for RCA-a, RCA-b and Piranha solutions, every month for BOE solution, every three months for KOH solution. RCA-a, RCA-b and Piranha solutions were additionally spiked with H_2O_2 prior to the next use.

Table 2-1.The list of recipes used for wet chemical processing in this work.

	Purpose	Mixture	Temperature and time
Piranha	Organic clean	4:1, H_2SO_4:H_2O_2	110 ^oC, 15 min
RCA-b	Ionic clean	1:1:6, HCl:H_2O_2:H_2O	75 ^oC, 10 min
RCA-a	Organic clean	1:1:6, NH_4OH/H_2O_2/H_2O	75 ^oC, 10 min
BOE	Oxide etch, H termination	10:1, H_2O_2:HF with small addition of NH_4F	19 ^oC, 1 min
Concentrated KOH	Si etch	30%v KOH	85 ^oC, variable
KOH-IPA	Texturing	1%w KOH, 7%v IPA	85 ^oC, 50 min
Concentrated HNA	Si etch / Smoothing	1:1:1, HF:HNO_3:CH_3COOH	19 ^oC, 1 sec
Diluted HNA	Smoothing	10:750:250, HF:HNO_3:CH_3COOH	19 ^oC, 10 min
Nitric oxidation	Smoothing	750:250, HNO_3:CH_3COOH	19 ^oC, variable

- The bathes and rinse tanks were dedicated to a particular process or chemical. Only the recipes described in Table 2-1 were used to do a particular oxidation or etch.
- All wet treatments were followed by 10 min DI water rinse.

Fig.2-10shows the setup of the chemical hoods.

2.2.2 Texturing

The saw damage removal using a concentrated KOH etch was done in a stainless steel tank with a heater at the bottom of the tank. The level of the solution was maintained by the addition of DI water prior to processing the next set of wafers. The

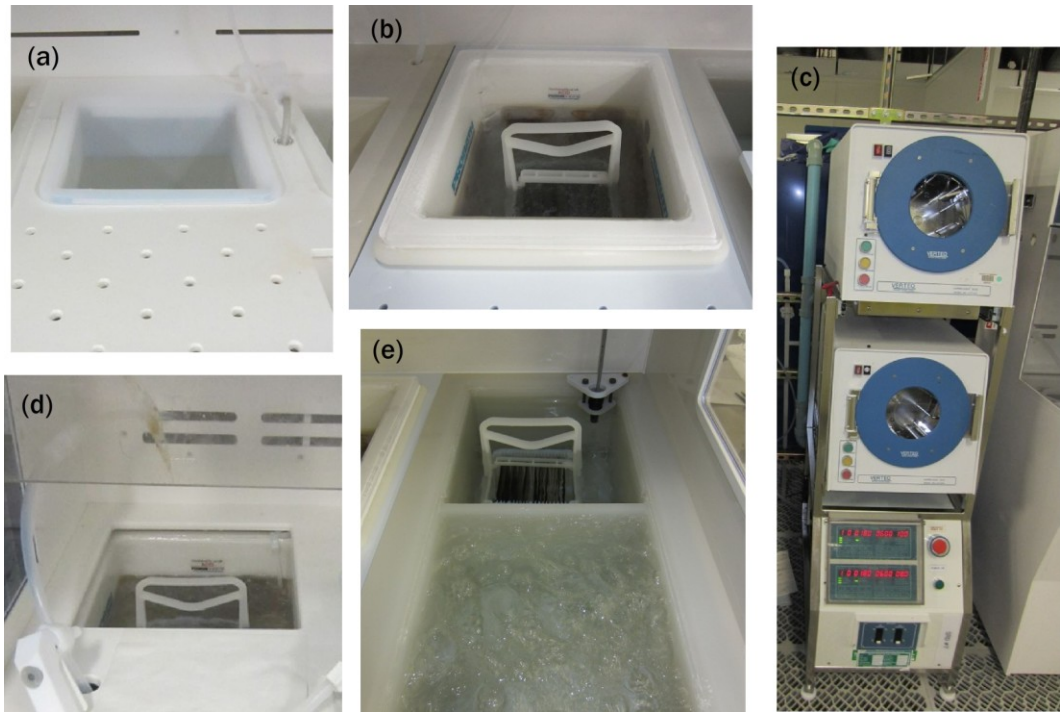


Fig.2-10. The photos showing chemical baths, rinse tanks and spin rinse driers used in this work. (a) a Teflon bath for BOE etch, (b) a quartz tank for RCA-b oxidation, (c) spin rinse dryers (d) a quartz tank for Piranha clean, (e) plastic tanks for DI water rinse; the tanks usually had two sections with faster and slower water circulation.

solution was manually stirred several times prior to etching until a stable temperature was reached.

Texturing was done with a standard KOH-IPA solution in a quartz tank. Repeatability and uniformity of texturing was one of the main issues in this work. Two main challenges in texturing are the depletion of KOH and evaporation of IPA. In an industrial environment, the concentration of chemicals can be monitored by the measurement of optical absorbance in a particular wavelength interval. In this work, however, such tools were not available. Instead, the KOH concentration was controlled using the etch rate. The KOH was refilled prior to the texturing of a new lot to maintain the etch rate. The IPA was assumed to evaporate completely if the tank was left opened for about an hour after texturing. Prior to the next texturing, the entire amount of IPA was added. In addition, a fresh texturing solution was conditioned by dissolving two 125 mm n-type CZ wafers. This was done in order to saturate the solution with silicates which was necessary to achieve uniform distribution of the sizes of pyramids and to avoid the formation of rough and porous layers (see Fig.4-11). Finally, all as-cut wafers were cleaned in Piranha or RCA-a solutions. The native oxide was removed in a BOE solution immediately before texturing. During texturing, the bath was closed with the lid. No stirring or agitation was used.

2.2.3 PECVD of Amorphous Silicon

PECVD is a popular chemical vapor deposition technique where the source gasses are dissociated using plasma ignited between the electrodes in the deposition chamber. The molecules, radicals, and atoms arrive to the surface of the substrate and after a short

surface diffusion settle at the surface site. Additionally they can take part in chemical reactions at the surface producing a thin film made of the materials supplied in a gaseous form. The properties of the film depend on multiple parameters such as substrate temperature, the gases and their flow rates, power and frequency of plasma, pressure in the chamber, substrate surface morphology, the presence of various contaminants in the chamber.

There exists a large variety of PECVD tools with many different configurations of deposition chambers (tube, shower head, in-line), confinement and location of plasma region (remote and direct), frequency at which the power supply creating electric field is operated (RF and VHF), and thermal systems (using resistive or lamp heaters). All the listed parameters may have a strong effect on the properties of the deposited film and should therefore be considered for a particular application.

In this work, a-Si films were deposited using an industry standard Applied Materials P-5000 cluster PECVD tool with three chambers dedicated to intrinsic, p- and n-doped films. The chamber used for the deposition of intrinsic a-Si films was additionally used to deposit SiN_x and SiO_2 for other lab needs. Along with the robotic handling, the chambers and susceptors were modified to accommodate standard 156 mm square solar wafers. After depositing approximately three microns of material, the chamber required cleaning in NF_3 plasma followed by coating the chamber walls with approximately 1 micron of SiN_x. Since the deposition was done on the substrates with various form factors (see below), 156 mm square crystalline silicon wafers capped with silicon nitride were used as the carriers for transferring the samples to the processing

chambers. Three chambers and the loadlock were pumped by four mechanical pumps. The baseline pressure and the pressure in the load lock were between 10 and 70 mTorr.

a-Si was deposited on both sides of the wafers which were manually flipped between the depositions. It was also found that low humidity allowed batch deposition of a-Si by using a single BOE etch with no performance degradation (see the discussion in Section 3.3). Each batch had 8 wafers. The size of the batch was determined by the size of the loadlock.

2.2.4 ITO and Metal Deposition

In this work, ITO that was previously developed for the applications in flexible electronics was used as a TCO. Although the properties of the film were not optimum for a SHJ solar cell, especially as a back IR reflector, no additional optimization was done due to the restricted access to the deposition tool. ITO was deposited by reactive sputtering using KDF 954 tool (former MRC).

Sputtering is a physical vapor deposition technique where the source material is knocked out from the solid target by heavy gas molecules such as Ar, ionized, and accelerated towards the target by the plasma ignited in the chamber. In the reactive sputter process, the knocked material additionally reacts with supplemental gasses, in this case O_2, in order to deposit the material with the required properties. Sputtering was also used to deposit metal electrodes for small area SHJ solar cells and TLM test structures. Cu, Ni, TiW, and Al metal targets were used for a particular application.

In addition to sputtering, metal electrodes were also deposited by evaporation. In evaporation, the source material is placed in a quartz crucible. Then the metal in the

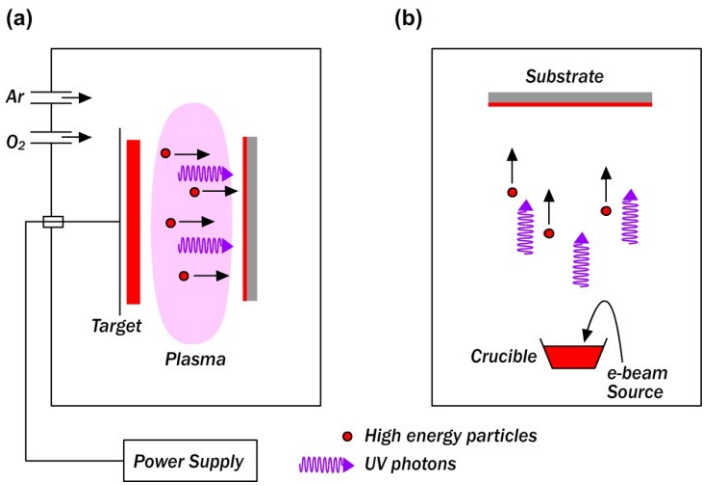


Fig.2-11.Schematic drawings of PVD tools showing the mechanisms damaging the passivation during metal deposition. Note that the amount of damage will depend on the intensity of UV radiation as well as on the energy and density of high energetic particles in plasma. It will therefore depend on a particular process and tool configuration. (a) sputtering, (b) e-beam evaporation.

crucible is heated up to reach the evaporation temperature either by the beam of electrons directed towards the crucible using a magnetic field, or by a resistive heater. The plate with the substrate is usually rotating to improve the uniformity of the deposited film. The schematic structures of the sputtering and evaporation tools are shown in Fig.2-11.

It should also be noted that the tools used in this work for metal deposition were limited by as low deposition rate (0.2 nm/s), small crucible size (limiting maximum thickness of the film per run), and small deposition area (designed for 4" round wafer). Therefore, metal deposition was only applied to the small area SHJ cells (usually 2x2 cm^2) and to various test structure, e.g. TLM patterns. Sometimes, approximately 300 nm of metal was sputtered at the rear side of large area SHJ cell where thickness uniformity does not play an important role.

A significant drawback of using physical vapor deposition for SHJ solar cells is the damage produced either by energetic particles or UV radiation[110]. Both mechanisms worsen the passivation by destroying Si-H bonds at the a-Si/Si interface and in the bulk of a-Si. After the deposition, however, the passivation quality can be restored by low temperature post deposition annealing, usually at 200-250^{o}C for 30-60 min. However, in certain cases the recovery was not complete. The most notable example was the degradation of the τ_{eff} in low carrier injection which could reduce the pFF. The damage was minimal in the case of metal sputtered on top of TCO, where TCO served as the protective layer absorbing particles and photons. Shielding, however, depended on the thickness of TCO. E.g. the effect was weaker when metal is deposited at the rear side of the cell which may have 200 nm of TCO versus ~90 nm of TCO on the front side.

2.2.5 Ag Screen Printing

Screen printing was used to form a metal grid on large area solar cells (> 100

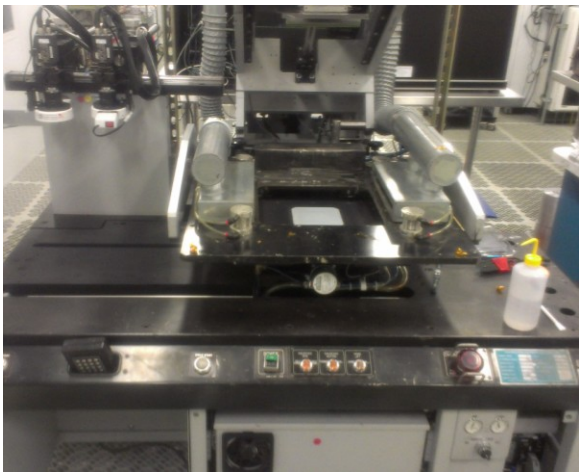


Fig.2-12. Screen printing setup showing AMI printer and a solar cell on the vacuum chuck.

cm^2). Due to the limitation of the metal deposition tools available in this work,all reported large area SHJ cells were bifacial, i.e. with the printed Ag grid from both sides. The front side performance of the bifacial SHJ cells was usually lower compared to the cells with full metal coverage due to the additional ITO sheet resistance at the rear plus less IR light reflected from the rear side back into the cell.

As the a-Si passivation is sensitive to high temperature (usually above 250 ^oC), a special low temperature Ag paste is used for SHJ solar cells. The paste for SHJ cells is similar to those used in organic electronic devices. However, the length of the fingers imposes additional requirements to the bulk conductivity or the paste. Unlike the pastes for high temperature annealing, the conductivity of low temperature pastes is not due to the sintering of Ag particles, but due to the conductivity of a polymer material, which becomes conductive after 200-250 ^oC curing for about 30 min.

A screen printer from AMI and the screens from PhotoStencil were used in this work (see photos on Fig.2-12). Typical printing conditions are summarized in Table 3-2.

Table 2-2.Typical settings of the screen printer and parameters of the screens used in this work.

Speed (inch/sec)			Snap off (mil)	Pressure ($lb/inch^2$)		Squeegee orientation
1-6			20-80	10-30		Vertical
Screen	Mesh	Mesh material	Emulsion thickness (mil)	Wire diameter (mil)	Bias	Finger opening (μm)
Type 1	325	stainless	0.8	0.9	300	100
Type 2	290	stainless	0.8	0.8	300	90

Printing was done in a print-flood mode. The pastes were stored in a clean room at 19^{o}C and were manually mixed for several minutes before printing. It should be noted that due to a small size of the market for SHJ cells, there are not many commercial pastes which can be used to make metal contacting grid. Most pastes used in this work were experimental pastes from different vendors.

The printed metal was cured at 200-250 ^{o}C in a muffle furnace in air ambient. The printed grid was tested for adhesion using a 'tape-test'. During the test,a Kapton tape was glued to the grid and then removed. The fingers with poor adhesion to the cell stay on the tape indicating problems with adhesion. Cu ribbons were soldered to the selected cells using a low temperature Sn-Bi solder with the melting point below 150 ^{o}C.

2.3 Substrates Used

The list of the used wafers and their IDs are given in Table 2-3. Double side polished wafers were used for lifetime optimization. High lifetime CZ wafers from two different vendors were used for making solar cells. CZ wafers also had different

Table 2-3. The list of wafers used in this work.

ID	grade	Size	Thickness (μm)	Resistivity (Ω-cm)	Surface	Orientation
W1	FZ	6" round	675	5,000	SSP	<100>
W2	FZ	6" round	300	1.7	DSP	<100>
W3	FZ	6" round	300	0.13	DSP	<100>
W4	CZ	125 mm square	160-170	3-5	as-cut	<100>

W4p – planar CZ, W4t – textured CZ

morphology of the surface shown in Fig.2-13. This is due to two different ingot cutting technologies: slurry sawing, where abrasive diamond particle are contained in the slurry, and diamond sawing, where the particles are adhered to the sawing wire. Diamond sawing is a relatively new technology which can allow thinner wafers with better yield[111].

Diamond cut wafers had characteristic trenches on the surface which preserved on the wafers after alkaline etch[112] and could be clearly seen on the PL images due to worse passivation by a-Si. One approach to mitigate this issue would be to use isotropic Si etch instead of concentrated KOH for damage removal. In addition, diamond cutting results in amorphization of Si at the surface[111] which changes the KOH etch rate and also influences KOH-IPA texturing.

Surface morphology of as-cut CZ wafers was found to have a critical impact on the subsequent damage removal, thinning, texturing and finally on a-Si passivation. Moreover, it was found that the morphology was also dependent on the etching time. As a result, the wafers thinned in concentrated KOH could have a poor texturing when the recipe previously developed for thick wafers was used. One direction of the future work will be to apply isotropic etchants for damage removal and thinning either instead of KOH or as a surface finish step. This can allow a unified surface morphology favorable for high quality texturing (small uniform pyramids)[113].

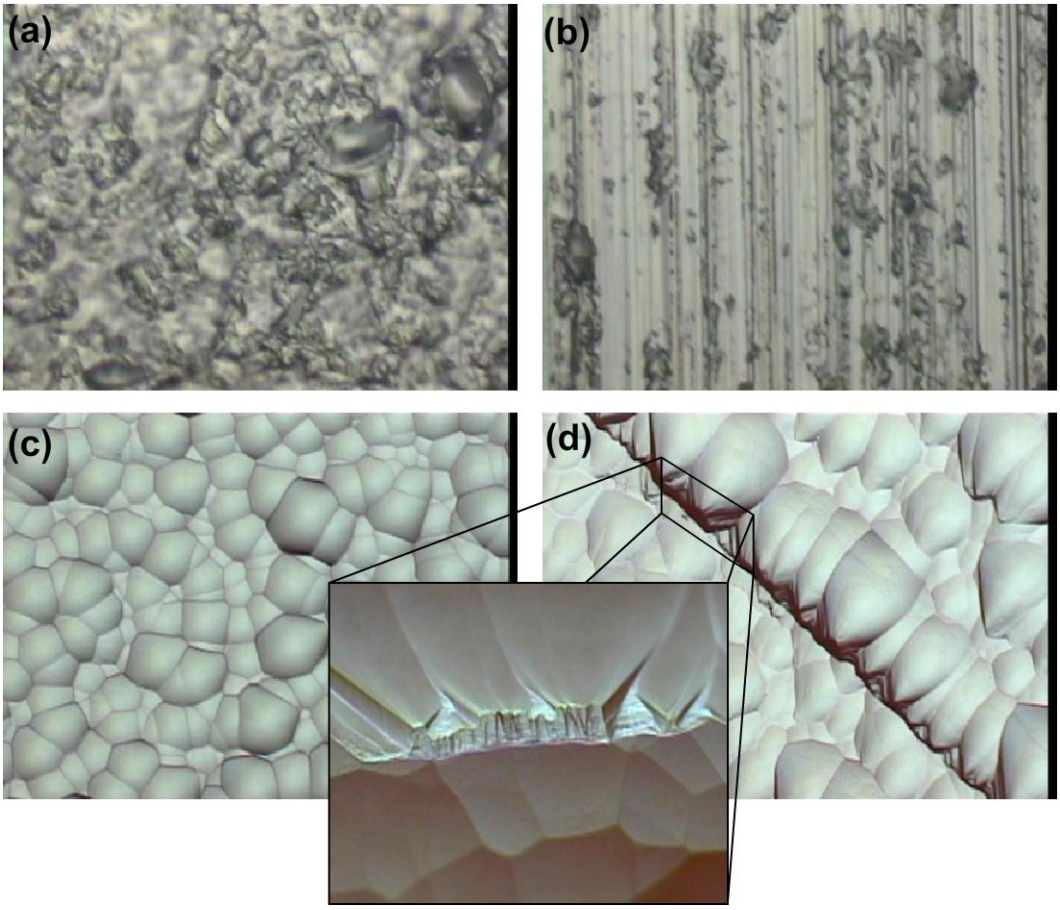


Fig.2-13.Optical microscopic images of two types of CZ wafers used in this work. As-cut surface of the (a) slurry cut wafer and (b) diamond cut wafer. The surface of the planar CZ wafers (W4p) after 10 min concentrated KOH damage removal: (c) slurry cut and (d) diamond cut. The grooves on the diamond cut wafers preserved after any time long KOH treatment. Note also that macroscopic morphology of the surface (the size of the polygons) differed depending on the KOH etch duration. This phenomenon also had impact on the texturing if it was done after the damage removal (see the discussion in Section 0).

2.4 Solar Cell Development Strategy

One of the main objectives of this work was to identify the minimum set of optimization parameters and characterization techniques necessary to develop a process flow resulting in a large area 20% SHJ cell. A strategy used to develop a SHJ solar cell with 20% efficiency is outlined in Table 2-4. First, the passivation of mirror polished FZ

Table 2-4.The sequence which was used in this work to develop SHJ solar cell process.

Step	Title	Process	Optimization target
1	(i)a-Si DOE	PECVD	Max τ_{eff} on mirror polished wafers
2	(i)a-Si on textured	Cleaning, texturing	Max τ_{eff} on textured wafers
3	doped a-Si DOE	PECVD	Min bulk resistivity
4	ITO	Sputtering	Max conductivity, min. absorbance
5(a)	ITO thickness	Deposition time	Min reflectance
5(b)	a-Si thickness	Deposition time	Tradeoff with multiple components
6	Front grid	Screen design	Min R_S, max J_{SC}

wafers by (i)a-Si:H film was developed. Then, the cleaning process that produced ultrapassivation of textured wafers was found. Then, the doped a-Si films were developed to achieve the highest possible doping, i.e. the Fermi level closest to the band gap edge. Bulk resistivity of the film was used as an optimization parameter since it was easy to measure and also since it was directly proportional to carrier density in the film. A better parameter characterizing the efficiency of doping would be the activation energy which does not depend on mobility. Activation energy can be measured by fitting the temperature dependent conductivity.

The next optimization step was the deposition of i-p/i-n stacks on the textured wafers targeting the highest lifetime. The goal of this step was to find the minimum possible thickness of (i)a-Si to produce >730 mV implied V_{OC} and >82% implied FF. As will be discussed in Section 3.6, the thickness of a-Si is involved in a number of tradeoffs and therefore should be carefully optimized. ITO was subsequently deposited with the deposition time set to produce a minimum of reflectance at 550 nm. Note that 1.5-1.7

times higher deposition time was required to achieve this condition on textured wafer. Finally, the thickness of the doped a-Si layers was optimized to reduce optical losses and preserve a high pseudo FF. This was done simply by reducing either the thickness of (p+)a-Si or (n+)a-Si (depending on which layer is on the front surface) until V_{OC} and pFF start to decrease.

The described procedure allowed large area cells with 730 mV V_{OC}, 36 mA/cm^2 J_{SC} and 74.5% FF. Efficiency was limited only by the bulk resistivity of Ag paste and several process deficiencies as discussed in Section 5.4.

Future SHJ cell optimization should include the reduction of optical losses in a-Si and ITO and the reduction of resistive loses in the front grid. The conventional ways to achieve higher current are: 1) developing ITO with higher mobility and lower carrier density (hence, lower absorption in the IR), 2) developing doped microcrystalline films with lower absorption by, for example, using VHF PECVD, 3) using graded a-Si and ITO layers. High resistance can be addressed either by using lower resistivity Ag pastes, by using multibusbar designs, or by switching to plated Cu metallization.

An approach to a 22% SHJ cell resulting from this work and based on the loss analysis is discussed in Section 6.8.

Chapter 3
OPTIMIZATION OF THIN FILMS

3.1 Introduction

Chapter 3 describes the development of a-Si deposition, the cleaning of textured wafers, and the deposition of ITO and the development of doped μc-Si films. Passivation performance, electrical and optical properties of the films are presented.

Optimization of a-Si and ITO films used for SHJ solar cells is usually done empirically due to the large complexity of the plasma deposition process. For fast and efficient optimization, a proper set of response parameters should be identified. In this work, such parameters were passivation quality of polished wafers by (i)a-Si:H, bulk conductivity of doped a-Si films, and transparence and conductivity of ITO. The thickness of all films was additionally optimized since it was involved in multiple tradeoffs. A separate study considered the cleaning of post alkaline etch wafers which was necessary to ensure low defect density at a-Si/c-Si interface and to avoid epitaxial growth of a-Si. The last section of this chapter is devoted to the development of n-type doped microcrystalline Si films which could be used at the front surface of rear emitter SHJ cell to reduce optical losses.

3.2 General Development Strategy

The development of thin films started with the optimization of the gap between the showerhead and the substrate targeting the lowest film thickness non-uniformity. A SiN_x deposition was used as its thickness was the fastest to measure using a reflectometer

(the thickness of a-Si can only be measured by ellipsometry; and the ellipsometer with short data acquisition time was not available in this work). As a result, the gap value of 392 mils (10 mm) producing 2% nonuniformity measured at 25 points across a 6" round wafer was found. The gap was fixed for all further thin films depositions. Note that here the gap was the distance between the substrate surface and the showerhead. Since the substrates used in this work had different thicknesses, the position of the ceramic substrate holder was adjusted for a particular wafer in order to preserve a 10 mm gap.

The deposition conditions of (i)a-Si:H film (pressure, power, H_2 flow) were varied in a DOE fashion with SiH_4 flow and temperature fixed at 40 sccm and 250 ^oC respectively. 40 sccm SiH_4 flow was picked based on the previous experience working with PECVD tool used in this work. It was found that relatively high SiH_4 flow should be used to ensure good thickness uniformity. 250 ^oC temperature set point was picked in accordance with the literature data which suggested that the best passivation is achieved at the boundary between microcrystalline and amorphous growth which occurs at moderate deposition temperatures[114][115][116]. Note that 250 ^oC was the setpoint of the thermocouple attached to the middle of the ceramic substrate holder. The actual temperature of the substrate was in 220-230 ^oC range.

A rotatable central composite DOE with 6 axial elements was used to vary the deposition conditions. For the development of μc-Si films SiH_4 flow was reduced in order to get higher hydrogen dilutions and higher crystallinity fraction (see the discussion in Section 0). First, the deposition rate was determined by depositing the films on polished wafers where the thickness could be measured by VASE. Then, the films with the required thickness were deposited on the appropriate substrates. The results were

analyzed either by JMP 10 Software or analytically. The film with better uniformity was picked if several recipes provided the same values of the optimization parameters.

3.3 Optimization of Intrinsic a-Si.

(i)a-Si:H film was optimized on single side polished <100> wafers (W1) targeting the highest τ_{eff}. Out of box wafers didn't get any additional cleaning except 1 min BOE dip followed by 10 min DI water rinse and spin rinse drying prior to the deposition. The process parameter space explored for various deposition parameters is listed in Table 3-1 with the measured τ_{eff} at $1x10^{15}$ cm^{-3}injection for selected recipes.

It was found that the films with relatively wide range of H_2 dilutions achieved good passivation. For example, τ_{eff} > 10 ms was measured on the samples passivated by the films with 67-91% H_2 dilution, while epitaxial growth was observed only at 720 sccm

Table 3-1. DOE parameters for optimization of (i)a-Si on mirror polished wafer (W1) and the recipes producing the films with the highest effective minority carrier lifetimes. Also shown the performance of the recipe suggested by the JMP analysis as an optimum.

ID	H2 flow (sccm)	H2 dilution ($H_2/(H_2+SiH_4)$)	Power (W)	Pressure (Torr)	τeff (ms)
DOE range	80-720	67-95%	30-60	2-4	
1	80	67%	6	3	13.1
2	80	67%	45	2	16.5
3	200	83%	60	3.2	14.6
4	400	91%	30	4	13.2
5	400	81%	45	3	8.1±0.15
DOE optimum	100	71%	60	2.25	15.8

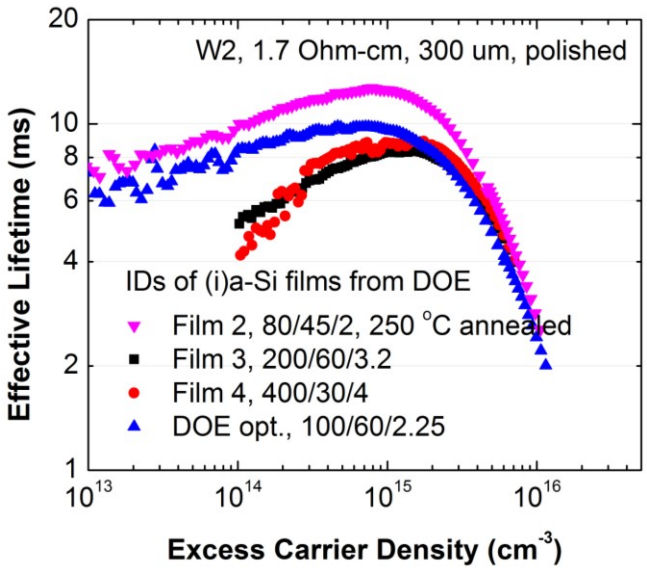


Fig.3-1. Effective minority carrier lifetime measured on mirror polished 1.7 Ohm-cm FZ wafers passivated with (i)a-Si:H recipes identified by the DOE. The recipes are listed in Table 3-1. Note the characteristic difference in passivation performance at lower injection levels. The optimum recipe was picked also taken into account thickness uniformity.

H_2flow corresponding to 95% H_2 dilution.

It is also interesting that good passivation was achieved for a wide range of chamber pressures and plasma powers indicating the presence of complicated dependences between all deposition parameters. It should be noted here that according to the literature, very good a-Si passivation can be achieved for a wide range of deposition conditions which are usually supplemented by post deposition annealing. Recently, several groups also reported H_2 plasma treatment of a-Si films[117][118] which has, in fact, a similar effect to the annealing in H^+ saturated ambient (except the film during annealing is not etched as is the case in plasma treatment[119]). The goal of this work was to achieve a sufficient passivation using a single layer film deposited at relatively high temperature with high deposition rate which would be suitable for large volume manufacturing tools.

The exact physical mechanism of (i)a-Si passivation and especially the control of passivation quality on the level of a-Si deposition parameters are not yet clearly understood. Several groups attempted to correlate the quality of passivation with the deposition conditions by Si-H bonding structure[120], hydrogen dilution ratios[121], surface treatments[122], and recently by H profiling of a-Si and a-Si/c-Si interface[116]. However, understanding of the deposition regime may be practically limited due to the sensitivity of the deposition to the configuration of PECVD chambers used by different groups. This includes gas flow dynamics, chamber materials, heat distribution in the chamber, plasma configuration, etc. Nevertheless, two factors leading to successful passivation are clear: 1) epitaxial growth should be avoided, 2) plenty of hydrogen should be supplied to the chamber. Therefore, using a DOE approach seemed to be the most efficient way to find the deposition regime yielding very good passivation where the DOE range was set taking into account two requirements listed above.

Four recipes from the DOE were selected for being tested on textured wafers (2, 3, 4 and optimized in Table 3-1). $\tau_{eff}(\Delta n)$ measured on polished wafers W2 passivated by the selected films are shown inFig.3-1. Note that only BOE clean was used for these wafers.

The next paragraph discusses the sensitivity of passivation to H-termination step. It is a common practice to transfer the wafers to the deposition chamber immediately after H-termination step. Several groups even reported not using DI water rinsing and drying after HF dip. H-termination is often also done prior to the deposition of a-Si on the second side of the wafer. In this work, a good passivation was achieved using a single 1 min BOE dip followed by 10 min DI water rinse and 10 min in the spin rinse drier.

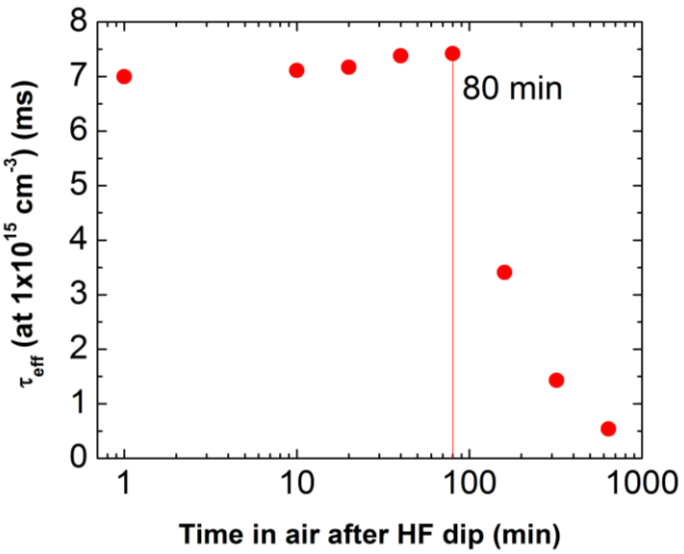


Fig.3-2. The degradation of effective lifetime measured on the samples left in the clean room ambient for a different amount of time after HF-termination in BOE. Note that 10 min DI water rinse and 10 min rinsing and drying in SRD was done on all the samples after BOE dip. The time started after the samples were removed from SRD.

Moreover, it was found that the wafer could spend approximately 80 min in the clean room environment before H-terminated surface was oxidized and passivation was worsened. Fig.3-2 shows the dependence of $\tau_{eff\text{-}15}$ on the time between BOE dip and transfer to the PECVD chamber.

It was also found that passivation quality is strongly dependent on the carrier used to transfer the wafer to the chamber. Although dielectric coated stainless steel carriers may be better suited for a-Si deposition in a production environment, this work had to use c-Si wafers as the carriers. The best passivation quality was achieved when c-Si wafers coated with 200 nm SiN_x were used.

Table 3-2. DOE parameter space and the recipes of optimized doped a-Si films. Also shown is the bulk resistivity of the optimized films.

	H2 flow (sccm)	Dopant flow	Power (W)	Pressure (Torr)	Resistivity (Ω-cm)
(n+)a-Si	50-300	30	27-60	1.5-3.7	
n-type opt.	175	30	45	2.5	90
(p+)a-Si	50-300	18	30-70	2-4.7	
p-type opt.	200	18	37	4	18,000

3.4 Optimization of Doped a-Si.

Optimization of doped films started from picking baseline intrinsic conditions (film 3) and ranging the flow of dopant gases in order to get the lowest resistivity. Trimethylborane (TMB) and phosphine (PH_3) were used as dopant sources.

As for intrinsic films, the deposition rate was identified first and then the films

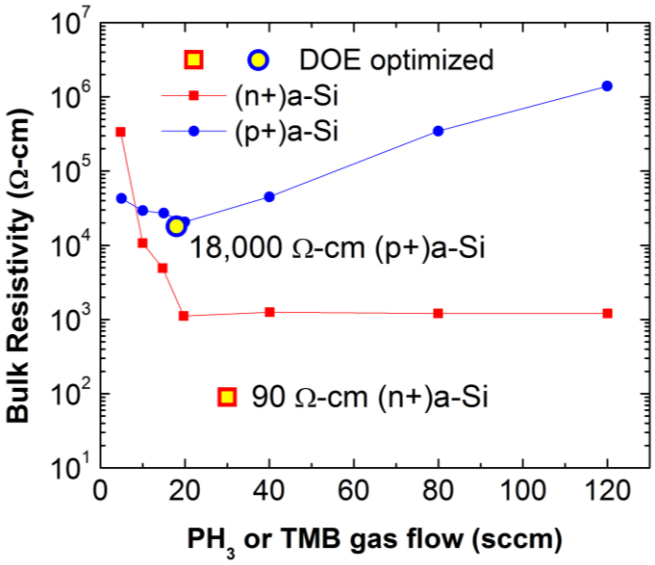


Fig.3-3. Bulk resistivity of the baseline doped a-Si films versus the flow of the dopants gasses. The graphs also shows the bulk resistivity of the optimized films.

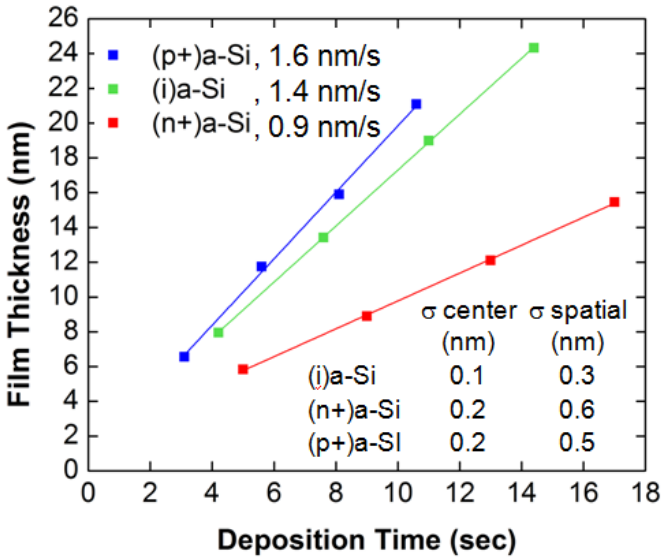


Fig.3-4. Linearity, uniformity, and repeatability of a-Si deposition. Note that the deposition rate used in this work was relatively high as compared to the literature data. This is primarily due to a high flow of SiH_4 used in this work. High flow of SiH_4 was also a reason for the amorphous growth of the films even at high hydrogen dilutions (see the discussion in Section 3.8).

with identical thickness were grown for resistivity measurements. Doped films were deposited on the glass microscope slide on top of 50 nm (i)a-Si film. It was considered that (i)a-Si didn't contribute to the conductivity. Fig.3-3 shows the effect of doping saturation for n-type films and a minimum in resistivity for the case p-type films. 30 sccm PH_3 and 18 sccm TMB were picked for further processing.

After the optimum dopant flows were identified, a DOE with the range of parameters recorded in Table 3-2 was conducted to optimize the films for the lowest resistivity. The obtained films were then used to prepare passivation test structures and solar cells.

The DOE approach allowed to reduce the resistivity of n-type film from 1,000 Ohm-cm down to 90 Ohm-cm, while the resistivity of p-type film stayed at the same

level – 18,000 Ohm-cm. Linearity, across wafer uniformity (5 points) and repeatability (3 wafers measured in the center) of the developed recipes is shown in Fig.3-4.

3.5 Deposition of ITO

As was stated above, due to the restricted access to the sputter tool, the properties of ITO were not optimized in this work. The only optimization parameter was film thickness. ITO films with equal thicknesses were deposited on both sides of the cell. The reflectance measured on the textured wafer with ITO films having the default (deposition time giving 75 nm film on planar surface) and optimized thicknesses is shown in Fig. 3-5. The film on textured wafer required 1.5 times longer deposition in order to get the reflectance minimum at 550 nm. It was also found that reflectance minimum, and therefore, presumably, the thickness of ITO, depended on the size of the pyramids, with

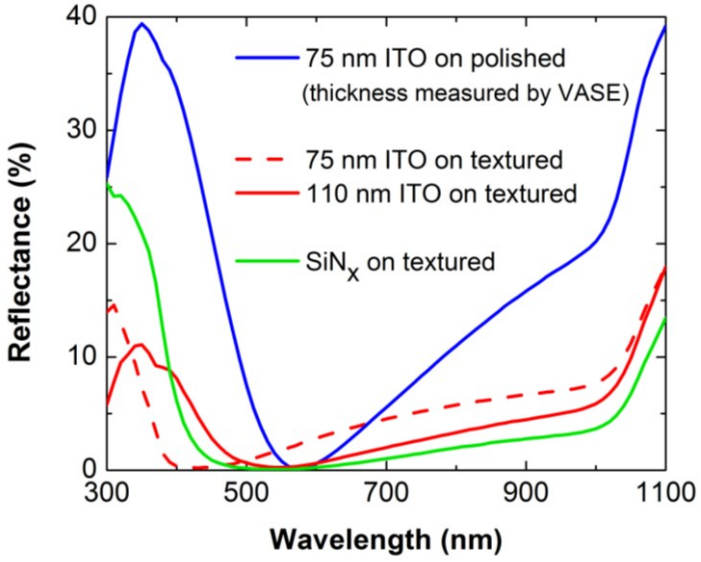


Fig. 3-5.Optimization of ITO thickness on textured wafer. Note that ITO and SiNx samples may had different initial texturing which may be responsible for the difference in reflectance at >700 nm. Also note that the texturing process developed during this work resulted in a wide range of reflectances of as textured wafers as shown in Fig.4-2).

smaller pyramids required longer deposition time.

The sheet resistance ($R_{\square}$) of the deposited film on textured wafer was 70-90 Ω/□, whereas the films with the same reflectance minimum on polished wafer had 50-60 Ω/□ $R_{\square}$. Sheet resistance also decreased approximately by 5-15 Ω/□ after annealing in the muffle furnace at 200-250 ^{o}C. Decreased sheet resistance was also accompanied by the increased IR absorption as measured by VASE. This was presumably due to the increased free carrier density (see the discussion in Section 3.7). Note that SHJ cells with ITO had to be annealed at a temperature at least 200 ^{o}C for 30 min in order to restore the passivation degraded due to plasma damage and also to cure the Ag paste. Therefore, the properties of ITO after annealing should be considered.

3.6 Optimization of a-Si Thickness

It should be noted first that the exact thickness of the films can be readily measured using VASE on mirror polished wafers only, whereas the thickness of the films on textured surfaces is generally unknown. The thickness of the films on textured wafers can be measured by TEM which involves a complicated sample preparation process. In this work, a cross sectional high resolution SEM was used to measure the thickness of a-Si films on textured wafers. In order to improve the accuracy of the measurement, a SiN_x buffer layer was deposited prior to the deposition of a-Si, followed by the delineation etch in BOE for 10 seconds. The SEM image of the prepared sample is shown in Fig.3-6.

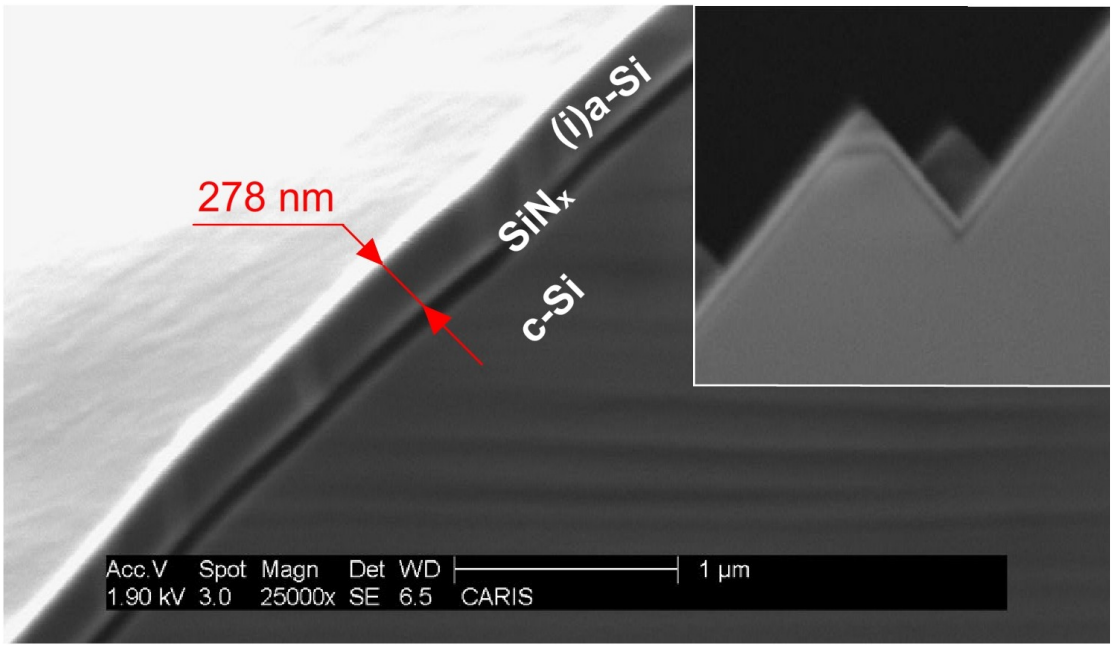


Fig.3-6. SEM image of (i)a-Si film deposited on textured wafer on top of SiN_x layer. The sample was then cleaved and etched in BOE for 10 sec in to create a contrast between (i)a-Si, c-Si and SiN_x. The measured thickness of (i)a-Si films turned out to be 1.5 times thinner than on planar wafer.

(i)a-Si deposition time was 300 sec which resulted in a 420 nm thick film on planar wafer. The measured thickness of (i)a-Si film on textured wafer turned out to be 278 nm which is 1.5 times thinner. And it follows that a 1.5 longer deposition time is required to achieve the desired film thickness on a textured wafer. In literature, a factor of 1.7 is commonly used to scale the deposition time on textured wafers. The exact value of the scaling factor will probably depend on the particular deposition regime used. For example, a gas flow limited deposition regime would produce the films with the same thickness independent on surface area. Therefore, the thickness difference between the films on planar and textured surfaces should be investigated for each particular deposition regime either by TEM, high resolution SEM or by a special VASE setup

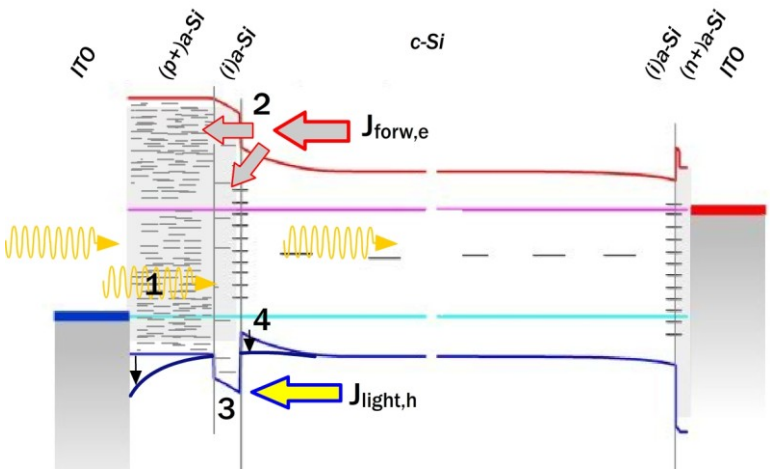


Fig.3-7. A schematic band diagram showing the tradeoffs involved in the optimization of the thickness of a-Si films. The tradeoff is among (1) parasitic absorption, (2) recombination through a-Si/c-Si interface and bulk a-Si states, (3) transport through (i)a-Si:H layer, and (4) band bending induced by the ITO near the surface of c-Si.

where the textured wafers are tilted such that the detector can collect the reflected light and probe the thickness of the film[123].

It should also be noted that due to the challenges in simulating plasma deposition process and electrical properties of a-Si films, and also due to the fact that a-Si is involved in multiple tradeoffs, the thickness of a-Si film is usually optimized empirically.

Table 3-3. A summary of the tradeoffs involved in the optimization of the thickness of a-Si layers. Note that the thickness and, in fact, the properties of the films may be different on textured wafer as compared to the polished wafer when equivalent recipes are used.

Thicker a-Si Film	Advantage	Disadvantage
(i)a-Si	Better Passivation	Parasitic Absorption
		Possible resistance
(p+)a-Si	High built in voltage	Parasitic Absorption
	No influence by ITO	Band bending by ITO
(n+)a-Si	Better Passivation	Possible resistance

The tradeoffs associated with a-Si films are summarized in Table 3-3 and shown schematically on the band diagram in Fig.3-7.

1) The first tradeoff is associated with optical losses. Parasitic absorption in a-Si is the Achilles heel of SHJ solar cells since it can reach several mA/cm^2 depending on a-Si thickness. a-Si films usually have τ_{eff} of the order of picoseconds and, hence, a short diffusion length. Therefore, the collection probability of the electron-hole pairs generated in a-Si films will approach zero. Note that there is experimental evidence from the measured QE data, that collection probability in (i)a-Si film is higher than zero due to the presence of the electric field quickly separating the carriers[124]. This will, however, depend on the properties of the particular (i)a-Si:H film and the heterojunction in general. For simplicity, in this work, absorption in all a-Si

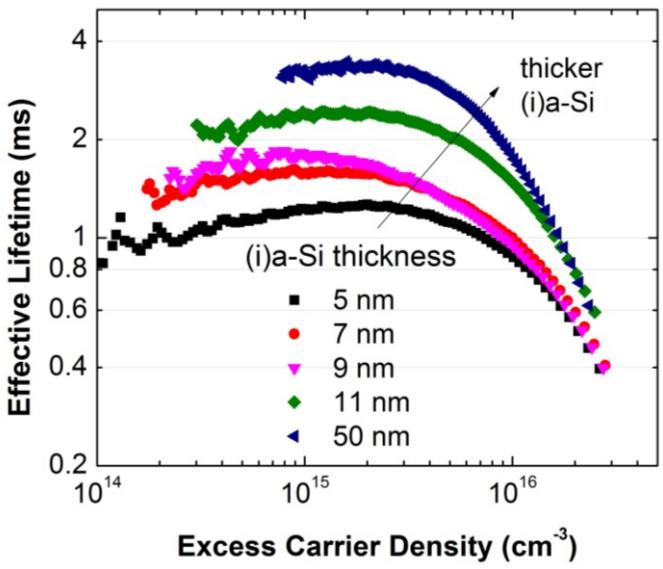


Fig.3-8. The dependence of the effective minority carrier lifetime measured on i-p/i-n passivated wafers (W4p) on the thickness of (i)a-Si:H layer.

layers was considered as a loss. Therefore, the thickness of (i)a-Si film on the front surface should be as low as possible.

2) On the other hand, thicker (i)a-Si is beneficial for surface passivation since it shields the carriers in c-Si from the highly defected (p+)a-Si layer as seen on the band diagram in Fig.3-7. Fig.3-8 shows experimental τ_{eff} measured on the textured wafers passivated with i-p/i-n stack with varying (i)a-Si layer thickness. It follows that for the combination of films used in this work, (i)a-Si should be at least 11 nm thick in order to provide sufficient passivation.
3) (i)a-Si may also cause the issues with the transport of minority carriers through the heterointerface increasing the series resistance of a solar cell. As follows from numerical simulation, the increase of both thickness and band gap of (i)a-Si layer may cause a significant drop of the fill factor[125][126].
4) Finally, (p+)a-Si should be thick enough to provide the amount of dopants sufficient to create a junction with a high built in voltage. It should also sustain the bending induced by ITO in order to achieve high V_{OC} and pFF. On the other side, (p+)a-Si is also absorbing light and, if very thick, may cause series resistance. (n+)a-Si does not contribute to the absorption, but if very thick, it can increase series resistance too. Thicker (n+)a-Si, however, may induce a stronger band bending to improve the passivation of the rear surface by the field effect[127][128].

In summary, the optimization of a-Si films involves multiple tradeoffs which strongly depend on the properties of particularly used films and are very difficult to

simulate. Therefore, the thickness of a-Si layers in the cell is usually optimized empirically.

3.7 Optical Properties of a-Si and ITO Films

Components of the complex refractive index of the used films measured by VASE are shown in Fig.3-10. Fig.3-10 also shows a thickness dependence of the complex refractive index of (i)a-Si film. In the considered films, the index stabilizes for thicknesses greater than 10 nm. For thinner films both refractive index and extinction coefficients are 10% lower. The reason for index variation can be the porosity of the upper layer of the film which occupies a large fraction of the volume when the film is thin, thus reducing the index of refraction. The data further used in optical simulation is averaged over the indexes measured on the films with 7-13 nm thicknesses.

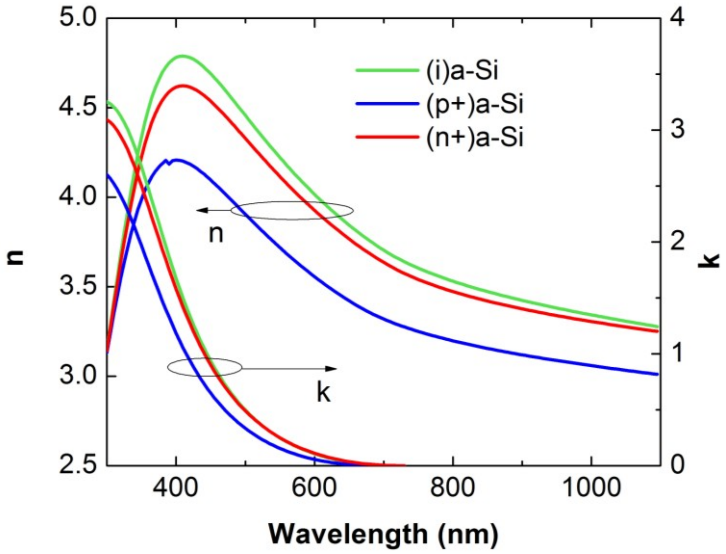


Fig.3-9.Optical constants of a-Si films measured by VASE. This data was further used in optical simulations. Note a relatively low index of (p+)a-Si film.

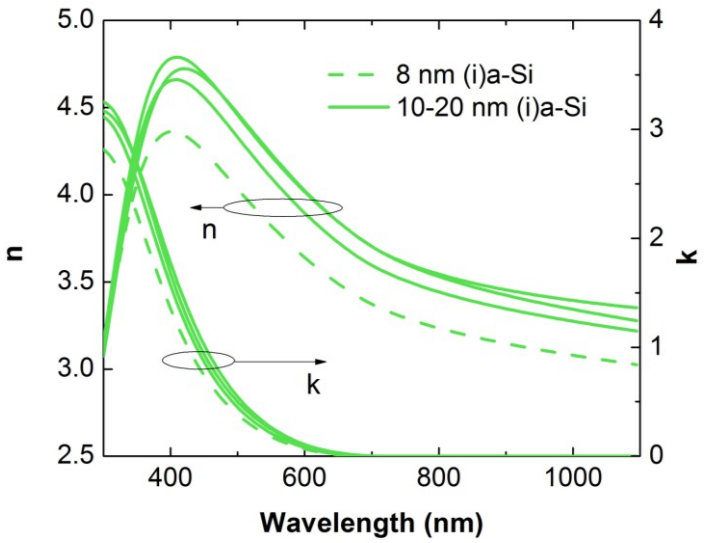


Fig.3-10. Index of refraction and extinction coefficient of (i)a-Si:H film obtained by fitting ellipsometric data for the films deposited on mirror polished <100> c-Si wafers. The data suggest that the films thinner than 10 nm may have a lower index of refraction presumably due to the thickness dependence of the film structure.

Optical constants of ITO are shown in Fig.3-11. As was mentioned above, annealing at 200-250 ^{o}C caused the increase of infrared absorption presumably due to the increased free carrier density. Refractive index also dropped from 2 to 1.9 at 633 nm. Optical constants of ITO are shown in Fig.3-11.

And Fig.3-12 compares the optical constants of ITO film used in this work with the films used by Holman et al.[129]. Comparison between the optical constants suggests that free carrier density in the ITO film used in this work is approximately $5x10^{20}$ cm^{-3}.

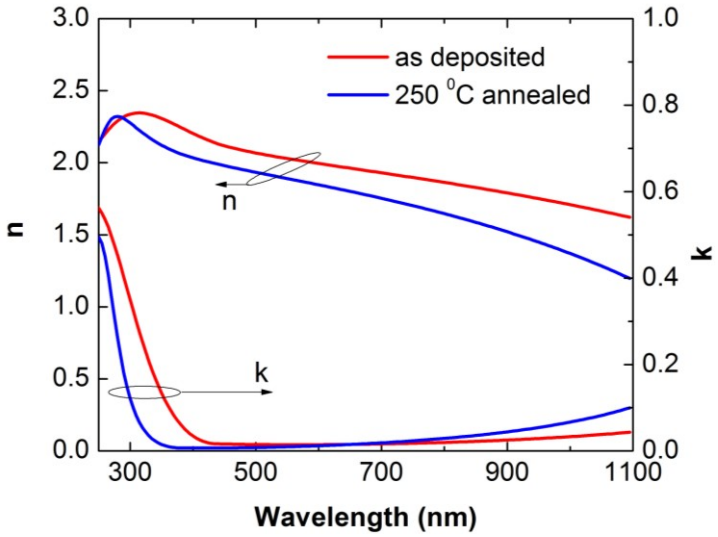


Fig.3-11.Optical constants of ITO measured by VASE before and after 30 min curing at 200 °C. The extinction coefficient at 1100 nm raised to 0.1 for the annealed film. Also note the difference in scale of k between ITO and a-Si. a-Si is a much stronger absorber in the visible range. However, the contribution of ITO may be high in IR regions since IR light may pass though ITO film several times until it is finally absorbed in c-Si or escapes the cell.

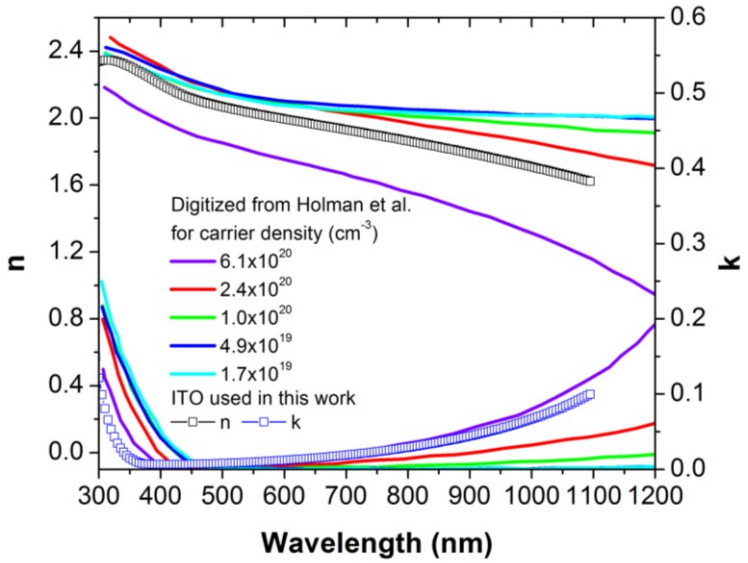


Fig.3-12.Comparison of the measured optical constants of ITO films used in this work to the data obtained by Holman et al. [129]. The comparison suggests that free carrier density in the used films is around $5x10^{20}$ cm^{-3}.

3.8 Development of Thin Microcrystalline Si films

A-Si at the front surface of SHJ cell is a source of parasitic absorption in the visible range of solar spectrum. For quantified analysis see the discussion in Section 6.5.2. Optical losses can be reduced by having thinner a-Si layer despite the limitations discussed in Section 3.6. Another way to reduce the losses at the front of SHJ cell is to use microcrystalline doped Si layers deposited by PECVD. Unlike a-Si, microcrystalline semiconductors have indirect band gap and therefore have a lower absorption coefficient.

Fig.3-13 compares extinction coefficients of a-Si film with bulk c-Si and microcrystalline Si film. In addition to a lower absorption coefficient, μc-Si films may achieve higher minority carrier lifetime compared to a-Si. In this case, the carriers generated in μc-Si have some probability to be collected, whereas in a-Si film this

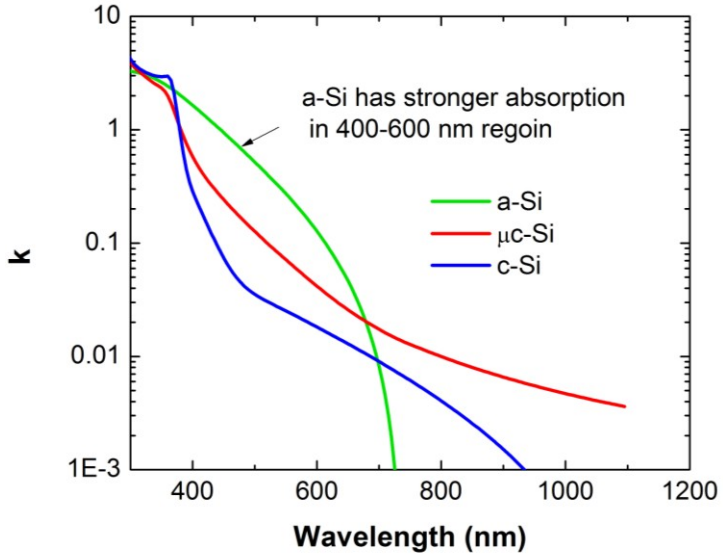


Fig.3-13.A comparison of extinction coefficients of a-Si, μc-Si and c-Si (from CompleteEASE database). Although the band gap of a-Si is around 1.7 eV, the fact that it is a direct band gap semiconductor makes the absorption of visible light more efficient.

probability is usually zero. On the other hand, the use of amorphous films as a minority carrier collector can be better as it will create a heterojunction with higher band offsets which may be beneficial for surface passivation. The approach of this work was to move (p+)a-Si film to the rear side of the wafer (see the discussion in Section 6.8) and develop microcrystalline n+ film for the majority carrier collector at the front side.

The deposition of thin μc-Si films can be challenging since the temperature of the deposition is limited by approximately 250 ^{o}C. Increasing the temperature further was found to worsen (i)a-Si:H passivation quality presumably due to hydrogen effusion outside the film. Microcrystalline Si films deposited by PECVD at low temperatures had been reported in literature earlier. Collins et al. suggests that high plasma power, high gas pressure, high H_2 dilutions and low SiH_4 flow are necessary to achieve microcrystalline growth regime[107]. Another key factor is the substrate on which the film is deposited. For example, a significant difference in crystallinity was observed between the films deposited on glass and on (i)a-Si . Finally, most PECVD systems that provided good crystallinity used VHF power supplies instead of conventional RF.

This work used glass slides with predeposited (i)a-Si film as substrates. First, intrinsic microcrystalline films were developed. Then, the films with the highest

Table 3-4. DOE parameter space and the recipe of the optimized (n+)μc-Si film. Also shown is the bulk resistivity of the optimized films.

ID	SiH_4 (sccm)	H_2 flow (sccm)	H_2 dilution ($H_2/(H_2+SiH_4)$)	Power (W)	Pressure (Torr)	PH_3 flow (sccm)
DOE range	7-40	500-2500	0.97-0.995	30-90	2.5-4.5	5-25
Optimum	7	1400	0.994	60	3.5	15

crystallinity were doped using a varying PH_3 to get the lower resistivity. Then, the films with device-relevant thickness were deposited.

It was first found that using a baseline SiH_4 flow equal to 40 sccm was a limiting factor preventing microcrystalline growth which was in agreement with the recipe design requirements proposed by Collins et al.[107]. Fig.3-14 (left)shows the dependence of Raman scattering of intrinsic μc-Si films on SiH_4 flow where H_2 dilution was kept constant. The data suggested that very small SiH_4 flow is required to get a high crystallinity fraction. Reducing the flow to 7 sccm, however, was problematic due to the limitations of mass flow controllers used in this work.

After the optimum SiH_4 flow was identified, other deposition parameters, i.e. pressure, power and H_2flow were varied using DOE methodology. The parameter space used in the DOE as well as the optimized deposition conditions that produced the films

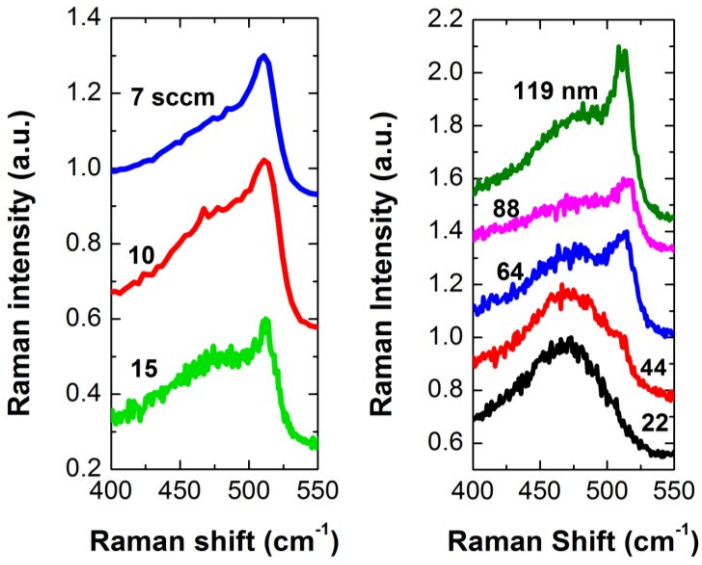


Fig.3-14. Raman crystallinity of intrinsic Si films deposited by RF PECVD on (i)a-Si/glass substrates at ~250 ^{o}C. (left) the dependence of crystallinity on SiH_4 flow for constant H_2 dilution, (right) the dependence of crystallinity on film thickness (in nm).

with the highest crystallinity fraction are summarized in Table 3-4. After the deposition rate was determined, the films with equal thicknesses were used to measure Raman scattering. It was found that PECVD configuration used in this work required very high H_2 dilution ratios (up to 99.4%) in order to achieve crystalline growth regime. The crystallinity fraction was also found to be a strong function of film thickness which is in agreement with literature data[130][106]. As shown in Fig.3-14 (right), with the reduced film thickness, the fraction of crystalline phase in the considered films decreased, making this recipe inappropriate for use in SHJ solar cells, where the thickness of the film should be about 10 nm.

Fig.3-15 shows the dependence of Raman crystallinity and dark conductivity of the films on PH_3 flow where the deposition conditions for the optimized intrinsic film were used and PH_3 flow was varied. It follows that the increase of PH_3 flow leads to

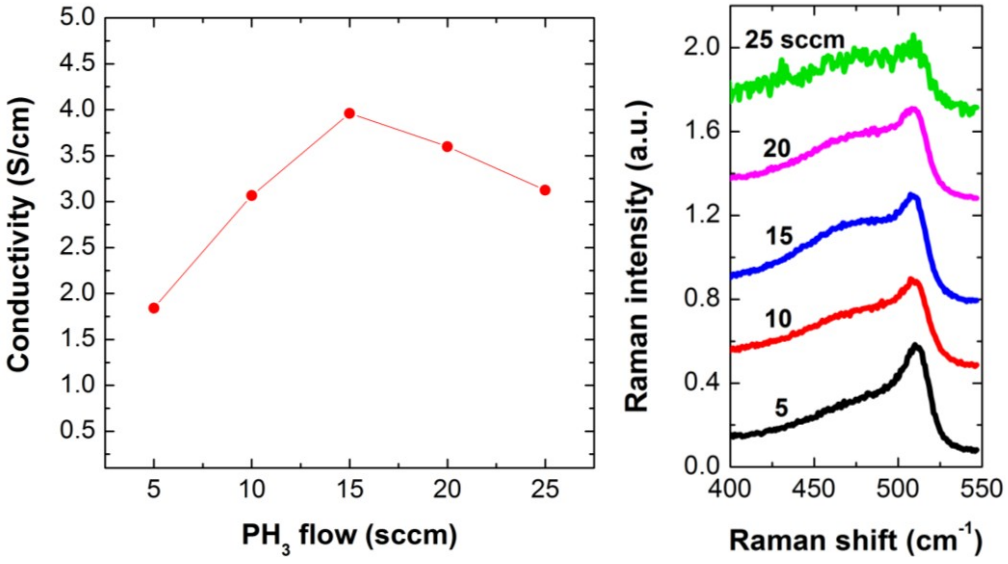


Fig.3-15. Conductivity of 140 nm thick (n+)μc-Si films doped with various flows of PH_3 (left) and Raman crystallinity of these films (right). Crystallinity drops with increased PH_3 flow. Conductivity peak is a compromise between reduced mobility and higher doping.

amorphization of the films. At the same time, a certain amount of PH_3 is necessary to dope the films. Thus, the maximum of conductivity is explained by the compromise between the reduction of mobility with increased amorphization of the films and the increased amount of dopant atoms supplied to the chamber with higher PH_3 flow.

In the last experiment of this study, the thickness of the optimized (n+)μc-Si film was varied. The dark conductivity of the deposited films is shown in Fig.3-16. Note that the device relevant thickness was between 5 and 15 nm. It follows that the current process produced the films with high fraction of a-Si phase if the film is less than 50 nm thick, which was the reason for the reduction of conductivity.

More optimization work will be necessary in order to improve crystallinity fraction for the device relevant thicknesses of μc-Si films. For example, H_2 plasma treatments or VHF power supply can be attempted. An alternative approach is to develop

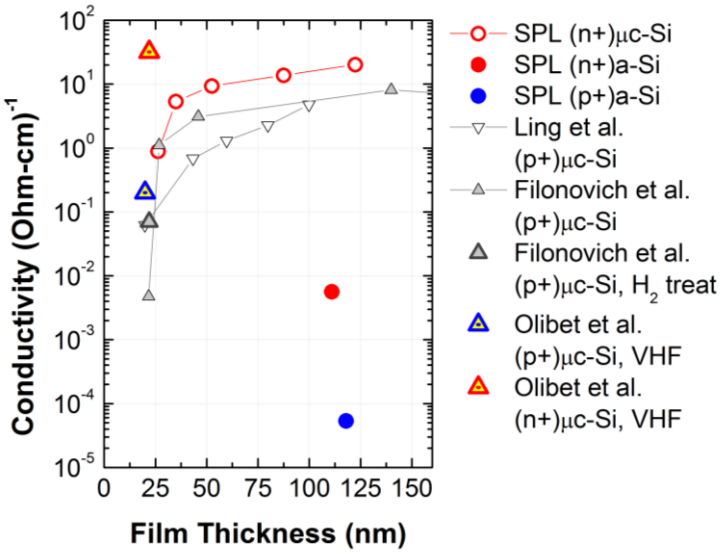


Fig.3-16. Thickness dependence of conductivity of the optimized (n+)μc-Si film and comparison to literature.

a-Si films with a small addition of C or O which can further increase the band gap making the films more transparent. Changing material properties, however, will be involved in other tradeoffs associated with electrical performance. A comprehensive optimization study would be necessary.

Chapter 4
ULTRAPASSIVATION OF TEXTURED WAFERS

Achieving repeatable and uniform passivation of textured wafers was one of the main challenges in this work. Chapter 4 presents a detailed description of the surface preparation process leading to state of the art passivation of post alkaline etch wafers by a-Si. The interactions between the morphology of the textured surface, follow up cleans, and a-Si deposition are discussed.

4.1 Passivation of Textured CZ Wafers

It was found that (i)a-Si film, which provided very good passivation on <100> mirror polished wafers, resulted in either negligible or poor passivation if applied to as-cut CZ wafers which were etched in alkaline solution either for damage removal or texturing. This work used KOH based etches which were followed by a full RCA clean. A poor passivation was attributed to either epitaxial growth induced by the nanoscale roughness present at the surface and not resolved by SEM imaging or to the metallic contamination trapped in the valleys between the pyramids which could not be neutralized by the full RCA clean. SEM images of textured surfaces attempted for passivation are shown in Fig.4-1.

In order to achieve good passivation of post alkaline etch wafers, three cleaning sequences were tested (see Table 2-1 for the particular recipe):

- Clean 1: RCA- b, concentrated HNA;
- Clean 2: RCA-b, diluted HNA;

- Clean 3: multi step nitric/acetic oxidation followed by Piranha and RCA-b oxidation (prior to the next oxidation the previous oxide was stripped in BOE)

The cleanings based on the mix of hydrofluoric, nitric and acetic acids (HNA) are known to cause increased reflectance due to the rounding of the pyramids. The increase of reflectance of textured wafers after Cleans 1 and 2 is shown in Fig.4-2. Dotted lines in Fig.4-2 also demonstrate the spread of front surface reflectance of as-textured wafers which was found to be a function of pyramids size. The value of reflectance at 700 nm is

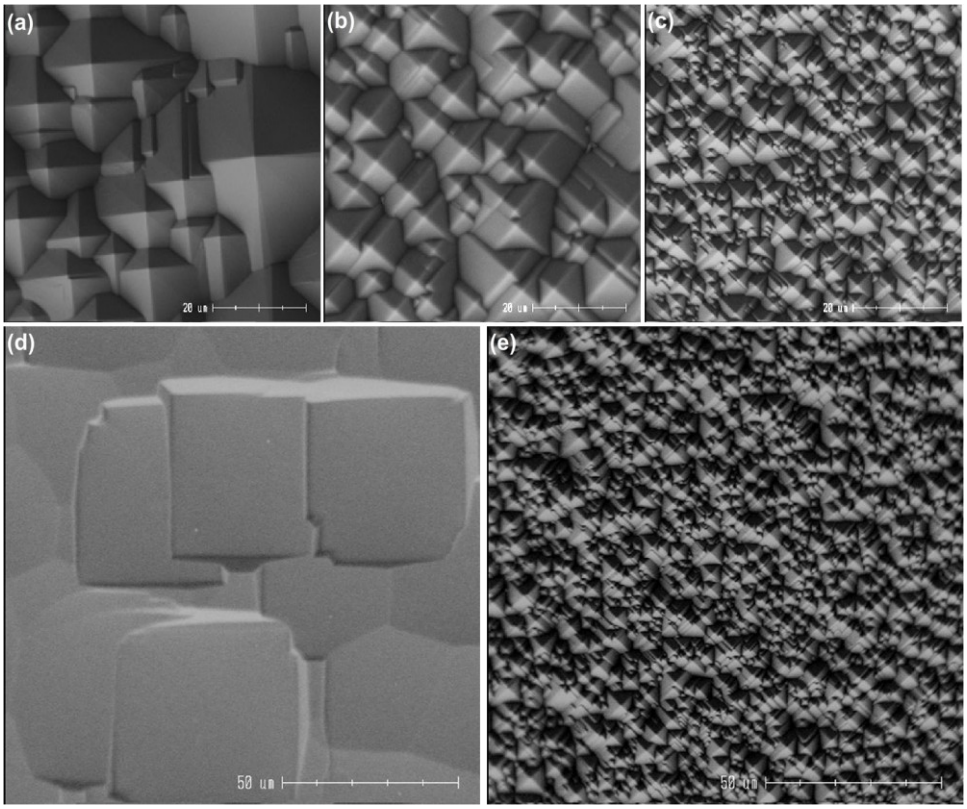


Fig.4-1. SEM images of textured wafers attempted for passivation in this work. (a) Large pyramids, (b) medium pyramids, (c) small pyramids, (d) planar surface after concentrated KOH etch, (d) a textured surface with small pyramids on the same scale as d for comparison. Note that the size of the polygons on planar wafers was determined by the etching time. The scales on top images are 20 microns and on the bottom images are 50 microns.

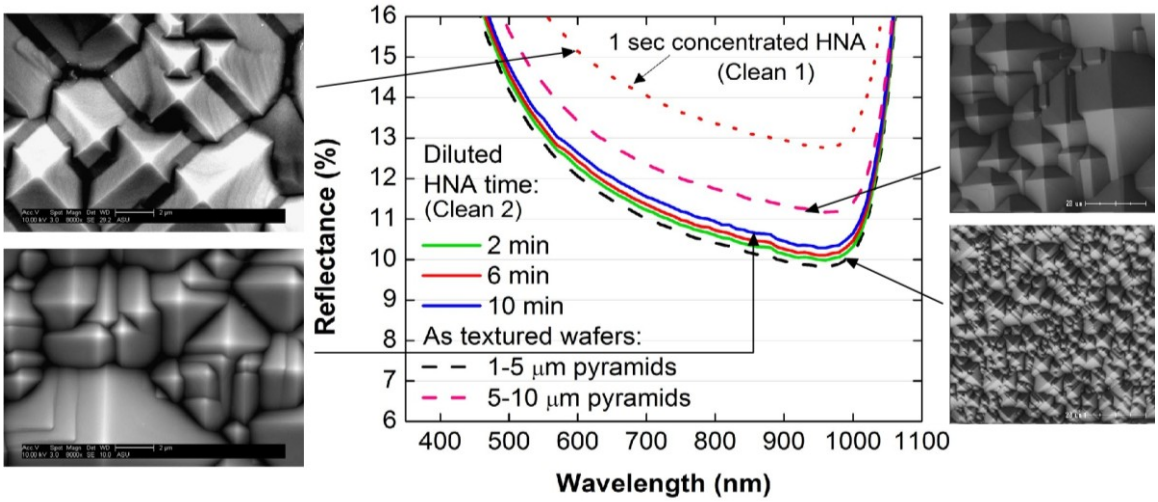


Fig.4-2. The effect of the size of the pyramids and various HNA treatments on the reflectance measured on textured wafers. Note that reflectance of as textured wafers varied depending on the average size of the pyramids. Smaller pyramids tended to produce lower reflectance.

further used as a metric. Smaller, 1-3 μm pyramids resulted in <11% reflectance, while the reflectance of the surface with larger pyramids could reach 12.5%. Reflectance could be even higher (up to 13%) for undertextured wafers with visible flat areas on the surface and also for the wafers with irregular surface features which sometimes occurred during texturing. The effect of different HNA based cleans on passivation is shown in Fig.4-3. After Clean 1 with only 1 second dip into concentrated HNA the reflectance increased to 14%, while τ_{eff} achieved only 1.5 ms.

Much better passivation was achieved using Clean 2 with 10 min diluted HNA treatment. τ_{eff} up to 3 ms on textured CZ wafers was measured with only 0.5% reflectance increase. Clean 2 was further used in this dissertation as a baseline for making SHJ solar cells. Later in the dissertation work, it was replaced with Clean 3 which achieved even

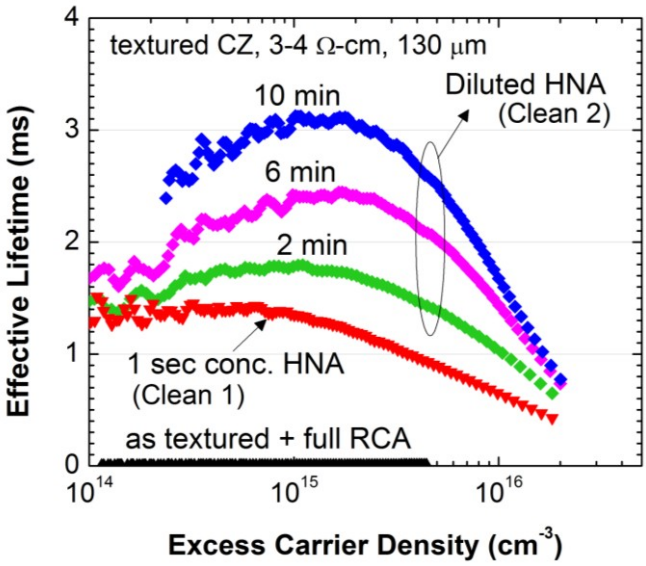


Fig.4-3. Effective minority carrier lifetime measured on textured wafers passivated with 50 nm (i)a-Si:H after Cleans 1 and 2 with varying HNA etching time. Note that textured wafers cleaned only using a standard RCA sequence had very poor passivation presumably due to the epitaxial growth of a-Si which is supported by measuring Raman scattering.

better passivation with no increase in reflectance, good uniformity, and repeatability. Clean 3 is discussed further in Section 4.3.

4.2 Surface passivation by i-p/i-n stack

After a sufficient passivation by (i)a-Si:H was achieved, the wafers were passivated by i-p/i-n stacks where the thickness of (i)a-Si was reduced to a minimum value which would reduce optical losses and still allow good passivation (see the discussion in Section 3.6).

The effective lifetime measured after i-p/i-n and ITO deposition on textured and planar wafers is shown in Fig.4-4. After ITO deposition, the wafers were annealed at 200 ^{0}C for thirty min in order to cure the damage produced by UV rays and/or high energetic

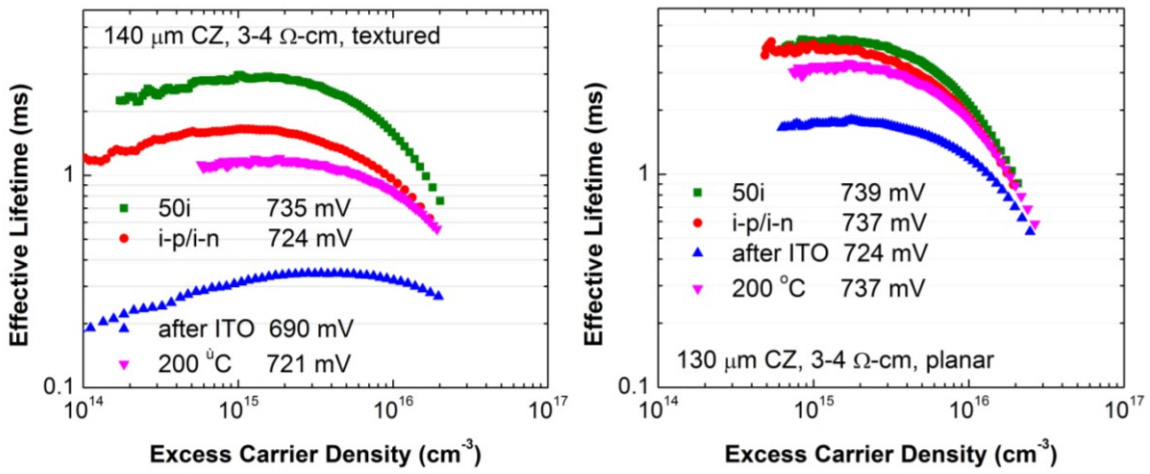


Fig.4-4. Effective minority carrier lifetime measured on CZ wafers passivated with i-p/i-n a-Si layers having device relative thicknesses. Planar wafer (right) and textured wafer (left). The wafers were cleaned using Clean 2 sequence.

particles during ITO sputtering (see the discussion below). Fig.4-4shows four main trends observed for the developed passivation process:

1. The effective lifetime on planar wafers was usually 1.5-2 times higher than on textured wafer.
2. The effective lifetime of the wafer passivated with i-p/i-n stack was 1.5-2 times lower compared to the wafer passivated with 50 nm (i)a-Si. Note that passivation quality also depended on the thickness of (i)a-Si layer in the stack (see the discussion in Section 3.6). 10 nm thick (i)a-Si:H film was used for the wafers in this study with the deposition time on textured wafers increased by a factor of 1.5 (in other words 7 sec was used to deposit (i)a-Si:H film on planar wafer and 10.5 sec to deposit on textured wafer). 15 nm thick (i)a-Si:H film achieved the same passivation performance as 50 nm (i)a-Si:H. 15 nm, however, was too thick to be used in a solar cell because of parasitic absorption and series resistance.

3. The effective lifetime always had strong injection dependence at <1e15 cm^{-3} injection.
4. The reduction of lifetime after ITO deposition could be restored by a low temperature annealing which recovered the implied V_{OC} almost completely. However, lifetime at intermediate and low injection could not be fully restored. The effect of ITO on recombination properties of SHJ solar cell was a topic of intense study in the last year. The degradation of lifetime at lower injections was attributed to the recombination through the states at ITO/(p+)a-Si interface[135], lower band bending at heterojunction induced by the workfunction of ITO[136][137], and to the damage of interface passivation during ITO sputtering[110].

τ_{eff} of textured CZ wafers was usually 1.5-3 times lower both in terms of maximum τ_{eff} (which could be used to estimate the pFF) and J_0 (which was used to

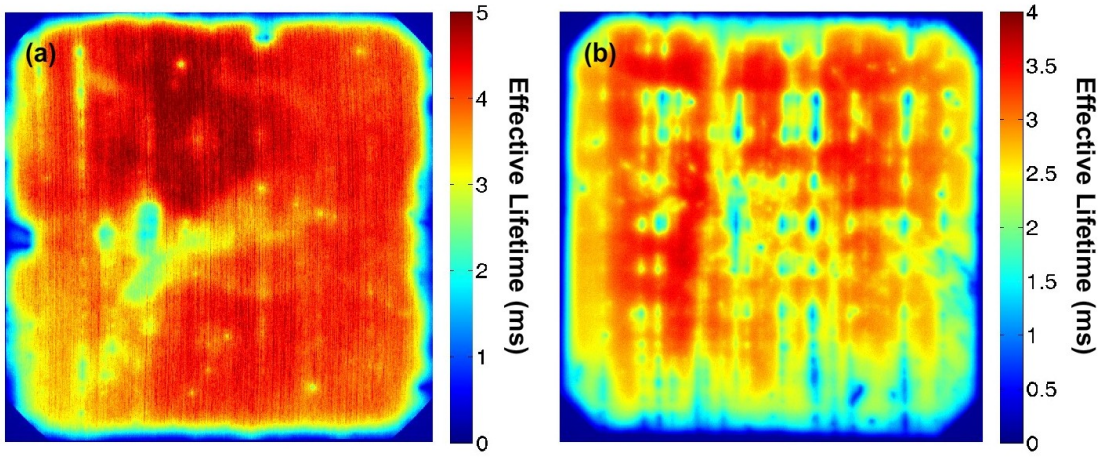


Fig.4-5. PL uniformity comparing planar (a) and textured (b) wafers passivated with i-p/i-n a-Si stack. Note the characteristic vertical lines with lower performance which are due to the trenches left after diamond cutting (see the images in Fig.2-13) .

estimate iV_{OC}). Textured wafers also experienced stronger spatial (within wafer) passivation nonuniformity as shown in Fig.4-5. McIntosh and Johnson gave a detailed comparison between recombination on planar <100> versus textured <111> surfaces passivated with thermal oxide[129]. They attributed the increase of recombination on textured wafers to higher surface area, higher density of dangling bonds, and the formation of additional defect states presumably induced by film stress.

In addition to the listed factors, the deposited a-Si films might have experienced local epitaxial growth resulting in uneven surface passivation and stronger injection dependence at $<1x10^{15}$ cm^{-3} injection. A similar effect on the τ_{eff} at lower injections was observed for local recombination centers in multicrystalline wafers[132].

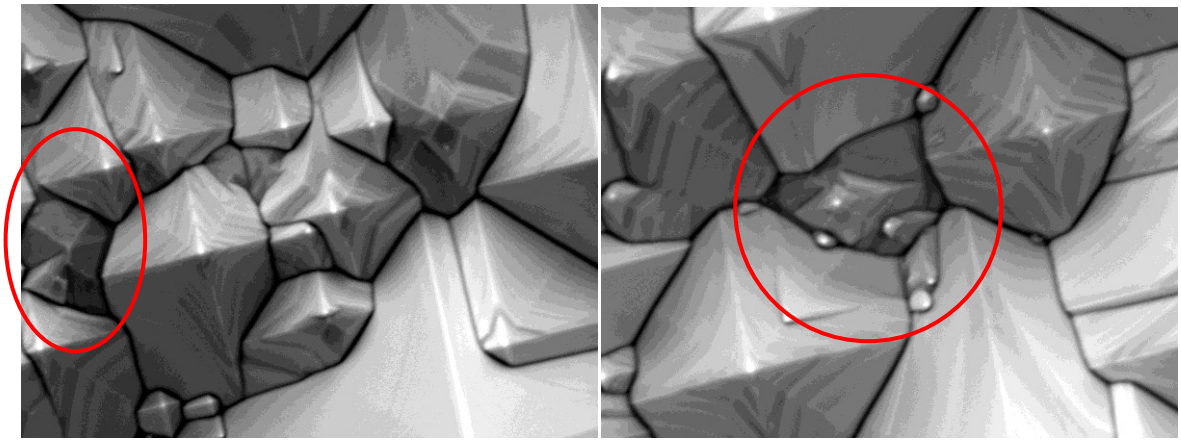


Fig.4-6.SEM images showing the examples of poorly textured regions which could be responsible for local reduction of passivation quality. Irregular features highlighted in red presumable caused local epitaxial growth of the deposited thin Si films. Another reason for poor passivation could be larger surface area with higher density of states. The horizontal scale on the images is 4 microns.

As was discussed earlier in Section 3.3, this work used a transitional deposition regime that produced the films at the boundary between microcrystalline and amorphous growth. Therefore, local epitaxy could easily be induced by nanoscale features present on

the surface of textured wafer. These features were, for example, observed in the valleys between the pyramids[133] and sometimes at the facets of the pyramids[134]. The examples of rough areas which could cause epitaxial growth are also shown in Fig.4-6.

4.3 Ultrapassivation of Textured Wafers

In addition to increasing the reflectance, a significant drawback of Clean 2 based on diluted HNA is poor uniformity and repeatability of HNA etch. The examples of passivation uniformity typical for Clean 2 are shown in Fig.4-7. In order to improve uniformity and repeatability of HNA etch the solution was 'seasoned' by etching a batch of dummy Si wafers for 10 min prior to etching the main batch. The solution was always stirred prior the dipping the wafers. It was found that the use of magnetic stirrers during

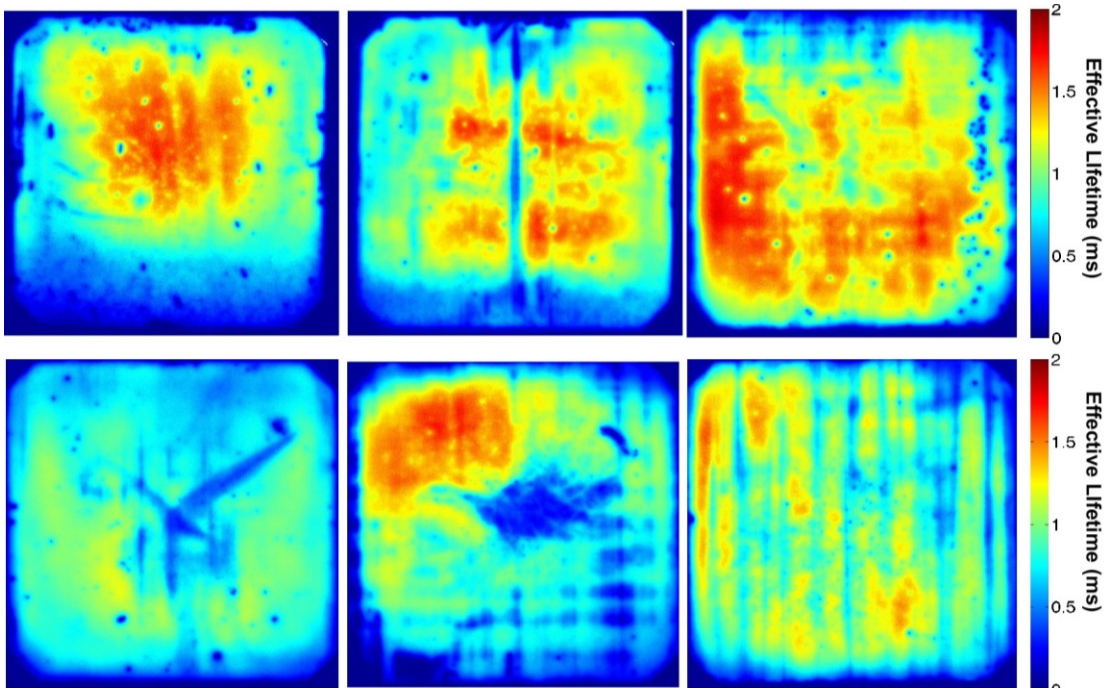


Fig.4-7. Calibrated PL maps showing the uniformity of surface passivation on textured wafers with i-p/i-n a-Si films cleaned using Clean 2. The top row represents slurry cut wafers and the bottom row – diamond cut.

the etch is not efficient and causes poor uniformity. Instead, manual agitation of the cassette during the etch was used. Etching was done in a beaker which can fit a standard 5" cassette, however, processing of batches of 20 wafers resulted in poor wafer to wafer uniformity and overall poor passivation performance. Instead, batches of 4 wafers were usually used. The solution was also found to have a limited lifetime. Usually, good results were obtained on the first 10-20 wafers, then the solution should have been replaced.

It was recognized that cleaning of post alkaline etch wafers was a key step in achieving good passivation quality. At that stage, three pathways towards further improving the passivation were considered:

1) Optimization of diluted HNA etch to include setting up of a larger volume plastic tank with the chiller to maintain the temperature at about 2-5 ^{o}C which is known to improve HNA etch uniformity. Introduction of the automatic agitation system in order to improve the flow of chemicals in the solution. This could be either mechanical agitation of the cassette or N_2 bubbling. Using different HNA recipes and 'seasonings'. For example, sacrificial glass or silicon can be used to "season" the solution prior to etching.
2) Switching to different (i)a-Si:H recipe with lower H_2 dilution to avoid epitaxy. Using hydrogen plasma treatments and layered (i)a-Si:H structures[117].
3) Using alternative cleaning recipes.

This work used the third path. An alternative multi step clean (Clean 3) was developed in order to achieve a repeatable and uniform passivation of 20 wafers batches with no increase in reflectance. The main idea behind Clean 3 is to decouple

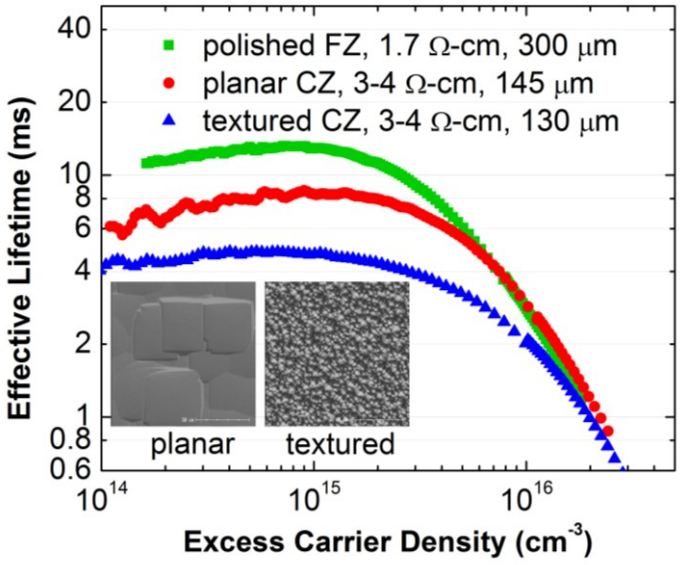


Fig.4-8. Passivation quality of post alkaline etch CZ wafers processed using Clean 3. The wafers were passivated by 50 nm (i)a-Si.The graph also shows τ_{eff} of polished FZ wafers processed by Clean 1 for comparison.

HNO_3/CH_3COOH oxidation and BOE oxide etching so that both reactions were naturally stopped when the entire surface was either oxidized or etched. It was suggested that this way a better uniformity could be achieved. It was known from literature that 10/750/250 HNA solution had approximately 2 nm/min etch rate. Therefore, 10 min etch used in Clean 2 should remove approximately 20 nm of Si. If one assumes that HNO_3/CH_3COOH oxidation consumes about 0.5 nm of Si, then about 40 oxidation/stripping cycles would be necessary to get an equivalent amount of Si etched. However, the first experiment with only 5 one minute cycles of oxidation and oxide striping each followed by 3 min DI water rinse resulted in very good passivation quality.

A repeatable passivation of textured wafers with 5 ms τ_{eff} using 50 nm (i)a-Si:H films and no increase in reflectance was achieved. τ_{eff} of textured and planar wafers passivated by 50 nm (i)a-Si after Clean 3 processing is shown in Fig.4-8. Fig.4-9

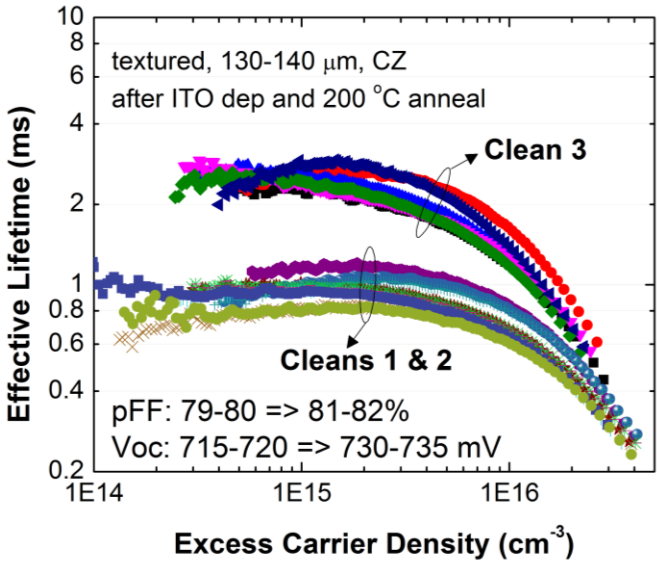


Fig.4-9. Effective minority carrier lifetime measured on non metalized SHJ cells processed using Cleans 1, 2 and 3. Due to a higher lifetime of Clean 3 the V_{OC} and pFF of the cells treated by Clean 3 reached 730-735 mV local V_{OC} and 81-82% local pFF measured by the Suns-V_{OC}.

compares τ_{eff} measured on non-metallized SHJ cells processed using Cleans 1, 2, and Clean 3, where local V_{OC} and pFF measured by the Suns-V_{OC} in the middle of the wafers are also shown.

Nitric-acetic oxidation did not require additional agitation or temperature control in order to achieve good wafer to wafer and across wafer uniformity. It also allowed for batches of 20 wafers (see uniformity study in Section 4.5).

A fresh mix of nitric and acetic acids was prepared for each oxidation. It was found that the wafers processed in nitric-acetic mix left in the lid-covered tank for over a week achieved 10-30% worse passivation. However, a detailed study of the lifetime of nitric-acetic solution was not done during the duration of this dissertation.

The exact mechanism responsible for the increase of passivation quality of post-alkaline etch wafers during nitric-acetic oxidation is unknown. One can speculate that high τ_{eff} is achieved due to:

1) Nanoscale smoothing of surface roughness and/or reconfiguration of dangling bonds at the surface which helps to avoid epitaxial growth of a-Si films. In other words, nitric-acetic oxidation is able to smooth the surface similar to HNA but with better uniformity. The problem with this explanation is that the amount of Si etched after 5 nitric-acetic oxidation cycles is about 1 nm which seems small to strip nanoscale surface features.
2) Neutralizing metallic contamination that is not stripped by the full RCA clean (for, example, Cu). An in-depth surface contamination study using, for example, inductively coupled plasma mass spectroscopy (ICP-MS) technique should be done to determine the concentration of impurities at the surface prior and after nitric-acetic treatment.

In order to understand the mechanism of sequential nitric-acetic oxidation, it was compared to a single oxidation in the mix of nitric and acetic acids for 5 minutes. Single wafers were processed. It turned out that 5 min oxidation was sufficient to achieve a good passivation quality which was only 10-15% worse compared to 5 oxidation cycles. Note also that the difference can be within the error imposed by passivation uniformity and repeatability. A wafer to wafer uniformity of single step oxidation also wasn't tested. The detailed study considering the effect of nitric-acetic oxidation of textured wafers on passivation quality is in progress.

4.4 Controlling Texturing and Surface Cleanliness.

This dissertation found that in addition to surface cleans, (i)a-Si:H passivation quality is also sensitive to the following factors: 1) surface morphology, 2) surface contamination by macroscopic particles, 3) handling of H-terminated wafers prior to (i)a-Si:H deposition, 4) handling of the wafers after a-Si deposition until it is capped with a TCO layer. The influence of the listed degradation mechanisms on surface passivation is summarized in Fig.4-10 which correlates microscopic images and photos of the wafers with PL images.

Macroscopic particles such as Si dust, fibers of fabric, organic tissue, etc. are

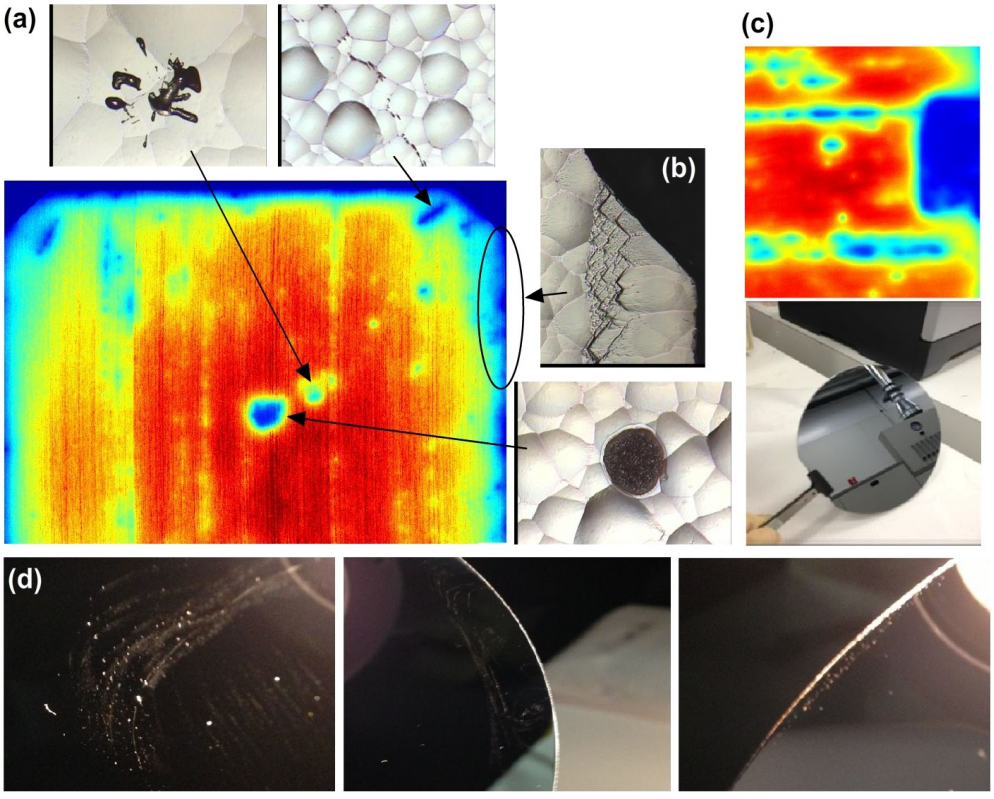


Fig.4-10. Microscopic images of various particles accumulated at the surface of the wafers during solar cells processing. (d) bright light inspection of mirror polished wafers showing accumulation of Si dust after handling with wand, tweezers and after spin rinse drying.

common to adhere to the surface of the wafer prior to a-Si deposition. The adhered particles shield the surface of c-Si wafer from a-Si deposition forming a local site with high surface recombination velocity. The examples are shown in Fig.4-10 (a). SHJ cells are particularly sensitive to this kind of contamination due to a high diffusion length. As a result, several microns wide particle can create a site pulling down local V_{OC} and pFF several mm around its actual location. A general practice was to minimize the time the wafers are exposed to air and keep them in clean wafer boxes. Wafer cassettes were washed in DI water for each new lot to clean them from Si dust which accumulated at the walls of the cassette. One additional source of contamination was rinsing and drying textured wafers in the spin rinse driers which were used in this work. It was found that Si dust, which could sometimes be created when the wafers hit the walls of the cassette during spinning, was trapped between the pyramids rather than washed away serving as local contamination source. It was therefore desirable to use static driers for processing SHJ cells.

Another common issue that affected passivation quality was associated with using the cassettes with wide walls and a small distance between the neighboring walls during alkaline etch. As a result, the wafers sometimes adhered to the walls of the cassette which worsened the circulation of chemicals producing a rough surface morphology as shown in Fig.4-10 (b). In order to resolve this issue, the cassettes with smaller coverage of the wafer surface and/or manual agitation of the cassette during etching to avoid sticking of the wafers would be required.

Wafer handling was found to affect passivation quality in two ways. Firstly, the tweezers or vacuum wands often left Si dust at the surface which shadowed a-Si

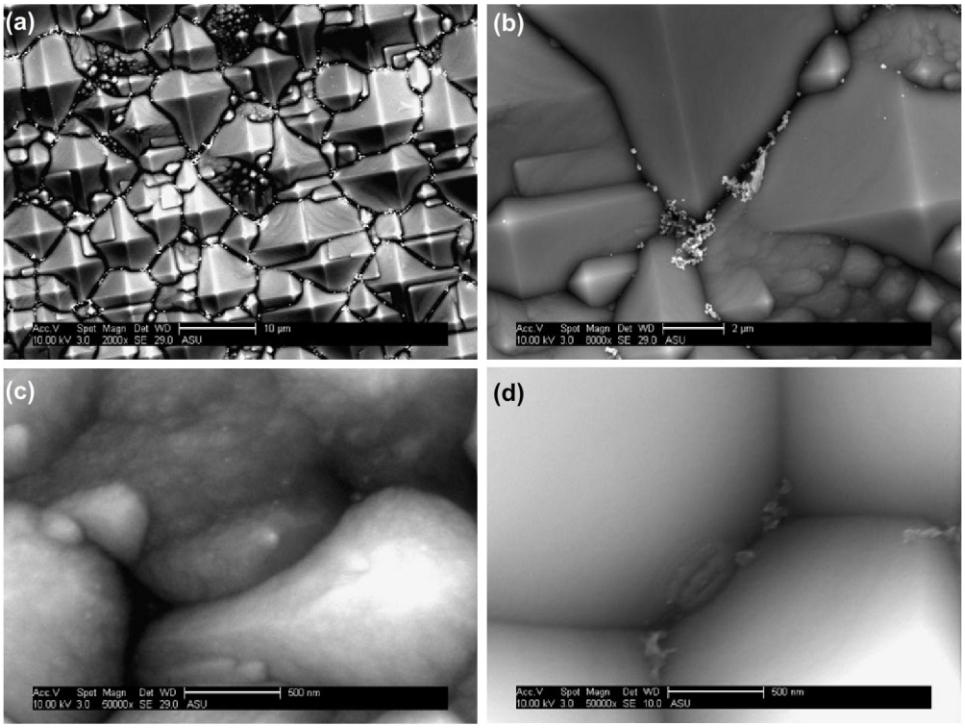


Fig.4-11.An example of poorly textured wafer having several characteristic features leading to τ_{eff} degradation. (a) general top view, (b) oxidized porous Si in between the pyramids, (c) the area having nanoscale roughness, (d) Si dust in between the pyramids. Images: Mark Bailly.

deposition. Secondly, if used after BOE dip, plastic tweezers as well as other materials (gloves and metal tweezers) led to complete neutralization of H-termination and poor passivation. The example is shown in Fig.4-10 (c). Consequently, it was desirable to minimize handling of the wafers especially after H-termination. Alternatively, special handling tools not affecting H-termination should be used to handle the wafers prior to a-Si passivation.

It was found, that in addition to the extensive post texturing clean, texturing quality and surface cleanliness prior to texturing should be carefully controlled. This is necessary to avoid local poorly passivated areas on the wafer which are usually visible in

PL images as local dark regions or spots. Textured wafers, for example, may have the areas of very small pyramids or even irregular structures at the surface which are not passivated using a-Si. The mechanism of degradation in this case is most probably due to the poor surface coverage by the a-Si film. It is also possible that nanoscale features are not smoothed by nitric-acetic oxidation and therefore may induce epitaxial growth. Another extreme fault mode is the formation of porous surface which is visible on SEM images as white spots due to the fact that porous surface is quickly oxidized. The examples of texturing with inappropriate surfaces are shown in Fig.4-11.

4.5 Uniformity and Repeatability of Passivation

In order to study passivation uniformity, two batches of 16 wafers were processed using Cleans 2 and 3 to make non-metallized SHJ solar cells. τ_{eff} was measured after ITO deposition and 200 ^{o}Cannealing. Therefore, the measured τ_{eff} was representative of the recombination properties of the complete SHJ solar cell. PL images were collected and

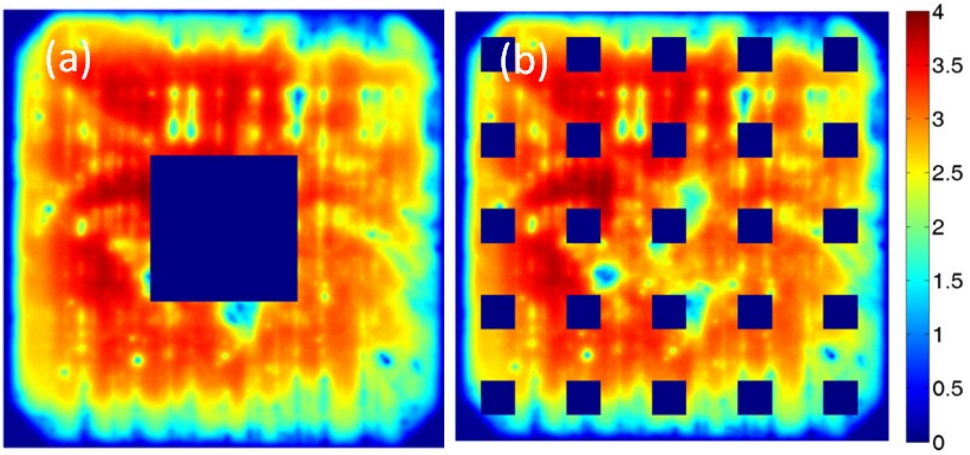


Fig.4-12. (a) the area used to calibrate PL image using effective minority carrier lifetime measured by a Sinton tester, (b) 25 square areas used in variance analysis. Lifetime was averaged across each of 25 squares.

calibrated using τ_{eff} measured in the middle of the wafer. The area used for calibration is shown in Fig.4-12 (a). Inverse lifetimes were averaged over 25 square regions across the wafer as shown in Fig.4-12 (b).Minitab routines were used for variance analysis.

The results are shown in Fig.4-13. The batch cleaned with Clean 3 resulted in 2.3 ms average τ_{eff} at $1x10^{15}$ cm^{-3}injection with 0.56 ms standard deviation, 40% variability due to spatial nonuniformity and 60% variability due to wafer-to-wafer nonuniformity.

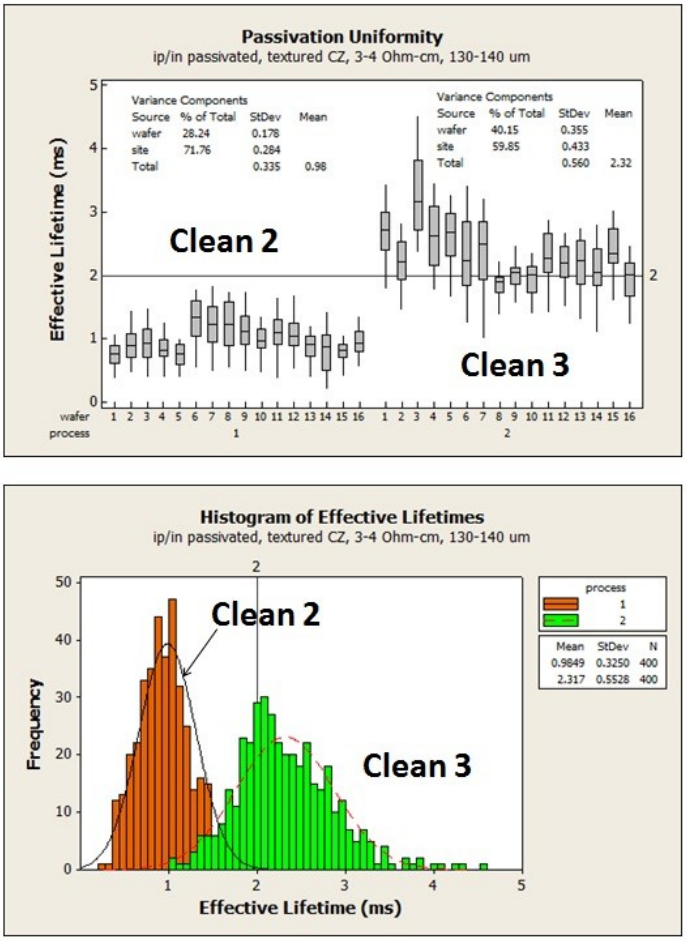


Fig.4-13. The results of the variance analysis of the effective lifetime of non metalized SHJ solar cells performed in Minitab. The wafers cleaned using Clean 3 achieved 2.3 ms mean lifetime with 0.6 ms standard deviation. 40% of variance in lifetime values came from wafer to wafer variation and 60% from the spatial variation.

Clean 3 had approximately 2.3 times better performance in terms of mean lifetime but its nonuniformity was higher with standard deviation equal to 0.56 ms which was two times higher than for Clean 2.

Thus, although a passivation quality allowing 730 mV V_{OC} and 82% pFF on large area solar cell was achieved, the uniformity of a-Si passivation of textured surface remained a challenge. The author speculates that the key to uniform passivation quality is the control of texturing quality. Textured wafers free of irregular features can achieve the uniformity close to the uniformity of planar wafers.

Chapter 5
SHJ CELLS ON 130 UM WAFERS

Chapter 5 presents the performance of large area SHJ solar cells fabricated in this work. Characteristic cells from two lots processed using different surface cleans (Clean 2 and 3) are compared. Several deficiencies of the process flow limiting the performance of the fabricated solar cells are discussed. Particular attention is paid to the resistance of low temperature Ag paste, printing quality, and additional edge resistance. First, the performance of the cells cleaned in diluted HNA (Clean 2) is discussed (Lot HI0042). Then, the components of the series resistance are analyzed using an analytical model. Finally, the performance of the cells cleaned using Clean 3 is presented (Lot HI0068).

5.1 The Cells Prepared Using HNA Clean

The performance of four complete SHJ cells from Lot HI0042 is summarized in Table 5-1. The cells reached 715-725 mV V_{OC} and 35-35.9 mA/cm^2 J_{SC}. The cells, however, suffered from low FF which was due to a high series resistance. The measured FF was only 67-68%. As a result, the efficiency of full area cells was only 17.2-17.7%. The V_{OC} of HI0042-20 cell turned out to be 3 mV lower than the implied V_{OC} extracted from the effective lifetime curve. The reason for the difference was a spatial nonuniformity of surface passivation caused by the nonuniformity of wet chemical cleaning process. 7 mV V_{OC} difference between the cells is also due to wafer to wafer variability of HNA etch used in Clean 2 sequence.

Table 5-1. The summary of the performance of 153 cm^2 bifacial SHJ solar cells prepared using Clean 2. The cell HI0042-20 was measured from both sides demonstrating 97% bifaciality. In order to reduce the length of the fingers and hence the series resistance, the cell HI0042-20 was cleaved along the crystalline planes. Note that the cells were measured n+ side up.

Cell ID	Area	Jsc	Voc	pFF	FF	Rs	Eff
	(cm^2)	(mA/cm^2)	mV	%	%	Ω-cm^2	%
HI0042-20 n+ up	153	35.8	718	80.2	68.7	2.6	17.7
HI0042-20 p+ up	153	35.6	717	80.9	67.4	3	17.2
HI0042-20 cleaved	15	35	715	79.6	73.3	1.4	18.4
HI0042-21	153	35.9	721	80.3	67.7	2.9	17.5
HI0042-23	153	35.9	725	81	68	3	17.7
HI0042-24	153	35.6	720	80.9	67.1	3.2	17.2

Fig.5-1 shows the PL and EL images representing the lifecycle of the cell HI0042-20. PL images after i-p/i-n and ITO deposition reveal nonuniformity of passivation quality across the wafer. High current EL image shows very high series resistance (R_S) in the fingers and around the edges of the wafer. The EL signal around the edges of the cell was weak even at low forward current which indicated significant resistance problems. One reason for edge degradation could be outgassing of the Kapton tape used to isolate the edges during ITO deposition for the cells in lot HI0042. Another reason could be very high resistance between a-Si and ITO caused by frequent handling of the edges of the wafers by vinyl gloves in the clean room. The handling occurred during lifetime and PL measurements, when the wafers were positioned on the carrier for ITO and a-Si deposition and sometimes when the wafers were transferred from cassette to cassette.

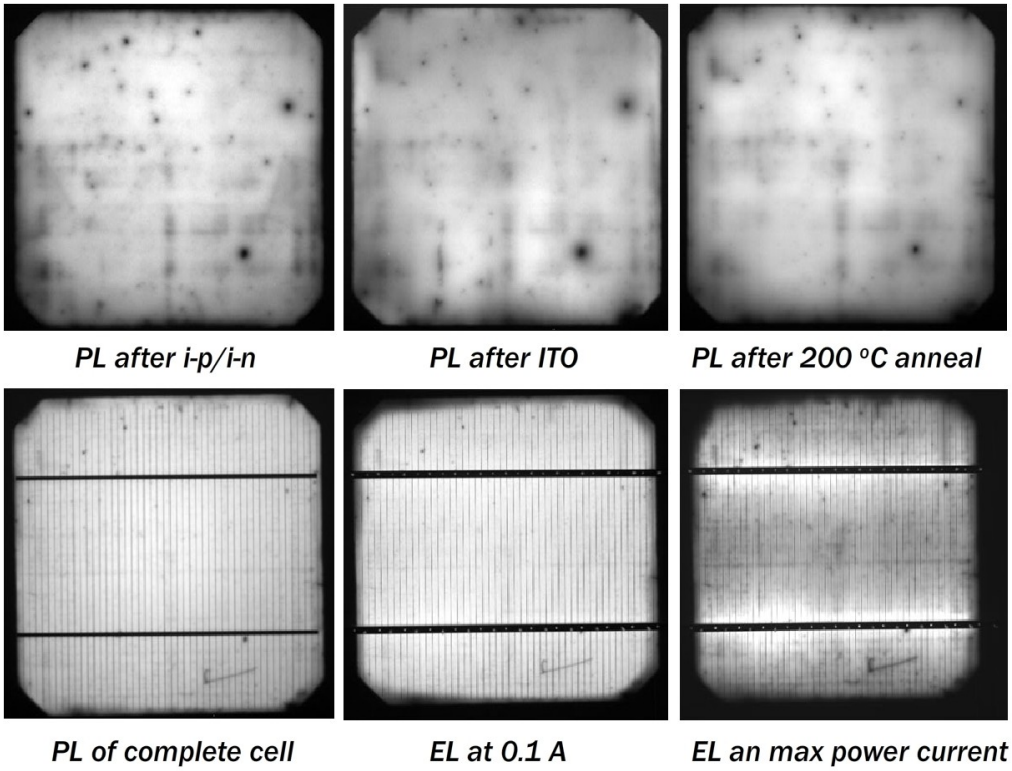


Fig.5-1.Lifecycle of the cell HI0042-20 cleaned using Clean 2 sequence..Note that the scale on all images was adjusted to get a better contrast.

Low bulk conductivity of the paste and edge resistance are the reasons for 67-68% FF, which is the main loss mechanism in the fabricated solar cells from lot HI0042.

Solar cell HI0042-20 was cleaved diagonally to get a 15 cm^2 SHJ cell which would have shorter fingers and would be free from edge resistance. Although the fingers in the diagonally cleaved cell had different lengths, the average length was approximately 20 mm. The performance of the cleaved cell is also shown in Table 5-1.The cleaved solar cell had lower J_{SC} and V_{OC} partly because of the higher area fraction shadowed by the front metal grid and partly due to the edge recombination. But since the cleaved cell had shorter fingers and no edge resistance, the FF raised to 73.3% resulting in 18.4% efficiency.

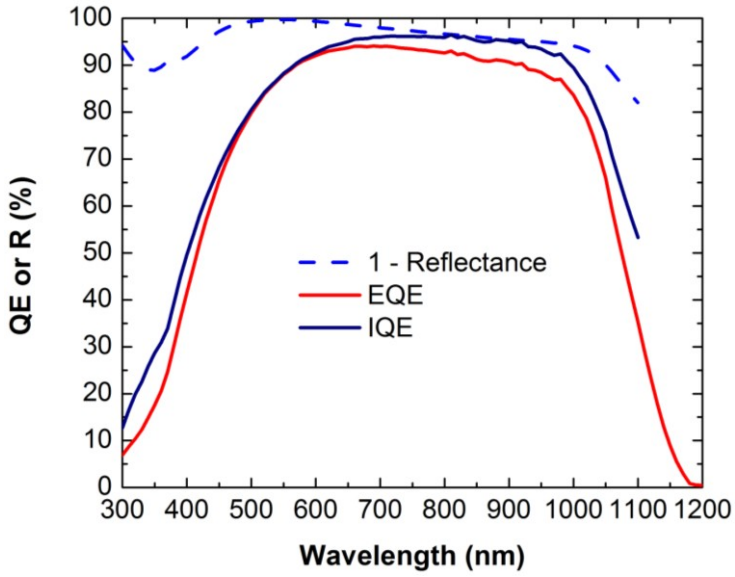


Fig.5-2.External quantum efficiency, reflectance and internal quantum efficiency measured on the cell HI0042-20. EQE was measured in between the fingers, while reflectance was measured on the non metalized cell. The cells in lot HI0042 had high parasitic absorption in the front (i)a-Si layers, relatively high reflectance and high losses in IR.

If illuminated from p+ side, the efficiency of the cell HI0042-20 turned out to be 0.5% absolute lower which was partly due to thicker (p+)a-Si layer used in the considered cell but mainly due to better printing on n+ side which resulted in lower resistance. No additional degradation of FF was observed when the cells were measured n+ side up. Fig.5-2 shows quantum efficiency of HI0042-20 and reflectance measured after ITO deposition. The main current loss mechanism in the fabricated cells (except metal shading), was the absorption in the front a-Si layers and ITO which was responsible for low response in 300-900 nm interval. In addition, the cells from lot HI0042 had relatively high IR reflectance due to the used texturing process (non-uniform pyramids size, large pyramids) and due to the use of HNA smoothing which adds 0.5%-1% absolute reflectance. Another source of IR losses was absorption in the rear and

frontITO and transmission of light through the rear surface since it also had a printed grid. For the detailed discussion of optical losses see Section 6.4.

5.2 Ag Paste Resistance

The increased FF of small area cells with short fingers and no edge resistance suggested that bulk resistivity of Ag fingers and a-Si/ITO resistance around the edge of the wafer are the main component of R_S. While both handling and using Kapton tape for edge isolation of the wafers can be avoided relatively easy, the resistivity of low temperature polymer Ag pastes can be a fundamental limitation of SHJ cells. For example, Panasonic is now using 3 busbars design for their 5" industrial cells, and 6" Roth & Rau cells have as many as 5 busbars. Both designs not only increase the shading losses but also increase the amount of expensive Ag used per cell. In this section, the resistance of SHJ cells is analyzed providing the conductivity of low temperature Ag pastes is fundamentally limited.

Low temperature Ag pastes from four vendors were tested in this dissertation. The printed grids were cured in a muffle furnace for 30 min in air ambient at different temperatures. Bulk resistivity of Ag was estimated by measuring the sheet resistance ($R_{\square}$) of 1.5 mm busbars. Fig.5-3 shows the measured $R_{\square}$of the busbar versus annealing temperature for three low temperature pastes from different vendors (1, 2, 3 and 4) as compared to the busbar $R_{\square}$ of high temperature pastes used for diffused solar cells in our lab (A and B). Note that the measured sheet resistance of the busbar was not a perfect metric of bulk resistivity since the height of the busbars differed from paste to paste and also depended on printing conditions which were different for different pastes used. It

was rather used as a quick and simple technique to characterize the resistivity of the pastes. It was found that the performance of two out of three pastes didn't reach the performance of high temperature pastes introducing high R_S losses even at 250 ^oC curing temperature. Fig.5-4 also shows specific contact resistivity measured using a transfer length method. Specific contact resistivity (ρ_c) between the considered pastes(Vendors 1 and 2) and ITO was close to 10 mOhm-cm^2 which is also 5-10 times higher than ρ_c between high temperature pastes and phosphorus emitter.

Increasing curing temperature lowered down both busbar $R_{\square}$ and specific contact resistivity. However, curing at 250 ^0C resulted in the degradation of surface passivation and reduction of V_{OC} and pFF. Therefore all cells in HI0042 were annealed at 230 ^oC. The pastes from Vendors 3 and 4 which were applied later for other lots required only 200 ^oC curing.

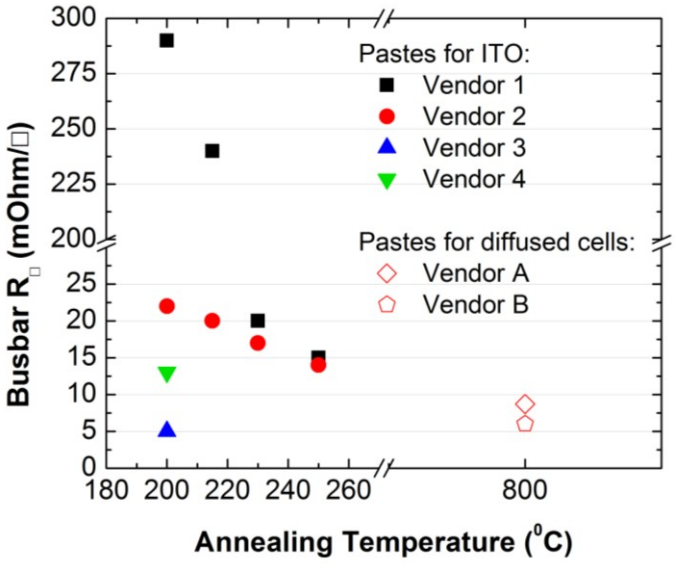


Fig.5-3. A sheet resistance measured on the screen printed busbars by a four point probe. The measured sheet resistance was assumed to be proportional to the bulk resistivity of the paste to the accuracy of busbar profile variations from print to print and for different pastes.

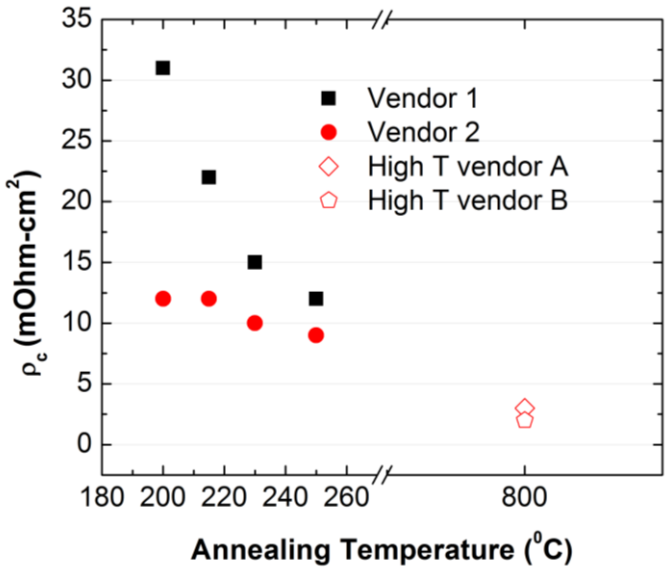


Fig.5-4. Specific contact resistivity between low temperature Ag paste and ITO measured on the solar cells. The measurement was done by isolating a TLM pattern on the solar cell using a diamond scriber. The measurement error, therefore, could be quite high.

Table 5-2. A set of parameters used to simulate R_S of SHJ with 2, 3 and 6 busbars. The width of the busbars is reduced to keep shading losses the same for all three cases. While the cell with 3 busbars can be measured in a conventional way, the 6 busbar cell would require soldering thin Cu wires prior to being measured.

	2 busbars 1.5 mm	3 busbars 1 mm	6 busbars 0.5 mm
Finger length (cm)	2.9	2	1.1
Finger height (μm)	15	15	15
Finger spacing (mm)	2.5	2.2	2.2
ITO $R_{□}$ (Ohm/□)	90	90	90
ρ_{Ag} (Ohm-cm)	$25x10^{-6}$	$25\ x10^{-6}$	$25\ x10^{-6}$
ρ_c (mOhm-cm^2)	10	10	10

In order to understand the potential gain from the use of shorter fingers for the reduction of series resistance, an analytical model was built and applied to the considered solar cells (see Section 6.6 for details). The main input parameters used in the model are listed in Table 5-2. Note that for simplicity, the model only considered the external series resistance neglecting the resistance in c-Si wafer, a-Si layers, and the interfaces between a-Si and ITO (except the edges). This can be a fair approximation for the considered cells since the contribution of internal components was relatively low compared to the external components such as bulk resistivity of the fingers and edge resistance. The model assumed that the total contribution of edge resistance is 1 Ohm-cm^2 although it wasn't directly measured. Also, note that the screen used to print HI0042 lot had 2.5 mm finger spacing, which is slightly wide for 90 Ohm/□ ITO. The breakdown of simulated R_S for

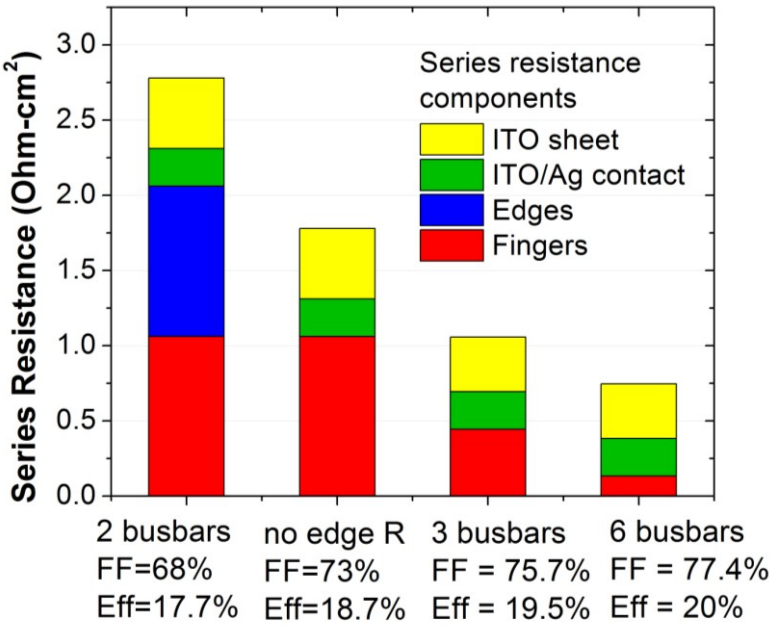


Fig.5-5. Series resistance of SHJ cells for the front grids with 2, 3 and 6 busbars predicted by the built analytical series resistance model. The model was based on the parameters measured on the cells from lot HI0042.

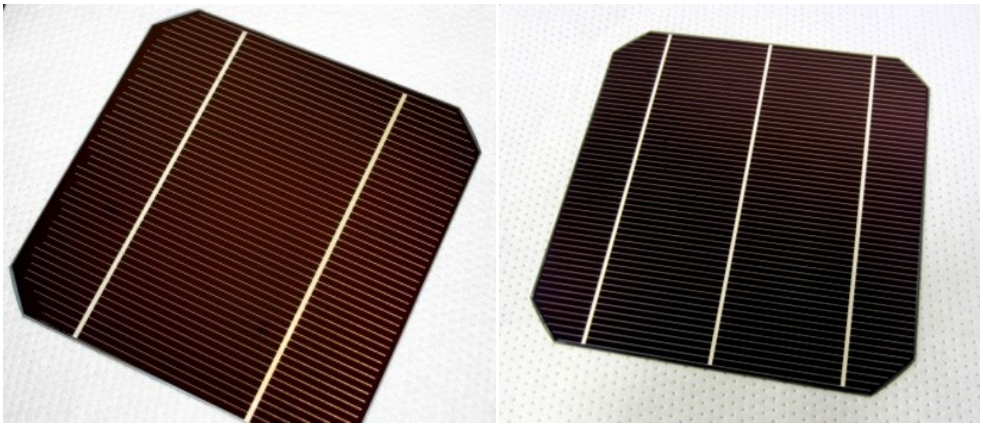


Fig.5-6.Cells from HI0042 (left) and HI0068 (right) compared. The cells in lot HI0068 obtained a grid with three busbar which was intended to reduce series resistance. The cells in HI0068 were also printed using a different paste, which resulted in poor printing quality and didn't allow achieving FF predicted by the model.

the cases with 2, 3, and 6 busbars is shown in Fig.5-5.

It follows from the model that if the same paste is used, the solar cell with 36 mA/cm^2 J_{SC} and 725 mV V_{OC} should have six 0.5 mm wide busbars in order to improve FF from 73% to 76.6% and achieve 20% efficiency. The cells prepared in this study should also be improved to avoid edge resistance.

5.3 Solar Cells Cleaned Using Nitric-Acetic Oxidation

The wafers in lot HI0068 were processed using Clean 3 which contained 5 cycles of nitric-acetic oxidation. As discussed in Section 4.3, the wafers processed using nitric-acetic oxidation had 2-3 ms τ_{eff} at 1x10^{15} cm^{-3}injection which corresponded to 82-83% pFF. The implied V_{OC} of the prepared cells was 730-735 mV promising 730 mV actual V_{OC}. HI0068 cells also had thinner (n+)a-Si layer (7 nm versus 9 nm in HI0042), slightly

Table 5-3.The performance of the cells in lot HI0068. The notable features of lot HI0068 were the usage of Clean 3 and Ag grid with three busbars.

Cell ID	Area	Jsc	Voc	pFF	FF	R_S	Eff
	(cm2)	(mA/cm2)	mV	%	%	Ohm-cm^2	%
HI0068-09	153	35.6	730	82.1	70.1	2.75	18.2
HI0068-15	153	35.6	729	82	70.4	2.63	18.2
Cleaved	8.1	35.1	718	79	74.2	1.1	18.7

thinner (i)a-Si layer (9 nm instead of 10 nm), the grid with 3 busbars and 2.1 mm finger spacing.

Electrical performance of two cells from HI0068 is summarized in Table 5-3. Indeed, the considered cells achieved >82% pFF and 728-730 mV, which is comparable

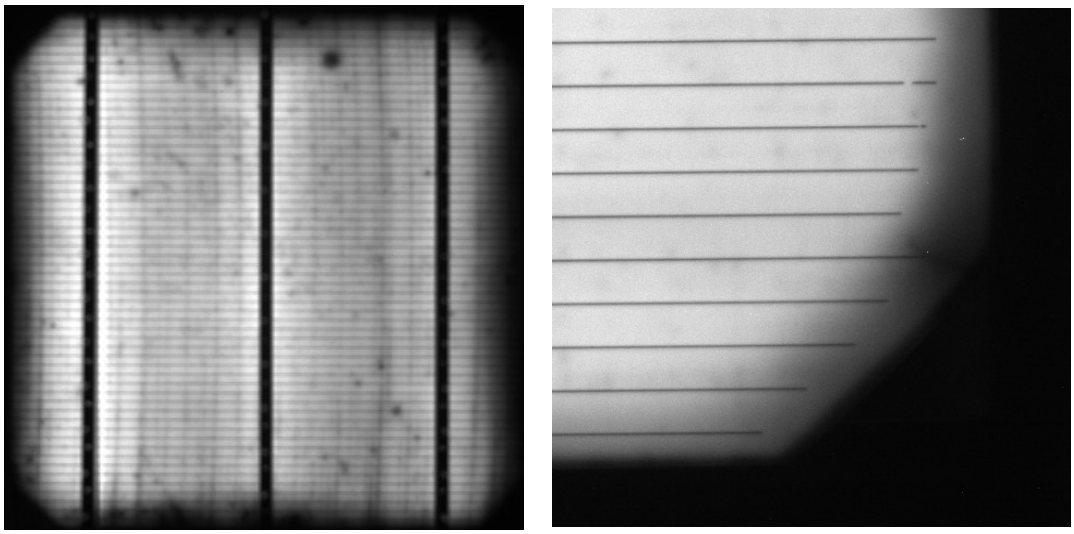


Fig.5-7. Left - maximum power current EL image of the cell HI0068-09 showing characteristic series resistance around the edges of the wafer presumably caused by the outgassing of Kapton tape used for edge isolation. Right – low current EL image of the cell from HI0042 showing the area actually shaded by the Kapton tape (~1 mm from the edge) with the area affected by the outgassing or handling (several mm from the edge). On low current EL image outgassing/handling area is visible due to a very high series resistance which is causing local voltage drop even at 0.7 mA/cm^2 forward current.

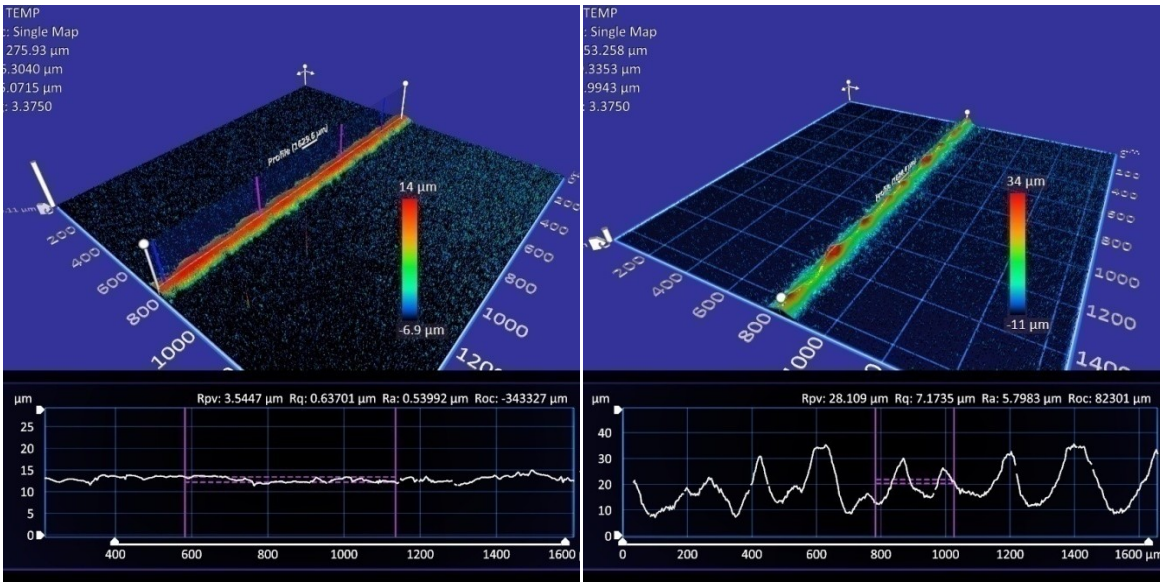


Fig.5-8. 3D optical profiles of the fingers printed using two different low temperature Ag pastes on the cells in lot HI0042 (left) and HI0068 (right). The paste used for HI0068 had noticeably higher viscosity. The width of both fingers was between 120 and 100 microns.

to the V_{OC} of the mass produced cells from Sanyo. The J_{SC} of the cells in HI0068 gained from less parasitic absorption in thinner front a-Si but lost due to larger area fraction shaded by 3 busbars and more densely spaced fingers. As a result, the current was at 35.6 mA/cm^{2}level which is approximately 0.4 mA/cm^2 lower than in 2 busbars cells from HI0042.

The cells in HI0068 were again processed using a Kapton tape for edge isolation. Also, no change in handling protocol was introduced. Therefore, the cells still had high series resistance around the edges as shown on maximum power current EL image in Fig.5-7 (left). Another difference with lot HI0042 was using a different Ag paste. The paste used in HI0068 had a slightly higher resistivity (about20 mΩ/□ compared to 15-17 mΩ/□ for the cells in HI0042). The overall printing quality was poor due to screen clogging. The printed grid had thin wavy fingers with characteristic thinning near the

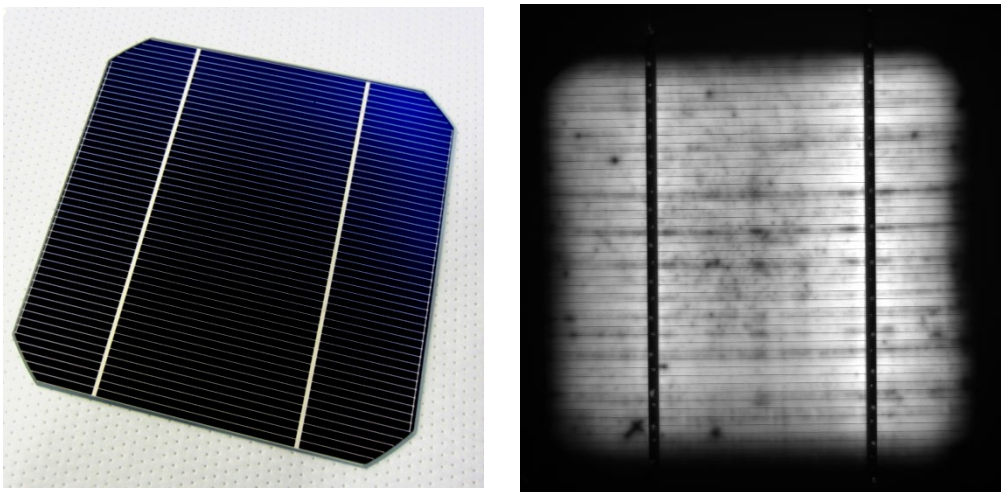


Fig.5-9. The cell from lot HI0068 with improved printing and stainless steel mask used for ITO edge isolation. Left – photo. Right – maximum power current EL image. The cell still had high series resistance around the edge suggesting that it is caused by handling rather than outgassing of Kapton tape.

busbars.3D optical profiles demonstrating characteristic shape of the fingers in lots HI0042 and HI0068 are shown in Fig.5-8.

As a result, the FF of the cells in HI0068 was only 70.4% instead of the 75.7% predicted by the series resistance model.

5.4 Improved Printing and Edge Isolation

In order to improve the quality of printing and avoid clogging a new screen, less dense mesh was purchased (mesh value was equal to 290 instead of 320 used previously). The used screen had 2 busbars, 2.2 mm finger spacing and 100 micron finger width. Also, in order to eliminate edge resistance, stainless steel shadow masks were applied to the wafers from lot HI0068 during ITO deposition. It turned out, though, that the cells still had edge resistance. This implied that outgassing of Kapton tape was not the only reason for it (see maximum power current EL images in Fig.5-9). It means that either the

Table 5-4.The performance of the cells in lot HI0068 measured using 10x10 cm^2 shadow mask with good printing quality and using aluminum shadow mask during ITO deposition for edge isolation.

Cell ID	Area	Jsc	Voc	pFF	FF	R_S	Eff
	(cm2)	(mA/cm2)	mV	%	%	Ohm-cm^2	%
HI0068-11	100	36.4	717	79.8	74.5	0.99	19.5
HI0068-12	100	36.3	714	78.9	74.3	0.95	19.3
HI0068-13	100	36.4	714	79.9	75.6	0.74	19.7
HI0068-14	100	36.5	712	79.5	73.5	1.24	19.1

process sequence of avoiding handling of the wafers by the gloves should be developed, or the wafers would have to be cleaned in either Piranha or RCA-a solutions prior to ITO deposition. Another short term solution could be using 10x10 cm^2 ITO islands on the wafer so that the cell area does not include the area degraded due to handling.

In order to neutralize the effects of edge resistance, the cells were measured using a 10x10 cm^2 shadow mask. Measured this way, the cells achieved <1 Ohm-cm^2 series resistance which is the lowest resistance measured in this work on large area devices. The performance of the cells measured with a shadow mask is summarized in Table 5-4. Because one third of the cell area was shadowed, it worked as a diode in the dark connected in parallel to the illuminated area of the cell which increased recombination losses. As a result, the V_{OC} and pFF of the masked cells was only 712-717 mV and 79-80% correspondingly. On the other side, using thinner (n+)a-Si and 2 busbars allowed to achieve 36.4 mA/cm^2 J_{SC}.

One additional loss mechanism in the cells from HI0068 is a relatively large area around the edge shaded by the mask during ITO deposition. The perimeter area without

ITO did not contribute to current collection and can be responsible for up to 0.5 mA/cm^2 loss of J_{SC} when the cell is measured shaded side up. An alternative edge isolation technique should be developed in order to minimize this loss. For example, wet or plasma etch on coin stacked cells could be done in order to etch ITO only at the very edge of the wafer leaving the film on the active side.

Another problem can be the time between a-Si and ITO depositions. Ideally, a-Si would be capped by ITO immediately after being deposited in the same tool without leaving the vacuum. In this work, however, the wafers were stored in plastic boxes for 1-10 days prior for ITO deposition. 2-4 hours before ITO sputtering, the wafers were dipped in BOE to remove the native oxide. 2-4 hours, however, was enough to reoxidize the surfaces again. Thus, there could be an additional series resistance component caused by a thin native oxide layer between a-Si and ITO.

Finally, there was an additional loss of J_{SC} and FF due to using a bifacial cell design. J_{SC} reduced due to the transmittance of IR light through the rear side of the cell. A blank metal deposition at the rear side of the cell in combination with a thick low index TCO should be used to reduce the losses of IR light. FF reduced because the cells were measured on the chuck which makes electrical contact only with the fingers protrusive from the wafer by about 10-35 microns. This circumstance adds lateral ITO resistance at the rear side to the overall series resistance of the cell.

In summary, the cells with 730 mV V_{OC} and 82% pFF on industrial CZ material were fabricated. The performance of the cells was limited mainly by a low FF which is due to the bulk resistivity of the paste and several fabrication process deficiencies. Maximum efficiency equal to 19.5% was achieved on the cell measured using 10x10 cm^2

shadow mask. Provided these losses are mitigated, the current process can achieve 20% efficiency. The analysis of optical and recombination losses is presented in Chapter 6.

5.5 Solar Cells with Cu Plated Grid

The wafers from the lot HI0068 were also sent to UNSW to do the plating of Cu. The photo of the plated cell and the IV curve measured at UNSW are shown in Fig. 5-10. The area of the cell (3.6 cm^2) was defined by the aperture mask. The width of the fingers was approximately 40 microns, the spacing between the fingers was 1 mm.

The real FF of Cu plated cells turned out to be 82.8% suggesting that the fabricated cells had a low internal series resistance. For the details of plating process the reader is referred to UNSW metallization team headed by Dr. Alison Lennon.

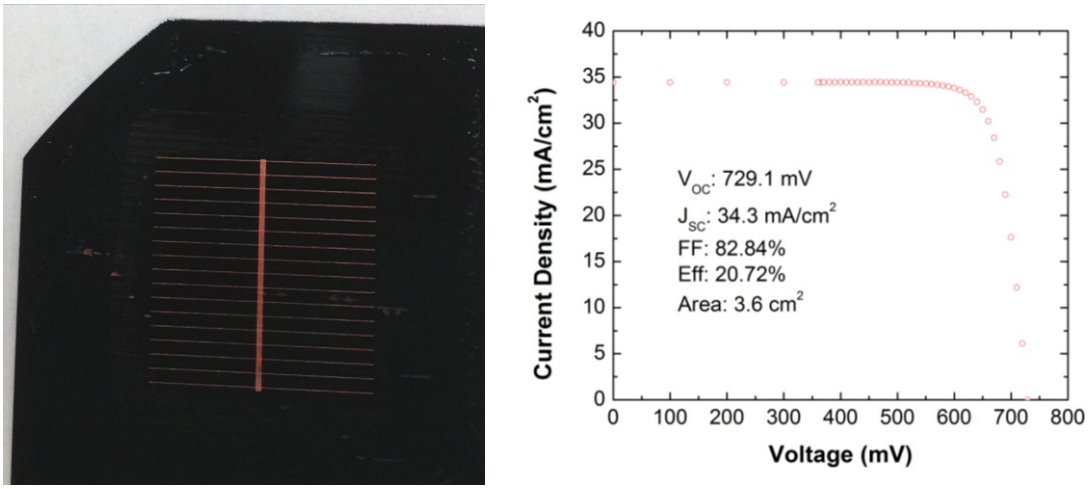


Fig.5-10. Cu plated SHJ cell from lot HI0068 (left) and its light IV curve (right). The cell achieved 82% FF and 20.7 efficiency measured using 3.6 cm^2 aperture mask. Plating was done by Vincent Allen from UNSW metallization team.

Chapter 6
MODELING AND LOSS ANALYSIS

As was discussed in Section5.4, the current SHJ cell process flow had a number of drawbacks which could be relatively easily eliminated to allow 20% efficiency large area wafers. In order to achieve >20% efficiency other power loss mechanisms need to be addressed. To understand power losses in the fabricated SHJ cell this work used analytical recombination and external series resistance models coupled with the optical model built using a ray tracing software. First, the validity and limitations of the used models are described. Then, the results of optical, recombination, and resistance simulations are presented in the form of power loss analysis. The chapter ends with the discussion of the potential improvements necessary to achieve >22% and >25% efficiency SHJ solar cell.

6.1 Analytical Model of SHJ Solar Cell

Recently, a number of groups have published studies of SHJ solar cells in which numerical simulators such as Sentaurus have been used. The subjects of these studies were the recombination at a-Si/c-Si interface (which determines V_{OC} and pFF)[138][139][140], the transport through a-Si/c-Si interface (which determines internal series resistance and, hence, contributes to the reduction of FF)[125], and the performance of SHJ cells having 2- or 3-dimensional unit symmetry cell (for example, silicon heterojunction interdigitated back contact solar cell)[141][126]. The models built using numerical simulators usually consider fundamental material parameters such as the

distribution and nature of defect states in the band gap of a-Si films and at a-Si/c-Si interface, the band structure of the ITO/a-Si/c-Si heterointerface (band offsets at a-Si/c-Si interface and Fermi level position in a-Si), as well as various transport mechanisms occurring in the device such as trap assisted and direct tunneling. Using a numerical approach to simulate recombination and transport in SHJ cells is fundamentally limited due to a number of reasons. 1) The first reason is that the necessary material parameters are very difficult to measure. 2) The second reason is that the properties of a-Si films and ITO/a-Si/c-Si heterojunction strongly depend on the deposition conditions which significantly differ between different groups. This fact limits the use of material properties reported by other groups. 3) The last reason is the absence of clear understanding of transport mechanisms taking place at ITO/a-Si/c-Si interface.

As a result, it seems very problematic to use numerical models in solving the basic tradeoffs in the design of SHJ cells such as the optimization of a-Si thicknesses. Numerical models, however, are necessary in order to design SHJ cells with 2- or 3-dimensional symmetry of carrier collectors, such as interdigitated back contact cells or point contact cells. Besides, numerical simulations can yield a deeper understanding of recombination and transport mechanisms taking place in SHJ cells. Therefore, further development of numerical models seems important.

This work, however, used an analytical model which relied on two main simplifications: 1) the effective recombination parameters extracted from the measured $\tau_{eff}(\Delta n)$ on non-metallized SHJ cell can be used to treat recombination losses; 2) and the internal series resistance associated with the transport through ITO/a-Si/c-Si interface is

small compared to external series resistance in the metal grid and therefore can be neglected.

One important property of SHJ cells making them convenient to simulate using analytical model is their one dimensional symmetry. It means that surface recombination properties in SHJ cells are homogeneous across the entire surface of the wafer. Therefore, surface recombination can be directly measured on the actual solar cell by lifetime tester without using area weighted recombination parameters measured on specially prepared test structures. Another important property of SHJ cells is that their recombination properties are finally defined prior to metallization. Therefore effective minority carrier lifetime measured after ITO deposition and curing is representative of the recombination properties of the complete solar cell. Due to this fact, the implied V_{OC} and implied pFF extracted from the $\tau_{eff}(\Delta n)$ curve measured after ITO deposition represent the V_{OC} and pFF of the complete SHJ solar cell to the accuracy of passivation uniformity across the wafer. For example, recombination in the conventional diffused junction cell cannot be directly measured and is usually obtained by putting together separately measured recombination properties of the wafer bulk, front surface emitter, rear surface BSF, and metal contacts.

With the above simplifications, the SHJ cell can be simulated by using a basic equation of the diode under light. The disadvantage of the applied approach, however, is that the insight into recombination at ITO/a-Si/c-Si interface such as the fraction of the carriers recombined through c-Si surface states compared to the carriers recombined through a-Si states and carriers recombined in the bulk of the wafer cannot be obtained. Another drawback of analytical model is that it doesn't treat the transport through ITO/a-

Si/c-Si interface which may have a strong effect on the FF of the solar cell. For example, as was previously shown by numerical simulations, several parameters of (i)a-Si:H such as band gap and thickness, may add series resistance or cause 'S-shape' behavior of the IV curve producing very low FF[125][126].

Finally, the author believes that due to a high complexity of the numerical models of SHJ solar cells and due to the strong dependence of material and device parameters on plasma deposition which presently cannot be simulated, the use of numerical simulations in predicting material and device parameters is limited. This work demonstrated that very good device performance can be achieved using empirical optimization of the films with only five optimization parameters: passivation quality for (i)a-Si film on polished wafer, passivation quality for (i)a-Si film on textured wafer, bulk conductivity for doped a-Si films, conductivity and transmittance of ITO, and thickness of all films. Numerical models of recombination and transport processes, however, would be necessary in the future when advance structures are tested in order to reach >25% efficiencies. The examples of these structures include using different materials to form a heterojunction (for example, GaP), using graded layers of a-Si with different doping or crystallinity, and using three-dimensional geometries such as interdigitated back contact or point contact cells.

6.2 Band Diagram of SHJ Solar Cell

Sketching a band diagram is a powerful tool in the analysis of a solar cell operation. The exact structure of the band diagram of the specific a-Si/c-Si system, however, is difficult to obtain due to the difficulty in measuring the necessary material

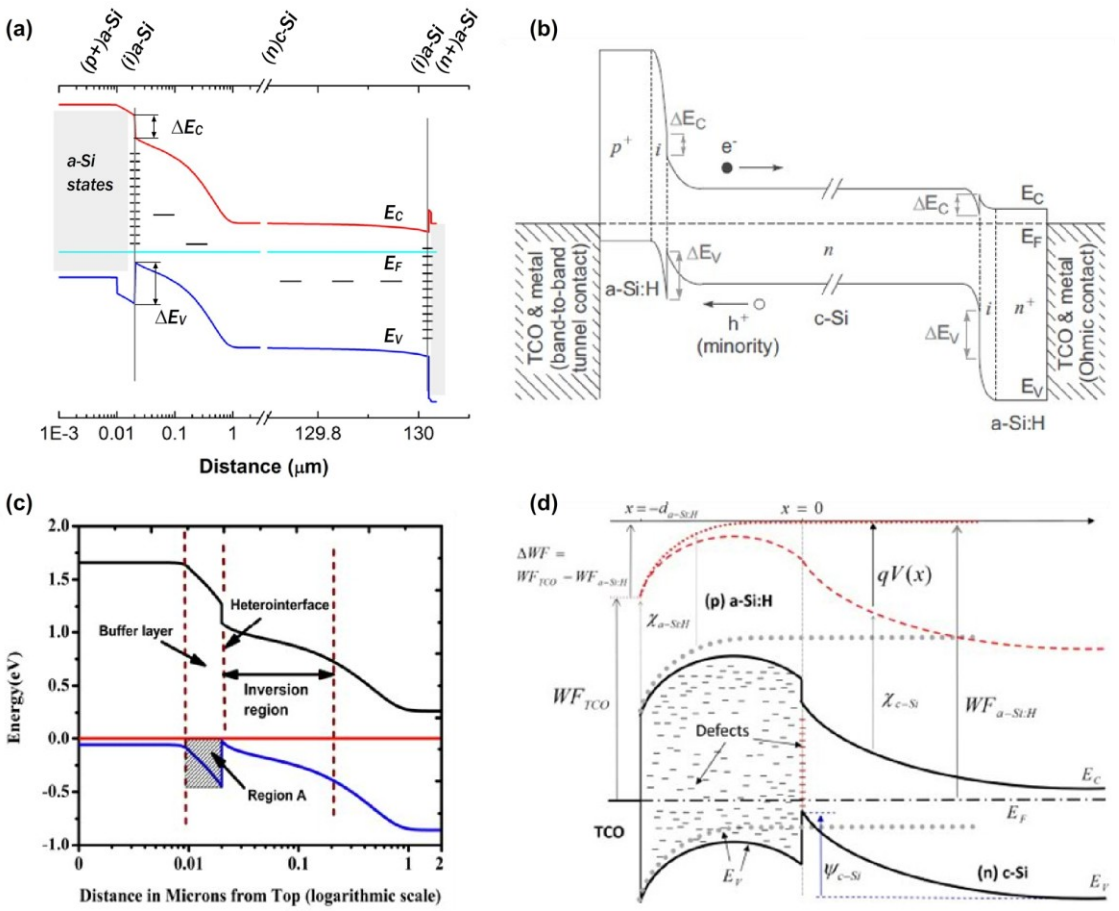


Fig.6-1. A comparison of a schematic band diagram used in this work (a) to the band diagrams of (p+)a-Si/(i)a-Si:H/(n)c-Si heterojunction solar cell reported in the literature (b and d) to the band diagram simulated using Sentaurus TCAD (c).

parameters, such as band offsets. Therefore, this work used the band diagrams generated in a numerical simulator PC1D [142] only for quantitative description of the SHJ solar cell operation. Fig.6-1 compares equilibrium band diagrams of SHJ cells with n-type c-Si base and p-type a-Si minority carriers collector reported in the literature with the band diagram generated by PC1D.

The comparison shows that PC1D generates a band diagram similar to what is generally considered to be a band diagram of SHJ solar cell. The model built in PC1D is

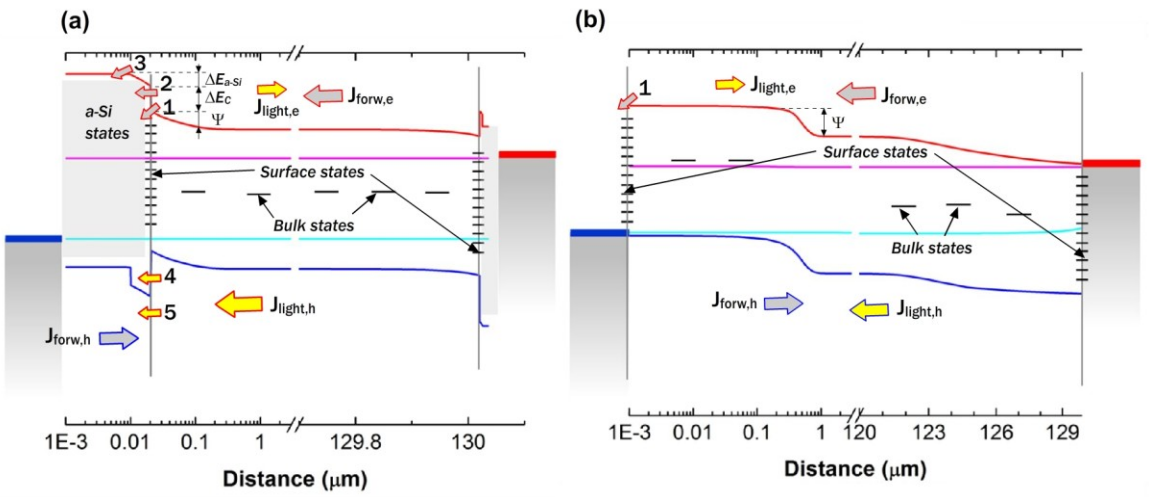


Fig.6-2. A comparison of the schematic band diagrams of silicon heterojunction (left) and diffused junction (right) cells at maximum power operation. The arrows indicate the flows of recombination (grey fill) and light generated (yellow fill) currents.

missing ITO and therefore cannot treat an additional band bending at a-Si/c-Si interface due to ITO work function. However, if the doping and thickness of (p+)a-Si are sufficient to sustain the band bending induced by ITO, which is the case for properly designed SHJ cell, ITO will not have any effect on a-Si/c-Si interface. Note also the visual differences between the band diagrams is due to the difference in the choice of the scale and the limits of the X axis.

Fig.6-2 compares band diagrams of a-Si/c-Si heterojunction solar cell with (p+)a-Si/(n)c-Si heterojunction and a p+/n/n+ diffused junction solar cell with boron emitter and phosphorus back surface field at maximum power point operation, i.e. under light and ~0.6-0.7 V electrical bias. Blue and red arrows with grey fill on the diagram represent hole and electron forward recombination currents, whereas the arrows with yellow fill represent light generated hole and electron currents respectively. The diagram also shows the location of surface recombination states originating from the dangling

bonds at the surface of c-Si wafer, the states in the bulk of the wafer which are due to impurity atoms or crystalline defects, and also the states in the bulk of a-Si films which are represented as the areas with the grey fill. Conduction band offset is labeled as ΔE_C, the built in potential is labeled as Ψ and potential difference in (i)a-Si:H is labeled as $\Delta E_{a\text{-}Si.}$

On the minority carrier collector side, i.e. at the (p+)a-Si/(n)c-Si side, the heterojunction has four main features which distinguish it from the p+/n diffused junction.

1. The first feature of SHJ is a different distribution and location of defect states near the surface which give origin to SRH recombination and, thus, contribute to forward recombination current of a diode. Three SRH recombination mechanisms are labeled in Fig.6-2 by the numbers 1, 2, and 3. Number one is recombination current due to electrons which overcome a voltage dependent potential barrier Ψ and reach surface states. $\Psi$is formed due to a band bending at c-Si surface. Because of the very small thickness and high doping of a-Si almost 100% of band bending occurs in the c-Si wafer causing the inversion of the surface. The amount of bending will depend on the doping of (p+)a-Si, i.e. the position of the Fermi level, which can be estimated by measuring the activation energy (extracted from the temperature dependent conductivity data). A strong band bending is necessary in order to get a high barrier Ψ and, hence, a high V_{OC} of the solar cell.

2. The second recombination mechanism is due to the electrons having energies with the values within the sum of Ψ and conduction band offset ΔE_C. Band offsets appear due to the difference in the band structure between a-Si and c-Si, in particular, the band gaps and electron affinities. The value of the offset in the conduction band and the valence band can be measured by UV photoelectron spectroscopy[143][144] and used in the model by adjusting the combination of band gap, doping and electron affinity. These high energy electrons have the probability to recombine through the bulk states in (i)a-Si:H through the trap assisted tunneling. Additionally, if (i)a-Si:H is thin enough, they have additional probability to reach (p+)a-Si with higher density of bulk defects and recombine through them. Finally, most energetic electrons which can overcome the potential barrier composed of Ψ, ΔE_C and band bending in (i)a-Si:H defined as $\Delta E_{a\text{-}Si}$, quickly recombine in through defect states in (p+)a-Si which is known to have the lifetime of the order of picoseconds[145]. It should be added here that the height of the potential barrier Ψ shielding bulk electrons from the surface states in SHJ cells is lower than in diffused junction cells imposing higher requirements on the passivation quality of the surface.
3. The passivation of the surface in SHJ cells can be more efficient, since diffusion of dopants (as a process) and dopant atoms themselves create additional defect states at the surface and in the vicinity of the surface, thus, reducing the effectiveness of passivation. For example, surface recombination velocity was experimentally measured to increase with the increased surface

concentration of dopant atoms[84]. In SHJ solar cells, the junction is induced and, thus, the surface passivated by the equivalent film may have lower density of defect states.

4. Another feature of SHJ is a lower concentration of majority carriers at the surface which are holes in the case of (p+)a-Si/(n)c-Si heterojunction. Whereas in diffused junction cells holes density is usually between $1x10^{18}$ and $5x10^{20}$ cm^{-3}, band bending in SHJ cell usually creates an inversion layer with only $1x10^{16}$-$1x10^{17}$ cm^{-3} holes which may also reduce Auger recombination as compared to the diffused junction.
5. Finally, the fourth difference is the presence of the valence band offset ΔE_V which may be an obstacle for light generated current of holes from the bulk of the wafer into (p+)a-Si collector in the case of improper cell design. The transport through the barrier formed by (i)a-Si is a topic of experimental and theoretical studies. It is believed that the transport is due to either trap assisted tunneling or thermionic emission of holes accelerated by the electric field present near the interface.

In summary, in SHJ cells, the minority carriers in the vicinity of the surface interact with well passivated surface states and additionally available a-Si states which are shielded from the minority carriers by a voltage dependent potential barrier and valence band offsets. In their turn, minority carriers in the diffused junction cell 'see' higher density of surface states, and have more opportunities for Auger and bulk SRH recombination in the emitter while they are shielded by a higher voltage dependent

potential barrier. Additionally, in the diffused junction cells, approximately 6% of surface area is metalized, where metal-silicon interface has a very high density of surface states.

6.3 Increasing V_{OC} of the Devices Based on a p-n Junction.

From the analysis of the band diagrams of SHJ and diffused junction cells, it follows that despite having several differences, their fundamental operation is similar and can be described by a diode equation by measuring or fitting dark saturation current densities and ideality factors. This will require the assumption that all recombination mechanisms taking place in SHJ cells are increasing exponentially with applied bias (alternatively one can say that recombination current is linear with carrier density at the boundary of the induced junction).

Based on the band diagram analysis, this section discusses the ways to increase the V_{OC} of SHJ cells. The discussion focuses on the minority carrier collector side of the cell and assumes that the device has a perfect majority carrier collector / minority carrier mirror. In order to increase the V_{OC} of the solar cell, one has to reduce forward current of a diode which is directed opposite to the light generation current. It should be noted here that recombination in conventional SHJ cell is so low, that light generated current from the bulk, i.e. $J_{light,h}$, is practically not affected by recombination and collection probability of the carriers generated in the wafer is 100%. $J_{light,h}$ is, thus, only reduced due to the forward recombination currents of the diode. Forward recombination current in an SHJ cell is determined by the height of the voltage dependent potential barrier, energy distribution of majority carriers and recombination mechanisms available for minority carriers.

The natural way to reduce the forward current would be to increase the potential barrier by higher doping in both sides of the junction. This will, however, increase Auger recombination and increase the average energy of the carriers in the conduction band. Thus, although the barrier can be increased by stronger doping, recombination current is still high, since more carriers with high energy capable to overcome the barrier will be available and more Auger recombination events will take place. Richter et al. recently published an updated parametrization of intrinsic recombination (cumulative Auger and radiative)[146] which was followed by the publication predicting the efficiency of c-Si solar cell limited by Auger and radiative recombination[147]. For example, using Richter parametrization, intrinsic V_{OC} limit for 0.1 Ohm-cm ($8x10^{16}$ cm^{-3} dopants) 150 μm thick n-type wafer will be only 698 mV, whereas for 10 Ohm-cm material it is 746 mV. Therefore, doping is always a matter of tradeoff which may also include internal resistance of the wafer. As a result, typical n-type material for SHJ cells has 1-10 Ohm-cm resistivity ($4.5x10^{15}$ – $5\ x10^{15}$ cm^{-3} doping density).

Another conventional way to reduce forward current is to reduce recombination paths for minority carriers. This is done by reducing the density of bulk defects and impurities, using light diffusions and high quality passivating films. For example, using FZ material (or high lifetime CZ material) and a-Si heterojunction passivation can allow Auger limited devices as was demonstrated during this work (see Section 7.2 for details). Reduction of recombination, however, is involved in multiple technological, design, and cost related tradeoffs. The V_{OC} of most solar cells is improved by taking exactly this path.

Finally, several hypothetical features which can increase the V_{OC} in SHJ cells are listed below. One way to reduce electron recombination current is to increase the

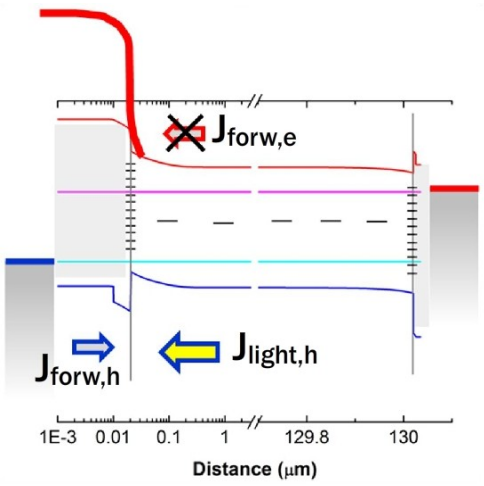


Fig.6-3. A schematic band diagram of a heterojunction solar cell where a forward electron current is suppressed by a high conduction band offset at the heterointerface. This way a device with the forward current dominated by a single type of carriers can be obtained. Such material systems, for example, exist in heterojunctions based on III-V alloys.

conduction band potential barrier for forward current of electrons from n-type base to p+ holes collector as shown in Fig.6-3.

This is, for example, possible in heterojunction devices based on III-V material where forward current is dominated by a single type of carriers[150]. To some extent, this mechanism takes place in SHJ solar cells too. However, in SHJ cells, the barrier separating the surface states from the electrons in the base is not high enough to reflect all minority carriers and the device is still sensitive to the density of surface states. Moreover, both intrinsic and p+ doped a-Si have high density of defect states in the band gap (higher in p+ a-Si) which provides additional recombination paths through the mechanism of trap assisted tunneling. Therefore, a hypothetical material inducing strong band bending shielding electrons from the surface would be necessary to reduce a forward current of electrons. In addition, high enough band bending would relax the

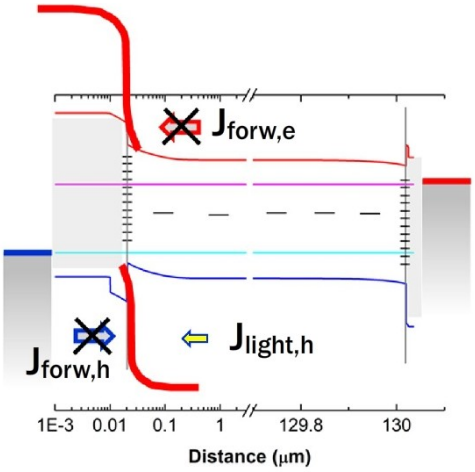


Fig.6-4.A schematic band diagram showing a way to reduce hole forward current by increasing a potential barrier in the valence band. This can be done, for example, by using higher band gap absorbers. Higher band gap materials, however, will absorb less IR light and light generation current can reduce.

requirement on the density of surface states and bulk defects of the band bending inducing material. One final requirement would be high transparency. Solar cells with forward current dominated by a single carrier type can be realized using III-V/Si material systems, for example, GaP/Si. As was mentioned in Section 1.6, the performance of the GaP/Si minority carrier collectors was theoretically described and predicted to achieve reasonably low dark saturation currents. Early experimental works, however, didn't achieve notable performance.

The next option would be to increase the barrier for the holes forward current, which can be done by using higher band gap absorbers (Fig.6-4). Higher band gap materials will, of course, have lower absorption coefficient reducing light generated current. Thus, this case just described the standard tradeoff between the junctions based on high and low band gap material.

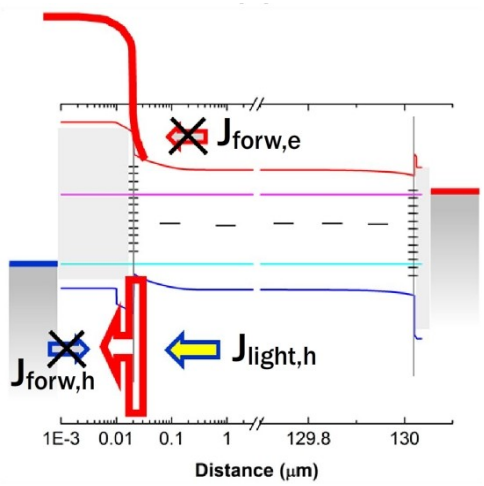


Fig.6-5. A schematic band diagram of a hypothetical heterojunction solar cell realizing a hole membrane in the valence band which would pass light generated holes towards the hole collector, but prohibit the forward recombination current of holes. Note that such material systems have not been demonstrated yet and may be fundamentally impossible.

An alternative to simply using higher band gap absorbers would be a hole membrane which would conduct the holes only in one direction as shown in Fig.6-5. The membrane would conduct light generated holes towards hole collector, but would not conduct the holes the other way, thus, neutralizing forward hole recombination current. The author, however, is not aware of a material system capable of realizing a charge membrane rather than a p-n junction where the 'membrane' action is voltage dependent.

It follows that V_{OC} and pFF of SHJ cells will be fundamentally limited by Auger recombination in the wafer which will give rise to the forward recombination current. This phenomenon will take place unless alternative material systems presumably based on III-V/Si heterojunctions are introduced in order to create the barrier for forward currents of electrons and holes. III-V/Si heterojunction can also potentially be used instead of (n)c-Si/(i)a-Si:H/(n+)a-Si heterojunction to form a majority carrier collector /

minority carrier mirror. Thus, the only way to increase V_{OC} in Auger limited devices is to thin the wafer, which will increase carrier density. However, to gain from the increased V_{OC}, thin wafers will require advanced light trapping schemes, which will allow to overcome a $4n^2$ limit. Without advanced light trapping, the optimum thickness of the wafer from the efficiency point of view will remain at around 100 microns as shown by Richter et al.

6.4 Optical Losses

Optical losses are commonly cited as the Achilles' heel of SHJ solar cells. Indeed, the front side of SHJ cell has a-Si layers with a high absorption coefficient and very low collection probability and approximately 80 nm of ITO with noticeable absorption in the visible range. As a result, SHJ cell usually have poor response below 600 nm as compared to the cells with diffused carrier collectors. In addition a large fraction of IR photons are absorbed in front and rear ITO which further reduces generation current. Finally, standard SHJ cells suffer from shading by the front metal grid. This section summarizes and quantifies optical loss mechanisms acting in SHJ solar cells. Potential ways to improve generation current are considered.

6.4.1 Model Description

This work used a three dimensional Monte Carlo ray tracer Sunrays to simulate the optical performance of the SHJ solar cell[148]. The wafers with random pyramids from both sides were simulated. The entrance of the rays to the simulation domain was randomized. The program simulated the path of 5,000 rays for each fifth wavelength in 300-1100 nm interval. The base of the pyramids was 3 microns which produced 9.5%

reflectance at 700 nm. Since the texturing used in this work resulted in the pyramids with 10.5-12% reflectance at 700 nm a flat area 0.2 microns wide was added to the geometry in order to produce the measured values of reflectance.

Optical constants of a-Si and ITO films were measured on <100> mirror polished c-Si wafer by spectroscopic ellipsometry. The measured optical constants used in this work are plotted in Fig.3-10. Optical constants for a-Si films with a device relevant thickness (10-15 nm) cured at 200 ^{o}C for 30 min averaged over the data measured on 5 wafers were used. Note that optical properties of a-Si films grown on <111> textured surfaces could differ from the films deposited on <100> surface. The simulation yielded cumulative generation rate profile, a total generation current and spectra of quantum efficiency, reflectance, transmittance and parasitic absorbance.

Optical losses can be analyzed by comparing QE and 1-R curves measured on the solar cells. Typical optical losses of an SHJ solar cell are summarized in Fig.6-6. The losses include parasitic absorption of visible light in the front ITO, parasitic absorption of visible light in a-Si films, parasitic absorption or IR light in the front and rear ITO films, IR absorption in rear metal, IR transmittance in the case of bifacial cells, front side reflectance, escape reflectance and, finally, the shading by the front grid.

There are two approaches which can be used to analyze parasitic absorption losses using the data generated by ray tracing software. In the first approach, the extinction coefficient (k) of the studied film is set to zero while refractive index is kept equal to the refractive index of the actual film. In the second approach the film is replaced with the hypothetical film having zero or lower k and different refractive index which will be representative of the alternative SHJ cell structure. For example, a-Si can be replaced

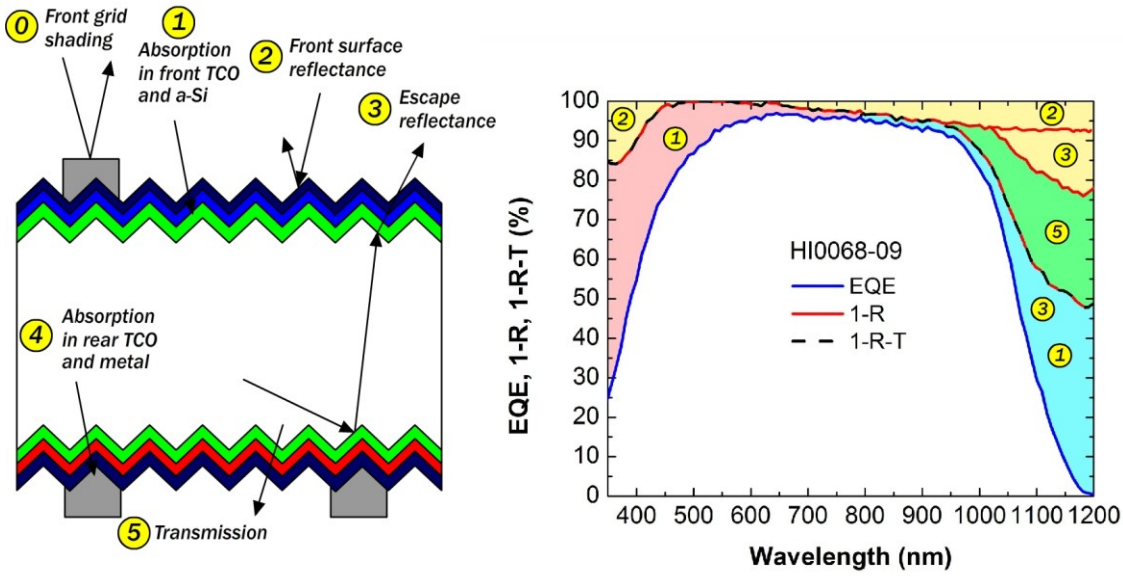


Fig.6-6. A schematic diagram showing 5 main optical loss mechanisms acting in a bifacial SHJ solar cell (left). The graph to the right shows a simulated quantum efficiency, 1 – Reflectance and 1 – Reflectance – Transmittance plots, where 100% would correspond to a complete absorption of the particular photons in c-Si wafer.

with thin thermal SiO_2or Al_2O_3 and ITO can be replaced with SiN_x. Note that in practice, having SiN_x on the front surface requires the use of different cell geometry, for example, interdigitation of n+ and p+ carrier collectors at the rear surface since a standard structure of SHJ cell requires a layer for lateral conduction at the front surface. QE of the simulated structures are compared yielding the contribution of the studied films in parasitic absorption.

6.4.2 Simulation of HI0068 Cell

This section presents optical simulation of a cell from lot HI0068 which achieved 18.4% efficiency. The cell had 135 micron thick double side textured substrate, approximately 80 nm thick ITO on both sides, and 17 nm a-Si layers on both sides. Ag

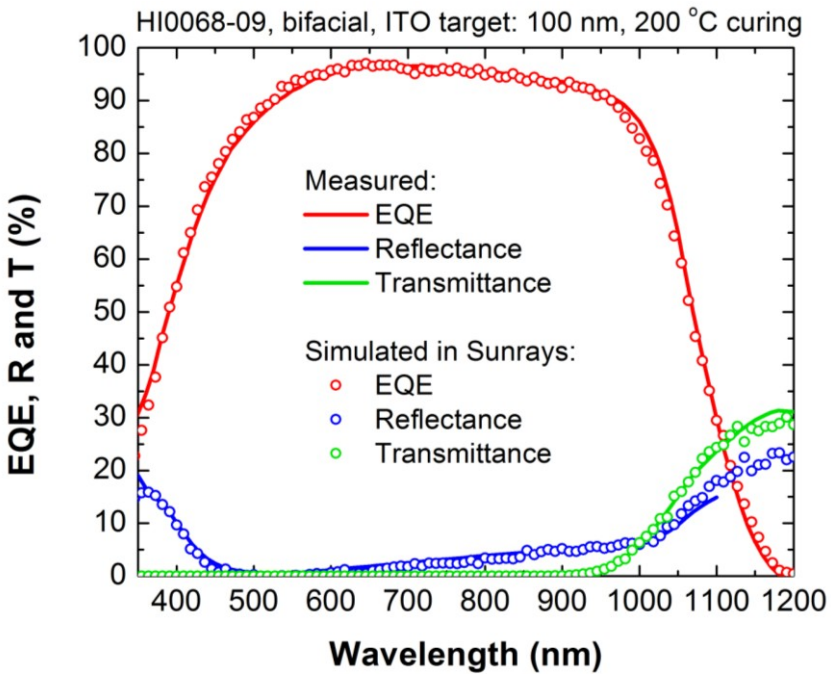


Fig.6-7. Quantum efficiency and reflectance simulated in Sunrays and the measured QE and reflectance for the cells from lot HI0068. Note that PV Measurement X10 tool which was used in this work for measuring QE, reflectance and transmittance only allowed to measure reflectance up to 1100 nm.

grid was printed using the screen with 3 busbars, 100 micron finger openings, and 2.2 mm finger spacing.

First, the optical model was evaluated by comparing simulated and measured quantum efficiency, reflectance, and transmittance curves. Simulated QE, R and T of the optical structure representative of the cell from the lot HI0068 together with the measured data are shown in Fig.6-7. A good match indicated that the built optical model could adequately treat the considered devices. Note that reflectance was only measured up to 1100 nm due to the limitation of the spectrophotometer used in this work (Si detector). The model was then used to analyze parasitic absorption and IR escape reflectance losses in the cell HI0068.

6.4.3 Parasitic Absorption in a-Si and ITO

Fig.6-8 shows the simulated hypothetical SHJ cells where the extinction coefficient was set to zero alternatively in a-Si and ITO films. The figure also shows the values of generation current for the corresponding case. The simulation shows that the front ITO is responsible for approximately 1.5 mA/cm^2 loss of J_{gen}. The major part of the los is a broadband absorption in the visible range (300-600 nm) and a relatively

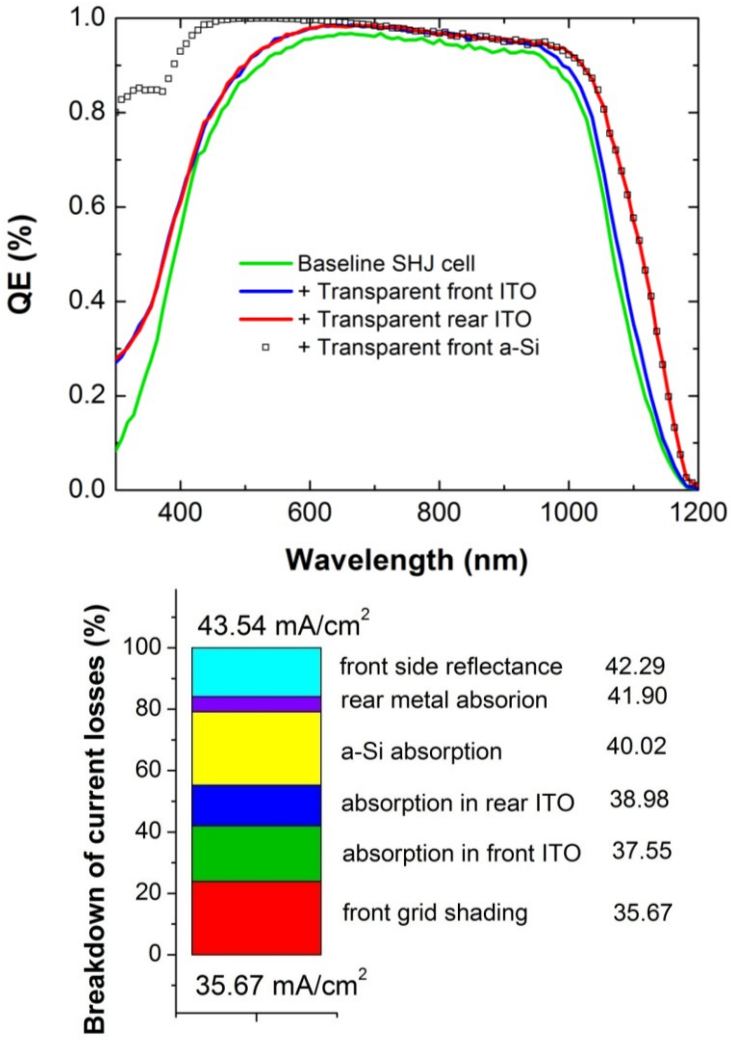


Fig.6-8.Simulated QE curves of SHJ solar cells where absorption coefficients were set to zero in a particular filmand the breakdown of optical loss mechanisms.

homogeneous absorption in the IR. ITO at the back side absorbs the photons with long wavelengths (950-1200 nm) with optical path length longer than the thickness of the wafer. A-Si films at the front side have a strong absorption in 300-550 nm range which results in about 1.9 mA/cm^2 current drop.

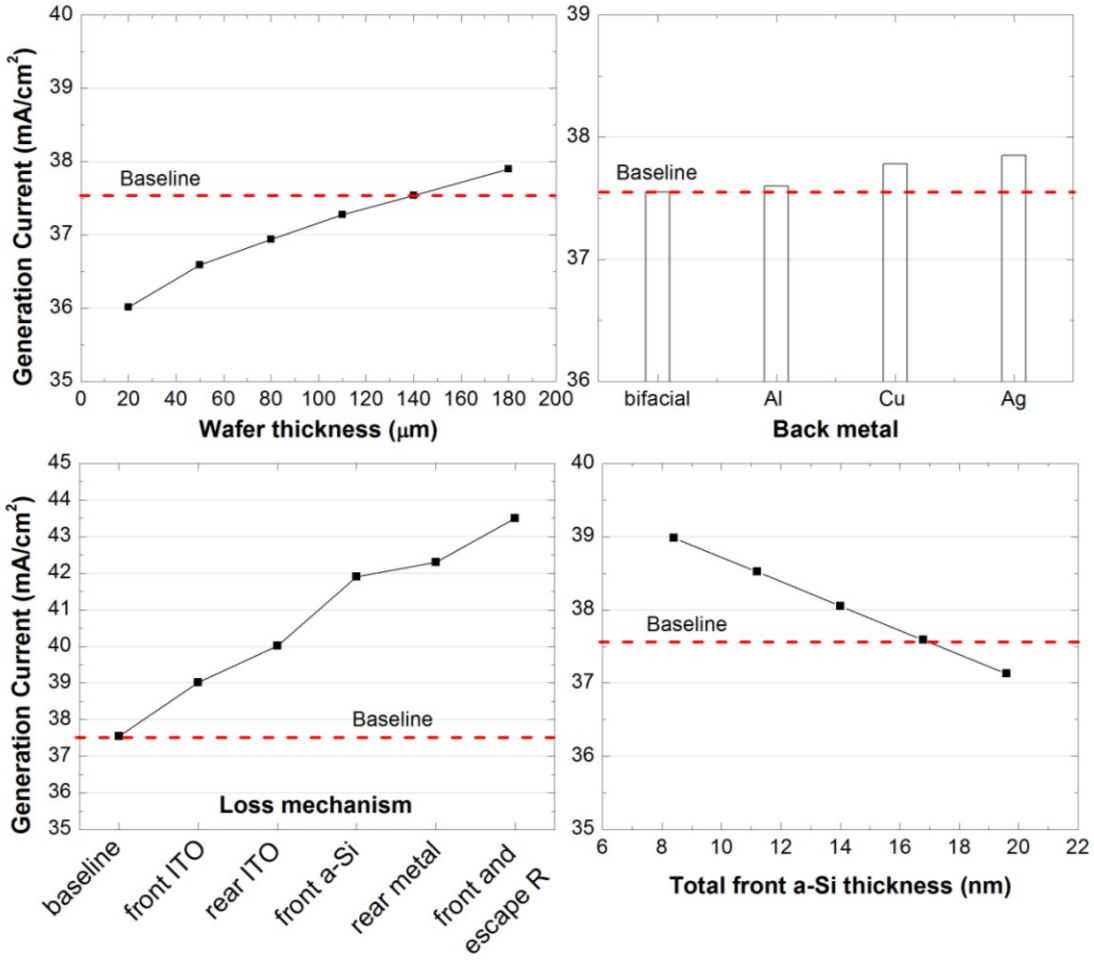


Fig.6-9.Generation current simulated in Sunrays for different variations of the baseline cells from lot HI0068. Wafer thickness, back surface metal layer as well as the cumulative thickness of a-Si films on the front surface were varied. Note that although intrinsic and doped a-Si have different optical constants (see Fig.3-10), the thickness of intrinsic film was varied for simplicity. The results are compared to the baseline J_{gen} which is representative of a cell from the lot HI0068.

6.4.4 The Ways to Increase Generation Current

Fig.6-9 summarizes optical losses for different practical optical structures in terms of J_{gen}. This work considered optical models of SHJ cells with varying a-Si thicknesses, varying wafer thickness, and various back metal reflectors. The figure also shows the breakdown of optical losses in a baseline SHJ solar cell (140 μm thick wafer, total a-Si thickness on the front side is 17 nm, 80 nm ITO on both sides, bifacial).

Note also that unlike a standard diffused junction solar cell, a typical SHJ cell with ~730 mV V_{OC} has negligible recombination losses at J_{SC}, and therefore its QE is determined solely by the optical losses. One exception can be the collection from the (i)a-Si films which is not considered in the model.

Recently, Holman et al. published the results of a comprehensive study of optical loss mechanisms in SHJ solar cells[124][129]. One of their main findings was that IR losses at the rear side of the cell can be reduced by using approximately 150-200 nm thick low carrier density ITO which can serve as a better back side reflector. Later, they published the performance of the devices having an optimized ITO/MgF_2 stack with local metal contacts at the rear surface with very high IR quantum efficiency[149]. The improved performance was due to a superior IR reflectance of ITO/MgF_2 stack as compared to conventional ITO/Ag or ITO/Cu stacks. Since this work could not vary optical properties of ITO film, no optimization of optical losses associated with back side reflection and parasitic absorption in ITO was done.

The graph in Fig.6-9 also compares the performance of SHJ cells with rear metal reflectors. It follows that sputtering Al at the rear side will not increase generation current since IR light escaping through the rear side in bifacial cell will now be absorbed in rear

Al, rear ITO, and will also contribute to front escape reflectance. Ag mirror in its turn can add approximately 0.3 mA/cm^2 generation current. Note that using Al (or Ti/Al, Ni/Al, and other stacks)at the rear surface can still be useful providing the rear TCO is optimized to have low IR absorption and good contact resistance to a particular metal.

6.5 Recombination Losses

As was pointed out in Section 6.3, V_{OC} of all silicon solar cells including SHJ cells is fundamentally limited by the combined bulk Auger and radiative recombination. In this section, analytical recombination model is applied to simulate V_{OC} and pFF a solar cell from the lot HI0068. The model yields the breakdown of recombination for different device parameters and suggests the potential ways to increase V_{OC} and pFF. It will be shown that surface passivation achieved in this work resulted in the situation when approximately half recombination at V_{OC} is due to Auger recombination. The recombination at maximum power point, however, is still dominated by surface recombination limiting the pFF.

6.5.1 Model Description

Recombination losses can affect all three device parameters: J_{SC}, FF and V_{OC}. However, the most sensitive to the changes in recombination is V_{OC}. J_{SC} in a SHJ solar cells is usually not affected by recombination and is equal to the generation current minus front grid shading losses. As was discussed in Section 2.1.1, the structure of SHJ cell allows to determine the implied V_{OC} and pFF of the complete solar cell prior to the metallization step with finally defined recombination properties.

Both IV curve and $\tau_{eff}(\Delta n)$ curve are the functions of recombination mechanisms acting in the solar cell and therefore are related with each other. IV and effective lifetime curves, thus, can be expressed in terms of recombination rates. Since recombination processes in a solar cell depend on minority carrier density, they can be calculated for a wide range of minority carrier densities and then used to analyze the performance of the device at different operation points.

Either electrical bias or excess carrier density can be used as a free variable. This work used an electrical bias, and excess carrier density was calculated using the following equation:

$$\Delta n = \frac{\left(-N_d + \sqrt{{N_d}^2 + 4({n_{i,eff}}^2 \exp\left(\frac{V}{k_b T}\right)} \right)}{2}, \tag{7}$$

where $n_{i,eff}$ is effective carrier density calculated using Schenk band gap narrowing and N_d is doping density in the bulk of the wafer.

Then, recombination rates can be written as follows:

$$U_{Auger} + U_{rad} = np(2.5\times10^{-31} g_{eeh} n_0 + 8.5\times10^{-32} g_{ehh} p_0 + 3\times10^{-29} \Delta n^{0.92} + B_{rad}) \tag{8}$$

$$U_{SRH} = \frac{np - {n_{i,eff}}^2}{\tau_p (n + n_t) + \tau_n (p + p_t)}, \tag{9}$$

with

$$n_t = n_{i,eff} \exp\left(\frac{E_t}{k_b T}\right) \quad and \quad p_t = n_{i,eff} \exp\left(\frac{-E_t}{k_b T}\right), \tag{10}$$

where a single trap state in the middle of the band gap was used giving $E_t = 0$;

$$U_{hi} = \frac{J_{0hi} \exp\left(\frac{qV}{n_{hi} k_b T}\right)}{qW} \quad and \quad U_{li} = \frac{J_{0li} \exp\left(\frac{qV}{n_{li} k_b T}\right)}{qW} \tag{11}$$

where U_{hi} and U_{li} are high injection and low injection surface recombination rates. Note that the introduced U_{hi} and U_{li} don't carry any physical meaning. The reason for using such notation is that the effective recombination close to V_{OC} injection can be directly measured and quantified in terms of J_{0hi} and n_{hi}. In its turn U_{li} was added in order to fit the measured effective lifetime curve, where J_{0li} and n_{li} were used as fitting parameters. Note also that the recent revision of Sinton tester spreadsheet using Richter parameterization and Schenk band gap narrowing was used in order to extract $J_{0,hi}$ from the measured effective lifetime curves[151].

Effective lifetime can then be written as

$$\tau_{eff} = \frac{\Delta n}{\left(U_{Auger} + U_{rad} + U_{SRH} + U_{li} + U_{hi}\right)} \tag{12}$$

The equation of the diode under light is written as

$$J = J_{gen} - J_{rec} \tag{13}$$

where J_{gen} is light generated current and J_{rec} is the voltage dependent recombination current.

According to the approach applied by Swanson[152] the recombination current can be broken down into its component parts:

$$J_{rec} = J_{Auger} + J_{Rad} + J_{SRH} + J_{surface,hi} + J_{surface,\mathrm{li}}, \tag{14}$$

where each part corresponds to a particular recombination mechanism. J_{Auger}, J_{rad}, J_{SRH} are due to the bulk Auger, radiative and Shockley-Read-Hall (SRH) recombination

respectively, $J_{surface,hi}$ is due to the recombination at the front and rear surfaces in high injection and $J_{surface,li}$ is due to the recombination at the surfaces in low injection.

Bulk recombination currents are given by:

$$J = qWU, \tag{15}$$

where q is electron charge, W is wafer thickness, U is a corresponding recombination rate.

Then, after introducing the fraction of the surface shaded by the front grid, the equation of the diode is

$$\begin{aligned} J = J_{gen}(1-shading) - qW(U_{Auger} + U_{rad}) - qWU_{SRH} - \\ - J_{0hi}\left(\exp\left(\frac{qV}{n_{hi}k_bT}\right)-1\right) - J_{0li}\left(\exp\left(\frac{qV}{n_{li}k_bT}\right)-1\right), \end{aligned} \tag{16}$$

where light generated current density is obtained using optical simulations and its direction was chosen to be positive.

V_{OC}, pFF and efficiency can be calculated from the IV curve, whereas effective lifetime can be plotted versus excess carrier density to give the idea about the data which would be measured on a considered solar cell by a Sinton tester. One challenge in simulating an SHJ solar cell using the measured effective lifetime data is a non-uniformity of passivation across the wafer. Fig.6-10 shows effective lifetime measured in 16 points across the wafers using a Sinton tester as compared to its calibrated band to band photoluminescence map. Effective lifetime curves usually have characteristic bell shapes peaking either around $2x10^{15}$ cm^{-3} or at $2\text{-}5x10^{15}$ cm^{-3}. The values of J_0 in their turn vary between 2 and 6 fA/cm^2 whereas effective lifetime close to maximum power operation point varies between 1.5 ms and 2.7 ms. Very precise estimation of V_{OC} and

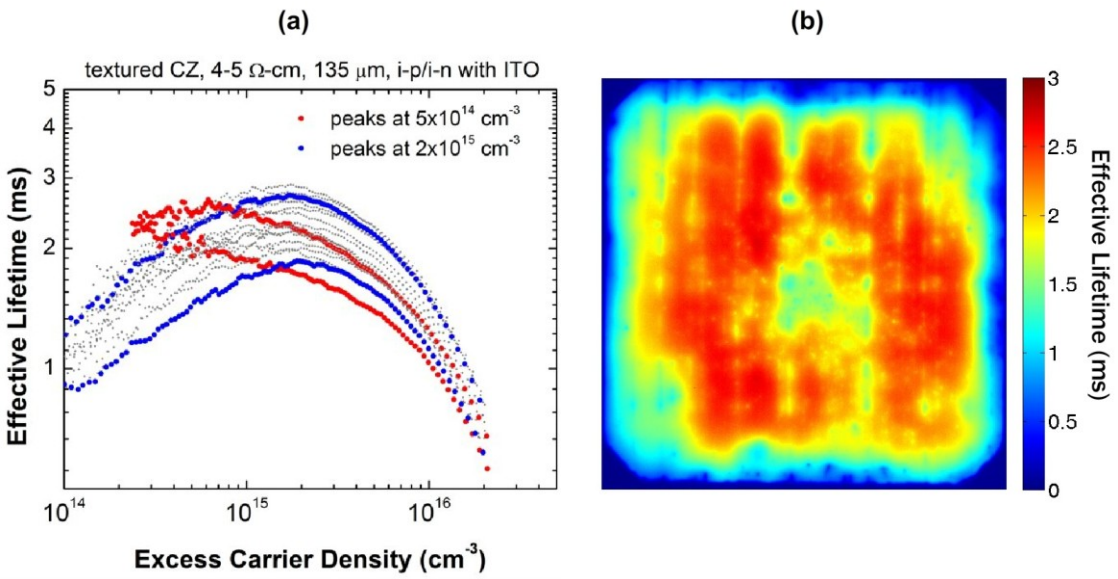


Fig.6-10. (a) Effective minority carrier lifetime measured by the Sinton tester in 16 points across the area of non-metalized SHJ solar cell. (b) a calibrated PL image of the same wafer. Nonuniformity of surface passivation typical for a-Si/c-Si systems makes it difficult to pick a model parameter which would represent the recombination in the complete solar cell.

pFF is possible if, for example, calibrated photoluminescence signal is averaged across the entire wafer. This method, however, will require advanced calibration of photoluminescence image since effective lifetime has a strong injection dependence.

This work used the values of effective lifetime measured in the middle of the wafer. Therefore, the results are representative of a solar cell, which would have a uniform passivation quality across the wafer. Note also that despite the mentioned uncertainty, the trends in the behavior of solar cell parameters are preserved therefore making the simulations instructive for the design of solar cells.

6.5.2 *Simulation of HI0068 Cells*

Fig.6-11 shows the simulated effective lifetime and the breakdown of recombination mechanisms in the cell HI0068-09 at V_{OC} and maximum power point. The Figure also shows injection levels corresponding to V_{OC} and MPP operation points on $\tau_{eff}(\Delta n)$ curve where recombination at MPP determines the pFF of the solar cells. Material parameters used in the model are listed in Table 6-1.

The model predicts 734 mV V_{OC} and 83.2% pFF compared to 730 mV and 82% measured on the actual cell. It also follows that in the considered cell Auger and radiative mechanisms are responsible for about 45% of recombination at V_{OC} with 43% contribution from surfaces, while the recombination at MPP is determined by the surfaces

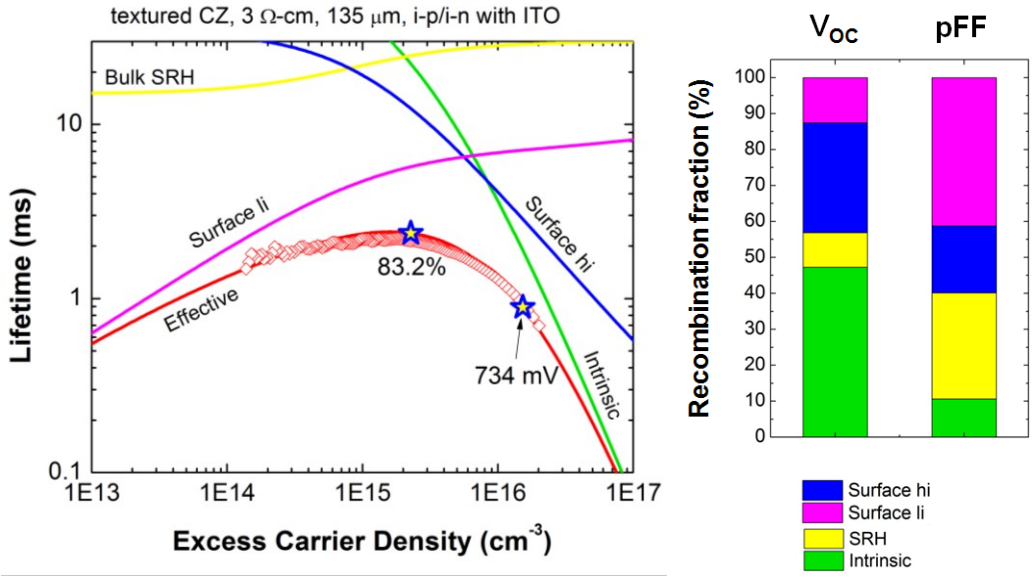


Fig.6-11. Left – the measured effective minority carrier lifetime and simulated lifetimes corresponding to a particular recombination mechanisms. Right – a breakdown of recombination mechanisms in the simulated solar cell at V_{OC} and MPP operation points.

Table 6-1. A list of parameters used in analytical recombination model to simulate the cell from the lot HI0068.

ID	ρ_{bulk} (Ω-cm)	τ_{SRH} (ms)	J_{0hi} (fA/cm^2)	n_{hi}	J_{0li} (nA/cm^2)	n_{li}	W μm	J_{gen} (mA/cm^2)	Shading (%)
HI0068	3	5	5	1	3	2	135	37.5	6

by 60% and 30% contributes bulk SRH recombination. Domination of recombination at maximum power by surfaces is limiting the pFF of a solar cell since surface recombination has high ideality factor (between 1 and 2).

Fig.6-12 (a) shows the implied IV curve of the solar cell obtained using recombination parameters of HI0068 (red line). It also shows the set of IV curves for the hypothetical solar cell where only selected recombination mechanisms are acting.

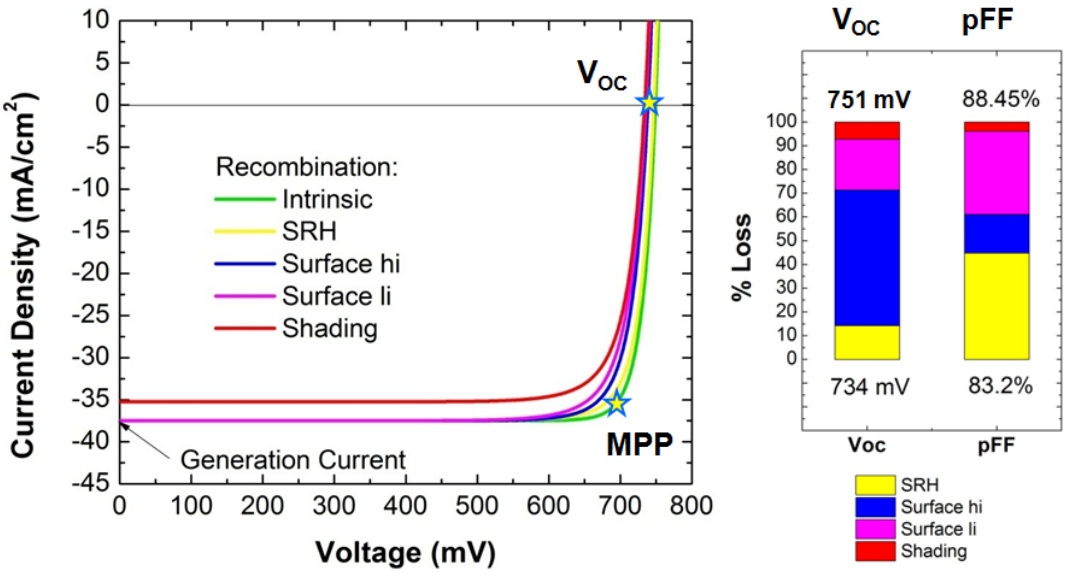


Fig.6-12. Left – simulated pseudo IV curves for a particular recombination mechanism for the solar cell from HI0068. The graph also shows the limiting V_{OC} and pFF for each added recombination mechanism. Right – a breakdown of non-intrinsic recombination losses at V_{OC} and MPP in the cell from HI0068.

Fig.6-12(b) shows the breakdown of extrinsic recombination losses which reduce V_{OC} and pFF compared to the intrinsic limit. It follows that in the considered solar cell surface recombination is responsible for 80% reduction of V_{OC} while at maximum power point both surfaces and SRH recombination equally contribute to the reduction of pFF.

6.5.3 Varying the Thickness of HI0068 Cells

The next study considered the performance of the solar cells processed on the wafers with different thickness using the flow similar to HI0068, i.e. recombination parameters from Table 6-1 were fixed, while the thickness of the wafer and generation current were varied. The used values of generation current are shown in Fig.6-13.

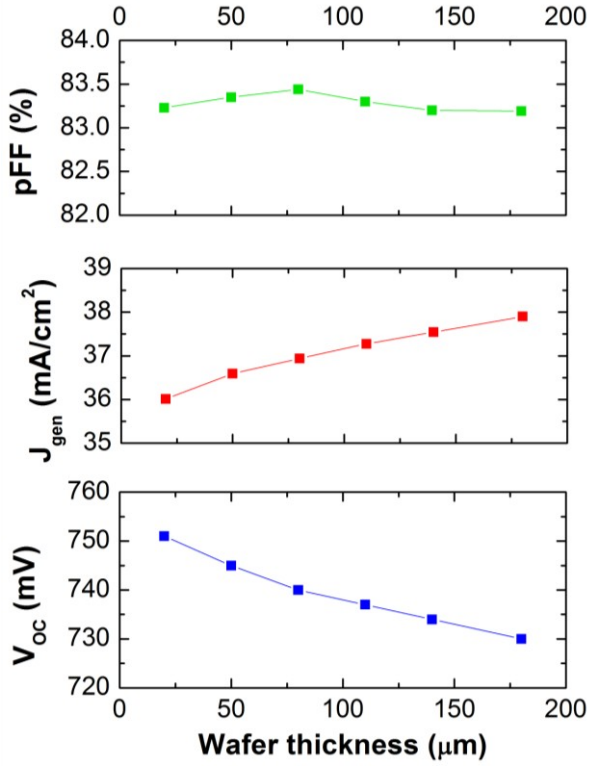


Fig.6-13. The simulated parameters of the cells in HI0068 versus wafer thickness. The passivation developed in this work allows the increase of V_{OC} with thinning the wafer.

They corresponded to the light trapping of the bifacial SHJ cell from HI0068. Fig.6-13 shows the increase of V_{OC} and reduction of J_{gen} with thinning the wafer. The pFF was almost independent on wafer thickness and remained at 83% level. V_{OC} increased from 730 mV for 180 μm thick wafer to 751 mV for 20 μm wafer, while the J_{gen} dropped from 37.9 mA/cm^2 to 36.01 mA/cm^2.

Fig.6-14 shows the simulated effective lifetime for different wafers thicknesses. It follows that on a 20 μm wafer with the passivation performance and light trapping equivalent to the cells from lot HI0068 maximum τ_{eff} is around 0.3 ms, however, the excess carrier density at open circuit operation increases leading to higher V_{OC}.

The contribution of different recombination mechanisms to overall recombination at V_{OC} and MPP versus wafer thickness is shown in Fig.6-15. The model shows that for the cells in HI0068, the role of surfaces would increase with thinning the wafer both at V_{OC} and MPP. Note that pFF remains at 83% level independent of wafer thickness since recombination is always dominated by low injection surface recombination term with ideality factor equal to 2. Higher pFF are possible in the devices limited by intrinsic recombination at maximum power point.

In summary, thinning the wafer may increase the average carrier density in the solar cell at open circuit, if surfaces have good enough passivation. This will increase the V_{OC}. Pseudo fill factor, however, will remain the same, since it is determined by the ideality factor of the dominant recombination mechanisms, which in most practical cases will be surface recombination at low injection with ideality factor higher than 1.

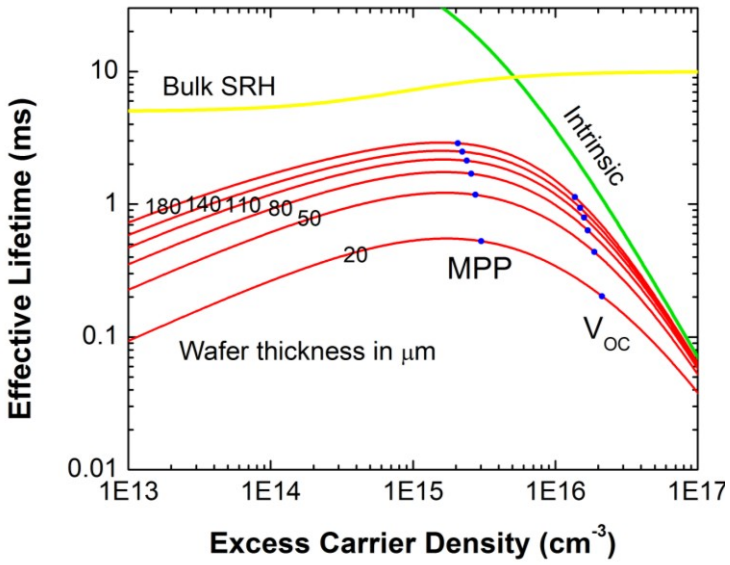


Fig.6-14. The simulated effective minority carrier lifetime curves for different wafer thicknesses. The plot also shows bulk SRH and intrinsic lifetime which are not dependent on substrate thickness. Note the shift of V_{OC} an MPP towards higher injection.

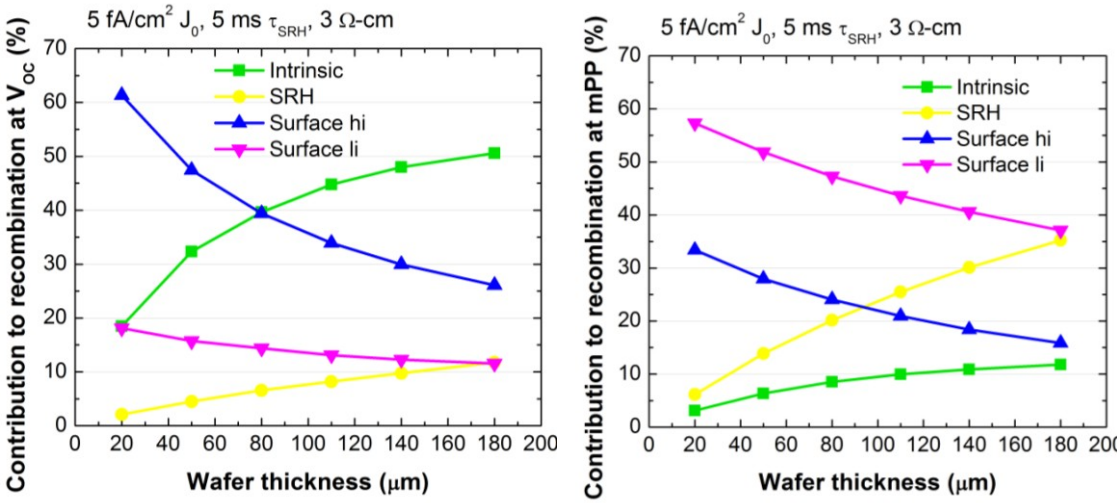


Fig.6-15. A breakdown of recombination mechanisms at V_{OC} (left) and MPP (right) versus wafer thickness in a simulated solar cell.

6.5.4 Reducing Recombination Losses in a SHJ Cell

Future heterojunction devices may realize more efficient minority carrier collectors and minority carrier mirrors either by further developing conventional passivation materials such as a-Si and SiO_2 or by using advanced heterojunction formed in III-V/Si material systems. For example, further improvements of plasma deposition and wafer cleaning processes may allow the reduction of interface states density while optimization of (i)a-Si:H and doped a-Si films may lead to the reduction of their band gap defects and, thus, less recombination. Fig.6-16 shows the hypothetical effective lifetime which would be measured on the device with 1 fA/cm^2 J_{0hi}, 15 ms bulk SRH lifetime and

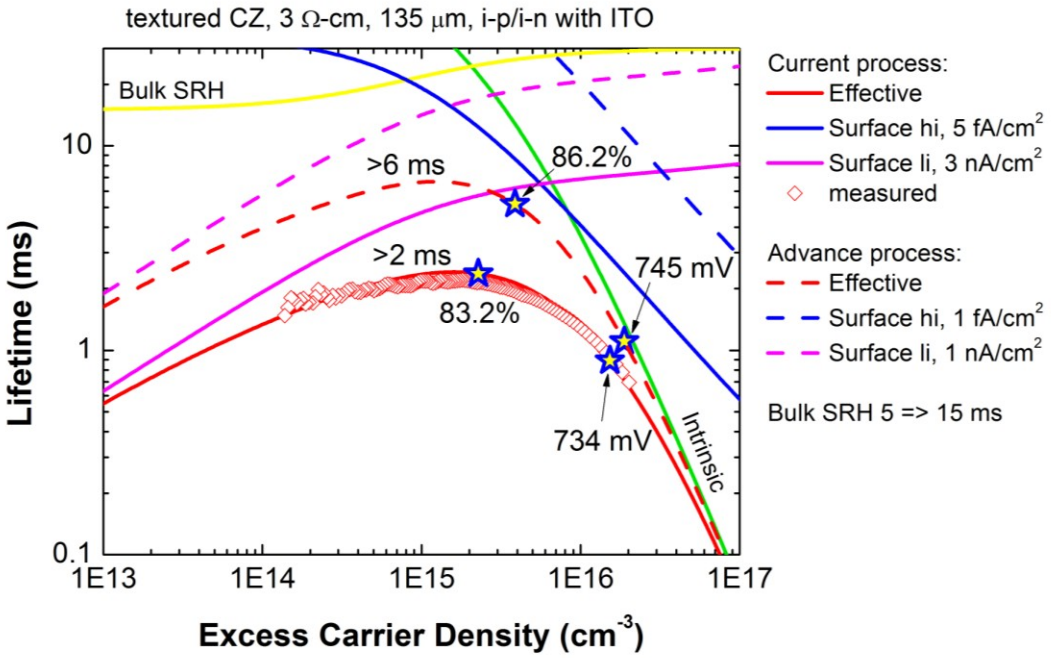


Fig.6-16. The dashed lines show simulated effective minority carrier lifetimes for a hypothetical SHJ solar cell with improved recombination properties. The model predicts that more than 6 ms lifetime can be measured on the current wafers providing surface passivation and bulk SRH lifetime are improved.

1 nA/cm^2 J_{0li}. Such devices will have more than 6 ms effective lifetime at 1x10^{15} cm^{-3}injection, while effective lifetime of the cells in HI0068 was only 1.5-2.5 ms. The model also predicts that 745 mV V_{OC} and 86% pFF are possible on high quality n-type CZ wafers with 135 μm thickness, if the surfaces are perfectly passivated.

One practical way to further improve passivation of c-Si by (i)a-Si:H is hydrogen plasma treatment which is in fact annealing in hydrogen atmosphere[117]. The temperature of the substrate during plasma treatment is usually higher than the deposition temperature and can be between 200 and 250 ^{o}C. At >200 ^{o}C hydrogen becomes mobile and can penetrate into (i)a-Si:H films passivating both bulk and interface defects. Another reported mechanism of plasma treatment can be the destruction of weak Si-H bonds introducing defect levels in the band gap.

Note that annealing temperature should not be raised above approximately 250 ^{o}C in order to prevent hydrogen effusion outside the films. The exact value of the critical temperature will depend on films capping (i)a-Si:H and on the properties of (i)a-Si:H itself. This work, for example, found that (i)a-Si:H layer deposited with relatively high H_2 dilution (400 sccm H_2 flow) did not degrade if annealed at 300 ^{o}C. The temperature limit also relaxed if (i)a-Si:H film was capped by a layer of SiN_x. Such structures could also be annealed at temperatures up to 300 ^{o}C without the degradation of passivation quality.

6.6 Series Resistance

A solar cell is a high current device which can generate 5-8 A current depending on the its area and light intensity. At the same time most solar cells use metal grids at the front surface to collect light generated carriers. The typical grid has H-pattern where two or three 1-2 mm wide vertical metal lines are usually used for soldering thick ribbons to interconnect the cells in a module and multiple 30-100 μm wide horizontal lines, also called the fingers, are used to extract the carriers from the minority carrier collector which usually covers the entire surface of the solar cell. The impact of series resistance on efficiency can be calculated by using an empirical relation for fill factor[167]:

$$FF_{R_S} = pFF(1-1.1r_S) + \frac{r_S^2}{5.4}, \tag{17}$$

where r_S is a normalized series resistance which is equal to $r_S = J_{SC}/V_{OC} \times R_S$.

Then the efficiency of the solar cell having series resistance is

$$\eta_{R_S} = J_{SC} \times V_{OC} \times FF_{R_S} \tag{18}$$

This work used an analytical lumped series resistance model to calculate series resistance losses. The components of the series resistance are shown on the schematic diagram in Fig.6-17. Series resistance models usually consider a unit symmetry cell (or sometimes several unit cells) and calculate area weighted series resistance components which can then be used to calculate power losses in the solar cell. For more details on calculation of series resistance, the reader is referred to the dissertation by Mette[168]. As was mentioned previously, this work neglected the contribution of the resistance which may occurred at the a-Si/c-Si/ITO heterojunction. Lateral resistance in the busbars was also neglected since all cells were measured using the probing bars with multiple current

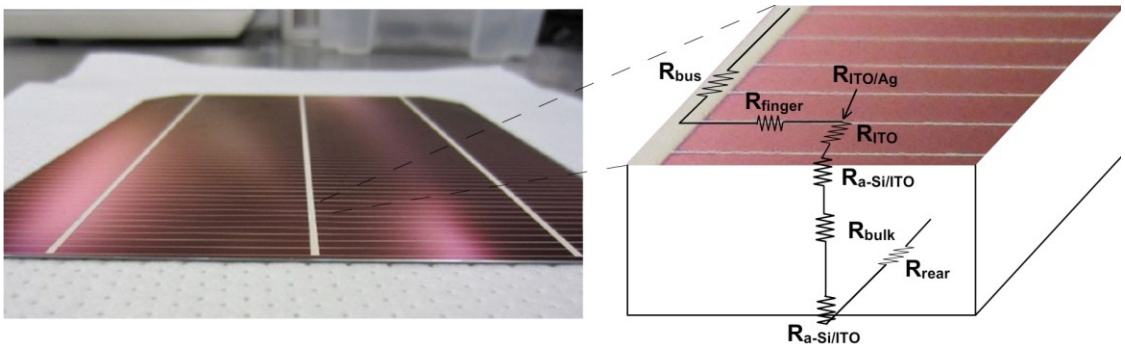


Fig.6-17. A photo of a solar cell from the lot HI0068 (left) and a schematic representation of the series resistance components in SHJ solar cell (right).

contacts spaced approximately 1 cm from each other. Specific contact resistivity of Ag/ITO contact was measured using a transfer length method. Bulk resistivity of the fingers was used as a fitting parameter to fit the measured values of series resistance since no special test structures to measured bulk resistivity were prepared in this work.

The major difficulty in evaluating series resistance losses of the cells in HI0068 (and other SHJ cells produced in Solar Power Lab so far) is poor printing quality which often resulted in broken fingers, irregular height and width of the fingers, and very strong non-uniformity of finger profiles across the area of the solar cells. Part of the reason for poor printing was the use of experimental pastes from different vendors which were found to have very different composition and physical properties. Also, due to the limited amount of the available paste printing, conditions were often optimized as long as the actual cells were processed. The three dimensional optical profiles measured on the cells from lots HI0068 and HI0042 demonstrating the deficiencies of the printing are shown in Fig.6-18.

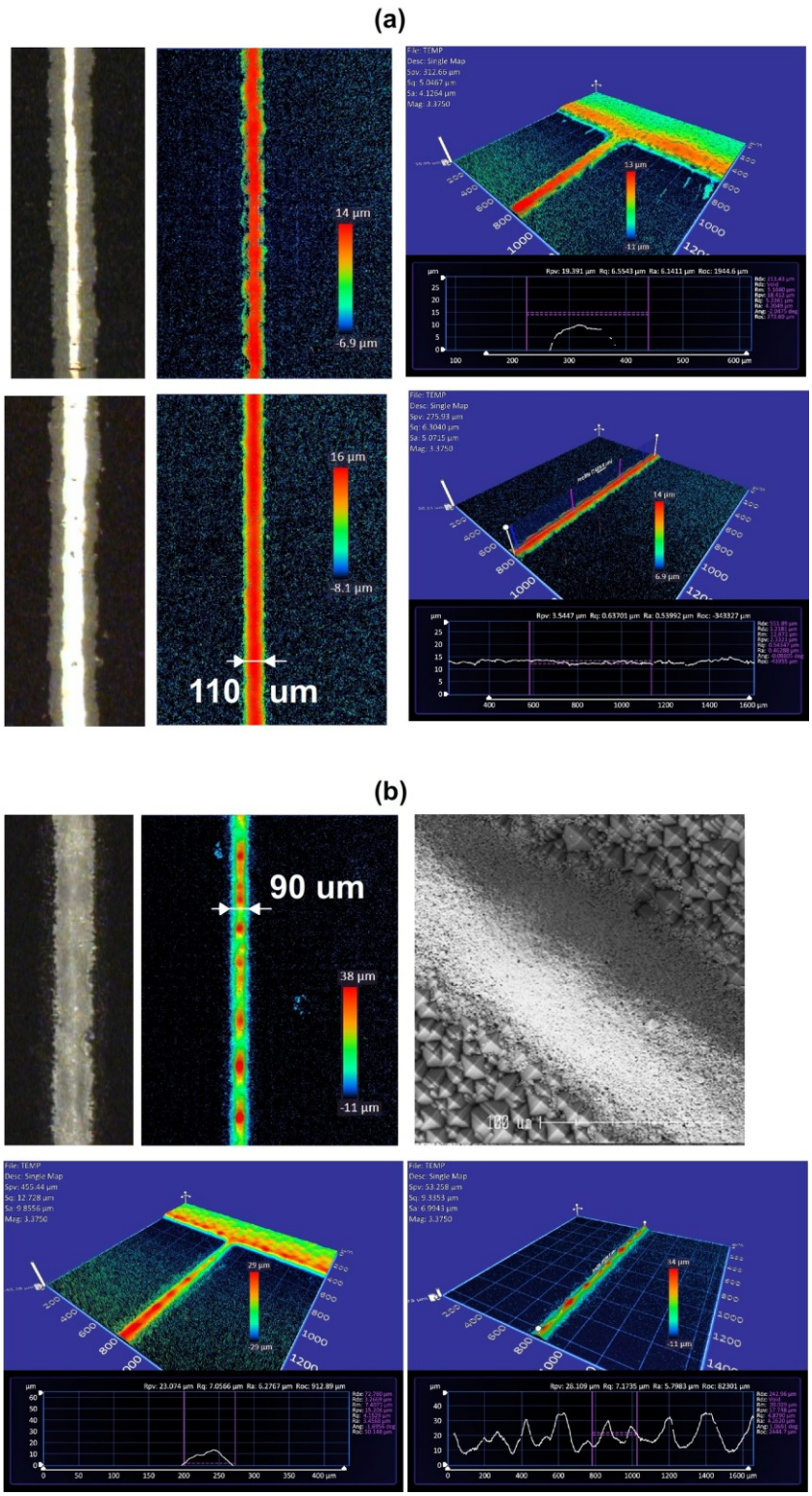


Fig.6-18. Optical microscope, 3D optical profiler and SEM images of the fingers printed on the cells from (a) HI0042 and (b) HI0068. Note that overall printing quality available in this work was bad which often resulted in irregular and very thin fingers.

One of the printing problems was the thinning of the fingers near the busbars where the current is maximum and therefore the voltage drop is high. This problem can be addressed by widening the openings in the screen where the fingers are connected to the busbar. Another problem was that several pastes used in this work produced the fingers with non-uniform height. This made it difficult to estimate the average cross section area of the finger which is required to calculate bulk resistivity by measuring the current voltage curve of the serpentine structure. Therefore, bulk resistivity was used as a fitting parameter. Another source of error was a varied edge resistance which was difficult to quantify (see the discussion in Section 5.3).

With the measured parameters, area weighted components of series resistance can be calculated according to the following equations:

$$R_{ITO} = \frac{1}{12} R_{\square ITO} \times s^2, \tag{19}$$

$$R_{finger} = \frac{1}{3} \rho_{Ag} \frac{s \times l}{h \times w}, \tag{20}$$

$$R_{c,Ag/ITO} = \frac{\rho_{c,Ag/ITO}}{4L_T}, \tag{21}$$

$$R_{wafer} = \rho_{wafer} W, \tag{22}$$

where s is finger spacing, l is finger length, h is finger height, w is finger width, $\rho_{c,Ag/ITO}$ is specific contact resistivity of Ag/ITO contact, $R_{\square,ITO}$ is sheet resistance of ITO, ρ_{Ag} is bulk resistivity of Ag paste, and W is wafer thickness.

The model neglected bulk resistance of the busbar, contact resistance between current probes and the busbar, and contact resistance between rear metallization and the

chuck. For bifacial cell lateral resistance of ITO and contact resistance of Ag/ITO contact were accounted twice.

The total series resistance is the sum of all components:

$$R_S = R_{bulk} + R_{ITO} + R_{contact} + R_{fingers} \tag{23}$$

Another factor associated with front grid design, which determines the efficiency of a solar cell, is the area shaded by the metal. For simplicity this work used the ratio of metal area to the area of the wafer as shading factor. In reality, some reflectance from the oblique surface of the fingers towards the wafer is possible. In addition, when encapsulated, the photons reflected from metal fingers may be reflected again from the glass and come back at a different angle to be absorbed by the solar cell. One additional loss component which was included in shading losses was the area around the perimeter of the wafer shaded during ITO deposition in order to prevent shorting between front and

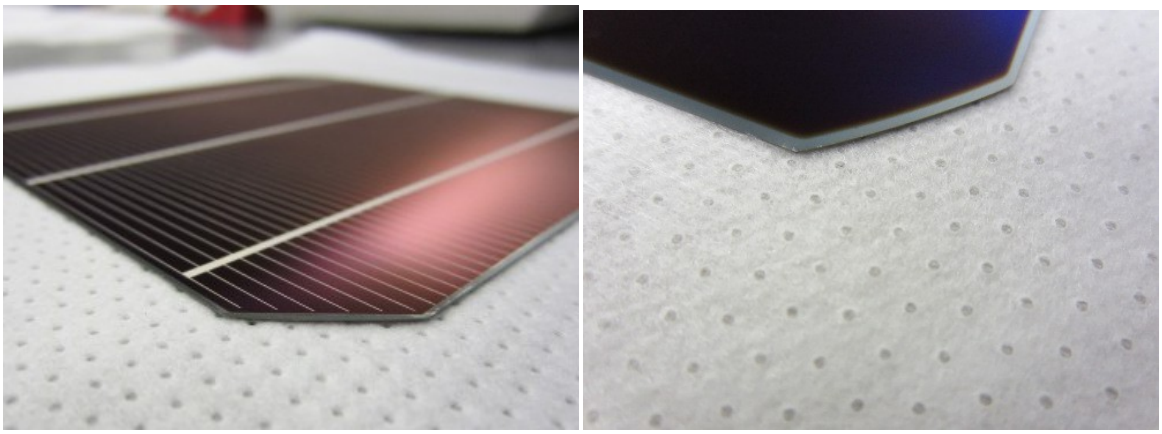


Fig.6-19. The photos showing the area around the perimeter of the wafer shadowed during ITO deposition using stainless steel shadow mask to prevent shunting between two sides of the cell. The shadowed area contribute optical losses, since a-Si has high resistance and the carriers separated near the edge will not be able to reach metal contacts. A better way to isolate the edges, either by plasma or wet treatment would be preferable.

rear ITO. This area was approximately 5 cm^2 in the cells from HI0068 (see Fig.6-19).

6.7 Waterfall Diagram

Finally, using the optical, recombination, and series resistance models described above, one can plot a waterfall diagram demonstrating the breakdown of power losses in a SHJ solar cell developed during this work. As before, the simulations used material and device parameters representative of the cells from lot HI0068. The cells in HI0068, for example, were made on 3 Ω-cm 135 μm thick wafers which determined upper efficiency limit. Later in this section, a possibility of achieving >25% efficiency based on realistic

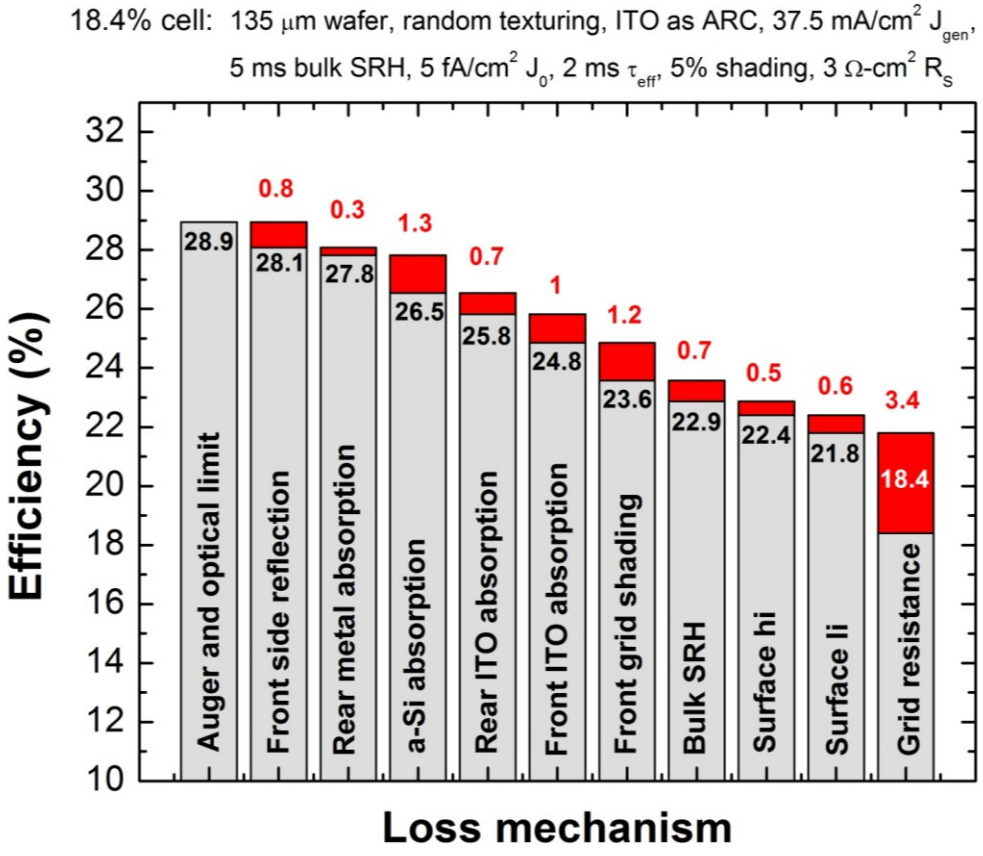


Fig.6-20. A waterfall diagram obtained from the built analytical model. The diagram reveals the components of power losses in HI0068 solar cell.

device parameters is analyzed.

Fig.6-20 shows a waterfall diagram representing the losses in HI0068 cells. The limiting light generated current was simulated in Sunrays assuming no reflectance from the front surface and a perfect lambertian reflector at the rear surface. Thus, the only loss mechanisms was the escape reflectance of IR light. The resulting generation current was equal to 43.5A/cm^2. A higher generation current would be possible in the devices having advance light trapping schemes. Such schemes, for example, could change the direction of IR photons and send them laterally along the wafer to increase the optical path length.

Table 6-2.The simulated losses in 18% cells from HI0068 in terms of V_{OC}, J_{SC}, pFF an efficiency.

Loss mechanism	Efficiency (%)	V_{OC} (V)	J_{SC} (mA/cm^2)	pFF
Auger and light trapping limit	28.94	0.751	43.5	0.885
Front reflectance	28.09	0.751	42.3	0.884
Rear metal absorption	27.81	0.751	41.90	0.884
a-Si absorption	26.53	0.750	40.02	0.884
Rear ITO absorption	25.82	0.749	38.98	0.885
Front ITO absorption	24.84	0.749	37.55	0.884
5% front grid shading	23.57	0.748	35.67	0.883
Bulk SRH	22.86	0.745	35.67	0.860
Surface hi	22.39	0.737	35.67	0.852
Surface li	21.80	0.734	35.67	0.833
Series resistance	18.42	0.734	35.67	FF: 0.703

Optical, recombination, and resistance losses and added sequentially estimate the contribution of a particular loss mechanism into an overall power loss.

Note also that the parameters of the actual solar cell are a function to spatial non-uniformity of recombination properties as was discussed earlier in this section. This fact is responsible for 4 mV and 1.3% absolute difference between the simulated and measured V_{OC} and pFF correspondingly. The simulated solar cell parameters for each particular loss mechanism are shown in Table 6-2.

It follows from the model that, in the considered cell, optical losses are the next important loss mechanism after the series resistance in the front grid. Total efficiency loss due to parasitic absorption in a-Si, ITO, rear metal, front grid shading, front side reflectance and escape reflectance reaches 5.37% absolute. In its turn, recombination loss is responsible only for 1.8% absolute reduction of efficiency.

6.8 22% SHJ Cell: Gaining from the Improved Cell Structure.

This section summarizes several straight forward SHJ cell design features to allow 2% absolute increase of efficiency. Increase of efficiency is primarily due to the increase of the generation current. Note that similar improvement can be achieved by other means. For example, using Cu metallization can increase both FF and J_{SC} due to thinner more conductive fingers. The proposed improvements are summarized in Fig.6-21.

As discussed in Section 6.4, a big fraction of optical losses in SHJ cell are due to parasitic absorption of visible light in the front a-Si and IR light in front and rear ITO. Usually, SHJ cells have p+ hole carrier collector at the front side. But thinning (p+)a-Si is

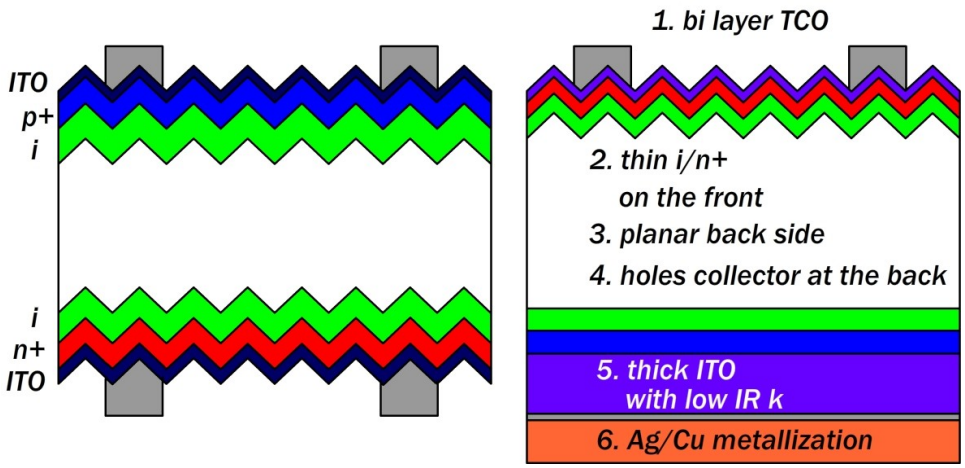


Fig.6-21.A summary of improvements leading to the reduction of optical losses and 2% absolute efficiency improvement.

limited by the influence of ITO work function, which can reduce the height of the potential barrier at the heterojunction, and, thus, reduce V_{OC} and pFF. Thinning (n+)a-Si on the other side, is not involved in such tradeoff. It is therefore beneficial to put n+ electron collector on the front side and move p+ hole collector to the rear. Since the diffusion length in the used n-type CZ material is very high, such castling won't affect the performance of the cells. Then (i)a-Si and (p+)a-Si at the rear can have the thickness only limited by a series resistance and passivation quality.

ITO at the rear side can be replaced with a TCO having negligible parasitic IR absorption and low index of refraction. The thickness of rear TCO should be picked in order to shield IR light from reaching metal and not to cause additional series resistance. In case of contact resistance problems, bi layer TCO can be used. In bi layer TCO the first thin layer serves as an electrical contact, while the second thick layer carries optical functionality. For example, high/low carrier density ITO or ITO/IZO bi layers can be used.

Another design feature can be a planar rear surface. Although some classical simulation studies suggest that both sides textured wafers are better for trapping of IR light[153], the cells with planar rear side can be attempted. Keeping the rear side planar is also beneficial for surface passivation as discussed in Section 4.2.

6.9 25% SHJ Cell

25% is efficiency record for single junction c-Si solar cells measured at 1 Sun light intensity. The record device reported by UNSW group was based on PERL technology. The cell was made on 400 um thick FZ wafer, had inverted pyramids, photolightographically defined three layer metallization and double layer antireflection coating. On the other side, SHJ cells have already reached 24% efficiency presumably using conventional random texturization, single layer ITO as antireflection coating and non-photolithographic metallization. It is quite possible that in 1-2 years, a new record silicon solar cell based on SHJ technology will be reported.

The goal of achieving 25% from the current process may be separated into 3 tasks. First, a baseline cell with reasonable series resistance should be produced. This should include using proper shadow masks for edge isolation, introduction of the sputtered back surface Ag reflector and achieving high quality printing with at least 1 Ohm-cm^2 series resistance. Improving series resistance will allow 20-21% SHJ cells. The recent results obtained using stainless steel shadow masks and the screens with 290 mesh are presented in Section 5.4. < 1 Ohm-cm^2 resistance was demonstrated on large area cell measured using 10x10 cm^2 aperture. However, high edge resistance still has to be addressed in order to achieve low resistance of full wafer cells.

Second, a better passivation by (i)a-Si:H/doped a-Si should be achieved to produce >6 ms effective lifetime on 3 Ohm-cm 130 um wafers. In addition, alternative metallization schemes such as Cu plating should be introduced to provide both lower resistance and front grid shading. Cu plated cell with 30 um fingers can achieve 3% shading and 0.5 Ohm-cm^2 series resistance which together with improved passivation (1 fA/cm^2 J_{0hi} and 1 nA/cm^2 J_{0li}) and better bulk material (15 ms VS 5 ms bulk SRH) will achieve 23.44% efficiency. Note that all optimizations listed in step 2 have already been demonstrated and, therefore, achieving 23% efficiency for different research groups seems highly possible.

Further efficiency improvements will require reduction of optical losses, which will probably require using the materials alternative to a-Si and ITO and possible

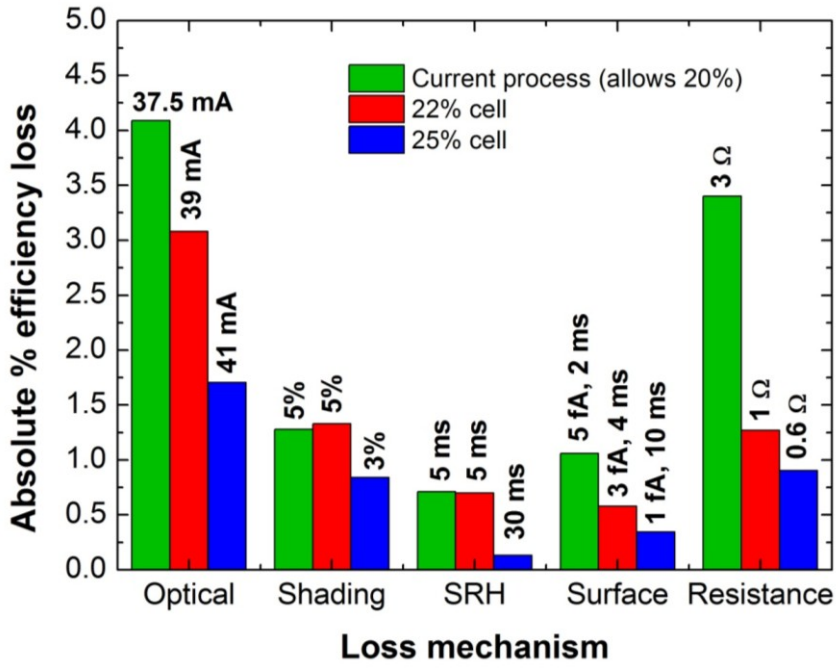


Fig.6-22. Losses of 25% cell compared to 21%

alternative light trapping schemes. 25.11% efficiency will be possible if generation current is increased to 41 mA/cm^2. The improvements necessary to achieve 25% c-Si solar cell are summarized on the diagram in Fig.6-22.

Chapter 7
SHJ CELLS ON 50 UM WAFERS

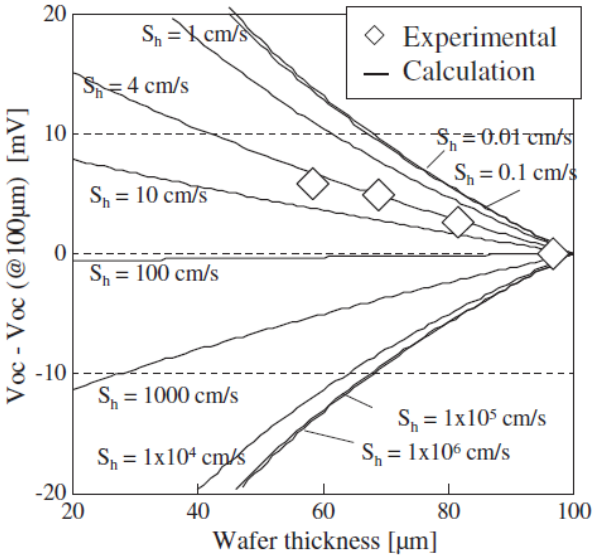
Chapter 7 presents the performance of non-metallized SHJ cells processed on 140-50 μm thick wafers. Thin wafers were obtained by wet chemical etching of c-Si. After thinning, the wafers were put through the baseline SHJ fabrication flow. The thickness was limited to 50 μm because thinner wafers broke during spin rinse drying and static driers were not available in this work. One of the goals of this study was to achieve the highest possible local $V_{OC.}$ Local V_{OC} was measured by Suns-V_{OC} without forming a front metal contact. Non textured wafers with relatively thick a-Si layers were used. This allowed to demonstrate >750 mV local V_{OC}.

7.1 Why Thin Wafers?

It was recognized early in the 1980'sthat the ultimate crystalline silicon solar cell would be relatively thin with the optimum being between 10 and 100 μm depending on the light trapping and intrinsic recombination parameters used in the simulation[169][171]. The key requirement leading to high efficiency on thin wafers is low recombination at the surfaces (where the solar cell usually has emitter and metal contacts). Swanson applied a very practical approach to calculate the limiting efficiency of a wafer silicon solar cell and included non-intrinsic loss mechanisms, where he also pointed out the need for the emitter and metal contacts with less than a 2 fA/cm^2 saturation current density (J_0)[154]. Such a low J_0 is possible in SHJ solar cells. The main advantage of SHJ technology is that the entire surface is passivated with intrinsic a-Si,

while metal contacts are shielded from the wafer surface by the stack of a-Si films and TCO layer.

Fig.7-1 compares the performance of ultra-thin SHJ cells reported by Tohoda et al. from Sanyo in 2012[155], with the performance of PERL cells which was published by Wang et al. in 1996[156]. Due to perfect passivation quality, the V_{OC} of SHJ cells increased on thinner wafer, while the V_{OC} of the PERL cell remained approximately the same. According to the model used by Tohoda et al., the effective area weighted surface recombination velocity allowing the increase of V_{OC} should be at least less than 100



Cell	Structure	Thickness (μm)	V_{oc} (mV)
WZnf3-3-e	n^+pp^+	44	643.4
WZth3-1-e	Figure 1	47[a]	698.5[a]
W4-6-2G	Figure 1	400	702[a]

Fig.7-1. A literature data showing the performance of SHJ cells [155] (upper graph) versus PERL cell [156] (the chart) made on thin wafer. The data suggests that unlike in SHJ cells surface passivation in PERL cells was not enough to achieve higher V_{OC} on thin wafer.

cm/s. In PERL cells surface recombination was at the level which does not allow higher V_{OC} on thinner wafers (100 cm/s in Tohoda's terms).Experimental data presented by the Sanyo group suggested that their HIT cell have achieved4 cm/s effective surface recombination velocity.

7.2 Demonstration of >750 mV V_{OC} on thin SHJ cell

The goals of this study were to demonstrate the level of surface passivation which would lead to the increase of V_{OC} on a thin wafer and to achieve >750 mV V_{OC} on a SHJ solar cell structure. Additional losses associated with parasitic absorption, transmission and series resistance were not considered, although the actual solar cell would have to be optimized in order to minimize short circuit current and fill factor losses. The main experimental results including the effective lifetime versus wafer thickness and V_{OC} of a 50-μm-thick SHJ solar cell are presented in Section 7.5. Section 7.4 introduces recombination model, which was used to calculate the implied V_{OC} based on the measured τ_{eff} and to analyze the contribution of different loss mechanisms at open circuit. A built recombination model is further used in Section 7.7 to propose practical ways to achieve >760 mV V_{OC}.

7.3 Experimental Details

SHJ solar cells were made on high lifetime n-type CZ wafers with 3-4 Ω-cm resistivity and initial thickness equal to 160-170 μm. The wafers were chemically thinned down to 146, 129, 100, 81, 50 and 44 μm. Thinning was followed by wet chemical cleaning and conditioning of the surface and plasma enhanced chemical vapor deposition of 10-15 nm intrinsic a-Si and 10-15 nm doped a-Si from both sides of c-Si wafer (i.e., i-

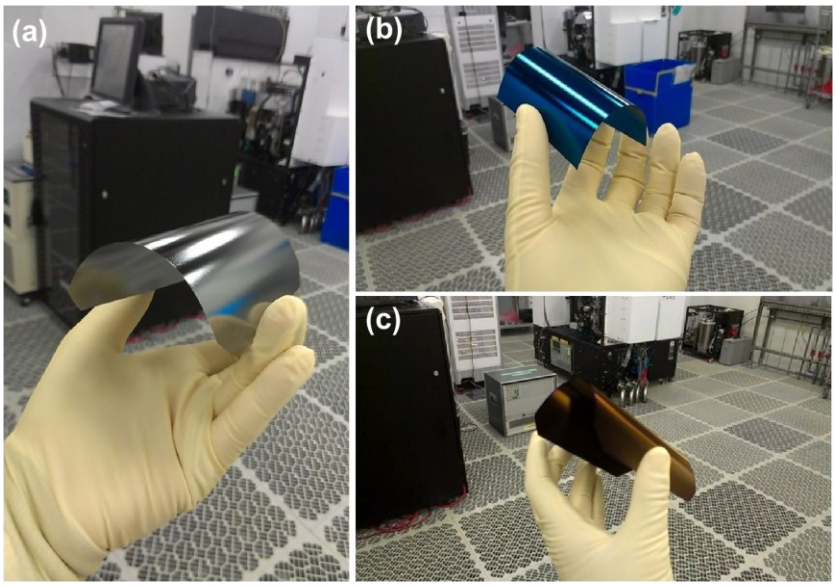


Fig.7-2.Photos of 50 μm thick c-Si wafers obtained by wet chemical thinning in concentrated KOH solution. (a) planar wafer, (b) non metalized 8x8 cm^2 SHJ solar cell on planar c-Si wafer, (c) non metalized SHJ cell on 125 mm wide textured CZ wafer.

p/i-n stack). Baseline a-Si films and Clean 2 were used in this study. The samples were completed by sputtering 90 nm of indium tin oxide on both sides of the wafer and annealing for 30 min at 200^{o}C in an air ambient to cure the damage produced by ITO sputtering. The photos of thin c-Si wafers are shown in Fig.7-2.

Effective lifetime was measured after a-Si and ITO deposition using a Sinton lifetime tester. V_{OC} was measured on a Sinton flash solar cell tester in Suns-V_{OC} mode and cross-checked using Oriel steady-state simulator. All effective lifetime and V_{OC} data was measured in the clean room environment with the temperature of the samples maintained at 25 ^{0}C by the resistive heaters built into the testers which correspond to the standard testing conditions. Photoluminescence (PL) images were captured by an in-house system using low pressure sodium bulbs for excitation and a silicon CCD camera (see Section 2.1.5 for details).

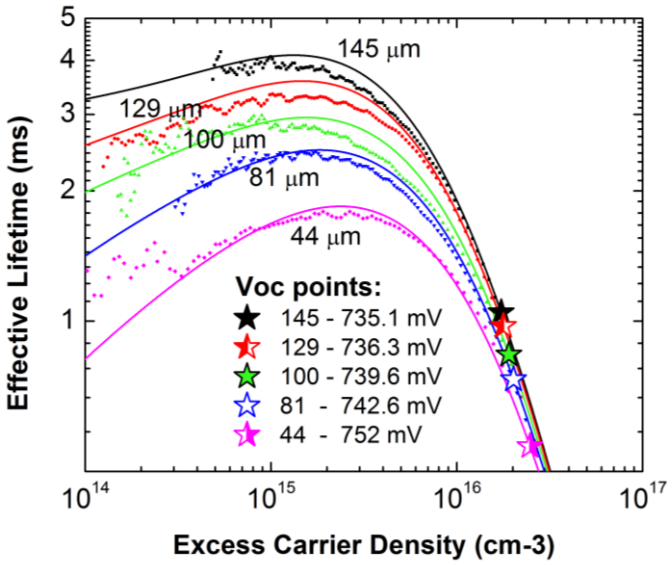


Fig.7-3. Effective minority carrier lifetime measured on i-p/i-n passivated planar CZ wafer with varying thickness. The graph also shows simulated effective lifetime curves, the injection level at implied V_{OC} and the values of implied V_{OC}.

7.4 Analytical model of SHJ solar cell

To calculate the implied $V_{OC,}$ this study used analytical recombination model introduced in Section 6.5. J_{gen} for thin SHJ cells with planar surface and for standard SHJ cells was simulated using a ray tracing program Sunrays. The optical constants of a-Si and ITO films measured by the spectroscopic ellipsometry as discussed in Section 6.4. Three light trapping cases were considered. J_{gen} was simulated as a function of wafer thickness for each case. The three cases labeled LT1, LT2 and LT3 are summarized in Table 7-1.

7.5 Experimental Results

Fig.7-3 shows the dependence of τ_{eff} on wafer thickness for i-p/i-n passivated non-textured wafers with 10-nm-thick a-Si layers. The J_{0hi} for the considered wafers was

Table 7-1.Three light trapping cases considered to study the increase of V_{OC} with thinning the wafer.

ID	J_{SC} (mA/cm2)	Comment
LT1	30.4	Non-textured, 15-nm-thick a-Si, non-metalized.
LT2	35.5	Textured, <10 nm a-Si, includes 6% shading.
LT3	39.5	Highest published on SHS.

1.7±0.3 fA/cm^2. To calculate iV_{OC} 4 ms bulk SRH recombination lifetime (which we usually measure at 1e-15 cm^{-3} injection for thick, well-passivated wafers from this vendor) and the LT2 light trapping option were used. Thus, the iV_{OC} shown in Fig.7-3 is representative of the V_{OC} which would be measured on a solar cells having 1.7 fA/cm^2 J_{0hi} and LT2 light trapping.

The measured thickness dependence of iV_{OC} is in agreement with experimental

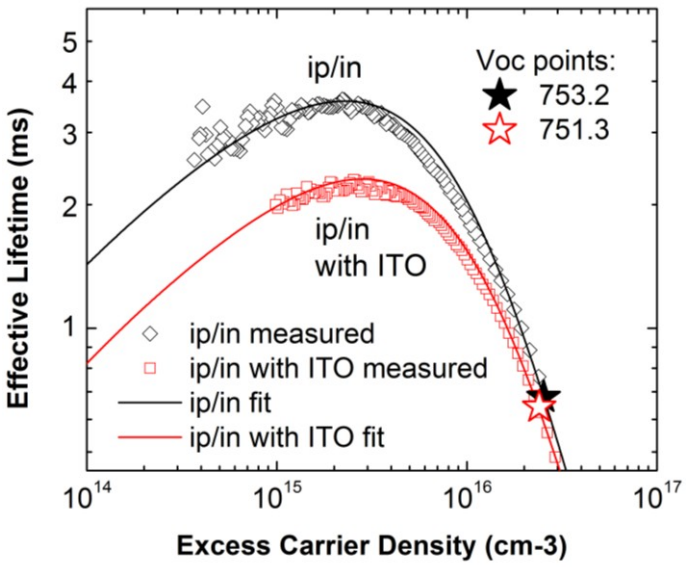


Fig.7-4. Effective lifetime measured after i-p/i-n deposition and after ITO deposition (followed by annealing at 200 ^{o}C for 30 min) on the high V_{OC} sample prepared using thicker (i)a-Si:H layers.

results by Tohoda et al., where the increase in the V_{OC} of SHJ solar cells with thinning the wafer was also observed. Thus, in thin solar cells with <2 fA/cm^2 J_{0hi}excess carriers will have lower lifetime but their concentration at open circuit will be higher, thereby increasing the V_{OC}.

In order to measure the actual voltage and achieve >750mV V_{OC} a non-textured 50-µm-thick i-p/i-n passivated wafer with 15-nm-thick a-Si layers was prepared. ITO was deposited on both sides of the wafer. The effective lifetime measured on a representative wafer before and after ITO deposition is shown in Fig.7-4. After i-p/i-n deposition the J_{0hi} was equal to 0.4±0.2 fA/cm^2. After ITO deposition and annealing the J_{0hi}increased to 0.7±0.2 fA/cm^2. As previously discussed in Section 3.6 this degradation of lifetime can be due to the party reversible damage to the interface passivation or to the bulk intrinsic a-Si by UV light and/or high energetic particles, e.g., Ar ions, accompanying ITO

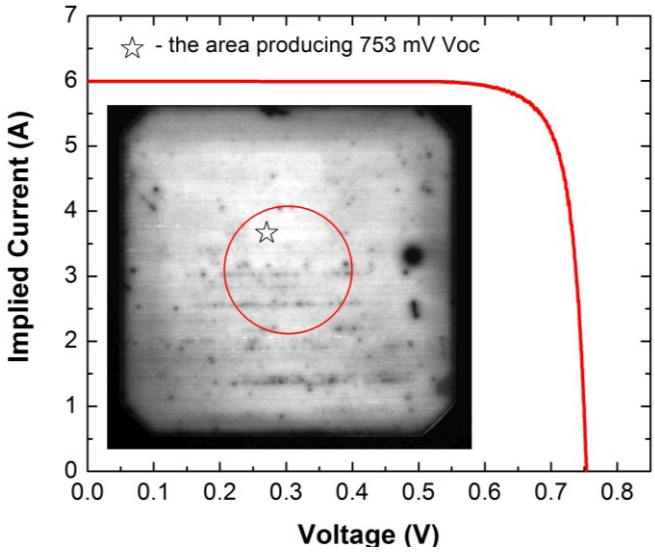


Fig.7-5. Implied IV curves obtained from the Suns-V_{OC} and PL map of the high voltage sample. The circle indicates the area sensed by the RF coil of the Sinton tester.

sputtering or by other mechanisms.

According to the built recombination model,0.7 fA/cm^2 J_{0hi}implies 751 mV V_{OC}, where LT1 trapping option and a 3 ms SRH bulk lifetime were used.

The device indeed produced 751±2 mV V_{OC} when measured in the area around the center of the wafer with the highest measured value being 753.4 mV. The area that produced 753.4 mV V_{OC} is marked by the star on the PL image shown in Fig.7-5 together with the implied IV curve measured by the Sinton flash solar cell tester. Note that 6A I_{SC} was used as an implied current. Fig.7-5 also shows the area corresponding to the detector (red circle) used in the Sinton lifetime tester meaning that the measured effective lifetime and J_{0hi} were averaged over this area. The PL image clearly indicates the areas of lower carrier density especially around the edges of the wafer. This implies that the V_{OC} of a complete solar cell after metallization would likely drop by several mV. Lower

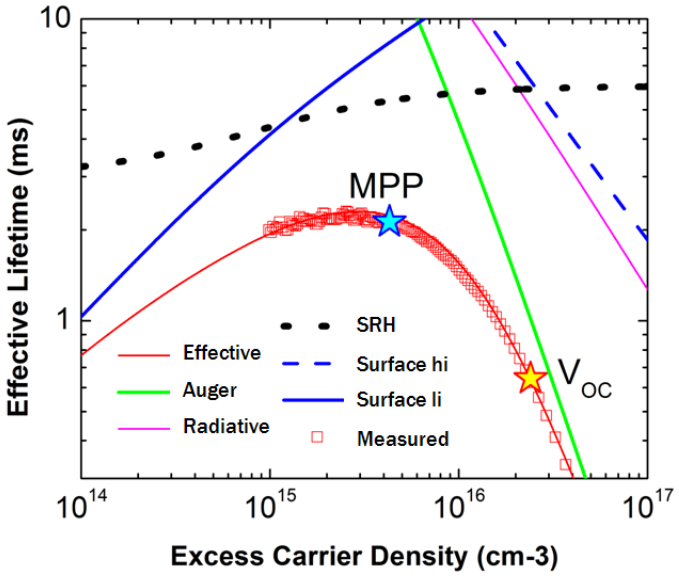


Fig.7-6. The breakdown of lifetimes in a high V_{OC} SHJ solar cell made on 50 micron thick CZ wafer .

performance around the edges is due to the non-uniformity of the wet etch process, the edge recombination, and the particles adhered to the surface prior to a-Si deposition.

Fig.7-6 shows the components of simulated τ_{eff} with the injection levels at V_{OC} and maximum power point (MPP). In accordance with the built model in solar cells with J_{0hi} equal to 0.7 fA/cm^2, Auger recombination is responsible for 70% recombination at V_{OC}, while the contribution of bulk SRH, bulk radiative and surfaces comprise the remaining 30% in approximately equal shares. The model also shows that for the solar cells with <2 fA/cm^2 J_{0hi} Auger recombination stays the dominant recombination mechanism at V_{OC} for any practical wafer thicknesses.

7.6 Errors in Measuring <2 fA/cm^2 J_0 by Photoconductance Decay

The method to measure saturation current density by Kane and Swanson implemented in a Sinton lifetime tester is presently ubiquitously used and has in fact become a standard way to characterize potential barriers in silicon solar cells. However, an accurate measurement of < 2fA/cm^2 saturation current represented a significant challenge since the value of the measured J_0 becomes comparable with the measurement error. For example, the reported thickness of the wafers was calculated from the measured mass and implies uniform thickness across the wafer. However, the thickness for a 50-μm-thick wafer measured by a micrometer revealed 4% thickness non-uniformity across the wafer; while changing the thickness parameter by 1 μm changes the calculated J_0 by 0.4 fA/cm^2. The measured V_{OC} also contained an error due to the spectral mismatch between the reference calibrated cell and SHJ cells[157].

Table 7-2.The parameters used to simulate the thickness dependence of V_{OC} of SHJ solar cells with various light trapping and recombination properties.

Case	Light Trapping	$J_{0front+rear}$ (fA/cm^2)	SRH τ_n, τ_p (ms)
1	LT1	0.7	3
2	LT3	0.7	3
3	LT3	0.1	10

Finally, the wafers used in this study have experienced 10% τ_{eff} non-uniformity across the wafer and about 5% non-uniformity across equally processed wafers due to the variability introduced by wet chemical processing. All τ_{eff} data was measured in the center of the wafers, which didn't always correspond to the best passivated area. The values of J_0 were calculated at 1.5e16 cm^{-3} injection.

7.7 Achieving >760 mV V_{OC}

One interesting application of the built recombination model is to look at the potential practical ways to achieve even higher V_{OC}. Three cases with the parameters listed in Table 7-2 were considered. Case 1 implies the same processing sequence as was used in this study. Case 2 considers the hypothetical SHJ cell which can achieve LT3 light trapping and at the same time preserve 0.7 fA/cm^2 J_{0hi}. Case 3 considers an SHJ cell made on FZ material with 10 ms bulk SRH lifetime, 0.1 fA/cm^2 J_{0hi}, and LT3 trapping, which would be representative of the ultimate SHJ solar cell.

The simulated V_{OC} versus wafer thickness for the considered cases is shown in Fig.7-7. Two stars label the V_{OC} of the best SHJ cell as well as 753 mV local V_{OC} achieved in this work.

Fig.7-7 demonstrates three main results: 1) assuming J_{0hi} stays at 0.7 fA/cm^2 level, 760 mV can be demonstrated using the current fabrication flow, if a SHJ solar cell is made on a 30-µm-thick substrate; 2) 760 mV is possible on a 40-µm-thick wafer, but the cell will have to achieve light trapping similar to the best SHJ cell (LT3) and keep J_{0hi}equal to 0.7 fA/cm^2; 3) finally, an SHJ cell can have 760 mV on a 50-µm-thick wafer if FZ material is used, and 0.1 fA/cm^{2}dark surface saturation current in combination with LT3 trapping is achieved.

In summary, in this study non-metallized SHJ solar cells on thin wafers were

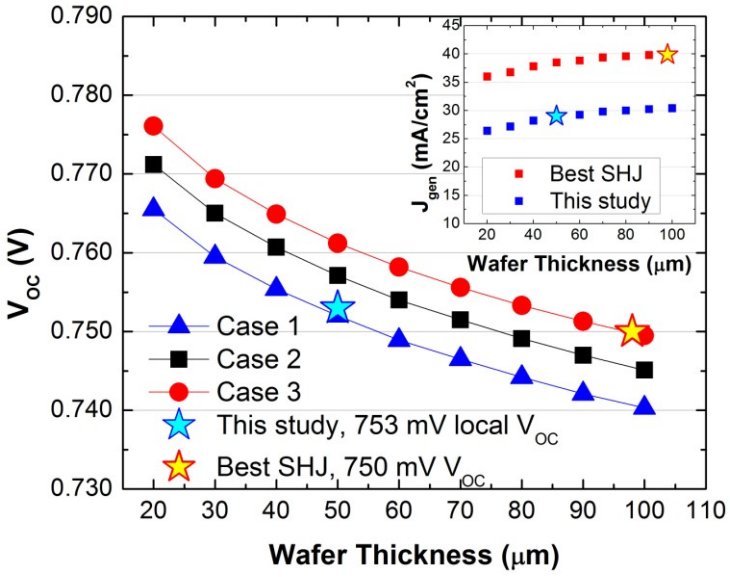


Fig.7-7.Calculated V_{OC} versus wafer thickness for different current-recombination assumptions. The inset shows generation current vs. wafer thickness calculated for LT1 and LT3 light trapping cases.

processed and>750 mV local V_{OC} on a 50-μm-thick wafer was measured. This result presented experimental evidence that thin wafers can achieve very high voltages, if the surfaces are nicely passivated and produce < 2fA/cm^2 cumulative front and rear surface saturation current at the V_{OC} operating point. Further, the challenge of measuring <2 fA/cm^2 saturation current was discussed. The recombination model built on the basis of Richter parametrization and measured J_{0hi} showed that up to 760 mV voltages are practically possible if either the wafer is further thinned down to 30 μm, or the light trapping similar to the record SHJ cell is achieved, or J_{0hi} is as low as ~0.1 fA/cm^2.

Chapter 8
SURFACE PASSIVATION BY A-SI/SIO2/SINX STACK

One application of the developed (i)a-Si:H passivation process is to use it to passivate n-type wafers. For example, it can be used at the front surface of interdigitated back contact solar cells stacked under a layer of SiN_x which will serve as an antireflection coating. Chapter 8 presents passivation performance of (i)a-Si/SiO_2/SiN_x (aSON) stack where SiN_x was additionally charged by corona tool. This stack was designed to achieve the ultimate passivation of n-type material by combining chemical and field effect passivation. The chapter also discusses optical properties and thermal stability of the aSON stack.

8.1 Surface Passivation of n-Type Material

High-quality high-throughout surface passivation of n-type crystalline silicon wafers with 1-5 Ω-cm resistivity is critical for mass production of thin high efficiency silicon solar cells. The main technological application of such passivation is the front surface of IBC solar cells with either diffused or heterojunction carrier collectors[158][60]. The main technologies currently used to passivate n-type wafers as well as their passivation performance are listed in Table 8-1. The table also lists the performance of passivated surfaces with phosphorus diffusion. The best reported passivation quality of n-type material was obtained by either using thermally grown SiO_2 in combination with the 'alneal' treatment[159] or Al_2O_3 formed by atomic layer

Table 8-1. Review of passivation technologies with passivation performance which can be found in the literature. Note that the presented results in most cases are achieved using R&D tools and processes. The passivation produced by mass production tools can be worse.

Technology	min S_{eff}	Deposition Technique	Reference
Mirror polished n-type wafer, 1-5 Ohm-cm			
Al_2O_3	1.3	PA-ALD	Richter [146]
Al_2O_3	1.2	PA-ALD	Veith [170]
SiO_2	2.4	Thermal Oxidation	Kerr [159]
SiN_x	1.6	PECVD	Wan [166]
a-Si	1	PECVD	Schüttauf [162]
a-Si	1.5	PECVD	Strahm [161]
organic	7*	Wet treatment	Chhabra [163]
aSi/SiN_x	1.3	PECVD	Koyama [176]
SiO_2/SiN_x	2.4	Thermal/PECVD	Larionova [174]
Al_2O_3/SiN_x		PA-ALD/PECVD	Bock [177]
80/200 Ohm n+ diffusion, planar wafer			
Al_2O_3	100/60	PA-ALD	Hoex [164]
SiO_2/SiN_x	--/10	Thermal/PECVD	Reichel [187]
SiN_x	45/30	PECVD	Kerr [188]

* effective lifetime measured while the substrate in the solution

deposition (ALD)[160]. Very good results were also achieved by hydrogenated a-Si[162] and SiN_x[166] films formed by plasma enhanced chemical vapor deposition (PECVD).

Dangling bonds at the surface of crystalline material create a quasi-continuous distribution of energy states in the band gap, thus, serving as Shockley Read Hall (SRH) states promoting recombination of minority carriers. With improved quality and/or reduced thickness of the bulk material, recombination at the surfaces becomes a dominant

recombination mechanism and therefore requires an advanced treatment. Recombination at the passivated surface is suppressed either by reducing the concentration of electronically active surface states or by reducing the concentration of minority carriers in the vicinity of the surface by the field effect[172]. Field effect passivation can be due to the charges present in the passivating films (SiN_x, Al_2O_3), or due to the band bending induced by the band alignment at the heterointerface (a-Si), or due to the low/high doping which can be created by diffusion, ion implantation or alloying of dopant atoms.

The surfaces of the solar cell also usually include areas that are highly doped and have metal contact, which represent an additional challenge for passivation. Recombination at the diffused surface will be directly proportional to the surface density of dopant atoms since they create additional lattice defects serving as recombination centers. In addition, the volume of the wafer with the diffused dopants (usually 0.5-5 μm deep into the wafer) will be a source of high Auger and SRH recombination. The metal/semiconductor interface will be a source of very high surface recombination, if not passivated, for example, by a tunnel oxide[173]. As a result, the overall recombination in a solar cell will be determined by the geometry of the device which will determine area weighted contribution of metal contacts, diffusions and bare passivated surfaces.

In addition to providing electronic passivation, if applied at the front surface of the solar cell, the film should also serve as an antireflection coating and have low parasitic absorption. Finally, passivation technology should ensure high throughput and reliability in order to be used in a production environment.

Presently, no single film can meet all three design and technological requirements. In order to resolve the tradeoff among passivation quality, optical losses

and scalability, various stacked structures were designated and tested for solar cells. The bottom film in the stack is intended to provide good chemical passivation, but is often limited either by parasitic absorption or slow deposition rate. The remaining upper films are responsible for antireflection properties, can provide hydrogen for additional passivation of surface states, fixed charges for field effect passivation, and serve as protective capping layers. Examples of such stacked structures include thermal-SiO_2 / PECVD-SiN_x[174] silicon-rich-SiN_x / nitrogen-rich-SiN_x[175], aSi/SiN_x[176], and Al_2O_3/SiN_x[177]. The passivation performance of selected stacks is also presented in Table 8-1. The main motivation of this study was to achieve the passivation quality previously only allowed by ALD Al_2O_3 and 'alnealed' thermal SiO_2 using a highly transparent stack deposited by a conventional PECVD at low temperature (< 250 ^oC). This was achieved by using an a-Si/SiO_2/SiN_x stack, where the thin a-Si film provides chemical passivation, SiN_x serves as an antireflection coating, the source of hydrogen, the repository of fixed charges and the capping layer, and the 10-nm-thick SiO_2 prevents the charges in nitride from leaking to the silicon, if nitride is additionally charged. The schematic diagram of the aSON stack is shown in Fig.8-1.

aSON stack allows < 1 cm/s effective surface recombination velocity (S_{eff}) on <100> polished FZ material as well as on standard industrial CZ wafers, both textured and planar. It is also demonstrated that an a-Si layer < 5 nm in thickness is sufficient to ensure very good passivation quality making the stack applicable to the front surface of IBC cells.

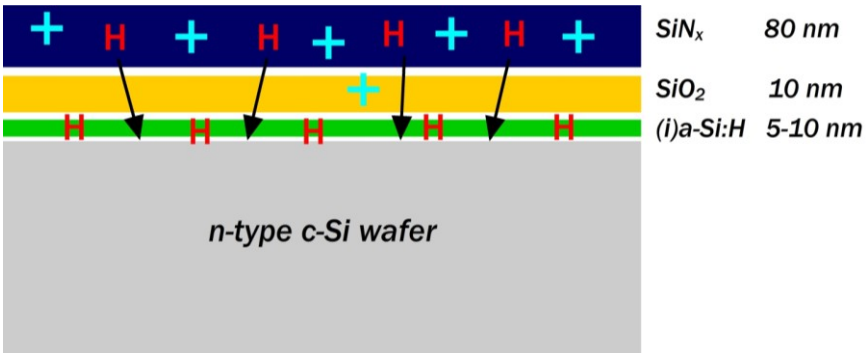


Fig.8-1.Schematic diagram of aSON stack. It is assumed that hydrogen from hydrogen rich SiN_x layer can diffuse towards a-Si and a-Si/c-Si interface at 250 ^{o}Cin order to improve the passivation quality. Additional charges in the bulk of SiN_x film can be permanently created by a corona discharge. The combination of both mechanisms allowed very good surface passivation

8.2 Experimental Details

Experimental details of this study are described in the following paragraph. Wafers W1, W3, and W4 were used. The FZ wafers were cleaned using Clean 1 with the last oxide strip immediately before a-Si deposition. The thicknesses of planar and textured CZ wafers after etching were 145 and 125 μm respectively. Alkaline etching was followed by a Clean 3 cycle with the final oxide strip right before transferring the wafers to the deposition chamber. 10 nm (i)a-Si, 10 nm SiO_2 and 80 nm SiN_x as measured by spectroscopic ellipsometry on polished wafers were used. A SiN_x film with a refractive index equal to 2 at 633 nm and atomic hydrogen content equal to 25%, as previously measured by ellipsometry and RBS respectively[178], was picked in order to provide low parasitic absorption and a sufficient amount of hydrogen to improve passivation during post deposition annealing. In order to obtain the films with the desired thicknesses on textured wafer, the deposition times were increased by a factor of 1.7 (note that a factor 1.5 was introduced after this experiment was complete, see Section 3.6). After deposition,

all wafers with the aSON stack were annealed for 30 min in air at 250 ^{o}C to cure the plasma damage caused by the SiO_2 and SiN_x depositions and to improve chemical passivation by redistributing hydrogen atoms in the stack. The wafers without a-Si were instead annealed for 30 min in forming gas (FGA) at 450 ^{o}C to improve the c-Si/SiO_2 interface. τ_{eff} and S_{eff} at 1x10^{15} cm^{-3} injection and J_0 at 1x10^{16} cm^{-3} injection (further τ_{eff-15}, S_{eff-15} and J_0) were also reported. S_{eff} was calculated assuming infinite bulk lifetime by

$$S_{eff} = W / (2 \times \tau_{eff}), \tag{24}$$

where W is wafer thickness.

J_0 was extracted from the measured τ_{eff} using the Sinton tester software. In the following discussion the values of J_0 were used to compare recombination properties at the injection level close to V_{OC} and τ_{eff-15} – at the injection closer to maximum power point of the solar cell.

In this study the density of positive charges in SiN_x was also increased by corona charging from the as deposited 1-2x10^{12} cm^{-2} to 8-9x10^{12} cm^{-2} where charge density was measured by CV analysis[179]. The data for the charged stacks is further designated by a plus sign (e.g. aSON+). Additional charging was possible due to the presence of amphoteric defects in the bulk of SiN_x (K centers). K centers are known to provide sites for permanent storage of charge. Our group previously showed that the charge of the K centers can be manipulated by a corona field providing nitride is separated from the silicon substrate by a relatively thick oxide which prevents the tunneling of charges from silicon into nitride or the nitride-oxide interface[179]. Note also, that although the charge is distributed through the volume of the nitride film, for convenience we report charge levels as effective interface areal densities.

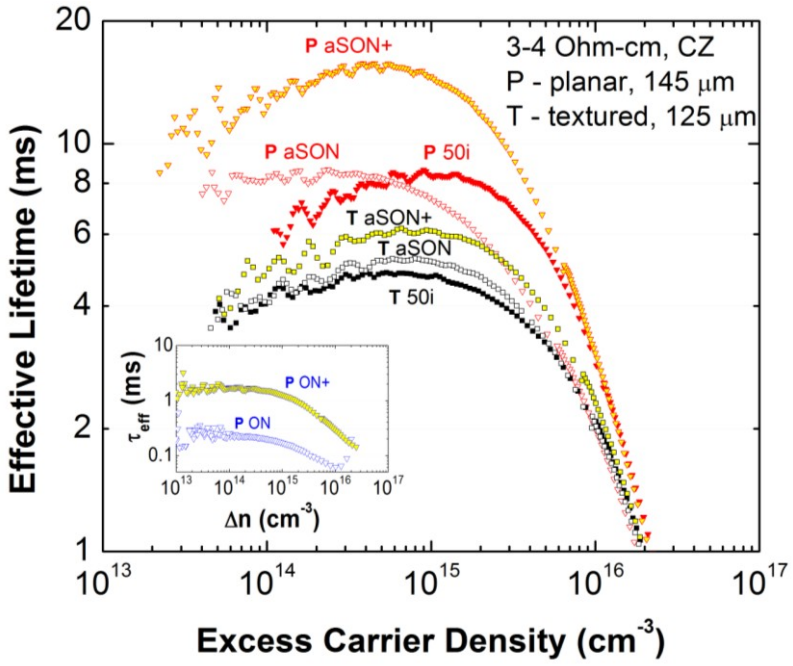


Fig.8-2.τ_{eff} measured on CZ wafers passivated with aSON stack compared to the passivation by 50 nm (i)a-Si:H and PECVD SiO_2/SiN_x stack (in the inset).

8.3 Performance of aSON passivation

Fig.8-2 shows τ_{eff} measured on CZ wafers passivated with the aSON stack before and after charging compared to the passivation by 50 nm (i)a-Si and by the stack of SiO_2 and SiN_x without (i)a-Si (ON stack). Fig.8-3 shows selected recombination parameters obtained from the measured τ_{eff} curves: $\tau_{eff\text{-}15}$, $S_{eff\text{-}15}$ and surface J_0. This work achieved >15 ms $\tau_{eff\text{-}15}$ on planar CZ wafers passivated with the aSON+ stack which implies >15 ms bulk SRH lifetime and demonstrates the quality of the contemporary CZ material. $\tau_{eff\text{-}15}$of the aSON stack before charging was very close to the τ_{eff} observed for the 50 nm (i)a-Si passivation; however, the performance at higher injection degraded which resulted in 2.4±0.36 fA/cm^2 J_0 as compared to 0.6±0.18 fA/cm^2 measured on the wafer with 50 nm (i)a-Si. After charging, J_0 reduced to 1±0.25 fA/cm^2.

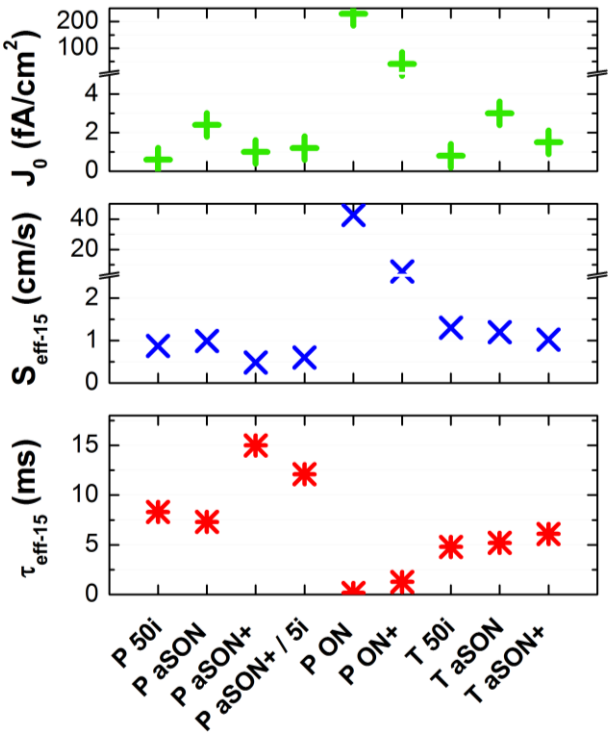


Fig.8-3.Selected recombination parameters extracted from the measured τ_{eff} curves for the considered passivating films. P—on planar CZ wafers, T—on textured CZ wafers. Plus denotes the wafers with the charged nitride.

All three cases represent nearly perfect passivation quality and would have a small contribution to the overall recombination of IBC solar cells which usually have diffused p+ and n+ carrier collectors at the back with overall J_0 of the rear surface > 50 fA/cm^2[158].

For comparison, state of the art IBC cells from SunPower were reported to achieve 8 fA/cm^2 J_0 at the front surface[22]. Note also that industrial IBC cells have high sheet resistance phosphorus diffusion at the front surface, also called a front surface field (FSF), which is formed in order to reduce lateral series resistance and stabilize thermal oxide, and which will increase overall J_0 of the surface. Therefore J_0 of the aSON stack measured in this work cannot be directly compared to the J_0 of SunPower cells since it

has FSF which carries additional functionality. The wafers without (i)a-Si:H layer demonstrated overall insufficient passivation quality with notably low performance at $>1x10^{15}$ cm^{-3} injection. J_0 of the ON+ stack was only 41 fA/cm^2.

The lower J_0 of the aSON stack as compared to J_0 of the 50 nm (i)a-Si can be attributed to flattening the bands at the surface and enhanced surface recombination, with 10 nm (i)a-Si:H providing slightly worse chemical passivation than 50 nm (i)a-Si:H. The process can be enhanced by the amphoteric nature of the interface defects which can trap negative charges with raising the Fermi level and compensate positive charges in the bulk of SiN_x. A similar effect may take place in the case of ON+ passivation, where the interface between PECVD SiO_2 and crystalline silicon is known to have a large density of amphoteric defects[180]. A precise measurement of the defect distribution at the surface and evaluation of their nature is necessary in order to build a recombination model and understand the increase in recombination of aSON and ON stacks at higher injection.

8.4 Optical Performance of aSON Stack.

a-Si at the front surface of the solar cell can impart a significant contribution to optical losses[124] (see also Section 6.4.2 for discussion). It is therefore desirable either to reduce the thickness of the a-Si film or to use the films with wider band gaps. Fig.8-3 shows recombination parameters of the wafer passivated with an aSON+ stack having 4.5±0.5 nm thick a-Si layer ("P aSON+ / 5i") which achieved 12 ms $\tau_{eff\text{-}15}$ and 1.6±0.4 fA/cm^2 J_0 on planar CZ wafer. Further reduction of film thickness in this work was limited by the relatively high deposition rate (1.5 nm/second) for a-Si deposition recipe. Less than 3 seconds deposition would be required to get thinner films, where very short

depositions are usually accompanied by non-uniform surface coverage due island growth which occurs during the first 1-2 seconds of deposition[181].Thinner films can be achieved by using recipes with lower deposition rates which can be obtained by, for example, reducing SiH_4 flow or plasma power. The overall optical losses of the aSON stack in this study were calculated using Opal 2 optical simulator[182]. It was found that 5 nm of (i)a-Si will be responsible for additional 1 mA/cm^2 loss of the short circuit current (J_{SC}) while the reflectance of the aSON stack will be equivalent to the reflectance of a conventional SiO_2/SiN_x stack to give another 0.8 mA/cm^2 loss of J_{SC}.

8.5 Passivation of Mirror Polished FZ Material

Aiming to achieve the intrinsic recombination limit (cumulative Auger and radiative recombination), the aSON stack was also applied to passivate mirror polished FZ wafers. Fig.8-4 shows τ_{eff} measured on FZ material before and after charging as well as the intrinsic lifetime limit calculated according to the parametrization by Richter et al.[146] τ_{eff} on 1.7 Ω-cm wafers matches Richter's limit in the $5x10^{14}$-$2x10^{16}$ cm^{-3} injection range (if, for example, 100 ms bulk SRH lifetime is added to the intrinsic lifetime) which implies that, for the wafer considered, the surfaces become electrically active only at injection levels below $5x10^{14}$ cm^{-3}.

τ_{eff} measured on 5000 Ω-cm wafers after charging produced a characteristic hump which is a known calibration issue of the older revisions of Sinton testers when measuring high resistivity material at low injection. The classic example of this feature is the data obtained by Kerr[159]and Olibet[183]. We therefore estimated the maximum τ_{eff} to be around 60 ms which is the highest reported in literature τ_{eff} measured by the

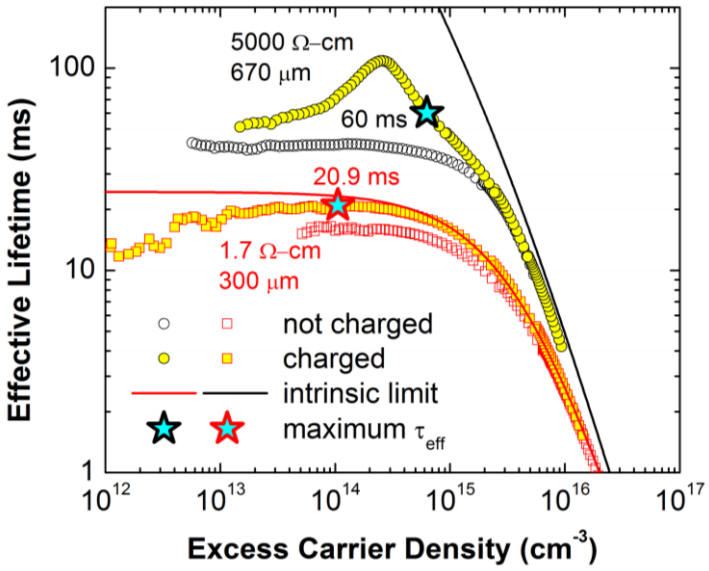


Fig.8-4.τ_{eff} measured on mirror polished FZ material passivated with the aSON stack. Solid lines show intrinsic limits calculated using Richter's parametrization. The hump in the measured τ_{eff} on 5000 Ω-cm wafer is due to a known calibration issue of the lifetime tester used in our lab. The maximum τ_{eff} was estimated to be around 60 ms.

photoconductance decay technique on silicon material. For example, > 100 ms τ_{eff} was measured by Trupke et al.[184] who, however, used quasi steady state photoluminescence.

8.6 Stability of aSON Passivation

a-Si passivation is known to degrade at temperatures above 300 ^{o}C[185] presumably due to hydrogen effusion outside a-Si film and a-Si/c-Si interface[186]. It would, therefore, be necessary to deposit aSON stack at the front surface of IBC solar cell after all high temperature steps, such as dopants diffusion, thermal oxidation, and metal contacts sintering are complete. The aSON stack can also be used for silicon heterojunction IBC cells, where heterojunction carrier collectors are formed at the rear surface first and, therefore, low temperature front surface passivation is needed.

Practical implementation of the aSON stack would require ensuring high reliability and low performance degradation in the natural environment. There are several known issues associated with using a-Si and charged nitrides on the front side of the solar cell. For example, UV radiation is known to degrade a-Si/SiNx passivation quality[187]. High energy UV light may also cause the charges to escape their potential wells in SiN_x film, thus reducing overall charge density[179]. Other possible fault modes include the interaction between the charged SiN_x and EVA (leakage of charges), the impact of atmospheric moisture, and potential induced degradation. A comprehensive reliability study is necessary to ensure the applicability of the aSON stack to mass production solar cells. Our group previously obtained initial passivation stability data for the charged ON samples stored in a clean room environment[179]. No significant degradation of passivation was observed after 6 months storage. Note also that for all practical solar cell applications additional corona charging would not be necessary in order to achieve passivation quality of the front surface which would not limit the performance of the device.

In summary, the passivation quality of a-Si/SiO_2/SiN_x stack deposited by conventional parallel plate PECVD at < 250 ^oC with and without additionally corona charged SiN_x was investigated. It was shown that the aSON stack can achieve the passivation quality previously only allowed by the 'alnealed' thermal SiO_2 and ALD Al_2O_3 on both planar and textured n-type CZ substrates. It was found that the wafers passivated with the aSON stack result in very low surface recombination at low and intermediate injection (up to $1x10^{15}$ cm^{-3}) while their performance yields the passivation produced by a 50 nm (i)a-Si at higher injections. The observed difference is, however,

insignificant compared to the conventional recombination associated with the diffused p+ and n+ carrier collectors making the aSON stack a good choice to passivate the front surface of IBC cells. τ_{eff} can be additionally improved by charging the SiN_x film using a corona discharge or other analogous techniques. The reliability of the passivation by the films with extra charging, however, may be an issue and will require an in depth study. Finally, a comprehensive recombination model with interface defect distribution, wafer doping, and density of fixed charges as input parameters would be necessary to understand relatively low performance of aSON stacks at higher injections.

Chapter 9
CONCLUSION

The main goals of this work were to develop a SHJ solar cell fabrication flow using industry compatible tools and process in a pilot production environment, study the interaction between the used fabrication steps, identify the minimum set of optimization parameters and characterization techniques needed to achieve 20% baseline efficiency, and analyze the losses of power in fabrication SHJ cells by numerical and analytical modeling.

SHJ solar cell are among the highest efficiency commercial solar cells. However, despite these high efficiencies, the adoption of the SHJ approach by industry has been hampered by the apparent difficulty in achieving consistent, high efficiency results using commercial processes. This is demonstrated by the long time lag between the initial good efficiencies from Sanyo and the development of similar results from other groups and by the difference between single solar cell results and module efficiencies.

The main conclusion of this thesis is that a high voltage large area SHJ solar cell can be developed using a small number of optimization parameters and commercial equipment.

The main contributions of this work are:

1. The demonstration that a process flow for large area 20% bifacial SHJ cell can be developed using a small number of optimization steps. Only 5 optimization parameters were used to give high voltage SHJ solar cells: (i)a-Si:H passivation quality of mirror polished wafers, (i)a-Si:H passivation quality of textured wafers,

bulk conductivity of doped a-Si, transmittance and conductivity of ITO, thicknesses of all films. The critical characterization techniques were also identified and used during this work.

2. The development and, for the first time, presentation of a cleaning sequence leading to a uniform and repeatable passivation of post alkaline etch wafers by (i)a-Si:H producing large area solar cells with 730 mV V_{OC} and 82% pFF. The clean is based on sequential nitric-acetic, Piranha and RCA-b oxidations and doesn't require layered a-Si structures, plasma treatments and post deposition annealing.
3. A detailed analytical analysis of power losses based on the measured optical, recombination and resistance parameters. The limitations of analytical approach were discussed. A roadmap to 22% large area industrial SHJ cell based on the built model was proposed. The model also predicted the material and device parameters requried to achieve >25% efficiency.
4. A demonstration of > 750 mV local V_{OC} on 50 microns thick SHJ cells.
5. Surface passivation based on a-Si/SiO_2/SiN_x stack which produced the lowest reported surface recombination velocity on both planar and textured wafers, which can be used on solar cell structures that do not require front contacts (e.g. interdigitated back contact solar cells).

The author hopes that the knowledge generated during this dissertation will help R&D labs to establish a baseline SHJ cells fabrication flow to achieve 20% efficiency. This is also hoped to allow more rapid development of SHJ technology to introduce innovative materials and processing techniques which will further increase the efficiency

of SHJ cells and will reduce manufacturing cost. The methods of silver-free metallization, high quality in-line plasma deposition of a-Si, low cost cleaning and automatic handling of thin wafers are of immediate importance .

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