Effect of Grain Orientation on Electromigration in Sn-0.7Cu Solder Joints

by

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ABSTRACT

Microelectronic industry is continuously moving in a trend requiring smaller and smaller devices and reduced form factors with time, resulting in new challenges. Reduction in device and interconnect solder bump sizes has led to increased current density in these small solders. Higher level of electromigration occurring due to increased current density is of great concern affecting the reliability of the entire microelectronics systems. This paper reviews electromigration in Pb- free solders, focusing specifically on Sn0.7wt.% Cu solder joints. Effect of texture, grain orientation, and grain-boundary misorientation angle on electromigration and intermetallic compound (IMC) formation is studied through EBSD analysis performed on actual C4 bumps.

DEDICATION

I would like to dedicate this effort to my beloved family, especially my parents for all their support throughout this journey. Thank you for always believing in me!

!LOS AMO!

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1. INTRODUCTION

In the past, the conventional solder material used for most electronic devices was lead. Pb-solders, offers many advantages such as a lower melting point, relative low cost of raw material, and a good electrical conductivity. However, the lead solder has been proven to have a negative influence on environment and human health. Lead is a heavy metal element and is a poisonous substance which can cause damage to human nervous system and even brain disorders. Due to the toxicity of lead, a campaign was initiated to restrict the use of lead. On July 1, 2006 the European Union Waste Electrical and Electronic Equipment Directive (WEEE) and Restriction of Hazardous Substances Directive (RoHS) banned the intentional addition of lead in most electronic device products in Europe. American manufacturing corporations were incentivized by special tax benefits if they reduce or remove the lead solder in the microelectronic devices. In addition, the RoHS Directive limited the use of lead to 0.1 wt% (1,000 ppm) in the solder [1]. Therefore, electronic industries pursued new solder compositions such as lead-free solders. Commercially used lead-free solders contain tin, copper, silver, and many other types of metals.

Due to the industry change from Pb-rich solders to Pb-free solders, research had to be conducted to ensure the same interconnect reliability will be obtained from the “new” solders. New issues aroused which affected the reliability of such solders. Focused studies on electromigration (EM) in interconnect solders, one of the most persistent reliability concerns in microelectronics packaging systems, were conducted in investigating the impact of transition from lead-rich to lead-free solder material

Electromigration is a mechanism involving the mass transport of an atom driven by combined forces of electric field and charge carriers. There are two forces that are exerted on the atoms that cause the mass transport which are a Columbic force produced by the electric field and the force exhibited from the momentum transfer in the flow of carrier charges [2]. Detail of EM mechanism is discussed in next Electromigration Section (see Section 2.3). In many electronic devices, electromigration affects interconnect electrical conductivity, causing a premature failure and impacting the performance of the component.

Consequently, there is an industry need to find a solution to reduce the effect of electromigration as the demand for smaller, high quality devices continuous to increase.

2. LITERATURE REVIEW

Flip chip also referred as C4 (controlled collapse chip connection) technology has been affected by continuous miniaturization and need for lead-free materials. A flip chip interconnection is the connection of an integrated circuit chip to a substrate. This package allows for high input/output (I/O) counts by bonding the contacts directly to the substrate. The C4 process consists of depositing solder bumps on solder wettable metal terminals on the active surface of the semiconductor chip that connects to the matching wettable pads on the ceramic, polymer, or composite substrate. The solder bumps are then aligned and reflowed at higher temperatures to form electrical and mechanical connections. An under bump metallization (UBM) layer is also used to improve adhesion between bond pads within the circuit and to provide protection from the environment (e.g. corrosion). The most common metallization layers are Al, Cu and electroless Ni [3]. Figure 1 below

shows a schematic of a flip chip package where the solder bump connects the Si chip and substrate along with the UBM layers.

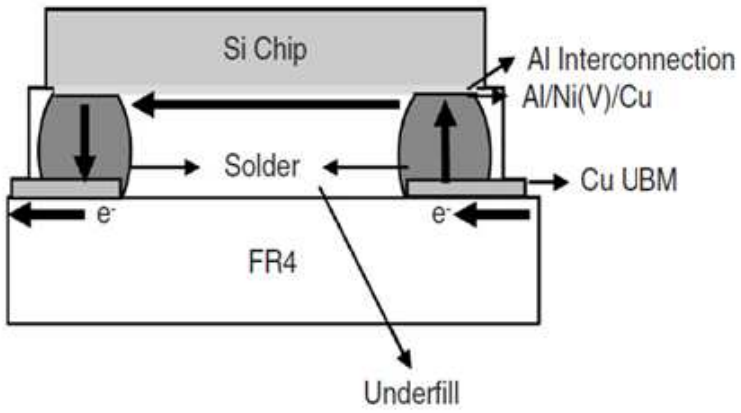

Figure 1: Schematic showing the flip chip package configuration where the Si chip and package is connected by the solder and UBM layers [4].

2.1 Solder Materials (Lead-rich and Lead-free)

In flip-chip technology, lead-based solder materials had ideal properties to be used, but the environmental hazard and awareness of the involving health risks triggered industries to look for alternatives. In the paper written by Zeng and Tu, the role of Pb in solders was discussed in great detail and summarized below [5].

Pb provides ductility to the solder, which is very important since the solders are exposed to thermal loading during manufacturing and undergo repeated shear, tension, and compression cycles during use/operation. In addition, Pb lowers the surface and interfacial energies of the solder. Surface energy is the interaction between the forces of cohesion and the forces of adhesion which determines whether or not wetting, the spreading of a liquid over a surface, occurs. If complete wetting does not occur, then a bead of liquid will form with a high contact angle which is a function of the surface energies of the system.

Addition of Pb reduces the surface energy, enabling a better contact between the surfaces. Comparing pure Sn with a Pb-solder, the wetting angle of molten eutectic SnPb on Cu is 11° and that of pure Sn on Cu is 35°. Figure 2 below is a schematic showing the difference of wetting angles between a SnPb solder and a Pb-free solder. Furthermore, the eutectic SnPb solder has a low eutectic point or melting temperature at 183 °C leading to low reflow temperatures typically around 200 °C. As a result, silicon does not have to be exposed to extremely high temperatures during the reflow process which is one of most important characteristics of SnPb solder [5].

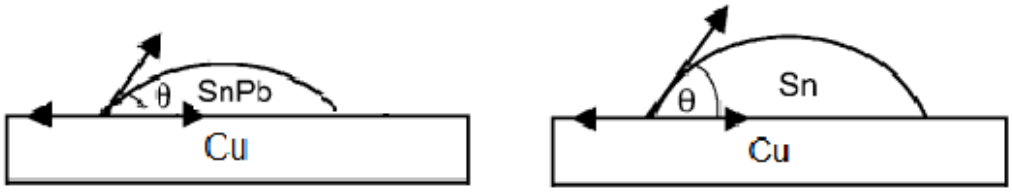

Figure 2: Schematic showing the wettability of a SnPb solder compared to a Sn-rich solder where the wetting angle of SnPb is much lower than Sn.

2.1.1 Pb-free Solder Characteristics

In an attempt to achieve the same or better properties of SnPb solders, many different elemental configurations were studied. Most of the compositions of Pb-free solders consist of eutectic Sn-alloys and noble metals such as Au, Ag, and Cu. A eutectic alloy is commonly used as solder because it has one single, low melting point [6]. Thus, the entire solder joint will melt or solidify at a certain temperature; otherwise partial melting or solidification may occur.

In general, eutectic Sn-noble metal alloys have a higher melting point compared to that of eutectic SnPb. This will result in higher reflow temperatures of approximately 30 °C higher than Pb-rich solders, which can increase the dissolution rate and solubility of Cu and Ni UBM layers in the molten solder as well as the rate of intermetallic compound (IMC) formation with the UBM layers. Furthermore, the wetting angle of "replacement elements" on Cu is higher than that of Pb which reduces the surface area of the overall solder contacting the Cu interconnect.

Microstructural differences are also present in SnPb and Pb-free solders. Pb-free solders generally consist of a mixture of solid solution Sn phase and IMC precipitate phases (see Figure 3a for a Sn-Ag-Cu solder alloy) while the SnPb solder consists of Pb-rich and Sn-rich solid solution grains with no evidence of IMC formation inside the solder balls (see Figure 3b). Intermetallic phases (IMC) at the solder joint are similar in chemistry for both lead-rich and lead-free due to the presence of the Cu pad, with some difference in morphology reported. IMC formation can be influenced by many different parameters and conditions, impacting the reliability of the solder. Most IMC layers are brittle in nature and its presence reduces the conductivity of interconnects. Therefore, it is important to better understand the mechanisms and morphology of IMC formation in these Pb-free solders compared to the historic SnPb solders [5].

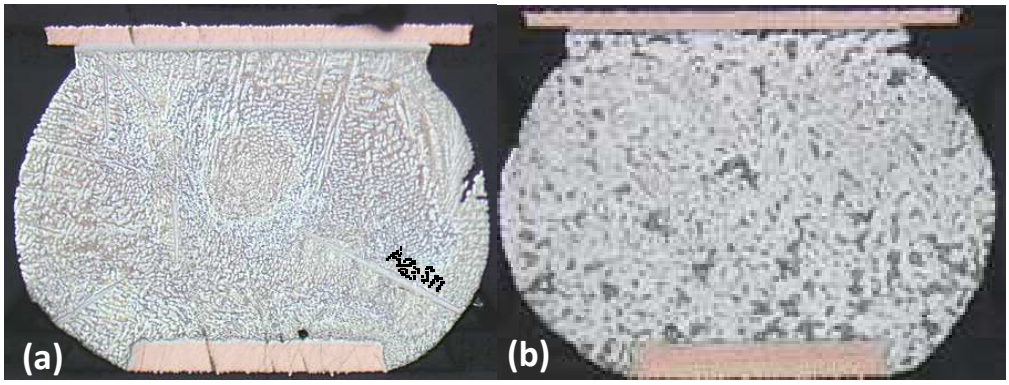

Figure 3: a) Representative lead free solder: Sn-0.4Ag-0.05Cu in wt% (SAC405) material with Sn-rich dendritic structure and IMC noted as Ag_3Sn. b) Representative lead-rich solder: SnPb material with Sn-rich and Pb-rich phases shown as light and dark regions, respectively.

Lead-free solders which primarily consist of Sn has body-centered tetragonal (BCT) lattice structure at temperatures above 13.2 °C (see Figure 4), with additional atoms located at 0.5, 0, 0.25 and at 0, 0.5, and 0.75. Crystal structure of Sn at low temperature is diamond, with semiconductor characteristic. BCT tin lattice parameters are a= b=0.583 nm, and c=0.318 nm, with ([001]/(100)) and ([110]/(001)) as the directions/planes having the most closed and the least- packing, respectively. The active slip system in Sn is believed to be (100) [001] [7].The atomic radius of tin is 0.151 nm. Anisotropic behavior, as well as, preferred crystal and IMC growth direction are therefore expected on single crystal grains of solder material. For example, one would expect the growth in the direction perpendicular to the least closed packed plane to dominate (the least closed packed a plane is to the surface plane, the easier it is for atoms to attach themselves to the crystal). This behavior lends itself to the fact that least close packed plane grows faster,

and growing plane assumes faces that are closed packed [8]. With HCP structure IMC forming at Cu-Sn solder joint, one would expect the IMC growth taking the basal plane front alignment with the c-axis.

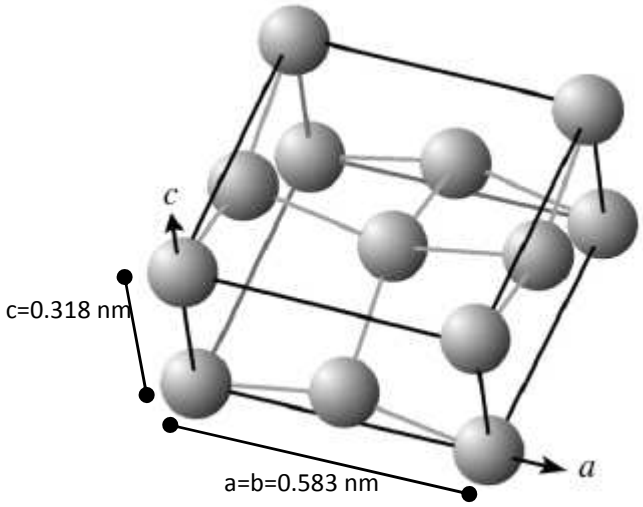

Figure 4: Tin BCT crystal lattice with additional atoms located at 0.5, 0, 0.25 and at 0, 0.5, and 0.75 [9].

2.1.2 Effect of Solder Grain Orientation

With reduction in solder bump size, the polycrystalline nature of the individual solder bumps lends itself to few grains, eventually approaching that of single crystal/grain morphology. This change in microstructure and the anisotropy associated with single crystals adds additional complexity to reliability analysis. ASU-Intel study presented in Section 3 of this report focuses on the effect of grain orientation on electromigration in solder interconnect.

Study performed by Tae-Kyu Lee et al. [9] investigated the impact of thermal exposure on Sn grain orientation in a wafer level chip scale package (WLCSP), and

further evaluated the effect of orientation on crack initiation and propagation and reliability of Pb-free solders. The solder bumps in this study were aged at 100 °C and 150 °C for 500 hours and then thermally cycled from 0° to 100 °C with 10 minute dwell time. The resulting grain orientations were quantified using EBSD analysis of the tested solders, and the color coding discussed below was established. The color scheme used was based on the orientation of solder grain c-axis with respect to the package plane (see Figure 5 below). The red oriented grain in this study was associated with Sn grain c-axis parallel to the package plane. Correspondently, joints with blue oriented grains were those with the c-axis highly inclined w.r.t. the package plane.

Lee et al. [9] studied the impact of Sn grain orientation on the mechanical and thermal properties of Sn solders. From this study, it was noted that the red oriented grains were more sensitive to crack initiation and propagation. Figures 6 and 7 show two solder joints where one has a “red” orientation (c-axis parallel to package plane) and the other has a “blue” orientation (c-axis perpendicular to package plane). The red-oriented joint has a large crack that propagated across the solder joint while the blue-oriented joint has a small crack in the corner of the joint. This study demonstrated the effect of grain orientation on the mechanical properties of the solder joints which influences the reliability of the package. This behavior is associated with the fact that Sn grain c-axis is aligned in the direction of the shear stress (developed during thermal cycling due to CTE mismatch between the package and device), which aligns the active slips system (001)[100] in the direction of shear stress, hence fast crack propagations can be observed relative to other grain orientations [9]. Compared to the red-oriented grains, green and

blue-oriented grains require higher stresses for plastic deformation (orientation and Schmidt factor effect) at the solder joint, hence the observed behavior.

It should be noted that thermal exposure and the resulting high thermal stresses developed due to CTE-mismatch at solder joints can result in formation of recrystallized grains and/or in solder grain rotation leading to grain realignment which impacts solder reliability. Figure 7 reveals the formation of recrystallized grain at the high stress region of the solder joint.

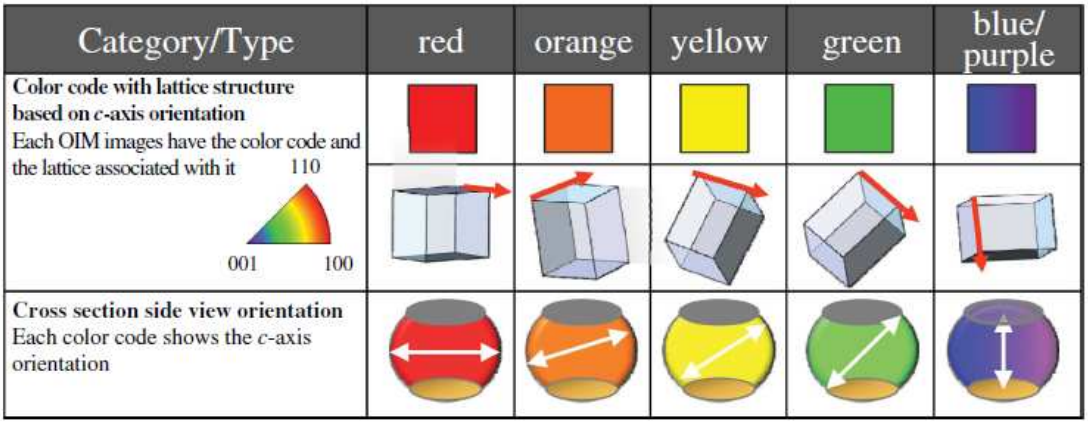

Figure 5: Chart showing the lattice structure with respect to color designation and c-axis orientation. (Red arrow represents the Sn-crystal c-axis) [9].

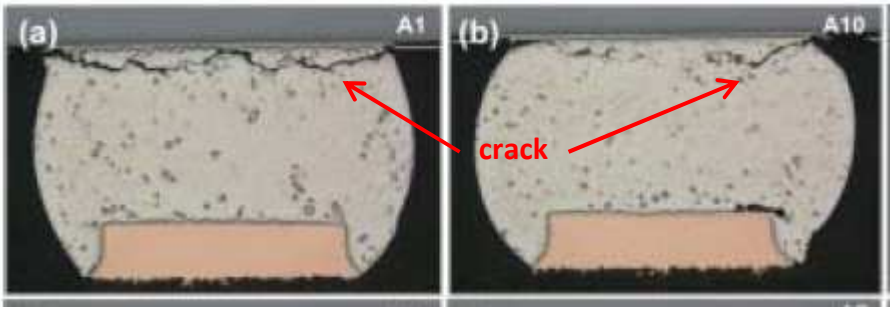

Figure 6: Optical images of two representative solder joints thermally tested. a) solder joint with crack propagating throughout the package plane. b) solder with small crack present [9].

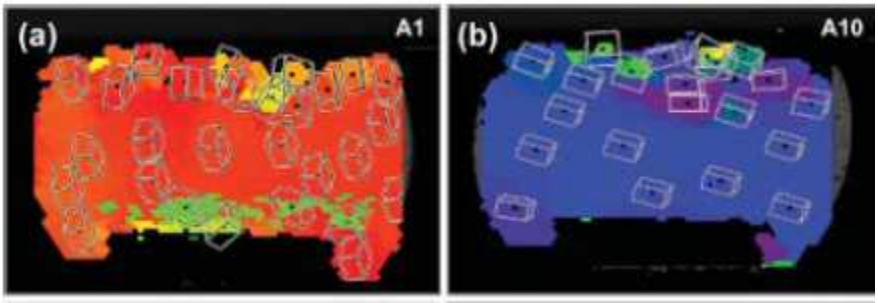

Figure 7: EBSD map showing crystal orientation and lattice structure from solder joints shown in Figure 6. a) large crack observed in red-oriented grain. b) small crack observed in blue-oriented grain. Both solders show recrystallized grains forming at the high stress region of the solder joint [9].

2.2 Intermetallic Compound (IMC) Formation in Solders

Lead-free solder materials which are now widely implemented in microelectronics components consist of primarily Sn and minor alloying elements. Without lead, and with higher processing temperatures, the intermetallic layers at the solder/UBM interfaces are

much thicker and have a different microstructure and morphology. In flip-chip manufacturing, this problem becomes more severe than other lead-free soldering processes in electronic packaging (e.g. wire bonding) because of the need to perform multiple reflow processes. A uniform IMC at solder joint is desired to improve the adhesion between the solder and the substrate and minimize stress concentration. On the other hand, excessive and thick IMC formation can lead to complete consumption of the UBM material, and can cause premature failure at the interface [10]. Increased reflow and/or operating temperature and with such high current densities, fast diffusion of atoms in the lattice is foreseeable, hence, potentially causing reliability issues.

The primary component of the solder alloy forming IMC at the solder joints is Sn reacting with Cu or Ni, which are the major constituents of under-bump metallurgy (UBM), to form IMC layers in both lead-free and lead-rich solders (in SnPb solders, Pb remains inactive). With the abundant supply of Sn in Pb-free solder compared to Pb-rich solder, the IMC growth at the solder-UBM joint is found to be substantially enhanced by EM due to the ample supply of Sn that is available to react with the UBM material [10].

For the solid-state reaction between Cu and Sn, and between Ni and Sn, the following reactions lead to IMC formation [11]:

$$\begin{aligned} 9Cu + Cu_6Sn_5 &\rightarrow 5Cu_3Sn \\ 6Cu + 5Sn &\rightarrow Cu_6Sn_5 \\ 3Ni + 4Sn &\rightarrow Ni_3Sn_4 \end{aligned} \qquad (1)$$

The Cu_6Sn_5 phase has either rounded or faceted scallop-type morphology after multiple reflows. As the Cu content increases due to time dependent diffusion, one expects the formation of Cu_3Sn in addition to Cu_6Sn_5 at the solder joints as well. Layer-type

morphology of the Cu_6Sn_5 and Cu_3Sn is observed and reported by other investigators [11]. Different IMC phases that are formed can be easily determined by using the appropriate phase diagrams (see Sn-Cu phase diagram in Figure 8). In SAC (Sn-Ag-Cu) solder system and/or in the presence of Ni metallization layer, ternary phase diagrams such as those shown in Figure 9 and 10, respectively, should be used. These figures not only reveal the different intermetallic compounds that can form with respect to percentage/content of material present, it also provides melting temperatures of different solder composition.

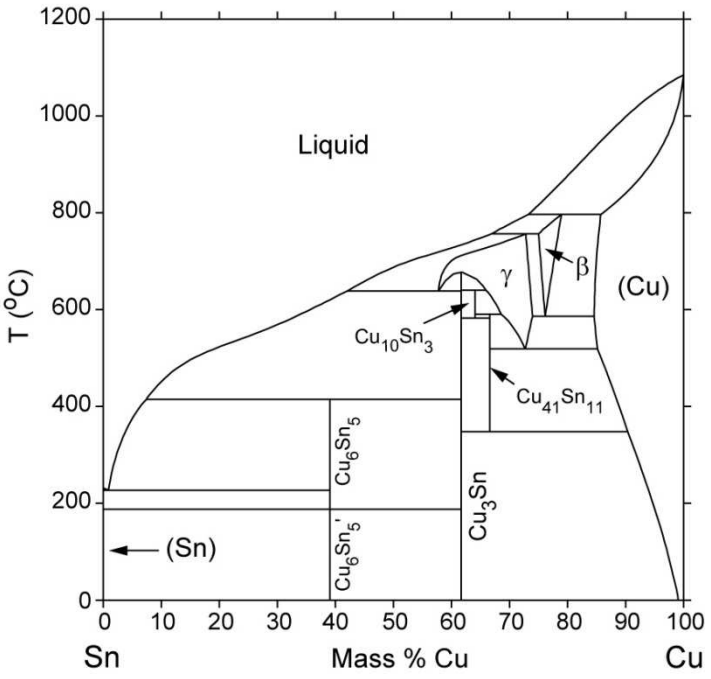

Figure 8: Sn-Cu phase diagram demonstrating the multiple phases depending in Cu mass percentages and temperature [12].

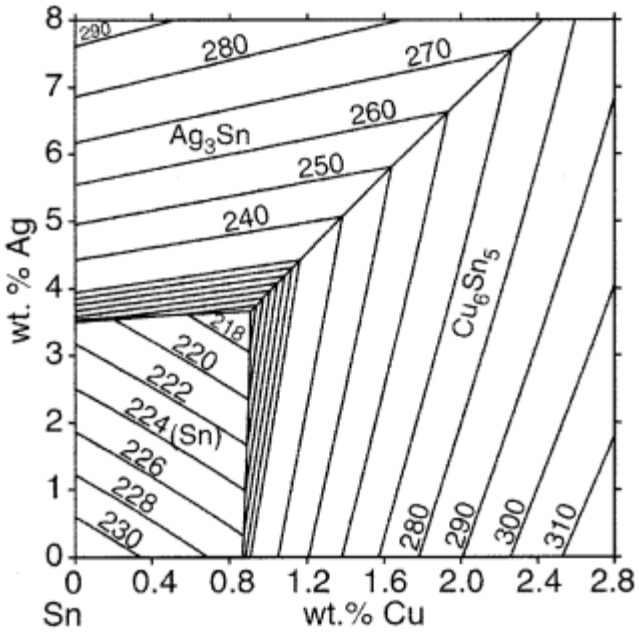

Figure 9: Close-up of tertiary phase diagram for Sn-Ag-Cu (SAC) solder [13].

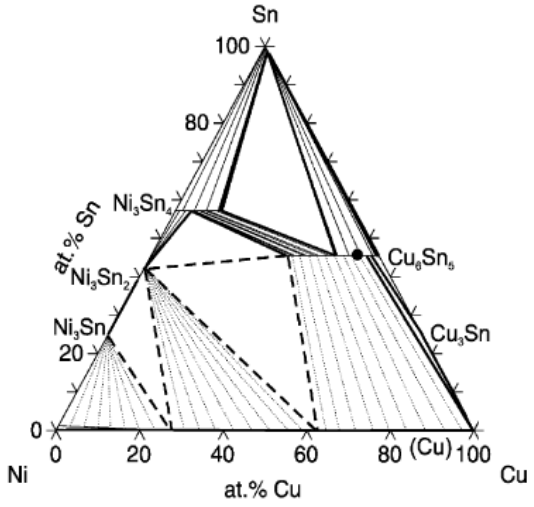

Figure 10: Tertiary phase diagram for Ni-Cu-Sn solder at 235 °C [5].

2.3 Electromigration in Interconnects

Electromigration associated with mass transport due to applied current is of critical concern for microelectronics component integrity. Electromigration in solder bumps can lead to premature failures by creating voids or hillocks which affect the mechanical, electrical, and thermal properties of the device. Voids are areas where atoms are depleted and are commonly developed on the cathode side where the electrons enter. On the other hand, hillocks are areas where atoms are deposited resulting in mass accumulation and are developed at the anode side where electrons depart. Void formation occurs when the flux of outgoing atoms exceeds the incoming flux causing an opening in the solder material. Conversely, hillocks occur when atoms are piled up at a point where the incoming atom flux exceeds the outgoing flux. These hillocks and voids are stress concentration areas that can influence mechanical integrity. These can also introduce an impedance mismatch in interconnects which increases the resistance and therefore affect the signal integrity of such device [14].

The following figures are scanning electron microscope (SEM) secondary images showing a cross-sectional view of a solder bump exposed to a current density of 1.3×10^4 A/cm^2 after 37.5 hours. Figure 11a shows the entire solder area and the electron direction going from top to bottom revealing the void and hillocks formation in the cathode and anode, respectively (see higher magnification photomicrographs in Figures 11b and 11c). Crack initiation due to stress concentration associated with voids and hillocks are also evident in Figure 11c.

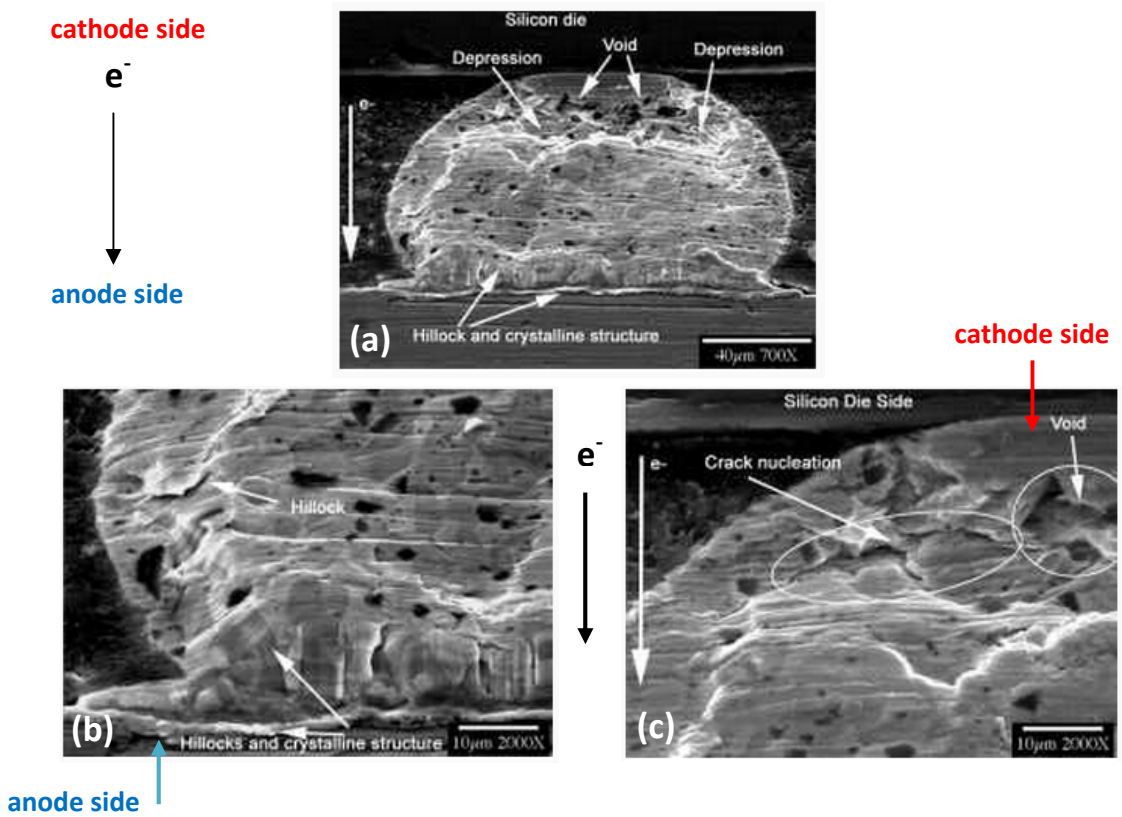

Figure 11: SEM images of solder joint after 37.5 hrs showing void and hillock formation, (b) anode side, (c) cathode side [15].

2.3.1 Effect of Electromigration on Intermetallic Compound (IMC) Formation

High current density associated with reduced interconnects and resulting electromigration mechanism can further aggravate the formation of intermetallic compounds in solder joints. As discussed in the next section, the flow of energetic electrons can lead to increased atom migration. This effect furthers the mobility of Cu atoms from UBM into Sn solder, leading to increased level of IMC growth. Many studies [11] [16] [17] have shown the increase level of IMC growth due to electromigration, over and beyond what is expected from thermally diffused atoms.

With increasing IMC, the current stressing will also increase since the contact area between the solder and the UBM will diminish as more atoms continue to migrate from the UBM to create more IMC. In addition, IMC layers can lead to local embrittlement which can lead to premature failures in the solder joint [1].

IMC growth results in a net volume change of the bump material, and the corresponding volume change ratios ($\Delta V/V_0$) can be significant. As the IMC growth continues, there is less solder material present affecting the mechanical and electrical reliability of the bump.

2.3.2 Physics of Electromigration

Electromigration is described as the mass transport of atoms driven by combined forces of electric field and charge carriers. The drifting electrons collide with atoms causing one of the atoms to exchange position with neighboring vacancies during current stressing. A schematic showing the migration of atoms for aluminum samples is shown in Figure 12. The necessary current density needed to initiate the movement of an atom is defined as the threshold current density. After stressing for an extended time, atoms in interconnects accumulate on the anode end resulting in void formation on the cathode side which can lead to open failure with time. In general, the average drift velocity of atom due to EM is given by Huntigton and Grone shown as below.

$$v = \frac{J}{C} = BeZ^*\rho j = \left(\frac{D_0}{kT}\right) eZ^*\rho j \exp\left(\frac{-E_a}{kT}\right) \quad (2)$$

where J is the atom flux, C is the density of metal ions, B is the mobility, k is the Boltzmann's constant, T is the absolute temperature, eZ^* is the effective charge of the

ions, ρ is the metal resistivity, j is the electrical current density, E_a is the activation energy of diffusion, and D_0 is the pre-factor of diffusion constant [2].

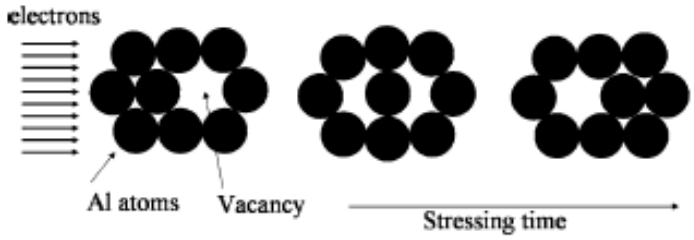

Figure 12: Schematic for EM of Al atoms along current flow [2] .

There are two main conditions that need to be satisfied for electromigration to occur. First, the atoms must have sufficient energy to overcome the barrier for diffusion. Second, there must be a site which is energetically and geometrically favorable for the atom to move in. Vacancies within the lattice, dislocation cores, grain boundaries and voids are potential favorable sites. At low temperatures, grain boundary migration dominates since vacancy formation requires lattice vibrations given by at higher temperatures [18].

2.3.3 Parameters Influencing Electromigration

Many parameters such as temperature, time, current density, current crowding, joule heating, and solder grain orientation influence the rate of EM. Details of their impact are discussed in the following sections.

2.3.3.1 Current Density Effect

Continuous miniaturization of electronic devices is driving the shrinkage of under-bump-metallization (UBM) layer and the solder bump contact area. Currently, the typical C4 (controlled collapse chip connection) solder bump size ranges from 50 μm to

100 μm. These solder bumps carry currents of approximately 0.2 A which results in a current density of approximately 10^4 A/cm^2. The smaller cross sectional areas exposed to higher currents leads to a drift of the atoms in the direction of the electron flow. This is characterized as the flux density [2].

The relationship between the current and the mean time to failure (MTTF) of a semiconductor circuit due to electromigration is approximated by Black's equation. This equation is derived as:

$$MTTF = Aj^{-n}e^{(\frac{Q}{kT})} \quad (3)$$

where A is a constant, j is the current density, Q is the activation energy for diffusion, k is Boltzmann constant, T is the absolute temperature, and n is a variable current density exponent which can be determined experimentally. From this equation, it is observed that the MTTF is inversely proportional to the current density. As a result, with increasing current densities due to area reductions, electromigration induced failures in interconnect will occur at a faster rate [19].

2.3.3.2 Current Crowding

In addition to the decreasing size factor, current crowding is another issue to consider. As shown in Figure 13 below, when the electrons flow through the UBM, the electric field path is horizontal. As the UBM meets with the solder bump, the electric field changes from its horizontal trajectory to a vertical path. The electrons entering the solder bump at the edge of the solder create a localized high current density area which is referred as current crowding. Localized high current density leads to increased tendency for nucleating a void at the edge of the solder bump [18]. As these voids develop, it

changes the current path by forcing the electrons to flow further before entering the solder bump. As the voids continue to grow, the current increases and it adversely impact the reliability of the solder bump further. Figure 13 demonstrates a schematic of current crowding and the change of electron flow direction. With increasing void size, the overall contact area between the solder bump and the UBM is reduced resulting in higher current densities.

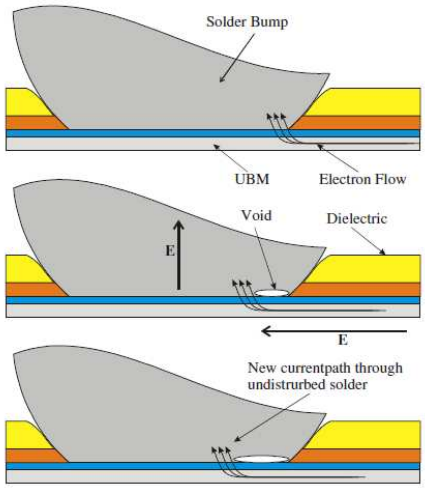

Figure 13: Schematic of current flow pattern of solder bump demonstrating the change of current path as the void increases in size [18].

2.3.3.3 Temperature and Joule Heating Effect

Due to the micro scale of the solder joints, the multiple copper and other metallic layers above the solder generate a large amount of heat (Joule heating) from the high current densities it experiences. This heat creates a thermal gradient in the order of 10^4 $°C/cm^2$ between the metal layers and the solder, which further affects the atom flux as expected by diffusion mechanism and the diffusivity equation shown below:

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right) \quad (4)$$

where D_0 is a temperature-independent coefficient, E_a is the activation energy for diffusion, k is Boltzmann constant, and T is temperature in Kelvin. Diffusivity is the material constant which represents the mobility of atoms or vacancies. Temperature plays an important factor in the diffusivity of atoms from the metallic layers to the solder material. As temperature increases, the diffusivity also increases.

Experiments by other investigators [20] have shown that the dominant diffusion mechanism in the solder joints is grain boundary diffusion, where the grain boundaries provide fast paths for Sn, Cu and other alloying elements to diffuse and grow intermetallic compounds. High rates of diffusion can cause shorts between the current carrying line and solder/UBM interfaces leading to interconnect failures [20].

2.3.3.4 Grain Orientation Effect on EM and IMC Formation

An electromigration study conducted by Chris Kinney et al. at the University of California demonstrated the influence of crystal orientation on intermetallic layer growth in SAC solder joints. The study was performed on thin, planar SAC solder layers between two Cu bars which were subjected to a uniaxial current. For this investigation, the samples were idealized to fully focus on the influence of current in the diffusion and growth of IMC excluding any thermal effects.

The samples consisted of three Cu segments connected by two solder joints of 250 μm length (Figure 14 shows the test setup). The testing parameters used were current

densities of 10,000 A/cm^2 and 11,500 A/cm^2 and an oven temperature of 100 °C.

Figure 14: Sample configuration with three Cu segments and two SAC solder joints with 6 mm and 250 μm in length, respectively [21].

Electron backscatter diffraction (EBSD) techniques were used to map and determine the crystallographic direction of grains over the entire solder joint. Kinney et al. introduced the concept of analyzing the EBSD data and color stereographic projection mapping to quantify the angle between the c-axis of Sn and the electron flow, varying from 0°-90°. A schematic of the color code map showing the orientation relationship between the c-axis and the electron flow is shown in Figure 15. Grain orientation map of their sample was hence color coded in a manner that a blue grain was indicative of grain orientation with the c-axis aligned/parallel to the electron flow, whereas the red color grain had its c-axis perpendicular to the electron flow.

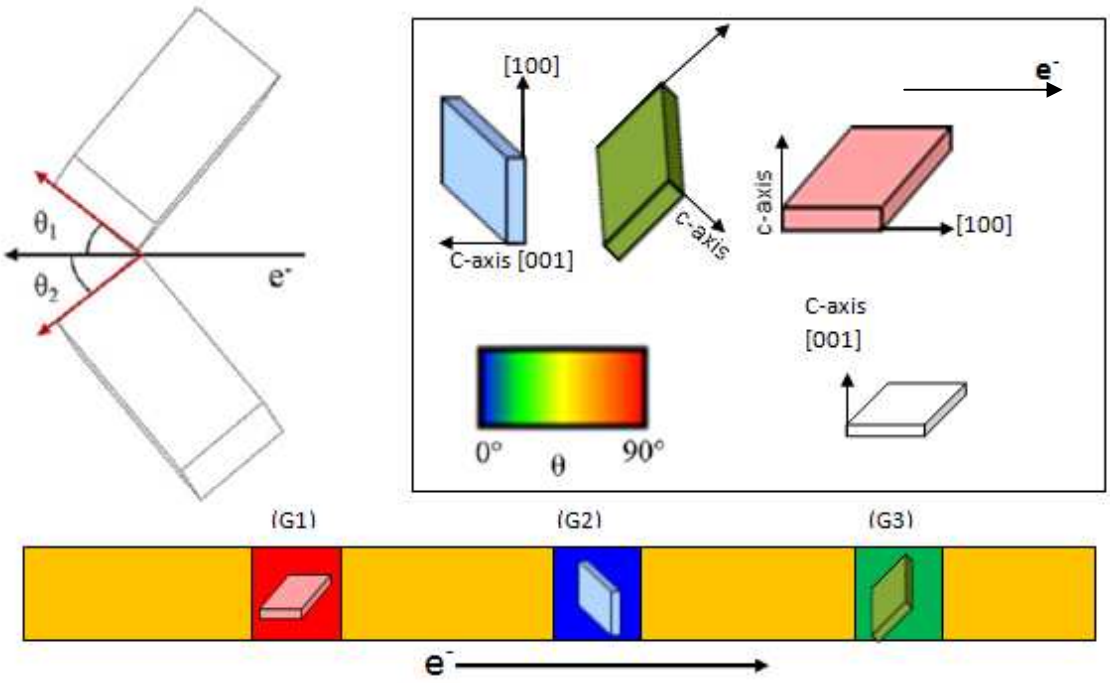

Figure 15: Schematic showing color gradient map in relation with c-axis of Sn and the electron flow. θ is the angle between such axis varying from 0-90 degrees. Examples of three lattice crystal orientations are shown colored to the corresponding color designation with respect to θ [21].

The testing was run on the lead-free samples over different times including 24 hrs, 48 hrs, 96 hrs, and 120 hrs for a group of solders oriented with c-axis mostly parallel to the electron flow (green color orientation in G3) and another group of solders with c-axis oriented perpendicular to the electron flow (red color orientation in G1). Figure 16 shows the solder samples with different orientations and tested at different times and Figure 17 shows the same solders highlighting only the amount of IMC formation with an HCP lattice structure. This study demonstrated that grains oriented with their c-axis parallel to the electron flow experienced significant IMC growth compared to samples containing

grains with their c-axis perpendicular to the electron flow. The IMC growth observed was nearly planar and constant along the Cu and Sn interface. It was proven that it is easier for electromigration to occur when both the grain orientation (c-axis alignment) and the electron flow direction are the same [21]. It is interesting to note that the IMC grain orientations reported by Kinney et al. (see Figure 17) is in line with the expected grain alignment (along HCP c-axis) we postulated earlier in section 2.1.1.

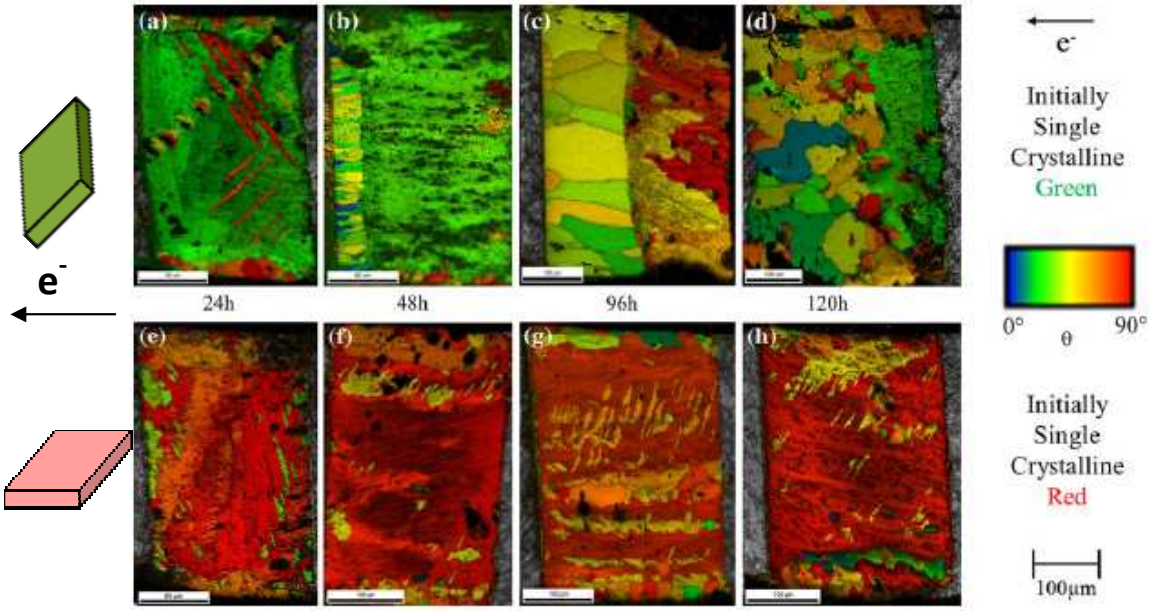

Figure 16: EBSD maps for two sets of solder orientations ("green" and "red" orientations) with respect to electron flow tested at 100℃ with 10 kA/cm^2 for different times (24, 48, 96 and 120hrs) [21].

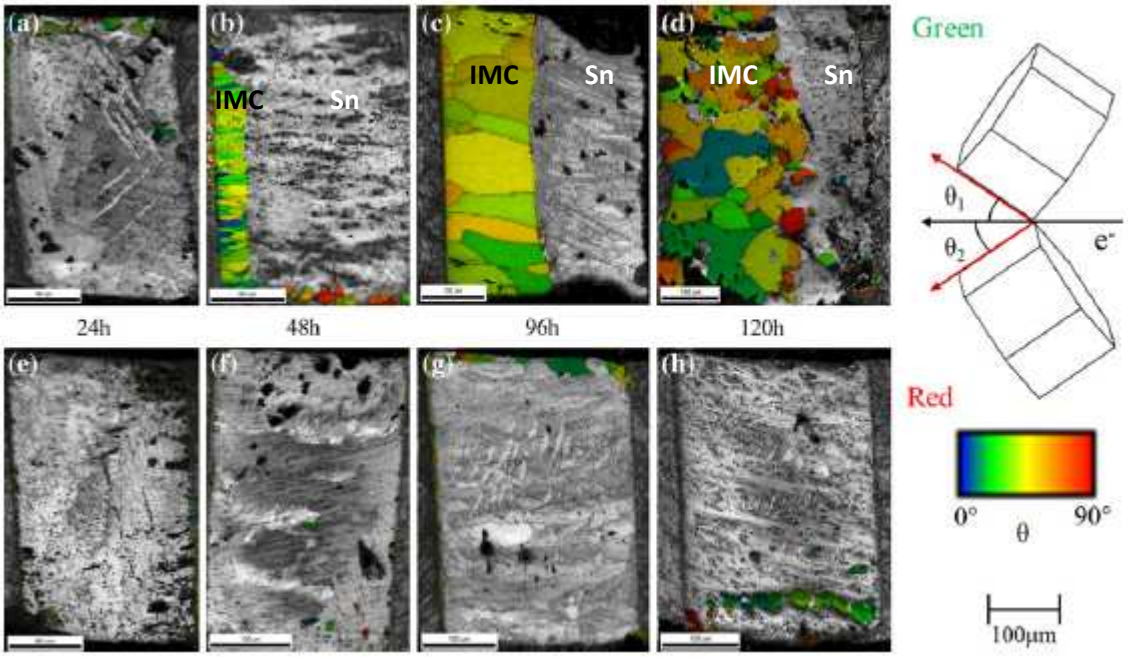

Figure 17: Same EBSD maps from Figure 16 with only the IMC region/grains highlighted for two sets of solder orientations ("green" and "red" orientations). It is shown that solders with "green" orientation have more IMC present than "red"-oriented solders over time. IMC grains growing with their basal plane (0001) normal to e- flow direction [21].

3. EBSD Analysis of First Level Interconnects (Flip Chip C4 Bumps)

The following sections discuss the steps taken to evaluate the effect of grain orientation on electromigration using EBSD analysis.

3.1 Experimental Procedure

For this study, three samples were provided by Intel which consisted of an array of first level interconnect (FLI) solders. The FLI solders are located between the chip and the package substrate in flip-chip ball grid array (FCBGA) as show in Figure 18. The interconnect material is Pb-free solder alloy of Sn-0.7Cu in wt%, consisting primarily of tin and minor additions of copper.

Electromigration test condition for all three samples were at a constant temperature of 165 °C and a current of 800 mA/bump. The samples were identified as sample 31, 36, and 39. The samples were I_{MAX} tested using an accelerated life test.

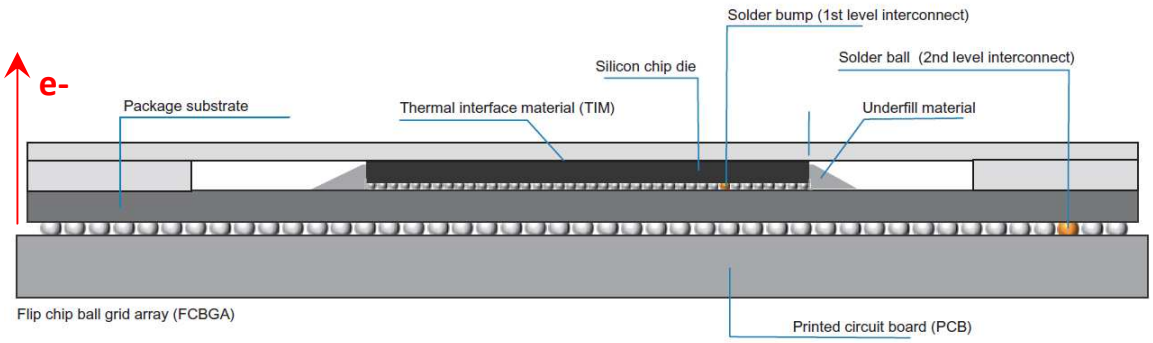

Figure 18: Schematic of FCBGA package showing location of FLI bumps [14].

3.1.1 Imax Testing

In our electromigration (EM) study to better understand the effect of orientation on EM, Intel manufactured samples were tested using accelerated life testing (ALT). One end-of-line (EOL) sample was provided in which we were able to determine the untested solder diameter and bump pad diameter to be approximately 84 µm and 64 µm, respectively. During the ALT, the controlled parameters are current density and temperature which were specified above. The current direction during ALT was the same among all the solder bumps. Figure 19 demonstrates the electrons moving from the cathode (substrate side, shown as the bottom side of the solder bump) to the anode (die side, shown as the top side of the solder bump).

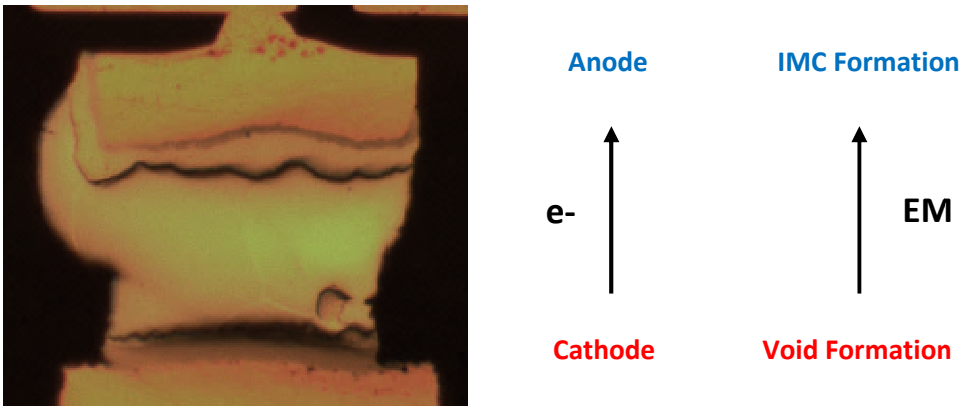

Figure 19: Solder bump showing the electron flow direction with respect to the solder alignment. Electron flow direction is from the cathode side (bottom of solder joint) to anode side (top of solder joint). Diffusion of atoms occurs along the same direction of the electron flow creating voids in the cathode side and IMC at the anode side.

The test conditions, as well as, the EOL and EM tested solder dimensions (averaged solder and substrate-side bump diameters) are listed in Table 1. With such

testing conditions, sample 36 failed at 221 hours, 39 failed at 215 hours and 31 at 227 hours.

Table 1: Sample and testing parameters used during EM testing.

Sample No	Avg. Solder diameter, µm	Avg. Bump pad diameter, µm	Current, mA	Current Density, A/cm^2	Test temperature, °C	Test Duration, Hours
EOL	84	64	None	None	None	0
31	78	60	800	24,881	165	226.75
36	82	56	800	24,881	165	221.86
39	78	59	800	24,881	165	214.96

3.2 Materials Characterization

Various characterization tools such as Optical microscopy, Scanning Electron Microscopy (SEM), and Electron Back-Scattered Diffraction (EBSD) were used in this study to analyze the effect of the parameters mentioned above on electromigration. The specifics of sample preparation and the characterization results are discussed in the following sections.

3.2.1. Sample Preparation for EBSD Analysis

Significant charging effect was observed on these samples when using ASU capabilities. Various techniques were utilized to increase the conductivity of the sample. One attempt was to mount dummy samples in conductive mounting material such as graphite. Carbon coating on the surface was also used. The amount of carbon coating had to be minimal since a thick carbon coating will reduce the x-rays signal for EBSD analysis. Another mounting material used consisted of mixing copper particulates with epoxy resin. This approach proved to be insufficient since the Cu particulates were

accumulating at the bottom of the mount, hindering the conductivity of the mounting media. Silver paint and copper tape were used to improve the overall conductivity between the mount, sample, holder, and microscope stage. Another challenge encountered was to achieve a completely flat surface. Since the solder material consists primarily of tin, uniform polishing was challenging because tin is a relative soft material compared to the neighboring materials (Cu and polymer materials). In addition, polishing was restricted to the FLI array. It was critical to maintain the EM-tested array and not polished through the area of interest. When the sample was not completely flat, black regions will appear in the EBSD maps with a confidence index of zero meaning there was no x-ray readings from this area.

In addition to the different sample preparations approaches used in alleviating the problem, we also used different scanning electron microscopes (SEM) available to this study at ASU (e.g., FEI XL-30 and FEI Nova 200 NanoLab). Due to the frequent occurring equipment problems/unavailability, and the reliability issues associated with the ASU systems during the course of this study, we were unable to obtain reliable results and decided to use an external laboratory resource that specializes on EBDS analysis. The three samples were sent to *EBSD Analytical,* a laboratory located in Utah. From the optical images, a number of solders were chosen from each sample for EBSD analysis. The criteria in which the solder were chosen for EBSD analysis was based on; (i) the amount of degradation or extensive IMC formation, (ii) lack of IMC or EM resistant solders, and (iii) IMC penetration along the grain boundary. The following solders were selected for detailed EBSD analysis in this study:

Sample #31: Solders 2, 7, 10, 14, 15, 16, 23, 25, 27
Sample #36: Solders 8, 9, 10, 33, 39
Sample #39: Solders 8, 9, 19, 20, 21, 22, 25, 26, 30

The sample preparation conducted at *EBSD Analytical* consisted of a brief polishing with 1200 grit SiC paper to improve sample flatness. Additional polishing steps were done using 1 μm alumina followed by 0.3 μm alumina. The final polish was done with 0.02 μm colloidal silica. In addition, a carbon coating of approximately 15 Å and silver paint were used to improve conductivity of the sample.

3.3 Results

Electromigration tested samples were characterized using various techniques. Details of the characterization techniques and the results are discussed in the following sections.

3.3.1 Solder EM analysis using Optical Microscopy

The first tool used was to capture images using an optical microscope to document the initial condition of the EM-tested samples received from Intel. Images were captured of the entire row of solders at 500x magnification. Sample 31, 36, and 39 consisted of 27, 41, and 36 solder bumps respectively shown in Figures 20-22. The photomicrographs of solder array reveal the extent of EM on different bump solder balls from which EM resistant solders (e.g. see sample 31, solders #1,10 and 11 in Figure 20 below), and those with extensive IMC formation (e.g. see sample 31, solders #22,23 and 25 in Figure 20 below) are identified. Presence of voids, and/or material loss were also noted on some solders (see sample 36, solder #35 in Figure 21). From each sample, representative solder bumps were chosen for EBSD analysis and texture pole figures for

these solder balls were constructed. Sample number and the solder position on array are also noted on these figures.

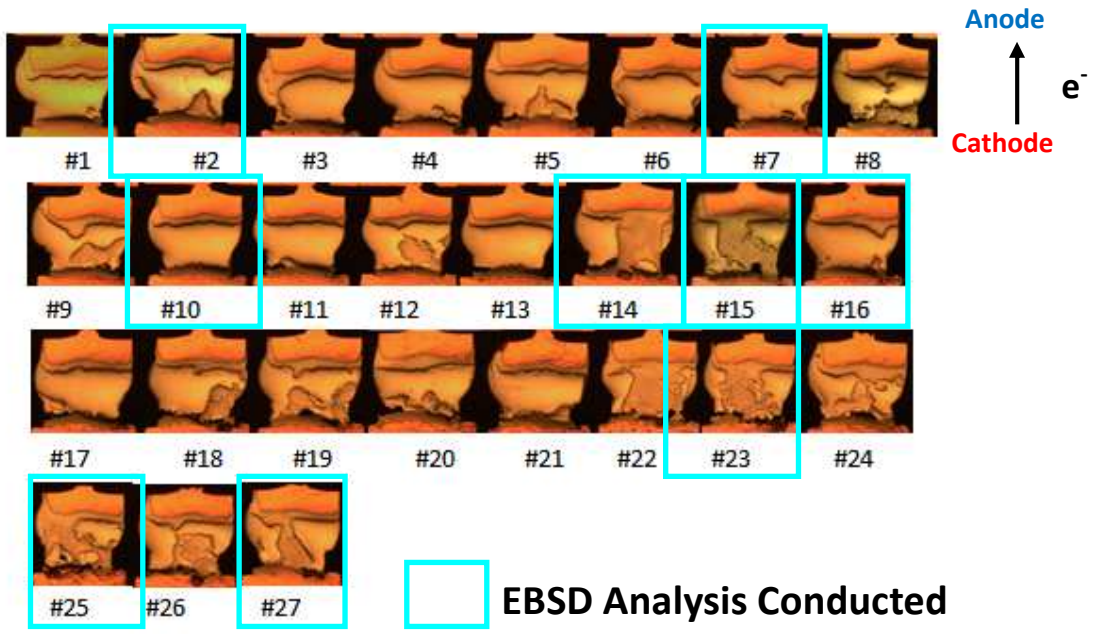

Figure 20: Optical images for solder array in sample #31.

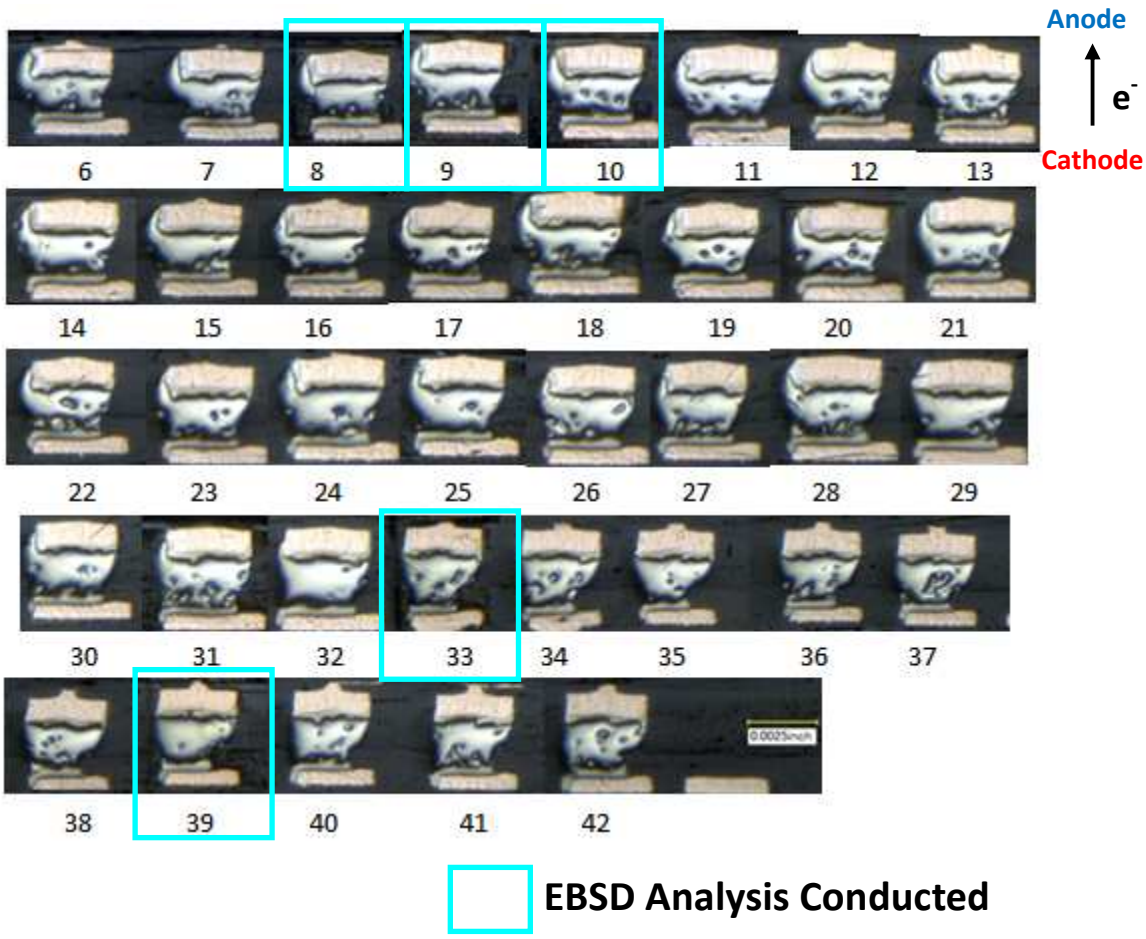

Figure 21: Optical images for solder array in sample #36.

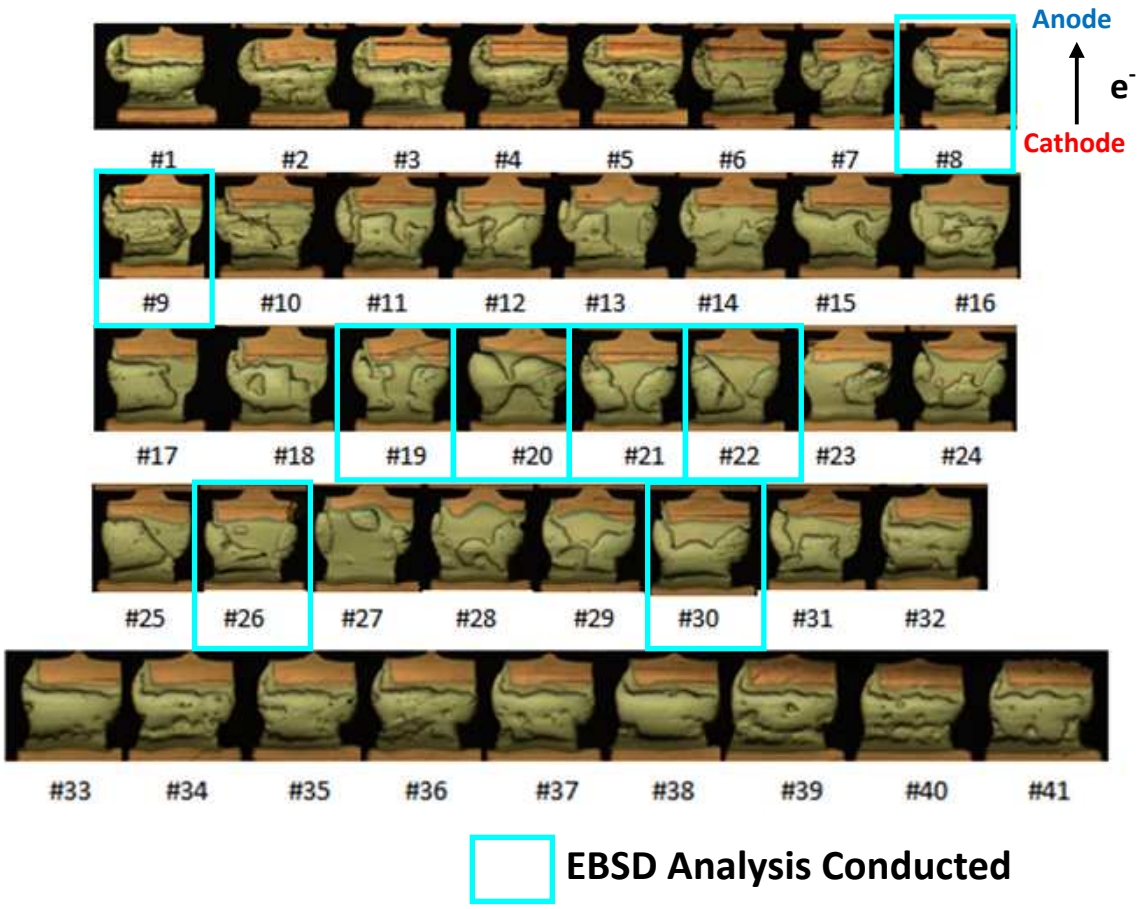

Figure 22: Optical images for solder array in sample #39.

3.3.2. Scanning Electron Microscope (SEM) Analysis

The next step was to obtain EBSD maps of representative bumps to further analyze the effect of orientation on electromigration. Extensive level of effort was devoted to obtain satisfactory EBSD maps with acceptable confidence indexes (CI) using the resources available at ASU. With the limited capabilities of ASU's XL-30 SEM system available to this project, we resorted to using outside lab services for EBSD characterization. Data obtained was analyzed and discussed below.

3.3.2.1.EBSD Data Analysis

High quality electron backscatter diffraction patterns (EBSPs) were obtained by *EBSD Analytical* where Kikuchi bands and poles were easily distinguished and indexed as shown in Figure 23. It should be noted that the bands are intersections of diffraction cones that correspond to a family of crystallographic planes, and a pole is referred to the intersection point of multiple bands/planes generated in EBSD analysis. Reliability of the EBSD analysis was based on Confidence Index (CI) metrics with values varying between 0 (low reliability) and 1 (high reliability).

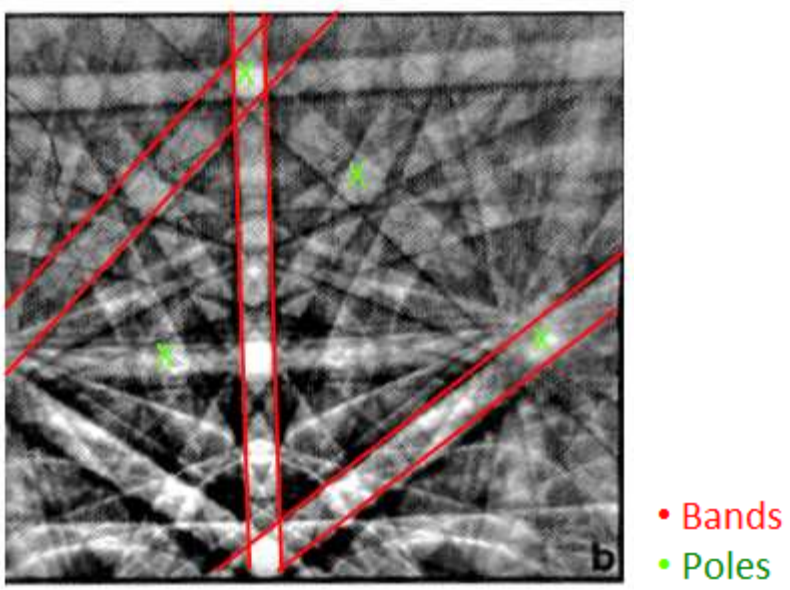

Figure 23: Example of electron backscatter patterns (EBSPs) where bands are highlighted in red and the poles are identified by green X's [22].

The raw EBSD data provided by *EBSD Analytical* lab were in the form of *Osc* files compatible to TSL OIM Analysis software. This data was further analyzed and manipulated at ASU lab by this investigator. Various forms and parameters of mapping were considered in this analysis to best identify any potential trend and relationships among the solders.

Figure 24 shows the appearance of the second solder bump in the array of sample 31 referred to as solder bump 31-2. The reason there is some difference between the optical image and the corresponding secondary electron (SE) SEM image is due to the sample preparation done previous to SEM documentation. As seen in Figure 24, the SE SEM image portrays a different plane of view after polishing, but still maintains characteristics that are unique and traceable to the original EM-tested bump.

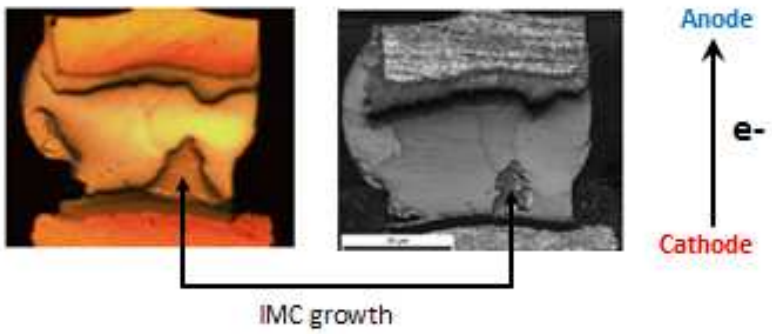

Figure 24: Optical image (left) and SE SEM image (right) of solder bump 31-2.

The first set of orientation image maps (OIM) developed were color grain maps associated with the inverse pole figures (IPF) with a reciprocal pole figure as shown in Figure 25 below. An inverse pole figure shows the pole that is parallel to a given sample direction. In other words, the orientation of the grain in question is based on the angle that the normal to plane-of-view has with that grain's [001] axis. Because of crystal symmetry, all the points in which the plane becomes parallel to the specified sample plane are plotted at the same position. This map displays the different grains present in the solder material and the pole figure reveals grain orientation with respect to a color gradient mode usually taken normal to the plane of the sample. In the case of solder 31-2

presented in Figure 25, there are six main grains within the solder and the orientation of each grain is colored with respect to the pole figure. For example, the light green colored grain has an orientation near [100] according to the pole figure presented in Figure 25 below.

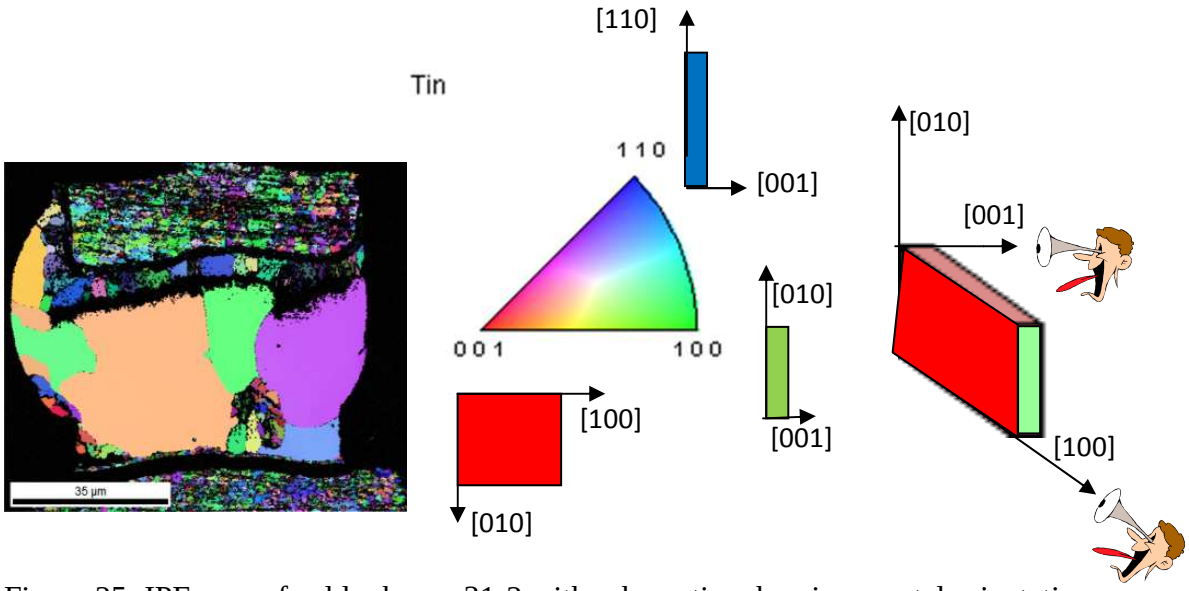

Figure 25: IPF map of solder bump 31-2 with schematics showing crystal orientation with respect to color designation.

In order to differentiate the solder material from the intermetallic layers and the copper traces, an elemental map was also obtained (see Figure 26). The areas of the interconnect colored in red, green and yellow correspond to tin, copper and IMC layers, respectively. It should be noted that the crystal structure of tin, copper and IMC layers are body centered tetragonal (BCT), face centered cubic (FCC), and hexagonal closed packed (HCP) crystal structures, respectively.

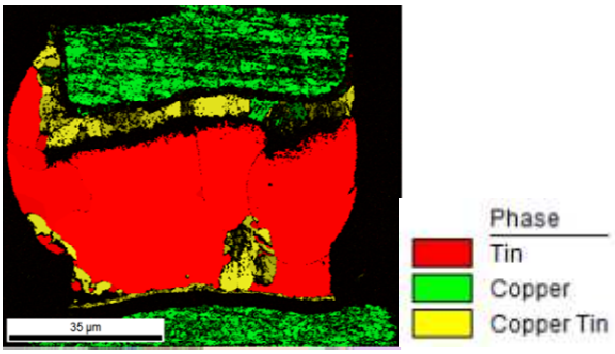

Figure 26: Elemental map of solder bump 31-2.

In our attempt to validate the results of the study by Kinney et al. [21] and to investigate the applicability of their conclusions to C4 interconnect bumps; we analyzed the EBSD data in accordance with that discussed in Section 2.3.3.4. In this approach, a different type of gradient color map is considered in displaying the grain orientations instead of using a basic IPF map which will be referred as stereographic projection 2 (SP2) maps [21]. As discussed earlier in Section 2.3.3.4, Kinney et al. evaluated the orientation effect on EM using the angle between the c-axis of Sn lattice structure and the electron flow direction. Since the electrical current flows along the solder bump axis or interconnect direction perpendicular to solder joint, we should also analyze the EBSD data with respect to the angle that solder grain [001] direction makes with the electron flow direction in the solder. In other words, we need to specify the orientation of the grain in such a way that it provides the angle between the vertical axis in the plane-of-view with that grain's [001] axis (i.e., 90 degree rotation compared to IPF shown in previous section).

Using this approach, we can manipulate our EBSD maps to reflect a color gradient in terms of the angle between the c-axis and the electron flow ([001]) that ranges

from 0 to 90 degrees (e.g. tolerance). Under such conditions, grains oriented parallel to the electron flow (an angle of 0°) will be represented by blue color while grains oriented perpendicular to the electron flow (an angle of 90°) will be colored red. This is also described in Figure 15 in more detail. Using these parameters, the EBSD map for solder 31-2 changed from a typical IPF map shown in Figure 25 to a new color gradient map (SP2) shown below in Figure 27. Note that the pole figure has only five main colors which range from blue to red. Using this approach, grains oriented with their [110] orientation or the [100] orientation along the current direction will both have their c-axis [001] perpendicular to the electron flow and will appear red since both are oriented 90° with respect to the electron flow ([001]).

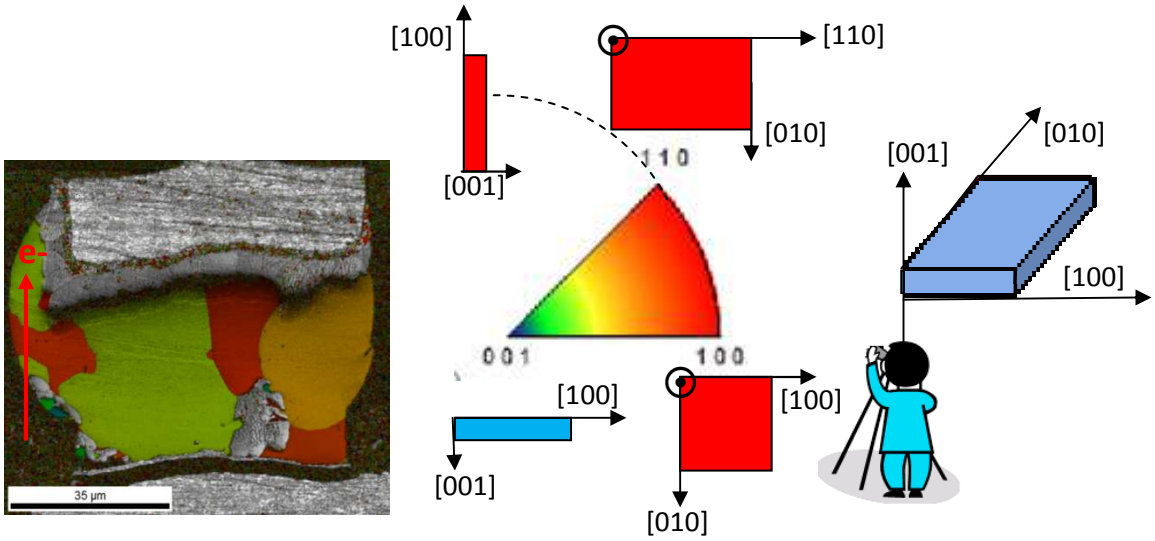

Figure 27: SP2 map w.r.t. the [001] from 0°-90° for solder 31-2 with schematics showing crystal orientation and color designation.

3.3.2.2.EBSD Test Results

EBSD data generated on selected solders from there EM tested samples are presented in Figures 28, 29, and 30 for samples 31, 36, and 39, respectively.

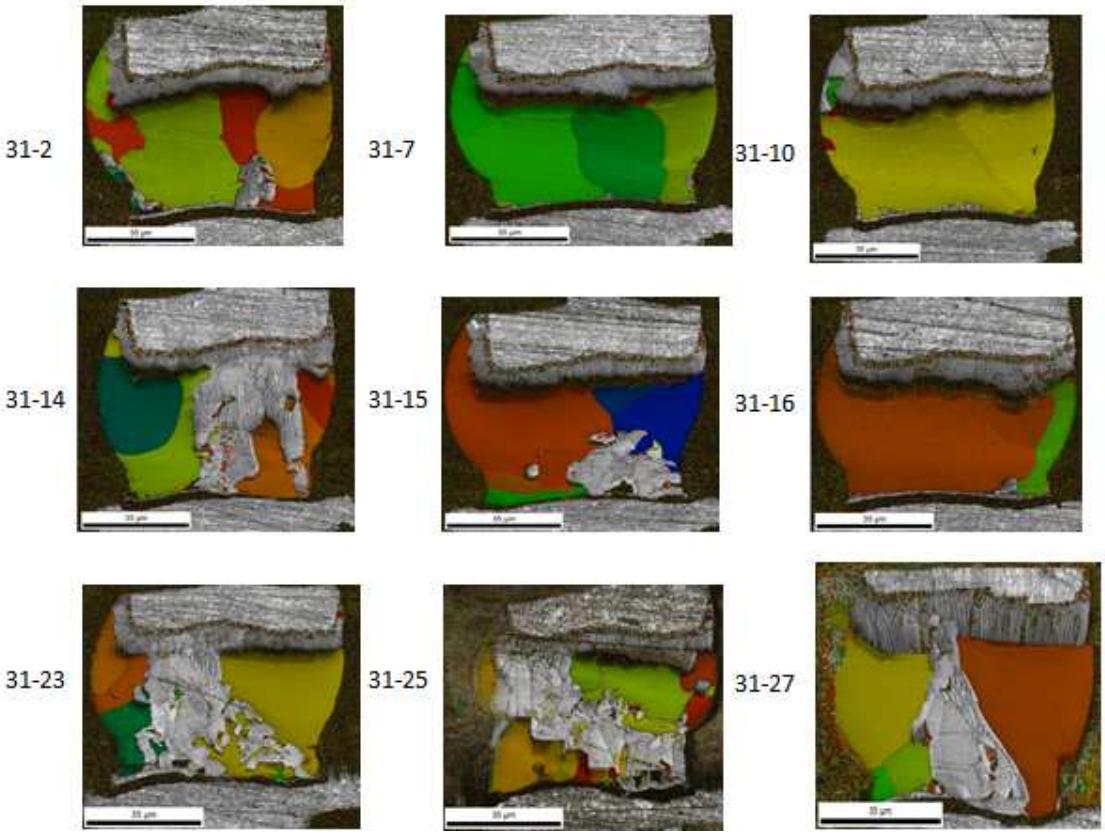

Figure 28: SP2 maps for selected solder bumps in sample 31.

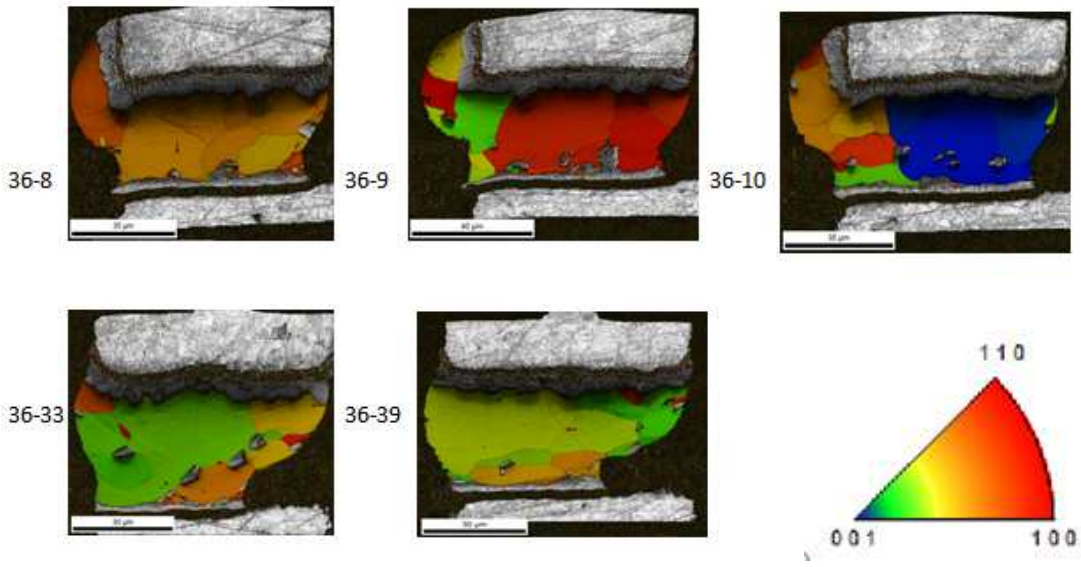

Figure 29: SP2 maps for selected solder bumps in sample 36.

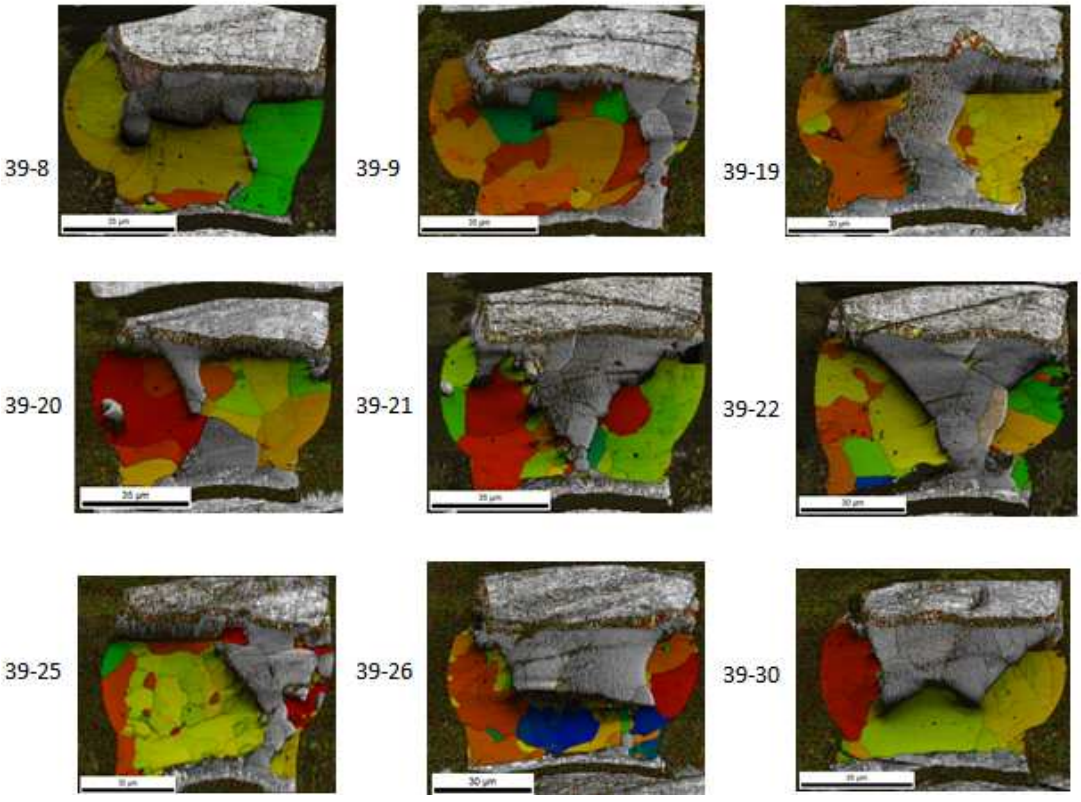

Figure 30: SP2 maps for selected solder bumps in sample 39.

In addition, EBSD data was collected for representative solders to show the HCP crystal orientation for the IMC layers as seen below in Figure 31.

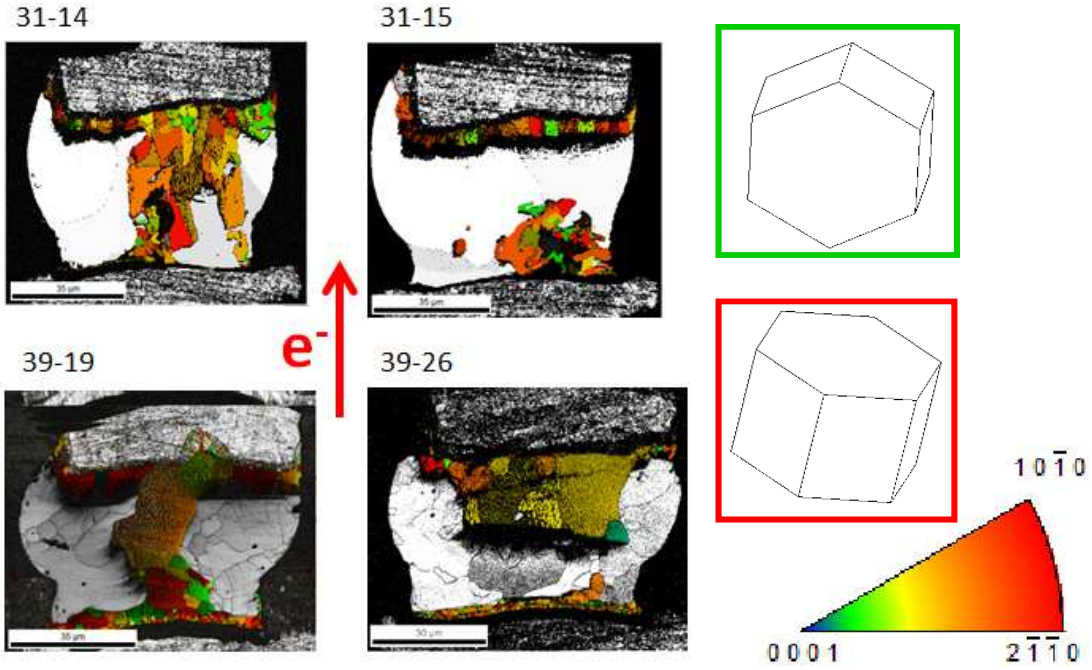

Figure 31: Representative solders showing HCP crystal orientation w.r.t. basal plane [0001]. Most IMC grains have their closed packed basal planes perpendicular to electron flow direction.

Key observations from the EBSD results are highlighted below:

- IMC rich regions are observed on both die (cathode) and package (anode) sides. Since IMC is expected to form on the cathode side, it is most possible that the IMC's noted in the package/anode side are the extension of the IMC formed in die side away from plain of view.
- All solders show IMC's neighboring grains with different orientations.

- There is no individual grain that has large amount of IMC's within it (e.g., no IMC region surrounded by same colored grain).
- Solders 31-15, 36-10, and 39-26 are the only solders with blue grains. i.e., only 3 out of 23 solders studied exhibit blue grain.
- In solder 39-26, the blue region is residing in the package (anode) side, showing major IMC on top (in the die/cathode side).
- The blue grain in solder 31-15 is in the die side, with IMC observed at the bottom in the Package side.
- Adjacent grains with similar orientations (low angle grain boundary) do not show any IMC at GB. (e.g., see solders 31-7, 31-10, 36-8, 36-39).
- The IMC grains show preferred orientation with the basal plane (closed packed plane of HCP structure) perpendicular to the electron flow (red oriented grains).

3.4 Discussion

Initial analysis of EBSD data presented in Figures 28-30, did not reveal definite correlation regarding a "preferred" orientation of an individual grain that promotes EM and IMC formation. However, significant IMC growth is clearly evident in between differently oriented grains, and grain misorientations appear to have an effect on the extent of IMC growth.

In an attempt to further investigate the grain orientation effect on IMC and to develop a relationship among the solder bumps, a single inverse pole figure was populated according to the corresponding grain orientations present on each bump. The detail of this effort and the results are presented in Appendix A.

One observation made was that grains orientated along the [001] (blue color) were not commonly seen in most of the solder bumps analyzed. Most of the colored grains ranged from green to red in the color spectrum. This effect may be associated with the complete consumption of the blue oriented grains. This hypothesis can be further validated through EBSD analysis of the EOL samples to investigate the statistics of the blue grains present compared to EM tested solders. Such study will not only test the grain consumption hypothesis, it may also shine a light on potential preferential grain growth (w.r.t. solder location within C4 array) occurring during solder solidification process under the presence of loading associated with CTE mismatch.

3.4.1 Effect of Crystal Packing on Electromigration

In this section, we have revisited the reported data on the effect of orientation on EM and have been able to explain the observed behavior noted on “single” crystal grained solders. As presented in Section 2.3.3.4, blue/green grains with c-axis parallel to electron flow direction exhibit a high IMC growth; while the red grains with c-axis perpendicular to the current flow has the lowest IMC growth and EM. Table 2 presented below includes our planar density calculations associated with different IMC growth fronts. The planar density is generally calculated by determining the fraction of total crystallographic area that is occupied by atoms. For these calculations, the plane of interest should be positioned so as to pass though the atoms centers [23]. Based on the planar density data reported in this table, one expects that grains oriented along [001] to have more evidence of electromigration since the plane density is lowest and therefore more interstitial locations are free for diffusion and ion displacement. This finding is in

line with the observation reported by Kinney et al. [21], and recommended for consideration in developing physics-based EM model and grain orientation effect.

Table 2: Correlation of plane orientation with color designation used in inverse pole figures, planar density and expected electromigration effect.

Orientation	**Color**	**Planar Density (atoms/nm^2)**	**Electromigration**
(001)	Blue	2.9	High
(011) and (101)	Green	5.2	Med-High
(110)	Red	7.6	Low
(100) and (010)	Red	9.7	Low

3.4.2 Effect of IMC Formation and Grain Misorientation on Electromigration

The information presented in Section 2.3.3.3 revealed the importance of grain boundary on electromigration. In this section, the effect of misorientation angle between the two adjacent grains on the extent of IMC growth is quantified. Table 3 reports the misorientation angle data between two corresponding adjacent grains (see Appendix B). The misorientation angles for the adjacent grains in each solder bump were measured individually as shown on the Figure 32 below. The misorientation angles ranging from 20° to 53° for samples were noted for solders showing IMC growth. For solders in sample 36, minimal IMC growth was observed and the values for misorientation angles were obtained between two adjacent grains with no IMC growth for comparison.

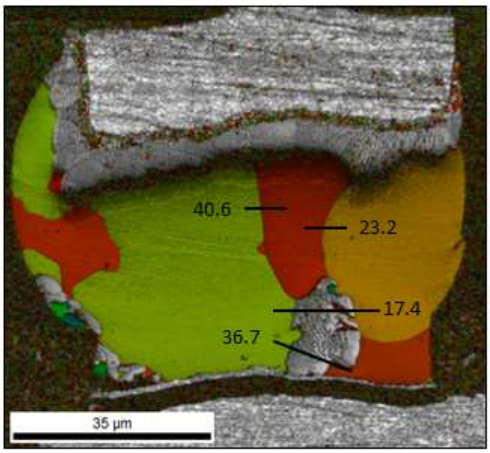

Figure 32: Misorientation angles measured between different grains in solder 31-2.

From the elemental maps, the amount of Sn and IMC was measured using OIM software. The percent of IMC layer (IMC%) was then calculated and tabulated in Table 4 (see Appendix B). The IMC formation of interest is the one growing within the solder bulk material and not necessarily at the Sn and Cu interface. To distinguish this, the IMC layer at the Cu and Sn interface of sample 31-7 was subtracted from the other solder IMC% calculations. We used sample 31-7 since this bump had little to no IMC present in the bulk of the solder. Most of the solders have a uniform IMC layer at the interface. A plot of misorientation angle vs. IMC% is shown in Figure 33.

The approach presented in this section was our attempt in testing our hypothesis that an increase in misorientation angle provides a more open site for ion migration during EM testing, hence, more IMC growth in high-angle grain boundaries compared to low-angle grain boundaries. The data personated in Figure 33 clearly shows most IMC formation occurring for large misorientation angles ranging from 20° to 53°, validating our hypothesis. The scatter observed in Figure 33 could be attributed by the grain

orientation in addition to the misorientation angle. For example even if the misorientation angle is low between two grains but one of the grains is oriented along the c-axis, IMC formation could grow at a faster rate since this is parallel to the electron flow. Further testing should be done to verify this statement.

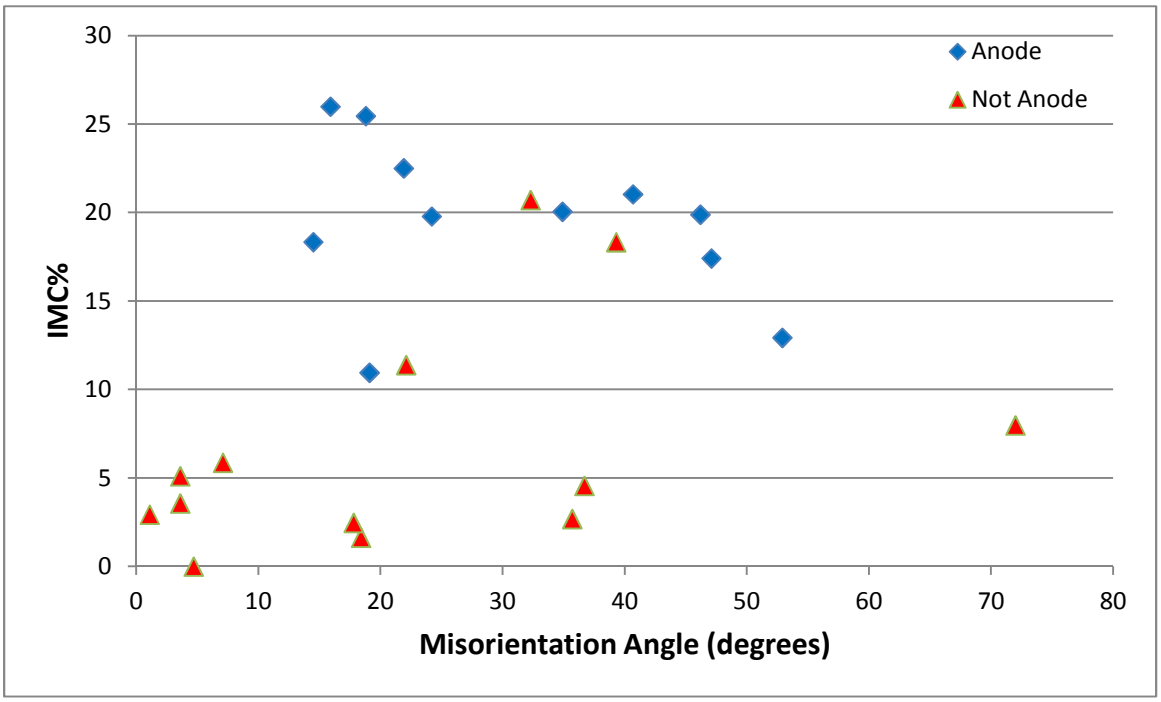

Figure 33: Graph showing the extent of IMC growth versus grain boundary misorientation angle. It should be noted that data points were distinguished between misorientation angles for grains between IMC formed at the anode and IMC formed away from the anode referred as “not anode.”

It is also important to note that the majority of the IMC growth evolved from grain boundaries. Grain boundary diffusion effect is believed to dominate the EM process and ion migration. In general, a large misorientation angle between grains will promote diffusion along a grain boundary. As seen in Figure 34, the rate of diffusion along the

grain boundary increases with increasing misorientation angle, θ, and reaches a maximum at θ=45° [24]. Therefore, IMC layers diffuse and grow faster along the grain boundaries.

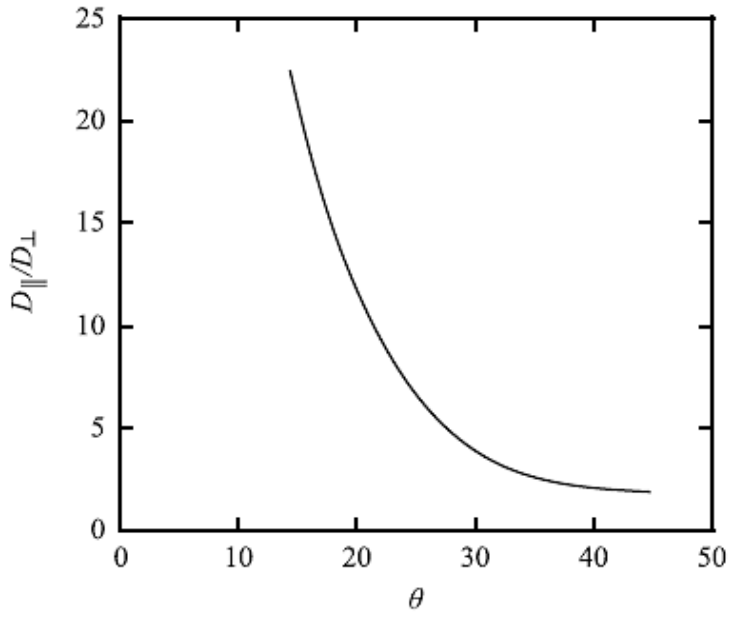

Figure 34: Effect of grain boundary misorientation angle on the diffusion of atoms along grain boundaries [24].

Diffusivity values were obtained from various studies to better understand the effect of grain boundary diffusion. Table 3 compiles the data obtained from each different study. Dyson et al. [25] and Kinney et al. [21] reported a ratio of diffusivities between the diffusivity along the c-axis and the diffusivity perpendicular to the c-axis. These values ranged from 65-500. These diffusivities correspond to lattice diffusion since the solders used were primarily single crystal and IMC growth was observed within the grain. On the other hand, the study from Li and Basaran [26] showed a ratio between the grain boundary diffusivity and lattice diffusivity which resulted in 10^6. This study

demonstrated that GB diffusion is about three orders of magnitude higher than lattice diffusion. Therefore when multi-grained solder is present, GB diffusion will be the dominant mechanism for EM which could explain why we are not seeing a clear grain orientation effect as the one observed in Kinney et al. study.

Table 3: Diffusivity ratios from literature comparing lattice and grain boundary diffusivities.

Study	$D_{lattice}$	D_{gb}
Dyson et al. [26]	$\frac{D_{\parallel c}}{D_{\perp c}} = 500$	-
Kinney et al. [21]	$\frac{D_{\parallel c}}{D_{\perp c}} = 65$	-
Li and Basaran [27]	-	$\frac{D_{gb}}{D_l} > 10^6$

4. Conclusion and Summary

Electromigration has proven to be a critical reliability issue especially in Pb-free solders joints. This mechanism causes void and hillock formation as well as intermetallic compound layers throughout the solder joint. The major factor influencing EM is the high current densities the solder bumps are exposed to due to miniaturization of the electronic devices. Factors such as the solder composition and grain structure of the solder are also influencing EM. Since the current and the temperature was approximately the same for all three samples, those factors are negligible to understand the effect of EM between the samples. From the data collected from this study, no direct correlation with the grain orientation and the amount of EM was observed at the solder bump. Grain orientations

varied from the entire color spectrum including green, yellow, orange and red. One orientation which was visibly not present on most solder bumps was the blue oriented grain (c-axis parallel to e- flow). The lack of such grain orientation might be because of complete grain consumption during EM. Further testing is recommended to prove this hypothesis.

The amount of IMC was measured for each the solders. Some of the IMC layers consumed more than 40% of the solder bump such as solder bumps 31-25 and 39-22. The misorientation angles measured between the grains adjacent to the IMC layer were relative large angles ranging from 20° to 53°. In addition, a grain boundary effect was observed. Diffusion of IMC layer along the grain boundaries was seen on most samples. Large misorientation angles between grains allow for faster diffusion rates. Work previously done by Chris Kinney et al. [21] suggested that IMC formation had a preferential orientation referred as the "green" orientation in which Sn c-axis is oriented almost parallel to the electron flow. One major difference between Chris Kinney et al. [21] study and this is that their samples were idealized neglecting thermal effects. Samples on this study were exposed to different thermal conditions and were also surrounded by non-metallic materials (e.g. polymers) which are commonly seen in microelectronic packages. In addition, samples used in Kinney et al. study were primarily single crystal. Most of the samples from our study have multiple grains present. Therefore as seen in Table 3, grain boundary diffusion becomes more dominant in multi-grained samples than lattice diffusion. Furthermore, a relationship between the amount of IMC and the misorientation angle between the grains surrounding the IMC layer was observed (see Figures 33 and

34). Higher misorientation angles allow for more IMC growth due to more open sites for ion migration during EM testing than lower misorientation angles.

Even though no clear correlation was obtained between the grain orientations on the effect of EM, it is known the anisotropic properties of Sn due to its body center tetragonal crystal lattice. Therefore, it should be noted that further analysis should be conducted to fully understand the influence of grain orientation and grain boundary misorientation angles of real life solder applications in non-ideal testing parameters to consider the thermal and mechanical effects on EM.

5. FUTURE WORK

It is recommended to perform serial sectioning of solder arrays with EBSD analysis to further characterize the 3D IMC distribution. This will allow to investigate IMC depth and the misorientation angles involved throughout the solder volume. X-ray tomography is also an alternative method but this technique is limited to show only the IMC extent though the volume and no grain orientation or misorientation angles will be determined.

In addition, EBSD analysis of the EOL is recommended to get statistics on the number of “blue” grains in untested conditions. This will provide information on whether the blue grains are consumed during the EM testing, and/or, if the grain orientation is influenced by processing.

Re-evaluated the EBSD analyzed solders to investigate the IMC grain orientations, and explore if preferred orientation is present. These additional testing and

analysis will provide more insight to fully understand the effect of grain orientation on EM.

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APPENDIX A
STEREOGRAGHIC PROJECTIONS

The following figures (see Figures 35-37) show such SP2 constructed for each solder bump analyzed. Different shapes were used to differentiate grains that were neighboring IMC layers and large and small grains within the solder bump. A legend is shown in Figure 32 describing the significance of these shapes.

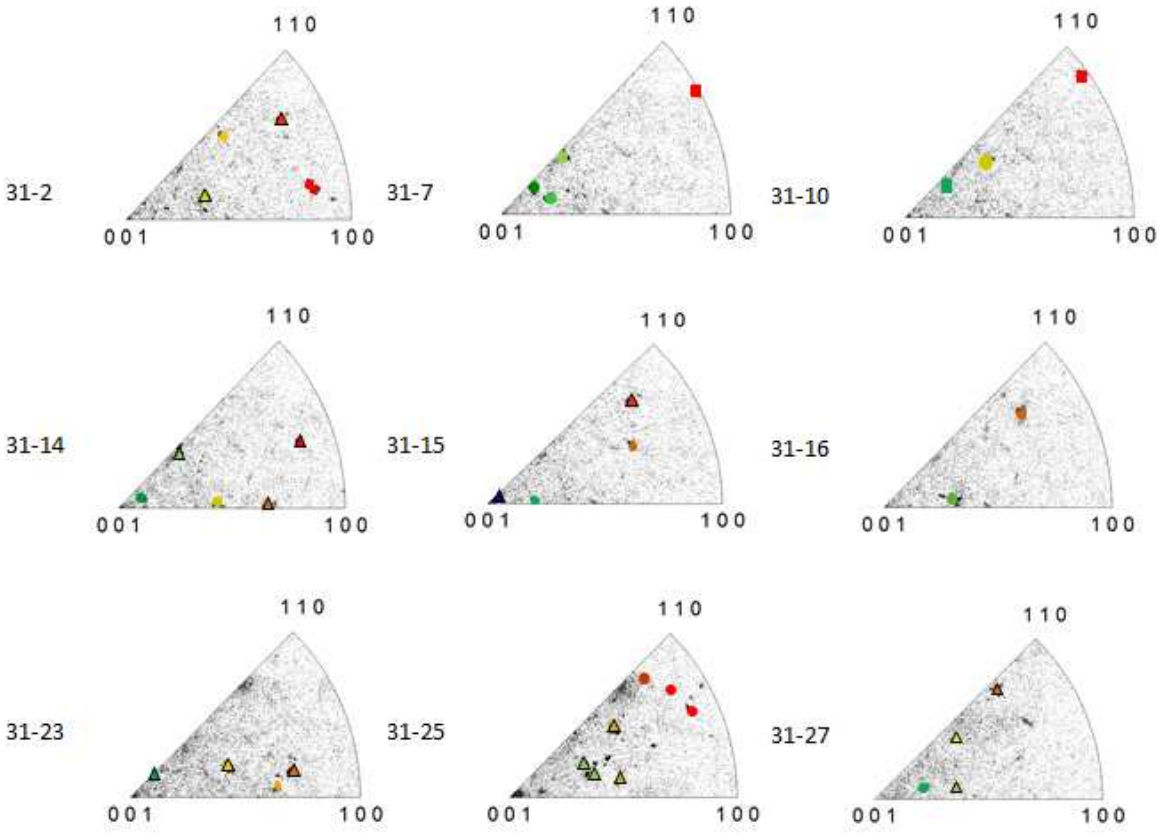

Figure 35: Inverse pole figures for selected solder bumps in sample #31.

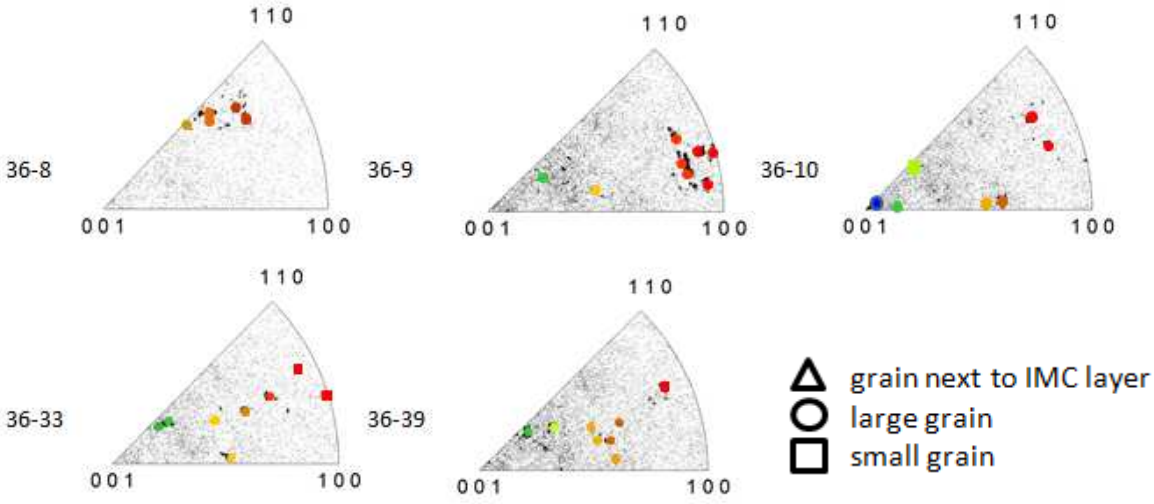

Figure 36: Inverse pole figures for selected solder bumps in sample #36.

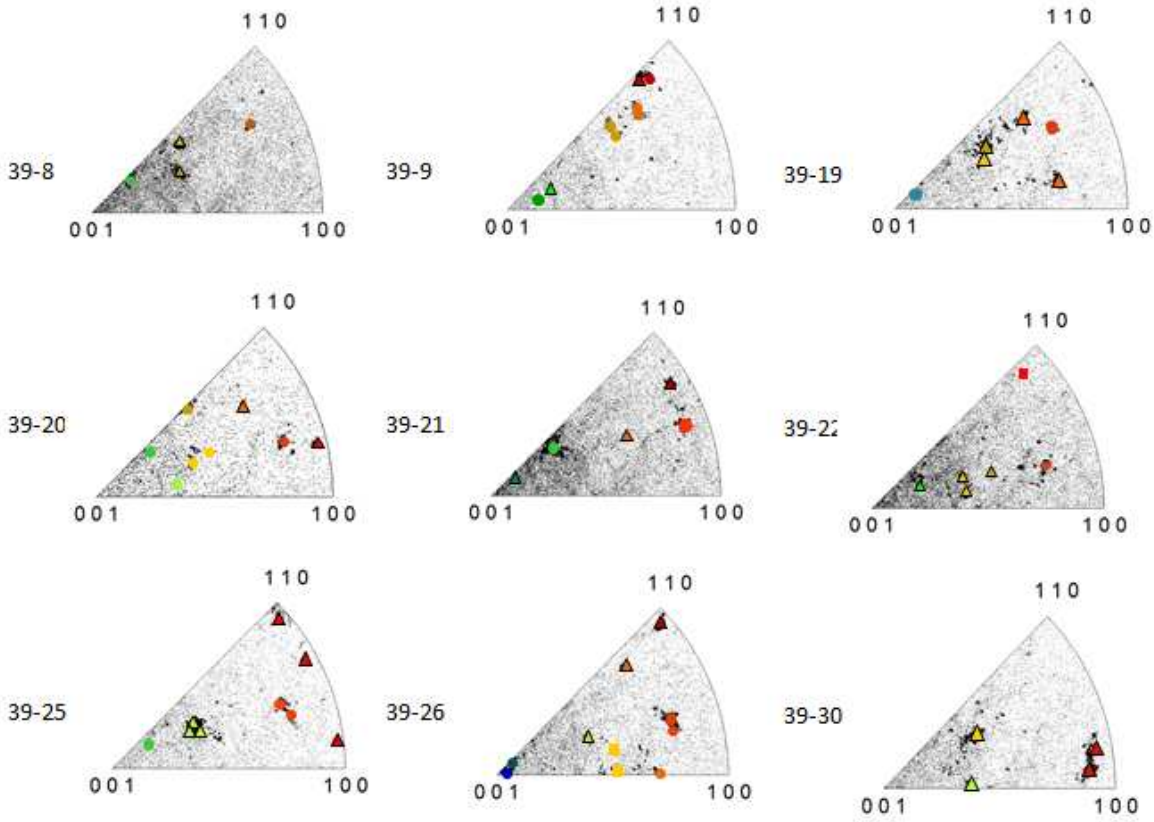

Figure 37: Inverse pole figures for selected solder bumps in sample #31.

The grain orientations neighboring the IMC layer identified in Figure 35 and 37 were compiled on Figure 38 for samples 31 and 39. Sample 36 was not considered since no significant IMC formation was observed. From the figure below, no clear orientation was apparent. There is high concentration of green to red orientations. The green orientation is the closest orientation parallel to the e- flow while the red orientation is perpendicular to the e-flow. From Kinney et al. study, EM was more prevalent for "green" grains which are the next closest to be parallel to the electron flow. In our study, the distribution of grains neighboring IMC varied among most orientations. From the samples analyzed, only one sample with the blue grain orientation was observed neighboring IMC layers.

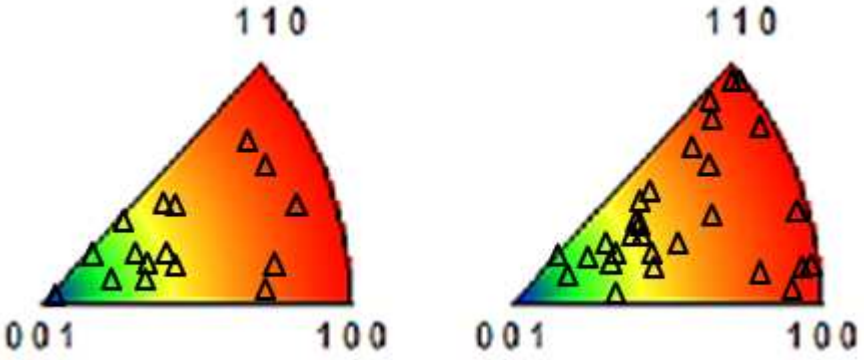

Figure 38: EM orientations compiled for Sample 31 (left side) and Sample 39 (right side).

APPENDIX B
IMC% & MISORIENTATION ANGLE DATA

Table 4: This table shows the misorientation angles measured as shown in Figure 31. Angles in BOLD and *italicized* correspond to the misorientation angles between grains with no IMC formation for those solders with little or no EM effect. The top row shows the color of the grains from which the misorientation angle was measured.

Solder ID	Angle	Angle	Angle	Angle	Angle	Angle	Angle	Angle	Angle	Angle	Angle	Angle	Angle	Angle
31-2				36.7		24.8								
31-7										***4.7***				
31-10											***1.1***			
31-14				21.7	41.7									
31-15		72.0												
31-16												***0.6***		
31-23						32.4	21.9							
31-25					38.1	18.8								
31-27				32.3			23.8							
36-8							***7.1***							
36-9													***3.6***	
36-10														***3.6***
36-33						***18.4***								
36-39					***17.8***									
39-8						19.1								
39-9					52.9			37.3						
39-19			39.3				14.5							
39-20							22.1	31.6			2.1	5.9		
39-21				18.8	46.2					1.0				
39-22						15.4								
39-25					46.4						2.7			
39-26							24.2							
39-30						8.2		34.9						

Table 5: IMC % calculations w. r.t to the amount of Sn and IMC disregarding the IMC formation at the Cu and Sn interface.

Solder ID	Sn	IMC	IMC%
31-2	0.59	0.19	4.56
31-7	0.57	0.16	0.00
31-10	0.56	0.18	2.94
31-14	0.48	0.29	21.03
31-15	0.54	0.21	7.98
31-16	0.58	0.18	2.69
31-23	0.49	0.30	22.50
31-25	0.49	0.33	25.46
31-27	0.58	0.31	20.71
36-8	0.51	0.19	5.87
36-9	0.54	0.19	5.11
36-10	0.54	0.18	3.57
36-33	0.54	0.17	1.63
36-39	0.55	0.17	2.47
39-8	0.57	0.23	10.95
39-9	0.53	0.24	12.93
39-19	0.53	0.28	18.34
39-20	0.54	0.23	11.39
39-21	0.55	0.30	19.88
39-22	0.50	0.34	25.99
39-25	0.61	0.29	17.41
39-26	0.52	0.29	19.79
39-30	0.57	0.30	20.06