A Fast Settling Oversampled Digital Sliding-Mode Controller for DC-DC Buck Converters

by

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ABSTRACT

Sliding-Mode Control (SMC) has several benefits over traditional Proportional-Integral-Differential (PID) control in terms of fast transient response, robustness to parameter and component variations, and low sensitivity to loop disturbances. An All-Digital Sliding-Mode (ADSM) controlled DC-DC converter, utilizing single-bit oversampled frequency domain digitizers is proposed. In the proposed approach, feedback and reference digitizing Analog-to-Digital Converters (ADC) are based on a single-bit, first order Sigma-Delta frequency to digital converter, running at 32MHz over-sampling rate. The ADSM regulator achieves 1% settling time in less than 5uSec for a load variation of 600mA. The sliding-mode controller utilizes a high-bandwidth hysteretic differentiator and an integrator to perform the sliding control law in digital domain. The proposed approach overcomes the steady state error (or DC offset), and limits the switching frequency range, which are the two common problems associated with sliding-mode controllers. The IC is designed and fabricated on a 0.35um CMOS process occupying an active area of 2.72mm-squared. Measured peak efficiency is 83%.

To my parents.

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Chapter 1

INTRODUCTION

1.1 Motivation

Power supplies play a major role in electronic systems. Both for portable devices such as mobile phones and tablets, as well as complex machines such as mainframe computers, satellites and communication systems, there is always need for regulated and robust DC supply sources (Fig. 1). The input to these power supplies known as Power Managements Circuits could be batteries (one-time use, or chargeable) or AC sources from the wall. The tasks of the power management circuits are to regulate the input source and also provide different DC levels. A simple mobile phone for example may need to have regulated 3V and 28V form its charged battery, which varies from 5V (when full) to 4V (when needs recharge) and would require a Low Drop-Out (LDO) linear regulator and a Boost switching regulator.

There are different categories of power supplies based on their operations: Linear regulators, Switching-Mode regulators. The linear regulators like Low Dropout regulators (LDO) utilize big transistors (MOSFET) in their active region. These types of regulators are less noisy, but their efficiencies are low. The switching-mode regulators utilize big transistors as switches. As opposed to the other type of regulators, these ones have higher noises and at the same time provide higher efficiencies.

Switching-mode supplies come in many forms such as switched-capacitor regulators and pulse-width-modulation regulators. The former utilizes capacitors as

storage elements and filters, and the latter takes advantage of both capacitors and inductors as storage elements and filters.

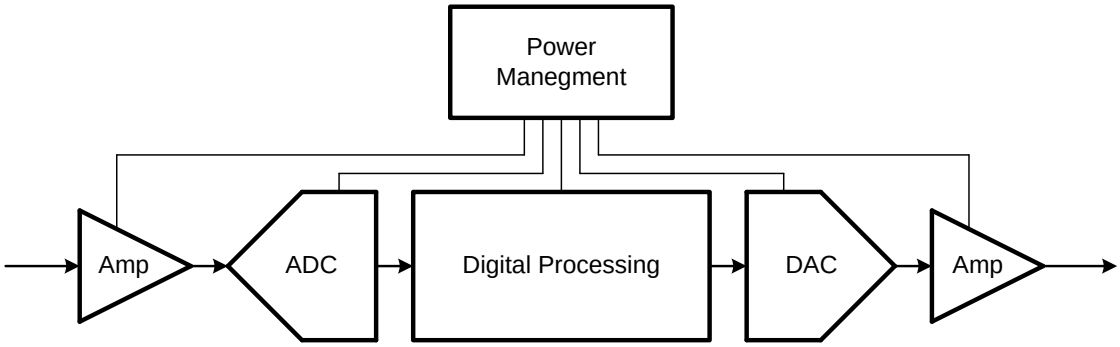


Fig. 1: Importance of power management in a typical signal chain of a modern electronic system.

If the output voltage of the power supply is bigger than the input voltage, the supply is referred to as Boost Converter (step-up); and if the output voltage is smaller than the input voltage, it is called Buck Converter (step-down) which is the type of regulators designed in this research.

Step-down or buck regulators are an essential part of low voltage battery operated electronic systems. The voltage conversion from the primary power source can be performed in more than one stage for better efficiency. Whether a single step-down converter is used or a multiple stages of step-down converters are implemented, the last stage must be able to reject the variations of the line and load due to fast transients in the state of the art processors.

Since most commercially available buck converters are designed in analog domain, they are very sensitive to environment and components variations. Replacing the

analog building blocks with their mixed-mode and digital counterparts makes switching regulators more robust to component variations and interest in digitally controlled switching converters have been increasing [1]-[15].

Fig. 2 shows the basic structure of an all-digital controlled DC-DC buck converter. The error voltage between the scaled output voltage and a reference voltage is digitized by an analog-to-digital (ADC) converter. The digitized error undergoes a specific compensation scheme, and the duty cycle control word is used to control the power train by a digital pulse width modulator (DPWM).

Minimizing analog complexity associated with digitization of the output and reference voltages is a challenging design problem in low-power digitally controlled DC-DC converters [1]-[3]. Another challenge associated with digitally controlled DC-DC converters is the need for a digitally controlled PWM generator (DPWM) block, which is needed to create the duty cycle control command for the power train.

DPWM is essentially a digital to duty-cycle converter, similar to a digital-to-analog converter (DAC), and even if the output of DPWM is a digital look alike (ground to supply) waveform, it conveys the analog information in its duty cycle. Due to transformation of an analog signal to digital domain and then back to analog domain, a phenomenon known as "Limit Cycle Oscillations" can happen.

Limit cycle oscillation is not a trait seen particularly in power converters; it is a unique feature of non-linear systems [16]. In a phase plane (explained in Chapter 2), a limit cycle is defined as an isolated closed curve. The trajectory has to be both closed, indicating the periodic nature of the motion, and isolated, indicating the limiting nature of the cycle (with nearby trajectories converging or diverging from it). Not every closed

curve in phase portraits is a limit cycle. Fig. 3 shows different types of limit cycles [16]. In (a) all trajectories converge to (0,0) after sometime, whereas in case (b) and (c) a few of the trajectories move away from the origin.

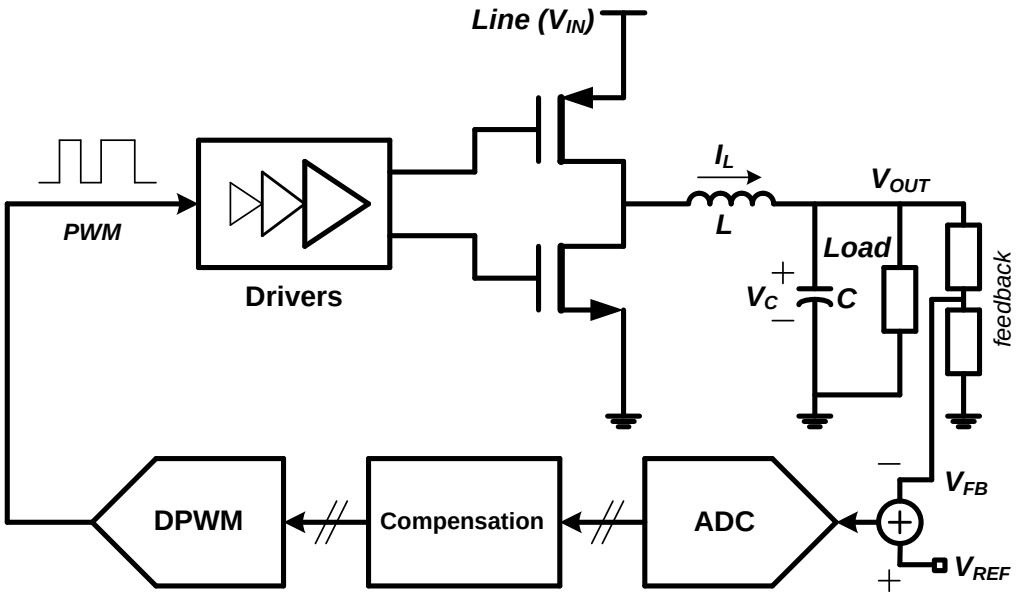


Fig. 2: An all digital DC-DC buck converter (step-down switching regulator).

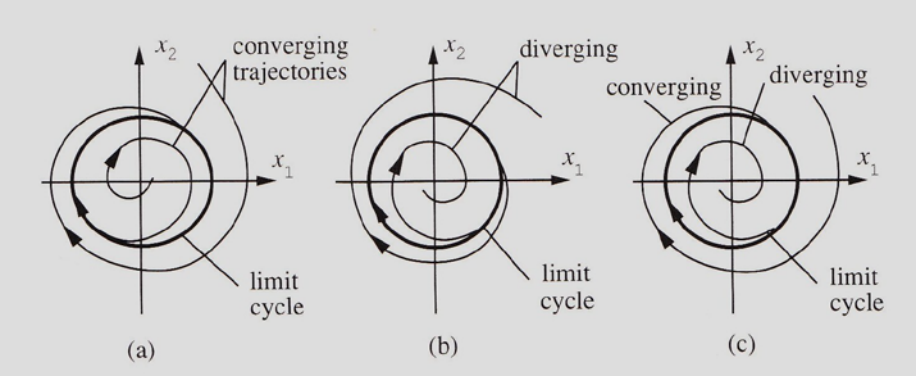


Fig. 3: Different limit cycles: (a) stable limit cycles, (b) unstable limit cycles, (c) semi-stable limit cycles.

In any digitally controlled system with a closed loop such as the buck converter in Fig. 2, if the following conditions are not met the limit cycle oscillations will occur, and the loop cannot settle to a zero error state:

1) resolution (DPWM) > resolution (ADC)

2) $0 < K_I \leq 1$

Where K_I represent the integrator coefficient, and implies that an integrator is needed in the feedback loop. In addition, the nonlinearity of the ADC and the DPWM blocks make the two conditions insufficient to eliminate limit cycle, and further attention is needed [12]. With the help of Fig. 4 it is easier to understand the relationship between the resolutions of the ADC and DPWM, along with the need for an integrator to eliminate the error.

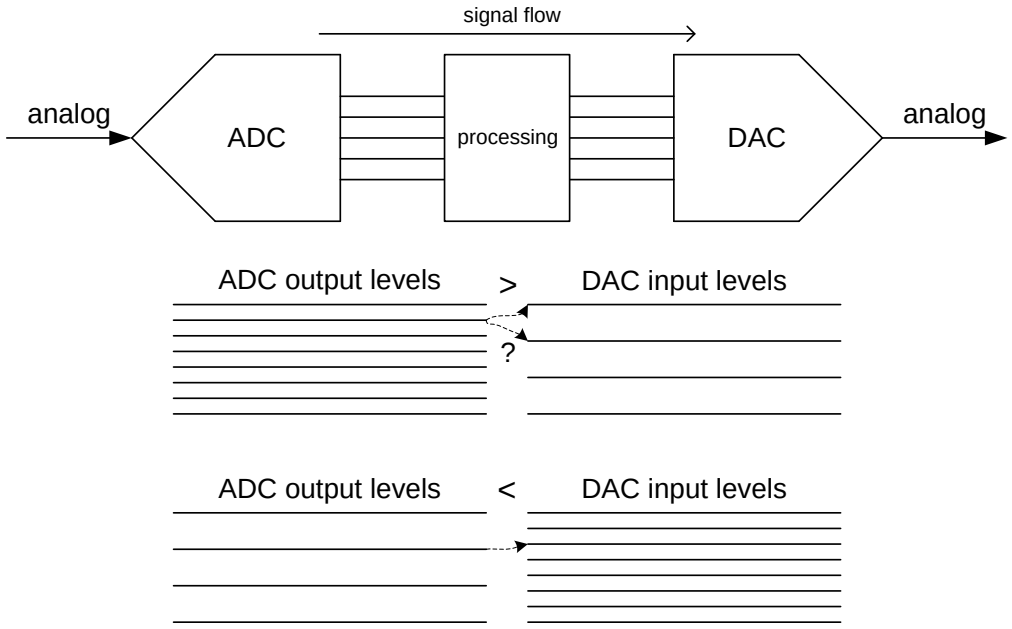


Fig. 4: Signal flow in the feedback of a digital closed-loop system, and the comparison of different choices for resolutions.

It can be easily seen that if the ADC has higher resolution, the closed-loop system may not be able to translate all the digital processed words into analog outputs, and the loop will not close, and toggle on a frequency lower than the switching frequency of the system (the DC-DC converter), which is not desirable. Conversely, if the DAC (or DPWM in a DC-DC converter) has at least one bit of resolution more than the ADC, the problem can be alleviated. Regardless of the other conditions needed to be met, this condition (*res.(ADC) < res.(DPWM)*) alone means that the higher dynamic range in the ADC (which in turn determines the accuracy or sensitivity of the control loop) requires even higher number of bits in DPWM, which means more power consumption and more complexity in the DPWM core.

The DPWM also causes delay and phase lag which is not desirable in feedback control systems. In order to eliminate the need for DPWM, prior approaches utilized sliding-mode-controller (SMC) or different forms of hysteretic controller.

The goals of this research are:

(1) To eliminate the sensitive analog blocks such as op-amps and comparators with their more robust mixed-signal block counterparts (to achieve such a goal, ADCs that utilize amplifiers and comparators in their architecture are being avoided).

(2) To replace the small signal or linear control approach with so called large signal and non-linear controls.

(3) To utilize controllers that generate the modulated pulses needed for control the power stage without the need for PWM (DPWM) block.

In the proposed approach shown in Fig. 5, a non-linear controller based on single-bit oversampling feedback ADCs and a digital sliding-mode controller is presented. The details of sliding-mode control and the controller itself are presented in the following chapters.

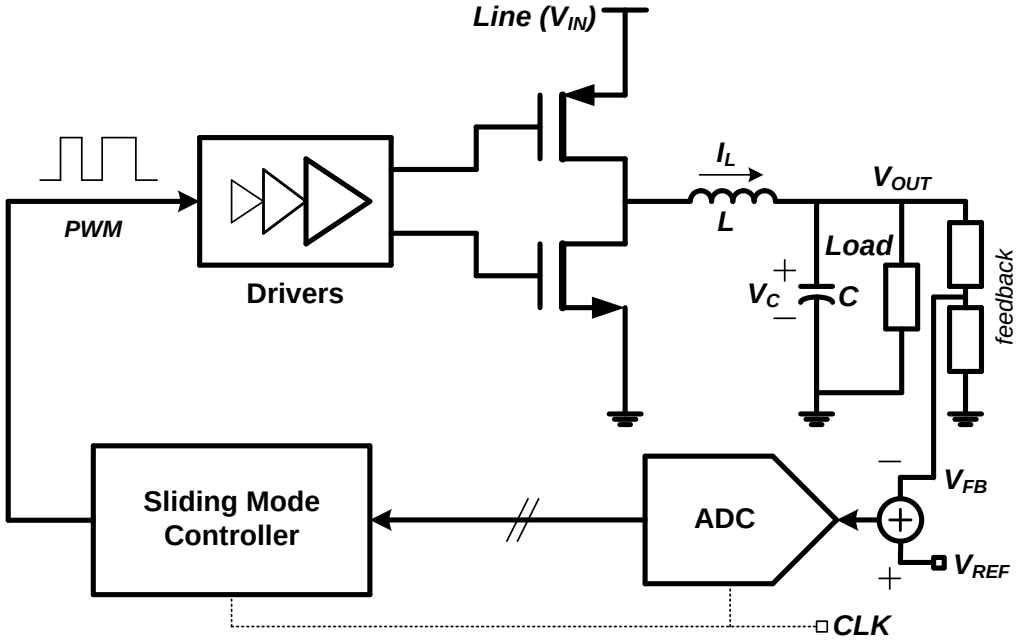


Fig. 5: The proposed oversampled, digital sliding mode control buck converter.

1.2 Thesis Organization

The rest of this dissertation is organized as follows. Chapter 2 covers the nonlinear control fundamentals, stability, phase portrait definition, analog sliding mode control theory, and prior art on Sliding Mode Control in DC-DC converters. The Proposed Digital Sliding Mode Controller and circuit level implementations are described

in Chapter 3. Measurement and experimental results are presented in Chapter 4; and Chapter 5 closes with conclusions and future work.

Chapter 2

BACKGROUND

2.1 Nonlinear Control

Most practical systems are non-linear by nature, due to many different reasons. Linear controllers can be used to control these non-linear systems if the systems are linearizable (at least in the vicinity of an equilibrium point). This has been used extensively by engineers known as small-signal analysis or AC analysis. Non-linear controllers on the other hand are superior choices in many applications due to the following (but not limited to) reasons [16]:

(1) *Improvement of existing control systems:* Linear control methods rely on the key assumption of small range operation for the linear model to be valid. When the required operation range is large (like when the load changes from a light-load to a heavy-load in a buck converter), a linear controller is likely to perform very poorly or to be unstable, because the nonlinearities in the system cannot be properly compensated for.

(2) *Analysis of hard nonlinearities*: Another assumption of linear control is that the system model is indeed linearizable. However, in control systems there are many nonlinearities whose discontinuous natures do not allow linear approximation. For example the buck converters change their structures back and forth between 2 distinct sub-structures.

(3) *Dealing with model uncertainties*: In designing linear controllers, it is usually necessary to assume that the parameters of the system model are reasonably well known. However, many control problems involve uncertainties in the model parameters, such as inductor model used in design process for a buck converter.

(4) *Design simplicity*: Good nonlinear control designs may be simpler and more intuitive than their linear counterparts. This is exemplified when a non-linear controller is used in the design of a buck converter.

Most linear and non-linear control methods are originated from the work of Lyapunov [16]. In 1892 Alexander Mikhailovich Lyapunov a Russian mathematician published: *The General Problem of Motion Stability.*

Basic Lyapunov theory comprises two methods introduced by him: the Indirect Method and the Direct Method.

The Indirect Method (Linearization Method) states that the stability properties of a nonlinear system in the close vicinity of an equilibrium point are essentially the same as those of its linearized approximation. Since most physical systems are inherently nonlinear, Lyapunov's linearization method serves as the fundamental justification of using linear control techniques in practice, i.e. shows that stable design by linear control guaranties stability of the original physical system locally (close to the linearization point).

The Direct Method is a powerful tool for nonlinear system analysis, and therefore the so-called Lyapunov Analysis often actually refers to the direct method. The direct

method is a generalization of the energy concepts associated with a mechanical system: the motion of a mechanical (or electrical) system is stable if its total mechanical energy decreases all the time.

In using the direct method to analyze the stability of a nonlinear system, the idea is to construct a scalar energy-like function (a Lyapunov function) for the system, and see whether it decreases. The power of this method comes from its generality: it is applicable to all kinds of control systems, for time-varying or time-invariant, finite dimensional or infinite dimensional. Unfortunately, the limitation of the method lies in the fact that it is often difficult to find a Lyapunov function for a given system.

Although Lyapunov's direct method is originally a method of stability analysis, it can be used for other problems in nonlinear control. One important application is the design of nonlinear controllers like the buck converters.

The basic philosophy of Lyapunov's direct method is the mathematical extension of a fundamental physical observation: if the total energy of a mechanical (or electrical) system is continuously dissipated, then the system, whether linear or nonlinear, must eventually settle down to an equilibrium point. Therefore, we could conclude the stability of a system by examining the variation of a single scalar function.

2.2 Stability

The concept of stability is almost always associated with the Bode gain and Bode phase plots. This method which is a small-signal analysis, meaning that the circuit (linear or non-linear) is linearized around a point of interest known as equilibrium point which is stable, has been used extensively in electrical engineering and many other closed loop

systems as well. In order to understand the stability from Lyapunov direct method and relate that to sliding-mode, the following examples are quite useful and insightful.

A hanging pendulum (shown in Fig. 6) is a simple non-linear system by nature. Its motion and behavior can be analyzed by linearization around a small angle, meaning small-signal analysis. At the same time, the pendulum can be viewed and analyzed from its mechanical energy transformation. After a disturbance, the pendulum swings and its energy switch back and forth between kinetic energy and potential energy. Starting from an arbitrary initial angle [16], the pendulum will oscillate and progressively stop along the vertical. Its stability has very little to do with the eigenvalues of some linearized system matrix, and it comes from the fact that the total mechanical energy of the system is progressively dissipated by various friction forces (like: gravity, hinge, etc.), so the pendulum comes to rest at a position of minimal energy.

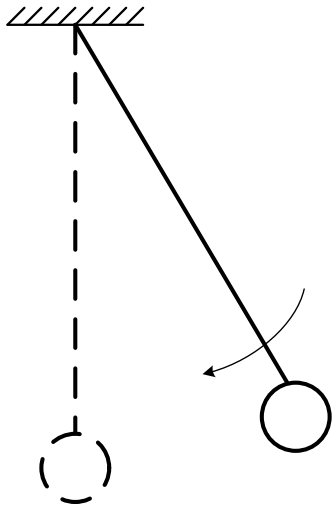


Fig. 6: Hanging pendulum, coming to rest (zero energy) due to gravity and other frictions.

Another good example to illustrate the point is the "warped table and marbles", shown in Fig. 7. Point "A" is not a stable point, since after mounting the marble on that

spot (not a simple task!), it takes very little energy for the marble to leave and never come back. Point "C" is a stable point, and the marble stays there for ever, unless it is forced to leave that spot. It should be noted that no matter how large or small a region around point "C" is being considered, the marble will stay put in its initial position "for ever". Point "B" on the other hand is of interest; since not only it is a stable point, it has interesting characteristics. For a [small] region around point "B", if the marble is disturbed, after some time it comes back to the final stable point of "B", or it comes back to its vicinity due to gravity. Considering the fact that there are a few initial conditions that the marble will run away and won't come back, for some initial conditions after "some time", the marble's position is within a region around point "B", if not at it point "B" exactly.

The last example helps with understating the definition of Exponential Stability and Asymptotic Stability, leading to Lyapunov Stability. From [16] we define:

The equilibrium state x=0 is said to be stable if, for any R>0, there exists r>0, such that if ||x(0)||<r, then ||x(t)||<R for all t>=0; otherwise, the equilibrium point is unstable. An equilibrium point 0 is asymptotically stable if it is stable, and if in addition there exists some r>0 such that ||x(0)||<r implies that x(t)→0 as t→infinity. An equilibrium point 0 is exponentially stable if there exist two strictly positive numbers α and λ such that $\forall t > 0, \|x(t)\| \le \alpha \|x(0)\| e^{-\lambda t}$ in some small ball B_r around the origin.

Lyapunov local stability: if, in a ball B_{Ro}, there exists a scalar function V(x) with continuous first partial derivatives such that; V(x) is positive definite (locally in B_{Ro}), V'(x) is negative semi-definite (locally in B_{Ro}), then the equilibrium point 0 is stable. If, actually the derivative V'(x) is locally negative definite in B_{Ro}, then the stability is asymptotic. Lyapunov global stability: assume that there exists a scalar function V of the

state x, with continuous first order derivative such that; V(x) is positive definite, V'(x) is negative definite, V(x)→infinity as ||x||→infinity, then the equilibrium at the origin is globally asymptotically stable.

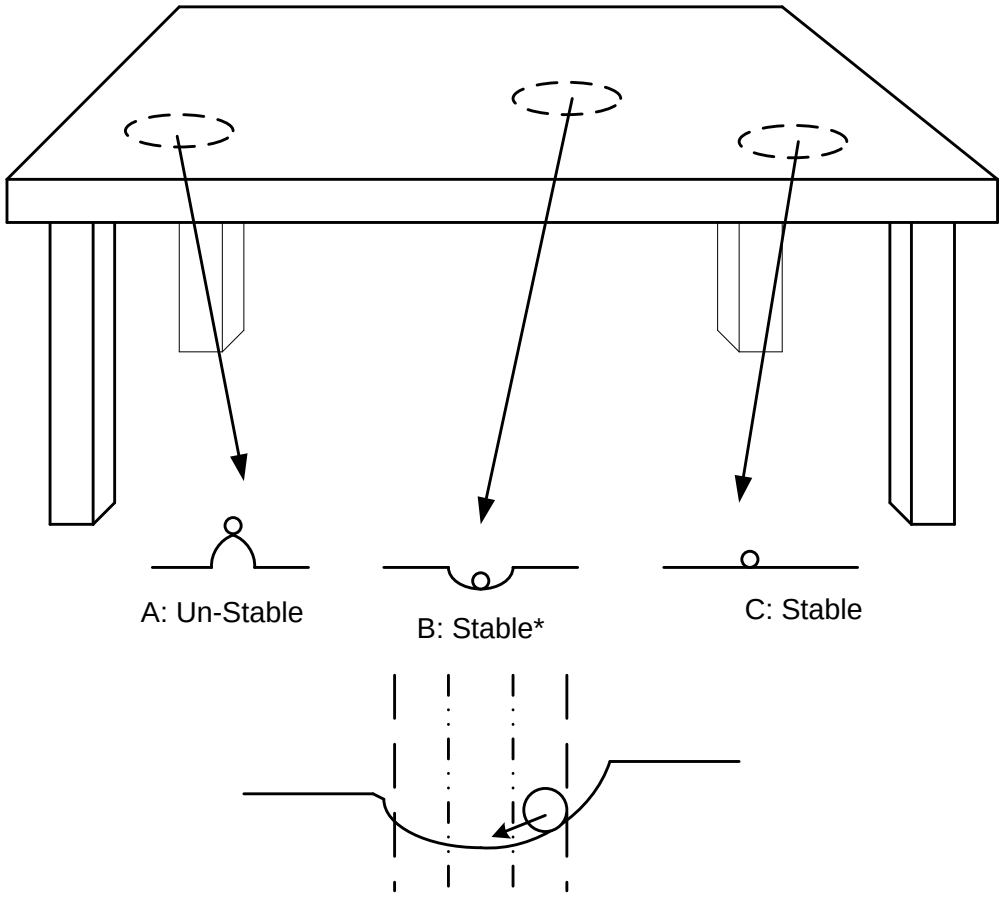


Fig. 7: Warped table and marbles, posing different examples for unstable points, stable-points and its various kinds.

2.3 Phase Portrait

A "state" of a circuit or system is defined as [17]: A set of data qualifies to be called the state of a network if it satisfies the following 2 conditions: (1) For any time, like t_1, the state at t_1 and the input waveforms (specified form time t_1 on) determine

uniquely the state at any time $t>t_1$. (2) The state at time t and the inputs at time t (and sometimes some of their derivatives) determine uniquely the value at time t of any network variable. The capacitor voltage and inductor currents are 2 examples of a state in a circuit; and the number of the states or order of a system depends on the number of storage elements like capacitors and inductors.

When the number of states goes up, the system is defined purely by vectors and it is presented with mathematical equations. On the other hand, for a second order system, like a DC-DC buck converter, the system and its behavior can be represented graphically as well as mathematically. When showed graphically, the result is referred to as Phase Portrait.

Fig. 8 shows the buck converter filter with the typical parasitics included and (1) represents its transfer function.

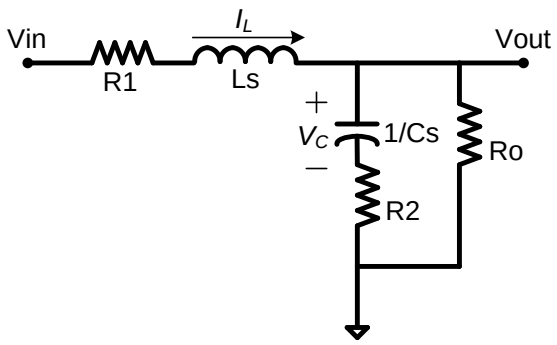


Fig. 8: Second order filter (buck converter), parasitics included.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{s\cdot\left(R_O R_2 C\right)+R_O}{R_O+R_1}}{s^2\cdot\left(\frac{R_O LC+R_2 LC}{R_O+R_1}\right)+s\cdot\left(\frac{L+R_O R_2 C+R_1 R_2 C+R_1 R_O C}{R_O+R_1}\right)+1}$$

where

$$\omega_O = \sqrt{\frac{R_O+R_1}{R_O LC+R_2 LC}}$$

$$Q = \frac{\sqrt{R_O LC+R_2 LC}\times\sqrt{R_O+R_1}}{L+R_O R_2 C+R_1 R_2 C+R_1 R_O C}$$

$$zero: \frac{-1}{R_2 C}$$

(1)

where Q represents the quality factor, ω_o the natural frequency, *R1* and *R2* represent series parasitic resistance of the inductor (DCR) and capacitor (ESR) respectively. *Ro*, *L* and *C* represent the output load and filter inductance and capacitance. Since most real components have parasitics like the ESR of the capacitor and the DCR of the inductor, the real and practical response of such a filter depends strongly not only on its components values, but also on the parasitics as well.

Shown earlier in Fig. 2, when the NMOS and PMOS switches of a buck converter turn off and on (in order to keep the output at a regulated state), the system representative point moves in the state-space. The following figures are presented as the natural paths the system (buck converter due to its filter) would take if it were given the chance.

Fig. 9 shows the state-space of the second order filter of a buck converter for the same capacitor value, with different ESR from 1mΩ to 100mΩ.

For same value of L=1.5uH, different capacitor values such as C=2.2uF and C=220uF (while keeping the DCR and ESR the same), show different response in the

state-space, shown in Fig. 10. This is very important when designing a non-linear controller like SMC, since the values of L and C play a big role in system time response and dynamics as well. Note that these plots are simulated in open loop format, and the circuit is forced to reach mid supply, 1.5V in these cases. Both simulations in Fig. 10 are stopped at the same exact time, after 500uSec. It can easily be seen that based on the Q of the system according to (1), system will respond differently for different values of filter elements.

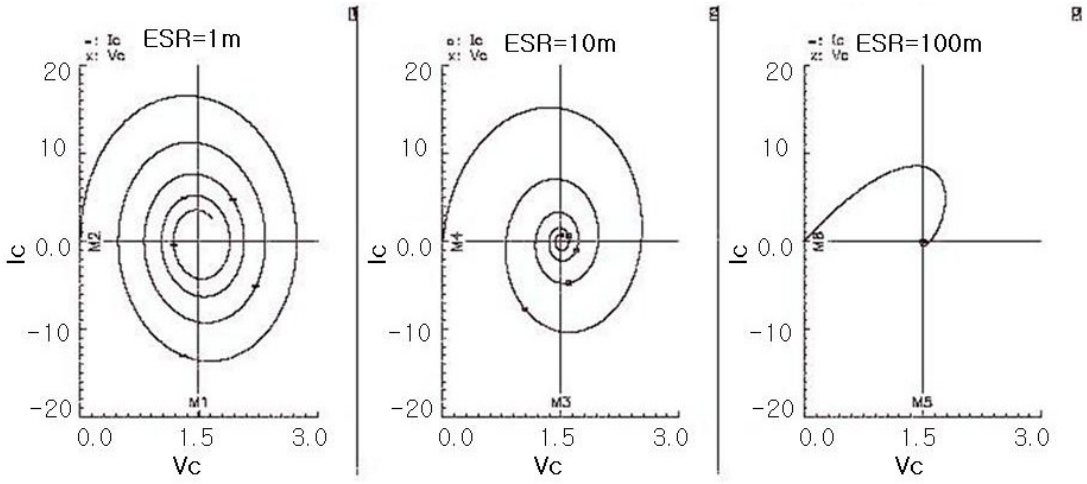
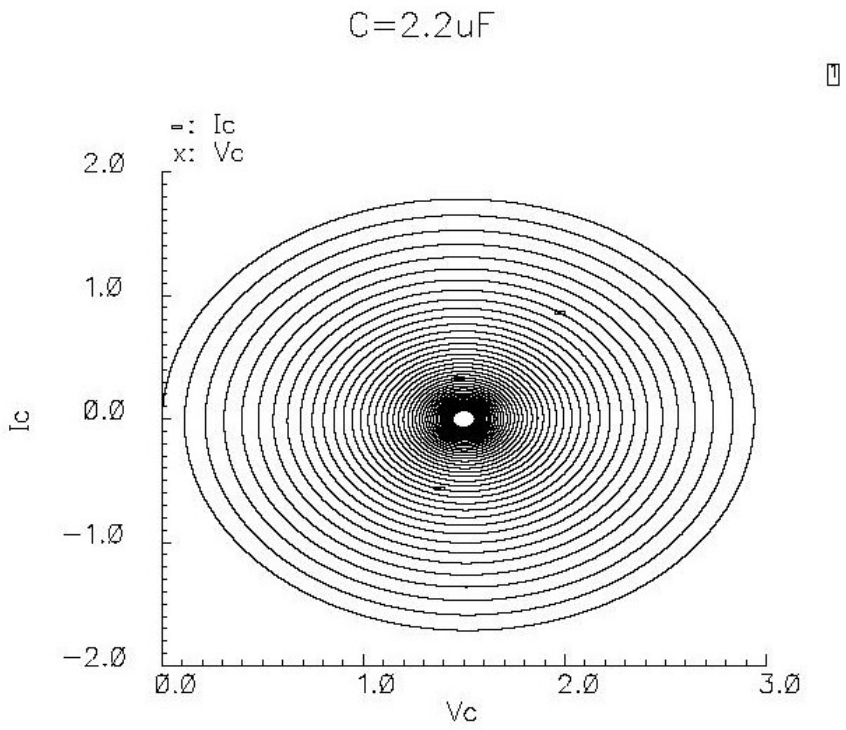


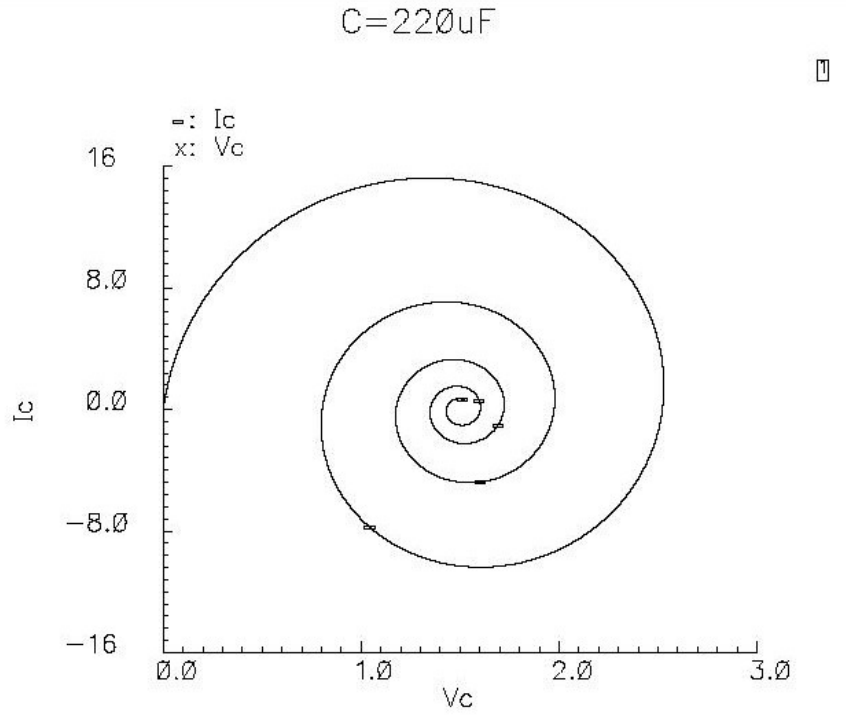
Fig. 9: Second order response in state-space, for various capacitors ESR, stop-time = 500uSec.

Fig. 11 shows the response for different initial conditions, and it also shows how the state-space for a second order buck converter is divided into 2 regions.

It has to be mentioned that in order to create the plots for the previous figures, first the circuit is run for a specific time (like 500uSec) and the states of interests like the capacitor voltage and current are being plotted vs. time, then the time is being eliminated. This way the state-space and its phase portraits are made.



(a) C=2.2uF



(b) C=220uF

Fig. 10: Second order response in state-space, for various capacitor values, stop-time = 500uSec.

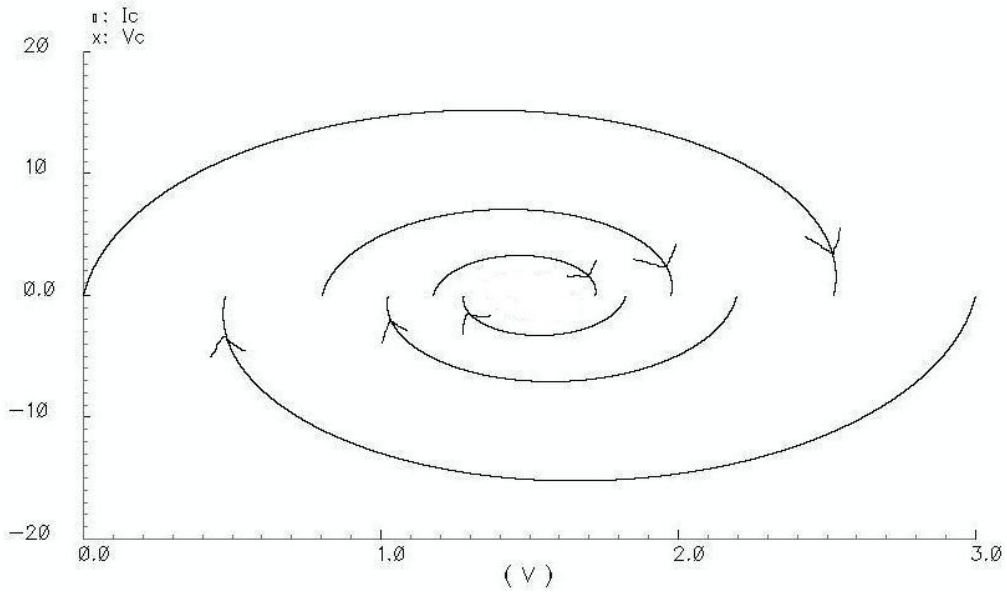


Fig. 11: Second order response for different initial conditions, division of state-space into 2 regions.

2.4 Analog Sliding Mode Theory

Most of the commercially available switching-mode power supplies (SMPS) are designed based on state-space averaging method [18], which essentially is a small-signal optimization method. Although this procedure works very well at steady state, it has a few shortcomings such as poor transient performance. For example when the load changes form a light-load to a heavy-load, the converter takes a long time to recover and bring the output voltage back to the desired value.

Switching regulators like DC-DC step-down converters are constantly changing from one structure to another structure due to the non-linear nature of the switches used in the design; thus they are classified as Variable Structure Systems (VSS), shown in Fig. 12.

Sliding-Mode-Controller (SMC) is a non-linear controller that is well suited for the variable structure systems and it is based on Lyapunov Direct Method. Therefore, it is a natural fit to utilize these controllers in switched-mode power supplies.

Fig. 12 shows the 2 distinct structures of a buck converter along with its trajectories in the state-space. Error-voltage (the reference voltage minus the capacitor voltage) and its derivative are chosen as the states of interests in this approach. In sliding-mode control (which is based on Lyapunov direct method and global stability), a surface (here a line S=0) is defined as the linear combination (not the only choice, perhaps an easy and more practical one) of the states and this surface (or line) divides the state-space into 2 regions.

When the NMOS switch is ON, the left side of the inductor is shorted to ground, and therefore the circuit's representative point or operating point travels from the top of the S=0 to its bottom. Once the PMOS switch is ON and the inductor is connected to V_{IN} or line, the reverse situation happens. By deriving a law that forces and controls the switches to turn ON and OFF in a way that when the operating point is pushed off from the zero error condition (the origin in Fig. 11), it comes back to it, the sliding-mode control is being formed.

The operation of the circuit is that after a disturbance or upon power-up it reaches the line (Reach Phase), and then it slides to the origin (Slide Phase) [20]. If a hysteresis band around the line S=0 is implemented (shown as dash lines in Fig. 12), the sliding-mode block creates the pulses necessary to control and operate the system and the PWM (or DPWM) block is no longer needed.

Since this type of control is not based on local linearization, the circuit behaves similarly for various conditions and it rejects the disturbances (line disturbance, load disturbance, etc.) significantly faster compared with a fixed-frequency small-signal based controller.

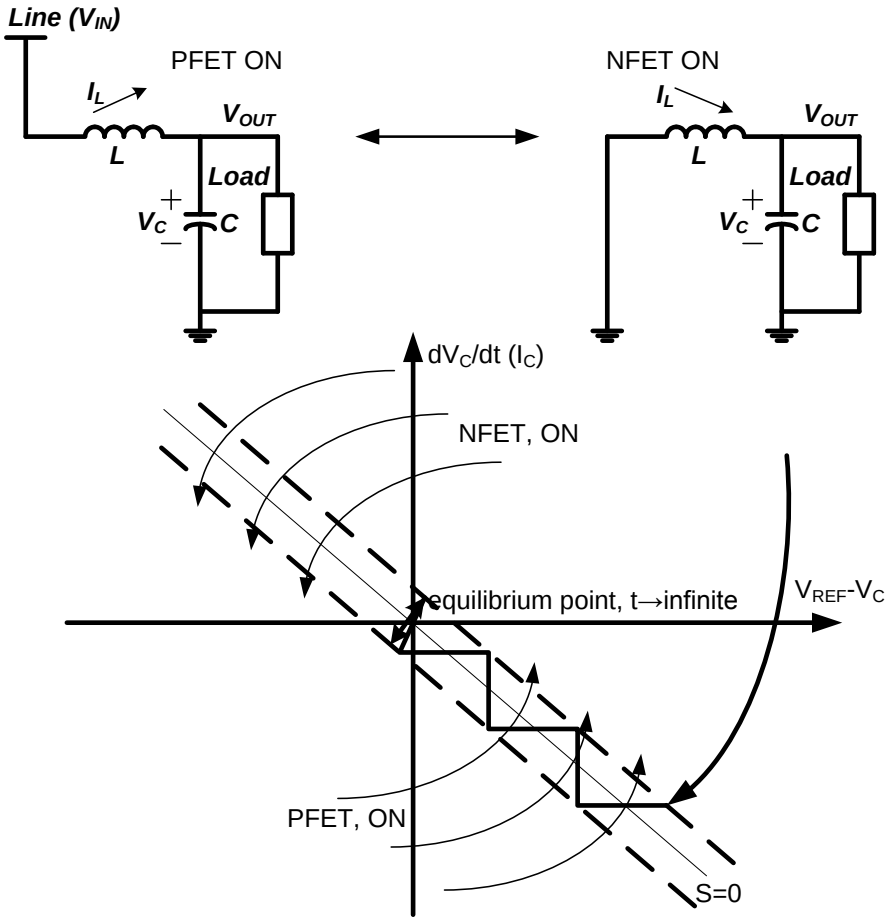


Fig. 12: Two distinct structural modes of a step-down buck converter, the L-C filter, the trajectories, and the sliding surface in the state-space.

Successful implementation of a sliding surface as a stabilizing reference path can be fully achieved by meeting three conditions [19]-[22].

(1) *The hitting condition*: whatever the initial conditions, the trajectories must reach the sliding surface.

(2) *The existence condition*: the trajectories are forced toward the sliding surface when they are close to it.

(3) *The stability condition*: the sliding surface will always direct the state trajectories toward a stable equilibrium point.

The analog sliding surface based on the error signal *e* is defined in (2) as:

$$e = V_{REF} - V_C$$

$$S_a = K_{1a} \cdot e + K_{2a} \cdot \left(\frac{dt}{d} e \right) = 0 \qquad (2)$$

where V_{REF} represent the reference voltage, V_C is the capacitor voltage, and *e* is the error voltage between the reference and capacitor voltage in analog domain. The coefficients K_{1a} and K_{2a} are the analog controller coefficient and *Sa* is the analog sliding law. Fig. 13 illustrates the implementation of the sliding mode controller in a buck converter. In order to meet the above conditions the controller needs to force the PWM signal to Vdd (or high) when S_a is positive, and force the PWM signal to zero (or low) when S_a is negative. Besides the following conditions needs to be satisfied per Lyapunov's requirement:

$$\lim_{for(S_a \to 0)} \left(S_a \cdot S_a{}' \right) < 0 \qquad (3)$$

2.5 Prior Art on Sliding Mode Control of DC-DC Converters

The proposed sliding-mode control is described in the next chapter, but a quick survey and review of the prior art are presented here. These works were chosen since they

introduced a digital implementation of sliding-mode control and bench test results were offered, and they were not based on theory and simulations.

In [13] feedback voltage is translated from voltage to frequency and compared with a reference frequency; and then SMC is implemented in frequency domain by reformulating the sliding control law. This method does not address the DC offset error associated with practical SMC; and therefore, the output voltage changes based on the output load current, shown in Fig. 14.

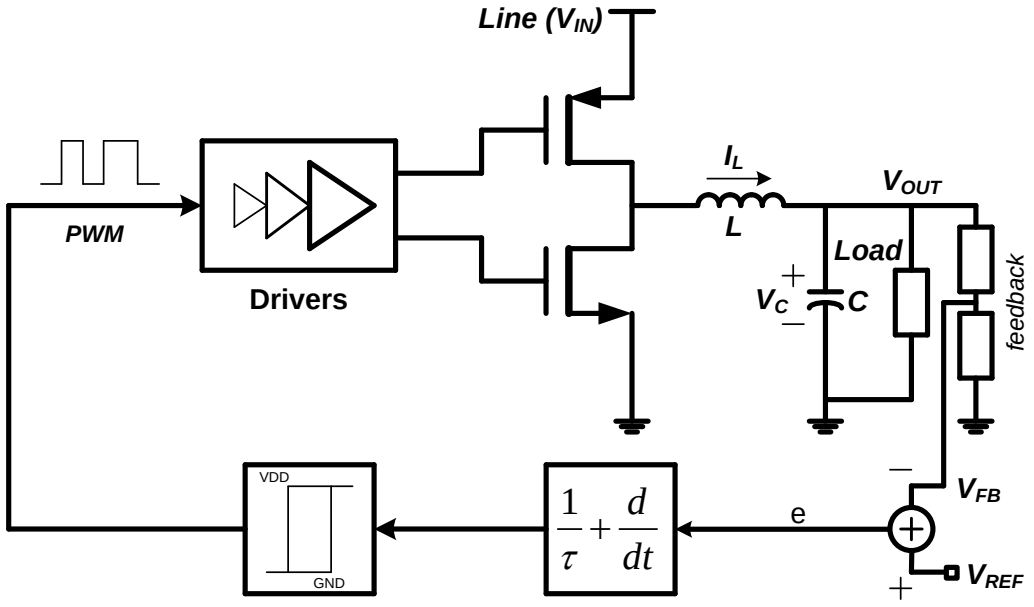


Fig. 13: Analog implementation of sliding-mode control in a step-down buck converter.

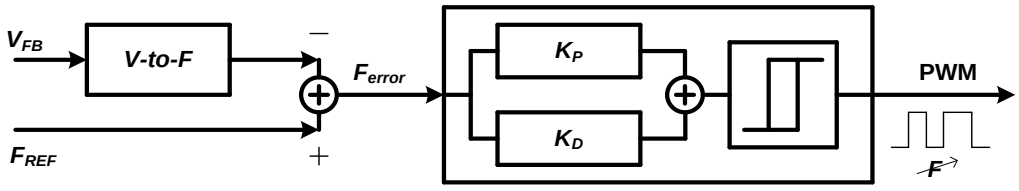


Fig. 14: Digital SMC with reformulation from voltage to frequency [13].

In [14] analog error voltage is sampled and a digital sliding-mode controller is used to adjust the duty cycle. This approach (Fig. 15) works on a fixed switching frequency. The fixed frequency approach slows down the transient response, and also creates tones and EMI similar to other fixed frequency converters. Since an integrator is used, there is no DC offset error.

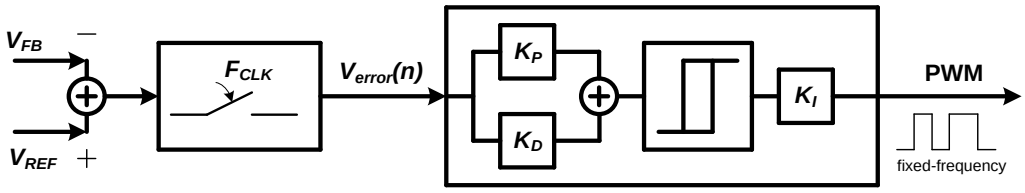


Fig. 15: Digital (discrete-time) SMC with fixed switching frequency [14].

In [15] a digital approach similar to [13] translates both feedback and reference voltages to frequency and reformulates the sliding control law. This approach includes an integrator so the DC offset error is absent. However, this approach has poor dynamics and shows large transients for a small load steps, presented in Fig. 16.

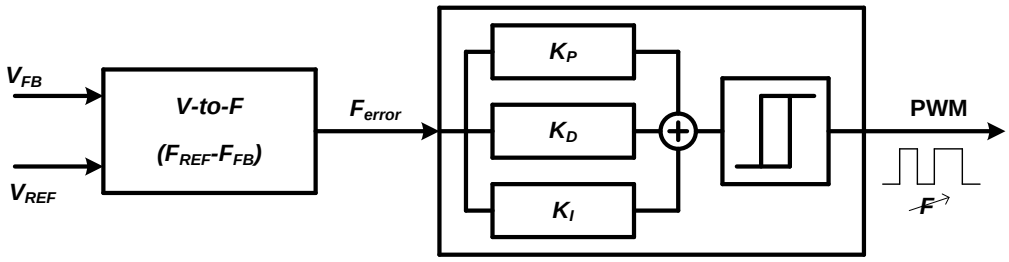


Fig. 16: Digital SMC with reformulation from voltage to frequency [15].

A simplified block diagram of the proposed controller is shown in Fig. 17 for comparison and the details are left for Chapter 3.

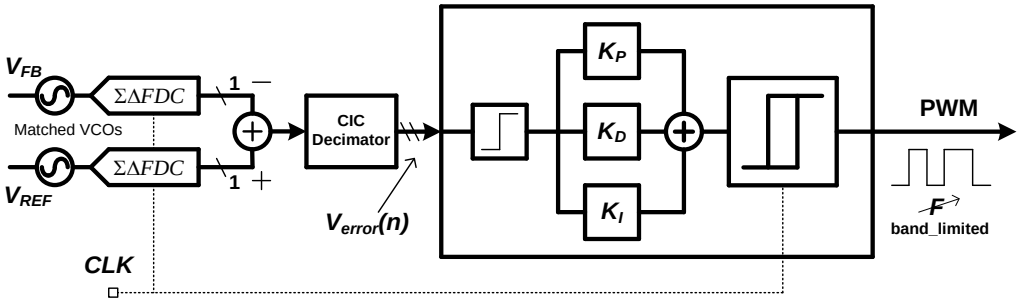


Fig. 17: Proposed digital sliding-mode controller, for comparison to prior art.

Chapter 3

METHODOLOGY

3.1 Top Level Architectural Design

The top level of the proposed architecture is presented here in Fig. 18. Compared to Fig. 2 (a conventional digitally controlled DC-DC buck converter) the small signal digital PID compensation block and DPWM block are replaced by a digital Sliding Mode Controller.

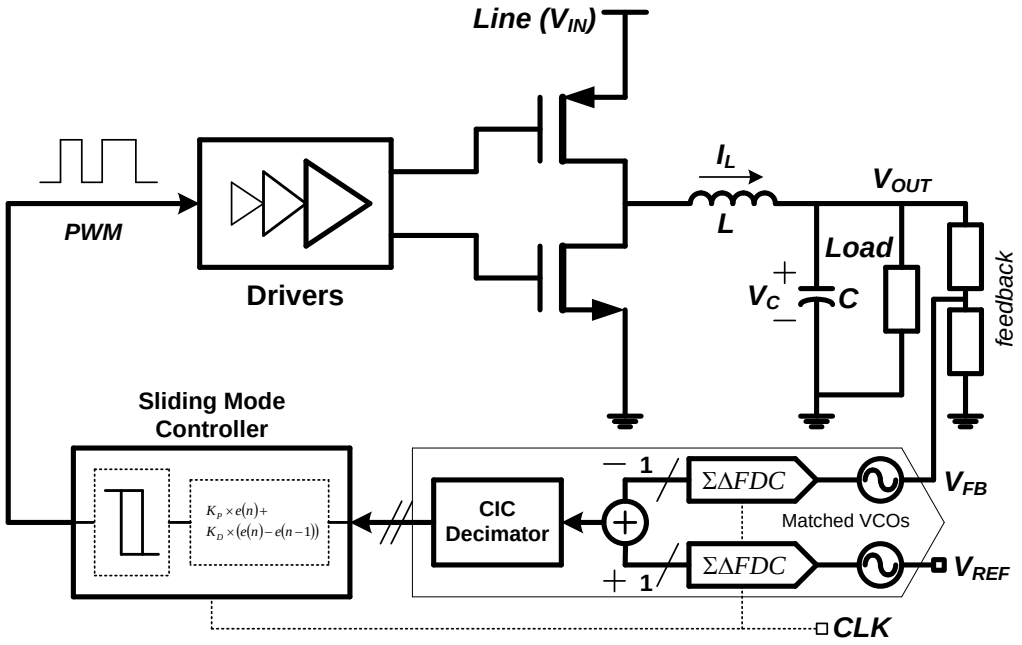


Fig. 18: The proposed oversampled, digital sliding mode control buck converter.

Similar to the analog implementation of sliding mode in a buck converter shown in Fig. 13, the digital difference between the output voltage (or scaled version of it) and a reference voltage undergoes through the digital sliding mode controller. The structure and

circuit implementation of the ADC and sliding mode are presented in the following sections, followed by a discussion on optimization of the loop and the role of the CIC decimator, and closing with a comparison to existing control schemes.

3.2 Frequency Domain Oversampled ADC Design

Analog-to-Digital (ADC) and Digital-to-Analog (DAC) converters are the gateway between the real world and the digital processing controllers and computers. Data in any format such as voice, video, temperature need to be processed in order to be saved, transported, measured, etc. Nowadays, most-if not all computers and controllers are digital; and therefore, the need to convert data from analog-format to digital-words and vice versa are essential functions.

There are many architectures for ADCs and DACs, but one way to categorize the converters is based on their over sampling ratio (OSR). If the sampling frequency of the converter is 2 times or just a bit more than 2 times the bandwidth of the signal of interest, the converter is called Nyquist rate converter.

If the sampling frequency is much more than the bandwidth of interest, the converter is referred to as Over-Sampling data converter.

$$f_{SAMP} \approx 2 \times BW \rightarrow Nyquist$$
$$f_{SAMP} >> 2 \times BW \rightarrow OverSampling$$

There are many advantages and some drawbacks in Over-Sampling converters, but one of the main features is that the anti-aliasing filters are not needed or their requirements are significantly relaxed, as opposed to Nyquist converters.

Sigma-Delta converters (ΣΔ) are in the over-sampling category. These converters are suited for lower bandwidths and very high accuracy (or higher number of bits). Fig. 19 is a block diagram of a typical (and traditional) ΣΔ ADC.

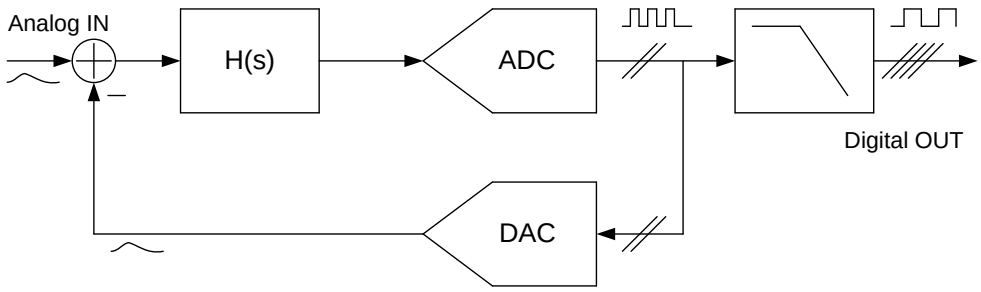


Fig. 19: Block diagram of a traditional ΣΔ ADC.

In this type of converters the analog input is passed through an analog filter (the H(s) block) and then quantized at the ADC block. The quantized signal is then fed back to be subtracted from the input. Since the nature of the data at the input of the modulator and the output of the ADC are different, the digitized signal needs to be converted back to analog with the help of DAC block. It can be seen that in this architecture, the input signal is being averaged so the output will eventually look exactly like the input. This is why these data converters work for lower bandwidths, and unlike the Nyquist rate converters, there is no direct relationship between the input and the output.

The output of the ADC block has higher rates and lower number of bits and in a complete ΣΔ ADC, a filter known as Decimator lowers the frequency and increases the number of bits to the desired output digital word. The H(s) block or analog filter that its function is averaging could be implemented in either discrete-time (D.T.) or continuous-

time (C.T.). It also could have orders other than one. In general, the resolution of a ΣΔ ADC could be increased by one or combinations of the following:

(1) Increasing the OSR

(2) Increasing the order of the filter

(3) Increasing the number of levels in the quantizer

The higher resolution does not come free obviously, and each one of the above methods brings some design challenges with itself. In general the overall accuracy of a ΣΔ ADC is shown in the following expression:

$$SQNR = \frac{3 \times (M+1)^2 \times (2L+1) \times OSR^{2L+1}}{\pi^{2L} \times 2} \qquad (4)$$

where M is the number of quantizer levels, L is the filter order, and OSR is the over-sampling ratio.

One of the main reasons ΣΔ ADCs offer higher accuracy is based on the fact that the added quantization noise (which happens in both Nyquist and Over-Sampling converters) is being shaped to higher frequencies, and then it is filtered out.

In order to understand the concept of quantization-noise-shaping or noise-shaping, an AC model is extremely helpful. Fig. 20 represents a linear model of a ΣΔ Modulator. In this model the quantizer is replaced simply by a noise source.

The signal transfer function assuming zero noise is:

$$STF_{(NQ=0)} = \frac{H(s)}{1+H(s)} \cdot X \approx X \qquad (5)$$

This shows that by utilizing high gain filters like integrators, the signal passes through the system without change. The noise transfer function turns out to be:

$$NTF_{(X=0)} = \frac{1}{1+H(s)} \cdot NQ \qquad (6)$$

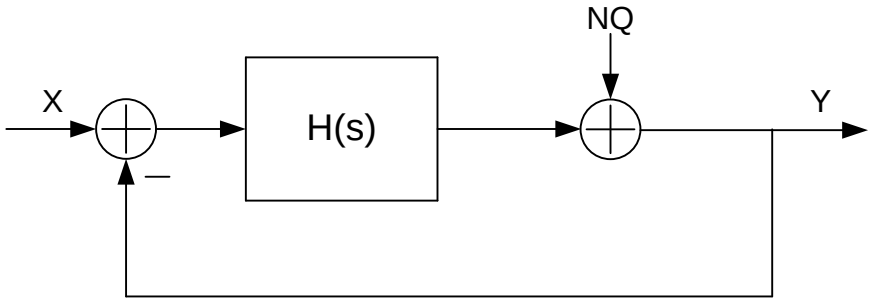


Fig. 20: Linear AC model of a ΣΔ Modulator.

The quantization noise on the other hand does not see the same transfer function, and it is high-passed.

A comparison (and conversion) of a traditional (discrete time) modulator to the VCO based open loop modulator based on [23] is presented in Fig. 21. It can be easily verified that in both configurations, the signal is being passed through and the noise is being high-passed.

VerilogA models were used to simulate and demonstrate the above discussion. A 1st order modulator is designed and normalized. It can be seen from Fig. 22 that the signal is low-passed or averaged through the modulator, and the quantization noise is high-passed. The high-passed noise is being filtered according to the bandwidth of interest.

Fig. 23 is presented to compare the noise-shaping effects. As mentioned earlier, by increasing the filter order, the noise-shaping improves. Shown in Fig. 23, a 1st order modulator suppresses the noise at the rate of 20dB/Dec, whereas a 2nd order suppresses the noise at double the rate, or 40dB/Dec.

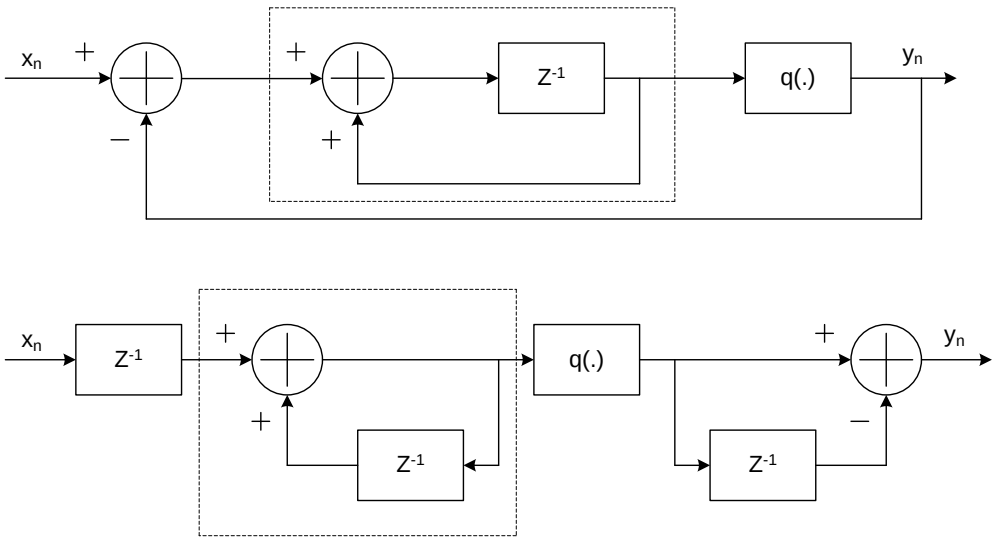


Fig. 21: Linear models of a traditional modulator and the open loop modulator utilized in this approach.

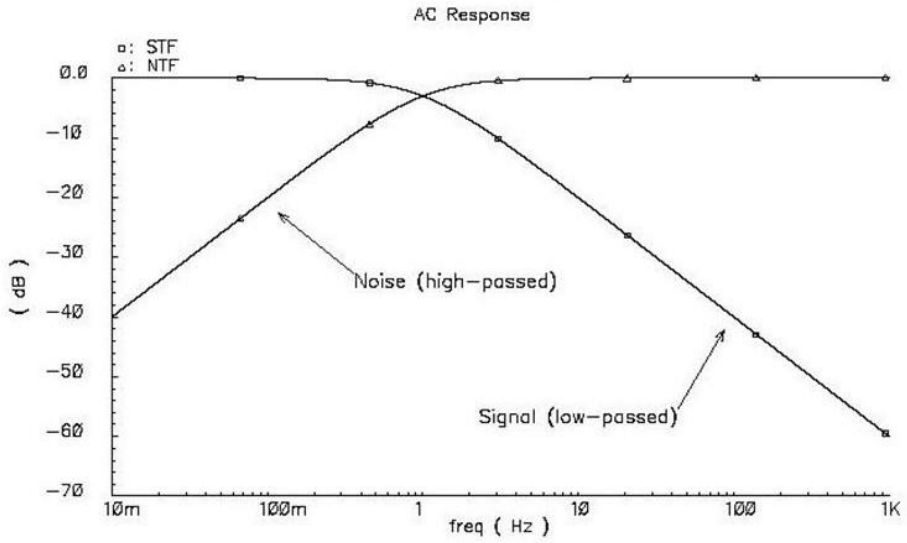


Fig. 22: STF and NTF in a 1st order modulator.

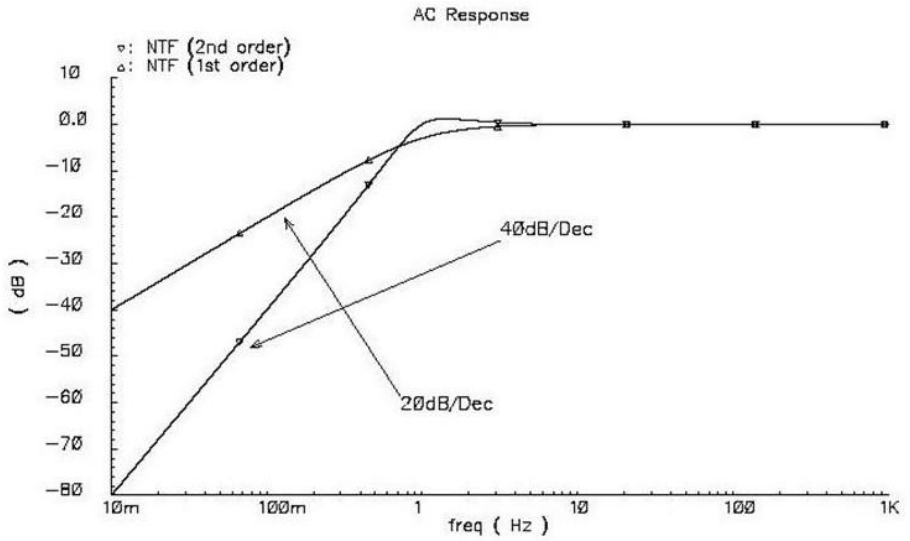


Fig. 23: Comparison of NTF in 1st and 2nd order modulators.

As described earlier, one of the critical components of a digitally controlled DC-DC converter is a feedback signal digitizer. The ADCs used for the digital DC-DC converter applications should be low power with high conversion efficiency. In the proposed DSM controller a frequency domain ΣΔ ADC approach is adopted. The reference voltage and the output capacitor voltage are fed to two matched current-starved VCOs followed by ΣΔ frequency discriminators based on [23]. The difference between these bit-streams is decimated by a SINC filter to create a digital error signal. The benefits associated with two matched ADCs instead of a single multiplexed ADC includes elimination of an advisory circuit to decide when and how often to switch back and forth between the reference and output voltage, and better common mode noise rejection.

As shown in Fig. 24, with the help of a VCO, two D flip-flops and one X-OR block, a first order ΣΔ frequency discriminator can be designed; and Fig. 25 presents the

KVCO curve of the VCOs used in the design. Since no DPWM block is used in the proposed design, even a lower SNR is acceptable, as long as the output voltage ripple requirements are met. Fig. 26 shows the measured FFT plot of the ADC (alone) for the following condition: fin=7.395 kHz, Vin_p=100mV, ENB≈8, SNR≈50, this matches the 20dB/dec like the simulation shown in Fig. 22.

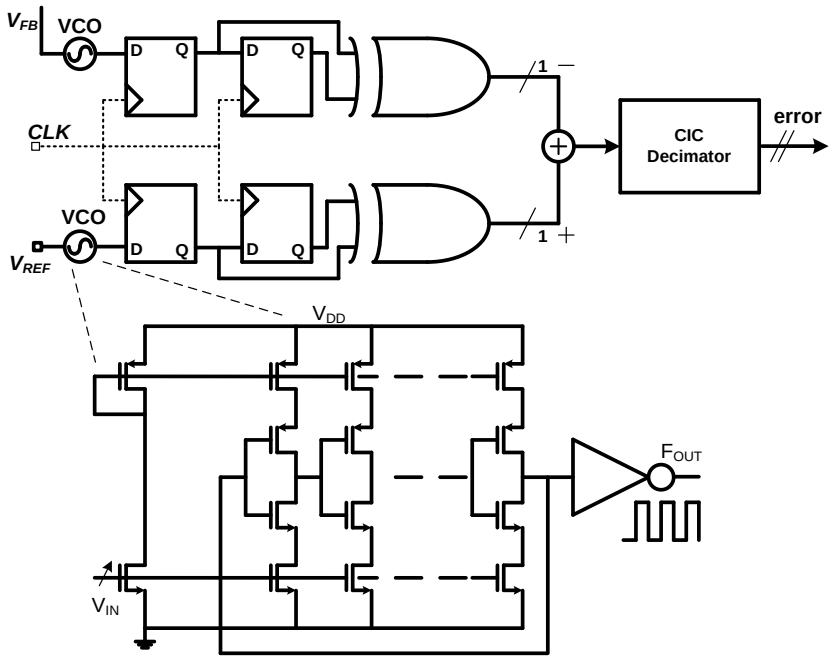


Fig. 24: Proposed frequency domain ΣΔ ADC, and Current-Starved VCO used as a voltage-to-frequency converter.

The proposed ADC has minimum analog complexity and can enable design re-use across different process technologies. Robustness of the ADC as opposed to analog intensive architectures is proven and shown in the experimental results in Chapter 4.

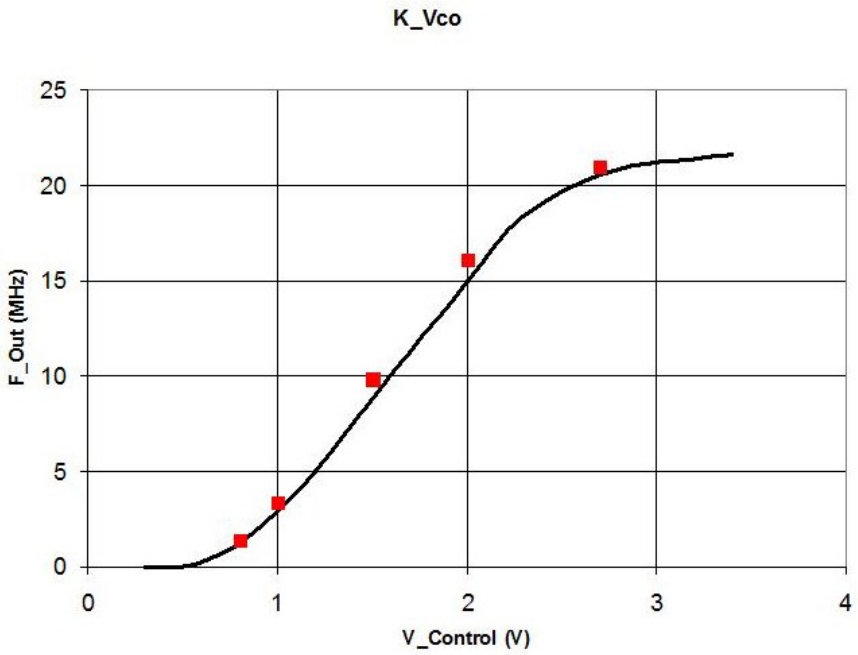


Fig. 25: K_Vco, simulated (dots) and measured (smooth line).

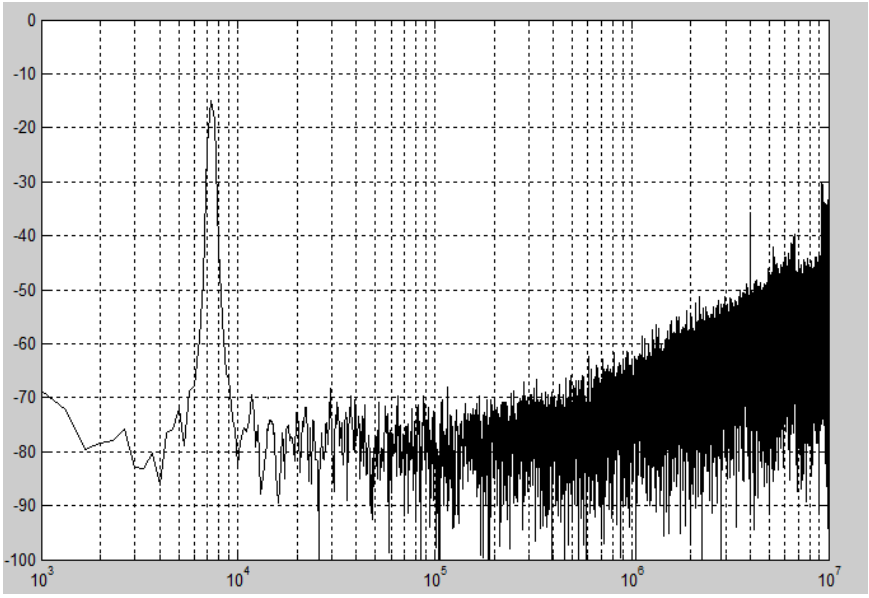


Fig. 26: Measured FFT (ADC alone) at: fin=7.395 kHz, Vin_p=100mV, ENB≈8, SNR≈50.

3.3 Digital Controller Design

Fig. 27 shows a conceptual view of the proposed digital sliding-mode controller.

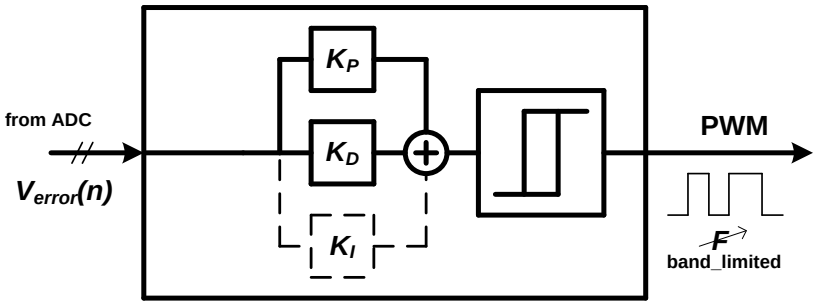


Fig. 27: The proposed digital sliding-mode controller.

The resulting error-word from the ADC goes through the sliding control law performed by the digital sliding-mode-control (DSMC) block. This error between the desired voltage and the output voltage first passes through the PD block (a proportional and differential), and then it goes to a hysteresis block. The input of the hysteresis block is a small signal as opposed to its output which is basically rail-to-rail. This rail-to-rail output is the desired PWM signal needed to generate necessary duty cycle for the functionality of the DC-DC converter and to ensures stability of the system.

Since a proportional and differential block (PD) is needed to perform the sliding-mode law, an alternative way to create the differential function of the block is chosen [11]. Fig. 28 shows how an integral block in a high-gain feedback loop can provide a differential function.

$$\frac{Y_1(s)}{X_1(s)} = s$$
$$\frac{Y_2(s)}{X_2(s)} = \frac{K}{1+\frac{K}{s}} \approx s \qquad (7)$$

where $X_1(s)$, $X_2(s)$, $Y_1(s)$, and $Y_2(s)$ represent the inputs and outputs of the blocks in s-domain respectively.

In order to create the modulated output signal or PWM, hysteresis can be applied to the integration, shown in Fig. 29.

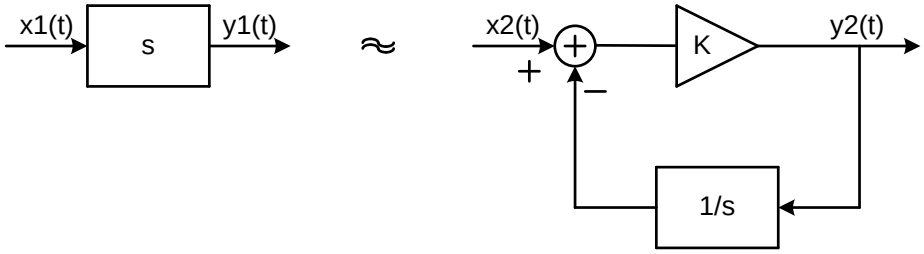


Fig. 28: Using an integrator in feedback of a high-gain loop to emulate a differentiator.

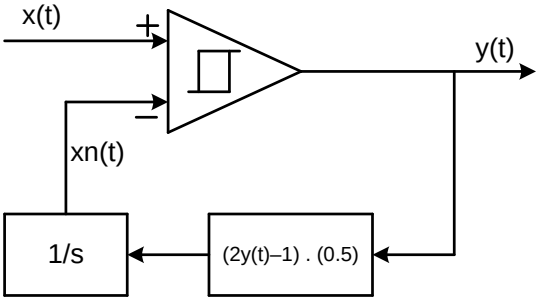


Fig. 29: Integration with added hysteresis to make modulated output pulses.

Using approximate averaged small-signal analysis:

$$\hat{X}n(s) = \frac{1}{s} \cdot \hat{Y}(s) \approx \hat{X}(s)$$
$$\Rightarrow \frac{\hat{Y}(s)}{\hat{X}(s)} \approx s \qquad (8)$$

where $\hat{X}(s)$, $\hat{X}n(s)$, and $\hat{Y}(s)$ represent the averaged value of the inputs and output of the loop shown in Fig. 29 in s-domain. The added block of $(2.y(t)-1).(0.5)$ is added in the loop to create a digital output of "0" and "1" or 0V and Vdd. This block oscillates and creates a 50% duty cycle for a constant input.

The complete proposed digital Sliding-Mode controller is shown in Fig. 30. It consists of the differentiator (based on an integrator in the feedback of a high-gain loop), an integrator in the forward path, and the *Fsw-Limiter* block.

Due to finite switching frequency of a practical DC-DC converter, a DC error occurs in the SMC controller. This error it is not systematic and it changes with load and input conditions. In the proposed approach a DC error canceling integrator (shown in a dash box in Fig. 30) is added to the controller with minimum impact on the system dynamics.

As shown in Fig. 30, the error-word takes two paths, one attenuation path to suppress the ripple at the output voltage and only passing the large transients, and another path to set the duty cycle and frequency (along with the DC offset canceling integrator).

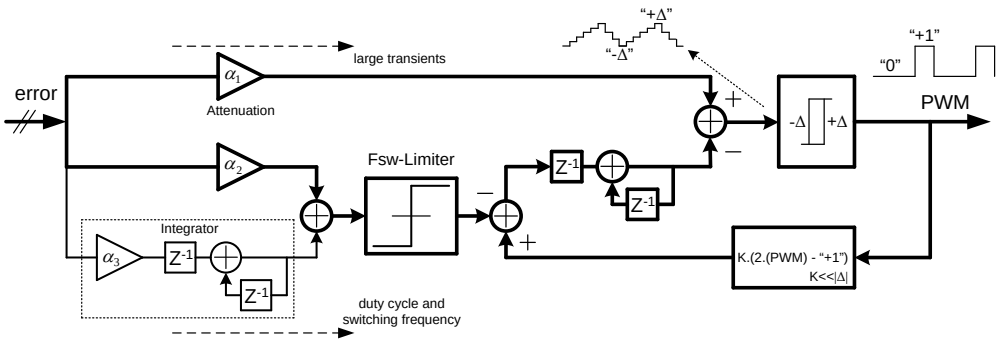


Fig. 30: The proposed Digital Sliding Mode Controller: two separate paths for error, DC offset cancelation integrator, and *FSW-Limiter* block.

In this approach, the capacitor voltage is chosen as the state variable to be controlled. The sliding surface is presented in (9) for discrete time as:

$$e(n) = V_{REF}(n) - V_C(n)$$

$$\Delta e(n) = e(n) - e(n-1)$$

$$S_d = K_{1d} \cdot e(n) + K_{2d} \cdot \Delta e(n) = 0 \qquad (9)$$

where $V_{REF}(n)$, $V_C(n)$ and $e(n)$ are reference voltage, capacitor voltage and the error between them at the time sample of n. K_{1d} and K_{2d} are the coefficients in digital domain, and S_d represent the digital sliding law. The sliding surface is being created by the error voltage and its derivative in digital domain.

A hysteresis band around the sliding surface (shown in Fig. 12 and Fig. 30) reduces the switching frequency to a more practical one, and the sliding surface divides the state space into 2 regions (Fig. 12). The controller toggles back and forth between 2 regions with a frequency mostly set by the hysteresis band (Fig. 30). The overall transfer function of the controller in Laplace-domain, considering oversampling can be approximated as:

$$\frac{PWM(s)}{e(s)} \approx \left(K_P + \left(K_D \cdot s\right)\right) + \left(K_I \cdot s^{-1}\right) \qquad (10)$$

where K_P (same as K_{1d} in (9)) is the proportional coefficient, K_D (same as K_{2d} in (9)) is the differential coefficient; K_I is the integral coefficient, and $e(s)$ is the error voltage.

The first part of the transfer function is the proportional and differential functions representing the sliding surface, and the second part of the transfer function is the integrator added to reduce the DC offset error without loss of generality. An improved digitized version of a hysteretic differentiator made from an integrator inside a high-gain

loop is employed in the proposed design [11]. A constant input to the differentiator generates a constant switching frequency f_{SW} at its output:

$$f_{SW} \approx \frac{K}{\left(T_{CLK} \cdot 4 \cdot |\Delta|\right)} \tag{11}$$

where f_{SW} is the DC-DC converter switching frequency, T_{CLK} is the oversampling clock, K is a constant, and Δ is the hysteresis band.

The stability of the DC-DC converter and the choice of the LC filter components are tied together. In a fixed-frequency and traditional DC-DC buck converter, choosing the filter capacitor and inductor could be based on the following relationships [24]:

$$I_{O(crit)} = \frac{\Delta I_L}{2}$$

$$L_{\min} \geq \frac{V_O \times \left(1 - \frac{V_O}{V_{I(\max)}}\right) \times T_S}{2 \times I_{O(crit)}} \tag{12}$$

$$C \geq \frac{\Delta I_L}{8 \times f_S \times \Delta V_O}$$

$$C \geq \frac{I_{O(\max)} \times \left(1 - \frac{I_{O(\max)}}{\Delta I_L}\right)^2}{f_S \times \Delta V_O} \tag{13}$$

where L and C denote the inductor and capacitor, $I_{O(crit)}$ is the minimum current to maintain continuous conduction mode, ΔI_L is the inductor current ripple, ΔV_O is the output voltage ripple, and f_S is the fixed switching frequency.

Stability and the choice of L and C for a buck converter with sliding-mode as the controller based on [20] and [21] are achieved by meeting the following relationships respectively:

$$0 < LC \cdot \frac{\alpha_I}{\alpha_D} \cdot \left(v_{REF} - v_C(ss)\right) - L \cdot \left(\frac{\alpha_P}{\alpha_D} - \frac{1}{R_{Load} \cdot C}\right) \cdot i_C(ss) + v_C < Vdd \tag{14}$$

$$-Vdd < k_1 \cdot (LC) \cdot x_1' - x_1 - \left(v_{REF} + L \cdot \frac{di_{Load}}{dt}\right) < 0 \tag{15}$$

where C, L, and R_{LOAD} denote the capacitance, inductance, and instantaneous load resistance of the converters, respectively; v_{REF}, Vdd, and $v_C(ss)$ denote the reference, input, and capacitor voltages, respectively; $i_C(ss)$ denotes the instantaneous capacitor current; α_P, α_D, α_I are the proportional, differential and integral coefficients; k_1 is the ratio of proportional and differential; and x_1 and x_1' denote the error voltage and its derivative.

In [13] the implementation of the stability is quite similar to (14) and (15), and it is employed here in this work:

$$\frac{K_P}{K_D} \approx 2 \times \frac{1}{2 \cdot \pi \cdot \sqrt{L \times C}} \tag{16}$$

where K_P and K_D are the proportional and differential coefficients from (10), and L and C are the filter inductance and capacitance respectively.

Of the three conditions that are required for the implementation of a sliding surface as a stabilizing reference path as stated earlier, the hitting condition in a buck converter is satisfied due to its alternating structural modes (Fig. 12). To meet the existence condition, the ratio of the proportional to differential coefficient should be as much as twice the natural frequency of the LC filter to maintain the sliding condition [13]. To achieve this K_P and K_D were set to the values of 0.06 and 6.8e-6 respectively and K_I was set to a value of 32 to stay stable. Since sliding-mode controllers are not too sensitive to parameters and circuit changes, a range for L and C are suggested (and acceptable for a

stable and functional converter) instead of fixed values, an advantage of SMCs in general and this methodology in particular. In this approach the ranges for L and C are from 1μH~2μH and 180μF~260μF respectively.

3.2.1 Wide-Band Limiter

If the switching frequency in a Sliding-Mode controller is not limited, the variation will be very wide. This is not desirable in many applications particularly hand held devices with transceivers on board. In this approach the error is limited by an upper and lower bound block called *FSW-Limiter*. This block is basically a digital clamp that limits the error in the lower path (shown in Fig. 30) of controller.

Fig. 31: Variation of switching frequency FSW (KHz) versus the band-limiting block range with respect to full-scale.

Approximately 7% of the full scale limits the switching frequency to 800kHz-1.2MHz range in this approach. Fig. 31 shows more choices and the frequency deviations trade off based on the required frequency of operation.

The full-scale refers to the ADCs full-scale input dynamic range, which is 2 volts (0V to 2V). As shown in the plot (Fig. 31) for a higher percentage of full-scale the switching frequency deviation is bigger and it provides greater range for line regulations and also faster responses for both line and load regulations. The drawback is that the frequency contents at the output have a wider band. Conversely, a smaller range of the full-scale has less frequency contents at the output with the price of having slower response time.

3.4 Optimization

As mentioned earlier the quantization noise shaping associated with ΣΔ modulation pushes the quantization noise to higher frequencies; and at the same time nonlinear systems such as the digital SMC can fold high frequency high power out of band noise to in-band. In addition to noise folding, higher frequency tonal content can intermodulate and bring the tones in-band, causing ripple at the converter output. If decimation is not used at the ADC output, the aliased noise within the converter bandwidth can leak to the regulator output.

This problem can be reduced by optimum filtering of the output of the noise shaped ADCs using high order SINC filtering with minimum phase delay. SINC filters provide effective sampling rate reduction with minimum hardware complexity. On the other hand, higher order decimation filtering can cause excessive phase delays, causing

stability problems. For a typical order N, decimate by M order SINC filter, the phase delay is represented by:

$$\angle H(f) = \pi \cdot N \cdot \left(\frac{f}{f_{CLK}} \right) \cdot (1 - M) \tag{17}$$

where *H(f)* is transfer function of the SINC filter. In order to suppress the first order noise shaped used in this design, a second order filtering is used. Typical order-B ΣΔ modulator generates a shaped quantization noise as follows:

$$E_q(z) = \varepsilon_q . (1 - z)^B \tag{18}$$

where ε_q is the quantization error noise density. In a digital SMC application the controller requires a high SNR estimation of digitized values of the state of interest (and its derivative) at every switching cycle. Therefore an optimum decimation ratio must be computed for a given switching frequency range.

The critical nonlinearity of the proposed digital SMC occurs at the input of the nonlinear hysteresis block; therefore it is critical to minimize quantization noise at that point. The quantization noise spectral density at the input of the nonlinear hysteresis block shown is represented as:

$$E_q(z) \cdot H(z) \cdot TF(z) = \varepsilon_q \cdot \left(1 - z^{-1}\right) \cdot \left[\frac{1}{M^2} \left(\frac{1 - z^{-M}}{1 - z^{-1}} \right)^2 \right] \times \left(\alpha_1 - \alpha_2 \frac{1}{1 - z^{-1}} + K \frac{1}{1 - z^{-1}} \right) \tag{19}$$

where *H(z)* is the 2nd order SINC response and *TF(z)* is the SMC transfer function. Total integrated noise power at the input of the nonlinear hysteresis block is represented as:

$$\varepsilon_{q,RMS}^2 = \int_0^{(f_{CLK})/2} C_1 \varepsilon_q{}^2 \sin^2\left(\frac{\pi \cdot f}{f_{CLK}}\right) \times \left(\frac{\sin(\pi M f / f_{CLK})}{\sin(\pi f / f_{CLK})}\right)^2 \cdot (K_1 + K_2 f)^2 \cdot df \quad (20)$$

where C_1 reflects the products of the constants. Optimum filtering of the output of the noise shaped ADCs using SINC filtering requires minimum phase delay with maximum noise suppression. Higher decimation ratio cause higher phase delay, which eventually causes instability in closed loop operations. On the other hand, lower decimation ratio cannot suppress out-of-band quantization noise, and effects of aliased noise and spurs can start showing up in-band. For a first order ΣΔ modulator sliding mode controller, the delay-quantization product could be minimized as:

$$\gamma = \min\left\{\varepsilon_{q,RMS} \cdot \left(\pi N \cdot \left(\frac{f}{f_{CLK}}\right) \cdot (1 - M)\right)\right\} \quad (21)$$

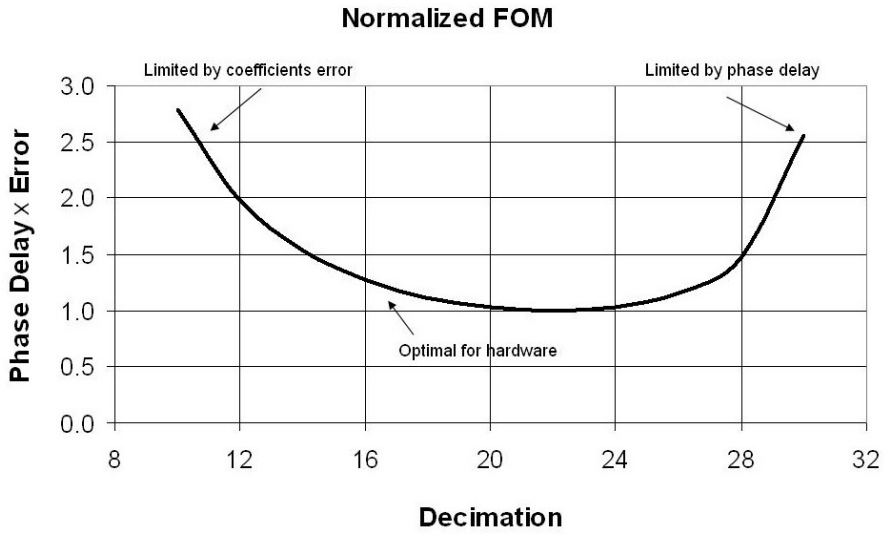


Fig. 32: Optimization of decimation ratio.

In Fig. 32 the normalized product of the delay times the integrated quantization noise associated with lower oversampling at the differentiator input for the proposed design is plotted vs. decimation ratio. Based on the figure of merit shown in Fig. 32, a decimation ratio of Decimation=16 gives the optimum noise and delay product.

3.5 Comparison to Existing Control Schemes

Since most available designs and particularly most of the commercial products in power management are based on small signal [18] approach and they require a form of compensations known as PID, the differences between these approaches and the claimed large signal PD or PID in the proposed design should be cleared. Besides, there are a few other types of fast transient controllers like Hysteretic controllers that could be compared with Sliding-Mode approach for their similarities and differences. These concepts along with misconceptions on shortcomings of SMC as opposed to their implementation's shortcomings are presented in the following subsections.

3.5.1 Small Signal PID vs. Large Signal PID

The proposed design of PD (or PID with the added integrator) is a large-signal PID, as opposed to the small-signal PID utilized in typical DC-DC converters or any other control systems. In the latter the PID is in charge of stability "only" and it is significantly slow since it is designed based on local linearization of a non-linear system (most practical systems), in SMCs (and our approach) the PD or PID is the main part of the controller. Although adding integration operation to any loop makes the system much slower to respond to disturbances, in practice [19] the integral action in this approach

(and in SMCs) is enabled only when the system is on the sliding line/surface, and only PD is in charge of the large transients. It is not possible to obtain similar performance (presented in Chapter 4) from a typical small signal PID controller presented in [28] [29].

3.5.2 Hysteretic vs. Sliding Mode

Hysteretic controllers are in fact a simplified version of SMC (or generally speaking hysteretic controllers and sliding-mode controllers are in the larger category of "Bang-Bang" non-linear controllers). Hysteretic controllers are fast since similarly to Sliding-Mode controllers they too can operate freely without the need for next clocks.

However hysteretic controllers don't provide the wide range of robustness for line and load variations, since they simply make the current (or in a few cases voltage) toggle between 2 pre-defined values [30] [31]. They provide poor load and line regulations and mostly being used as a secondary controller (along with a fixed frequency main controller) when there is a need to respond to a large transient, or they are used as a second stage following an LDO or another buck converter to provide fast tracking of a reference as adaptive power supplies. One should consider the true efficiency when comparing these types of hysteretic controllers to a complete controller such as a self-sufficient sliding-mode buck converter.

Sliding-Mode controllers on the other hand work on the states of the system and bring the system to a zero error constantly upon power up and any other disturbances and they provide excellent line and load regulations.

3.5.3 Filter Capacitor's ESR

It's very important to distinguish the practical sliding-mode control's shortcomings in general and the issues with its implementation in buck converters.

Wide variation of switching frequency and DC offset error are the shortcomings associated with sliding-mode in general, since ideal sliding-mode based on Lyapunov theory is difficult (impractical) to achieve. Problems with the ESR of the filter capacitor, which makes the difference between the capacitor's voltage (the state of interest) and output voltage bigger and therefore causing accuracy errors at the output, is a trait that belongs to buck converters and the way sliding-mode is implemented. If one can measure, estimate, or even guess the values of the states of interests (or the value of the state and its derivative) for every switching cycle, the accuracy error or dependency of the output voltage on the ESR of the capacitor is no longer an issue. In many implementations of sliding-mode such as this work, the value of the output voltage is being taken in lieu of the filter capacitor voltage; therefore, a low ESR capacitor is required. This does not project any practical limitations or drawbacks in these implementations.

Most of the manufacturers of commercial integrated circuits, if not all, provide datasheets that require specific external components for their ICs to perform and function properly. For example, most power linear regulators known as LDOs require a minimum (and maximum) ESR for the external filter capacitor [26] to operate for the wide range of loads and other conditions without any oscillations.

Chapter 4

MEASUREMENTS

4.1 CMOS Technology Process

In order to make the design more robust to the harsh environment, a robust process technology was utilized. Fig. 33 shows the die micrograph, which was fabricated on a 5-layer metal, 1-level poly, 0.35μm radiation hardened CMOS process, by Sandia National Laboratory. For completeness, a quick review of the process is presented.

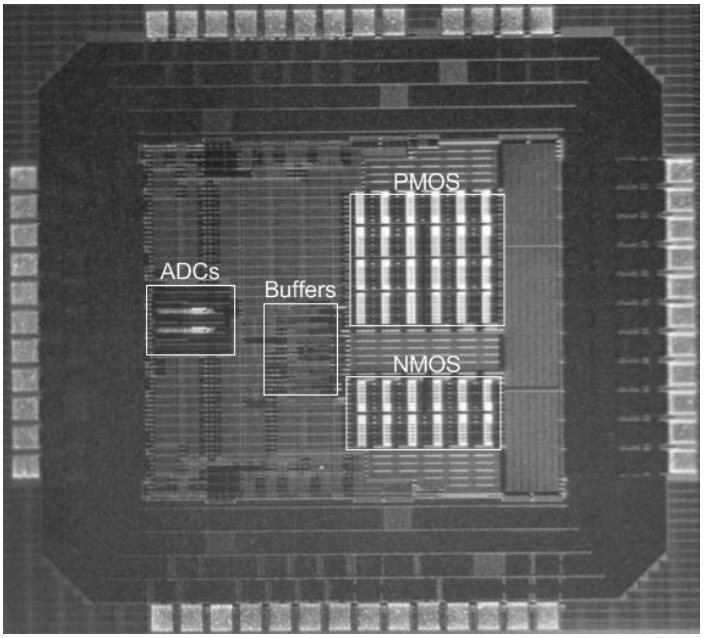


Fig. 33: The die micrograph.

Sandia National Laboratory offers CMOS7 process a Rad-Hard process technology which has been used in many of their internal digital designs. With collaborations between ASU and Sandia Lab, the process technology kit was optimized

and tested for analog and mixed-mode designs. BUSFET – A Radiation-Hardened SOI transistor is the main feature of this process, shown in Fig. 34. A shallow source and deep drain, along with the body-source tied together have proven robustness against radiation [25]. A comparison of the CMOS7 FET with a regular FET is shown in Fig. 35 for various tests conditions.

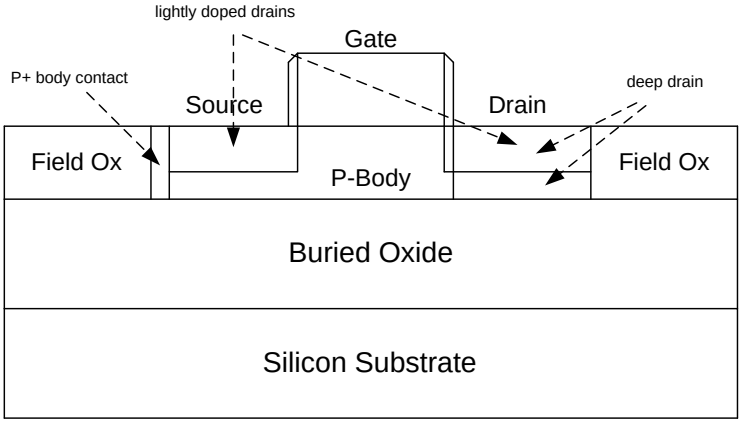


Fig. 34: BUSFET, a Rad-Hard FET from CMOS7 by Sandia.

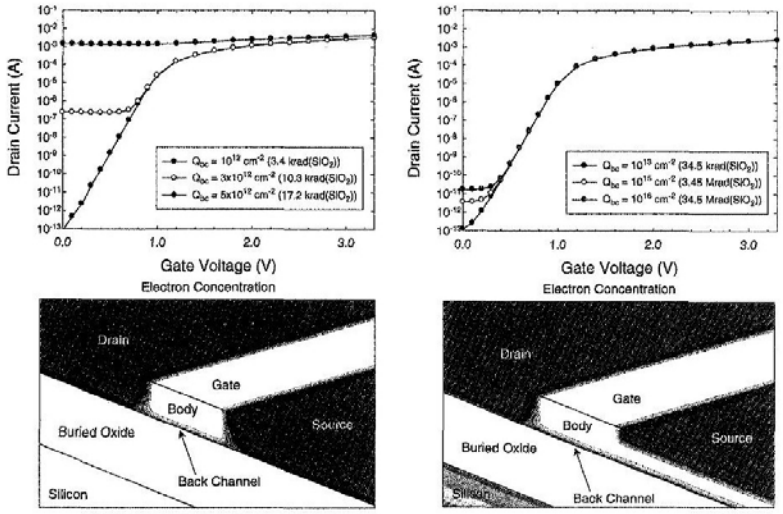


Fig. 35: Comparison of regular FET (left) to BUSFET (right).

Shown in Fig. 35 the simulated [25] response of a standard partially depleted SOI-MOSFET to radiation-induced charge buildup at the back-channel interface is shown on the left side, compared to a partially-depleted SOI-BUSFET on the right side. For a regular FET a back-channel charge density of $5x10^{12}$ cm^2 illustrates a conducting path between the drain and the source. On the other hand for the BUSFET although the back-channel interface is inverted, there is no conducting path between the drain and the source.

4.2 Test Setup

The manufactured chip was tested and measured for various conditions, and its performance matched the theory. The results for typical operations are presented in section 4.3, and the special test set up and conditions for radiation along with the performance summary are described in section 4.3.1.

In order to observe the load regulations as shown in Fig. 36, the load consists of a low impedance resistor in series with a high impedance resistor, and a power FET in parallel with the high impedance resistor. The power FET is switched OFF and ON with a pulse generator to change the loading from no-load condition (low output current) to heavy load condition (high output current).

Most DC supplies do not provide pulsed outputs or Vdds, and most (if not all) signal generators cannot tolerate heavy loading on them. In order to observe the line regulations, a separate board was designed. A power amplifier was designed in buffer mode, and the signal generator was used as its input. The amplifier output was pulsed accordingly and used as VDD or line.

4.3 Results

Fig. 37 shows line regulation for VIN=3.6V, and VOUT=1.2V. The input voltage (line) is changed to 20% of its value at a frequency of 1 kHz. The controller settles for 1% accuracy within 20µSec with less than 3% overshoot or undershoot. This is much faster than a fixed frequency switching regulator.

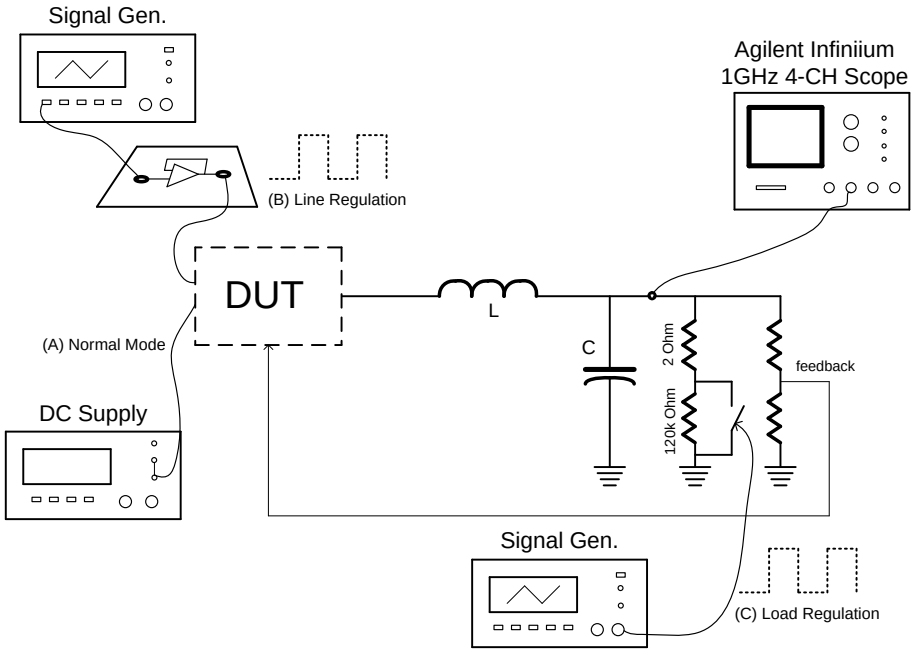


Fig. 36: Test set up.

Fig. 38 presents load regulation. The converter achieves 1% settling in 5µSec with an average switching frequency of 1MHz, and maximum undershoot of 5% for VIN=3.6V, VOUT=1.2V.

It can be seen that the regulator responds to the heavy demand of the load in such a short time, since it has the ability to change the frequency and duty cycle to absorb the disturbance. In a fixed frequency regulator, the loop needs to wait for the clock to make

correction and it has a limited window of opportunity to do so. This is why it takes much longer time for those regulators to respond to similar load demands.

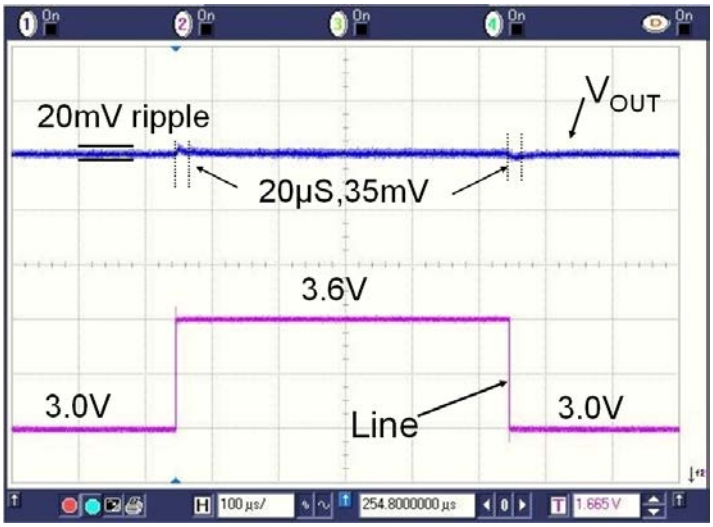


Fig. 37: Line regulation, Vout (top trace, 100mV/div), Line (bottom trace, 300mV/div), and time (100us/div).

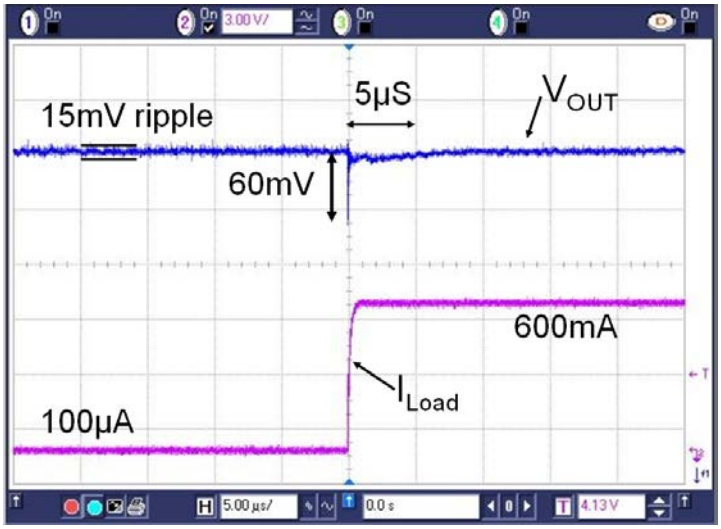


Fig. 38: Load regulation, Vout (top trace, 50mV/div), Load change command (bottom trace, 0.1mA-600mA), and time (5us/div).

The efficiency of the converter was tested under the following conditions: VIN=3.6V, Vout=2.5V, oversampling clock frequency of 32MHz, and switching

frequency of ~1MHz. The results of efficiency vs. output current are shown in Fig. 39. Peak efficiency of more than 80% in light to medium load region is achieved. This is significant in this class of controllers.

Measured power spectral density of the converter output voltage for a periodic load between 100µA to 600mA switching at a rate of 1kHz, resolution BW=10kHz is presented in Fig. 40. The output spectra show no spurs, with most of the concentration of the power only around the 800kHz to 1.2MHz. A fixed frequency regulator shows spurs of the harmonics (of the switching) on the x-axis, which is not desirable by system engineers.

The measured output ripple for a wide range of oversampling clock frequency of 22MHz-42MHz, which translates to a typical switching frequency of 900kHz-1.7MHz is 23mV, neither a function of switching frequency nor the ESR of the filter capacitor, as long as the ESR is reasonably low, shown in Fig. 41.

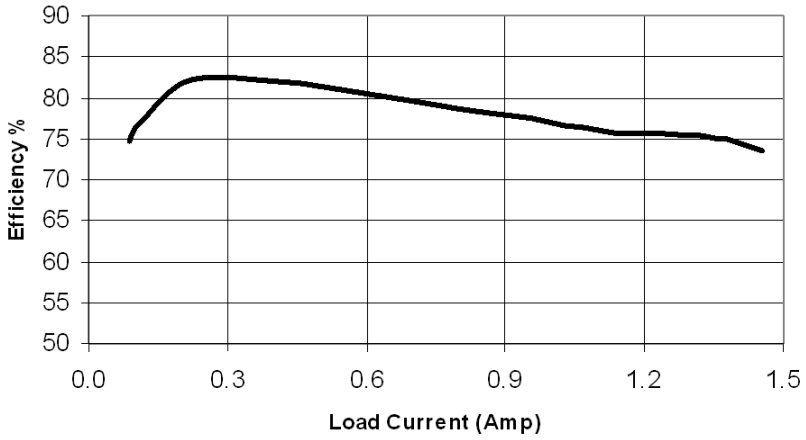


Fig. 39: Efficiency vs. output current (Amp).

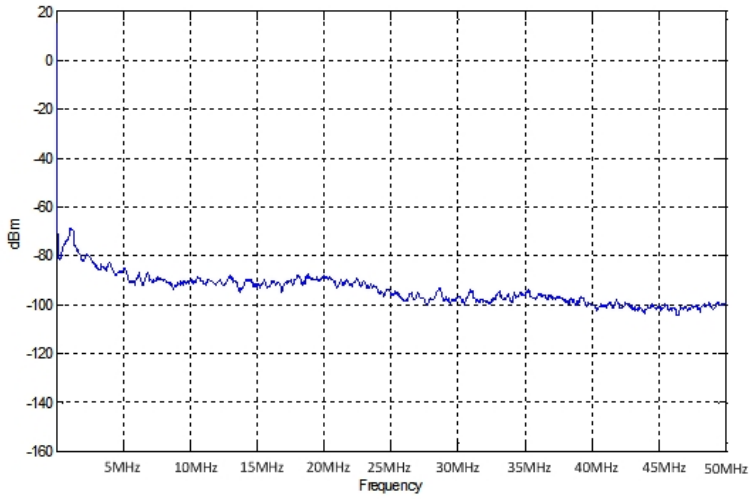


Fig. 40: PSD of the output shows no spurs repeated on the switching frequency and its multiples.

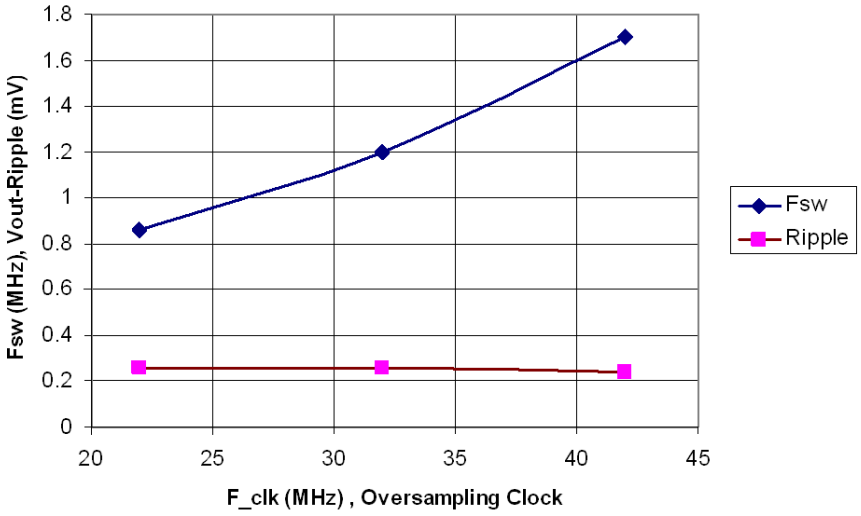


Fig. 41: Output voltage ripples and frequency as a function of the oversampled clock (diamonds: switching frequency; squares: ripples).

4.3.1 Radiation Testing

Space Micro (one of the sponsors of this research project) built and populated five (5) test and demonstration boards for the purpose of single event transient testing (SET)

at JPL's picosecond-scale pulsed laser facility, which is able to provide short, intense, and precise laser pulse so that SET response can be monitored at locations throughout the die. This is important to characterize the SETs pulse width and amplitude.

In order to access the sensitive die, it was necessary to have direct optical access to the test chip shown in the previous photos. In lab demonstrations, the die was encapsulated, but for the laser test, it was left exposed, with encapsulation along with perimeter to protect the wire bonds only. The photo below (Fig. 42) shows this arrangement.

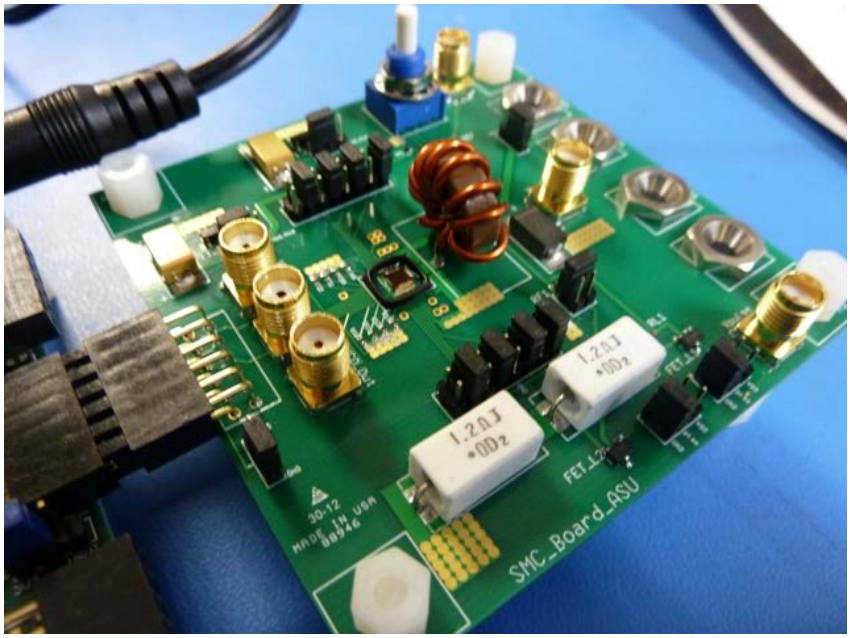


Fig. 42: Photo of Test PCB with Exposed Die (Courtesy of Space Micro).

The JPL pulsed laser has the following parameters:

- Laser: mode-locked Ti:sapphire (Spectra-Physics Tsunami laser)
- Wavelength: 800 nm
- Pulse length: approximately 2 ps

- Energy: up to 100 pJ per pulse
- Beam waist: 1.0 ± 0.2 µm
- Position accuracy: 0.1 µm
- Effective LET: ~100 MeV-cm^2/mg

The laser's effective LET is an order of magnitude estimate. The laser can not precisely correlate to heavy ion LET. Related to this, the laser measurements can not be used to calculate SET rates in the space radiation environment. However, it offers enough insight to perform a basic SET analysis.

Fig. 43 shows the test setup for the SET laser test. The laser was scanned across the entire exposed die to investigate regions sensitive to transients. Special attention was paid to the sigma-delta ADCs, as it was suspected that those would be the most sensitive regions. The output voltage was attached to an oscilloscope in order to capture transients and correlate them to a location on the die. The location of the laser was shown on a video screen, which shows the laser down to individual transistors. The process was repeated for multiple load and clocking stress conditions. The test was conducted at ambient temperature, approximately 25 °C.

In addition, the part was tested at high loads and non-ideal frequencies, from 28 MHz to 34 MHz, as well as offset the voltages on the ADCs, while exposing to the 100 pJ laser pulses, summarized in Table 1.

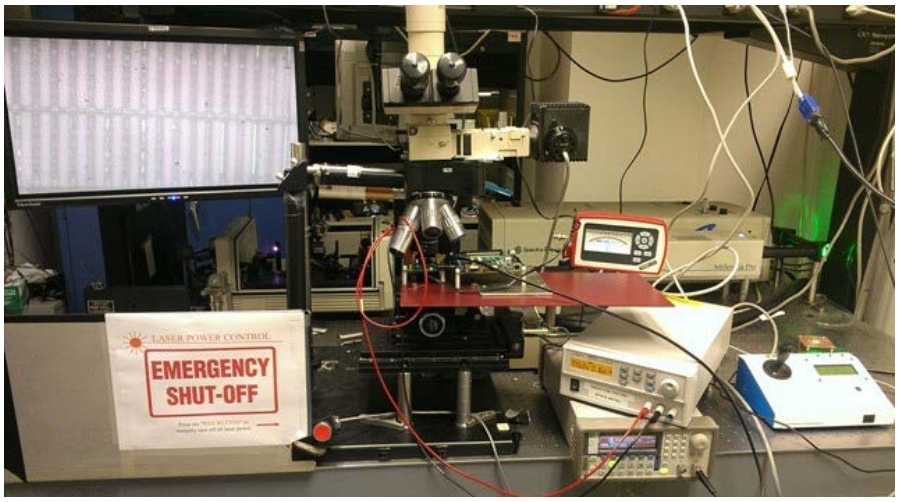


Fig. 43: Pulsed Laser SET Test Setup at JPL, with Video Screen on left, DUT at center, and Laser Source and Controls on right (Courtesy of Space Micro).

Table 1
S.E.T Testing Conditions

Laser Pulse Energy	Load Current (A)	Input Voltage (V)	Output Voltage (V)
60 pJ	.19 A	3.6	1.2
60 pJ	.89 A	3.6	1.2
100 pJ	.89 A	3.6	1.2

In all tests, at all locations on the die, no single event transient was observed. Therefore, the conclusion is that the accessible areas on the test die are immune to SETs. This is due to combination of the design, the fabrication process. The area of most concern, the ADCs, have proven invulnerable to SETs.

4.4 Comparison

The performance summary and comparison with two of the references are presented in Table 2. These references were chosen, since both provided a digital approach for sliding-mode, and both had proof of concept with manufactured ICs.

Efficiency is a direct function of frequency of operation and that explains better efficiencies for [13] and [15]. In addition to that, [13] needs a pre-regulated supply whose power consumption must be included in efficiency calculations. Moreover, as mentioned earlier, this work was done on a Rad-Hard process which was not optimized for analog and power management designs.

Regarding line and load regulations, this work shows superior performance for wide ranges of load and line disturbances.

Table 2
Performance Summary and Comparison

Parameter	[13] , 2002	[15] , 2010	This Work
Technology	0.25um CMOS	0.35um CMOS	0.35um CMOS
Die Area	1.43mm2	1.3mm2	2.72mm2
Vin/Vout (V)	2.5/1.1~2.3	1.6~3.3/0.9~3.0	2.8~3.8/1~2.5
Vout Ripple	<15mV	<30mV	<23mV
Switch. Freq. (MHz)	0.460-0.860	0.250*	0.800-1.2
Efficiency	89%~95%	96.5%(max)	72%~83%
Settling Time	5us (for 80mA)	0.6us (for 45mA)	5us (for 600mA)
Overshoot	65mV	122mV	60mV
Settling Time Line reg.	pre-regulated input	N/A	20us (for 20% line-jump)
Overshoot for line reg.	pre-regulated input	N/A	3%

*Extracted from the plot, not reported

Chapter 5

CONCLUSION

A digital sliding mode controller for point of the load applications employing frequency domain sigma-delta ADCs and a high-bandwidth digital hysteretic differentiator was introduced. The DC error associated with the SMC controllers was removed by utilizing an integrator, without impacting the first order behavior expected from the SMC controllers (in a second order buck converter). To avoid a wide variation in the switching frequency response, a frequency-limited operation was implemented.

Experimental results showed fast transient responses to load and line disturbances. The digital SMC controller proved robustness to disturbances and fast transient responses to load and line variations.

Sliding-mode-control, a very robust and powerful non-linear control has had its place in many applications such as: Underwater Vehicles, Automotive Transmissions and Engines, High-Performance Electric Motors, Robot Manipulators, Power Systems, and for the past few years Switching Regulators as well.

One of the earliest work [21] (perhaps the 1st work to be published) that utilized sliding-mode in a step-down switching regulator implemented the method in analog form. That work promised and demonstrated a superior performance as opposed to the more traditional or small signal design methodology.

Since then, many researchers [4]-[7], [9]-[10], [13]-[15], [22], and [32]-[35] have published their works on sliding-mode control in switching mode regulators like step-down buck converters. Tan, et. al., in [20] offers an extensive survey on almost all the

papers on this topic. Most of those works have been theoretical and only a few of them offered measured results from manufactured chips. A quick and yet comprehensive survey and comparison of the recent works on digital implementation of sliding-mode control (in step-down buck converters) is presented in Chapter 2.

This work has advanced the concept of robust and fast non-linear controllers for buck converters. This methodology can be implemented in other (similar) applications such as: step-up or boost converters, LDOs, multi-phase buck converters, and many more.

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