# Interlaboratory Study to Determine Repeatability of Damp-Heat Test Method for Potential-Induced Degradation and Polarization in Crystalline Silicon Photovoltaic Modules

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***Abstract*—To test reproducibility of a technical specification under development for potential-induced degradation (PID) and polarization, three crystalline silicon module types were distributed in five replicas each to five laboratories. Stress tests were performed in environmental chambers at 60°C, 85% relative humidity, 96 h, and with module nameplate system voltage applied. Results from the modules tested indicate that the test protocol can discern susceptibility to PID according to the pass/fail criteria with acceptable consistency from lab to lab; however, areas for improvement are indicated to achieve better uniformity in temperature and humidity on the module surfaces. In the analysis of variance of the results, 6% of the variance was attributed to laboratory influence, 34% to module design, and 60% to variability in test results within a given design. Testing with the additional factor of illumination with ultraviolet light slowed or arrested the degradation. Testing at 25°C with aluminum foil as the module ground was also examined for comparison. The foil, as tested, did not itself achieve consistent contact to ground at all surfaces; but methods to ensure more consistent grounding were found and proposed. The rates of degradation in each test are compared and details affecting the rates are discussed.**

## I. INTRODUCTION

Standardized testing helps ensure that: characteristics and performance of products are consistent, people use the same definitions and terms, and products are tested the same way. Such testing helps to reduce cost by providing photovoltaic (PV) product manufacturers and their customers with the information they need to ensure PV product lifetime, increase availability and performance, and decrease operation and maintenance costs of PV systems.

Round robins and interlaboratory testing for PV products occur regularly for power performance and more recently for PV packaging materials—especially the polymeric compounds [1]. However, there is little published literature on interlaboratory comparisons for durability of finished modules, such as for chamber testing for module durability and design qualification. Methodologies for performing interlaboratory studies exist, such as ASTM D7778-12, which was referenced for this work [2].

In the last decade, polarization [3] and potential-induced degradation (PID) [4] have come to be understood as critically important failure mechanisms that are not examined in standardized testing. Mechanistic aspects of PID occurring in conventional crystalline silicon films have been studied by Neumann and coworkers [5]. PID is understood to largely involve $Na^+$ migration toward the Si, especially interacting with stacking faults in silicon, leading to failure of the p-n junction. Various modeling to estimate durability in the field based on accelerated lifetime testing has also been published [6,7], but there are few confirmations of these tests with modules in the natural environment.

Implementation of accelerated testing for PID falls largely in the categories of (1) tests with heat and humidity, whereby the adhered water molecules on the module surface provide an extent of conduction to the grounded module frame [8] and (2) use of some conducting medium such as a metal foil applied to ground the module face. Application of heat and humidity in an environmental chamber promotes ionic conduction in module packages [9]. In comparisons to the performance of modules in the natural environment, the finite conductivity provided by the damp heat has been found to correctly evaluate PID in the presence of module frame-based mitigation techniques that impede leakage current flow to ground [10]. The method would be expected to represent the interactions between poor-quality glass and water (such as sodium leaching), and it has the ability to make electrical connections in declivities and pores on the module surface. However, the non-condensing humidity level in chamber tests does not generally provide an infinitely conductive path all the way to the center of large modules—rather, the PID effect is concentrated toward the module edges [11]. In many instances, this mimics the behavior in the natural environment [12]. Alternately, foil placement on the module surface contacts the whole module face [10] and may be desired to approximate the situation of a very highly conductive soiling layer, or a continuous water layer pooling for extended periods of time on the whole module face that is connected to ground.

A component of the work to arrive at conditions for a standardized test for the effects of system voltage durability comes from field comparisons with accelerated tests [13,14]. Tests show that with system voltage bias applied at 85°C and 85% relative humidity (RH), modules may show series-resistance degradation outside of the scope of this work. Testing at 60°C and 85% RH appears to primarily actuate the

PID mechanism, so this condition was used as the condition for comparison. The choice of 96 h comes from a study showing that designs that pass this damp heat with voltage-bias stress-test level for this duration with less than 5% relative degradation also do not degrade in the natural environment in Florida (USA) for a period of about 3 years, the extent tested [10].

Testing may have inherent variability from lab to lab; however, a goal of a test method for durability and safety is to have, within usual constraints of cost and time, the best achievable repeatability, independent of which laboratory the test is done. This interlaboratory comparison was therefore carried out to quantify the repeatability of the proposed damp-heat test with system voltage bias for PID susceptibility and to understand the possible sources of variability. A second goal was to see if the specified sample size (two modules per polarity) is adequate considering variations that might exist in the commercially shipped modules that were used. Any omissions and practical problems in the procedure, new ideas, or information for better execution and repeatability of the tests elucidated by multiple labs carrying out the testing are discussed for iterative improvements of the test methodology.

The test with foil on the module face is inherently done with the module in the dark. Unless lamps are placed in the environmental chamber or a chamber with a port window, the chamber tests are also done with the modules in the dark. It is necessary to have some understanding of this real-world environmental parameter and the effect of light added intentionally or unintentionally during testing, and we examined this here. Finally, the degradation of a module type stressed at 25°C with aluminum foil serving as the module ground was compared to that with the damp-heat stress-test method.

## II. Experiment

Three crystalline silicon module designs were distributed in five replicas each to five laboratories for a draft (unfinalized) testing procedure following that being developed within the International Electrotechnical Commission (IEC 62804). The delivery to each lab consisted of (with some exceptions) two modules for test in each polarity, and a control. The five-lab comparison was carried out according to the test plan for PID given in Table I. The stress tests were performed in environmental chambers at 60°C, 85% RH, and with a 96 h dwell. Module nameplate system voltage was applied to the cells by means of the shorted module leads [8] (two modules in each polarity) during the dwell and the ramps from and to ambient. The nameplate voltage for all modules tested was 1000 V. Stipulated tolerances for the dwell period of the chamber stress testing was ± 2°C and ± 5% RH. In anticipation of a pass/fail criterion (such as would be used in a qualification test), a successful "pass" was considered when both modules tested in the given polarity at the given test lab degrade less than 5%. Visual inspections and leakage-current tests must also be successfully passed. Recording and reporting of leakage current from the modules during the stress testing was proposed as optional because not all participating labs had the capability. Leakage current for the purpose of these tests is primarily used as an indicator of stability of the test environment (i.e., chamber conditions).

Table I
Test Sequence of the Interlaboratory Study. IEC 61215 Ed. 2. Refers to the Crystalline Silicon Terrestrial Photovoltaic Modules - Design Qualification and Type Approval [16]

| Step | Process |
|---|---|
| 1 | Check in modules |
| 2 | 5–20 kW/m$^2$ light soak |
| 3 | Rinse and wipe module surfaces |
| 4 | IEC 61215 Ed. 2, 10.1, visual inspection |
| 5 | I-V measurement under solar simulator |
| 6 | Electroluminescence imaging |
| 7 | IEC 61215 Ed. 2, 10.3 insulation test |
| 8 | Damp heat with bias stress; 60°C ± 2°C, 85% RH ± 5 % RH, + or – 1000 V, 96 h with no interruptions; measurement of leakage currents encouraged but optional |
| 9 | IEC 61215 Ed. 2, wet leakage-current test |
| 10 | I-V measurement under solar simulator |
| 11 | Electroluminescence imaging |
| 12 | IEC 61215 Ed. 2, 10.1, visual inspection |
| 13 | IEC 61215 Ed. 2, 10.3, insulation test |

Modules in this study were known based on preliminary testing to be significantly more sensitive in either the positive or negative polarity. Modules were chosen to be near the pass/fail limit vis-à-vis the 60°C/85% RH/-1000 V stress condition applied for 96 h to attempt to get useful statistics (without "censoring"). Stated another way, we could have chosen modules that don't exhibit any degradation, and modules that degrade an extreme amount, and shown how well the test differentiates the two; but such results would be less useful. Information about the modules selected is shown in Table II. In some cases, modules provided for test in the less-sensitive polarity were placed under test outdoors instead, the results of which may be published in the future when available.

Neither *in-situ* nor *ex-situ* current-voltage (I-V) measurements were performed on the module over the course of the stress test. Open-market modules with near-sequential serial numbers were chosen (but not necessarily currently shipping modules—one design was manufactured five years prior). They were not specially designed modules for the test.

The effects of light irradiating three module designs during the course of high-voltage stress testing in a damp-heat chamber were tested using Q-Labs UV-A bulbs with 340-nm peak irradiance. The total irradiance was 5 W/m$^2$, which corresponds to 0.2 suns of the AM1.5G spectrum considering the 290- to 400-nm band. The module surface was maintained at 60°C and 85% RH, which was achieved by setting the

chamber temperature and relative humidity to 59°C and 91% RH, respectively (for a dew point of 57°C). The effects of irradiance were explored on three different commercial silicon cell module types labeled A, B and C.

Finally, a comparison between the interlaboratory test condition in the damp-heat environmental chamber and an alternative room temperature foil test was explored to give a point of reference and understand the differing natures of these tests. A single module type was sent to one laboratory for testing in both the environmental chamber at 60°C, 85% RH, for 96 h and at 25°C with aluminum foil used as the ground electrode. The aluminum foil was covered with a polymeric mat to press the foil on the glass face to achieve constant contact to it. Two replicas went through each of the two tests. As in the damp-heat stress test, the shorted module leads were connected to the energized terminal of the -1000 V power supply (the PID-sensitive polarity of the module type) and the module frame was grounded.

TABLE II
DESCRIPTION OF THREE MODULE DESIGNS DISTRIBUTED BETWEEN FIVE LABS FOR INTERLABORATORY TESTING

| | |
|---|---|
| Module 1 | – 230 W class multicrystalline (mc)-Si module design (15.6 cm × 15.6 cm cell)<br>– Susceptible to degradation with cell circuit in negative voltage bias<br>– Manufactured from 2011 onward<br>– Based on previously published reports of PID tests under different conditions, the module was expected to show a PID signal, but less than 5% degradation in negative bias was expected. |
| Module 2 | – A 170 W class mc-Si module design (72 12.5 cm × 12.5 cm cells)<br>– Susceptible to degradation with cell circuit in negative voltage bias<br>– Manufactured in 2008 or 2009<br>– Expected to show PID based on prior data under different conditions, but significant scatter in the data had been expected due to poorer process control and increased variability in the cells made during this period and considering evidence from prior electroluminescence (EL) imaging. |
| Module 3 | – 235 W class crystalline Si module, 12.5 cm × 12. 5 cm cells<br>– Susceptible to degradation with cell circuit in positive voltage bias<br>– Manufactured in 2012<br>– Expected to show significantly less than 5% degradation based on pre-tests. |

## III. RESULTS AND DISCUSSION

### A. *Interlaboratory Test Results*

Results from the interlaboratory study laid out based on the test design in ASTM D 7778-12 are shown graphically in Fig. 1. Module type 1 failed in the negative polarity test at one of the five labs when one of the two replicas tested there failed with power degradation of greater than 5% (relative). Module type 2 failed in the negative polarity test at all five labs when at least one of the two modules tested failed at each lab. Module type 3 passed in all cases at all labs. Only power-performance degradation yielded failures; factors such as insulation test, visual inspection, and wet leakage-current test did not trigger any failures.

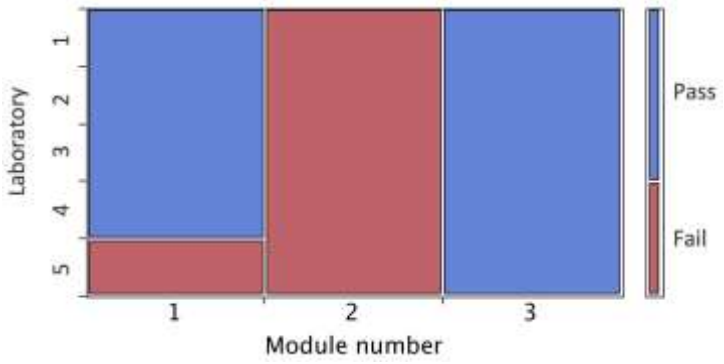


Fig. 1. Overview of the fraction of modules passed or failed for three different module types tested at five labs showing results only in their susceptible voltage polarity. If one or two modules tested in the given polarity failed ($P_{max}$ drop > 5%), that type is considered to have failed in that polarity at the given test lab.

To understand the distribution of results in the next level of detail, the relative degradation through all the stress tests in damp heat with positive or negative bias is shown in Fig. 2, with sample size, mean, and standard deviation shown in Table III. First, we can see the performance in the non-sensitive polarity, that little if any degradation is found as anticipated, and a view of the standard deviation from the intrinsic variability in the test (essentially module flash-testing) is manifested.

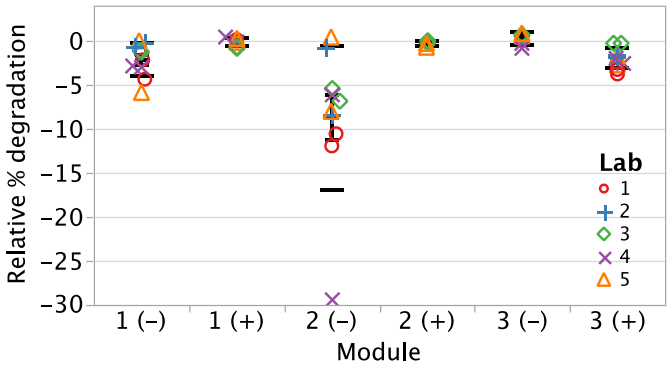


Fig. 2. Relative percent degradation in both polarities. Mean degradation and standard deviation markers are also given. The markers distinguish the five test labs.

Table III
SAMPLE SIZE, MEAN, AND STANDARD DEVIATION OF DEGRADATION AFTER STRESS TESTING FOR EACH LEVEL (MODULE DESIGN NUMBER AND POLARITY)

| Level | Number | Mean | Standard Deviation |
|---|---|---|---|
| 1 (-) | 10 | -2.12 | 1.87 |
| 1 (+) | 8 | -0.10 | 0.43 |
| 2 (-) | 10 | -8.70 | 8.22 |
| 2 (+) | 4 | -0.29 | 0.32 |
| 3 (-) | 6 | 0.30 | 0.68 |
| 3 (+) | 10 | -1.99 | 1.31 |

Module type 1 failed only at lab 5 in the negative-bias configuration. Considering a normal distribution, the mean degradation of 2.12% and standard deviation of 1.87%, there is about a 6% probability (a 1 in about 17 chance) of a module replica displaying greater than 5% degradation. We note that the second replica of module type 1 (the complement module of the one that degraded more than 5%) barely degraded at all at the same lab, denoted by red makers in the 1(–) column in Fig. 2. This hints that conditions at lab 5 are not uniformly more stressful causing the one failure of type 1. Variability in the module PID sensitivity or the inability to apply stress uniformly on modules at lab 5 are possible explanations.

Module type 2 exhibited the most extensive mean degradation and standard deviation in the negative-bias stress configuration. Viewing the mean degradation of 8.7%, it clearly does not meet the criterion of less that 5% degradation; therefore, failure through the protocol is fitting. However, it is seen that at two different labs, one of the two replicas tested of type 2 is measured to not degrade at all. A concern would then be about the chances of a false-pass, which would occur if these two designs happened to arrive at the same laboratory. There are 45 different combinations when the number of samples is ten with two samples in each combination, as is the case in this testing. The probability of those two modules ending up at one lab for a false-pass is 1 in 45 (2.22%). A fair question is whether two modules are sufficient for evaluating susceptibility to PID considering the variability. Any desired increase in the confidence interval could come from increasing the sample size to three or more, or retesting more frequently.

Module type 3 showed the least degradation in performance (1.99%) and smallest standard deviation (1.13%) in positive bias, which is its more sensitive configuration. In view of the near superposition of the points such as in the results from labs 1 and 3, the results were well reproducible within the given labs.

An analysis of variance was performed to explore the relative contribution to the variability factors for which we can analyze: the influence of the severity of the lab stress tests, influence of the module type with respect to PID sensitivity, and residual effects, which could consist of variability in PID sensitivity from module to module within a module type and the ability of the lab to obtain reproducible results on a given module type with a given PID sensitivity. The result of the analysis of variance is given in Fig. 3. Figure 3 (top) shows the module degradation (susceptible bias only) viewed as a function of lab to determine if any labs are consistently more severe than others. Lab means that are shown in Fig. 3 (top) indicate that labs 1 and 4 produce greater degradation; however, the mean for lab 4 is pulled down by the performance of one module of type 2, which was found above to have great variability in performance. Figure 3 (bottom) shows the computed contribution in percent for the variability components. From the analysis, it is found that the influence of the laboratory at which the modules were tested was the least influential parameter on the degradation; the module design was second-most influential; the most influential was variability in PID sensitivity from module to module within design—inclusive of the ability of the lab to obtain reproducible results on a given module with a given PID

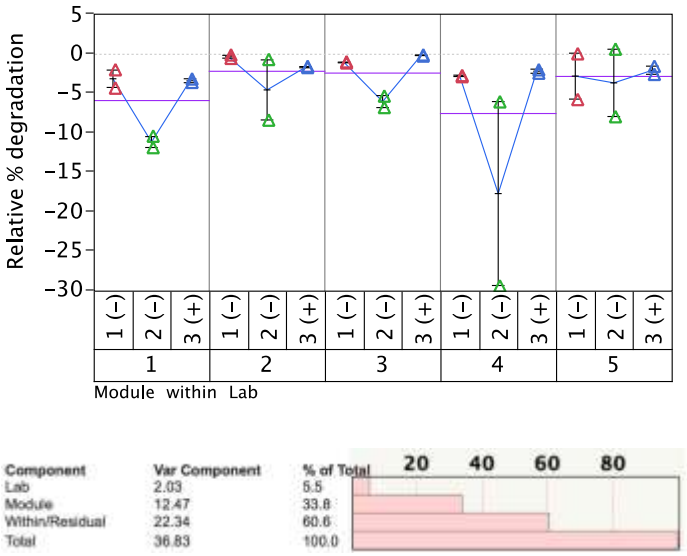


Fig. 3. Module degradation, susceptible bias only as indicated by (+) or (-) viewed as a function of lab to determine if any labs are more severe than others. The analysis shows that the choice of lab was the least influential component of the variance; the type of module was the next important factor, but variation of measured results *within* a given module type at a given lab (residual) was the most influential.

sensitivity. However, capability of good reproducibility within a given lab has previously been shown [10]. To further determine the effect of possible inadvertent variation in the stress levels applied by the laboratory to yield different outcomes of the test, the median degradation for each module type measured in the various laboratories was calculated and then added to the individual degradation data points. Median values were chosen as the point of reference to minimize effects of outlying data points on the analysis. The results of this analysis are collected in Fig. 4. With the larger pool of data, mean results for each lab and a grand mean are tabulated. The mean of lab 4 is pulled down in value for one data point; however, the balance of lab 4 data points is well centered on the line of zero deviation from the mean. Lab 1 displayed –2.3% in relative degradation compared to the mean, with tight grouping suggesting that this lab was more stressful. To the extent of data taken, no statistically significant differences in the data sets could be found considering the intersection of the 95% confidence intervals. However, it is likely that if the number of modules tested increased beyond six per lab per polarity, then the confidence in the means would tighten and statistically significant differences might then emerge.

Electroluminescence was performed before and after stress testing according to the test protocol. Example results for each module design are shown in Fig. 5. Module type 1 in Fig. 5 showed 2.1% relative degradation. Some regions of darkening on the right-hand side of the module after stress testing can be distinguished. Module type 2 in the example shown degraded 29%. Cells up to the third row from the edge appear significantly degraded according to their relative sensitivity. The replica of module type 3 shown degraded 3.7%. Evidence of degradation can be seen throughout the

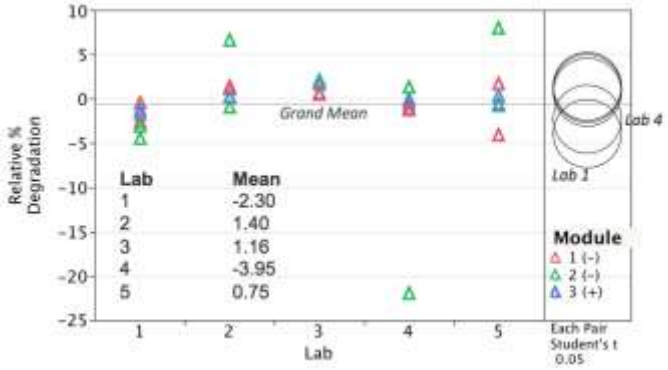


Fig. 4. Relative degradation (%) of the modules shown after subtracting median degradation for each module type, tested only in their sensitive polarity versus lab. The circles on the right show the 95% confidence intervals of the means. The analysis failed to show a statistically significant difference in degradation between labs. Degradation based on the means may be more pronounced in labs 1 and 4; however, lab 4 results contained a significant outlier.

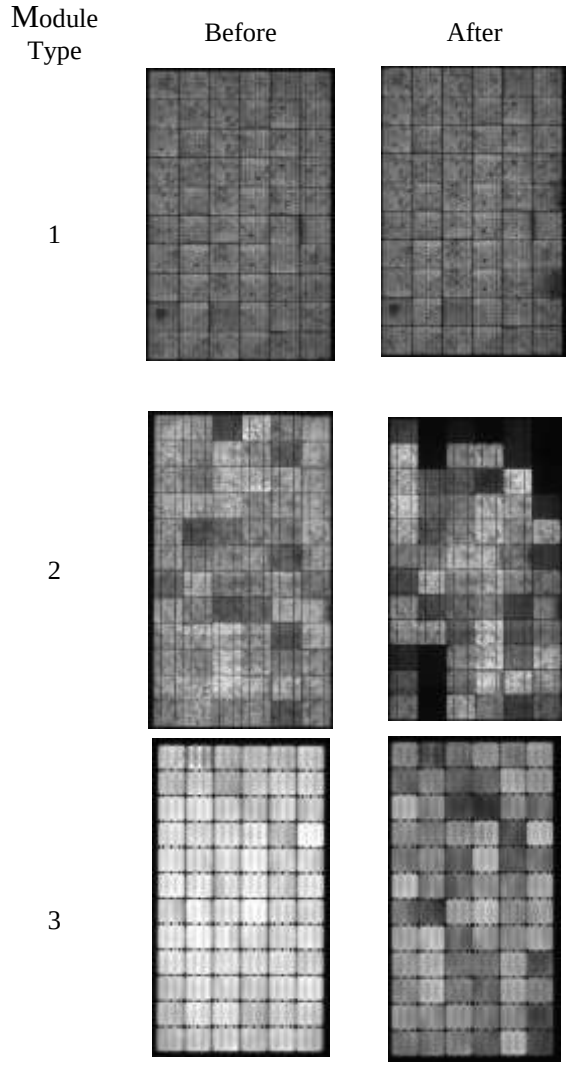


Fig. 5. Electroluminescence examples for each of the three module designs tested shown before and after stress testing in an environmental chamber at 60°C, 85% RH, -1000 V, for 96 h.

cells in this module. Depending on the module design and materials, cells, and their susceptibility, electroluminescence signatures vary greatly and degradation is not necessarily confined to the very edges of the modules with the stress protocol applied.

*B. Extraneous Effects*

The understanding of potential causes for variability in the interlaboratory study that we can control are discussed here. The initiation sequence in this work involved placing the voltage bias on the modules before ramping the temperature and humidity to the stress level. However, work of Mathiak and coworkers [11] have shown spikes in leakage current with this initiation sequence because the modules remain cooler than the chamber air temperature just after the ramp to the setpoint temperature, leading to extra humidity on the module. An outcome of this work was to propose modifying the protocol henceforth by first ramping the temperature, waiting until the module and chamber air temperatures were at setpoint (the allowable tolerance remaining at ± 2°C), then ramping up relative humidity to its setpoint, followed by a stabilization time, and then application of the system voltage bias. This additional stabilization time allows for all chamber components to reach their equilibrium.

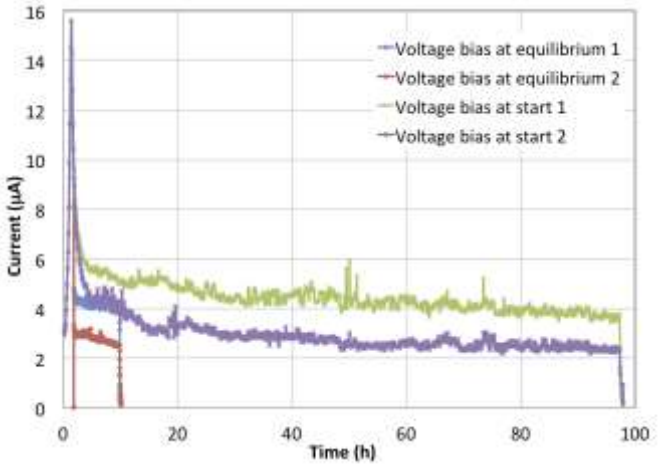


Fig. 6. Comparison of leakage current obtained with procedure used in the interlaboratory study (voltage bias at start) compared to that when voltage bias is applied to the modules after equilibrium is reached in the environmental chamber. The four example curves shown are differing modules. The modules with voltage bias applied at the start were run for 96 h according to the protocol of this study. The voltage applied when modules were at equilibrium was applied for an 8 h dwell.

Examples of the leakage-current excursions that occur when the voltage bias is applied at the start and when effects of higher-than-equilibrium humidity exist are compared to the case of voltage applied when the module temperature and surface relative humidity is already in equilibrium (Fig. 6). Although the current transient in these nonequilibrium conditions is not long in the scope of a 96 h test, it can easily be minimized and doing so will reduce an element of variation from test to test. When voltage is applied after equilibrium is reached, a much narrower current spike of less than one-minute duration can be seen.

Effects of temperature and relative humidity on leakage current have been well studied and give a quantitative feedback of the effective stress on the module. Considering the exponential dependency on temperature and super linear

dependency on relative humidity [9], it is favorable to keep the tolerances minimized for better reproducibility. IEC 60068-2-78 *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*, recommends tolerances of ± 2°C and ± 3% in RH [15], which is tighter than the tolerances set out in this interlaboratory study and that of IEC 61215 for RH (± 5% RH) [16]. All labs in this study could maintain ± 3% in RH; therefore, the recommendations of IEC 60068-2-78 would best be followed in the future to minimize variability from lab to lab.

Modules are known to recover under heat and reverse bias. Effects of illumination simultaneous to application of voltage bias have been studied in the case of polarization by SunPower, who reported that ultraviolet (UV) light will ionize electrons in the silicon nitride and effectively bleed charge and reduce the electrical potential across the nitride [17]. As such, a similar process in the case of PID in conventional cells should exist, whereby reduction in electrical potential across the nitride will reduce the electromotive force for positive ions advancing toward the silicon active layer of the cell. Further, any photoionized electrons in the antireflective coating may neutralize advancing positive charge.

One must be aware of any mitigating influence of intentional or unintentional illumination during testing to obtain reproducible results in environmental chamber tests for PID. To quantify the effects of the light in the UV region that has the potential to change degradation behavior under system voltage bias, three module designs were stress tested for PID in the chamber with and without 0.2 suns of the UV-A band illumination; Fig. 7 shows the results of the power loss versus time. Whether illuminated or not, the sample surfaces were successfully maintained at 60°C ±1°C, and 85% RH ±3%. Leakage currents monitored for the modules were about the same or greater with illumination than in the dark, indicating maintenance of the conditions for ionic transfer over the partially conductive surface of the glass, even with the illumination.

The results for the dark chamber configuration show that module types A and C are relatively less sensitive modules to system voltage stress. The degradation in these modules is completely arrested when under illumination within the timeframe under examination, about 96 h. Module type B, a more PID-sensitive design, was tested in more iterations to gain some statistical significance because greater performance spread could be seen among the samples. Type B degraded faster in the dark relative to the other designs and the degradation was not arrested by the 5 W/m$^2$ UV-A illumination—it was slowed. Reference [17] discusses how the UV light-induced shunting within the antireflective coating provides a recovery effect, which must exceed the rate of degradation in the dark to arrest polarization.

### *C. Comparison of Damp-Heat Method with Full-Face Grounding at Room Temperature*

The damp-heat chamber provides an adsorbed layer of water molecules on the glass. Depending on the nature of the glass, slight solubility of the glass in water exists [18]. A partially conductive water layer transports charge, to an extent, to the grounded module frame. Alternatively, the glass may be grounded with use of a metal (e.g., Al, Cu) foil

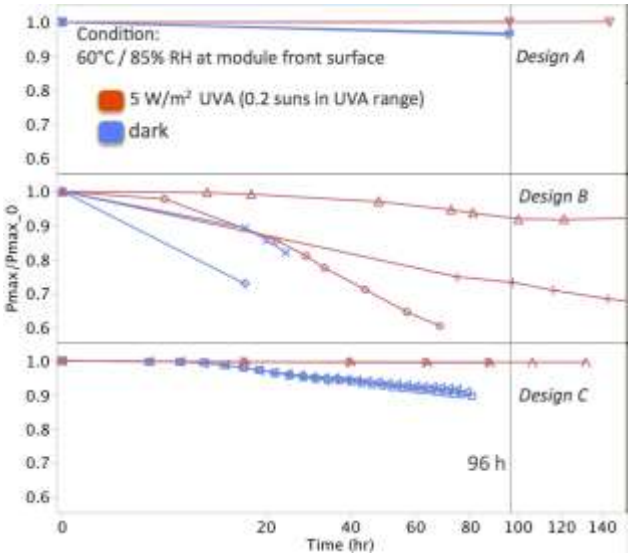


Fig. 7. Degradation of three modules with and without UV-A light irradiance in chamber at 60°C, 85% RH, and -1000 V. The 5 W/m$^2$ UV-A irradiance slows or arrests the degradation.

pressed onto it [19]. There is also motivation for using the foil method in a standardized test due to the convenience of not requiring humidity generation in precise concentrations or for grounding the entirety of the module face; so the relationship with the stress used in the interlaboratory study should be clarified.

The rate of degradation of a module design stressed at 60°C, 85% RH, and rated system voltage of -1000 V is compared to the rate of the same module design stressed at 25°C, -1000 V, and foil on the module face (Fig. 8). Two replicas (modules 3 and 4) degrade to about 0.75 of the initial power in the 60°C, 85% RH, -1000 V, and 96 h stress condition which is similar to that used in the interlab study; however, interim module power measurements were taken to clarify the degradation curve in this case. These breaks for module power testing, despite efforts to minimize their time, could influence the degradation rates.

In the first test, module 1 had the frame grounded and aluminum foil placed on the glass and the foil was weighted down with a rubber mat and wrapped around the module frame. In this case, no degradation could be seen to the extent tested, and resistance between the grounding point on the module and the foil was found to be high because of a thin insulating anodization on the Al frame. When the anodization coating was removed, where power-supply ground and frame and foil were well-connected electrically, degradation was readily observed. It is seen that unlike adsorbed water molecule layers, the foil does not penetrate for conduction to all surfaces, cavities, interfaces, and pinholes; so special care—such as pressure applied to foil to the faces and forcing conduction to all relevant module parts—is required to promote grounding to the surfaces as completely and reproducibly as possible. After better conduction to ground with aluminum foil is achieved, we find that degradation to 0.95 of the initial power occurs in a factor of 3 to 4 times longer for this module type compared to the 60°C, 85% RH, -1000 V condition applied for 96 h. Studies based on leakage

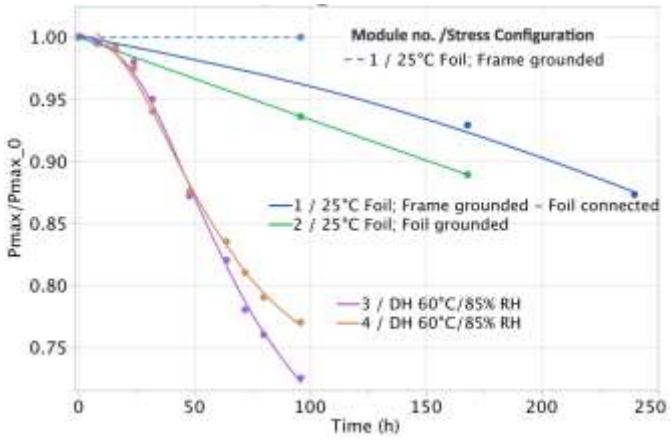


Fig. 8. Comparison of the interlaboratory stress test condition (60°C/85% RH) to the 25°C foil test. With the foil test, a boost in the PID rate is seen by abrading through the insulating coating on the frame or ensuring the foil-frame-ground, after which the Al foil method produces 3–4 times slower degradation to 5% relative degradation than the 60°C/85% RH condition.

current similarly show a factor of three difference in the rate between these conditions [20]; however, other studies show differing behavior [21]. There, the start-up sequence in damp heat that applies the system voltage on the module after the modules have come to thermal equilibrium would avoid the leakage-current pulse from the excess humidity and thus be less stressful. Different module materials, sizes, conductivities, and stacking-fault defect concentrations in the silicon could also influence the relative rates of degradation between the two test types.

## IV. Summary and Conclusions

Three module designs completed testing at five labs to compare the effects of system voltage on the durability according to a proposed test protocol. The test appears successful with respect to the scope of this interlaboratory study, with results of the three modules analyzed showing consistent pass/fail results, except for one design with mean degradation -2.12% (relative) that failed at only one lab. An analysis of variance indicated that lab-to-lab variability was the least influential variable. Considering all modules except one gross outlier, the greatest deviation in power performance difference from the mean of all labs was 2.3% (relative). The module design was the second-most influential contributor to variability in the results. The largest variability is attributed to differences measured within a given module design, with one module type degrading in the range of close to 0% to almost 30% relative. The probability of a false pass in a module type with mean degradation of 8.7% relative exhibiting the most variability in PID resistance between replicas was found to be 2.22 % considering two replicas tested. Testing more replicas or testing more frequently would further reduce the uncertainty.

Items introduced intentionally or unintentionally that affect reproducibility of results were discussed. Illumination by UV-A light was found to slow or arrest PID, similar to what has been found with polarization. Ionization in the silicon nitride may provide increased conductivity for a shunting path across the nitride antireflective coating, and the ionized electrons themselves may neutralize the advance of positive ions approaching the silicon cell.

Feedback from participants in the interlaboratory study is a critical component for debugging test protocols. Ramping to the stress temperature while avoiding excess humidity on the module and the humidity tolerance band reduction were proposed for future implementation in the test protocol. While anticipating better reproducibility, this would decrease the severity of the test because of avoidance of nonequilibrium excess moisture and reduced leakage current at the start.

A comparison of the test protocol with a 25°C foil test was performed to collect a data point on the relationship between the degradation rates. Unlike humidity, which adheres on all surfaces independent of topology, special precautions need to be made to ensure full contact between grounding point, frame, glass, and foil. With this understanding, we found three to four times the rate to 5% degradation with the 60°C, 85% RH, -1000 V condition compared to the 25°C, foil, -1000 V condition. The rates of PID associated with the test methods are expected to depend on test start-up sequence in damp heat, details of the grounding with foil, and the nature of the modules.

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