A Neodymium Based Hybrid Fault Current Limiter

by

Jay Prigmore

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved March 2013 by the
Graduate Supervisory Committee:

George Karady, Chair
Raja Ayyanar
Kory Hedman
Keith Holbert

ARIZONA STATE UNIVERSITY

May 2013

ABSTRACT

This dissertation presents a new hybrid fault current limiter (FCL) topology that is primarily intended to protect single-phase power equipment. It can however be extended to protect three phase systems but would need three devices to protect each individual phase. In comparison against the existing fault current limiter technology, the salient features of the proposed topology are: a) provides variable impedance that provides a 50% reduction in prospective fault current; b) near instantaneous response time which is within the first half cycle (1-4 ms); c) the use of semiconductor switches as the commutating switch which produces reduced leakage current, reduced losses, improved reliability, and a faster switch time (ns- μ s); d) zero losses in steady-state operation; e) use of a Neodymium (NdFeB) permanent magnet as the limiting impedance which reduces size, cost, weight, eliminates DC biasing and cooling costs; f) use of Pulse Width Modulation (PWM) to control the magnitude of the fault current to a user's desired level. g) experimental test system is developed and tested to prove the concepts of the proposed FCL. This dissertation presents the proposed topology and its working principle backed up with numerical verifications, simulation results, and hardware implementation results. Conclusions and future work are also presented.

DEDICATION

I dedicate this dissertation to my fiancée, as this dissertation would not have been completed without your constant support. You have supported me through all of the frustrations and challenges that surmounted during my time at Arizona State University. I am forever grateful and appreciate the support and encouragement throughout this whole process.

ACKNOWLEDGMENTS

First, I would like to thank my chair Dr. George Karady for his support, encouragement and suggestions. I would also like to thank the members of my Ph.D. committee Dr. Raja Ayyanar, Dr. Keith Holbert, and Dr. Kory Hedman for their support. Also, I would like to thank my fellow students at ASU and in particular my undergraduate researchers, Jorge Mendoza and Sierrah Grey, who helped work on this project.

Finally, I would also like to thank my fiancée, my family, friends, and classmates for their moral support and willingness to help throughout this process. Without you, none of this would be possible.

TABLE OF CONTENTS

	Page
LIST OF TABLES	vi
LIST OF FIGURES	vii
LIST OF SYMBOLS / NOMENCLATURE	xiii
CHAPTER	
1 INTRODUCTION AND OBJECTIVE OF THE WORK	1
Motivation	1
Objective	1
Requirements Of The FCL	3
Aim Of Present Work	4
Structure Of The Report	5
2 LITERATURE REVIEW	6
Fault Current Limiter Literature Review	6
3 INITIAL SOLID-STATE FCL DESIGN	41
Initial FCL Design	41
Operating Principle	42
Power Requirements	44
Simulation Results	49
Initial FCL Conclusion	55
4 FERROMAGNETIC MATERIAL COMPARISON	57
Hysteresis Modeling	57
Magnetic Material Design	65

CHAPTER	Page
PLECS Simulations.....	70
Conclusions	80
5 PROPOSED FCL DESIGN	81
A Neodymium Hybrid Fault Current Limiter	81
Finite Element Analysis	88
Neodymium Core Optimization	92
Conclusions	100
6 RESULTS.....	103
Simulation Results	103
Experimental Results	136
Conclusions	146
7 CONCLUSIONS AND FUTURE WORK.....	148
Conclusions	148
Contributions	150
Future Work	151
Relevant Publications.....	152
REFERENCES	154
APPENDIX	
A PLECS SIMULATIONS	158
B MICROCONTROLLER CODE	165
C AMPL CODE	177

LIST OF TABLES

Table	Page
1. Current DOE sponsored fault current limiter projects	7
2. Impedance values of DFCL with increasing current and fault current values with DFCL compared to no DFCL	11
3. Cost, weight, size comparison of new and old design for SCFCL	30
4. Parameters used in PMFCL experiment	33
5. Requirements and solutions of hybrid FCL	35
6. Parameters of initial SSFCL.....	45
7. Ferromagnetic material properties	69
8. FCL high voltage design parameters.....	70
9. Summary of magnetic material characteristics for FCL applications	79
10. Copper coil stress results.....	91
11. Ferromagnetic material input data	98
12. Optimized ferromagnetic core design results	99
13. NdFeB N52 parameters.....	104
14. Hysteresis loop logic	108
15. Statistical analysis of hybrid FCL's performance.....	122
16. Comparison of FCL results	123
17. Low voltage simulation parameters	135
18. Statistical analysis of hybrid FCL hardware	145

LIST OF FIGURES

Figure	Page
1. Responses to FCL need survey performed by CIGRE WG A3.16	3
2. Current status of DOE sponsored FCL projects	8
3. Permeability of magnetic material vs. Magnetic Field Intensity	9
4. Conventional core with random domains (left) and DFCL core with radially pre-aligned domains (right)	10
5. Incremental permeability for the DFCL as the Magnetic Field Intensity increases..	11
6. Typical semiconductor switch used in FCL applications	13
7. Conduction losses of IGBT's in an SSFCL application	14
8. Typical SCFCL configuration	17
9. Total magnetic decoupling configuration	17
10. Partial magnetic decoupling configuration	18
11. Open-core configuration	18
12. Two-core SCFCL configuration for single phase applications	19
13. A three-leg core for SCFCL applications	20
14. Flux distribution in a three-leg core	20
15. SCFCL with a common core and trifilar windings	21
16. Test circuit for SCFCL with common core and trifilar windings	22
17. Prototype of 10kV SCFCL with common core and trifilar windings	22
18. DC circuit for SCFCL with trifilar windings	23
19. Fault current induced into the DC bias system	23
20. SLG fault for SCFCL with trifilar windings	24

Figure	Page
21. Two phase to ground fault.....	24
22. Three phase to ground fault.....	25
23. Concept diagram of Zenergy Power's SCFCL	26
24. Zenergy Power's SCFCL graphic representation	26
25. Installation of Zenergy Power's SCFCL	27
26. Full-load and steady-state fault test.....	27
27. 82 cycle fault endurance test	28
28. Double-fault sequence test which simulates re-closer operation.....	29
29. New compact design of the SCFCL.....	30
30. PMFCL configuration with steel core.....	31
31. Series connected PMFCL topology	32
32. Parallel connected PMFCL topology	32
33. Prototype model of PMFCL.....	33
34. Limited and prospective fault current in PMFCL.....	34
35. Schematic of hybrid FCL with superconducting limiter	36
36. Experimental results of hybrid FCL with superconducting limiter.....	36
37. AC hybrid FCL with semiconductors	37
38. Operation of hybrid FCL in fault limitation mode	38
39. Initial SSFCL design	41
40. Steps taken to find equivalent impedance of proposed limiter.....	46
41. Displays the prospective fault current and overvoltage in the system without the proposed device.....	50

Figure	Page
42. Zoomed in version of Figure 41	51
43. Displays the proposed FCL during normal operation and fault operation.....	52
44. Displays a zoomed in version of Figure 43	52
45. Worst-case scenario of Figure 43 at negative peak current.....	54
46. PWM signal for each SiC MOSFET.....	54
47. Energy dissipated by initial FCL.....	55
48. Depiction of the Preisach Relay Hysteron	58
49. Preisach Plane.....	59
50. Simulation flowchart for Preisach method	60
51. Simulation flowchart for Jiles-Atherton method	65
52. Ferromagnetic core design and casing.....	67
53. NdFeB and SmCo core design	69
54. Line voltage (top) and prospective fault current without FCL (bottom).....	71
55. Voltage across the FCL (top) and limited fault current with a laminated steel core (bottom).....	72
56. Hysteresis curve obtained in the simulation for a laminated steel core using the Preisach model	73
57. Voltage across the FCL (top) and limited fault current with an AlNiCo core (bottom).....	74
58. Hysteresis curve obtained in the simulation for an AlNiCo core using the Preisach model	75
59. Voltage across the FCL (top) and limited fault current with a SmCo core (bottom)	76

Figure	Page
60. Hysteresis curve obtained in the simulation for a SmCo core using the Preisach model	77
61. Voltage across the FCL (top) and limited fault current with an NdFeB core (bottom)	78
62. Hysteresis curve obtained in the simulation of an NdFeB-N42 core using the Preisach model	79
63. Proposed Hybrid FCL	81
64. Simulated stress subjected to the 0 AWG wire during fault limitation mode	90
65. PSCAD model of proposed hybrid FCL	103
66. PSCAD model of NdFeB core	104
67. PSCAD inductance calculation	105
68. Jiles-Atherton hysteresis method implemented in PSCAD	106
69. Hysteresis loop controller	107
70. Fault detection algorithm of the controller	109
71. Step 2 and 3 of the control algorithm	110
72. Step 4 of the control algorithm	111
73. Step 5 of the control algorithm	112
74. Control algorithm implemented in PSCAD	113
75. Prospective fault current	114
76. Zoomed in version of Figure 74	114
77. Limited fault current and voltage with FCL	115
78. Zoomed in version of Figure 76	116

Figure	Page
79. Initial switching of the proposed FCL	117
80. Switching state of proposed FCL	118
81. Fault detection algorithm.....	119
82. Zoomed in version of Figure 81	119
83. Hysteresis curve of the NdFeB core.....	121
84. Reference sinusoidal wave for PWM technique.....	124
85. Updated controller algorithm to include PWM	125
86. Worst-case prospective fault current.....	126
87. Maximum limitation scenario for PWM.....	126
88. 15 kA controlled fault current scenario.....	127
89. Zoomed in version of Figure 88.....	128
90. Semiconductor switch current for the 15 kA scenario.....	128
91. PWM signal for the 15 kA scenario.....	129
92. Total harmonic distortion for the 15 kA scenario.....	129
93. 22.5 kA controlled fault current scenario.....	130
94. Zoomed in version of Figure 93	131
95. Semiconductor current for the 22.5 kA scenario	131
96. PWM signal for the 22.5 kA scenario.....	132
97. Total harmonic distortion for the 22.5 kA scenario.....	132
98. Current and voltage for the 30 kA scenario	133
99. PWM signal for the 30 kA scenario.....	133
100. Semiconductor current for the 30 kA scenario	134

Figure	Page
101. Total harmonic distortion for the 30 kA scenario.....	134
102. Low voltage simulation results	135
103. Low voltage NdFeb core design	137
104. Hardware test system setup	138
105. FCL operation for a current zero crossing fault inception angle.....	140
106. FCL operation for a positive peak current fault inception angle.....	141
107. FCL operation for a negative peak current fault inception angle.....	142
108. FCL transition from fault limitation mode to normal operation mode.....	143
109. PLECS simulation of FCL	159
110. PLECS simulation of magnetic materials.....	160

LIST OF SYMBOLS

Symbol	Page
1. T_C – Curie Temperature	14
2. ϕ_{knee} – Flux at knee of hysteresis curve	16
3. V_{LL} – Line to Line Voltage	41
4. R_{line} – Line resistance.....	41
5. X_{line} – Line reactance	41
6. T_{ON} – On period per cycle.....	42
7. T - Period	42
8. R_{TC} – Transient resistor	42
9. I_{pu} – Per unit current	44
10. Z_{EQ} – Capacitor and MOV equivalent impedance	44
11. R'_C - Equivalent resistance of Capacitor and MOV	44
12. X'_C - Equivalent reactance of Capacitor and MOV	44
13. X_{CSLim} - Parallel reactance of capacitor and MOV.....	44
14. V_{RMS} – Root-mean-square Voltage.....	45
15. $Z_{Positive}$ - Positive cycle impedance.....	46
16. $Z_{Negative}$ - Negative cycle impedance.....	46
17. X_{Lim} - Initial FCL reactance.....	46
18. R_{Lim} - Initial FCL resistance	46
19. $Z_{Limiter}$ – Equivalent FCL impedance	46
20. $Z_{Snubber}$ - Snubber impedance	46
21. i_{sc} - Short-circuit line current without FCL	47

Symbol	Page
22. V_{smax} – Maximum sinusoidal voltage.....	47
23. θ_{line} - Line phase angle	47
24. I_{Tfault} - Current value at time fault occurs	47
25. T_{fault} – Time of fault inception	47
26. τ_{line} - Time constant of the line	47
27. i_{lim} - Limited fault current	47
28. θ_{lim} - Phase angle with limiter inserted.....	47
29. T_{del} - Detection time of initial FCL controller	47
30. τ_{lim} - Time constant with initial FCL	47
31. E_{FCL} - Energy of initial FCL	48
32. t - Simulation time	49
33. E_{1cycle} - First cycle energy dissipated by initial FCL	55
34. $\frac{di}{dt}$ – Rate of change of the current	55
35. $\frac{dv}{dt}$ – Rate of change of the voltage	55
36. H_c – Magnetic field coercivity	58
37. H – Magnetic field strength.....	58
38. $\gamma_{\alpha\beta}$ - Elementary Preisach hysteron	58
39. α - Limit for Preisach hysteron	58
40. β - Limit for Preisach hysteron	58
41. $B(H)$ – Magnetic flux density.....	58
42. $\mu(\alpha, \beta)$ - Preisach distribution function.....	58

Symbol	Page
43. S – Preisach plane	58
44. α_J - Mean field parameter for Jiles-Atherton method	61
45. B_{sat} - Saturation flux density	61
46. μ_0 - Permeability of free space	61
47. $\frac{dB}{dH}$ - Instantaneous magnetic core permeability for Jiles-Atherton.....	62
48. $\mu_{core}(B, H)$ - Instantaneous magnetic core permeability.....	63
49. $\frac{\Delta B}{\Delta H}$ - Instantaneous magnetic core permeability for Preisach	63
50. L- Inductance	63
51. Ψ - Flux linkage.....	63
52. N- Number of turns	63
53. Φ_B - Magnetic flux.....	63
54. A_{core} - Cross-sectional area of magnetic core.....	64
55. l_{mean} - Mean path length	64
56. L_{coil} - Length of coil.....	64
57. Φ_{avg} - Averager flux per cycle.....	68
58. B_{pk} – Peak flux density	68
59. f - Frequency.....	68
60. B_{rem} - Remanence flux density.....	69
61. H_{sat} - Saturation magnetic field strength.....	69
62. ρ - Electrical resistivity	69
63. V_{LN} – Line to Neutral voltage	70

Symbol	Page
64. I_n – Nominal current	70
65. I_{sc} – Potential peak fault current	70
66. I_{sc_ss} – Potential steady-state fault current	70
67. t_{FCL} – Maximum FCL duration	70
68. PR – Percent reduction of fault current	70
69. I_{Lim_LS} – Laminated steel limited peak fault current	72
70. $I_{Lim\_LS\_SS}$ – Laminated steel limited steady-state fault current	72
71. I_{Lim_AL} – AlNiCo limited peak fault current	74
72. $I_{Lim\_AL\_SS}$ – AlNiCo limited steady-state fault current	74
73. I_{Lim_SmCo} – SmCo limited peak fault current	76
74. $I_{Lim\_SmCo\_SS}$ – SmCo limited steady-state fault current	76
75. I_{Lim_NdFeB} – NdFeB limited peak fault current	78
76. $I_{Lim\_NdFeB\_SS}$ – NdFeB limited steady-state fault current	78
77. V_{FCL} – Voltage across the FCL	79
78. M_1 – Arbitrary threshold value for current magnitude	86
79. M_2 – Arbitrary threshold value for slope of current	86
80. I_{Mech} – Current in the fast mechanical contact switch	87
81. I_{Semi} – Current in the semiconductor switch	87
82. F_{radial} – Mean radial force	89
83. D – Mean diameter of copper coils	89
84. h – Height of the copper coils	89

Symbol	Page
85. σ_{radial} - Maximum tensile strength of copper.....	89
86. A_{wind} - Cross-sectional area of copper wire.....	89
87. F_{axial} - Mean axial force	89
88. h_{eff} - Effective height or distance between core legs.....	89
89. σ_{axial} - Mean stress due to axial forces in copper wire.....	89
90. l_{coil} – Distance between the coils	89
91. t_{coil} - Radial dimension of the coil	89
92. P_n - Price of ferromagnetic material.....	93
93. n - Indice of ferromagnetic material dimensions.....	93
94. Mag_n - Number of magnets.....	93
95. GP_n - Price of wire gauge selected	93
96. $wirelength_n$ - Length of wire for number of turns.....	93
97. $numlength_n$ - Number of cores needed for length	93
98. $hcore_n$ - Height of optimized core	93
99. $length_n$ - Length of individual core.....	93
100. $numwidth_n$ - Number of cores for width.....	93
101. $numheight_n$ - Number of cores for height.....	93
102. $height_n$ - Height of an individual core	93
103. $lcore_n$ - Length of optimized core.....	93
104. $wcore_n$ - Width of optimized core	93
105. $width_n$ - Width of an individual core.....	93
106. $Acore_n$ - Cross-sectional area of optimized core	93

Symbol	Page
107. $lmean_n$ - Mean path length of optimized core.....	93
108. g - Indices of wire gauges	95
109. $Gaugenum$ - Number of gauges in AWG input table.....	95
110. $GaugeAmpacity_g$ - Amperage rating for AWG sizes.....	95
111. $wirediameter$ - Diameter of selected wire size	95
112. $diameter_g$ - Diameters for all AWG wire sizes	95
113. $Gauge$ - Selected AWG wire size	95
114. $Gaugesize_n$ - Gauge size in AWG input table.....	95
115. $wireres_n$ - Resistance of selected wire size.....	95
116. $GaugeRes_g$ - Gauge resistance in AWG input table	95
117. N_n - Number of turns for optimized core.....	95
118. Isc_new_n - New limited peak fault current.....	96
119. Iss_new_n - New limited steady-state fault current.....	96
120. $PRsc_n$ - Peak fault current percent reduction achieved.....	96
121. $PRss_n$ - Steady-state fault current percent reduction acheived.....	96
122. $PRmin_n$ - Minimum desired percent reduction	96
123. H_{hys} - Current hysteretic applied field strength value.....	108

Chapter 1

INTRODUCTION AND OBJECTIVE OF THE WORK

I. Motivation

The motivation behind this project is to help protect power systems from potential damaging fault current. With renewables being increasingly incorporated into the grid, the prospective fault current increases to ranges that the current protection schemes may not be able to handle, thus causing catastrophic damages to components in the line. As transitions to a “smarter” grid are constantly occurring, the old protection schemes will either need to be upgraded (very expensive) or supplemented. The idea behind this project is to create a Fault Current Limiter (FCL) to limit the prospective fault current to levels where the existing protection can operate as fault current magnitudes rise more due to distributed generation being added to the system. Some constraints considered in the development of the proposed system in Chapter 3 is size, weight, maintenance, initial cost, re-occurring cost, reliability, energy handling capability, fast response and low losses during normal operation. This will allow for the existing protection schemes to operate accordingly without the need for upgrades. The most important benefit of a FCL in utility systems is the possibility to upgrade the electric grid to higher transmission capabilities while maintaining existing fault current limits for transformers and circuit breakers [1].

II. Objective

The objective of the work is to find a solution to limit the prospective fault current to acceptable values for a maximum of 60 cycles or until an existing circuit breaker can interrupt the fault. The constraints and criteria required for the design are discussed in the

section below as there are no standards yet for FCLs even they are being developed by CIGRE [2]. Another objective of the work would be to help optimize the physical design of the core for the cheapest cost while maintaining a maximum inductance needed by the desired level of fault limitation. The FCL will be designed for distribution level (7.2 kV) and could be extended to transmission level systems. Lower level systems do not require the speed of interruption or limitation that the medium and high voltage levels need [1].

A. Necessity of fault current limiters in today's power grid

In an ever-expanding Power Grid that has increasing power demand, the transmission and distribution lines must transfer greater power than ever before. This creates line overloading and higher fault current during a fault, which can be disastrous since the grid was built and designed in the United States for a load during that time period. Thus, to alleviate the fault, higher rated circuit breakers will be needed to interrupt the increased fault current. Although upgrading the equipment can relieve some of these problems, the upgrades are usually too expensive and impractical because the increasing demand will outpace the upgrades capability and would result in further upgrades. Other solutions such as construction of new substations, bus splitting, current limiting reactors, high impedance transformers, sequential breaker tripping are found to be either a compromise of the cost or the reliability of the system [3]. Thus, the development of a device that does not compromise on the cost of upgrades or the reliability of the system and is economically feasible warrants the development of a fault current limiter. The questions that need to be answered are what type of fault current limiter is best for a specific situation and what requirements are needed of the FCL to insure as small of an impact on other equipment as possible. In a recent survey sent to utility companies by the CIGRE WG A3.16

(working group for FCL testing standards), 26% of the answers indicated no need for fault current limitation while 47% indicated a need without restrictions for Medium Voltage (MV) networks and 21% for High Voltage (HV) networks [4]. The rest of the responses (10% for MV and 6% for HV) are characterized by a need for FCLs with restrictions or comments such as costs and reliability. Figure 1 graphically displays the Utility's representative responses for need of a FCL.

Figure 1 – Responses to FCL need survey performed by CIGRE WG A3.16 [4].

III. Requirements Of The FCL

The limited fault current must be a sinusoidal waveform and the detection of the fault must be determined as fast as possible but ideally within 4 ms. The individual components of the FCL must be able to withstand the power requirements placed upon them during fault operation. The FCL must also operate for at least 60 cycles without being destroyed. Another requirement is the cost of the proposed device must be kept well below the cost of upgrading a circuit breaker or other system components. Circuit breaker

upgrades are expensive, as there is the cost of a new circuit breaker and an additional cost of the line being out of service while the upgrades are performed. The pricing goal for producing the FCL should be less than the cost of the purchasing price of a few capable circuit breakers. Due to these constraints, the most feasible solution for fault current limitation at the power level is a hybrid FCL that has non-linear impedance during fault operation but negligible impedance during normal operation. Also, location of the FCL is crucial, otherwise the relay's algorithm may miss-interpret the additional impedance caused by the FCL as part of the line impedance. If the FCL were placed in between the PT and relay, this could place the fault outside of the particular relay's protection zone [5]. However, if the FCL is placed outside of the PT and the relay, the relay is properly able to determine the fault line and trips the breaker accordingly. Therefore, the FCL will need to be placed in the optimal location in the system. The proposed hybrid topology is described in the Chapter 5.

IV. Aim Of The Present Work

In this comprehensive exam, a new FCL topology is presented. A hybrid topology is discussed as a more robust solution to the increased fault current problem currently being experienced by utilities and will be investigated in the next chapters. The hybrid system will include a new concept using a Neodymium (NdFeB) permanent magnet as the limiting impedance as well as a novel controller to control this new conceptual system. Finite Element Analysis is performed to determine the minimum wire gauge needed in this design. A custom casing is designed to physically hold the NdFeB magnets in place once assembled. The specific operating characteristics are presented and as well as the

simulation results. The ferromagnetic properties of the NdFeB core are shown to be modeled accurately and the simulations demonstrate the feasibility of the proposed design.

V. Structure Of The Report

This report is structured as follows:

- In Chapter 1, the motivation and the objective of the work are presented.
- In Chapter 2, the literature review of Fault Current Limiters is presented.
- In Chapter 3, an initial power electronic based FCL design is briefly discussed and determined to be infeasible due to cost objective.
- In Chapter 4, numerous ferromagnetic materials are presented and analyzed for possibilities of the magnetic core in the proposed FCL design and Neodymium (NdFeB) is chosen as the most suitable core material.
- In Chapter 5, a description of the proposed hybrid FCL and its operating principle as well as Finite Element Analysis on the copper coil windings.
- In Chapter 6, the simulation results are presented for the full 7.2 kV model in PSCAD.
- In Chapter 7, conclusions and future work are presented such as the low voltage hardware experimental results, the finalization of the core optimization program and possible inclusion into the FREEDM system.

Chapter 2

LITERATURE REVIEW

I. Fault Current Limiter Literature Review

A Fault Current Limiter (FCL) is a device that can limit excess current when a fault occurs. FCLs offer condition-based increase in impedance (resistive and/or reactive) between normal conducting mode and current limiting mode. The objective is to limit the prospective fault current (peak and RMS) to a desired but safe value. The safe value is typically higher than the nominal current value but less than the maximum operating value of protection devices such as circuit breakers (CB). By limiting the prospective fault current within these ranges, the CB's and relays can operate without a change in their coordination settings. There can be added functions incorporated in the device such as current interruption and current isolation. Various types of fault current limiters are being developed; the most common are Superconducting (SFCL), Solid State (SSFCL) and Saturated Iron-Core (SCFCL). The Department of Energy (DOE) has several sponsored projects to determine which is the most applicable for the cheapest cost. The current FCL projects are shown below in Table 1 [1].

Table 1 – Current DOE sponsored fault current limiter projects.

Specification	American Superconductor	Silicon Power	SuperPower	Zenergy (formerly SC Power Systems)
Name	Super Limiter™	Solid-State Current Limiter	Superconducting Fault Current Limiter (SFCL)	Fault Current Controller (FCC)
Installed Location for Device	- First HV component testing December 2008 - Commissioning at SCE in 2012	Design verification testing in 2Q09 at Test Lab	Plan to install and test at AEP's TIDD substation in Ohio	Plan to install and test in a utility grid, currently negotiating with a major utility. Separate project with California Energy Commission will test a similar 15-kV class FCL with SCE.
Design	- Resistive FCL 3-phase, transmission level voltage - Low-inductance bifilar coil switching module technology using 2G wire	Uses high power semiconductors Super-gate turn-off thyristor (SGTO)	- Resistive FCL - Matrix design has parallel, 2G HTS elements and conventional coils	- DC-based iron core - One DC first-generation HTS coil for a three-phase AC FCL - Saturable reactor-type FCL - Suitable for 2G materials, when available
Ratings (final design)	Voltage: 138 kV, 2000 A Class 115 kV, 1200 A at SCE site	Voltage: 69 kV Amps: 1,000 A	Voltage: 138 kV Amps: 1200 A	Targeting a three-phase transmission-level device at: Voltage: 138 kV Amps: 2,000 to 4,000 steady-state
Fault Current Reduction	20–50% Reduction – 37 % at SCE (63 kA to 40 kA)	50%-60% reduction	20%–50% reduction	20% to 40% reduction of a 60 kA to 80 kA fault
Testing Protocol Basis	Cable, Transformer	Transformer, Reactor, and Circuit Breaker	Transformer, Reactor, and Circuit Breaker	Transformer and Series Reactor

The typical fault reduction is as low as 20% and as high as 60% as seen in Table 1. Most of the sponsored projects are 3 phase designs but single-phase designs are also applicable. As shown in Table 1, different testing procedures are being performed on each of the FCLs. Some uncommon limiters are inductive, variable resistive and electro-dynamic. Presently, the current status of the DOE supported FCL projects are displayed below in Figure 2.

Figure 2 – Current status of DOE sponsored FCL projects [1].

Figure 2 shows only a few FCLs such as Superconducting, Saturable Iron Core, Solid-State and Hybrid topologies are being developed and tested in industry today. They are also only in the beginning testing phases and yet to have been developed for the full-scale model in a transmission system. Thus, the current technology is only available for distribution levels and testing facilities can only provide adequate testing for such levels [1]. The types of FCLs to be discussed are listed below:

- 1) Electromagnetic Dynamic
- 2) Solid-State
- 3) Superconductive
- 4) Saturable Iron Core
- 5) Hybrid

A. Electromagnetic Dynamic FCL

An Electromagnetic Dynamic Fault Current Limiter (DFCL) is designed to automatically and instantaneously adjust its impedance according to the magnitude of the fault current. This limits the current to a narrow range of values regardless of the magnitude of the fault current. The DFCL operates within 8 ms for 60 Hz to effectively protect equipment and it operates at ambient temperature; therefore, requiring no cooling system once the fault has been cleared [6]. The DFCL is called “dynamic” because the impedance varies with the current magnitude. The DFCL works on the principle of varying inductance and inductive reactance of a coil wound on a core which has magnetic permeability proportional to the magneto motive force (MMF) impressed on the magnetic circuit [6]. This creates a direct proportionality between the current passing through the coil and the reactance caused by an incremental permeability. Figure 3 shows the operating zone of the permeability of the magnet with respect to magnetic field intensity (H).

Figure 3 - Permeability of magnetic material vs. Magnetic Field Intensity [6].

The inductive reactance will be constant in the linear zone of μ_r (permeability) and will decrease with saturation. The DFCL has low impedance in normal operating

conditions and once the current starts to rise, the impedance of the DFCL rises along with it to limit the current effectively. Figure 4 shows a physical property of the core material used in the DFCL. It has radially pre-aligned magnetic domains in the inward and outward directions compared to more conventional cores with random magnetic domain alignment [6].

Figure 4 - Conventional core with random domains (left) and DFCL core with radially pre-aligned domains (right) [6].

Having the magnetic domains pre-aligned in the radial direction results in low permeability for lower currents, medium permeability for medium currents and high permeability for high currents. The domains do not rotate or grow for lower MMF since they are already pre-aligned and the MMF impressed by the coil is in a circumferential direction [6]. Also, the flux per unit current (Φ/I) is low for low currents and increases as the current increases. Figure 5 shows the incremental permeability for the DFCL.

Figure 5 - Incremental permeability for the DFCL as the Magnetic Field Intensity increases [6].

The effect of the DFCL on limiting fault currents is shown in Table 2. All values are per unit quantities and the DFCL meets or exceeds current SFCL limiting effects. The varying impedance of the DFCL is shown relative to the varying current flowing through the device.

Table 2 - Impedance values of DFCL with increasing current and fault current values with DFCL compared to no DFCL [6].

All values are in p.u.

Impedance of Fault	Impedance of DFCL	Fault currents in p.u. (source impedance 0.1 p.u., line impedance 0.05 p.u.)						Fault currents with No DFCL or inductor
		DFCL	Impedance of fixed inductor with / without Superconducting switch					
			0.07	0.15	0.20	0.25	0.30	
0.00	0.4	1.82	4.55	3.33	2.86	2.50	2.22	6.67
0.20	0.3	1.54	2.38	2.00	1.82	1.67	1.54	2.86
0.30	0.25	1.43	1.92	1.67	1.54	1.43	1.33	2.22
0.40	0.18	1.37	1.61	1.43	1.33	1.25	1.18	1.82
0.50	0.1	1.33	1.39	1.25	1.18	1.11	1.05	1.54

1. Values of other components taken for above calculations are: Source impedance = 0.1 pu, Line impedance = 0.05 pu, Source voltage=1 pu

2. Bold face numbers represent unsafe values.

As shown in Table 2, the DFCL limits the fault current within a specific range due to its varying impedance property. With a 0.4 p.u. impedance of the DFCL, the fault current through the DFCL is 1.82 p.u. compared to a fault current of 6.67 p.u. without the DFCL. With a fault impedance of 0.4 p.u., the DFCL only needs to provide a 0.1 p.u. impedance into the circuit to achieve its limiting effect. It limits the fault current to 1.33 p.u., in comparison to no DFCL fault current of 1.54 p.u. Therefore, the DFCL operates as planned by limiting short-circuit current within a range of values by applying a varying impedance that corresponds to the magnitude of the current. A shortcoming of this device is that it can only limit fault currents for 3 seconds and then the device will breakdown. The unsafe values referenced in Table 2, refer to the devices in the system being destroyed due to the high fault current.

B. Solid-State FCL

An FCL developed using solid-state devices provides an advantage of producing repeated switching patterns so that on occurrence of a fault, the fault current is always limited to a predetermined level. The operation of SSFCLs utilize the switching of semiconductors for the condition based impedance [7]. The semiconductors will force the current to go through impedance during fault current limitation mode to limit the peak and RMS fault currents. However, the semiconductors must be able to withstand the overvoltage placed upon them during limitation mode otherwise the material properties will break down and controllability will be lost [8]. Generally, a Metal Oxide Varistor (MOV) is used to protect the semiconductors from the overvoltage. A typical configuration of a power semiconductor switch used in FCL applications is shown below in Figure 6.

Figure 6 – Typical semiconductor switch used in FCL applications [8].

In Figure 6, two semiconductors are connected in series by both of their emitter terminals. The advantage of connecting them in this configuration is the need for only one gate driver. If the semiconductors were connected in anti-parallel they would need separate gate drivers for each module, which would further increase costs. The MOV shown in Figure 6 provides the overvoltage support for the semiconductors. Also, the capacitance shown limits the di/dt and dv/dt times of the semiconductors to avoid breakdown [9]. One disadvantage with SSFCLs is the introduction of harmonics into the system [10]. These harmonics are typically of 3rd and 5th order, which could potentially disrupt the protection systems already in the line. Since, the semiconductors will be gated ON during normal operation; switching losses are not of much concern unlike in inverter/converter applications. Thus the conduction losses are far more important in choosing the semiconductor switch.

Figure 7 – Conduction losses of IGBT's in an SSFCL application [8].

With the introduction of Silicon Carbide devices into the market, the conduction losses are reduced which makes SSFCLs more attractive of a solution. Another issue with SSFCLs is the gate driver is floating which means the gate driver circuit will need high side isolation from the potential fault currents. Otherwise, the fault current could reach the gate drive circuit of the semiconductors and destroy it. The worst-case scenario would be realized by having no control of the semiconductor devices during fault current limitation mode.

C. Superconductive FCL

Superconducting FCLs offer almost zero impedance in the line under normal operating conditions. In the event of a fault, the superconducting material introduces large impedance into the circuit, which limits the sharp rise of fault current. The superconductor achieves this impedance by being heated up due to the excess current and once it reaches the critical temperature (T_C) of the given superconductor, a 2nd order phase transition occurs in the superconducting material and the impedance is inserted into the line.

The heating is caused by the I^2R losses. However, once the fault subsides, the superconductor needs to be cooled down by an outside source below its critical temperature; otherwise the impedance will stay in the circuit due to the critical temperature being well below room temperature at 78 degrees Fahrenheit and will result in unnecessary losses. There are low temperature superconductors whose critical temperature resides a few degrees above absolute zero and requires liquid helium as the cooling mechanism. Liquid helium is inherently expensive which makes the low temperature SFCL unfeasible. This has led to the development of high temperature superconductors that have a critical temperature that can be cooled by liquid nitrogen, thus making them cheaper and more attractive as an FCL. This aspect alone has kept them as a frontrunner for an FCL.

Yttrium Barium Copper Oxide (YBCO) superconductors have improved in their production progress and have reduced costs but has mostly been abandoned in FCL applications due to manufacturing the superconductors are still too expensive [7]. YBCO conductors have a disadvantage of different quench properties due to the critical current density and the higher n -value associated with superconductors. This results in a higher electric field with increased current which results in less sensitive quench time with respect to the di/dt time of the fault current [7]. However, a new advancement in superconducting technology for FCL applications is the introduction of Magnesium Diboride (MgB_2) superconductors [7]. The major advantage of MgB_2 is cost; the expected cost used for superconducting material in FCL applications will be reduced. The disadvantage of MgB_2 is its critical temperature of 39 K [7]. Thus liquid Neon (LNe_2) is needed to cool down the superconductor below its critical temperature instead of the standard liquid Ni-

trogen (LN₂). Superconductors in FCL applications are primarily used in Saturable Iron Core FCLs as a way to reduce losses during normal operation of the FCL.

D. Saturable-Core FCL

Saturable Iron Core FCLs (SCFCL) involve saturating the iron core above the ϕ_{knee} of the hysteresis curve in a ferromagnetic material; which is the point where the inductance produced by the iron core is negligible. This point corresponds to the upper right corner of the B-H curve which will be further explained in the Preisach and Jiles-Atherton methods of hysteresis in Chapter 4. The most important advantage of SCFCLs is that the core saturation effect makes the FCL inherently react to a fault [11]. Saturable Iron Core FCL's can be further divided into the method of saturating the Iron Cores; Superconducting biased FCLs and Permanent Magnet biased FCLs.

a. Superconducting Biased

The superconducting biased SCFCL operates such that a separate DC bias system is used to create a flux in the iron core that biases the core into saturation. Biasing the core into saturation gives a low value of relative permeability (μ_r) which results in negligible impedance introduced in the line. Also, after a fault clears the FCL is saturated again because the DC bias system is still operating and instantaneously re-saturates the core. One configuration of a SCFCL is shown in Figure 8

Figure 8 – Typical SCFCL configuration [11].

The drawback to the configuration in Figure 8 is the overvoltage induced across the DC winding [12]. Since both the DC winding and AC winding share the same magnetic flux path and the DC winding usually has a larger number of turns, an overvoltage is induced across it. A solution to the DC winding over voltage is found in Figure 9 by decoupling the DC and AC magnetic flux paths [11].

Figure 9 – Total magnetic decoupling configuration [11].

This inherently causes different legs in the core to be saturated at different levels. The advantage of this configuration is there is low overvoltage in the DC winding but the core size would need to be increased to keep the core in saturation because the nominal AC current could take the core out of saturation [11].

Figure 10 – Partial magnetic decoupling configuration [11].

The configuration in Figure 10 only partially decouples the AC and DC winding so it results in an overvoltage across the DC winding, however this overvoltage is proportional to the AC and DC number of windings. This configuration is an average of the previous two configurations. In Figure 11, the DC winding saturates the core and the winding sees a closed magnetic path.

Figure 11 – Open-core configuration [11].

The SCFCL operates by the AC winding alternatively taking one of the legs of the core in and out of saturation to restrain the fault current [11]. The disadvantage in Figure 11 is the AC winding requires a higher number of turns to produce the same inductance value for fault limitation than in Figure 8. Also, Figure 11 has the highest AC resistance of the presented configurations, which would result in more losses during normal operation.

A two-core configuration of an SCFCL designed for a single phase is shown in Figure 12 [13].

Figure 12 – Two-core SCFCL configuration for single phase applications [13].

In Figure 12, the core operates by saturating both of the cores using the same DC bias system. When a fault occurs, each core limits one half of the AC sinusoidal fault current. Therefore for each half-cycle, core 1 is being brought out of saturation while core 2 is being saturated. For the next half-cycle, the opposite occurs; core 1 is being saturated while core 2 is being brought out of saturation. As previously stated, an overvoltage is induced in the DC bias system, which can produce a large current in the DC system. Therefore, protection or controllability of the DC system is needed [13]. One method of protecting the DC system is to introduce a power semiconductor to be gated ON during normal operation and gated OFF during fault limitation mode but this would require an external controller and fault detection methods. Also, the semiconductor would need to be rated for the overvoltage placed upon it during fault limitation mode and must be able to handle the switching transients.

A three-leg SCFCL is introduced in Figure 13. The three-leg core is used in single-phase applications and typically the wires used in the DC winding are superconducting wires. The superconducting wires produce fewer losses during normal operation. The

AC windings are wired in magnetically opposite directions to limit the full sinusoidal waveform.

Figure 13 – A three-leg core for SCFCL applications [13].

Figure 14 shows the flux distribution in a three-leg core. The DC flux biases both outer legs into saturation so there is very small but negligible impedance in the line during normal operation. Since the AC flux goes through the middle leg, the DC winding overvoltage is reduced. Furthermore, the gap insertion allows for a reduction in material needed to build the core but as the gap increases, the number of DC winding turns is increased [13].

Figure 14 – Flux distribution in a three-leg core [13].

Therefore, a compromise is needed to determine the optimal gap length and DC winding turns. However, the reduction in magnetic material is still the most important design parameter. One way to further reduce the magnetic material is to eliminate the

middle leg of the three-leg core design. In doing so, results in increased peak fault current thus diminishing the limiting ability of the FCL [13].

A new design of an SCFCL has recently been introduced that will reduce the magnetic material needed to 33% of its original value. The design introduces trifilar windings and a common core [14]. The configuration is displayed in Figure 15.

Figure 15 – SCFCL with a common core and trifilar windings [14].

The configuration in Figure 15 uses only one saturable core for all three phases. To achieve this, trifilar windings are wrapped around the core. The windings are wrapped in sequential order by a-phase, b-phase, and c-phase. By being wrapped in sequential order, the fluxes from each phase cancel each other out during normal operation. The DC bias system could be removed if the phases were completely symmetrical which would give a zero flux [14]. However, the DC windings are needed to drive the core into saturation because of asymmetry in the network. One advantage of this configuration is the reduction of the number of DC turns needed to bias the core into saturation. Another advantage of placing all three phases on one core is the magnetic coupling is improved which results in reduction of stored magnetic energy due to phase currents [14]. Since the inductance of the SCFCL is proportional to the stored magnetic energy the nominal line

impedance is practically non-existent. The windings used are made of XLPE aluminum MV cables and they are designed to provide enough dielectric insulation between the individual phases [14]. The prototype is built for a 10kV/6.8MVA network with a 400 A nominal current. The network configuration and testing setup is shown in Figure 16 and Figure 17 [14].

Figure 16 – Test circuit for SCFCL with common core and trifilar windings [14].

Figure 17 – Prototype of 10kV SCFCL with common core and trifilar windings [14].

The FCL is inserted in series in the line with opposite magnetically wound windings for both the AC and DC windings. The potential fault current is 5.9 kA due to 2.9 kA from the network and another 3 kA from the motor that acts as a load. The voltage

drop during normal operation is 1% of the rated voltage [14]. Figure 18 shows the DC bias system used in Figure 16.

Figure 18 – DC circuit for SCFCL with trifilar windings [14].

The voltage induced across the DC windings influences the DC current in the circuit. This can have an effect on the peak of the limited fault current and to preserve the value of the limited fault current, the DC circuit needs to be interrupted during fault operation [14]. Figure 19 shows the experimental induced DC circuit current during a single line to ground fault. The nominal DC current is 400A but when a fault occurs, the over-voltage induced on the DC windings causes a portion of the fault current to travel in the DC system. The extra current is AC current which could influence the peak of the limited fault current to a higher value than desired [14]. To interrupt the DC circuit a power semiconductor should be used instead of the series diode shown in Figure 18.

Figure 19 – Fault current induced into the DC bias system [14].

The initial low voltage hardware results show the correct functionality of the SCFCL with common core and trifilar windings. The 10kV prototype is built but only tested at 400V. The experimental results are shown below in Figure 20 for a single line to ground fault.

Figure 20 – SLG fault for SCFCL with trifilar windings [14].

The SCFCL limits the potential fault current for a single line to ground fault to approximately 3 times the nominal value. The potential fault current seen in the experimental setup reaches 2 kA peak for a single line to ground fault [14]. Therefore, a 40 times fault current is limited to just 3 times the nominal value. Since the fluxes of each of the wires sum up to zero, a 2 phase to ground fault (LL-G) and a 3 phase fault are investigated to see if the SCFCL can determine if a fault has occurred. Figure 21 shows a two phase to ground fault while Figure 22 shows a three phase to ground fault on the SCFCL.

Figure 21 – Two phase to ground fault [14].

Figure 22 – Three phase to ground fault [14].

The main disadvantage of using trifilar windings for a SCFCL is due to not being able to limit the prospective fault current for a two or three phase to ground fault. This SCFCL only can limit single line to ground faults. Therefore, a common core is undesirable for full system protection. If only SLG faults are of concern the trifilar windings and common core would be a cost effective solution.

Zenergy Power has been granted a DOE project to develop a HTS SCFCL for distribution and transmission networks. The difference in the design from previous SCFCLs is the introduction of the superconducting material in the DC windings instead of the AC windings [15]. Using the superconducting wires on the DC bias system requires less energy to saturate the iron-core than normally. The result is an increase in efficiency due to having fewer losses in the circuit as well as needing less energy to saturate the core. Also, during a fault the superconducting material is brought out of saturation to limit the fault current induced in the DC system [15]. The basic SCFCL concept is shown in Figure 23.

Figure 23 – Concept diagram of Zenergy Power's SCFCL [16].

Each of the iron cores only limits one half of the AC current for each phase. The DC windings are wrapped around one leg of the core for each individual core, which limits the overall amount of windings needed and allows for only one DC bias system. The AC coils are wrapped in magnetically opposite directions for each of the iron cores since only one core is used to limit one half cycle. To limit all three phases, six cores would need to be wrapped together in the DC system as shown in Figure 24.

Figure 24 – Zenergy Power's SCFCL graphic representation [16].

The initial percent fault reduction is 20% with a future objective of 40% fault reduction [16]. The design incorporates cast-epoxy AC coils and a cryogenic cooling sys-

tem using liquid nitrogen at 68K to cool the superconductors [16]. Installation of the device is shown in Figure 25.

Figure 25 – Installation of Zenergy Power’s SCFCL [16].

This device has been constructed and inserted into the “Avanti Circuit” in Southern California Edison’s Shandin substation in San Bernardino, California [16]. Certain tests were performed on the SCFCL such as a full-load steady-state fault test in Figure 26, an endurance test of 82 cycles in Figure 27, and a double fault sequence test to simulate re-closer operation in and Figure 28.

Figure 26 – Full-load and steady-state fault test [16].

Figure 26 shows the SCFCL limits the 23 kA RMS prospective steady-state fault current to approximately 16 kA RMS which is about a 30% reduction. The peak prospective fault current of 37 kA is limited to 25 kA (32% reduction).

Figure 27 – 82 cycle fault endurance test [16].

Figure 27 shows the test performed to determine the durability of the SCFCLs. SCFCL's in theory should be able to limit the fault to a specific level continuously if thermal requirements are still met [17]. The prospective peak fault current in Figure 27 is shown to reach 50 kA with steady-state fault current to be approximately 25 kA. The SCFCL successfully limited the fault current for over 1 second which is plenty of time for a circuit breaker to interrupt the limited fault current.

Figure 28 – Double-fault sequence test which simulates re-closer operation [16].

In Figure 28, a test is performed to simulate a re-closer's operation with the FCL in the line. Initially the SCFCL limits the fault current for approximately 500 ms and then the re-closer opens for 2 seconds where it re-closes into a sustained fault. The SCFCL is forced to operate immediately and limit the fault current as desired. The test shows the SCFCL's ability to recover from multiple faults quickly and provide automatic support to the system [17]. Zenergy Power has developed a smaller more compact SCFCL based on the information gain from the initial design. This "Compact" design reduces the size, weight and cost without losing any operational functionality [17]. Figure 29, shows the new compact design of the SCFCL from Zenergy Power. The cost, size and weight reduction are given in Table 3.

Figure 29 – New compact design of the SCFCL [16].

Table 3 – Cost, weight, size comparison of new and old design for SCFCL [16].

Parameter	Old Design	New Design
Iron Core Weight (lbs)	252K	67K
Cost of Iron @ \$3/lb	\$ 756K	\$ 201K
FCL Size (core iron + AC coils)	19' x 19'	10' x 7'

The size has been considerably reduced to one-half the original value, while reducing the cost and weight of the device by 25% each.

Some of the disadvantages to SCFCLs with a DC bias system are listed below [11]:

- Size and cost
- Reduction of the amount of magnetic material (cost).
- Reduction of losses during normal operation.
- Reduction of the overvoltage in the DC winding during faults.

- Cryogenic cooling system malfunctioning.
- Energy used to power the cooling system for DC windings.

Therefore, another method involving a rare earth metal, neodymium (NdFeB) permanent magnets has been introduced to remove the DC bias system.

b. Permanent Magnet Biased

A Permanent Magnet biased FCL (PMFCL) operates like a SCFCL but instead of having a DC-bias system to bias the iron core into saturation, a permanent magnet such as Neodymium (NdFeB) is used as the middle leg of the E-core design to bias the iron core into saturation or can be sandwiched by two E or C cores. Incorporating the NdFeB permanent magnet, eliminates the need for an additional winding and power supply which addresses the issue of reliability [18]. A typical configuration of a PMFCL is shown in Figure 30.

Figure 30 – PMFCL configuration with steel core [18].

Two windings are wrapped around the middle leg to limit both half's of an AC sinusoidal current. The NdFeB permanent magnet is sandwiched between two steel cores in Figure 30. However, steel is rarely used in FCL applications and the majority of the core is made up of iron. Typical series and parallel PMFCL topologies are presented in Figure 31 and Figure 32. The series configuration requires twice as much material than the parallel configuration and therefore will not be considered in design choices due to cost issues. Each core limits each half of an AC current.

Figure 31 – Series connected PMFCL topology [19].

Figure 32 – Parallel connected PMFCL topology [19].

Figure 32 is the desired topology due to less magnetic material required for limitation purposes as well as size reduction of the entire FCL. Only 1 NdFeB permanent magnet is needed to saturate the iron core for an entire AC current. One concern with using a permanent magnet to bias the iron core is the iron core may go into reverse saturation mode and lose all fault current limiting capability if the fault current reaches a high enough value [19]. An experimental setup study has been undertaken and the results

show the correct functionality of the PMFCL. The parameters used for the components in the experimental design are shown in Table 4.

Table 4 – Parameters used in PMFCL experiment [20].

Component	Material	Length or Turns	Cross Section(mm)
Magnetic Core	Ferrite(R2KW)	760 mm	40×40
Permanent Magnet	Nd-Fe-B(N30)	160 mm	80×40
Coil	Copper	440 turns	ϕ 1.2

The topology is the same as in Figure 32 but the experiment only used one core for limitation to actively compare the results of the PMFCL with normal operation [20]. To further explain the concept from the experiment the experimental prototype is shown in Figure 33.

Figure 33 – Prototype model of PMFCL [20].

The remanence B_r and coercivity of the permanent magnet shown in Figure 33 are 1.1 T and 796 kA/m for a NdFeB (N30) magnet. The voltage is set to 60 V with a nominal current of 1.5 A [20]. The PMFCL limits the 20 A prospective fault current to approximately 9 A. Figure 34 shows both the limited and prospective fault current in the exper-

imental setup. The positive portion of the waveform is limited by the PMFCL while the negative portion is not limited due to the windings of the experimental prototype. Figure 34 clearly shows the capability of a PMFCL as it reduces the prospective fault current by 55%.

Figure 34 – Limited and prospective fault current in PMFCL [20].

One major advantage of a PMFCL is the elimination of the DC bias system in SCFCLs. By removing the DC bias system, reliability is increased in the system and the PMFCL should operate as expected. One concern of a PMFCL is the reverse saturation of the iron core due to a high magnitude fault current which ends up diminishing the PMFCLs limiting capability [20].

E. Hybrid FCL

Due to the concerns in the practical application of superconducting FCLs, hybrid FCLs were introduced. They are combined devices including superconductors, semiconductors, conventional fuse or circuit breaker and fast switches. Kyushu electric developed hybrid fault limiters using a vacuum arc commutation method. This limiter has a restriction in increasing the current limiting capabilities that could be a problem during expansion. ABB developed a hybrid fault limiter consisting of fast switch, circuit breaker

and parallel resistor that could be used in extra high voltage circuit. Both these configurations are superconductor-free solutions, which mean they will need extra fault current sensors, algorithms and fast switch operated by magnetic repulsion force supplied through an additional current source. Their size and cost do not seem to be practical. The basic requirement and solutions provided by hybrid FCLs is given in Table 5.

Table 5 – Requirements and solutions of hybrid FCL

Requirements	Solutions
Minimization of superconductor usage and cryogenic burdens	Superconductors were used for only fault current sensing and commutation of fault currents.
High voltage applications	Fast switch could endure high voltage not a superconductors
Fast switch operation and fault current commutation	Electromagnetic repulsion force was used, and its current source is fault current itself commutated by superconductors
Coordination and reclosing scheme	Coordination and reclosing scheme was considered by commutation method
Cost	1/10 reduction compared to superconducting fault current limiters

One novel idea for a hybrid FCL is developed using a fast mechanical contact with superconducting material [21]. The device proposed in [21] uses an asymmetric HTS as the limiting impedance. The schematic is shown below in Figure 35.

Figure 35 – Schematic of hybrid FCL with superconducting limiter [21].

The operation of the hybrid FCL in Figure 35 is such that the current flows through the resistive SFCL and through the asymmetric coils into the fast mechanical switch and then to the load. Normally the current bypasses the current limiting reactor. The system is designed for a 500 V/ 1 kA system and the peak current is limited to 6 times the rated value. The experimental results as shown in Figure 36 show a 2 cycle fault being applied to the system. The results confirm the correct operation of the device and the hybrid FCL fully limits the potential fault current.

Figure 36 – Experimental results of hybrid FCL with superconducting limiter [21].

The disadvantage of the system is the cryogenic system used to constantly cool the superconductors as well as the design of only 500 V and 1 kA rated values. A more applicable design for a distribution system is shown in Figure 37. The design is used in marine applications for a 6.6 kV network. The device consists of a main conduction module, deflection serial assistance module, parallel deflection arc limitation module, current limitation module, and an energy storage and discharge module [22]. The main conduction module is based on a fast mechanical contact that must provide enough insulation during fault limitation mode to prevent an arc from re-striking the line. The deflection serial assistance and parallel deflection arc limitation modules force the current to flow from the main conduction module to the current limitation module. This allows the fast mechanical contact to open arc free thus extending the life of the device. The current limitation module limits the current and prevents the di/dt time from rising to an unsafe value. The energy storage and discharge module is used to store the extra energy created by the fault and to discharge it through the parallel resistor [22].

Figure 37 – AC hybrid FCL with semiconductors [22].

The disadvantage of the design is shown in Figure 38. The mechanical contacts open and close every half cycle once the fault current approaches the zero crossing point and is below the specified max fault current allowed. The maximum limited fault current reaches 5.5 kA but the maximum allowable current magnitude used for the controller is approximately 2 kA.

Figure 38 – Operation of hybrid FCL in fault limitation mode [22].

The algorithm used for fault detection is only based off of current magnitude and therefore, a better detection algorithm is needed to determine the fault is sustained and the mechanical contact will not reclose during a fault. Possible considerations include di/dt control and/or a phase lock loop control in addition to the current magnitude control.

F. Desired Characteristics for FCLs

For an optimal FCL, certain design characteristics of an ideal FCL must be considered. An ideal FCL should have the following characteristics:

1. Zero resistance/impedance at normal operation
2. Large impedance in fault conditions

3. No power loss in normal operation and fault cases
4. Fast impedance when fault occurs
5. Fast recovery when fault is cleared
6. Reliable current limitation at the defined fault current
7. Low cost
8. Good reliability
9. Smaller size than comparable devices.
10. No damage to components in the FCL

The FCL should appear invisible to the system under normal operating conditions and should have zero effect on other components in the system. Also, the power losses should be limited to zero in any operation mode. However, once a fault occurs, fast and high impedance needs to be placed into the system to limit the magnitude of the fault current in a range where relays can distinguish between a fault and normal operation. This allows the relays to send the control signal reliably to the circuit breakers to interrupt the fault once the distinction has been made. The FCL should not limit the fault too little where the circuit breaker's rating is not sufficient enough for the magnitude of the current. Having too small of an impedance leads to poor voltage regulation under normal loads. Also, the inserted impedance shouldn't be too much that the relays interpret the magnitude as a normal operating condition and thus does not send a trip signal to the circuit breaker. One-way to achieve this is to input variable impedance that depends on the magnitude of the fault current to limit it within a specific range of values as in [6]. The FCL should also respond almost instantaneously to both the DC offset and the RMS cur-

rent so that it covers all operating characteristics. Once the fault has cleared, the FCL should return to normal operating condition mode (zero impedance, zero power losses) as fast as possible. Typical fault limitation is 50% of the short-circuit current.

G. FCL Literature Review Conclusion

Although there are some viable solutions for a FCL, each of the presented topologies have fundamental weaknesses such as on-state voltage drop, power handling capability, complex gate drive system, introduction of harmonics in the power grid, slow response of passive device, complex and expensive cooling systems and power losses after fault has ended. Therefore, there is still a need for a FCL design that can dynamically change its impedance during fault operation to limit the fault current to a preset value for the protection of system components. In addition, a FCL must be able to detect the fault and insert the limiting impedance at a desired time of less than 4 ms to keep the first peak of the short circuit current from occurring and damaging components. The first peak of the fault current is the most dangerous and needs to be limited to a lower value. The FCL must be able to operate reliably and minimize normal operating losses.

Motivation for new research is to construct a FCL within a specific space and cost requirement such as 1 cubic meter that can withstand the power requirements put upon it during a short-circuit. The goal is to develop a FCL that is cost and size effective while meeting or exceeding the given requirements. Also, there is no previously developed FCL that combines all of the advantages of different types of FCLs into one FCL. The proposed FCL in Chapter 5 includes all of the advantages of each type of FCL with minimal disadvantages.

Chapter 3

INITIAL SOLID-STATE FCL DESIGN

I. Initial FCL Design

The initial FCL design is a SSFCL that uses semiconductor switches to commute the current during normal operation and to switch the current over to the limiting impedance during fault limitation mode. The device is rated for 12.47 kVLL and 100 A. The limiting impedance is designed to limit the maximum short-circuit current to 2 times the rated value. Figure 39 shows the initial proposed design.

Figure 39 – Initial SSFCL design

The line resistance and inductance is assumed to be $R_{line} = 0.5 \frac{\Omega}{mile}$ and $X_{line} = 0.6 \frac{\Omega}{mile}$. The system is design for a 5 mile line and the semiconductor switch is chosen to be 10 kV/ 10 A SiC MOSFETs.

II. Operating Principle

Under normal operating conditions, the SiC MOSFETs are conducting current with each SiC MOSFET only conducting one half of the period. However, when a fault occurs, the control logic determines if the fault current is above a preset reference value and then by PWM, switches the SiC MOSFETs ON and OFF corresponding to the difference of the fault current compared to the reference current. As the fault current increases, the duty ratio of the SiC MOSFETs decreases due to the inversely proportional relationship. The duty ratio is defined as:

$$Duty = \frac{T_{ON}}{T} \quad (3-1)$$

Each SiC MOSFET has a maximum duty ratio of 0.5 because only half of the period the device will be conducting current, while the minimum duty cycle is 0. A duty ratio of zero means a fault has occurred and the current is passed to the limiter. The PWM is set for 1 kHz which is fast compared to the 60 Hz line current; therefore the maximum on time for each SiC MOSFET is 500 μ s per period during a fault, otherwise the SiC MOSFETs are constantly on and conducting the entire 60 Hz sine wave. The proposed limiting impedance combines the advantages of a buck converter such as full control of voltage and current throughout the entire operating period with the advantages of a non-linear resistance typically used in FCL designs. However, this device differs from a typical DC buck converter because the current and voltage produced are sinusoidal instead of preset to a specific value. Also, this design includes two buck converters that are connected in anti-parallel to limit both the positive and negative half of the fault current. Another difference in the proposed limiter is typically in buck converters the resistance is

constant and never changes but the resistance has been changed to be a Metal Oxide Varistor (MOV) to provide the dynamical impedance. In the proposed initial SSFCL, as the current increases due to the fault, the resistance in the MOV changes accordingly to limit the maximum current to two times the rated value. Another new component included in the proposed FCL, which is not part of the standard buck converter, is a resistor in parallel ($R_{rC} = 100 \Omega$) to suppress switching transients and increase the di/dt time of the semiconductor components.

The inductance and capacitance for the limiting impedance is chosen from available parts in the market. However, the capacitance value will need to be achieved by connecting multiple parallel capacitances together to achieve the current rating for this application. The resistance in the limiter is also found by incorporating available parts in the market. The normal operating current is 10A due to the SiC MOSFET maximum current rating but further advancements are being made to reach 120 A. During normal operation the operating current is passing through the SiC MOSFETs with only small conduction losses and onto the load. However, once a fault occurs, the SiC MOSFETs are shut down within a few μs and the current is forced through the limiting impedance.

In this application of fault current limitation, the fault current is assumed to be 10 times the rated current but in industry fault current magnitude varies. Therefore, a non-linear resistance would be a better choice to ensure the maximum fault current does not exceed a circuit breakers maximum interruptible fault current. The MOVs will clamp down on the fault current magnitude and help to produce a sinusoidal waveform. The MOVs should be selected to operate in the region before saturation occurs during fault operation to provide the variable impedance. Otherwise, the MOV will saturate and not

provide any resistance. The control signals for each SiC MOSFET accounts for this variable resistance and sends the proper gate signal to each SiC MOSFET for correct operation. A graph of this operation is shown in Figure 46.

The limiting impedance is selected due to its non-linear impedance. Also, the cost of components included in the design is relatively cheap compared to other solutions such as ferromagnetic iron cores or superconducting materials. The novelty of the design is explained above and provides an alternative solution for fault current limitation that achieves fast response and non-linear impedance.

III. Power Requirements

The proposed FCL will have high device stresses such as overvoltage, fault current and energy absorption placed upon it during fault operation. Therefore, theoretical calculations need to be performed to discover the maximum operating time for the proposed FCL before breakdown occurs. A single line to ground fault across the load forces the proposed FCL to dissipate the entire fault current as it is now referenced to ground instead of floating in the system. The MOV and capacitor system impedance can be approximated by (3-2) when the per unit current (I_{pu}) through the device is greater than 0.98, which constantly occurs for fault current [23].

$$Z_{EQ} = R'_C - jX'_C \quad (3 - 2)$$

where Z_{EQ} is the equivalent impedance and R'_C and X'_C are defined in (3-3) and (3-4) respectively.

$$R'_C = X_{CSLim} (.0745 + .49e^{-0.243*I_{pu}} - .6e^{-1.4*I_{pu}} - 35e^{-5*I_{pu}}) \quad (3 - 3)$$

$$X'_C = X_{CSLim} (.101 - .005749I_{pu} + 2.088e^{-0.8568*I_{pu}}) \quad (3 - 4)$$

X_{CSLim} is the reactance of the capacitor in parallel with the MOV. Since the maximum fault current is designed to be twice the rated current, $I_{pu} = 2$ is substituted in for the calculations involving (3-3) and (3-4). Therefore, $Z_{EQ} = 1,792.16 - j2,471.1 \Omega$. The power dissipated by the FCL would be at a maximum when the maximum fault current and impedance are used in the calculations. Table 6 shows the parameters used in the FCL for both the power calculations and simulations.

Table 6 – Parameters of initial SSFCL.

Voltage	7.2 kV _{RMS}
Current	10 A
L _{LIM}	60 μ H
C _{LIM}	500 nF
MOV	10 kV _{RMS}
R _{LIM}	100 Ω
R _{Snubber}	1 M Ω
C _{Snubber}	80 μ F

The equivalent impedance needs to be calculated to be able to find the power dissipated through the proposed limiter. The steps taken to calculate the equivalent impedance of the proposed limiting impedance are shown in Figure 40.

Figure 40 – Steps taken to find equivalent impedance of proposed limiter.

The combined impedance for both the positive and negative impedance is given by (3-5):

$$Z_{Positive} = Z_{Negative} = X_{Lim} \parallel R_{Lim} + Z_{EQ} \quad (3 - 5)$$

where X_{Lim} is the impedance for the limiting inductance and is found to be $j22.619 \text{ m}\Omega$. Therefore, $Z_{Positive} = Z_{Negative} = 1,792.16 - j2,471.08 \Omega$. For the final step in Figure 3.3-2, the overall equivalent impedance of the proposed FCL is determined by (3-6).

$$Z_{Limiter} = Z_{Positive} \parallel Z_{Negative} \parallel Z_{Snubber} \quad (3 - 6)$$

where $Z_{Snubber}$ is the equivalent impedance of the snubber circuit. Based on the values presented in Table 1, $Z_{Snubber}$ is negligible in the calculation of $Z_{Limiter}$. The total impedance of the limiting device is found to be $Z_{Limiter} = 896.8 - j1233.33 \Omega$. The short circuit line current without the FCL in the line is calculated in (3-7) [24].

$$i_{sc} = \frac{V_{smax} \sin(\omega t - \theta_{line})}{|Z_{line}|} + \left(I_{Tfault} - \frac{V_{smax} \sin(\omega T_{fault} - \theta_{line})}{|Z_{line}|} \right) e^{-\frac{t-T_{fault}}{\tau_{line}}} \quad (3-7)$$

where T_{fault} is the time the fault occurs and is assumed in the calculations to be 5 ms for a near maximum value and the angle, line impedance and time constant can be calculated in (3-8), (3-9), and (3-10) respectively.

$$\theta_{line} = \tan^{-1} \left(\frac{X_{line}}{R_{line}} \right) \quad (3-8)$$

$$|Z_{line}| = \sqrt{R_{line}^2 + X_{line}^2} \quad (3-9)$$

$$\tau_{line} = \frac{L_{line}}{R_{line}} \quad (3-10)$$

where L_{line} is the line inductance, R_{line} is the line resistance, θ_{line} is the phase angle, V_{smax} is the maximum value of the voltage and I_{Tfault} is the magnitude of the line current when the fault occurs. From the parameters in the circuit $i_{sc} = 1815.31$ with $I_{Tfault} = 10$ A for worst-case scenario and $t = 5$ ms.

Once detection of the fault has occurred and the FCL is inserted into the line, the parameters of the equivalent circuit are changed. The limited fault current can be calculated from (3-11).

$$i_{lim} = \frac{V_{smax} \sin(\omega t - \theta_{lim})}{|Z_{lim}|} + \left(I_{SCmax} - \frac{V_{smax} \sin(\omega(T_{fault} + T_{del}) - \theta_{lim})}{|Z_{lim}|} \right) e^{-\frac{t-(T_{fault}+T_{del})}{\tau_{lim}}} \quad (3-11)$$

where I_{SCmax} is the maximum value of the first peak of the short circuit current [24]. For this proposed FCL $I_{SCmax} = 20$ A. T_{del} is the time to activate the FCL which, includes turn ON and OFF times of the switching device as well as the detection time. T_{del} is assumed to be 2 ms. The proposed FCL introduces both a resistance and induct-

ance into the system. Therefore, the new limiting impedance Z_{lim} , time constant τ_{lim} , and angle θ_{lim} are given by (3-12), (3-13), and (3-14), respectively.

$$|Z_{lim}| = \sqrt{(R_{line} + R_{limiter})^2 + (X_{line} + X_{limiter})^2} \quad (3-12)$$

$$\tau_{lim} = \frac{L_{line} + L_{FCL}}{R_{line} + R_{FCL}} \quad (3-13)$$

$$\theta_{lim} = \tan^{-1} \left(\frac{X_{line} + X_{limiter}}{R_{line} + R_{limiter}} \right) \quad (3-14)$$

Energy dissipation can be calculated by taking the integral of the real power absorbed for a given amount of time as shown in (3-15) and derived in [23] and [24].

$$E_{FCL} = \int_{t_1}^{t_2} i_{lim}^2 R_{FCL} dt \quad (3-15)$$

where i_{lim} is the limited fault current, as shown in (3-11) and R_{FCL} is the real part of the limiting impedance ($Z_{limiter}$). Since the system is 60 Hz, converting the power dissipated to per cycle determines how long the limiter could sustain the fault current. Therefore, from (3-15), the energy dissipated by the FCL for one second is $E_{FCL} = 14.718 \text{ kJoules}$. However, since the first peak of the fault current causes the most damage (i.e. device destruction), the energy dissipated by the proposed FCL for the first cycle is calculated to be $E_{FCL} = 4.79748 \text{ kJoules}$. Lowering the detection time T_{del} within the μs range reduces the energy dissipated by the FCL significantly. This demonstrates the need for faster, more accurate fault current detection. Also, the components selected must be suitable for the energy handling capability as described above.

IV. Simulation Results

The simulation software used is PLECS (Piecewise Linear Electrical Circuit Simulation). PLECS is a Simulink toolbox and a standalone simulation tool developed by Plexim that specializes in power electronics and system level simulations. PLECS has the advantage of using the control systems available in Simulink to control the power electronic circuit as desired for the proposed FCL. PLECS assumes the power electronic components as ideal components with no reverse recovery or leakage current.

A fault is programmed to occur at times $t = 0.355\text{ s}$ and $t = 0.9964\text{ s}$, and end at times $t = 0.7055\text{ s}$ and $t = 1.297\text{ s}$, respectively. The fault is set to occur at the worse-case scenario and not at zero-crossing points, which demonstrates the FCL is capable of fault current limitation within μs along any point of the sinusoidal waveform. The μs reaction time of the proposed FCL enables the device to protect sensitive loads from being damaged by the potential fault current. The control system operates by comparing the magnitude of the current through the device with a reference signal and then sends the proper PWM signal to the SiC MOSFETs. Once the compared value exceeds a certain preset value, the switches are turned off and forced into blocking mode, thus passing all fault current through the limiting impedance. Figure 41 displays the potential fault current in the system as well as the overvoltage spikes caused by the fault without the FCL in the system.

Figure 41 - Displays the prospective fault current and overvoltage in the system without the proposed device.

The magnitude of the prospective fault current shown in Figure 41 agrees with the calculated prospective fault current found in (3-7) to be 1,815.31 A. The need for semiconductor switching is apparent by the prospective fault current in the system. The SiC MOSFETs can limit the initial peak of the fault current by turning off within μ s. Figure 42 is a zoomed in version of Figure 41 for the fault that occurs at $t = 0.355$ s.

Figure 42: Zoomed in version of Figure 41.

The normal current through the system is 10 A, as shown in Figure 41 and Figure 42. When the fault occurs, the potential fault current in the system reaches 1800 A due to the fast transient and the inductive load in the system. The system voltage is 7.2 kV_{RMS} but the potential overvoltage, as shown in Figure 41, exceeds 35 kV within a few ms. The magnitude of the fault current and voltage greatly exceeds the power requirements of any devices operating in the system and justifies a need for a FCL to be placed for protection. Also, the FCL needs to operate as fast as possible to limit the initial rise of the fault current to an allowable level for the correct protection equipment, such as circuit breakers, to operate for a sustained fault. Figure 43 displays the potential fault current with the proposed FCL in the system. Figure 44 shows a zoomed in version of Figure 43 at the positive maximum current.

Figure 43: Displays the proposed FCL during normal operation and fault operation.

Figure 44: Displays a zoomed in version of Figure 43.

Once the fault occurs, the proposed limiter acts upon the potential fault current and limits the fault current to 18 A sinusoidal, which is less than the designed value of 20 A maximum. Therefore, the FCL operates as expected, and the MOV's variable impedance increases as the fault reaches the 20 A maximum value, thus producing the sinusoidal waveform. The load voltage drops to zero due to the fault occurring across the load. However, when the fault occurs in Figure 43, the entire system voltage ($7.2 \text{ kV}_{\text{RMS}}$) appears across the proposed FCL, since the SiC MOSFETs are now turned off. Also, the noticeable overvoltage that is shown in Figure 41 is reduced to two times the rated voltage by the FCL. This ensures the SiC MOSFETs will be able to handle the induced over voltage without device failure occurring. Figure 45 shows a zoomed in version of Figure 43 at the worst-case scenario if the fault occurs at the negative peak of the current waveform.

Figure 44 displays the fast switching transients caused by turning the SiC MOSFETs off and rerouting the current through the limiter. When the fault occurs, a fast switching transient and DC component occur, but ends within ms as the fault current is switched to the limiter. The fast switching transient for the worst-case scenario, reaches a magnitude of 80 A before the controller detects that a fault has occurred. The fast transient ends in 2 ms and the entire fault energy is absorbed by the FCL. Figure 46 shows the PWM signal used to control the SiC MOSFETs during the simulation at time of fault occurrence at $t = 0.355\text{s}$. The PWM signal is the same for all cases.

Figure 45- Worst-case scenario of Figure 43 at negative peak current.

Figure 46: PWM signal for each SiC MOSFET.

The energy placed upon the FCL is shown in Figure 47.

Figure 47: Energy dissipated by initial FCL.

The energy absorbed for one cycle is calculated in the simulation and is found to be $E_{1Cycle} = 3.3235 \text{ kW}$. This varies about 1 kW from the previous calculation because the detection time in the simulation program is in μs as compared to the previous calculation that assumed 5 ms.

V. Initial FCL Conclusion

The previous calculations in Chapter 3 are an approximation to the real system and therefore would include some error. Varying the length of time of the fault shows the feasibility of the FCLs' ability to withstand the significant power requirements caused by the fault for half of a second. This is more than enough time for other protection equipment to detect the fault and operate as intended. In addition, the $\frac{di}{dt} = 1.1205 \frac{A}{\mu\text{s}}$ and $\frac{dv}{dt} = 92.8755 \frac{V}{\mu\text{s}}$ time are reduced well within the maximum values of 100 A/ μs and with the proposed FCL, which protects the components in the system by limiting the rise and

fall of the current/voltage respectively. Controlling the di/dt and dv/dt times ensure the SiC MOSFETs can handle the stresses of the system and extends their operational life. Overall, the SSFCL works as designed but the power requirements placed upon the device during fault limitation require multiple devices to be placed in series and parallel configuration. The result of cascading the devices introduces unexpected costs which would negate the cost-effective solution. In addition, the energy dissipated by the FCL is a relatively high value and building this system would require cascading multiple in parallel to be able to handle the power without being destroyed which is determined to not be cost effective and therefore, another solution will need to be investigated. The losses in steady-state operation would be too great to warrant the development and installation of this FCL design. Therefore, a different design is proposed in chapter 5 that is cost effective, reliable and combines all the advantages of different FCLs together with no significant disadvantages. In Chapter 4, a comparison of different magnetic materials is presented to determine which material is most effective for FCL applications and that material is used in the proposed design in Chapter 5.

Chapter 4

FERROMAGNETIC MATERIAL COMPARISON

Four ferromagnetic materials are compared to determine which material is the most suitable for FCL applications. The four materials compared are Laminated Steel (M4), Aluminum-Nickel-Cobalt (AlNiCo-8 cast), Samarium-Cobalt (SmCo-5), and Neodymium (NdFeB-N42). Laminated Steel M4 (iron core) is a standard material used in the design of transformers and is the material of choice for previous FCL topologies presented in the literature review. The other three materials are not as readily used but are investigated to determine if there are any added benefits as compared to Laminated Steel. When placed in an AC circuit, each of the ferromagnetic materials exhibit hysteresis. Therefore, an accurate model of the hysteresis effect is warranted since the changing core's permeability creates the nonlinear inductance.

I. Hysteresis Modeling

To accurately model the nonlinear characteristics of a ferromagnetic material, different modeling methods of hysteresis were analyzed and used in determining the most feasible ferromagnetic material for this FCL application. The two methods of hysteresis analyzed are the Preisach method of hysteresis and the Jiles-Atherton method of hysteresis. The Preisach method is initially used in PLECS to determine which material is most suitable for FCL applications and the Jiles-Atherton method is used in PSCAD to further design and test the FCL after the ferromagnetic material is chosen. The PLECS developers implemented the Preisach method in PLECS while the author implemented the Jiles-Atherton method in PSCAD.

A. Preisach Method of Hysteresis

The Preisach model is a mathematical representation of the nonlinear permeability of a ferromagnetic material during all operation modes [25]. The basics of the Preisach model start with the elementary Preisach hysteron [26]. The hysteron acts like a relay where certain threshold values α and β are the particular ferromagnetic material's coercive field (H_c). Figure 48 shows the basic relay hysteron used in the Preisach model and is in the public domain.

Figure 48 – Depiction of the Preisach Relay Hysteron.

The hysteron has two possible states, either in the same direction as the applied field H , $\gamma_{\alpha\beta} = +1$ or in the opposite direction, $\gamma_{\alpha\beta} = 0$. The switching of the sign occurs at β for a field in the positive increasing direction and α for a field in the negative increasing direction. $\beta \geq \alpha$ is always true for each dipole in the ferromagnetic material. The applied magnetic field H , will induce a magnetic flux density $B(H)$ in the material which can be expressed by (4-1).

$$B(H) = \int_S \mu(\alpha, \beta) \gamma_{\alpha\beta}(H) d\alpha d\beta \quad (4 - 1)$$

where $\gamma_{\alpha\beta}(H)$ is the elementary Preisach hysteron, $\mu(\alpha, \beta)$ is the distribution function, S is the Preisach plane, and α, β are the threshold values associated with the particular ferromagnetic material [27]. An illustration of the Preisach plane is shown in Figure 49.

Figure 49 – Preisach Plane [27].

Each point in the Preisach plane is represented by a probability density function. In the simulations in PLECS, a Lorentzian distribution function is used and is developed by the creators of PLECS [28]. Any point outside the Preisach plane is zero and since the major hysteresis curve is symmetrical, any value inside the plane is given a value of 1 and $\mu(\alpha, \beta) = \mu(-\alpha, -\beta)$. However, to model the minor loops in the hysteresis curve, the region S^- corresponds to the dipoles with $\gamma_{\alpha\beta}(H) = -1$ and S^+ corresponds to $\gamma_{\alpha\beta}(H) = +1$ in Figure 49. The simulation method for the Preisach method is shown below in the flow chart in Figure 50.

Figure 50 – Simulation flowchart for Preisach method.

The Preisach model in Figure 50 is equation (4-1) and has the necessary inputs such as the B_{rem} and H_c . The core permeability is then calculated using equation (4-10) and the inductance is calculated using equation (4-13). Once the inductance is calculated, the updated inductance is inserted into the system and the process is repeated until the fault has ended.

B. Jiles-Atherton Method of Hysteresis

The Jiles-Atherton method of hysteresis is a numerically based model that includes all of the mechanisms that occur at magnetization of a ferromagnetic material. The

Jiles-Atherton model needs some pre-determined parameters before it can be implemented [29]. These parameters include α_j , which is the mean field parameter defining the magnetic coupling between domains in the material and determines the shape of the hysteresis curve. Other values include the saturation flux density (B_{sat}), μ_0 , and H . Typical values of α_j range between 0 and 1. The magnetic flux density $B(H)$ is found by equation (4-2) [15].

$$B(H) = B_{sat} * \left(\coth \frac{H}{\alpha_j} - \frac{\alpha_j}{H} \right) + \mu_0 * H \quad (4 - 2)$$

Where B_{sat} is the saturation flux density, α is the mean field parameter, H is the applied magnetic field, and μ_0 is the permeability of free space. The hyperbolic cotangent can be represented by hyperbolic sine and cosine functions in (4-3).

$$\coth(x) = - \frac{\sinh(2x)}{1 - \cosh(2x)} \quad (4 - 3)$$

Where $x = \frac{H}{\alpha_j}$. Further representation of the hyperbolic functions ($\sinh(2x)$ and $\cosh(2x)$) can be shown by exponential functions shown below in (4-4) and (4-5).

$$\sinh(2x) = \frac{e^{2x} - e^{-2x}}{2} \quad (4 - 4)$$

$$\cosh(2x) = \frac{e^{2x} + e^{-2x}}{2} \quad (4 - 5)$$

An issue occurs when $H \rightarrow 0$ as equation (4-2) becomes numerically unstable. To remedy this numerically unstable problem, an approximation is made as H approaches zero and is shown below in (4-6) [15].

$$B(H) = B_{sat} * \left(\frac{H}{3\alpha_j} \right) + \mu_0 * H \quad (4 - 6)$$

To accurately model the core's instantaneous permeability while traversing through the hysteresis loop, the slope of the hysteresis loop must be calculated and can be found by differentiating equations (4-2) and (4-6). The core's instantaneous permeability is the key parameter in the FCL design because it produces the nonlinear inductance.

$$\frac{dB}{dH} = \mu_0 * \left[\frac{B_{sat}}{\mu_0} * \left(\frac{\alpha}{H^2} - \frac{1}{\alpha_j} \text{csch}^2 \frac{H}{\alpha_j} \right) + 1 \right] \quad (4 - 7)$$

as H approaches 0 the following approximation is made.

$$\frac{dB}{dH} = \frac{B_{sat}}{3\alpha_j} + \mu_0 \quad (4 - 8)$$

The $\text{csch}^2(x)$ function can be represented by the $\sinh(x)$ and $\cosh(x)$ functions as shown below in (4-9).

$$\text{csch}^2(x) = \frac{4\sinh^2(x)}{(1 - \cosh(2x))^2} \quad (4 - 9)$$

where $x = \frac{H}{\alpha}$ and $\sinh(x)$ and $\cosh(x)$ functions are given in (4-4) and (4-5) respectively. In conclusion, both methods of hysteresis are able to accurately model the nonlinear characteristics of ferromagnetic materials. The Jiles-Atherton method is simpler to implement than the Preisach method and has the advantage of being numerically represented.

C. Inductance Calculation

The Jiles-Atherton method is used in the PSCAD simulations of the proposed FCL in Chapter 5. However, for the PLECS simulations shown in this chapter, the Preisach method is used because a default library component in PLECS uses the Preisach

method [28]. The idea of this comparison is to determine if the magnetic properties of each of the studied materials influence fault current limiting capability. Utilizing the individual ferromagnetic properties of each material, the time-varying nonlinear permeability (μ_{core}) is given as a function of B and H and can be calculated based on the output of the Preisach model (4-1) and the Jiles-Atherton model (4-7 and 4-8).

$$\mu_{core}(B, H) = \frac{\Delta B}{\Delta H} = \frac{dB}{dH} \quad (4 - 10)$$

The magnetic core changes its permeability based on the change in the magnetic flux density and the magnetic field strength applied. In the simulation, the permeability of the core is calculated at each time step for the given magnetic field strength and magnetic flux density. The permeability is then updated based on the new value for the core's permeability. The calculation for $\mu_{core}(B, H)$ can be achieved after each time-step by subtracting the previous iteration values for H and B from the current H and B values. This method allows for the inductance of the ferromagnetic core to be modeled as a nonlinear inductance. This nonlinear inductance varies depending on the current through the core and the voltage across the core.

Faraday's law states the inductance (L) of the ferromagnetic material can be calculated from (4-11).

$$L = \frac{d\Psi}{di} = \frac{Nd\Phi_B}{di} \quad (4 - 11)$$

where Ψ is the flux linkage, Φ_B is the magnetic flux and can be expressed as $\Phi_B = B(H) * A_{core}$, N is the number of turns, and di is the rate of change in the current. Substituting (4-1) into (4-11) for the nonlinear inductance yields:

$$L(B, H) = \frac{NA_{core} * d(B(H))}{di} \quad (4 - 12)$$

where A_{core} is the cross-sectional area of the core. The nonlinear inductance can be modeled as a function of the flux density and magnetic field strength for the Preisach model (4-13).

$$L(B, H) = \mu_0 \mu_{core}(B, H) \frac{N^2 A_{core}}{l_{mean}} \quad (4 - 13)$$

where μ_0 is permeability of free space and l_{mean} is the mean path length. The nonlinearity of the inductance produced by the ferromagnetic material is utilized for fault current limitation purposes. The Jiles-Atherton model uses the following equation for its inductance calculation and is based upon equation (4-14).

$$L(B, H) = \frac{\mu_0 A_{core} N}{l_{mean}} \int_{-L_{coil}/2}^{L_{coil}/2} \mu_{core}(B, H) * H(x) dx \quad (4 - 14)$$

where $H(x)$ is the applied magnetic field a distance x along the coils of the core. Equation (4-14) is used in the PSCAD simulations shown in Chapter 6 to calculate the instantaneous inductance of the magnetic core. The simulation flowchart for the Jiles-Atherton method is shown in Figure 51.

Figure 51 – Simulation flowchart for Jiles-Atherton method.

The Jiles-Atherton simulation method is approximately the same as the Preisach method besides the equations used to calculate B , $\mu_{core}(B,H)$, and $L(B,H)$. The Jiles-Atherton method uses equations (4-2), (4-6), (4-10) and (4-14). Again, after each time step, the inductance is calculated and inserted into the system.

II. Magnetic Material Design

Each of the previously listed ferromagnetic materials is analyzed to determine which material is most suitable for FCL applications. The physical design of the ferromagnetic core resembles a transformer as two “C-cores” are connected together. Compared to standard saturable core FCLs, the design differs from and SCFCL because the DC bias system is eliminated which in turn eliminates the third (middle) leg. Eliminating

the third leg in the core reduces the material cost of the core since the middle leg is typically twice the size of the outer legs [13]. The maximum magnet size produced for NdFeB and SmCo is 0.102 m x 0.056 m x 0.102 m and the overall core dimensions used in the PLECS simulations are 0.61 m x 0.203 m x 0.61 m. Physically assembling the ferromagnetic core for NdFeB and SmCo would require stacking of individual cores to reach the desired core parameters. The individual cores would need to be assembled, side-by-side and one on top of the other to reach the desired core shape. While assembling, the ferromagnetic core would need to be demagnetized and then re-magnetized to insure their polarity is in the same direction. A casing is needed to hold the desired core shape and prevent any of the individual magnetic cores from separating from the desired core shape. The designed core shape is shown below in Figure 52. The coils are vertically wrapped around an outer leg of the core and the casing.

Jorge Mendoza performed the drawings for the casing design as I supervised him during his undergraduate research. The drawings were created in SolidWorks.

Figure 52 – Ferromagnetic core design and casing.

To calculate the peak AC flux density (B_{pk}) produced in the core, Faraday's law of induction is used in equation (4-15).

$$V(t) = N \frac{d\Phi_B}{dt} \quad (4 - 15)$$

Substituting $\Phi_B = BA_{core}$ and solving for B yields (4-16).

$$B(t) = \frac{1}{NA_{core}} \int_0^T V(t) dt \quad (4 - 16)$$

where T is the period. B(t) is at a maximum when $\frac{dB(t)}{dt} = 0$. To determine the peak AC flux density (B_{pk}) in the core design, a standard method for practical transformer design is used. For a sinusoidal wave, the flux in the core will change from positive to negative per half cycle. The average rate of change of flux per cycle is given by equation (4-17).

$$\Phi_{avg} = 4f\Phi_B \frac{Wb}{s} \quad (4 - 17)$$

The average EMF (voltage) produced per turn is shown in (4-15) and the RMS value is 1.11 times the average EMF. Thus, the peak AC flux density in a transformer type core is found by substituting (4-17) into (4-15) and solving for B yields following equation (4-18) [30]. 10^8 is dependent on the definition of 1 Wb/sec = 1V and 1 Wb = 10^8 flux lines.

$$B_{pk} = \frac{V_{RMS} * 10^8}{4.44NfA_{core}} (Gauss) \quad (4 - 18)$$

A conversion factor of 1 Tesla is equal to 10,000 Gauss is needed to convert B_{pk} into SI units. For the proposed FCL, the saturation flux density will be achieved with the physical and electrical parameters, which insures the entire hysteresis curve is traversed.

For the permanent magnets (NdFeB and SmCo), the pull forces of each magnet create a dangerous situation for assembly as the cores could slam together and cause bodily harm to a worker or could shatter upon impact. To remedy this situation, the magnetic cores would need to be demagnetized by heating each core past their Curie temperature (T_C) before assembly or ordering them demagnetized from the manufacturer. After the magnets are demagnetized, assembly should present no harmful situation from the magnets themselves. Upon a fault, the magnets will regain their magnetization and continue traversing through the hysteresis loop until the fault ends. Another option would be to energize the line and re-magnetize the permanent magnets before a fault occurs. Figure 53 shows the individual magnets stacked to the desired core shape in Figure 52.

Figure 53 – NdFeB and SmCo core design.

The properties of each of the materials are used as the inputs into the PLECS simulation model as the basis for the comparison and are shown in Table 7. The dimensions of the core studied are approximately $\frac{1}{6}$ the size of a typical FCL in [16].

Table 7 – Ferromagnetic material properties [31–34].

Property	NdFeB N42	SmCo 5	AlNiCo 8 Cast	Laminated Steel – M4
N	60	60	60	60
$A_{core} (m^2)$	0.04129	0.04129	0.04129	0.04129
$l_{mean} (m)$	1.6256	1.6256	1.6256	1.6256
$B_{rem} (T)$	1.3	1.06	0.83	0.42
$B_{sat} (T)$	1.5	1.35	1.1	0.6
$H_c \left(\frac{kA}{m} \right)$	994.718	736.092	131.303	234.754
$H_{sat} \left(\frac{kA}{m} \right)$	1,114.085	915	138.303	242.711
$\rho (\Omega * m)$	1.6×10^{-6}	0.86×10^{-6}	0.47×10^{-6}	0.51×10^{-8}

B_{rem} is the remanence flux density, B_{sat} is the saturation flux density, H_c is the coercivity, H_{sat} is the saturation field strength, and ρ is the electrical resistivity of ferromagnetic material and is used to model the resistance of the material. The coil resistance in the simulation is ignored since the inductance of the core is much greater than the resistance of the coils. The only parameters changed while comparing the different materials are the individual material properties while the physical design remains the same throughout each core. By keeping the core parameters the same, the ferromagnetic material properties can be examined to determine which material is the most suitable for FCL applications by providing the most inductance for a given size.

III. PLECS Simulations

PLECS is used to determine which ferromagnetic material is most suited for FCL applications. The system parameters used in the high voltage simulations are given in Table 8. The PLECS simulation configurations are shown in Appendix A as well as the custom C code written for the controller described in Chapter 5.

Table 8 – FCL high voltage design parameters.

Line to Line Voltage	V_{LL}	12.47 kV
Line to Neutral Voltage	V_{LN}	7.2 kV
Nominal Current	I_n	1.25 kA
Potential Peak Fault Current	I_{sc}	50 kA
Potential Steady State Fault Current	$I_{sc\ ss}$	26 kA
Line Frequency	f	60 Hz
Maximum Fault Duration	t_{FCL}	1 sec
Asymmetry Factor	$\frac{X}{R}$	20
Percent Reduction	PR	45-55%

In PLECS, a fault is programmed to occur at time $t = 0.2$ s which is the negative peak of the line current. A peak current value is used to determine the response of the

FCL under the worst-case scenario. The maximum fault duration is 1 sec due to the design requirements in Table 8. Each core must be subjected to the worst-case scenario to determine the practicality of each magnetic material. Figure 54 shows the voltage from the source and the prospective fault current without any FCL in the system.

Figure 54 - Line voltage (top) and prospective fault current without FCL (bottom) .

The nominal line current (I_n) is 1.25 kA. The voltage is 7.2 kV_{LN} and the prospective peak fault current (I_{SC}) is 50 kA with a steady-state current (I_{SC_SS}) of 26 kA. The objective is to determine the amount of reduction of I_{SC} and I_{SC_SS} given a specific ferromagnetic material. The first ferromagnetic material examined is laminated steel (M4). The properties of laminated steel are given in Table 7. Figure 55 shows the voltage across the FCL and the limited fault current with a laminated steel core.

Figure 55 - Voltage across the FCL (top) and limited fault current with a laminated steel core (bottom).

During a fault, voltage is placed upon the FCL relative to its impedance. The voltage across the laminated steel FCL is approximately 1.2 kV. Switching to the FCL once a fault has occurred causes switching transients across the FCL. The MOV conducts the switching transient current for the short time and protects the ferromagnetic core from stress induced by the transient voltage. The limited peak fault current (I_{Lim_LS}) with a laminated steel core FCL is 44 kA and the limited steady-state fault current ($I_{Lim\_LS\_SS}$) is 24 kA. The laminated steel core produces a reduction of 12% for the peak fault current and a 7.69% reduction for the steady state fault current.

Figure 56 shows the hysteresis curve produced during the simulation of a laminated steel core FCL using the Preisach model of hysteresis to model the nonlinearities of the core. The M4 core saturates relatively quickly and does not provide adequate current

limitation because the majority of the sine wave causes the M4 core to operate in the saturated state.

Figure 56 - Hysteresis curve obtained in the simulation for a laminated steel core using the Preisach model.

The Preisach model of hysteresis is accurate during the simulation as the input parameters in Table 7 are mostly within agreement with the simulated values. The M4 core is only able to provide a small amount of fault current limitation for the given core design because the magnitude of the fault current quickly saturates the core, which provides little inductance. Figure 57 shows the voltage across the FCL and limited fault current for an AlNiCo core.

Figure 57 - Voltage across the FCL (top) and limited fault current with an AlNiCo core (bottom).

The voltage across the AlNiCo core FCL is 1.8 kV. The switching transients are commutated through the MOV for protection purposes. Since the voltage across the AlNiCo FCL is greater than in the laminated steel case, the limited fault current is expected less than in the laminated steel case. The limited peak fault current (I_{Lim_AL}) is 39 kA and the limited steady state fault current ($I_{Lim\_AL\_SS}$) is 22 kA. Thus, the AlNiCo core FCL provides a 22% reduction in peak fault current and a 15.38% reduction in steady state fault current.

Figure 58 shows the simulated hysteresis curve of an AlNiCo core FCL using the Preisach model of hysteresis.

Figure 58 - Hysteresis curve obtained in the simulation for an AlNiCo core using the Preisach model.

AlNiCo saturates relatively quickly which provides little fault current limitation. The magnitude of the fault current causes the AlNiCo core to saturate for most of the sine wave and thus providing ineffective limitation. To increase the effectiveness of the AlNiCo core, there would need to be either an increase in the number of turns or the cross-sectional area of the core or by reducing the mean path length of the core. These modifications to the core design should result in an increase fault current limitation. The AlNiCo core operates mostly in the saturated region of the hysteresis curve. The core is determined to be ineffective in limiting the fault current with the given system and core parameters. Figure 59 shows the voltage across the FCL and the limited fault current for an SmCo core FCL.

Figure 59 - Voltage across the FCL (top) and limited fault current with a SmCo core (bottom).

The voltage across the SmCo core FCL is 3.8 kV. The switching transients are limited by the MOV and the core is unaffected by the high rate of change of the voltage. The inductance of the SmCo FCL produces enough impedance for the FCL to achieve the desired voltage across the device. The limited peak fault current (I_{Lim_SmCo}) is 23 kA with a limited steady-state fault current ($I_{Lim\_SmCo\_SS}$) of 13 kA. Therefore, the SmCo core FCL produces a 54% reduction in peak fault current and a 50% reduction in steady-state fault current. The design specifications given in Table 8 have been achieved. The hysteresis curve for a SmCo core FCL is given in Figure 60.

Figure 60 - Hysteresis curve obtained in the simulation for a SmCo core using the Preisach model.

The SmCo core is able to limit much more of the fault current as its coercivity is greater than the M4 and AlNiCo cores. The SmCo core has a greater resistance to saturation and provides an effective inductance for a longer percentage of the fault current.

The hysteresis curve agrees with the input parameters for the SmCo core. Figure 61 shows the voltage across an NdFeB core FCL and the limited fault current through the NdFeB core during normal and fault limitation mode.

Figure 61 - Voltage across the FCL (top) and limited fault current with an NdFeB core (bottom).

The voltage across the NdFeB core FCL is 3.95 kV, which achieves the desired amount of voltage placed upon the device. The MOV conducts the switching transient as designed within 2 μ s to avoid component failure during the conversion from normal mode to fault limitation mode. The inductance created by the NdFeB core produces enough impedance to achieve the desired voltage across the device. The limited peak fault current (I_{Lim_NdFeB}) is 22 kA and the steady-state fault current is ($I_{Lim\_NdFeB\_SS}$) is 12.5 kA. The NdFeB core produces a 56% reduction in peak fault current and a 51.92% reduction in steady-state fault current. The NdFeB core achieves or exceeds the desired limitation requirements given in Table 8. Figure 62 shows the simulated hysteresis curve of an NdFeB core FCL.

Figure 62 - Hysteresis curve obtained in the simulation of an NdFeB-N42 core using the Preisach model.

The hysteresis curve shows the NdFeB core's wide range of fault current limitation. The core is able to provide a nonlinear inductance for a longer period because it does not saturate as quickly as AlNiCo and M4. In comparison with SmCo, the NdFeB core out performs but only slightly. A summary of the magnetic material characteristics for FCL applications is shown in Table 9.

Table 9 - Summary of magnetic material characteristics for FCL applications.

Property	NdFeB N42	SmCo 5	AlNiCo 8 Cast	Laminated Steel – M4
V_{FCL}	3.95 kV	3.8 kV	1.8 kV	1.2 kV
I_{Lim}	22 kA	23 kA	39 kA	44 kA
PR_{peak}	<u>56 %</u>	<u>54 %</u>	<u>22 %</u>	<u>12 %</u>
$I_{Lim_{SS}}$	12.5 kA	13 kA	22 kA	24 kA
PR_{SS}	<u>51.92%</u>	<u>50 %</u>	<u>15.38 %</u>	<u>7.69 %</u>

IV. Conclusions

In each of the cases, the voltage across the FCL before a fault occurs is zero because the FCL should have no current flowing through it and thus no voltage drop would occur. The result of no voltage drop is no losses during normal operation and increased efficiency of the system. For the given parameters, only the SmCo and NdFeB cores are feasible solutions. Laminated steel and AlNiCo cores would need to either increase in size or increase the number of turns to achieve the same fault current limitation results as the SmCo and NdFeB cores. The AC fault current magnetizes, demagnetizes and re-magnetizes each ferromagnetic core in the opposite direction of the first magnetization before demagnetizing again and repeating the cycle. Traversing the entire hysteresis curve allows for only one ferromagnetic core needed to limit a sinusoidal fault current.

The NdFeB core is chosen as the desired core instead of SmCo for FCL applications due to its cost advantage. While the SmCo magnets have a higher curie temperature, the FCL should not experience temperatures above 80⁰ C and since the limiting capability of NdFeB is greater than SmCo, NdFeB is the ferromagnetic material of choice. NdFeB approximately has a one-sixth size reduction as compared to the traditional laminated steel (M4) for an equivalent fault current limiting inductance. The size and weight reductions achieved by using an NdFeB core are of a particular importance for FCL applications in urban substations, which are limited on the available land for the FCL.

PROPOSED FCL DESIGN

I. A Neodymium Hybrid Fault Current Limiter

The proposed FCL is to include all of the advantages described in the literature review without any relevant disadvantages. A hybrid FCL topology is introduced which combines many advantages from different FCLs without any significant disadvantage. The hybrid FCL is shown in Figure 63 and includes a fast mechanical contact switch in parallel with a semiconductor switch, an NdFeB core, and an MOV.

Figure 63: Proposed Hybrid FCL

One novelty of this design is to develop a self-contained unit of solid-state turn-off switch in parallel with a fast mechanical contact system. The advantage of having a mechanical contact in parallel with the semiconductor switch is the absence of power

losses due to the voltage drop across the semiconductors while gated ON. Therefore, there will be no power losses during normal operation which is ideal for a FCL and the losses will only occur during fault current limitation mode as expected and not necessarily a concern. The fast mechanical contact switch does not need to be rated to interrupt the current but just to withstand the normal current and the voltage placed across it during limitation mode. Insulation of the voltage by the fast mechanical switch is crucial to the concept otherwise an arc will re-establish a path for the fault current to flow and no limitation will occur. By including a semiconductor switch in parallel with the fast mechanical contact switch, the mechanical switch will cost less since no interruption of current is needed by the mechanical contact. The mechanical contact switch will not incur an arc while opening since the semiconductors provide an alternative path for the current to flow. It simply just transfers the current to the semiconductors, which perform the interruption and transfer the fault current to the ferromagnetic core. The semiconductor switch must be able to conduct the fault current for at least 1 ms and the rated current for 1 second in case the mechanical switch fails to operate.

Therefore, the FCL is proposed to be a Neodymium hybrid FCL which is designed as a SCFCL but instead of using Iron as the core material, a stronger, more permeable material such as NdFeB will be used as the entire core material. This should reduce the core size by about one-sixth while maintaining the same or better fault current limiting characteristics. The operation principle of the ferromagnetic material is once the NdFeB material has been saturated, the ferromagnetic properties of NdFeB require the dipoles of the material to exert more work to change direction of their orientation thus producing a higher inductance to limit the fault current. NdFeB is the strongest magnet in

production today and it uses the rare earth metal, Neodymium (Nd), which has one of the strongest magnetic permeability's for any ferromagnetic material. The type of NdFeB material chosen to be in the proposed design is NdFeB (N52) due to the highest remanence value and maximum energy handling capability of 52 MGOe [33]. Another advantage of this system is the DC bias system typically used in saturable cores will be removed completely so as to not constantly require a DC power source, therefore, saving power from constantly applying the DC current to the core and avoiding high fault current in the DC circuit. This improves efficiency and lowers cost of the proposed FCL. A Metal Oxide Varistor (MOV) will be applied in parallel to the FCL to provide over-voltage support due to lightning strikes. A summary of the advantages of the proposed FCL is given below.

Advantages of the proposed device are:

1. No voltage drop during normal operation
2. No continuous power losses due to ON-state voltage drop of the semiconductors or low inductance value of the saturable core.
3. Cheaper mechanical contact system since there will be no interruption by the mechanical contact which results in no damage to the mechanical contact itself.
4. Temperature of semiconductors and saturable core are almost negligible because they will only operate for small amounts of time (ms).
5. Smaller saturable core design with improved fault limitation.
6. Removal of the DC bias system completely which in turn reduces operating cost and simplifies the design.

7. Over 1 second fault handling capability and should effectively limit the fault current longer.
8. Potential marketability for utilities to install the device and protect current systems. Also, can be used in all power electronic based systems such as the FREEDM System.

A. Operating Principle

This idea is different from all the previous hybrid FCL concepts, as it truly would create self-contained switch modules and would need a controller to send the appropriate gate signals. The operating principle begins under normal operation, where the line current will go through the fast mechanical contact system, while everything else is OFF. Once a fault occurs the operation is as such:

1. Turn ON the semiconductor switches quickly to provide an alternate path for the fault current.
2. Then open the fast mechanical contact system.
3. Once the mechanical switch is open, turn OFF the semiconductor devices to force the current through the NdFeB ferromagnetic core.
4. Stay in the faulted state until the fault has been removed by a breaker down the line or until the line is taken out of service due to a continuous fault.
5. Once the fault has been cleared, close the fast mechanical contact switch and begin normal operating mode.

Steps 1-4 should all happen as fast as possible and should occur before the initial peak of the fault current reaches its maximum value (4-5 ms). The goal is to have this device detect and operate within 1 or 2 ms to reduce the initial peak of the fault current.

Currently, saturable core devices can operate within 4 ms but they are in series with the transmission line, thus having normal operating losses of approximately 1-2% [16]. The semiconductor switches must be able to switch off the fault current and withstand the high voltage across it without breaking down. However, the semiconductor switch will not need to commutate the full peak fault current but only a percentage of it depending on the operation speed of the controller and in particular the mechanical switch. The fast mechanical contact switch would not need to interrupt the current but transfer it to the semiconductor switch and be able to withstand the voltage placed upon it once opened. Otherwise an arc could occur which would re-establish current flow through the mechanical switch preventing any fault current limitation. There should be no arc while transferring the current to the semiconductor switch thus prolonging the life of the metal contacts significantly by eliminating any degradation caused by an arc.

Another application for this device could be in temporary upgrading of a substation. Utilities could use a forklift or an 18 wheeler and transport the proposed device to a system than needs a breaker or transformer upgrade and could temporarily be connected to the line until these upgrades are made. Then it could be disconnected and transported to another substation that needs upgrading and so forth. In addition, this device could potentially be the utility short circuit current limiter mentioned in the FREEDM loop protection project. The proposed FCL could be designed to limit the fault current to a 50% reduction upon request.

B. Controller Operation

A novel controller must be developed because standard commercial relays such as the SEL 551 from SEL laboratories are too slow to operate and detect the fault in one-

quarter cycle. The fastest operating time of a SEL 551 is 40 ms which is too slow for this FCL application [35]. Also, the detection time for a fault is at worst 5 ms which is also too slow for the proposed FCL operating time. Furthermore, a different detection control scheme is needed and is presented below. The controller is sampling at 5 kHz or every 200 μ s. The control algorithm used in detecting the fault and maintaining the faulted state uses two key methods of detection. The first method is the overcurrent method where an arbitrary preset value (M_1) is compared to the absolute value of the current magnitude. If the magnitude of the current exceeds M_1 then a fault has occurred and the controller operates the FCL as previously described. M_1 is chosen in the simulations as twice the nominal current but can be changed to allow for faster or slower operation of the FCL as desired.

The second method of detection used is the rate of change of the current method ($\frac{di}{dt}$) or the slope. The controller stores the previous current measurement as an old measurement. At the next sample, the magnitude of the current is measured and subtracted from the previous measurement. This result is divided by the sampling time-step or the sampling frequency, which is 200 μ s. Then an absolute value is taken of this result and compared to the arbitrary value M_2 . M_2 is pre-determined and is typically 2-5 times the maximum value of the rate of change of the nominal current. This method approximates the slope of the current and is typically the initial triggering detection method of a fault but not always. Changing M_2 will cause the controller to operate faster or slower depending on the desired user's requirements.

In addition, safety measures have been implemented in the controller to insure the controller does not operate incorrectly. For example, if the controller fails to operate or if

the semiconductors breakdown, the entire system will default to its normal operating state, inherently acting like the FCL is not in the line. If the mechanical switch bounces or an arc is established because the insulation is not adequate at any point in the limitation process the controller will revert to the beginning of operation and begin the fault sequence again until the operation occurs as designed. At each point in the operation, the current through the mechanical contact switch (I_{Mech}) and the semiconductor switch (I_{Semi}) are monitored. If the current is not equal to zero when the mechanical switch is supposed to be open or when the semiconductor switch is supposed to be OFF, then the controller will restart the operation of the FCL from the beginning.

C. Feasibility of the Proposed FCL.

The feasibility of the proposed FCL is determined by surveying current commercial products that can meet the desired specifications of the proposed FCL. For example, ABB Inc. has produced a fast mechanical contact switch that can operate at 36 kV_{RMS}, 50 kA_{RMS}, can withstand the fault current for at least 1 second and can operate less than 1.5 ms [36]. For the semiconductor switch, Mitsubishi Electric is one of many companies that produce high power (>1kV) IGBTs. Mitsubishi Electric commercially has a 6.5 kV, 750 A IGBT that would need to be cascaded with 40 devices in parallel for a maximum of 30 kA and at least 2 devices in series for a total voltage of 13 kV [37]. However, these IGBT modules can provide 10.2 kV of isolation for a minimum total of 20.4 kV blocking capability. The operation time of the IGBT module is 1.8 μ s turn ON delay with a maximum of 9 μ s turn OFF delay [37]. For the MOV, Copper Power Systems currently produces surge arresters from 3-345 kV with 100 kA withstand capability [38]. The feasibility

ity of the fast mechanical contact switch, the semiconductor switch, and the MOV are all proven by the availability of commercial products. The operation of each of the devices is within the requirements for the proposed FCL and the high voltage model can be built using the presented parts or any substitutions from other competitors.

II. Finite Element Analysis

Since the core material has been chosen as NdFeB and the core shape has been designed, the next step is to determine the minimum size of copper coils needed within the design constraints and the current application. To perform the copper coil analysis, Finite Element Analysis (FEA) is performed to structurally determine if the coils can withstand the short-circuit current placed upon it during fault limitation mode. The intent of the investigation is to identify potential mechanical failures of the proposed FCL with the pre-determined electrical design constraints. Finite Element Analysis is performed on the high voltage model as shown below. The FEA simulations were performed by Jorge Mendoza who is an undergraduate researcher that I supervised and mentored during the design process. With my guidance, he performed the FEA simulations and reported the results to me on a weekly basis.

A. High Voltage Model

The high voltage model simulates the mechanical forces that will be present during a prospective steady-state fault current ($I_{SC_{SS}}$) of 26 kA. The system consists of copper wire coiled cylindrically around the ferromagnetic core. The structural scenario imitates a thin walled cylindrical pressure vessel. The method described is the accepted

model for transformer design [39]. Simulations were conducted using the ANSYS static structural analysis software.

The radial forces on the copper wire are produced by the axial flux interaction caused by the current passing through the wire. The mean radial force is given by (5-1).

$$F_{radial} = \frac{2\pi(NI_{Lim})^2 D}{h} * 8.8964 * 10^{-8} \quad (5 - 1)$$

Where I_{Lim} is the limited peak fault current, D is the mean diameter of the coil, h is the height of the coil, and $8.8964 * 10^{-8}$ is the constant conversion from tons to newton. The radial force in (5-1) will create tensile stress on the outer winding of the coil and compressive stress on the inner winding. Typical failures occur at the maximum tensile stress of the coil [40], as described by (5-2).

$$\sigma_{radial} = \frac{F_{radial}}{2\pi A_{wind}} \quad (5 - 2)$$

Where σ_{radial} is the maximum tensile stress of the coil given in $\frac{N}{m^2}$ and A_{wind} is the cross-sectional area of the wire. The axial forces are generated as a result of the radial flux interaction caused by the current passing through the coil [40]. The mean axial force is given by (5-3).

$$F_{axial} = \frac{2\pi^2 A_{wind} (NI_{Lim})^2 D}{h_{eff}} * 8.8964 * 10^{-8} \quad (5 - 3)$$

Where h_{eff} is the effective height or distance between the ferromagnetic core legs. The mean stress due to axial forces is given by (5-4).

$$\sigma_{axial} = \frac{F_{axial} l_{coil}^2}{2t_{coil} b^2} \quad (5 - 4)$$

Where l_{coil} is the distance between the coils, t_{coil} is the radial dimension of the coil, and b is the axial dimension of the coil. The calculated stress analysis results were modeled to define a structurally stable base size for the copper winding under radial stress of a 26 kA prospective steady state fault current to determine the worst-case scenario for safety purposes. This scenario simulates the situation of no limitation of the fault current in case of FCL failure. An assumption with the model is the mechanical failure would most likely occur from the radial forces produced by the fault current instead of the axial forces due to the specific design of the core [39]. Therefore, only the radial forces are calculated and simulated. Finite Element Analysis is performed to determine the feasibility of different gauges of wire for this FCL application. Figure 64 shows the stress analysis of a 0 AWG wire when subjected to a prospective steady-state fault current of 26 kA which is the worst-case scenario and should be simulated for safety purposes.

Figure 64 - Simulated stress subjected to the 0 AWG wire during fault limitation mode.

The maximum simulated radial stress for a 0 AWG copper wire is 131.6 MPa and is less than the maximum structural strength of the copper of 140 MPa [41]. Although the result is close to the maximum tensile strength of copper, the simulated current of 26 kA through the coils is the worst-case scenario and the mechanical limits should not be reached under any operating conditions.

The test is repeated for 00 AWG, 1 AWG, and 2 AWG copper wires to determine the minimum size of copper wire needed for the proposed FCL. A summary of the copper coil stress analysis results are shown in Table 10.

The minimum wire gauge needed for the FCL application is 0 AWG. Any wire gauge larger than 0 AWG should theoretically maintain structural integrity while subjected to the electrical design constraints of the proposed FCL. The percent error is calculated from the theoretical and simulated stress and is given in Table 10. The minimum and maximum structural energy error is given directly from ANSYS in joules and applies to the calculation error when simulating the stress placed upon the coils. The FEA simulation is concluded to be accurate since the error is in magnitude of picojoules. These results are only valid for the current dimensions and would need to be simulated again with different system and core parameters.

Table 10 – Copper coil stress results.

Wire Gauge (AWG)	Radial Force (kN)	Calculated Theoretical Stress (MPa)	Simulated Stress (MPa)	Percent Error	Max Structural Energy Error (pJ)	Min Structural Energy Error (pJ)
00	709.3	87.6	93.43	6.69%	116	57.8
0	736.8	124.2	131.6	5.93%	83.6	41.8
1	894.5	175.7	184.9	5.24%	67.3	33.6
2	1,005.3	249.4	261.03	4.67%	58.0	29.0

III. Neodymium Core Optimization

A method to optimize the NdFeB core design is developed using Mixed Integer Programming (MIP) techniques. The chosen optimization program is A Mathematical Programming Language (AMPL), which interfaces with several different solver programs to solve optimization problems. The chosen solver is knitro due to its ability to converge to a solution with nonlinear constraints. The program is not designed to be an exact solution, as some of the nonlinearities are not accounted for and approximations are made for these nonlinearities; however, it should give a very good approximation to the actual core design. Although the optimization method is designed for NdFeB, any ferromagnetic material will work with the proposed core optimization method with only small changes in the core's physical and magnetic input parameters. Some design assumptions were made in the program such as the core is split up into two sections and is labeled in Figure 53. Each section has a second identical section. For example, the top horizontal section has the same dimensions as the bottom horizontal section and both vertical sections of the core are also of the same dimensions. The width is constant throughout the entire core to ensure conformity. Another core design assumption is the height of the horizontal sections is equal to the length of the vertical sections, which creates a square design.

The program is designed to optimize the physical and electrical properties of the ferromagnetic core with given system parameters while meeting the user's desired fault current limitation level. The objective is to minimize the costs to build the ferromagnetic core, which includes the cost of the magnets and the cost of the copper wires as shown in (5-5). Installation costs and the casing design were neglected in the model. Currently, only 1 size of NdFeB magnet is used but implementing multiple sizes of magnets and dif-

ferent ferromagnetic materials could be used to determine an overall cheaper core and improve the robustness of the optimization program.

$$\min \sum_{\forall n \in N} P_n \text{Mag}_n + G P_n \text{wirelength}_n \quad (5-5)$$

subject to:

A. Physical constraints for core dimensions:

$$\text{Mag}_n = \sum_{\forall s \in S} 2(\text{numlength}_s + \text{numwidth}_s + \text{numheight}_s) \quad (5-6)$$

$$\text{numlength}_{n+1} = \frac{hcore_n}{length_n} \quad (5-7)$$

$$\text{numwidth}_{n+1} = \text{numwidth}_n \quad (5-8)$$

$$\text{numheight}_{n+1} = \frac{(hcore_{n+1} - 2 * hcore_n)}{height_n} \quad (5-9)$$

$$lcore_n = length_n * \text{numlength}_n \quad (5-10)$$

$$wcore_n = width_n * \text{numwidth}_n \quad (5-11)$$

$$hcore_n = height_n * \text{numheight}_n \quad (5-12)$$

$$length_n \leq lcore_s \leq 10 * length_n \quad (5-13)$$

$$width_n \leq wcore_s \leq 10 * width_n \quad (5-14)$$

$$height_n \leq hcore_s \leq 10 * height_n \quad (5-15)$$

$$lcore_1 = hcore_2 \quad (5-16)$$

$$lcore_2 = hcore_1 \quad (5-17)$$

$$wcore_1 = wcore_2 \quad (5-18)$$

$$Acore_n = hcore_n * lcore_n \quad (5-19)$$

$$Acore_n \geq length_n * width_n \quad (5-20)$$

$$lmean_n = 2(lcore_n - lcore_{n+1}) + 2(hcore_{n+1} - hcore_n) \quad (5 - 21)$$

Equation (5-6) sums up the number of magnets needed for the length, width, and height dimensions of the optimized core. (5-7), (5-8), and (5-9) are used to calculate the number of magnets that make up each section of the core design as shown in Figure 53 and are integers because fractions of a magnet are not possible when only one size of magnet is used. Eq. (5-9) subtracts $hcore_1$ from $hcore_2$ to account for the magnets already being counted in the horizontal legs of the core for the total magnets needed calculation in (5-7). The width of the core is assumed to be constant throughout the core and is guaranteed by (5-8) and (5-18). Equations (5-10), (5-11), and (5-12) are used to calculate the dimensions of the core based on the input dimensions of an individual core and the number of individual cores needed.

Equations (5-16), (5-17), and (5-18) are used to guarantee the desired core shape such that the core is a square. The length of each section is equal to the height of the opposite section as shown in Figure 53. Equations (5-13), (5-14), and (5-15) are practical constraints such that the core cannot physically become prohibitively large and expensive. These constraints aid the program in converging to a solution. Changing the maximum amount of magnets from 10 to 20 in (5-13), (5-14), and (5-15) does not alter the solution. The number of cores can be expanded to account for higher voltages and currents but 10 or 20 are acceptable for the system parameters given in Table 8. The cross-sectional area is constrained by (5-19) and (5-20) as the cross-sectional area must equal the height of the bottom horizontal leg multiplied by the width and it cannot be smaller

than the dimensions of a single individual core. The mean path length of the core is calculated in (5-21).

B. Physical constraints for copper wires:

A FOR loop is used to search through the American Wire Gauge table in Appendix C to determine an acceptable wire gauge based on the nominal current and is shown below. The FOR loop selects the minimum wire gauge size needed based on the current rating of the wire. In a NEC wire gauge table the rating is based off of very conservative 1A/700 mil for long wires. A safe assumption of 1A/200 or 300 mil is used in the optimization program for short wires and justifies the 3 times the wire rating. It is assumed the smallest wire gauge is the cheapest wire gauge and once determined, the wire size is saved and the FOR loop is exited. However, prices for each wire gauge can be updated periodically and the cheapest wire can be selected.

for ($g < \text{Gaugenum}$)

if ($3 * \text{GaugeAmpacity}_g > I_n$)

$$\text{wirediameter} = \text{diameter}_g \quad (5 - 22)$$

$$\text{Gauge} = \text{Gaugesize}_n \quad (5 - 23)$$

$$\text{GP}_n = \text{GP}_g \quad (5 - 24)$$

$$\text{wireres}_n = \text{GaugeRes}_g \quad (5 - 25)$$

break;

end

end

$$0.8(h\text{core}_{n+1} - 2 * h\text{core}_n)(l\text{core}_n - 2 * l\text{core}_{n+1}) \geq N_n * \text{wirediameter}_n^2 \quad (5 - 26)$$

$$\text{wirelength}_n = 2 * (2 * w\text{core}_n + 2 * l\text{core}_{n+1}) * N_n \quad (5 - 27)$$

The physical constraints are included to insure the core dimensions are compliant with the core design. Constraints (5-22), (5-23), (5-24), and (5-25) aid in selecting the appropriate wire gauge and use these selected dimensions in further calculations. Equation (5-26) constrains the number of turns to a maximum of 80% of the inner air gap of the core, which is the area between both the vertical and horizontal legs. Also, any adjustments to the number of turns can be made without having to modify the core dimensions. An approximation is made to the amount of copper wire needed in (5-27) as with each level of turns, the length of each turn increases due to overlapping. As the turns occupy more inner area of the core, the length increases; to account for this overlap the wire length needed is multiplied by a factor of 2.

C. Electrical constraints:

$$\mu_{core_n} = \frac{B_{sat_n}}{(H_{sat_n} - H_{c_n})} \quad (5 - 28)$$

$$L_n = \frac{\mu_0 \mu_{core_n} N_n^2 A_{core_n}}{l_{mean_n}} \quad (5 - 29)$$

$$I_{sc\_new_n} = \frac{V L N_n}{\left(2\pi L_n + \frac{V L N_n}{I_{sc_n}}\right)} \quad (5 - 30)$$

$$I_{ss\_new_n} = \frac{V_n}{\left(2\pi L_n + \frac{V L N_n}{I_{ss_n}}\right)} \quad (5 - 31)$$

$$PR_{sc_n} = \frac{I_{sc_n} - I_{sc\_new_n}}{I_{sc_n}} \quad (5 - 32)$$

$$PR_{ss_n} = \frac{I_{ss_n} - I_{ss\_new_n}}{I_{ss_n}} \quad (5 - 33)$$

$$PR_{sc_n} \geq PR_{min_n} \quad (5 - 34)$$

$$PR_{ss_n} \geq PR_{min_n} \quad (5 - 35)$$

A linear approximation is made with (5-28) as it calculates the maximum permeability of the core during its transition from saturation and into unsaturation and then to reverse saturation. This transition is nonlinear and is the property that produces the nonlinear inductance, which limits the fault current. In this optimization program, the maximum value of μ_{core_n} is of concern as the maximum fault current is limited when the core is at its maximum permeability. Another way to calculate μ_{core_n} is to input it into the simulation by obtaining it from the slope of the demagnetization curve provided by the manufacturer or by using different methods such as the Jiles-Atherton or the Preisach method.

Faraday's Law is used to calculate the inductance produced by the ferromagnetic core in (5-29). μ_{core_n} is dependent on the magnetic properties of the ferromagnetic material. N , A_{core_n} and l_{mean_n} are all variables and can be optimized to produce the maximum amount of inductance for the lowest cost. The new peak and steady state short-circuit current is calculated in (5-30) and (5-31) respectively, with the FCL's inductance inserted in the line.

Equations (5-32) and (5-33) determine the minimum amount of fault current reduction achieved by the current ferromagnetic core design. The desired minimum percent reduction is given by the user but is typically between 45-55% while (5-32) and (5-33) only guarantee that the limitation is greater than or equal to the desired limitation requirement, it does not guarantee the range of limitation. The percent reduction can be between the user's desired minimum and 100% reduction. However, limiting the fault current to zero (100%) will never be achieved because it is too expensive when compared to

the minimum limitation requirement. The ferromagnetic core would essentially act as a circuit breaker.

The optimization program includes the following parameters and variables as inputs, which are dependent on the physical, electrical, and magnetic characteristics of the ferromagnetic material. The core design is optimized based on the user's system information such as voltage and current levels. Table 8 gives the input table of system parameters with the desired level on limitation. Table 11 gives the input data for the ferromagnetic material.

Table 11 – Ferromagnetic material input data.

Parameter	Symbol	Value
Length (m)	<i>length</i>	0.102
Height (m)	<i>height</i>	0.102
Width (m)	<i>width</i>	0.0508
Price (\$)	P_n	821.65
Weight (lbs)	<i>weight</i>	8.675
Remanence Flux Density (T)	B_{Rem}	1.48
Saturation Flux Density (T)	B_{Sat}	1.6
Coercivity (kA/m)	H_C	891.3
Saturation Coercivity (kA/m)	H_{Sat}	986.3
Permeability of Free Space (H/m)	μ_0	$4\pi * 10^{-7}$

Table 12 gives the results of the optimization program, which includes the design parameters of the core, cost of the core, and the percent reduction of both the peak and steady-state fault current.

Table 12 – Optimized ferromagnetic core design results

Parameter	NdFeB Core
Total cost of the core (\$)	\$16,818.13
Area of the core (m ²)	0.0052
Mean path length (m)	2.0866
Number of turns	436
Overall dimensions (l x w x h) (m)	0.6236 x 0.508 x 0.6233
Weight (lbs)	177.6
Maximum inductance (mH)	0.625045
Percent reduction peak	62.07 %
Percent reduction steady-state	45.00 %
Number of magnets needed	20
Wire gauge needed	500 MCM
New peak fault current level (kA)	18.965
New steady-state fault current level (kA)	13.750
Number of magnets needed for length(1)	6
Number of magnets needed for width(1)	1
Number of magnets needed for height(1)	1
Number of magnets needed for length (2)	1
Number of magnets needed for width(2)	1
Number of magnets needed for height(2)	4

The desired percent reduction of 45% has been achieved for both the peak and steady state fault current levels. The peak and steady state fault currents are reduced to 18.965 kA and 13.75 kA respectively. The wire gauge needed is determined to be 500 MCM with 436 turns. The total cost for the core material is \$25.919.42 for single-phase

protection. To protect a three phase system there would need to be 3 similar cores for each line which brings the total cost to \$77,758.26 not including labor costs.

In comparison with a SCFCL in [16], a three phase FCL costs between \$200,000 and \$300,000. The optimization method has reduced the cost by approximately 3-4 times in comparison with the designs in [16] while maintaining the user's request for a 45% reduction of both the peak and steady state fault current. The weight has also been reduced from 20,000 - 50,000 lbs to 177.6 lbs due to iron's relative weight when compared to NdFeB. The 177.6 lbs core weight does not include the weight of the casing just the ferromagnetic core weight as the casing would add additional weight.

IV. Conclusions

In conclusion, a novel hybrid FCL is presented that utilizes an NdFeB core as the limiting inductance. The operating principle of the proposed FCL is described as well as the control techniques used to detect a fault. The nonlinear hysteresis effects of a ferromagnetic core are exploited and utilized for fault current limitation purposes. The proposed FCL has the following distinct advantages:

1. No voltage drop during normal operation which equates to zero continuous power losses due to ON-state voltage drop of the semiconductors or low inductance value of a saturable core.
2. Cheaper mechanical contact system since there will be no interruption (arc) by the mechanical contact which results in no damage to the mechanical contact itself.

3. Temperature of semiconductors and saturable core are almost negligible because they will only operate for small amounts of time (ms). For example, a 26 kA fault current for 1 ms results in a dissipation of 26W. However, if the 26 kA fault current is conducted for 10 ms the resulting power dissipation is 260 W and the semiconductor switch can easily accommodate this power dissipation.
4. Smaller saturable core design (one core) with improved fault limitation.
5. Removal of the DC bias system completely which in turn reduces operating cost, material cost and simplifies the design.
6. At least 1 second fault handling capability and should effectively limit the fault current longer. The feasibility of this statement is shown in Chapter 6.
7. Potential marketability for utilities to install the device and protect current systems. Also, can be used in all power electronic based systems such as the FREEDM System or as a temporary solution for utility upgrades.

Finite Element Analysis is performed on the copper coils to structurally determine the minimum gauge of wire needed for the high voltage model. For the high voltage model, wire gauges from 0 AWG and greater can structurally handle the 26kA steady-state fault current placed upon it without physically breaking. The error in the simulated stress is of picojoule magnitude and it is concluded that the simulations are accurate. The theoretical and simulated stress varies by 4-6% but is still within the maximum value of stress of copper (140 MPa). The FEA results were produced by Jorge Mendoza during his work as an undergraduate researcher as I supervised him and provided him with guidance.

A Mixed Integer Programming (MIP) optimization method has been developed to determine a physical design for a ferromagnetic core used in fault current limiter applications. The optimization program optimizes the core dimensions for the lowest cost while meeting the specific user's requirements such as the amount of fault current reduction desired. The optimization method is developed as a general method where a user can input their specific system requirements and run the optimization program to obtain the optimized core design for their given system inputs.

the electrical resistivity of the core. The inductance is calculated by equation (4-14) at each time step and updated for the next time step. The input in Figure 66 is the current through the ferromagnetic core and the output is the current to the load.

Figure 66 – PSCAD model of NdFeB core.

The NdFeB core is modeled as a nonlinear inductor that is controlled by a set of equations described by the Jiles-Atherton method of hysteresis in Chapter 4. The NdFeB characteristics are described in Table 13.

Table 13 – NdFeB N52 parameters.

Property	NdFeB N52
N	436
$A_{\text{core}} (\text{m}^2)$	0.0052
$I_{\text{mean}} (\text{m})$	2.0866
$B_{\text{rem}} (\text{T})$	1.48
$B_{\text{sat}} (\text{T})$	1.6
$H_c (\text{kA/m})$	891.3
$\rho (\Omega \cdot \text{m})$	1.6×10^{-6}

The equation for the nonlinear inductance is shown implemented in PSCAD in Figure 67, which is described by equation (4-14).

Figure 67 – PSCAD inductance calculation.

PSCADs standard units are in kA instead of A so a factor of 1000 must be applied to the result of the inductance in Henry. H_{hys} is the current value for the applied field strength after the hysteresis calculation has taken place. Each point on the hysteresis curve is calculated at each time step and the updated inductance is inserted into the system. Equations (4-2), (4-6)-(4-8) are realized by the exponential approximations given in equations (4-3)-(4-5) and (4-9)-(4-14). The implemented Jiles-Atherton method of hysteresis in PSCAD is shown below in Figure 68 as block diagrams. A selector switch is used to change between equations (4-2) and (4-6) as well as (4-7) and (4-8) when calculating the flux in the core.

α is chosen to be 0.8 for curve fitting purposes most similar to NdFeB. When the current reaches a values less than $1 \mu\text{A}$, the approximation functions are used ((4-6) and (4-8)) in place of the hyperbolic functions due to the equations becoming unstable. A comparator is used to determine when to switch between the two functions.

In PSCAD, control logic had to be developed to accurately model the hysteresis loop of a ferromagnetic material in PSCAD based upon the previous state of hysteresis. The hysteresis curve is divided into 4 cases which gives PSCAD the correct state of hysteresis. Each of the four cases developed are to determine which equation to use while traversing through the hysteresis loop. All four cases are shown below in Figure 69 and correspond to a particular section of the BH curve.

Figure 69 – Hysteresis loop controller.

The purpose of using the cases is to determine which curve should be used. The BH curve is broken down into two symmetrical curves with the only difference being the

intersection of the x-axis or $\pm H_c$. Equation (6-1) describes the two options H_{hys} can take depending on the previous current values.

$$H_{hys} = H \pm H_c \quad (6 - 1)$$

Each of the cases described above select whether H_c should be positive or negative for the correct H_{hys} calculation which insures hysteresis is modeled correctly during the simulations. The cases shown in Figure 69 are described by the equations below in Table 14.

Table 14 – Hysteresis loop logic.

	$B(H) \geq B_{sat} $	$B(H) < B_{sat} $
$H \geq 0$	Case 1: $H_{hys} = H + H_c$	Case 2: $H_{hys} = H - H_c$
$H < 0$	Case 4: $H_{hys} = H + H_c$	Case 3: $H_{hys} = H - H_c$

Table 14 shows the 4 different cases used in the hysteresis logic and the conditions needed when determining which symmetrical curve to use. The logic is needed to determine the appropriate value for H_{hys} during the simulations.

The controller described in Chapter 5 is implemented in PSCAD as standard logic blocks in the PSCAD library. There are six inputs to the controller but only 2 outputs to the FCL which are the gate signals of the fast mechanical contact switch and the semiconductor switch. The six inputs are the load current, M_1 , M_2 , semiconductor current, fast mechanical contact current, and current through the ferromagnetic core. Each of these input signals are needed to properly operate the proposed hybrid FCL's control system.

Figure 70 – Fault detection algorithm of the controller.

Step one of the controller is to detect the fault, which is shown below in Figure 70. The input to the controller is the instantaneous current magnitude. Sampling occurs at 5 kHz and the absolute value of both the current magnitude and slope of the current are compared with the M_1 and M_2 values respectively. A start-up delay of 150 ms is chosen to prevent accidental switching while the line is initially energized. If either constraint is violated a fault is set to occur. The system is allowed to reach a steady state before the fault detection is activated. To insure unwanted switching, a counter is implemented to 50 such that there must be 50 consecutive normal conditions before the FCL will return to normal operating mode. The output of step 1 is a logic signal that determines if the system is experiencing a fault or not.

semiconductors until the mechanical switch has zero current flowing through it, the arc typically seen when opening up a breaker would be nonexistent thus lengthening the life of the mechanical contact switch. Step 4 is shown below in Figure 72.

Figure 72 – Step 4 of the control algorithm.

Again, a turn OFF delay is implemented to model the physical time of the semiconductor switch turn OFF. The output of step 3 is given as the input in step 4. Finally, step 5 in the control algorithm is to send the appropriate gate signals to the semiconductor switch and the fast mechanical contact switch. Figure 73 shows step 5 of the control algorithm.

fault current while Figure 76 shows a zoomed in version of the first fault in Figure 75. The top graph in Figure 75 is the line current which normally is 1.2 kA but the line current increases to 50 kA peak and 25 kA steady-state during a fault. The bottom graph in Figure 75 is the input voltage or the source voltage with a voltage value of 7.2 kV_{LN}.

Figure 75 – Prospective fault current.

Figure 76 – Zoomed in version of Figure 75.

With the design parameters in Table 13, the proposed hybrid FCL is included in the line. Figure 77 shows the limited fault current provided by the proposed hybrid FCL.

Figure 77 – Limited fault current and voltage with FCL.

The top graph in Figure 77 is the line current while the bottom graph is the voltage across the load (green) and the FCL (red). For the top graph, the green line is the current in the fast mechanical contact switch, the blue line is the line current, and the red line is the current through the NdFeB core windings. For both of the faults, the maximum limited peak fault current is 18.75 kA while the steady-state current is 13.65 kA. The peak current is limited by 62.5% and the steady-state current is limited by 45.4%. The desired limitations in Table 8 are thus achieved with the core design characteristics. Figure 78 shows a zoomed in version of Figure 77.

Figure 78 – Zoomed in version of Figure 77.

The proposed hybrid FCL produces a sinusoidal limited fault current instead of a square wave or any other type of distorted wave. A majority of the voltage is placed upon the FCL during fault limitation mode but the NdFeB is able to provide a nonlinear inductance, which limits the prospective fault current levels. The load voltage is also phase shifted due to the introduced inductance from the NdFeB core. In Figure 78, the FCL current and load current are identical and in PSCAD only the FCL line is shown even though the load current follows the curve exactly. Figure 79 shows the initial peak of the fault current and the limitation effect of the proposed hybrid FCL.

Figure 79 – Initial switching of the proposed FCL.

The fault is detected at the initial sampling time and is set to begin fault limitation mode because M_2 is violated. The entire transition to fault limitation mode occurs within 1.5 ms as shown by Figure 79. The limiting factor in the proposed FCL is the fast mechanical contact switch as it can only open within 1 ms. If the fast mechanical contact switch could operate faster, the initial peak of the fault current before limitation occurs would be reduced. The top graph is the current and the bottom graph is the voltage. The load current (blue) follows the FCL current (red) once the transition has occurred. The proposed FCL is able to limit the rising fault current of 50 kA to 18.75 kA and steady-state current to 13.7 kA. The correct operation of the proposed FCL is shown in Figure 80.

Figure 80 – Switching state of proposed FCL.

The entire switching operation of the fast mechanical contact switch and the semiconductor switch occurs within 1.5 ms. The top graph in Figure 80 is the current while the bottom is the voltage. The fast mechanical contact switch current and the load current are identical before and during the first part of fault inception. However, the mechanical contact switch is opened (blue line) after the semiconductor switch (green line) is turned ON but before it is turned OFF as described in Chapter 5. A time delay is included to model the physical time it takes to open the mechanical switch and turn ON/OFF the semiconductor switch that is shown in Figure 71 and Figure 72. The semiconductor switch turns OFF approximately 100 μ s after the fast mechanical contact switch is opened and the entire hybrid FCL is operating as designed. For a worst-case scenario, 100 μ s is used as the switching time and is approximately 10 times greater than the com-

mercially available switch mentioned in Chapter 5. The fault detection control techniques are shown in Figure 81 with a zoomed in version in Figure 82.

Figure 81 – Fault detection algorithm.

Figure 82 – Zoomed in version of Figure 81.

The pink line in Figure 82 shows the threshold values M_1 and M_2 for fault detection. The controller operates as expected and there is no improper switching due to errors or wrong identification of fault current existent in the system. M_2 does set off the controller before M_1 is exceeded but comparing the top graphs (slope) in Figure 81 and Figure 82 with the middle graphs (magnitude). The peak of the slope occurs when the magnitude is at its lowest point and the lowest point of the slope occurs as the magnitude is at its peak, which is the expected result for a sinusoidal wave. The bottom graph in both Figure 81 and Figure 82 is the fault signal, which determines if the system is in a faulted state or normal operation.

An XY plot in PSCAD is used to plot the hysteresis curve experienced by the NdFeB core during fault limitation mode and is shown in Figure 83. The Jiles-Atherton accurately models the hysteresis of the NdFeB core as the remanence flux (B_{rem}) and the coercivity (H_c) are achieved by the manufacturer specifications in [33]. As the current rises, the NdFeB core is introducing its nonlinear inductance as dictated by the slope of the hysteresis loop. The NdFeB core traverses the hysteresis loop every cycle of AC current and achieves the desired limitation requirements described by the system input parameters. The equations used to produce Figure 83 are (4-2) through (4-15) and the implementation of the equations in PSCAD is shown in Figure 68. The x-axis is H in kA/m and the y-axis is B in T.

Figure 83 – Hysteresis curve of the NdFeB core.

A statistical study covering a variety of potential scenarios has been performed and the results are presented below. In this study, the system fault current magnitude is varied to determine the limiting effect of the hybrid FCL over a range of different current magnitudes. Five case studies were performed that varied by degree of magnitude of 5 kA each. The simulations were performed with 30 kA, 35 kA, 40 kA, 45 kA, and 50 kA peak fault current levels and the FCL's performance is tracked and analyzed. In addition to the varying fault current magnitudes, the fault inception angle is also varied by 1ms for 2 cycles. This variation amounts to 34 tests performed for each peak fault current magni-

tude. The average values, standard deviation, minimum, and maximum for each scenario are presented below. The results of this study are given below in Table 15.

Table 15 – Statistical Analysis of Hybrid FCL's performance

50 kA Potential Peak Fault Current				
	<i>Delay (ms)</i>	<i>I_{pk} (kA)</i>	<i>I_{ss} (kA)</i>	<i>V_{pk} (kV)</i>
Min	0.11	13.75504256	13.2731447	19.20386076
Max	2.31	24.05426763	13.31680404	20.01093506
Mean	0.427647059	20.22734206	13.29249462	19.74562193
Std. Dev	0.600230636	3.353831261	0.011252799	0.225136514
45 kA Potential Peak Fault Current				
	<i>Delay (ms)</i>	<i>I_{pk} (kA)</i>	<i>I_{ss} (kA)</i>	<i>V_{pk} (kV)</i>
Min	0.11	13.43594833	12.85489345	19.09268791
Max	3.11	22.77450059	12.86332002	19.9600973
Mean	0.615882	19.24954334	12.85804262	19.71611022
Std. Dev	0.872097	3.08490176	0.002007613	0.217980839
40 kA Potential Peak Fault Current				
	<i>Delay (ms)</i>	<i>I_{pk} (kA)</i>	<i>I_{ss} (kA)</i>	<i>V_{pk} (kV)</i>
Min	0.11	12.67940112	12.11628709	19.4267071
Max	2.91	21.29975208	12.12753723	19.88370944
Mean	0.627647	18.03850737	12.11848715	19.68456961
Std. Dev	0.863805	2.857725221	0.00205108	0.15019202
35 kA Potential Peak Fault Current				
	<i>Delay (ms)</i>	<i>I_{pk} (kA)</i>	<i>I_{ss} (kA)</i>	<i>V_{pk} (kV)</i>
Min	0.11	11.98961712	11.46583013	19.23192384
Max	2.91	20.01860398	11.46936123	19.82345403
Mean	0.633529	16.98005813	11.46708665	19.62193546
Std. Dev	0.866385	2.661713801	0.000827656	0.174106144
30 kA Potential Peak Fault Current				
	<i>Delay (ms)</i>	<i>I_{pk} (kA)</i>	<i>I_{ss} (kA)</i>	<i>V_{pk} (kV)</i>
Min	0.11	11.03198386	10.62119487	18.77705713
Max	3.71	18.28893816	10.62265406	19.75330001
Mean	0.757059	15.56149015	10.62169019	19.55611136
Std. Dev	0.982265	2.387529312	0.00033644	0.226260508

The proposed FCL is able to limit the fault current for a variety of fault current levels. Therefore, it is an acceptable device for power system protection. The peak fault current has a greater standard deviation in each of the cases due to the fault inception angle. The steady state current values have a low standard deviation for each case because the DC component of the fault current has had ample time to decay, which is expected. The hybrid FCL is capable of limiting the peak fault current below the desired minimum percentage of 50% reduction. At the worst-case scenario, the maximum peak fault current is 24 kA, which is dependent on the angle of fault inception.

The optimization results in Chapter 5 are compared with the PSCAD results and are concluded to be accurate. Table 16 compares the results between AMPL and the average PSCAD results and displays the error between the two programs. The average values are calculated over a 34 test case scenarios with the detailed results being displayed later in this Chapter.

Table 16 – Comparison of FCL results.

Parameter	AMPL (kA)	Average PSCAD Results	Percent Error
Potential Peak Fault Current (kA)	18.965	20.22	6.2%
Potential Steady State Fault Current (kA)	13.75	13.29	3.34%

The optimization of the ferromagnetic core is designed to achieve an approximate solution to the actual design. Based on the results from both programs, the optimization program for the core design provides an accurate design as the percent error between peak values is 6.2% and between the steady state values is 3.34%. To achieve the exact

same results between the programs, the number of turns can be increased or decreased accordingly since only 80% of the inner area of the core is occupied which allows for small modifications. For this given system and optimized ferromagnetic core design, the optimization results are concluded to be an accurate and sufficient design.

C. Pulse Width Modulation

Including the semiconductor switch in parallel with the mechanical switch and the NdFeB core, allows for the user to control the magnitude of the fault current by the use of Pulse-Width Modulation (PWM). A user can over-design the NdFeB core to limit the prospective fault current to two times the rated current and by the use of PWM; any current magnitude from full limitation to minimum limitation (no FCL) can be controlled by PWM. Only small modifications to the controller presented in Chapter 6 are necessary to implement PWM to the system. The PWM technique used is the comparison of the sinusoidal current with a reference sinusoidal current of a specific magnitude. Figure 84 shows the reference sinusoid wave and the minimum and maximum values of fault current along with the desired reference value. The sampler in Figure 84 is sampling at 10 kHz.

Figure 84 – Reference sinusoidal wave for PWM technique.

The change in the controller algorithm to implement PWM only changes at the final stage, as the system still operates as previously described but instead of the semiconductors turning OFF to divert the fault current to the NdFeB core; they are allowed to turn back ON and OFF to achieve the desired magnitude of fault current. The updated controller takes the output of Figure 84 and adds an XOR gate for the semiconductor gate logic. Figure 85 displays the updated controller algorithm in its final stage.

Figure 85 – Updated controller algorithm to include PWM.

Assuming the worst-case scenario of prospective fault current of 50 kA peak and 25 kA steady state as shown in Figure 86, PWM is applied for three different reference values to prove the applicability of the method. Figure 86 represents the case when the semiconductors are gated ON the entire fault current with the NdFeB core not providing any fault current limitation or when the FCL is not in the system. This is the worst-case scenario and the maximum value of potential fault current.

Figure 86 – Worst-case prospective fault current.

The maximum possible limitation scenario is when the semiconductors are gated OFF for the entire duration of the fault current. Figure 87 shows the maximum possible limitation for the designed core previously described. The peak-limited current is 25 kA with a 12.5 kA steady state value. The controllable fault current can be between the range of 50-25 kA peak and 50-12.5 kA steady-state. Half of the source voltage is placed upon the FCL while the other half is handled by the source.

Figure 87 – Maximum limitation scenario for PWM.

The MOV clamps down on the voltage transients and suppresses them to a manageable level of 20 kV. The first scenario observed is when the reference value is equal to 15 kA. The fault current and voltage are shown in Figure 88.

Figure 88 – 15 kA controlled fault current scenario.

The blue line in the top graph of Figure 88 is the controlled fault current while the green line is the mechanical switch current and the red line is current through the NdFeB core. The bottom graph of Figure 88 displays the source voltage (green) and the voltage across the FCL (red). Once the fault ends there is a few cycle recovery time due to the DC component in the NdFeB core. The majority of the fault current is passing through the NdFeB and a small amount is flowing through the IGBTs. The voltage across the FCL changes at each time the semiconductors switch ON and OFF. However, the voltage transients are still limited to 20 kV and the dv/dt is held below the maximum value for the IGBTs due to the MOV. Figure 89 shows a zoomed in version of Figure 88.

Figure 89 – Zoomed in version of Figure 88.

The fault current is primarily sinusoidal with only a small amount of harmonics injected into the system. Due to the high limitation requirement, the majority of the current is flowing through the NdFeB core with small amount flowing through the semiconductor switch as shown in Figure 90.

Figure 90 – Semiconductor switch current for the 15 kA scenario.

The semiconductor current reaches 15 kA before being turned OFF and transferring the current the NdFeB core. The PWM gate signal for the semiconductors is given in Figure 91. The semiconductors are being switched ON and OFF to control the magnitude

of the fault current as designed. The gate signal is shown to be OFF for longer periods of time during the initial peak of the fault current because the NdFeB core can only limit the peak fault current to 25 kA instead of the desired 15 kA. Once the DC component diminishes, the semiconductor switch is gated ON for a longer period of time before being gated OFF. The duty ratio of the semiconductors is greater once the DC component diminishes than it is before it diminishes.

Figure 91 – PWM signal for the 15 kA scenario.

By switching ON and OFF the semiconductor switch results in harmonics in the system. However, the Total Harmonic Distortion (THD) is well within practical limits.

Figure 92 shows the THD for the 15 kA scenario.

Figure 92 – Total harmonic distortion for the 15 kA scenario.

The THD reaches 2% but quickly falls to 0.2% during the majority of the fault before it jumps back up to 1.25% when the fault ends. The next scenario is with the desired fault current magnitude of 22.5 kA. The controlled fault current is shown in Figure 93.

Figure 93 – 22.5 kA controlled fault current scenario.

The fault current magnitude is controlled to 22.5 kA and the NdFeB core is needed less than it is in the 15 kA scenario because the constraints have been relaxed and it is not needed as much as it was in the 15 kA scenario. A higher percentage of fault current is flowing through the semiconductor switch, which implies a greater duty cycle for the semiconductor switch. The voltage transients are more frequent because of the increased switching in the semiconductors. However, the voltage transients are suppressed to 20 kV due to the MOV.

Figure 94 – Zoomed in version of Figure 93.

The current in the semiconductor switch is greater in the 22.5 kA scenario as when compared to the 15 kA scenario. The semiconductor current is shown in Figure 95.

Figure 95 – Semiconductor current for the 22.5 kA scenario.

The PWM signal for the semiconductor switch is shown in Figure 96 for the 22.5 kA scenario.

Figure 96 – PWM signal for the 22.5 kA scenario.

The duty cycle is greater for the 22.5 kA scenario than in the 15 kA scenario. The semiconductor switch is turned ON for a longer period of time and the NdFeB core is inserted in the system less frequently. The THD for the 22.5 kA scenario is given in Figure 97.

Figure 97 – Total harmonic distortion for the 22.5 kA scenario.

The THD peaks at 2.1% and settles down to 0.2% during the fault duration. Once the fault ends, another spike occurs from the switching of the components but is still within acceptable values. The final scenario tested is the 30 kA scenario. The controlled current for the 30 kA scenario is given in Figure 98.

Figure 98 – Current and voltage for the 30 kA scenario.

The controlled current is determined to be approximately 30 kA with the current through the NdFeB core being less than the previous two scenarios. A majority of the fault current is sent through the semiconductor switch as the constraints on the current are relaxed even more. The PWM signal sent to the semiconductor switch is shown below in Figure 99.

Figure 99 – PWM signal for the 30 kA scenario.

The PWM signal in the 30 kA scenario has a higher duty ratio than either of the other scenarios because more current is allowed to pass through the semiconductors to

control the current to 30 kA. Figure 100 and Figure 101 show the semiconductor current and THD for the 30kA scenario.

Figure 100 – Semiconductor current for the 30 kA scenario.

Figure 101 – Total harmonic distortion for the 30 kA scenario.

In conclusion, PWM can control the fault current magnitude to a desired value. By controlling the fault current, the NdFeB core can be overdesigned which will extend the life the hybrid FCL as well as allow existing protection systems from needing to change settings. Using PWM in the proposed hybrid FCL injects small harmonics but the injected harmonics are well within acceptable limits.

D. Low Voltage Model

A low voltage simulation model is built to confirm the correct modeling of the NdFeB core in PSCAD and is compared to the experimental results for proof of concept purposes. A fault occurs at $t = 0.3$ seconds and lasts for 0.5 seconds. The parameters used

in the low voltage simulations are given in Table 17. The low voltage core design is given from the optimization program described in Chapter 5 with updated system parameters.

Table 17 – Low voltage simulation parameters

Line to Neutral Voltage	V_{LN}	20 V
Nominal Current	I_n	1.25 A
Potential Peak Fault Current	I_{sc}	10 A
Line Frequency	f	60 Hz
Maximum Fault Duration	t_{FCL}	1 sec
Asymmetry Factor	$\frac{X}{R}$	20
Percent Reduction	PR	45-55%
Number of Turns	N	461
Cross-sectional Area of Core	$A_{core} (m^2)$	0.00016
Mean Path Length	$l_{mean} (m)$	0.2
Remanence Flux Density	$B_{rem} (T)$	1.48
Saturation Flux Density	$B_{sat} (T)$	1.6
Coercivity	$H_c (kA/m)$	891.3

The low voltage simulation results are shown in Figure 102. The prospective fault current is 10A and the FCL is designed to limit the fault current to approximately 50%. The limited fault current with the low voltage FCL in the system is given below.

Figure 102 – Low voltage simulation results.

The low voltage FCL limits the fault current to 4.75A, which is approximately a 50% reduction. The load and the fault impedance are both resistive to model the experimental test setup in the next section.

II. Experimental Results

A. Set-Up

An experimental test system is built to verify the correct modeling of the hybrid FCL in PSCAD and AMPL. The system is tested at Arizona State University's power electronics lab. The main objectives of the low voltage model are to test the current limiting capabilities of the designed FCL and to verify the correct operation and modeling of the FCL in PSCAD. The oscilloscope used is the LeCroy waveRunner 104MXi and has a sampling speed of 10 Gigasamples/sec and a 4 channel input. The sampling speed of the oscilloscope is set to 100,000 samples/sec. The controller used is the TI C2000 Launchpad model number F28027 and is set to take samples at 5 kHz. The controller is also tested to verify correct order of operation and to determine the average operation time of the FCL. The designed NdFeB core for the experiment is shown in Figure 103 and has the parameters given in Table 17.

Figure 103 – Assembled NdFeB core with casing and windings.

The NdFeB core's casing was built at the machine shop at Arizona State University and Jorge Mendoza (undergraduate researcher) put the NdFeB core together including the windings around the core. The purpose of the the case is to hold the individual NdFeB magnets in place and prevent them moving around and possibly breaking when subjected to a current. The NdFeB core is designed to resemble a transformer as it has removable connections as well as a removable leg of the core to wind all of the windings around and then slide into the core shape without having to take apart the entire design. Each layer of windings has insulating tape to insulate the windings from one another and prevent short circuit in case of a melted wire. Each of the individual cores in the casing is aligned in the same flux direction to guarantee conformity. The entire test system is shown in Figure 104.

Figure 104 – Hardware test system.

The gate driver is the VLA536-01R gate driver by Powerex and is made for a half bridge topology. The protection circuitry in the gate driver is shorted as advised by an application engineer from Powerex for this particular application. Only one gate driver out of the two on the board is needed for this application. The control circuitry is isolated from the main test system by opto-couplers in the gate IGBT gate driver, the reed relay isolation transformer and the current transformers. The controller is connected and powered by a PC using the Code Composer Studio Program V5 by Texas Instruments. The controller code is written in C and can be found in Appendix B. The IGBTs are developed by Fuji Electric model number 2MB175F-060 and they have a maximum voltage of 600V and a maximum current rating of 75A which is well above the test system param-

ters. Two IGBTs are needed for an AC switch however since they are connected back to back or emitter to emitter, only one gate signal is needed to turn ON and OFF both of the IGBTs.

Two DC power supplies are used to provide power to the Gate driver and the Op-amps used to step up the gate signal from the controller to a value the mechanical switch can handle. Each CT has a 1 ohm resistor across its terminal with a ratio of 100:5 and 3 turns inside the CT. Therefore, each value measured in the oscilloscope must be multiplied by 20 and divided by 3 to observe the actual current flowing in the system. The CT output is also connected to the input of the controller where the control algorithm determines if a fault has occurred and switches the components in the proper order. The output of the controller is sent to the mechanical contact switch and the IGBT gate driver. The mechanical contact switch needs 16V to operate but the controller only outputs 3.3V so a voltage follower op-amp circuit is created to step-up the voltage to 18 V for correct operation. The IGBT gate driver is active low so when the controller gate signal is 0V the IGBTs are gated ON. Therefore the logic is inverted in the controller to send a 3.3V signal to turn OFF the IGBTs and to send a 0V signal to turn ON the IGBTs.

B. Results

The experimental parameters are the same as the simulation parameters given in Table 17. To verify correct operation for any fault inception angle, the peak positive and negative scenarios will be presented as well as a zero crossing. The first hardware scenario is the zero crossing current scenario and the results are presented in Figure 105. The red graph is the sum of the current in all 3 parallel branches, the yellow graph is the cur-

rent through the mechanical contact switch, the blue graph is the current through the semiconductor switch, and the green graph is the current through the NdFeB core.

Figure 105 – FCL operation for a current zero crossing fault inception angle.

The nominal current is approximately 1.25A with a prospective fault current of 10A. The proposed FCL is able to limit the fault current to 4.5A and is able to operate within the 4 ms operation time. The controller transitions the FCL from normal operation mode to fault limitation mode in approximately 1.75 ms. There are no false trips during the fault and there is no bouncing of the mechanical switch or reestablishment of the current through the mechanical switch either. As the mechanical switch opens the current is transferred to the semiconductor switch. Zero current flows in the semiconductor switch until the mechanical switch is almost fully opened because of the semiconductors' impedances are greater than the mechanical switch's impedance. The semiconductors incur a 2.5V voltage across when gated ON. The FCL produces a sinusoidal current and is within 200 mA of the simulated value, which amounts to a 5% difference from the

PSCAD simulations. The second scenario observed is the positive peak scenario and is shown in Figure 106.

Figure 106 – FCL operation for a positive peak current fault inception angle.

The current in the positive peak is approximately 4.5A and operates in approximately 1.5 ms. Since the current is already closer to a maximum limit of the controller, the controller can detect the fault faster due to less time steps until a constraint is violated. Again, there is no improper switching and the current flows through the NdFeB core once the FCL has transitioned from normal operating mode to fault limitation mode. Again the semiconductor current begins to rise as the mechanical switch is opened and the current is transferred to semiconductors. Once the mechanical switch is closed, the semiconductors are turned OFF and the fault is diverted to the NdFeB core, which limits the fault current. The third and final scenario presented is the negative peak fault current and is shown in Figure 107.

Figure 107 – FCL operation for a negative peak current fault inception angle.

The peak fault current is limited to 4.5A and the system operates within 2 ms. The semiconductors begin to conduct current as the mechanical switch is opening. Then the current is transferred to the NdFeB core. Figure 108 depicts the transition from fault limitation mode to normal operation mode once a fault has ended. The controller has a delay implemented in it for approximately 2.5 cycles, which prevents inaccurate measurements, or conversion errors made by the controller. The controller must stay in the faulted state for a predetermined amount of time steps before returning to normal operation mode. This delay is arbitrary and can be selected on a case by case basis.

Figure 108 – FCL transition from fault limitation mode to normal operation mode.

The current is again limited to approximately 4.5A and once the fault ends the controller keeps the FCL in fault limitation mode until the desired time delay has been exceed in which the controller closes the mechanical contact switch and the system returns to normal operation. The current magnitude during the delay period is approximately 1A before it returns to 1.25A as normal. The green (NdFeB) and red (all) lines are in sync during the fault and during the delay transition period. However once the delay is exceeded, the yellow (mechanical) and red (all) lines are in sync with the green (NdFeB) line returning to zero. The blue (semiconductor) line is zero during the entire transition.

The experiment is performed 30 times with random fault inception angles. The results of this study are to determine the repeatability of the proposed FCL and determine the variability in fault current limitation based of different fault inception angles. Also, the controller operation is recorded to determine the average operation time and the standard deviation. The results of the study are presented in Table 18.

The average maximum current magnitude over the 30 tests is 4.506 A. The maximum and minimum values for the current magnitude are 4.74 A and 4.24 A. The standard deviation of the current magnitude is 0.158 A. In comparison with the PSCAD low voltage simulations, the error is approximately 5% for the average current magnitude. The average operation time for the controller is 1.761 ms which is well below the 4 ms goal. The minimum and maximum operation times are 1.5 ms and 2.12 ms respectively. The standard deviation is 0.177ms and the controller is concluded to operate as designed with no false trips and quick detection of a fault.

Table 18 – Statistical analysis of hybrid FCL hardware

	Maximum Magnitude (V)	Maximum Magnitude (A)	Operation Times (ms)
1	0.666	4.44	1.75
2	0.634	4.23	1.5
3	0.638	4.25	1.63
4	0.635	4.23	1.89
5	0.638	4.25	2.12
6	0.648	4.32	2.04
7	0.675	4.50	1.53
8	0.701	4.67	1.71
9	0.687	4.58	1.81
10	0.696	4.64	1.9
11	0.711	4.74	1.63
12	0.705	4.70	1.68
13	0.687	4.58	1.52
14	0.692	4.61	1.56
15	0.657	4.38	1.82
16	0.661	4.41	1.66
17	0.672	4.48	2.07
18	0.681	4.54	1.97
19	0.693	4.62	1.64
20	0.684	4.56	1.73
21	0.699	4.66	1.79
22	0.704	4.69	1.58
23	0.709	4.73	1.76
24	0.688	4.59	1.58
25	0.695	4.63	1.94
26	0.654	4.36	1.99
27	0.66	4.40	2.01
28	0.647	4.31	1.63
29	0.681	4.54	1.72
30	0.679	4.53	1.67
AVERAGE	0.6759	4.506	1.761
STD DEV	0.02371432	0.158095466	0.17782886
MIN	0.634	4.226666667	1.5
MAX	0.711	4.74	2.12

III. Conclusions

In conclusion, the proposed FCL is tested in PSCAD for its current limiting capabilities, the correct operation of the controller, and the correct hysteresis modeling of the NdFeB core. The proposed hybrid FCL is capable of limiting the prospective fault current to within the design parameters given in Table 8. A 62.5% reduction in peak fault current is achieved while a 45.4% steady-state fault current is achieved by the core parameters given in Table 16 for that particular scenario.

NdFeB provides a one-sixth size reduction for the same current limiting capabilities as compared with iron. In addition, the hysteresis of the NdFeB core is modeled correctly by the Jiles-Atherton method and the core provides the nonlinear inductance by its change in permeability. The entire transition between normal operation mode and fault limitation mode occurs within 1.5 ms, which will limit the first initial peak of the fault current. The fast mechanical contact switch does not need to interrupt the current but only transfer it to the semiconductor switch where the semiconductors then transfer the current to the NdFeB core thus eliminating any arc from occurring. An MOV is placed across the entire hybrid FCL to limit switching transients and clamp down on the voltage. The experiments prove the concept of the hybrid FCL and its correct operation. The designed system operates as expected and the controller can transition the system from normal operation mode to fault limitation mode within 2 ms. The modeling of the NdFeB core is determined to have been accurate and entire system operates as designed because the hardware and simulation results are within good agreement. PWM has been implemented into the simulations to prove the ability to control the magnitude of the fault current if a current limiting element is over designed. The PWM allows an operator to specify what

current level is desired for their existing protection system. The hybrid FCL injects very little harmonics during PWM and is determined to not affect current protection systems. The proposed FCL is shown to be a feasible solution to fault current limitation and the only solution, which allows a user to determine the fault current magnitude for their particular system. The hardware results and the simulations prove the feasibility of the design and its applicability in power systems.

CONCLUSIONS AND FUTURE WORK

I. Conclusions

In conclusion, a new hybrid fault current limiter is proposed for a 15 kV distribution system that utilizes a fast mechanical contact switch in parallel with a semiconductor switch, a MOV, and an NdFeB core. NdFeB is chosen over iron core and AlNiCo because of its fault current limiting capabilities such as reduced core size, higher energy handling capability, and lighter weight. NdFeB is chosen over SmCo due to cost but either material would work. The ferromagnetic properties of NdFeB are modeled by the Jiles-Atherton method of hysteresis. The hysteretic parameters match the manufacturer's data and are concluded to be modeled correctly. Finite Element Analysis is performed on the copper coils in the windings to determine the minimum gauge of wire needed to structurally handle the fault current placed upon it.

The normal operation of the FCL allows the current to flow through the fast mechanical contact switch but once the controller detects a fault has occurred the operation is as such:

- Turn ON the semiconductor switch to provide an alternative path for the current to flow.
- Open the fast mechanical contact switch and transfer the current to the semiconductor switch. An arc should not occur across the mechanical contact switch since the current has an alternative path.
- Turn OFF the semiconductor switch to transfer the current to the NdFeB core for limitation and continue in this state until the fault has ended.

- Implementation of PWM in the system allows the user to control the magnitude of the fault current in their system which would minimize protection setting changes.
- Once fault has ended, close the mechanical contact switch and begin normal operation again.

The entire switching operation is designed to occur before the first peak of the fault current or 4 ms and the operation time in the simulations and hardware is within 2 ms. The core dimensions are designed to limit a prospective fault current of 50 kA by 45-55% and the simulation results show a peak limitation of 62.5% with a steady-state limitation of 45.4% which is within the design parameters for one scenario. Statistical analysis is performed on the limiting capability of the FCL to determine the average limited fault current as well as the maximum, minimum, and standard deviation. The simulations show the feasibility of the proposed hybrid FCL and its application to the power system today.

A Mixed Integer Programming (MIP) optimization method has been developed to determine a physical design for a ferromagnetic core used in fault current limiter applications. The optimization program optimizes the core dimensions for the lowest cost while meeting the specific user's requirements such as the amount of fault current reduction desired. The optimization method is developed as a general method where a user can input their specific system requirements and run the optimization program to obtain the optimized core design for their given system inputs. A low voltage hardware model has been developed and tested with the results verifying the simulation results. PWM has been implemented in the simulations, which shows the feasibility of controlling the fault

current magnitude to a desired level. By controlling the fault current magnitude, the NdFeB core can be overdesigned to extend the life of the device. Using PWM injects a small amount of harmonics but does not violate any harmonic limits and the existing protection settings should still be used without any changes. The harmonics are not necessarily important since the proposed FCL is designed to operation for only 1 second. The experimental test system is within good agreement of the PSCAD simulations with only a 5% error in most test cases. The controller is able to operate on average 1.75 ms which is well below the desired value of 4 ms. The controller does not experience any false trips during a fault and will stay in the faulted state for a predetermined amount of cycles after the fault has ended.

II. Contributions

The following list is contributions made by the author.

- 1) Presented a new topology for fault current limitation that limits the prospective fault current by approximately 45-55%. The proposed FCL has no distinct disadvantages but combines the advantages of numerous FCL topologies into one device.
- 2) Performed a comparison of 4 different ferromagnetic materials to determine which material is the most suitable for FCL applications. Neodymium (NdFeB) is selected as the core material of choice by cost, size, and limiting capabilities.
- 3) Developed a casing and core design used in the hybrid FCL that is similar to a transformer with the help of Jorge Mendoza as my undergraduate researcher.
- 4) Performed Finite Element Analysis (FEA) on the copper coils to determine the minimum size of wire gauge needed for this specific application of the FCL. This

work was performed by Jorge Mendoza while I supervised and gave him guidance.

- 5) Developed a novel control algorithm to perform the desired switching operations of the proposed hybrid FCL.
- 6) Developed the proposed FCL model in PSCAD and simulated the operation of the device which confirms the feasibility of the proposed FCL.
- 7) Modeled the hysteresis of the NdFeB core accurately using the Jiles-Atherton method and implemented it in PSCAD using exponential functions.
- 8) Developed an optimization method to design a ferromagnetic core for use in fault current limiter applications. This method is a general method where a user inputs system information, magnetic material information, and a wire gauge table and the optimized core results in an acceptable design with minor modifications.
- 9) Developed and implemented PWM to control the fault current magnitude to a user's desired level in the simulations.
- 10) Built and tested a low voltage hardware model which proves the correct operation of the proposed FCL. The controller algorithm is able to detect and transition the FCL from normal operation mode to fault limitation mode in less than 1.75 ms. The hybrid FCL is determined to be modeled correctly in the simulations as the hardware and simulations are within good agreement.

III. Future Work

For future work, tap settings could be implemented in the core design to change the level of fault current limitation. In addition, PWM could be implemented in the hard-

ware system to determine the practical feasibility of controlling the fault current magnitude.

Experimentally building and testing a medium voltage FCL should be performed to determine any design discrepancies between the low voltage model and a higher voltage model. A full-scale model should be built and tested to verify the design as well.

IV. Relevant Publications

While At Arizona State University:

A. Authored:

- [1] J. Prigmore, G. Karady, "An ETO-Based AC Buck-Type Fault Current Limiter for Use in the FREEDM Project," in *Applied Power Electronics Conference and Exposition, 2012. APEC '12. Twenty-Seventh Annual IEEE*, 2012, p. 6 pp. 1042-1047.
- [2] J. Prigmore, G. Karady, "A Novel 7.2 kV Fault Current Limiter for Use in the FREEDM Project," *In Proc 2012 IEEE Transmission and Distribution*, 7-10 May 2012.
- [3] J. Prigmore, J. Mendoza, G. Karady, "A Neodymium Permanent Magnet Fault Current Limiter For Use in the FREEDM Project," *In Proc 2012 IEEE PES Integrated Smart Grid Technologies Europe (ISGT-EU)*, 8-11 October 2012.
- [4] J. Prigmore, J. Mendoza, G. Karady, "Comparison of Four Different Ferromagnetic Materials for Fault Current Limiter Applications," *IEEE Transactions on Power Delivery*, Accepted: February 21st, 2012.

B. Co-Authored

- [5] T. Werho, P. DeGuzman, A. Singh, J. Prigmore, and G. Karady, "Autonomous switch fault current limiter," in *IEEE North American Power Symposium (NAPS)*, 2011, 2011, pp. 1-5.

C. Submitted

- [6] J. Prigmore, G. Karady, "Optimization of a Ferromagnetic Core Using Mixed Integer Programming for Fault Current Limiter Applications," *IEEE Transactions on Power Delivery*. Submitted February 22nd, 2013.
- [7] J. Prigmore, J. Mendoza, G. Karady, "A Neodymium Hybrid Fault Current Limiter." *IEEE Transactions on Power Delivery*. Submitted March 20th, 2013.

Before Arizona State University and Unrelated Publications:

- [8] J. Prigmore, G. Tcheslavski, and C. Bahrim, "An IGCT-based Electronic Circuit Breaker design for a 12.47kv distribution system," in *Power and Energy Society General Meeting, 2010 IEEE, 2010*, pp. 1-5.
- [9] J. Han, J. Prigmore, S. Solanki, Z. Wang, "Modeling and Coordinate Controller Design in a Microgrid System in RTDS," in *Power and Energy Society General Meeting, 2013 IEEE, 2013, 2013*, Vancouver, Canada, pp. 1-8.
- [10] J. Han, J. Prigmore, Z. Wang, S. Solanki, "Coordinate Controller Design of a Hardware in the Loop Microgrid System with RTDS," *IEEE Transactions on Smart Grid*, Submitted March 15th, 2013.

REFERENCES

- [1] M. Marchionini, B. Fall, N. Steurer, "An Assessment of Fault Current Limiter Testing Requirements," 2009.
- [2] M. Steurer, "Standards Developments for Fault Current Limiters," in *EPRI SC Conference*, 2011.
- [3] L. Kovalsky, X. Yuan, K. Tekletsadik, A. Keri, J. Bock, and F. Breuer, "Applications of superconducting fault current limiters in electric power transmission systems," *Applied Superconductivity, IEEE Transactions on*, vol. 15, no. 2, pp. 2130–2133, 2005.
- [4] H. Schmitt, "Fault current limiters report on the activities of CIGRE WG A3.16," in *Power Engineering Society General Meeting, 2006. IEEE*, 2006, p. 5 pp.
- [5] J. Jager, "Interaction between fault current limiters and protection - A glance at the final report of CIGRE WG-A3.16," in *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE*, 2008, pp. 1–3.
- [6] P. R. Deo and T. P. Shah, "Innovative electromagnetic dynamic fault current limiter operating at ambient temperature for smart grids," in *Innovative Smart Grid Technologies (ISGT), 2010*, 2010, pp. 1–6.
- [7] M. Noe, M. Steurer, S. Eckroad, and R. Adapa, "Progress on the R&D of fault current limiters for utility applications," in *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE*, 2008, pp. 1–4.
- [8] O. Vodyakho, C. Widener, M. Steurer, D. Neumayr, C. Edrington, S. Bhattacharya, and H. Mirzaee, "Development of solid-state fault isolation devices for future power electronics-based distribution systems," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, 2011, pp. 113–118.
- [9] O. Vodyakho, M. Steurer, D. Neumayr, C. S. Edrington, G. Karady, and S. Bhattacharya, "Solid-state fault isolation devices: application to future power electronics-based distribution systems," *Electric Power Applications, IET*, vol. 5, no. 6, pp. 521–528, 2011.
- [10] M. M. R. Ahmed, G. A. Putrus, L. Ran, and L. Xiao, "Harmonic analysis and improvement of a new solid-state fault current limiter," *Industry Applications, IEEE Transactions on*, vol. 40, no. 4, pp. 1012–1019, 2004.

- [11] D. Cvoric, S. W. H. de Haan, and J. A. Ferreira, "Comparison of the four configurations of the inductive Fault Current Limiter," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 3967–3973.
- [12] D. Cvoric, S. W. H. de Haan, and J. A. Ferreira, "Guidelines for 2D/3D FE transient modeling of inductive saturable-core Fault Current Limiters," in *Electric Power and Energy Conversion Systems, 2009. EPECS '09. International Conference on*, 2009, pp. 1–6.
- [13] D. Cvoric, S. W. H. de Haan, and J. A. Ferreira, "New saturable-core Fault Current Limiter topology with reduced core size," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, 2009, pp. 920–926.
- [14] D. Cvoric, S. W. H. de Haan, J. A. Ferreira, M. van Riet, and J. Bozelie, "Design and testing of full-scale 10 kV prototype of inductive fault current limiter with a common core and trifilar windings," in *Electrical Machines and Systems (ICEMS), 2010 International Conference on*, 2010, pp. 1879–1884.
- [15] P. Papadopoulos, A. E. Umenei, I. Grau, R. Williams, L. Cipcigan, and Y. Melikhov, "Effectiveness of a new inductive fault current limiter model in MV networks," in *Universities Power Engineering Conference (UPEC), 2010 45th International*, 2010, pp. 1–5.
- [16] F. Moriconi, F. De La Rosa, A. Singh, B. Chen, M. Levitskaya, and A. Nelson, "An innovative compact saturable-core HTS Fault Current Limiter - development, testing and application to transmission class networks," in *Power and Energy Society General Meeting, 2010 IEEE*, 2010, pp. 1–8.
- [17] F. Moriconi, F. De La Rosa, F. Darmann, A. Nelson, and L. Masur, "Development and Deployment of Saturated-Core Fault Current Limiters in Distribution and Transmission Substations," *Applied Superconductivity, IEEE Transactions on*, vol. 21, no. 3, pp. 1288–1293, 2011.
- [18] S. C. Mukhopadhyay, F. P. Dawson, M. Iwahara, and S. Yamada, "Analysis, design and experimental results for a passive current limiting device," *Electric Power Applications, IEE Proceedings -*, vol. 146, no. 3, pp. 309–316, 1999.
- [19] Z. Liang, L. Qing-min, L. Hong-shun, and W. H. Siew, "Study on the feasibility of developing high voltage and large capacity permanent-magnet-biased fault current limiter," in *Universities Power Engineering Conference (UPEC), 2009 Proceedings of the 44th International*, 2009, pp. 1–5.
- [20] L. Hongshun, L. Qingmin, Z. Liang, M. Yuan, and S. Wah Hoon, "An equivalent magnetic circuit coupled model of PMFCL for transient simulation," in *Universities Power Engineering Conference (UPEC), 2009 Proceedings of the 44th International*, 2009, pp. 1–5.

- [21] J. Na, Y. Kim, J. Jang, Y. Hwang, S. Choi, K. Ryu, and T. Ko, "Design and Tests of Prototype Hybrid Superconducting Fault Current Limiter with Fast Switch," *Applied Superconductivity, IEEE Transactions on*, vol. PP, no. 99, p. 1, 2011.
- [22] J. M. Francis, M. Dupraz, J.P. Besrest, R. Armata, "New topology of hybrid circuit breaker / current limiter for MV AES networks," *AES 2005*, 2005.
- [23] J. Mahseredjian, P. J. Lagace, S. Lefebvre, and A. Chartrand, "Superposition technique for MOV-protected series capacitors in short-circuit calculations," *Power Delivery, IEEE Transactions on*, vol. 10, no. 3, pp. 1394–1400, 1995.
- [24] D. Cvoric, S. W. H. de Haan, and B. Ferreira, "CB stress reduction and comparison of energy dissipation for two types of FCLs," in *Transmission and Distribution Conference and Exposition, 2008. T&D IEEE/PES*, 2008, pp. 1–7.
- [25] H. Arab and F. Faghihi, "Implementation of Preisach-type model for studying of B-H curve influence on the behavior of flux-coupling type SFCL," in *Electrical Power & Energy Conference (EPEC), 2009 IEEE*, 2009, pp. 1–6.
- [26] S. Y. R. Hui and J. Zhu, "Magnetic hysteresis modeling and simulation using the Preisach theory and TLM technique," in *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, 1994, pp. 837–842 vol.2.
- [27] H. Skarrie, "Design of Powder Core Inductors," Lund University, 2001.
- [28] P. GmbH., "PLECS User Manual," Zurich, Switzerland, 2012.
- [29] D. Jiles and D. Atherton, "Ferromagnetic hysteresis," *Magnetics, IEEE Transactions on*, vol. 19, no. 5, pp. 2183–2185, 1983.
- [30] W. Chen, *The Electrical Engineering Handbook*. New York: Else-vier Academic Press, 2005, p. pp. 169.
- [31] M. S. Inc., "Physical Properties of Alnico Magnets," 2012. [Online]. Available: <http://www.magnetsales.com/Alnico/Alprops.htm#magnetic>.
- [32] M. S. Inc., "Table of Properties for SmCo Magnets," 2012. [Online]. Available: www.magnetsales.com/SMCO/smcoprops.htm.
- [33] M. S. Inc., "Table of Properties of NdFeB Magnets," 2012. [Online]. Available: www.magnetsales.com/Neo/Neoprops.htm.
- [34] A. Steel, "Selection Of Electrical Steels for Magnetic Cores," West Chester, OH, 2007.
- [35] S. Laboratories, "SEL-551/SEL-551C Overcurrent and Reclosing Relay," 2007.

- [36] ABB Inc, “UFES- Ultra Fast Earthing Switch,” 2011.
- [37] Mitsubishi Electric, “HVIGBT Modules,” 2011.
- [38] Cooper Power Systems, “Surge Arresters,” 2011.
- [39] M. Waters, *The Short-Circuit Strength of Power Transformers*. England: Macdonald, 1966.
- [40] A. C. de Azevedo, I. Rezende, A. C. Delaiba, J. C. de Oliveira, B. C. Carvalho, and H. S. de Bronzeado, “Investigation of Transformer Electromagnetic Forces Caused by External Faults Using FEM,” in *Transmission & Distribution Conference and Exposition: Latin America, 2006. TDC '06. IEEE/PES*, 2006, pp. 1–6.
- [41] J. C. Olivares-Galva, F. de Leo, P. S. Georgilakis, and R. Escarela-Prez, “Selection of copper against aluminium windings for distribution transformers,” *Electric Power Applications, IET*, vol. 4, no. 6, pp. 474–485, 2010.

APPENDIX A
PLECS SIMULATIONS


```

// Specify Time delay for switching of both semiconductors and mechanical switch
#define BrDELAY ParamRealData(0, 0)
#define SDELAY ParamRealData(1, 0)

// Specify Variables needed for correct operation
double turn_on_time;
int n;
int flag;
double Checkvalue; //Outputs any value needed to be checked for confirmation of correct
operation
double didt;
double Old_Iload;
double Old_Time;
double Time_Delay; // Prevents multiple switching from occurring once fault triggered
first time

```

The following code is written in the “Start function code” section of the custom C block in PLECS.

```

if (NumParameters != 2)
{
    SetErrorMessage("Two Parameters Required (BrDELAY, SDELAY).");
    return;
}
if (ParamNumDims(0) != 2 || ParamDim(0,0)!=1 || ParamDim(0,1)!=1 || BrDELAY <=0)
{
    SetErrorMessage("Mechanical Switch Delay time must be a positive scalar.");
}
if (ParamNumDims(1) != 2 || ParamDim(1,0)!=1 || ParamDim(1,1)!=1 || SDELAY <=0)
{
    SetErrorMessage("Semiconductor Delay time must be a positive scalar.");
}

```

The following code is written in the “Update function code” of the custom C block in PLECS

```

// Previous input is the same as the last output
// Fault Conditions more than preset values
didt = abs((Iload-Old_Iload)/(CurrentTime-Old_Time));
if (CurrentTime >= Time_Delay)
{
    if (Iload>M1 || didt>M2)
    {

```

```

if (PREV_INPUTbr==1 && PREV_INPUTmos==0)
// Breaker Closed and Semiconductor OFF
{
    flag = 1;        // Set the case value
    if (n<1)
    {
        turn_on_time = CurrentTime +SDELAY;    //Time Delay for
        SemiConductor
        n++;
    }
}
if (PREV_INPUTbr==1 && PREV_INPUTmos==1)           // Breaker
Closed and semiconductor ON
{
    flag = 2;
    if (n<1)
    {
        turn_on_time = CurrentTime +BrDELAY;    //Time Delay for fast
mechanical switch
        n++;
    }
}
if ((PREV_INPUTbr==0 && PREV_INPUTmos==1) || (PREV_INPUTbr==0
&&PREV_INPUTmos==0))
{
    flag = 3;
    if (PREV_INPUTbr==0 && PREV_INPUTmos==1)
    {
        Time_Delay = CurrentTime+0.0166; // Keep output fixed
for 1 cycle.
    }
}

switch (flag)
{
case 1:        // Turn on Semiconductors when fault occurs
    {
        if (CurrentTime>=turn_on_time)
        {
            DiscState(0)=1;    // Gate for Breaker
            DiscState(1)=1;    // Gate for Semiconductors
            n=0;
        }
        else
        {

```

```

        DiscState(0) = PREV_INPUTbr; // Gate for breaker
        DiscState(1) = PREV_INPUTmos; // Gate for semiconductors
    }
    break;
}
case 2:      // Open breaker when semiconductors are ON
    {
        if (CurrentTime >= turn_on_time)
        {
            DiscState(0)=0;
            DiscState(1)=1;
            n=0;
        }
        else
        {
            DiscState(0) = PREV_INPUTbr;
            DiscState(1) = PREV_INPUTmos;
        }
        break;
    }
case 3:      // Fault is continuous
    {
        DiscState(0) = 0;           // Breaker Open
        DiscState(1) = 0;           // Semiconductors open
        break;
    } // case
} // switch
} // if (condition)
else
{
    DiscState(0) = 1;
    DiscState(1) = 0;
    n=0;
    turn_on_time = 0;
    if (IFcl >= 10)
    {
        DiscState(0) = 0;
        DiscState(1) = 0;
    } // If statement
} // Else Statement
} // First if statement for the Delay period
else
{
    DiscState(0) = 0;
    DiscState(1) = 0;
}

```

```

    }
    Old_Time = CurrentTime;
    Old_Iload = abs(Iload);

```

The following code is written in the “Output function code” in the custom C block in PLECS.

```

if (IsMajorStep)
{
    Output(0) = DiscState(0);
    Output(1) = DiscState(1);
    PREV_INPUTbr = Output(0);
    PREV_INPUTmos = Output(1);
    Output(2) = abs(didt);
    Checkvalue = abs(Output(2)); // delete once verified for correct operation and re-
duce to 2 outputs
    if (CurrentTime<0.2)
    {
        Output(0) = 1;
        Output(1) = 0;
        PREV_INPUTbr = Output(0);
        PREV_INPUTmos = Output(1);
    }
}

```

APPENDIX B

MICROCONTROLLER CODE

```

//#####
//
// File: FCL_Controller.c
//
// Title: Hybrid FCL Controller Code.
//
// Group: C2000
// Target Device: TMS320F2802x
//
//! \addtogroup example_list
//! <h1>ADC Start-Of-Conversion (SOC)</h1>
//!
//! Interrupts are enabled and the ePWM1 is setup to generate a periodic
//! ADC SOC - ADCINT1. Two channels are converted, ADCINA4 and ADCINA2.
//!
//! Watch Variables:
//!
//! - mechanicalDetection[10] - Last 10 ADCRESULT0 values
//! - semiconductorDetection[10] - Last 10 ADCRESULT1 values
//! - ConversionCount - Current result number 0-9
//! - LoopCount - Idle loop counter
//
// (C) Copyright 2012, Texas Instruments, Inc.
//
// Control Code Written by Jay Prigmore and Jorge Mendoza
// Arizona State University
// 11-12-2012
//#####
// $TI Release: f2802x Support Library v200 $
// $Release Date: Tue Jul 24 10:01:39 CDT 2012 $
//#####

#include "DSP28x_Project.h" // Device Headerfiles and Examples Include File

#include "f2802x_common/include/adc.h"
#include "f2802x_common/include/clk.h"
#include "f2802x_common/include/flash.h"
#include "f2802x_common/include/gpio.h"
#include "f2802x_common/include/pie.h"
#include "f2802x_common/include/pll.h"
#include "f2802x_common/include/wdog.h"
#include <stdio.h>
#include <math.h>

// ##### control limits #####

```

```

// # These values are in mV          #
// # CT ratio of 100:5                #
// # 3 turns of wire in CT           #
// # Normal steady state values are:  #
// # mag = 200 mV for 1.33 A          #
// # der = test                       #
// #####
#define triggerVoltage 400 // 3000 = 3V; 600 or 500 might be a good number (225 nor-
mal current)
#define triggerDer 600 // 600*(sind(0)-sind(4.32))/0.2
#define open 0
#define closed 1

// Prototype statements for functions found within this file.
interrupt void adc_isr(void);
void Adc_Config(void);

// Global variables used in the Controller Code:
uint16_t LoopCount;
uint16_t ConversionCount, prevConversionCount;
uint16_t mechanicalSwitchVoltage[10];
uint16_t semiconductorVoltage[10];
uint16_t lineVoltage[10];
uint16_t clearflag;
uint16_t interCount;
uint16_t mechanicalLatch, semiconductorLatch, lineCurrentMag, lineCurrentDer;
uint16_t faultSeq, mechanicalStatus, semiconductorStatus, lineStatus;

// Handling of the hardware modules and board specific code.
ADC_Handle myAdc;
CLK_Handle myClk;
FLASH_Handle myFlash;
GPIO_Handle myGpio;
PIE_Handle myPie;
PWM_Handle myPwm;

// ##### Main Program #####
// This program is used to set up the board which includes
// memory allocation, enabling the input and outputs,
// configure ADC, Set up PWM, set up timer for switching freq
// #####
void main(void)
{
    CPU_Handle myCpu;

```



```

PLL_Handle myPll;
WDOG_Handle myWDog;

// Initialize all the handles needed for this application
myAdc = ADC_init((void *)ADC_BASE_ADDR, sizeof(ADC_Obj));
myClk = CLK_init((void *)CLK_BASE_ADDR, sizeof(CLK_Obj));
myCpu = CPU_init((void *)NULL, sizeof(CPU_Obj));
myFlash = FLASH_init((void *)FLASH_BASE_ADDR, sizeof(FLASH_Obj));
myGpio = GPIO_init((void *)GPIO_BASE_ADDR, sizeof(GPIO_Obj));
myPie = PIE_init((void *)PIE_BASE_ADDR, sizeof(PIE_Obj));
myPll = PLL_init((void *)PLL_BASE_ADDR, sizeof(PLL_Obj));
myPwm = PWM_init((void *)PWM_ePWM1_BASE_ADDR, sizeof(PWM_Obj));
myWDog = WDOG_init((void *)WDOG_BASE_ADDR, sizeof(WDOG_Obj));

// Perform basic system initialization for PWM timer module
WDOG_disable(myWDog);

CLK_enableAdcClock(myClk);
CLK_enableTbClockSync(myClk);
CLK_enablePwmClock(myClk, PWM_Number_1);

(*Device_cal)();

//Select the internal oscillator 1 as the clock source
CLK_setOscSrc(myClk, CLK_OscSrc_Internal);

// Setup the PLL for x10 /2 which will yield 50Mhz = 10Mhz * 10 / 2
PLL_setup(myPll, PLL_Multiplier_10, PLL_DivideSelect_ClkIn_by_2);

// Disable the PIE and all interrupts
PIE_disable(myPie);
PIE_disableAllInts(myPie);
CPU_disableGlobalInts(myCpu);
CPU_clearIntFlags(myCpu);

// If running from flash copy RAM only functions to RAM
#ifdef FLASH
    memcpy(&RamfuncsRunStart, &RamfuncsLoadStart, (size_t)&RamfuncsLoadSize);
#endif

// Setup a debug vector table and enable the PIE
PIE_setDebugIntVectorTable(myPie);
PIE_enable(myPie);

// Register interrupt handlers in the PIE vector table

```

```

    PIE_registerPieIntHandler(myPie, PIE_GroupNumber_10,
    PIE_SubGroupNumber_1, (intVec_t)&adc_isr);

    // Initialize the ADC module which is used to read the
    // voltage values from the current transformers connected to the switches.
    ADC_enableBandGap(myAdc);
    ADC_enableRefBuffers(myAdc);
    ADC_powerUp(myAdc);
    ADC_enable(myAdc);
    ADC_setVoltRefSrc(myAdc, ADC_VoltageRefSrc_Int);

    // At each triggered interrupt, the ADC is triggered
    // to convert the analog voltage values to digital and
    // store them in the ADC buffer. The following code enables
    // this functionality.

    // Enable ADCINT1 in PIE
    PIE_enableAdcInt(myPie, ADC_IntNumber_1);
    // Enable CPU Interrupt 1
    CPU_enableInt(myCpu, CPU_IntNumber_10);
    // Enable Global interrupt INTM
    CPU_enableGlobalInts(myCpu);
    // Enable Global realtime interrupt DBGM
    CPU_enableDebugInt(myCpu);

    // Initialize all of the global variables used to monitor
    // and flag the critical code sequence.
    LoopCount = 0;
    ConversionCount = 0;
    prevConversionCount = 0;
    mechanicalLatch = 0;
    semiconductorLatch = 0;
    lineCurrentMag = 0;
    lineCurrentDer = 0;
    faultSeq = 0;
    mechanicalStatus = 0;
    semiconductorStatus = 0;
    lineStatus = 0;
    clearflag = 0;
    //int i;
    //for (i=0; i<10; i++)
    //{
    //    lineVoltage[i] = 0;
    //}

```

```

// ##### Configure ADC
#####
// The following code sets the physical input location and trigger sources
#
// for the ADC. These ADC channels are physically connected to the current #
// transformers that are used to read the voltage values which represent #
// the amount current being transferred by each switch. This allows the code #
// to read voltage values from the buffer that corresponds to each ADC channel. #
// Note: Channel ADCINA4 will be double sampled to workaround the ADC 1st sam-
ple#
// issue for rev0 silicon errata
#####
ADC_setIntPulseGenMode(myAdc, ADC_IntPulseGenMode_Prior);
//ADCINT1 trips after AdcResults latch
ADC_enableInt(myAdc, ADC_IntNumber_1); //Enabled
ADCINT1
ADC_setIntMode(myAdc, ADC_IntNumber_1, ADC_IntMode_ClearFlag);
//Disable ADCINT1 Continuous mode
ADC_setIntSrc(myAdc, ADC_IntNumber_1, ADC_IntSrc_EOC2); //setup
EOC2 to trigger ADCINT1 to fire
ADC_setSocChanNumber (myAdc, ADC_SocNumber_0,
ADC_SocChanNumber_A4); //set SOC0 channel select to ADCINA4
ADC_setSocChanNumber (myAdc, ADC_SocNumber_1,
ADC_SocChanNumber_A4); //set SOC1 channel select to ADCINA4
ADC_setSocChanNumber (myAdc, ADC_SocNumber_2,
ADC_SocChanNumber_A2); //set SOC2 channel select to ADCINA2
ADC_setSocChanNumber (myAdc, ADC_SocNumber_3,
ADC_SocChanNumber_A6); //set SOC2 channel select to ADCINA6
ADC_setSocTrigSrc(myAdc, ADC_SocNumber_0,
ADC_SocTrigSrc_EPWM1_ADCSOCA); //set SOC0 start trigger on EPWM1A, due to
round-robin SOC0 converts first then SOC1
ADC_setSocTrigSrc(myAdc, ADC_SocNumber_1,
ADC_SocTrigSrc_EPWM1_ADCSOCA); //set SOC1 start trigger on EPWM1A, due to
round-robin SOC0 converts first then SOC1
ADC_setSocTrigSrc(myAdc, ADC_SocNumber_2,
ADC_SocTrigSrc_EPWM1_ADCSOCA); //set SOC2 start trigger on EPWM1A, due to
round-robin SOC0 converts first then SOC1, then SOC2
ADC_setSocTrigSrc(myAdc, ADC_SocNumber_3,
ADC_SocTrigSrc_EPWM1_ADCSOCA); //set SOC2 start trigger on EPWM1A, due to
round-robin SOC0 converts first then SOC1, then SOC2
ADC_setSocSampleWindow(myAdc, ADC_SocNumber_0,
ADC_SocSampleWindow_7_cycles); //set SOC0 S/H Window to 7 ADC Clock Cycles,
(6 ACQPS plus 1)

```

```

    ADC_setSocSampleWindow(myAdc, ADC_SocNumber_1,
ADC_SocSampleWindow_7_cycles); //set SOC1 S/H Window to 7 ADC Clock Cycles,
(6 ACQPS plus 1)
    ADC_setSocSampleWindow(myAdc, ADC_SocNumber_2,
ADC_SocSampleWindow_7_cycles); //set SOC2 S/H Window to 7 ADC Clock Cycles,
(6 ACQPS plus 1)
    ADC_setSocSampleWindow(myAdc, ADC_SocNumber_3,
ADC_SocSampleWindow_7_cycles); //set SOC2 S/H Window to 7 ADC Clock Cycles,
// (6 ACQPS plus 1)

// Configure GPIO 0-3 as outputs
GPIO_setMode(myGpio, GPIO_Number_0, GPIO_Mode_GeneralPurpose);
GPIO_setMode(myGpio, GPIO_Number_1, GPIO_Mode_GeneralPurpose);
GPIO_setMode(myGpio, GPIO_Number_2, GPIO_Mode_GeneralPurpose);
GPIO_setMode(myGpio, GPIO_Number_3, GPIO_Mode_GeneralPurpose);

GPIO_setDirection(myGpio, GPIO_Number_0, GPIO_Direction_Output);
GPIO_setDirection(myGpio, GPIO_Number_1, GPIO_Direction_Output);
GPIO_setDirection(myGpio, GPIO_Number_2, GPIO_Direction_Output);
GPIO_setDirection(myGpio, GPIO_Number_3, GPIO_Direction_Output);

GPIO_setLow(myGpio, GPIO_Number_0); // Mechanical Switch
GPIO_setHigh(myGpio, GPIO_Number_1); // Semiconductor switch (Original was
set LOW)
GPIO_setLow(myGpio, GPIO_Number_2);
GPIO_setHigh(myGpio, GPIO_Number_3);
// Ground pins are J2(1) and J5(2).

// ##### PWM Set-UP #####
// The following statements set up the PWM module and its timing parameters
// for operation. The period for the PWM timer and the value to compare are
// set. The compare value (CMPA) is used to set the counter-compare module to
// constantly check and generate a signal to the PWM module.
#####

// Enable PWM clock
CLK_enablePwmClock(myClk, PWM_Number_1);

// Setup PWM
PWM_enableSocAPulse(myPwm); // Enable SOC on A group
PWM_setSocAPulseSrc(myPwm, PWM_SocPulseSrc_CounterEqualCmpAIncr);
// Select SOC from from CPMA on upcount
PWM_setSocAPeriod(myPwm, PWM_SocPeriod_FirstEvent);
// Generate pulse on 1st event
PWM_setCmpA(myPwm, 0x0080); // Set compare A value

```

```

PWM_setPeriod(myPwm, 0x00C8);    // Set period for ePWM1 (50 micro seconds)
PWM_setCounterMode(myPwm, PWM_CounterMode_Up);    // count up and start

// The following for-loop is used to keep the CPU in a busy waiting mode until
// an interrupt is received.

// Wait for ADC interrupt
for(;;)
{
    LoopCount++;
}

}
// ##### FCL Control Code Section #####
// The following code is the control code to determine the correct operation of the FCL.
// #####

interrupt void adc_isr(void)
{
    // This count variable is used to keep track of what interrupt instance is being checked
    interCount ++;

    // The following statements read in the voltage values (millivolts) into the integer
    // arrays. A history of 10 integers are stored to be able to calculate the derivative.
    // Get ADCRESULTS ----- //
    // discard ADCRESULT0 as part of the workaround to the 1st sample errata for rev0
    lineVoltage[ConversionCount] = ADC_readResult(myAdc,
ADC_ResultNumber_1); // J1(6) PIN
    semiconductorVoltage[ConversionCount] = ADC_readResult(myAdc,
ADC_ResultNumber_2); // J1(8) PIN
    mechanicalSwitchVoltage[ConversionCount] = ADC_readResult(myAdc,
ADC_ResultNumber_3); // J1(2) PIN

    // The following statements set flags if a derivative or magnitude limit is reached
    // indicating that a fault has occurred.
    // Fault Probes
    // --- derivative check --- //
    if (ConversionCount == 0)
        prevConversionCount = 9;
    lineCurrentDer = ((lineVoltage[ConversionCount] - lineVoltage[prevConversionCount])/200); // Might not be 200 will have to check
    // Convert negative values of derivative to positive
    if (lineCurrentDer < 0)
    {
        lineCurrentDer = lineCurrentDer*(-1);
    }
}

```

```

    }
    // --- magnitude check --- //
    lineCurrentMag = lineVoltage[ConversionCount];
    // Convert Current magnitude negative values to positive
    if (lineCurrentMag < 0)
    {
        lineCurrentMag = lineCurrentMag*(-1);
    }
    // The following conditional statement checks if the magnitude and the derivative limits
    // have been reached. The first one identifies the non-fault state and ensures that the
    // mechanical switch has been closed for normal operation. The next conditional
    // statement identifies the fault state then sets the state flag to indicate the fault.
    //!!! Note: the derivative limit check has not been tested and does not offer the required
    // functionality.
    // if (no fault)
    // normal operation
    if ((lineCurrentMag < triggerVoltage && faultSeq == 0) && lineCurrentDer <
triggerDer) // Change to AND
    {
        if (mechanicalLatch == open)
        {
            GPIO_toggle(myGpio, GPIO_Number_0); // J6(1) pin
            mechanicalLatch = closed;
            mechanicalStatus = closed;
        }
    }
    // fault detected
    else if ((lineCurrentMag > triggerVoltage && faultSeq == 0) || lineCurrentDer >
triggerDer)
    {
        faultSeq = 1;
        lineStatus = 1;
    }
}

// Once a fault has been detected, the state flag allows the program to continuously enter
// the conditional statement that manages operation of the mechanical and semiconductor
// switches.

// Fault Sequence
if (faultSeq > 0)
{
    // This switch statement checks the state of the fault sequence and applies the appropriate
    // case.
    switch (faultSeq)
    {

```

```
// In case 1, the conditional statement verifies that the semiconductor switch is in the
// non-faulted state (open) and then sends a voltage signal to the GPIO port and sets the
// semiconductor switch flag to closed.
```

```
// case 1: Turn on Semiconductors
```

```
    case 1:
    if (semiconductorLatch == open)
    {
        GPIO_toggle(myGpio, GPIO_Number_1); // J6(2) pin
        semiconductorLatch = closed;
    }
```

```
        semiconductorStatus = closed;
```

```
// The following conditional statement is the exit check of the semiconductor switch.
// Once the status has been set to closed, indicating that the semiconductor switch has
// closed physically, the next state of fault management is set. The break statement
// indicates that it is the end of the case and allows the execution of the code to exit the
// switch statement.
```

```
    if(semiconductorStatus == closed)
    {
        faultSeq = 2;
    }
    break;
```

```
// In case 2 of the fault sequence, the semiconductors are powered on to allow fault
// current to flow through. Now, the mechanical switch needs to open to break the current
// flow through it and begin to divert it to the magnet. The following conditional
// statement verifies that the mechanical switch is currently closed and then sends a
// voltage signal to the GPIO port to open the mechanical switch and sets the state of the
// mechanical switch to open.
```

```
    case 2:
    if (mechanicalLatch == closed)
    {
        GPIO_toggle(myGpio, GPIO_Number_0); // J6(1) pin
        mechanicalLatch = open;
    }
```

```
        mechanicalStatus = open;
```

```
// The following conditional statement is the exit check of the mechanical switch. Once
// the status has been set to open, indicating that the mechanical switch has closed
// physically, the next state of fault management is set. The break statement indicates that
// it is the end of the case and allows the execution of the code to exit the switch
// statement.
```

```
    if(mechanicalStatus == open)
    {
        faultSeq = 3;
    }
```

```

        break;

// In case 3 of the fault sequence, the mechanical switch is closed and the semiconductor
// switch needs to open to completely divert current to magnet. The conditional statement
// verifies that the semiconductors are closed and then sends a voltage signal to GPIO to
// switch the semiconductors to open and sets the semiconductor flag to open.
        case 3:
            if (semiconductorLatch == closed)
            {
                GPIO_toggle(myGpio, GPIO_Number_1); // J6(2) Pin
                semiconductorLatch = open;
            }

// The following conditional statement was designed to ensure that the fault current has
// been cleared for 1ms. Each iteration of the interrupt service routine increments the flag
// until 1ms has been reached. Additionally, the flag indicating that the line has been
// cleared is set. poll for zero fault
            if (lineVoltage[ConversionCount] < triggerVoltage &&
lineCurrentDer < triggerDer)
            {
                clearflag++;
            }

            if (clearflag > 4800) // approximately 40ms of cleared fault
            {
                lineStatus = 0;
                clearflag = 0;
            }

// The following conditional statement checks that the line has been cleared of fault
// current and sets the flag to continue the next iteration of the interrupt service routine for
// normal operation.
            if (lineStatus == 0)
            {
                faultSeq = 0;
            }
            break;
        }

    } // if (fault)

// The following conditional statement ensures that only 10 values are logged into the
// array of length 10. These arrays include the semiconductor and mechanical voltages.
// If 10 conversions have been logged, start over
    if (ConversionCount == 9)

```



```

{
    ConversionCount = 0;
    prevConversionCount = 9;
}
else
{
    ConversionCount++;
    prevConversionCount = ConversionCount - 1;
}

// Once the interrupt service routine is complete, flags must be cleared to allow the next
// interrupt to be serviced by the CPU with this interrupt service routine.

// Clear ADCINT1 flag reinitialize for next SOC
ADC_clearIntFlag(myAdc, ADC_IntNumber_1);
// Acknowledge interrupt to PIE

PIE_clearInt(myPie, PIE_GroupNumber_10);

return;
}

```

APPENDIX C

AMPL CODE

```
# Jay Prigmore
# NdFeB FCL Optimization Program
# Arizona State University
# 7-12-12
```

```
# The objective of this program is to calculate the minimum cost to produce
# a fault current limiter with a desired range of inputs using NdFeB Permanent
# Magnet as the core material for FCL applications. It gives an approximation
# to the core parameters and the limited fault current level specified by the
# percent reduction given.
```

```
##### System Parameter Inputs #####
# Voltage Level (Line to Neutral) (V)          VLN #
# Nominal Current (A)                          I_n  #
# Prospective Peak Fault Current (A)           I_sc  #
# Prospective Steady-State Fault Current (A)    I_ss  #
# Frequency (Hz)                              freq #
# Percent Reduction Desired [min,max]          PR  #
#####
```

```
##### NdFeB Inputs Parameters #####
# Length of Material (m)                      length #
# Width of Material (m)                      width  #
# Height of Material (m)                     height #
# Price of 1 unit ($U.S)                     Price  #
# Weight of 1 unit (kg)                      weight #
# Remanence Flux Density (T)                  Brem   #
# Saturation Flux Density (T)                 Bsath   #
# Coercitivity (A/m)                         Hcoerc  #
# Maximum Energy Product (kJ/m^3)             BH(max)#
# Saturation Coercitivity (A/m)               Hsat    #
# Curie Temperature (Celcius)                 Tc     #
# Permeability of Air (H/m)                   mu_zero #
# Maximum Core Permeability (H/m)             mu_core #
#####
```

```
##### Outputs #####
# Total Cost ($U.S)                          Total Cost #
# Area of the Core (m^2)                     Acore    #
# Mean Path length (m)                       lmean    #
# Number of turns                             N        #
# Dimensions (length x width x height) (m)   Dimensions #
# Number of magnets needed                    Mag_num  #
# Wire Gauge (AWG) (m)                       Gauge    #
# Maximum Inductance (H)                      L        #
```

```

# Percent Reduction                                PR_calc    #
# Weight of Device   (lbs)                        TotalWeight#
# New Peak Fault Current Level (A)                I_sc_new    #
# New Steady State Fault Current Level            I_ss_new    #
#####

##### Input Sets #####
set SYSTEM;          # System Data                #
set NDFEB;           # NdFeB Data                  #
set GAUGENUM;        # Copper Wire Gauge           #
#####

##### Parameters #####
# System Parameters
param VLN             {SYSTEM}; # 1 Line to Neutral Voltage
param I_n             {SYSTEM}; # 2 Nominal Current
param I_sc            {SYSTEM}; # 3 Potential Peak Fault Current
param I_ss            {SYSTEM}; # 4 Steady-State Fault Current
param freq            {SYSTEM}; # 5 Frequency
param PRmin           {SYSTEM}; # 6 Desired Minimum Percent Reduction
param PRmax           {SYSTEM}; # 7 Desired Maximum Percent Reduction

# Core Parameters:
param length          {NDFEB}; # 1 Length of NdFeB magnet in m= .102 m
param height          {NDFEB}; # 2 Height of NdFeB magnet in m= .102 m
param width           {NDFEB}; # 3 Width of NdFeB magnet in m= .0508 m
param weight          {NDFEB}; # 4 Weight of NdFeB magnet    = lbs
param Price           {NDFEB}; # 5 Price of NdFeB magnet     = $USD
param Brem            {NDFEB}; # 6 Remanence Flux Density    = 1.48 T
param Bsat            {NDFEB}; # 7 Saturation Flux Density= 1.6 T
param Hcoerc          {NDFEB}; # 8 Coercitivity= 11.2kOe = 891.3 kA/m
param Hsat            {NDFEB}; # 9 Saturation Coercitivity= 32 kOe = 2,586 kA/m or
986.3e3
param Tc              {NDFEB}; # 10 Curie Temperature   = 80 Celcius
param mu_zero         {NDFEB}; # 11 Permeability Constant   = 4*pi*e-7
param mu_core         {NDFEB}; # 12 Maximum Permeability of Core (del-
ta_B/delta_H)
param coreimpedance;   # 13 Core Impedance= 160e-6 ohm*cm

# param mu_core; let mu_core:=2e-5;
# BHMAX = 52 MGOe = 413.8 kJ/m^3
# Wire Gauge Parameters
param GaugeSize       {GAUGENUM}; # 1 Gauge Name
param diameter        {GAUGENUM}; # 2 Wire gauge diameters
param GaugeAmpacity   {GAUGENUM}; # 3 Gauge Ampacity

```

```

param GaugePrice      {GAUGENUM}; # 4 Price of Wire Gauge per meter
param GaugeRes        {GAUGENUM}; # 5 Gauge Resistance per meter
param wirediameter    {GAUGENUM}; # Diameter of chosen wire
param Size; let Size:=2; # Number of Segments in Core ( horizontal and vertical legs)
param pi; let pi:=3.14159265359;
#####

##### Variables #####
# Core Variables:
var N {n in NDFEB} >=1;# integer; # Number of turns
var Acore{n in NDFEB};      # Area of Core
var lmean{n in NDFEB} >= 1; # Mean Path Length
var Magnum {n in NDFEB} >= 1;# integer; # Number of magnets needed for design
var Gauge{n in NDFEB}>=0;    # Wire Gauge Needed
var L{n in NDFEB} >=0;      # Maximum Inductance
var lcore{s in 1..Size};    # core length sides
var wcore{s in 1..Size};    # core width sides
var hcore{s in 1..Size};    # core height sides
#var mu_core {n in NDFEB} >=0; # Core Permeability
var numlength{s in 1..Size} >= 1;# integer; # Number of magnets for sides of core
var numwidth{s in 1..Size} >=1;# integer; # Number of magnets for sides of core
var numheight{s in 1..Size} >=1;# integer; # Number of magnets for sides of core
var I_sc_new {n in NDFEB};   # New Peak Fault Current
var I_ss_new {n in NDFEB};   # New Steady State Fault Current
var wirelength{g in GAUGENUM} >=0; # Length of Copper Coil
var wireres{g in GAUGENUM} >=0;   # Resistance of chosen wire
var PR_sc{n in NDFEB};        # Percent reduction for peak current
var PR_ss{n in NDFEB};        # Percent reduction for steady-state current
#####

##### Input Data #####
data;
# System Parameters
param: SYSTEM: VLN I_n I_sc I_ss freq PRmin PRmax:= include FCLSystem.dat;
data;
# NdFeB Parameters
param: NDFEB: length height width Price weight Brem Bsat Hcoerc Hsat Tc mu_zero
mu_core:= include FCLNdFeB.dat;

# Wire Gauge Parameters
param: GAUGENUM: GaugeSize diameter GaugeAmpacity GaugePrice GaugeRes:=
include FCLGauge.dat;
#####

##### Objective #####

```

```

# objective
minimize TotalCost {n in NDFEB}: Price[n]*Magnum[n]+GaugePrice[n]*wirelength[n];
#####

##### Constraints #####
#### Physical Constraints ####
subject to LengthConst1 {n in NDFEB}: lcore[n] = length[n]*numlength[n];
# length of actual core * number of cores needed to meet length
subject to WidthConst1 {n in NDFEB}: wcore[n] = width[n]*numwidth[n];
# width of actual core * number of cores needed to meet width (depth)
subject to HeightConst1 {n in NDFEB}: hcore[n] = height[n]*numheight[n];
# height of actual core * number of core to meet desired height

subject to LengthConst2 {n in NDFEB}: numlength[n+1] = hcore[n]/length[n];
# length of actual core * number of cores needed to meet length
subject to WidthConst2 {n in NDFEB}: numwidth[n+1] = numwidth[n];
# width of actual core * number of cores needed to meet width (depth)
subject to HeightConst2 {n in NDFEB}: numheight[n+1] = (hcore[n+1]-
2*hcore[n])/height[n]; # length of actual core * number of cores needed to meet length

# Practical Physical Constraints
subject to LcoreConst {s in 1..Size, n in NDFEB}: length[n] <= lcore[s] <= 10*length[n];
# practical maximum and minimum limits for lcore
subject to WcoreConst {s in 1..Size, n in NDFEB}: width[n] <= wcore[s] <= 10*width[n];
# practical maximum and minimum limits for wcore
subject to HcoreConst {s in 1..Size, n in NDFEB}: height[n] <= hcore[s] <= 10*height[n];
# practical maximum and minimum limits for hcore

# Number of Magnets Needed Summation Constraint (Nonlinear constraint)
subject to TotalMagnetNumberConst {n in NDFEB}:
    Magnum[n] = sum {s in 1..Size} (2*(numlength[s]*numwidth[s]*numheight[s]));
# Sum of all the magnets needed to create physical design

# Additional Constraints
subject to CoreDesignConst1: lcore[1] = hcore[2]; # length of core 1 = height of core 2.
(Horizontal Legs)
subject to CoreDesignConst2: lcore[2] = hcore[1]; # legnth of core 2 = height of core 1.
(Vertical Legs)
subject to CoreDesignConst3: wcore[1] = wcore[2]; # Depth is the same at each leg of the
core

#### Parameter Constraints ####
subject to CrossSectionalAreaConst {n in NDFEB}: Acore[n] = hcore[n]*wcore[n];
# height of core leg 1*depth of core = Acore (Vertical Leg)

```

```

subject to MeanPathLengthConst1 {n in NDFEB}: lmean[n] = 2*(lcore[n]-
lcore[n+1])+2*(hcore[n+1]-hcore[n]); # Mean Path Length Constraint

subject to CrossSectionalConst2 {n in NDFEB}: length[1]*width[1] <= Acore[n];
# Cross sectional area is greater than product of magnet length and width
for {g in GAUGENUM} { # Determines and saves the minimum wire gauge needed
for the given normal current rating (I_n)
    if 3*GaugeAmpacity[g] > I_n[1] then{
        let wirediameter[1] := diameter[g];
        let Gauge[1] := GaugeSize[g];
        let GaugePrice[1] := GaugePrice[g];
        let wireres[1] := GaugeRes[g];
        break;
    }
}

subject to WireGaugeConst {n in NDFEB}: 0.8*(hcore[n+1]-2*hcore[n])*(lcore[n]-
2*lcore[n+1]) >= N[n]*wirediameter[n]**2; # Core maximum limit for height
subject to WireLengthConst {n in NDFEB}: wirelength[n]
=2*(2*wcore[n]+2*lcore[n+1])*N[n];
#subject to TurnsConst {n in NDFEB}: N[n] <=150;

##### Electrical Constraints #####

# Inductance Calculation Constraint (Non-Linear Equality)
subject to InductanceConst {n in NDFEB}: L[n] =
(mu_zero[n]*mu_core[n]*N[n]**2*Acore[n])/lmean[n];
# Inductance Calc approximation

# System Fault Current Calculation
subject to NewPeakFaultConst {n in NDFEB}: I_sc_new[n] =
VLN[n]/((2*pi*freq[n]*L[n])+(VLN[n]/I_sc[n])); # Reduced Peak fault current ...
VLN/I_sc models system resistance. +wireres[n]*wirelength[n]
subject to NewSteadyStateFaultConst {n in NDFEB}: I_ss_new[n] =
VLN[n]/((2*pi*freq[n]*L[n])+(VLN[n]/I_ss[n])); # Reduced Steady-State Fault current
.... VLN/I_ss models system ss resistance +wireres[n]*wirelength[n]

# Percent Reduction Constraint
subject to PRdefinitionConst1 {n in NDFEB}: PR_sc[n] = ((I_sc[n]-
I_sc_new[n])/I_sc[n]); # Percent reduction formula
subject to PRdefinitionConst2 {n in NDFEB}: PR_ss[n] = ((I_ss[n]-
I_ss_new[n])/I_ss[n]); # Percent reduction formula
subject to PercentReductionConst1 {n in NDFEB}: PRmin[n]<= PR_sc[n];
# Percent Reduction Peak
subject to PercentReductionConst2 {n in NDFEB}: PRmin[n]<= PR_ss[n];
# Percent Reduction SS

```

```
#####
option solver knitroampl; # minos, knitroampl, cplex
solve;
display TotalCost[1];

##### OUTPUT FILE #####
for{n in NDFEB} {
printf "Optimal NdFeB design for given parameters\n" > FCLOptimization.txt;
printf "\t\t\t\t\tNew NdFeB Core\t\t\tOld Saturable Iron Core\n" > FCLOptimization.txt;
printf "Total Cost for the Core ($): \t\t\t$%7.2f\t\t\t$200,000-300,000\n", TotalCost[n] >
FCLOptimization.txt;
printf "Area of the Core (m^2): \t\t\t%4.4f\t\t\t0.9213\n", Acore[n] > FCLOptimization.txt;
printf "Mean Path Length (m): \t\t\t%4.4f\t\t\t16\n", lmean[n] > FCLOptimization.txt;
printf "Number of Turns: \t\t\t%4d\t\t\t32\n", N[n] > FCLOptimization.txt;
printf "Overall Dimensions (l x w x h): \t\t\t%2.4f\t\t\t%2.4f\t\t\t%2.4f\t\t\t4 x 3 x 5\n", lcore[n],
wcore[n], hcore[n+1] > FCLOptimization.txt;
printf "Total Weight of the Core (lbs): \t\t\t%4.2f\t\t\t14,000-50,000\n",
weight[n]*Magnum[n] > FCLOptimization.txt;
printf "Maximum Inductance (mH): \t\t\t%7.7f\n", L[n]*1000 > FCLOptimization.txt;
printf "Percent Reduction Achieved Peak: \t\t\t%4.2f Percent\t\t\t45-55\n", PR_sc[n]*100
> FCLOptimization.txt;
printf "Percent Reduction Achieved SS: \t\t\t%4.2f Percent\t\t\t45-55\n", PR_ss[n]*100 >
FCLOptimization.txt;
printf "Number of Magnets Needed: \t\t\t%6d\n", Magnum[n] > FCLOptimization.txt;
if Gauge[n] > 40 then printf "Wire Gauge Needed: \t\t\t\t%4d MCM\n", Gauge[n] >
FCLOptimization.txt;
else printf "Wire Gauge Needed: \t\t\t\t%4d AWG\n", Gauge[n] > FCLOptimization.txt;
printf "New Peak Fault Current Level (kA): \t\t\t%7.2f\n", I_sc_new[n] > FCLOptimization.txt;
printf "New Steady-State Fault Current Level (kA): \t\t\t%7.2f\n\n", I_ss_new[n] >
FCLOptimization.txt;
printf "Other Potential Desired Information\n\n" > FCLOptimization.txt;
printf "Number of Magnets needed for length1: \t\t\t%4.2f\n", numlength[n] > FCLOptimization.txt;
printf "Number of Magnets needed for width1: \t\t\t%4.2f\n", numwidth[n] > FCLOptimization.txt;
printf "Number of Magnets needed for height1: \t\t\t%4.2f\n\n", numheight[n] > FCLOptimization.txt;
printf "Number of Magnets needed for length2: \t\t\t%4.2f\n", numlength[n+1] > FCLOptimization.txt;
printf "Number of Magnets needed for width2: \t\t\t%4.2f\n", numwidth[n+1] > FCLOptimization.txt;
printf "Number of Magnets needed for height2: \t\t\t%4.2f\n", numheight[n+1] > FCLOptimization.txt;
}
```



```
printf "Core Permeability Calculation:      \t%4.1f\n", mu_core[n] > FCLOptimiza-
tion.txt;
printf "Length of Wire Needed for Turns: \t%4.3f\n", wirelength[n] > FCLOptimiza-
tion.txt;
printf "Resistance of turns: \t%4.7f\n", wireres[n]*wirelength[n] > FCLOptimization.txt;
};
#####
```

	Size (AWG/MCM)	Diameter (m)	Ampacity (A)	Price (\$/m)	Resistance (ohms/m)
1	20	0.00081	7	0.18	0.0333
2	18	0.00102	10	0.33	0.0209
3	16	0.00129	15	0.71	0.0132
4	14	0.00163	22	0.79	0.00827
5	12	0.00205	33	1.04	0.00520
6	10	0.00259	40	1.58	0.00327
7	8	0.00326	55	2.48	0.00206
8	6	0.00412	75	3.95	0.00129
9	4	0.00519	95	6.20	0.000814
10	3	0.00583	110	7.62	0.000645
11	2	0.00654	130	9.03	0.000512
12	1	0.00735	150	13.12	0.000406
13	0	0.00825	170	14.74	0.000322
14	00	0.00927	195	18.13	0.000255
15	000	0.0104	225	22.47	0.000202
16	0000	0.01168	260	27.60	0.000161
17	250	0.0127	290	35.31	0.00013609
18	300	0.01391	320	42.13	0.00011341
19	350	0.01503	350	48.41	0.00009721
20	400	0.01606	380	53.04	0.00008498
21	450	0.01704	405	60.65	0.00007651
22	500	0.01796	430	68.26	0.00006804
23	600	0.01967	475	82.15	0.00006045
24	700	0.02125	520	94.70	0.00005463
25	750	0.022	535	102.86	0.00004881
26	800	0.02272	555	108.67	0.00004339
27	900	0.0241	585	120.05	0.00003870
28	1000	0.0254	615	131.43	0.00003402
29	1250	0.0284	665	142.81	0.00002857
30	1500	0.03111	705	154.19	0.00002311
31	1750	0.0336	735	165.57	0.00002022
32	2000	0.03592	750	176.95	0.00001732

Source <http://www.interfacebus.com/table-of-awg-wire-gauge-standards-metric.html>

Source <http://amasci.com/tesla/wire1.html>

Source <http://www.pearen.ca/Reference/wire.htm>

Prices from <http://www.phelpsdodge.com.ph/Word%20Documents/THHN.pdf>

Prices were determined on January 7th 2013.

General rule for short wire use 1A/200 or 300 mils and for long wires use 1A/700 mils for constant current.

The ampacities in the table use 1A/700 mils which is a very conservative estimate.