An Electrical-Stimulus-Only BIST IC For
Capacitive MEMS Accelerometer Sensitivity Characterization

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved October 2017 by the
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December 2017

ABSTRACT

Testing and calibration constitute a significant part of the overall manufacturing cost of microelectromechanical system (MEMS) devices. Developing a low-cost testing and calibration scheme applicable at the user side that ensures the continuous reliability and accuracy is a crucial need. The main purpose of testing is to eliminate defective devices and to verify the qualifications of a product is met. The calibration process for capacitive MEMS devices, for the most part, entails the determination of the mechanical sensitivity. In this work, a physical-stimulus-free built-in-self-test (BIST) integrated circuit (IC) design characterizing the sensitivity of capacitive MEMS accelerometers is presented. The BIST circuitry can extract the amplitude and phase response of the acceleration sensor's mechanics under electrical excitation within 0.55% of error with respect to its mechanical sensitivity under the physical stimulus. Sensitivity characterization is performed using a low computation complexity multivariate linear regression model. The BIST circuitry maximizes the use of existing analog and mixed-signal readout signal chain and the host processor core, without the need for computationally expensive Fast Fourier Transform (FFT)-based approaches. The BIST IC is designed and fabricated using the 0.18- μm CMOS technology. The sensor analog front-end and BIST circuitry are integrated with a three-axis, low-g capacitive MEMS accelerometer in a single hermetically sealed package. The BIST circuitry occupies 0.3 mm^2 with a total readout IC area of 1.0 mm^2 and consumes 8.9 mW during self-test operation.

ACKNOWLEDGMENTS

First and foremost, I would like to thank my advisors, Dr. Bertan Bakkaloglu and Dr. Sule Ozev, for their tremendous support, endless patience, and invaluable assistance that have led me to complete my Ph.D. degree successfully. Also, I would like to thank Dr. Sayfe Kiaei and Dr. Umit Ogras for serving as my Ph.D. committee members, challenging me to extend my knowledge and capabilities. I must also thank my project mates Vinay Kundur and Naveen Sai Jangala for their great friendship, help, and hard work. Special thanks to James Laux for his support in software and system related issues.

I also would like to present my special thanks to Freescale team members Dr. Tehmoor Dar, Mike Cheperak, Peggy Kniffin, Bruno Debeurre, Ray Sessego, Dr. Mark Schlarmann and many others for their valuable support during this research.

Finally, I want to thank my parents Senay Ozel and Selahattin Ozel for always being there for me. I could not have done this without their love, encouragement and constant support.

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CHAPTER 1

INTRODUCTION

Microelectromechanical systems (MEMS) represent a class of miniature electro-mechanical systems [1]. The MEMS technology has rapidly expanded in the last 50 years and has been implemented in many areas, such as consumer products, aerospace, automotive, biomedical, chemical, military, optical displays, wireless and optical communications and fluidics, etc., where miniaturization is valuable [2]. MEMS-based motion sensors such as MEMS gyroscopes and MEMS accelerometers are a class of inertial sensors [3]. They are in micro-scale. Compared to traditional ones, they have the advantage of small size, low cost, lightweight, low power consumption, high sensitivity, excellent linearity and high precision [4]. Thus, they have been applied extensively in the areas of automobiles, consumer electronics, spacecraft and robotics [5], specifically in the consumer-grade application of motion interface [6]. For instance, in the automotive industry, accelerometers are used for airbags; pressure sensors are used for monitoring the engine and tire pressure, and gyroscopes are used for navigation and control. Overall, the MEMS technology is extensively applied in our daily life.

The increase in their popularity helped with reducing the cost and complexity of fabrication as well as packaging techniques with high-performance readout electronics [7]. However, testing and calibration of MEMS devices are still an important component of their overall manufacturing cost [8], [9]. In some safety-critical sensor applications such as automotive-electronic systems, it can go up to 60% of the entire cost of the unit [10]. This percentage is coming down, but the physical world prevents it happening smoothly. The

physical world is unpredictable, thus requiring comprehensive testing, evaluation, and fine-calibration.

Testing of MEMS includes device characterization tests, product qualification tests, fabrication tests, product tests and in-field tests especially self-tests [11]. The purpose of the characterization tests is to examine the performance limits of the device under test (DUT) and to gather information about how their performances are affected by fabrication tolerances and environmental conditions. Characterization tests are crucial to determine the pass-fail criteria of the device. Qualification tests are the basis of qualification procedures for various stages of the fabrication process and the final product. These tests are specific to a given product and are applied in accordance with the requirements of a certain standard. For example, an automotive application includes around 50 standardized tests [11]. Fabrication tests are used to observe the entire production chain. They consist of a set of parametric tests for all production steps, and they need to guarantee the repeatability of all manufacturing procedures within predefined tolerances. Product testing is used to verify the requirements of a product is met. They are at the core of the final production test. In-field tests are used to detect deviations from typical performance-related specifications caused by the environmental conditions. Therefore, they are important to enhance the reliability of a MEMS device.

To eliminate defective MEMS dies to save costs associated with packaging and/or application-specific integrated circuits (ASICs), MEMS devices require extensive characterization at the wafer level. There are two major wafer level testing approaches: static and dynamic measurements. Static measurements are straightforward structural tests, such as continuity and dc tests. The primary objective is to eliminate defective MEMS dies.

Currently, static measurements are more commonly used in the industry, due to their low cost and low complexity implementation. However, they are time-consuming and has limited fault coverage. Dynamic measurements can extract more diagnostics information, but due to their high cost, they are currently used in a small number of applications. A few examples of dynamic measurements include measuring frequency-dependent characteristics such as resonance frequency and damping factor of MEMS sensors.

In addition to testing, calibration is another critical step in MEMS manufacturing [12]. Due to process variation in fabrication and their sensitivity to environmental disturbances, such as shock, vibration and temperature change, a significant portion of the MEMS sensor signals includes errors such as noise, offset and drift. Additionally, these errors can be accumulated over time. To facilitate accurate readings from the devices and maximize their performance across a broad range of mechanical excitation, effective calibration of their mechanical to electrical conversion characteristics is necessary. Conventional calibration methods require applying physical stimulus and measuring its electrical response [13]. However, physical stimuli require the use of specific and sophisticated automatic test equipment (ATE), which is far more expensive in comparison to standard mixed-signal testers. Furthermore, even after calibration at the manufacturing site, the devices change their behavior during field operation [14]. Developing low-cost calibration schemes applicable at the user side that guarantee the continuous reliability and accuracy is a critical need.

Over the past several decades, various electrical-only testing and calibration approaches have been proposed and implemented for MEMS devices. These methods can be summed up in 4 main categories: sensitivity testing, symmetry testing, parameter

extraction and indirect testing. Although these methods are built-in-self-test (BIST) compatible, not all of them can be used as an electrical-only calibration method, without the need for physical stimuli.

In sensitivity testing, the electrostatic force generated by a self-test (ST) voltage is used to mimic the action of an inertial force caused by a physical acceleration [15]–[17]. Several excitation plates are reserved for BIST as shown in Fig. 1.1. The output response is measured and compared to the right device behavior. Voltage-induced electrostatic force is simple to generate, and hence it has been widely used for in-field BIST of MEMS accelerometers. The main disadvantage of the electrical sensitivity testing method is that considering the fabrication variations, the ST voltage needs to be corrected for each device before the device operates in ST mode, which makes it a challenge to be utilized as a calibration method.

Fig. 1.1. BIST of a surface-micromachined comb accelerometer using electrostatic force [17].

Symmetry testing is very similar to sensitivity testing regarding actuation method as it also uses electrical excitation to generate the effect of physical acceleration. Fig. 1.2 shows a typical MEMS differential capacitance structure. Here MM denotes the movable-mass, F1 and F2 represent fixed plates, while B1 and B2 are both beams of the MEMS

devices. MM is anchored to the substrate through two flexible beams B1 and B2. In symmetry testing, each of the top and bottom fixed capacitance plates is divided into two equal portions as shown in Fig. 1.2. The basic idea of symmetry test scheme is to check if the two symmetric capacitances (e.g., C1 and C2 in Fig. 1.2) on the same side of the MM remain equal after activation.

Fig. 1.2. Schematic diagram of a capacitive MEMS device and the structure of the symmetry test scheme [19].

The method aims to detect any asymmetry caused by local defects, wear, and problems due to imperfection in the design and fabrication process [18]–[20]. It yields higher fault coverage compared to sensitivity testing. The primary disadvantage of this method is that it is unable to detect defects common to both sides of the structure. Furthermore, it can only be applied to symmetrical structures, which limits its application area. Note that none of the preceding techniques can be used as an alternative calibration method since they can only measure electrical sensitivity. Although several pre-defined voltages can be applied to generate electrostatic forces that can be used to calibrate the system, in theory, too many tolerances prevent straightforward implementation of such a principle [7].

The basic idea behind parameter extraction is to use a single-tone or multi-tone ac signal that actuates the sensing beams and varies the capacitance of the accelerometer to

predict the mechanical parameters such as mass, damping coefficient and spring constant while using regression-based mapping technique [21]. In most cases, an active capacitance sensing circuit measures the effective capacitance of the beam. Although this method does not evaluate the sensitivity of the device, it has the potential to eliminate the use of expensive physical test instrumentation for calibration purposes. This is because it effectively shows how the electrical parameters are correlated with parameters of the mechanical structure. Using this approach, the parameters were predicted with an accuracy of less than 5% of the actual value in simulations [21].

The parameter extraction method assumes the system is under external acceleration and it is in its linear response region. However, the voltage-controlled parallel-plate electrostatic actuator, which is commonly used in MEMS accelerometers is a nonlinear system making it burdensome to reach a closed form solution [22]. Rather than attempting to model the system and solve for the mechanical parameters, an indirect method can be used to measure parameters highly correlated with the sensor dynamics; such as resonance frequency, electrical sensitivity, non-linearity or pull-in voltage. In [23], the deviation in amplitude response and the resonance frequency of a Pierce oscillator is used to detect possible structural defects such as missing fingers, short fingers, and tilted arms.

Fig. 1.3. Block diagram of a capacitive MEMS sensor utilizing a Pierce oscillator [23].

Fig. 1.3 shows the block diagram of the proposed test setup. At resonance, the input and the output of the delay line are shorted, and the delay cells form a ring oscillator. It has been shown that even minor deviations from the nominal device capacitance shifts the frequency of oscillation notably and this information is correlated to structural defects. In [24], two distinct calibration procedures have been evaluated: analytical method and regression method. Fig. 1.4 shows the schematic view of the sensor system and the expected output waveforms for various excitation modes.

Fig. 1.4. Block diagram of a BIST system that can measure natural frequency, electrical sensitivity, and pull-in voltage of an accelerometer to calibrate the mechanical sensitivity [24].

In analytical method, mechanical sensitivity is calculated from natural frequency, electrical sensitivity and pull-in voltage measurements. Mechanical sensitivity was predicted with a best-case accuracy of $\pm 15\%$ in this method. In regression approach, after using 120 sensors for training purposes, electrical parameters were mapped to actual mechanical sensitivity by using multivariate adaptive regression splines (MARS) method and $\pm 5\%$ accuracy in sensitivity prediction was achieved.

In this study, a low area and power overhead on-chip circuitry for testing and physical-stimulus-free calibration purposes is presented. A set of necessary electrical measurements, which can be conducted with on-chip circuitry is analyzed. Using the proposed low-complexity BIST circuitry, a statistical model is also developed. This work

presents the first monolithic implementation of electrical-only self-test and calibration methodology. The circuitry includes three major blocks: a digital-to-analog converter (DAC), a dc-blocked charge-to-voltage (C2V) amplifier, and an analog-to-digital converter (ADC) as displayed in Fig. 1.5.

Fig. 1.5. Simplified block diagram of the proposed BIST IC.

The proposed approach measures the amplitude and phase response, as well as the offset of the capacitive MEMS accelerometers, which establishes a correlation between the mechanical sensitivity and the electrical characteristics applying multivariate linear regression method and predicts the mechanical sensitivity employing the built statistical model. Experimental results of the fabricated devices show 0.55% rms error in the predicted mechanical sensitivity with respect to mechanical stimulus. The BIST circuitry is built on a single poly, 6LM 0.18- μm CMOS process and dissipates 8.9 mW of power during self-test operation. When circuit blocks that are shared with the regular mode of operation such as ADC and C2V converter of the front-end are excluded, the proposed BIST circuitry only occupies 0.3 mm².

1.1 Outline

The rest of the dissertation is organized as follows: in chapter 2 system level operation of the BIST circuitry and its correlation to physical stimuli is introduced. Circuit

level implementation of the BIST approach is described in chapter 3. Signal extraction is introduced in chapter 4, and it is followed by system level simulation and measurement results in chapter 5. Lastly, the conclusion is presented in chapter 6.

CHAPTER 2

MEMS BIST SYSTEM LEVEL IMPLEMENTATION

2.1 Introduction

The BIST-based test and calibration methodology assumes that MEMS sensor response to electrical stimulus and physical stimulus are highly correlated. The proposed statistical model aims to establish this correlation with the minimum computational burden to enable fully-electrical sensitivity prediction. As Fig. 2.1 shows, the proposed method includes two phases: statistical learning and production testing.

Fig. 2.1. Block diagram of the proposed BIST-based test and calibration methodology.

The primary goal of the learning phase is to gather data and build the model between the mechanical sensitivity and electrical characteristics of the training devices. Therefore, it involves both electrical and physical actuation. Once the model is built, the need for physical stimulus vanishes in production test phase, and sensitivity can be predicted through electrical measurements only. One thing to note in statistical learning phase is that there might be defective devices that behave significantly different than the

bulk of the population and they display random behavior. Due to this randomness, they may corrupt the learning process. Therefore, the statistical model does not include far-off behaving devices.

2.2 Spring-Mass Structure and its Calibration

Fig. 2.2 shows the mechanical structure of a spring-mass capacitive accelerometer. Two fixed plates together with an MM form the capacitors, C_{s1} and C_{s2} . Depending on the axis chosen, the fixed plates are named as $x1-x2$, $y1-y2$ or $z1-z2$.

Fig. 2.2. Simplified mechanical structure of a spring-mass capacitive accelerometer.

If an acceleration of a is applied in any direction, the MM will respond to this excitation and move by an amount of x , then, C_{s1} and C_{s2} can be calculated as:

$$C_{s1} = \epsilon \frac{A}{d-x} \quad C_{s2} = \epsilon \frac{A}{d+x} \quad (2.1)$$

Here ϵ is the dielectric permittivity, A is the area of the sense plates and d is the nominal distance between MM and fixed plates. Assuming $x \ll d$, one can obtain a linear relation between ΔC_s , the capacitance difference between C_{s1} and C_{s2} , and the applied acceleration a in g (earth's gravity) as:

$$\Delta C_s = 9.8 \frac{2 \cdot \varepsilon \cdot A}{d^2} \frac{m}{k} a \quad (2.2)$$

where m is the mass of the MM and k is the spring constant. The coefficient between the measurable quantity ΔC_s and a is the untrimmed mechanical sensitivity of the system, defined by

$$S = \frac{\Delta C_s}{a} = 9.8 \frac{2 \cdot \varepsilon \cdot A}{d^2} \frac{m}{k} = 9.8 \frac{2 \cdot \varepsilon \cdot A}{d^2} \frac{1}{(2\pi \cdot f_0)^2} \quad (2.3)$$

Here f_0 is the mechanical resonance frequency of the spring-mass system. In most cases, calibration of capacitive MEMS accelerometers involves determining the trimming value, which is a function of S . As shown in Eq. 2.3, the mechanical sensitivity of a capacitive MEMS accelerometer is directly proportional to two capacitors, C_{s1} and C_{s2} , and inversely proportional to the square of f_0 . Thus, one can conclude that the frequency domain amplitude response of a capacitive MEMS device is directly related to mechanical sensitivity. This is because the low-frequency amplitude response A_{low} as well as the roll-off (A_{high} / A_{low}) are linked to C_{s1} and C_{s2} , and the resonance frequency, respectively. Notice that the amplitude response is likely to change by parasitics in the sensor, the sensor-to-ASIC connection and the loading by the ASIC or tester. Hence, using phase information provides an additional tool to establish an improved relationship with mechanical sensitivity.

2.3 Electrically-Controlled Capacitive Accelerometer

The operating principle of an electrically excited capacitive accelerometer is similar to a physically stimulated one, but different dynamics must be considered. For a voltage-controlled spring-mass capacitive accelerometer, the induced electrical force on an MM, defined by F_e , is given by

$$F_e = \frac{1}{2} \frac{\varepsilon \cdot A}{d^2} V^2 \quad (2.4)$$

where V is the voltage across MM and fixed excitation plate. Note that there is a square-law relationship between force F_e and applied voltage V . Therefore if a sinusoidal signal at a frequency of f_{in} is applied to a fixed excitation plate, due to quadratic relation, acceleration at $2f_{in}$ as well as an offset term of d_{off_elec} will be generated. Thus, the total offset between plates for an electrically excited accelerometer is the vector sum of d_{off} and d_{off_elec} . Here d_{off} is the shift in the nominal distance d between MM and fixed plates caused by the process variations in MEMS fabrication. Although we are interested in the ac response for the physical-stimulus-free calibration technique, the total static offset is a major component of the proposed statistical model since it alters the electrical force and causes a change in the ac characteristics of the device. Thus, the mathematical model must include the total offset for a more accurate sensitivity prediction.

For an electrostatically-actuated beam, electrostatic attractive force F_e leads to a decrease of the gap spacing, thereby stretching the spring. This gives rise to an increase of the spring force, which opposes the electrostatic force. The phenomenon called pull-in instability occurs because the F_e increases non-linearly with decreasing gap spacing, whereas the spring force is a linear function of the change in the gap spacing. The pull-in voltage V_{pull_in} can be defined as the voltage at which the restoring spring force can no longer balance the electrostatic force F_e . The V_{pull_in} can be obtained based on the equivalence of forced and minimization of potential energy and is given by [25]

$$V_{pull\_in} = \sqrt{\frac{8}{27} \frac{k \cdot d^3}{\varepsilon_0 \cdot A}} \quad (2.5)$$

where ε_0 is the permittivity of free space.

2.4 Statistical Modeling Approach

In our statistical model, the mechanical sensitivity S is a function of four parameters extracted from four electrical measurements during the learning phase as shown below:

$$S = f(A_{low}, A_{high} / A_{low}, \phi_{high}, V_{off}) \quad (2.6)$$

where S is the dependent variable and only taken in the learning phase under the physical stimulus. Regarding sensor dynamics, A_{low} is related to electrical sensitivity and total MM offset, (A_{high} / A_{low}) and ϕ_{high} are related to the resonance frequency, and V_{off} is linked with MM offset. Here ϕ_{high} is the phase shift due to an electrical excitation signal with a frequency close to the resonance frequency of the sensing device. Also, V_{off} is the dc output voltage of the BIST IC corresponding to total static MM offset. The statistical model aims to establish the correlation between the mechanical sensitivity and the electrical characteristics from a set of training devices by fitting a regression line equation given in

$$S = c + \alpha_1 A_{low} + \alpha_2 (A_{high} / A_{low}) + \alpha_3 \phi_{high} + \alpha_4 V_{off} \quad (2.7)$$

Due to its simplicity, accuracy, and ease of implementation in the production test phase, multivariate linear regression method is used to establish the correlation. As shown in Eq. 2.7, $\alpha_1, \alpha_2, \alpha_3, \alpha_4$ are the weights of each independent variables, and they relate the electrical observations with the mechanical sensitivity. After correlation is established using a sufficient number of training devices, Eq. 2.7 is used to calculate S_{pre} , the predicted mechanical sensitivity of the DUT, during the production test phase. The accuracy of the statistical model and therefore of the proposed electrical-only sensitivity characterization counts on the % rms error between S and S_{pre} .

CHAPTER 3

BIST CIRCUIT IMPLEMENTATION

3.1 Modes of Operation

The block level diagram of the proposed BIST IC is shown in Fig. 3.1. It has two modes of operation: electrical stimulus based BIST mode and functional readout mode. Electrical stimulus mode aims to measure the frequency response of the sensor under test.

Fig. 3.1. Block level diagram of the proposed BIST IC.

During BIST operation, an on-chip sine-weighted DAC stimulates one of the fixed electrodes of the accelerometer with a sinusoidal excitation. The ac part of the capacitance between MM and the non-selected electrode causes V_{out} to be generated at the output of the C2V. Note that the proposed circuitry can switch between stimulus and sensing plates, which enables characterization of both sense capacitors during BIST mode.

Functional readout mode is used to measure the sensitivity of the accelerometer under the physical stimulus. This mode is required to build the correlation between electrical parameters and mechanical sensitivity of the sensor to validate the proposed electrical-only testing and calibration approach. During this mode, the dc voltage of V_{int} , which is proportional to ΔC_s , is generated at the output of the integrator, which is in the

feedback path of the charge amplifier. The transfer function between the sensor input and V_{int} for frequencies below f_0 is given as:

$$\frac{dV_{int}}{da} = 9.8 \frac{2 \cdot C_s}{d} \frac{V_{cm}}{C_i} \frac{1}{(2\pi \cdot f_0)^2} \quad (3.1)$$

where V_{cm} is the common-mode (CM) voltage of the chip, 1.65 V. V_{int} at two distinct accelerations is used as the sensitivity estimate of the device.

3.2 Sinusoidal Stimulus Generation

Traditional test methodologies require an ATE that can generate high-quality stimuli. However, the stimulus generator of a BIST IC needs to be compact and require minor design effort. Its performance requirements are usually not as stringent as an ATE's. The following two sections briefly talk about the most popular two techniques used for sinusoidal signal generation.

3.2.1 Phase-Locked Loops (PLLs)

PLLs for decades have been one of the most common ways to generate signals on-chip. A PLL typically consists of a reference clock, a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a frequency divider as shown in Fig. 3.2.

Fig. 3.2. Block diagram of a typical PLL structure.

PFD, as the name implies, compares the phase difference between the reference clock and the feedback signal and generates pulses that control the switches in CP. These current pulses are then filtered out to prevent unwanted spurious noise and converted to a control voltage that tunes the frequency of the VCO. Divider controls the frequency relationship between the reference clock and the output signal.

3.2.2 Direct-Digital Frequency Synthesizer (DDFS)

DDFSs are commonly designed using a topology developed by Tierney et al. [26]. This powerful yet simple architecture, which is displayed in Fig. 3.3 applies the modulo 2^L overflowing property of an L -bit accumulator to produce the phase argument to the sine function generation logic [26]. The 2^L words of the accumulator output are mapped into phase values so that

Fig. 3.3. The overall architecture of a typical DDFS structure [26].

$$\theta(n) = 2\pi(\phi(n) / 2^L) \quad (3.2)$$

where $\phi(n)$ represents the contents of the phase accumulator at time $t = n / f_{clk}$. Here f_{clk} is the clocking frequency of the synthesizer. On each clock cycle, a digital frequency tuning word M is added to the previous value of the accumulator such that $\phi(n+1) = M + \phi(n)$. Thus, the output frequency of the DDFS is given by

$$f_{out} = \frac{M \cdot f_{clk}}{2^L} \quad (3.3)$$

DDFS based sine wave generation has significant advantages over other frequency synthesis techniques. As seen in Eq. 3.3, remarkably fine frequency resolution can be achieved since each additional phase accumulator bit halves the frequency spacing. Another significant benefit of a DDFS is fast switching speed. A DDFS may tune between any frequencies in one reference clock period [26].

Generating a sine-wave using PLL technique requires a lot of design effort, and its complex architecture makes it less suitable to use in a BIST IC. Due to its simplicity and low die area overhead, an on-chip DDFS with a sine-weighted DAC is used to excite the selected electrode and displace the proof-mass.

3.2.3 Digital-to-Analog Conversion

3.2.3.1 Control Logic

The control logic forms an important part of stimulus generation. It is composed of an up-converter followed by a decoder and a digital logic as shown in Fig. 3.4. The counter is a 5-bit up counter, and it is reset every 24 cycles. The five most significant bits (MSBs) of the DDFS's phase accumulator is used as the clock for the counter. The decoder then generates 24 phases and the digital logic groups these phases and controls the switches of the DAC [27].

Fig. 3.4. Block diagram of the digital circuitry that controls the DAC switches [27].

3.2.3.2 Sine-Wave Generation

The most widely used sine-wave generation methods are current-steering, switched-capacitor (SC) and resistor string methods. Current-steering D/A converters are formed using an array of matched current sources that are switched to the output [28]. The current is then converted to voltage with a simple resistor. Current source DACs are popular due to the smaller space used by MOSFET current elements and capacity to perform some calibration tricks [29]. SC DACs are the most common DAC topology for ADC architectures. They can be configured to realize different functions, making them good for implementing various types of mathematical algorithms in addition to DAC operation [29]. One of the biggest benefits of capacitor DACs is that capacitor arrays use no quiescent current, unlike resistor or current arrays. SC DACs trade clock cycles and time for reduced components versus resolution. Resistor DACs are valued for their simplicity and speed. They are not preferred in very low-power architectures since they consume continuous current, unlike capacitive DAC topologies. Here due to its simplicity, sine-wave generation is implemented using a resistive string as shown in Fig. 3.5.

Fig. 3.5. Block diagram of the sine-weighted resistor string.

The figure also shows the resistor values used in the resistor string. The chain is composed of series or parallel combinations of the unit resistor of 3.7 kOhms, and it generates a sine-weighted waveform. The switches p1-p13 are controlled by the control logic block displayed in Fig. 3.4. The timing diagram illustrating the switching behavior of the switches of the resistor string is given in Fig. 3.6. Here only one of the switches is turned-on at a given time. Note that this diagram shows the switching behavior only for the DAC output voltages above V_{cm} .

Fig. 3.6. An example timing diagram of the switches that control the resistor string output.

Note that the output of the resistive string is filtered out to minimize the effect of the glitches due to switching and harmonic distortion on the DAC output. The filter output drives a rail-to-rail input transconductance amplifier whose output is used to stimulate the accelerometer electrically.

3.2.3.3 Rail-to-Rail Input DAC Transconductance Amplifier

The resistor string is followed by a buffer amplifier to isolate the sensing device from the signal generator. For the usual differential pair used as an input stage of a differential amplifier, with 1 V threshold voltage and 3 V power supply, the input common-mode range is less than 2 V [30]. This is a significant drawback especially for a general-purpose amplifier such as a unity gain buffer used in this application. In a simple rail-to-rail input stage, an n-channel differential pair and a p-channel differential pair are used in parallel as shown in Fig. 3.7.

Fig. 3.7. Rail-to-rail input amplifier used in signal generation block [27].

There are three operation regions; when the V_{cm} is near the negative power supply, only the p-channel pair operates. For V_{cm} near the positive power supply, only the n-channel pair runs. For V_{cm} around mid-rail, both differential pairs work. Therefore, at least one of the two differential pairs will be working for any V_{cm} between the rails. The transconductance amplifier used in DAC achieves a unity gain frequency (UGF) of 75 MHz with a typical dc gain and phase margin of 46 dB and 80°, respectively. Also, total integrated noise from

100Hz to 12 kHz is $72 \times 10^{-6} \text{ V/Hz}^{0.5}$ at 300 K. Noise specification of the amplifier is not stringent since the DAC noise does not have a direct influence on the total output noise of the BIST signal chain.

3.2.4 Proposed Sine-Weighted DDFS Based Stimulus Generator

System-level diagram of the proposed stimulus generator is shown in Fig. 3.8. For an operating frequency of 1 MHz, f_{out} can achieve 15 Hz frequency resolution. The sine-weighted DAC can generate a 2.7 V_{pp} output voltage swing as displayed in Fig. 3.9. This swing results in a capacitance variation that is equivalent to 6g peak physical acceleration approximately, and it enables sufficient output for dynamic characterization of the sensor. Even though included, the proposed approach does not require a low-pass filter to suppress higher order harmonics of f_{out} since these harmonics are well beyond the resonance frequency of the sensor and thus do not cause displacement of the proof-mass.

Fig. 3.8. System-level representation of the sine-weighted resistor string based direct digital stimulus generator DAC.

Fig. 3.9. Output waveform for 1 kHz DAC output.

The measured power spectral density (PSD) plot of the DAC output for a 1 kHz electrical stimulus signal is given in Fig. 3.10. As can be seen from the figure, DAC output yields some degree of harmonic distortion. It achieves 45 dB spurious-free dynamic range (SFDR).

Fig. 3.10. PSD of DAC output for a sine-weighted excitation signal of 1 kHz.

Fig. 3.11. The layout of the excitation signal generation block.

The layout of the stimulus signal generation circuitry is given in Fig. 3.11. It occupies an area of $475\mu\text{m} \times 260\mu\text{m}$ and dissipates 0.8 mW. Note that BIST IC can also utilize an external stimulus signal to characterize the sensor.

3.3 Analog Front-End Design

Fig. 3.12 illustrates the single-ended version of the SC charge amplifier operating at f_s of 1 MHz. As a result of a sinusoidal electrical excitation at a frequency of f_{in} , the capacitance varies at the second harmonic of the excitation frequency, and its value can be represented as:

$$C_s(t) = C_{s\_dc} + C_{s\_ac} \sin(2\pi \cdot 2 \cdot f_{in} \cdot t) \quad (3.4)$$

where C_{s_dc} represents the base capacitance, and it is much larger than the mechanical

Fig. 3.12. The proposed SC charge amplifier with a multi-rate servo feedback based dc-blocking. sensing capacitance C_{s_ac} . Since stimulus frequency f_{in} is much less than the sampling rate f_s , the sensing capacitance can be assumed constant during sampling phase of ϕ_1 . Thus, at the end of integration period of ϕ_2 , the voltage at the charge integrator output $|V_{out}[n]|$ is represented by:

$$|V_{out}[n]| = \left(\frac{C_{s\_dc}[n-1]}{C_i} + \frac{C_{s\_ac}[n-1]}{C_i} \right) \times V_{cm} \quad (3.5)$$

C_{s_ac} given in Eq. 3.5 primarily depends on the sensitivity of the sensor, and its typical value is 4.05 fF/g for the accelerometer under test. To have a sufficiently high amplitude sensor response at the end of the BIST signal chain, C_i is kept low to maximize the gain term of (C_s/C_i) . The charge amplifier used in this work has an optional gain mode of 7 dB, 10 dB, and 16 dB. The high gain of charge amplifier also helps with suppressing the noise contributions from subsequent stages. However, keeping C_i low also increases the dc signal level. Therefore, the read-out ac signal has a very high CM dc level in comparison to its ac level. If not successfully removed, this high dc level would saturate

the analog-front-end following the signal. Eliminating the dc part is not needed in conventional MEMS readout circuits under the physical stimulus since the sensor is read-out fully-differentially [31], [32]. Furthermore, some of the earlier electrical-only testing approaches did not require removing the dc term because they either employed sense plate or proof-mass portioning [19], which causes an electrical insulation between excitation and readout plates and makes differential readout feasible. Unlike earlier approaches, the proposed BIST circuitry operates independent of the MEMS sensor design and enables both post-fabrication as well as in the field self-test and calibration of capacitive sensors.

3.3.1 Continuous-Time (CT) Equivalent of the Analog Front-End

The high-pass nature of the front-end can be represented by the CT equivalent of the SC front-end as shown in Fig. 3.13. Here R_s , R_i , R_{fb} , and R_{int} are the equivalent resistances of the capacitances C_s , C_i , C_{fb} clocking at f_s and C_a clocking at $f_s/8$ given in Fig. 3.12, respectively. Note that R_s and R_{fb} are shown as negative resistances because of their switching configurations.

Fig. 3.13. CT equivalent of the SC servo-loop high-pass filter based charge amplifier.

The transfer function between V_{in} and V_{out} is given by

$$V_{out}(s) = \frac{R_i}{R_s(s)} \frac{R_{int} \cdot R_{fb} \cdot C_{int} \cdot s}{R_{int} \cdot R_{fb} \cdot C_{int} \cdot s + R_i} V_{in}(s) \quad (3.6)$$

shows that the front-end circuitry has a high-pass response with a cutoff frequency of

$$f_p = \frac{R_i}{2\pi \cdot R_{int} \cdot R_{fb} \cdot C_{int}} \quad (3.7)$$

Note that due to sensor dynamics, only R_s is a function of frequency. For an electrical stimulus signal at a frequency higher than f_p , V_{out} corresponds to the ac part of the MEMS capacitance with a gain of R_i/R_s .

Also, the transfer function between V_{in} and V_{int} is given by

$$V_{int}(s) = -\frac{1}{\frac{R_i}{R_{fb}} + R_{int} \cdot C_{int} \cdot s} \frac{R_i}{R_s(s)} V_{in}(s) \quad (3.8)$$

reveals that for a static actuation, V_{int} represents the dc part of MEMS capacitance with a gain proportional to $-R_{fb}/R_s$. The magnitude response of the transfer function given in Eq. 3.6 is shown in Fig. 3.14. To maximize the frequency characterization bandwidth of the proposed method, the high-pass corner f_p has to be maintained low. This requirement is met if R_{int} , R_{fb} , and C_{int} are chosen high, and R_i is chosen small. Note that R_i is set by the gain requirement of the charge amplifier. To increase the effective resistance of the integrator R_{int} and keep the feedback capacitor relatively small, the servo feedback integrator

Fig. 3.14. The magnitude response of the SC servo-loop and the charge amplifier.

is clocked at an 8x lower frequency than the rest of the circuitry. Since the frequency response of the sensor differs with respect to the selected axis, the value of C_{fb} in the feedback path is controlled by 3-bits and controls the high-pass pole from 0.5 kHz to 2.5 kHz in 0.3 kHz increments. The dc elimination provided by servo block also helps to filter out flicker noise components and inherent readout chain offsets.

3.3.2 Analog Front-End Amplifier

A fully-differential telescopic-cascode amplifier shown in Fig. 3.15 is used as the analog front-end amplifier. A telescopic-cascode typically has higher frequency capability and consumes less power than other topologies. Its high-frequency response arises from the fact that its second pole corresponding to the source nodes of cascode devices is determined by the parasitic capacitance of only two devices instead of three, as in the folded-cascode case [33]. The main disadvantage of a telescopic-cascode amplifier is limited output swing. Since the output swing of the front-end cannot exceed 1 V, which is the maximum peak-to-peak differential input voltage to guarantee that the A/D is stable, limited output swing was not a problem in this study. Simulation results of the front-end amplifier show a typical UGF of 100 MHz with a worst-case dc gain and phase margin of 74 dB and 83°, respectively. High UGF and dc gain of the amplifier help with fast and accurate settling requirement of the SC front-end.

Fig. 3.15. Fully-differential telescopic-cascode amplifier and its CMFB circuit used for analog front-end and servo-loop amplifiers.

The common-mode feedback (CMFB) scheme uses two differential pairs. The source-coupled pairs M13-M15 and M14-M16 together sense the CM output voltage and generate an output that is proportional to the difference between output CM and V_{cm} .

Fig. 3.16. Bias current generator using an external reference voltage and a resistor, and its start-up behavior.

Reference bias currents for the DAC, the analog front-end, and the ADC are generated using an external 1.2 V reference voltage and an external resistor of 12 kOhms as shown in Fig. 3.16. The figure also shows the settling behavior during power-up for three different corners. The worst-case phase margin for the bias loop is 58°.

Fig. 3.17 below shows the V_{cm} generation using a voltage divider. This V_{cm} is buffered and used for C2V, gain and ADC blocks.

Fig. 3.17. CM generation circuitry for C2V and A/D modulator.

Fig. 3.18. The layout of the analog front-end block.

The layout of the analog front-end is given in Fig. 3.18. It occupies an area of 820 μm x 500 μm and dissipates 4 mW.

3.4 Analog-to-Digital Conversion

Depending on the operation mode, V_{out} or V_{int} is applied to the ADC to get digitized and further processed by the core signal processor. Fig. 3.19 shows the typical performance of some of the commonly used ADC topologies [34]. To synchronize the signal

Fig. 3.19. Comparison of commonly used ADC architectures regarding resolution and sampling rate.

transfer between the front-end and the ADC, the same sampling frequency is used. Targeting 9-bit resolution over a BW of 12 kHz with a sampling rate of 1 MHz, a white star indicates this region. Thus, folding ADC or delta-sigma modulator (DSM) can be selected as the ADC architecture. To maximize the signal-to-noise ratio (SNR) for the high oversampling ratio (OSR) and due to its non-stringent matching requirements compared to folding ADC, a discrete-time DSM topology is selected [35].

3.4.1 Oversampling and Quantization

Oversampling is one of the key concepts in DSMs that enhances the resolution of the system. Oversampling increases the resolution by decreasing the spectral density of the

in-band noise. Although Nyquist rate ADCs have a sampling rate twice the bandwidth of the signal of interest, oversampling converters use higher sampling rates. The OSR is defined as:

$$OSR = \frac{f_s}{2 \cdot BW} \quad (3.9)$$

where BW is the maximum input signal frequency.

3.4.2 Filtering and Decimation

Since the input is oversampled and significant quantization noise included at high frequencies, the instantaneous output of a DSM is not a meaningful representation of the input signal [36]. A better estimate of output can, therefore, be obtained by smoothing the output sequence as shown in Fig. 3.20.

Fig. 3.20. Signal chain that employs oversampling to lower quantization noise [36].

The digital filter cuts off noise outside the signal band, thereby reducing the power of the quantization noise at the output by a factor of OSR . Since $\hat{y}$ occupies the range $\pm\pi/OSR$, it can be downsampled by OSR , resulting in the sequence v_1 , which is at the Nyquist rate. The combination of the digital filter and down sampler is called the decimation filter.

3.4.3 Noise Analysis

Before discussing the implementation of A/D, noise sources impacting the BIST system resolution and accuracy must be described. These noise sources can be grouped

into three main categories: mechanical, electrical and quantization [37], [38]. Brownian motion of the MM is the primary cause of the mechanical noise, and it enters the system at the proof mass as a force generator. Electrical noise and quantization noise are primarily due to interface electronics and $\Sigma\Delta$ modulator, respectively.

3.4.3.1 Brownian Noise

The noise is a function of structural parameters of the sensor and can be represented as an equivalent acceleration white noise of [38]

$$a_n^2 = \frac{4 \cdot k \cdot T \cdot b}{(9.8 \cdot m)^2} \quad (3.10)$$

where k is the Boltzman's constant (1.38×10^{-23} J/K), T is the temperature in Kelvin, b is the damping coefficient in N/(m/s). As an example, for typical parameters of $m = 3.3 \times 10^{-12}$ kg and $b = 0.15 \times 10^{-3}$ N/(m/s), the equivalent noise force of the accelerometer under test equals 1.58×10^{-12} N/Hz^{0.5} at 300 K, corresponding to an effective input acceleration of 49×10^{-6} g/Hz^{0.5}. Eq. 3.10 shows that reducing damping coefficient or increasing mass can lower the mechanical noise floor. In most accelerometer designs, mechanical noise is not the dominant source of noise, and it has been shown that it can be reduced to 0.1×10^{-6} g/Hz^{0.5} to increase the sensitivity of the sensor [37].

3.4.3.2 Electrical Noise Sources

To quantify the effects of electrical noise, it is helpful to refer all noise sources to the sensor input. This can be accomplished in two steps. First, refer all the noise generators to the output of the charge integrator. Second, convert them to an equivalent acceleration noise through dividing by the transfer function between sensor input and charge integrator

output. For frequencies below the mechanical resonance frequency f_0 this transfer function is given by Eq. 3.1.

The noise behavior of the front-end op-amp is dominated primarily by two noise sources: thermal noise and flicker ($1/f$) noise. In many cases, the effects of $1/f$ noise may be reduced using large input devices. Also, the servo feedback method is applied to the front-end, the op-amp flicker noise is considerably reduced and can be ignored in this analysis. Op-amp thermal noise can be referred as an equivalent noise source of V_n as shown in Fig. 3.21.

Fig. 3.21. Simplified schematic view of the charge amplifier for the equivalent thermal noise calculation.

The voltage variations due to op-amp white noise are integrated onto the integrating capacitor C_i from the sense and the servo feedback capacitors, C_s and C_{fb} . The equivalent noise at the output of this circuit is [38]

$$\overline{V_{out,n}^2} = \frac{C_T}{C_i} \cdot \frac{2\pi \cdot f_u}{f_s} \cdot \overline{V_n^2} \quad (3.11)$$

where $C_T = C_s + C_{fb} + C_i + C_p$ and f_u is the unity-gain bandwidth of the amplifier. Assuming that the op-amp noise is dominated by the input transistors, Eq. 3.11 may also be written as [38]:

$$\frac{\overline{V_{out,n}^2}}{\Delta f} = \frac{16}{3} \cdot \frac{C_T}{C_i} \cdot \frac{k \cdot T}{C_{out}} \cdot \frac{1}{f_s} \quad (3.12)$$

where C_{out} is the effective load capacitance of the op-amp. Notice the noise floor at the output of the charge integrator is independent of transistor parameters. This noise can be lowered by increasing sampling frequency, load or integrating capacitance.

The kT/C noise is generated by thermal noise sampling of the switches. The equivalent kT/C noise at the output of charge integrator due to front-end amplifier can be expressed as:

$$V_{kT/C}^2 = \underbrace{\frac{4 \cdot k \cdot T}{f_s \cdot C_s}}_{\text{Input Noise Density}} \cdot \left(1 + \frac{C_{fb}}{C_s}\right) \cdot \underbrace{\left(\frac{C_s}{C_i}\right)^2}_{\text{Gain}^2} \quad (3.13)$$

The equation indicates that the noise can once again be lowered by increasing f_s or C_i and reducing C_{fb} . Note that a similar noise source exists at the input of A/D, and sampling capacitor must be sized such that the input SNR is not degraded.

3.4.3.3 Quantization Noise

In an A/D system, the error caused by quantization must be considered. In a quantizer that operates at Nyquist rate, the rms value of the error is given in equation

$$e_{rms}^2 = \frac{\Delta^2}{12} \quad (3.14)$$

where Δ is the quantization level spacing. Therefore, the quantization error lies between $\Delta/2$ and $-\Delta/2$, and have an equal probability of taking any value in between. If the quantizer input stays within the input range of the quantizer, and changes by large amounts from sample to sample so that its position within a quantization interval is random [36], the noise power inside the signal bandwidth for an oversampling quantizer is given by

$$e_{rms}^2 = \frac{\Delta^2}{12 \cdot OSR} \quad (3.15)$$

Conceptually, oversampling provides resolution in time, instead of resolution in amplitude. Resolution in amplitude can be obtained after decimation. Note that, doubling the sampling frequency improves the SNR caused by quantization noise by only 3 dB. Thus, oversampling alone does not improve the resolution of the system as desired.

3.4.3.4 Noise Shaping

Noise shaping property is the primary purpose of usage of delta-sigma modulation. Consider the first order DSM shown in Figure Fig. 3.22.

Fig. 3.22. A simple negative-feedback amplifier with one sample delay [36].

By inspection, we have

$$V(z) = \underbrace{\left(\frac{A}{1 + Az^{-1}} \right)}_{\text{SignalTransferFunction (STF)}} U(z) + \underbrace{\left(\frac{1}{1 + Az^{-1}} \right)}_{\text{Noise TransferFunction (NTF)}} E(z) \quad (3.16)$$

As $A \rightarrow \infty$, the *STF* approaches unity, while the *NTF* tends to zero. Therefore, the quantization noise is shaped and carried to higher frequencies. Hence, in-band noise power of the system is lowered by using a DSM compared to an oversampling quantizer. Equivalent in-band quantization noise for a $\Sigma\Delta$ modulator can be expressed as [37]:

$$V_q^2 = \left[\frac{\pi^L}{\sqrt{2L+1} OSR^{L+0.5}} e_{rms} \right]^2 \quad (3.17)$$

where L is the order of the modulator, and e_{rms} is given in Eq. 3.14. The above equation shows that, as the order of the DSM increases, the more quantization noise is carried to high frequencies and the less in-band quantization noise is observed.

The discussion above presents the individual noise components and their expressions. As Eq. 3.10 shows, the mechanical noise depends on the sensor parameters. Also, most of the electrical noise sources are a function of sampling frequency f_s and the value of integrating capacitance C_i . It is possible to lower the total electrical noise by increasing f_s and C_i . However, circuit parameters such as slew rate and unity gain bandwidth of the amplifiers put an upper limit on the sampling frequency. Even though increasing the integrating capacitance reduces the absolute voltage noise, it lowers the sensitivity of the front-end charge amplifier. Thus, the sampling rate and integrating capacitance should be optimized to obtain desired dynamic range and resolution.

Table 3.1. Summary of the mechanical and electrical noise components referred to the modulator input and their expected spectral density values.

Noise Source	Expression	Value $\left[\frac{V^2}{Hz} \right]$	Value $\left[\frac{dBV_{rms}}{Hz} \right]$
Brownian Noise	$\left(a_n \times \frac{\Delta V}{\Delta A_{in}} \right)^2 \times A_{pre\_amp}^2$	0.22 E-9	-96.5
Front-End Amplifier	$\frac{16}{3} \times \frac{C_T}{C_i} \times \frac{kT}{C_{out}} \times \frac{1}{f_s} \times A_{pre\_amp}^2$	2.78 E-12	-115.6
kT/C	$\frac{4kT}{f_s C_s} \times \left(1 + \frac{C_{fb}}{C_s} \right) \times \left(\frac{C_s}{C_i} \right)^2 \times A_{pre\_amp}^2$	0.21 E-10	-106.8
Quantization	$\left(\frac{\pi^2}{5^{0.5} OSR^{2.5}} \times e_{rms} \right)^2$	0.25 E-10	-106.0

* $C_T = C_s + C_{fb} + C_i + C_p = 0.34 + 0.3 + 0.1 + 1.5 = 2.24$ pF, C_{load} = Sampling Cap of Pre-Amp = 3.6 pF, $A_{pre\_amp} = 4.5$, Quantization noise calculation assumes an input signal at 3.1 kHz.

Individual noise components referred to the input of modulator as well as the quantization noise of the modulator are summarized in Table 3.1. As seen from the table, mechanical Brownian noise is the dominant noise source for the proposed application and since it solely depends on the device parameters, lowering the mechanical noise is not under our control. However, electrical noise sources can be controlled mainly by choosing proper f_s , C_i , and C_s values.

Table 3.2 below shows the key sensor parameters that can be used to calculate the equivalent acceleration due to an electrical stimulus and the noise acceleration due to Brownian noise as well as electrical noise sources. From Eq. 2.4, expected rms acceleration a_e is 4.13 g. Also, the spectral density of Brownian noise for the sensor under test is calculated as $49 \times 10^{-6} \text{ g/Hz}^{0.5}$.

Table 3.2. Parameters of the three-axes capacitive MEMS sensor integrated with the BIST IC.

Typical Sensor Parameters	x-axis y-axis	z-axis
Movable Mass (m)	3.3 ng	8.7 ng
Natural Frequency (f_0)	5.1 kHz	3.2 kHz
Damping Coefficient (b)	0.15 mN/(m/s)	0.49 mN/(m/s)
Sense Capacitor Gap (d)	1.6 μm	1.6 μm
Sense Plate Area (A)	6e-8 m^2	6e-8 m^2
Sense Capacitor (C_s)	340 fF	320 fF
Integrating Capacitor (C_i)	100 fF	100 fF
Common-Mode Voltage (V_{cm})	1.65 V	1.65 V

Integrating this noise over 12 kHz results in 5.4×10^{-3} rms noise acceleration. Note that the noise calculation does not include electrical noise sources or substrate noise. Thus,

expected the best-case SNR is 57.7 dB. Since peak signal-to-quantization noise (SQNR) of a 1st order 1-bit modulator for an OSR of 41.7 is below 50 dB, a 2nd order DSM is selected.

3.4.4 Circuit Implementation

Cascade of Integrators Feedback (CIFB) architecture with single-bit quantizer is selected for ease of application. A generic block diagram of 2nd order DSM with CIFB topology is shown in Fig. 3.23. Using Matlab sigma-delta toolbox and the specifications given in Table 3.2, we can get the following coefficient values [35]:

$$a = [0.2112, 0.1334], g = 0, b = [0.2112, 0, 0], c = [0.1763, 5.81]$$

Fig. 3.23. Typical second-order CIFB modulator structure [36].

Among these, all coefficients except c_2 will translate into capacitor ratios. The coefficient c_2 turns out to be unimportant, since 1-bit quantizer merely cares about the sign of its input, and c_2 is positive. To implement capacitance ratios simpler, the coefficients are adjusted as follows:

$$a = [1, 1], g = 0, b = [1, 0, 0], c = [0.4, 0.5]$$

Table 3.3 summarizes important design specifications of the modulator.

Table 3.3. Specifications summary of the A/D modulator.

A/D Design Parameters	Specification
Sampling Frequency	1 MHz
Signal Bandwidth	12 kHz
Power Supply	3.3 V
Modulator Architecture	CIFB
Order of Modulator	2
Number of Bits in Quantizer	1-bit
Input Full Scale Range	1 V _{p-p} differential
Integrator Swings	± 1 from V _{cm}
Power and Area	Not stringent

3.4.4.1 Sampling Capacitors and Switches

The thermal noise constraint determines the absolute values of the sampling capacitor C_s and feedback capacitor C_{fb} of the first integrator. Here thermal noise contribution of the second integrator is ignored due to a high in-band gain of the first integrator. Both the switch resistance and the amplifier contribute to the input referred noise. However, if $g_m \gg (1/R_{on})$, where g_m is transconductance of the first integrator amplifier, and R_{on} is on-resistance of the sampling switches, noise contribution of op-amp can be neglected [39]. The mean square noise voltage yielding an SNR of 60.7 dB (57.7 dB plus 3 dB margin) relative to the power of a full-scale ($V_p = 0.5/2$) sine-wave is

$$V_n^2 = \frac{V_p^2 / 2}{10^{SNR/10}} = \frac{0.25^2 / 2}{10^{60.7/10}} = 2.66 \times 10^{-8} \text{ V}^2/\text{Hz} \quad (3.18)$$

The in-band input-referred mean-square noise voltage associated with the first integrator is approximately [36]

$$V_n^2 = \frac{4 \cdot k \cdot T}{OSR \cdot C_s} \quad (3.19)$$

Equating Eq. 3.18 to 3.19 yields $C_s > 15$ fF. To improve noise margin and matching, $C_s = 400$ fF is chosen. Thus, C_{fb} is equal to 1 pF.

Fig. 3.24. (a) Block level diagram of the second-order discrete-time MEMS readout $\Sigma\Delta$ modulator and (b) Schematic view of the implemented second-order modulator.

Fig. 3.24 shows the implementation of the second-order discrete-time single-loop delta-sigma modulator.

3.4.4.2 Integrator Amplifier Gain Requirement

The transfer function of a delayed (non-inverting) SC integrator with an ideal amplifier is given by

$$\frac{V_o(z)}{V_i(z)} = \frac{C_s}{C_{fb}} \frac{z^{-1}}{1-z^{-1}} \quad (3.20)$$

Here as expected, integrator's pole is located at $z_p=1$, and the dc gain is infinite. The same transfer function with a finite gain amplifier is defined by

$$\frac{V_o(z)}{V_i(z)} = \frac{C_s / C_{fb}}{\left(1 + \frac{1}{A}\right) \cdot (1 + \varepsilon)} \frac{z^{-1}}{\left(1 - \frac{1}{1 + \varepsilon} z^{-1}\right)} \quad (3.21)$$

where A is the dc gain of the amplifier. Here ε is represented by

$$\varepsilon = \frac{C_s}{C_{fb} \cdot (A + 1)} \quad (3.22)$$

We can see that finite amplifier gain has two effects: a small reduction in the integrator's gain constant and inward shift of the integrator's pole ($z_p \approx 1 - \varepsilon$). Thus, the *NTF* gain at dc changes from its ideal value of zero, and the modulator loses its ability to achieve infinite precision with dc signals [36]. There exists a dead band around $V_i = 0$, and it results in a minimum amplitude being present at the modulator input before it can generate the least significant bit (LSB). The width of the dead zone is proportional to $1/A^2$ for a second-order modulator, and the worst dead band is usually associated with the output pattern $\{+1, -1\}$ [36]. For the modulator presented, the feedback pattern produces a periodic sequence $x_2 = \{+1.32 \text{ V}, -1.32 \text{ V}\}$ at the output of the second integrator. In order to resolve, say, a $15 \mu\text{V}$ input, the required dc gain

$$A > \sqrt{\frac{1.32}{15\mu}} = 49.4 \text{ dB} \quad (3.23)$$

3.4.4.3 Integrator Amplifier Unity Gain Bandwidth and g_m Requirements

The UGF of the amplifier decides how fast amplifier settles and it is given by

$$UGF = -\frac{\ln(x/100)}{2\pi \cdot \beta \cdot t} \text{ Hz} \quad (3.24)$$

where x is the settling accuracy in % LSB, β is the feedback factor, t is the settling time.

For $x = 0.1\%$, $\beta = 0.72$, and $t = 250$ ns, UGF results in 6.8 MHz.

The g_m of the amplifier is a function of the effective loading capacitor C_L , and since the integrator is an SC circuit, it varies with the clocking phase. Fig. 3.25 displays the loading situation for both clock phases. According to that, the worst-case C_L is calculated as 685 fF. Here a parasitic capacitance of 200 fF is assumed at the input of the amplifier.

Fig. 3.25. Loading conditions of the integrator amplifier for both sampling and integration phases [35].

Assuming UGF of 10 MHz and C_L of 700 fF, the required g_m is

$$g_m > 2\pi \cdot C_L \cdot UGF = 44 \times 10^{-6} \text{ (1/Ohms)} \quad (3.25)$$

But to lower the noise contribution of the first integrator op-amp compared to the noise of the switch, $g_m \gg (1/R_{on})$ must be satisfied as mentioned before. In other words, g_m is decided by the noise requirement other than the bandwidth requirement or the value of C_L . Here the sampling switch on-resistance is selected as 12.5 kOhms. Therefore, g_m should be set to a value greater than 400 μ S.

on or off and they just offer small resistance along the signal path. Since the sampling frequency is 1 MHz, chopping frequency of 500 kHz is selected. Note that chopping clock must be non-overlapping.

‘Chop 1’ shown in Fig. 3.27 modulates the input signal to 500 kHz. At this point, offset and $1/f$ noise are located at low frequency, but the signal sits around 500 kHz. Thus, offset and $1/f$ noise do not mix with the signal. After ‘chop 2’, the signal at 500 kHz is down-converted to baseband and offset and $1/f$ noise is pushed to 500 kHz. Therefore, applying a low-pass filter to the output of the amplifier eliminates the offset and $1/f$ noise caused by the OTA. ‘Chop 3’ is added to reduce the current mirror mismatch between M9 and M10 transistors.

Fig. 3.27. Folded-cascode amplifier with chopper switches [35].

‘Chop 3’ is added to reduce the mismatch between current mirror transistors M9 and M10. Chopper switches are added to lower voltage glitches during the non-overlapping time of chopping clock. These glitches if not removed increases the residual offset after chopping. Fig. 3.28 shows the structure of chopper modulator and demodulator. Large transistor sizes should be avoided to reduce clock feed-through and charge injection.

Fig. 3.28. Chopper modulator and demodulator [35].

An SC CMFB as shown in Fig. 3.29 is used for the amplifier. The main advantages of SC CMFBs are that they impose no restrictions on the maximum allowable differential signals, have no additional parasitic poles in the CM loop, and are highly linear [40]. Switches are implemented as T-gates.

Fig. 3.29. SC CMFB circuit used for the amplifier [35].

Due to its inherent linearity, a simple single-bit quantizer is used. Higher order quantizers are more complex, and resulting DACs might suffer from mismatches and non-linearity. Here, the comparator is shown in Fig. 3.30 serves as a single-bit quantizer. Most comparators have cross-coupled structure. In this case, M3-M4-M7-M8 form cross coupling. M1 and M2 should be strong enough to overwrite the previous bit. Increasing M1 and M2 increases voltage kick back to the input. Therefore, care must be taken not to oversize or undersize the input transistors M1 and M2. The sizes of M3-M4-M7-M8 determine the speed of regeneration [35].

Fig. 3.30. Comparator circuit serves as a one-bit quantizer for the modulator [35].

The clock generator that accomplishes non-overlapping clock signals is realized with a simple circuit constructed of logic gates and is displayed in Fig. 3.31. The generator produces 8 clock phases. In this circuit, the non-overlap and delay times can be controlled by adjusting the number of inverters. Here 10x inverters are used to generate complementary signals. This ensures that crossing of signal and its complement happens near mid-supply. Capacitors can be inserted on intermediate nets to control the delay further. Fig. 3.32 shows the generated non-overlapping clock phases. A non-overlapping time of ~23ns is used.

Fig. 3.31. Non-overlapping clock generator utilized for the front-end and modulator blocks [35].

Fig. 3.32. Non-overlapping clock phases [35].

3.4.4 Analog-to-Digital Converter Simulation Results

Input referred noise of modulator both with and without chopping technique is given in Fig. 3.33. ‘No chopping’ curve shows the dominance of $1/f$ noise in the bandwidth of interest. Total integrated noise over 13 kHz bandwidth for chopped and no chop case is 0.2mV and 2.4mV, respectively.

Fig. 3.33. Modulator input-referred noise w/ and w/o chopping [35].

RC extracted post-layout PSD result of the modulator for a 6 kHz, 1 V_{pp} input signal is given in Fig. 3.34. SNDR of 60 dB and offset of ~1mV is achieved as targeted.

Fig. 3.34. PSD at modulator output for 1 V_{pp} differential input (post layout R+C+CC extracted) [35].

SNDR as a function of input signal power is displayed in Fig. 3.35. Here 0 dB corresponds to full-scale, which is 1 V_{pp} differential input. SNDR peaks to almost 63 dB at +2 dB full-scale and drops by -3 dB from peak SNDR at +3.1 dB. In other words, this modulator can handle +3.1 dB over the full-scale range (FSR) before SNDR starts reducing drastically. SNDR starts decreasing for amplitudes exceeding FSR because the optimal quantizer gain decreases and degrades the noise-shaping. The minimum signal that modulator can detect will be its thermal noise.

Fig. 3.35. Modulator SNDR as a function of input signal power [35].

3.4.5 Analog-to-Digital Converter Layout

A/D system contains both analog and digital blocks. Digital blocks such as non-overlapping clock generator may produce lots of supply, ground and substrate noise. In order not to degrade the performance of analog blocks, digital power domain should be well isolated from analog power. Fig. 3.36 shows the layout of the modulator. It occupies an area of 0.2 mm² and dissipates 2.5 mW.

Fig. 3.36. The layout of the $\Sigma\Delta$ modulator.

CHAPTER 4

SIGNAL EXTRACTION

4.1 Introduction

Given that the displacement due to electrical excitation is much smaller than the gap between conducting plates, the MEMS system can be linearized around its operating point. Thus, for an electrical stimulus signal of $\sin(2\pi f_{int}t)$, the MEMS sensor responds with $A_c \sin(2\pi 2f_{int}t + \emptyset)$. Here the amplitude and phase responses are represented by A_c and $\emptyset$, and their values depend on the capacitance variation due to stimulus signal and the resonance frequency of the device, respectively. In addition to sensor response, A/D output yields an interfering signal of $A_{int} \sin(2\pi f_{int}t)$ due to capacitive coupling between the excitation and readout plates. Here A_{int} is the amplitude of this interfering signal, and it depends on the excitation frequency. Thus, the amplitude extraction technique must be immune to the amplitude of the interference signal. Note that the interference signal does not experience any phase shift with frequency.

The statistical model of the developed BIST-based calibration method requires that the response of the sensor amplitude and phase information, A_c and $\emptyset$, is measured. Spectral analysis of the A/D output through fast Fourier transform (FFT) can be a straightforward solution for extracting phase and amplitude response of the MEMS device. However, the computational cost makes FFT ineffective as a self-testing and calibration method for sensor applications. Fig. 4.1 shows the block diagram of the all-digital amplitude and phase extraction technique used in this study.

Fig. 4.1. Block diagram of the proposed all-digital amplitude and phase extraction method.

4.2 Amplitude Extraction

The single-bit $\Sigma\Delta$ A/D output is first followed by a decimation filter to generate V_{dec} , which has a sampling rate of 31.25 kSps. The significant signal components at the output of decimation filter following the $\Sigma\Delta$ ADC are given as:

$$V_{dec}(nT_s) = A_c \sin(2\pi 2f_{in} nT_s + \phi) + A_{int} \sin(2\pi f_{in} nT_s + \phi) + v_n \quad (5.1)$$

where T_s is equal to $32 \mu s$. Here v_n is the total sampled in-band noise voltage. Since the MEMS sensor is stimulated with a known amplitude and phase electrical stimulus signal, synchronous amplitude detection is used to provide increased resistance to noise and interference. The mathematical operations applied during amplitude extraction are given in

$$A_c = \text{avg} \left\{ \max \{ |V_{dec}(nT_s)| \} \times \sum_{k=-\infty}^{k=+\infty} \delta \left(n - k \frac{T_{in}}{4} \right) \right\} \quad (5.2)$$

where $T_{in} = 1/f_{in}$ and $\text{avg} \{ \}$ is the time averaging operator, $\max \{ \}$ is the maximum selector, $V_{dec}(nT_s)$ represents the decimated ADC output and $\delta(n)$ is the Fermi-Dirac function,

representing impulse sampling of the full-wave rectified signal. First, the MEMS response signal is rectified for peak detection. Noting that rectification doubles the frequency content in the response signal, its peaks are sampled at $4f_{in}$, which guarantees only the sensor response to electrical excitation will be down-converted to dc. Next, an averaging filter is applied to suppress high-frequency components generated due to sampling and reduce the in-band thermal noise power. The method also ensures that the spurious signals due to DAC clock are filtered out. Depending on the required accuracy of amplitude extraction method, the number of points during averaging can be increased although this will raise the test and calibration time.

4.3 Phase Extraction

The phase information at a given frequency is embedded into the average of the DAC clock and sensor response multiplication. To minimize AM noise impacting phase mode noise, and ease numerical mixing operation, the response signal first goes through a hard limiter. In the case of $\phi \leq 180^\circ$, this average phase information V_{ph} is given in

$$V_{ph} = \text{avg}\{V_{dac}(t) \times V_{res}(t)\} = 1 - \frac{4\tau}{T_{in}} \quad (5.3)$$

where $\tau = (\phi / 2\pi) \times (T_{in} / 2)$. As shown in Fig. 4.1, V_{res} and V_{dac} are the input signals to the multiplier, and they represent the processed sensor response and DAC output, respectively. Using the relationship between τ and ϕ , one can find the phase response of the device ϕ in rad as:

$$\phi = -(V_{ph} - 1) \times \pi \quad (5.4)$$

The stimulus frequency at which the phase shift is $\pi/2$ is called the electrical resonance frequency of the device. The electrical resonant frequency is lower than the mechanical resonant frequency due to electrically induced negative stiffness k_{elc} given in Eq. 5.5.

$$k_{elc} = V^2 \frac{\epsilon A}{d^3} \quad (5.5)$$

Eq. 5.5 indicates that there is a square-law relationship between V and k_{elc} . It is imperative to note that the developed statistical model does not require the actual value of the resonance frequency, but the phase shift caused by the device at frequencies close to the resonance frequency. It is true that this phase shift is highly correlated with the mechanical resonance frequency of the device.

4.4 Offset Extraction

The BIST IC can measure the sensor offset in two different ways. In normal readout mode servo integrator output V_{int} is proportional to $C_{s1} - C_{s2}$. Thus, measuring this node when the device is stationary yields the offset information V_{off} . However, this voltage depends on the absolute value of C_{fb} so it can be as good as process variations. Electrical stimulus based BIST mode can also be used to extract the device offset. For a device with non-zero static offset, the amplitude of capacitance variation depends on the stimulus plate. Thus, the offset information lies within the ratio of amplitude readings taken from different plates, A_{ratio} . This technique yields more accurate results because it is ratio-based and independent of the gain variations of the signal chain.

CHAPTER 5

SYSTEM LEVEL SIMULATION AND EXPERIMENTAL RESULTS

5.1 Simulation Setup and Results

To evaluate the correlation between electrical and mechanical characteristics as well as the effectiveness of the proposed sensitivity prediction method, first, the linear regression technique has been practiced on 600 distinct sensor models. The population of 600 devices was generated with typical dispersions applied on k , m and d_{off} values of the sensing device. Here the average values of k , m and d_{off} for the training devices are 3.5 N/m, 3.3×10^{-12} kg and 0 μ m, respectively. The simulations were performed in the CADENCE environment using a sensor model implemented in Verilog-A. The model describes the translation motion of a damped mechanical system caused by either a physical acceleration of a or an excitation voltage of V by implementing the equations given in Eq. 2.2 and Eq. 2.4. The code also models the mechanical noise due to the Brownian motion of the MM. Capacitance and mechanical sensitivity measurements were taken at 0 g and $\pm$ 8 g, respectively.

Table 5.1 summarizes the % rms error in sensitivity prediction for randomly chosen 100 devices with respect to a different number of training set sizes. The error for the no training case is calculated assuming the predicted sensitivity is the average sensitivity of the training device set. Apparently, having a higher number of devices in the training set provides a better snapshot of process variations and thus better prediction accuracy. However, even several hundred devices suffice to achieve a good estimate of the sensitivity. It is also observed that in the case of training with a single parameter, f_0 is more effective than

Table 5.1. RMS error in sensitivity prediction as a function of training size.

Training Set Size	% RMS Error In Sensitivity Prediction					
	No Training	Information Used In Learning Phase				
		Offset	$\left(\frac{C_{s1}+C_{s2}}{2}\right)_{0g}$	f_0	$f_0, \left(\frac{C_{s1}+C_{s2}}{2}\right)_{0g}$	$f_0, \left(\frac{C_{s1}+C_{s2}}{2}\right)_{0g}, \text{Offset}$
100	7.83	7.83	7.53	6.40	1.19	1.07
200	7.72	7.70	7.42	6.35	1.17	1.06
300	7.59	7.56	7.33	6.25	1.15	1.04
400	7.57	7.55	7.31	6.24	1.14	1.03
500	7.56	7.54	7.29	6.23	1.11	1.00

capacitance and offset information. As seen in the last column, if all three parameters are used for training purposes the sensitivity error can be lowered from 7.56% to 1.00%.

Fig. 5.1 shows the progression of error for the sensitivity prediction after each measurement for 100 randomly picked sample device instances. Here, the training set size is 500. The largest improvement in error is achieved when both f_0 and average of C_{s1} and C_{s2} information are included in the statistical model as we have concluded before.

Fig. 5.1. Progression of prediction error after each measurement.

Next, the top-level simulations of the proposed BIST IC together with 100 sensor models were performed. The ac measurements were collected at one very low-frequency f_{low} , and one at relatively higher frequency f_{high} in a stationary position. The absolute values of the frequencies depend on the f_0 of the sensor under test. To characterize both of the sense capacitors C_{s1} and C_{s2} , the excitation signal has been applied to both of the fixed plates. Mechanical sensitivity measurements were taken at ± 1 g. Table 5.2 summarizes the measurements taken for a given device mode and their relations to the parameters used in the statistical model.

Table 5.2. Measurements for each device mode and their interpretations in the statistical model.

Device Mode	Measurement Node	Measured Parameters	Extracted Parameters
Electrical stimulus based BIST mode	V_{out}	A_{low_x1}, A_{low_x2}	$A_{low} = \frac{A_{low\_x1} + A_{low\_x2}}{2}, A_{ratio} = \frac{A_{low\_x1}}{A_{low\_x2}}$
		A_{high_x1}, A_{high_x2}	$A_{high} = \frac{A_{high\_x1} + A_{high\_x2}}{2}$
		$\phi_{high\_x1}, \phi_{high\_x2}$	$\phi_{high} = \frac{\phi_{high\_x1} + \phi_{high\_x2}}{2}$
	V_{int}	V_{int_0g}	$V_{off} = V_{int\_0g}$
Functional readout mode	V_{int}	$V_{int\_+1g}, V_{int\_ -1g}$	$S = \frac{V_{int\_+1g} - V_{int\_ -1g}}{2}$

For example, A_{low_x1} and ϕ_{high_x2} correspond to the amplitude, and the phase shift for low and high-frequency stimulus signals applied to x1 and x2 fixed plates, respectively. To keep the simulation duration minimal, f_{low} and f_{high} are chosen as 0.5 kHz and 2 kHz, respectively.

The linear regression method has been practiced on 90 sensors for the learning purposes and 10 sensors for the test purposes. This process has been repeated, and the entire population of 100 devices was characterized. Fig. 5.2 shows the actual and predicted sensitivities of the total population.

Fig. 5.2. Sensitivity prediction performance of the proposed BIST IC using simulation results.

According to this, the proposed method achieved 1.24% rms error in the mechanical sensitivity prediction. The increase in predicted sensitivity error from 1.00% to 1.24% is thought to be the result of less number of devices used in training process and the contribution of BIST IC.

5.2 Experimental Setup and Results

A die photo of the standalone BIST IC and together with the sensor is given in Fig. 5.3. Although the entire chip occupies 4.5 mm^2 on a single-poly, 6LM $0.18\text{-}\mu\text{m}$ CMOS process, the BIST circuitry including the front-end, the internal DAC, and the $\Sigma\Delta$ modulator only employs 1.0 mm^2 silicon area. The center of the BIST chip is intentionally left unused to reduce the possible interference between the sensor and the highly sensitive electronics. The chip consumes 8.9 mW of power while running at a speed of 1 MHz.

Fig. 5.3. (a) The die photograph of BIST IC and (b) The die photograph of the inertial sensor and BIST IC.

The experimental setup and the procedure for the measurements are displayed in Fig. 5.4. A USB interface is used to control the device mode, excitation plates, the gain, and the high-pass pole of the front-end. Correct phase shift measurements are guaranteed by triggering all the devices at the beginning of the stimulus cycle. The excitation frequencies f_{low} and f_{high} are chosen to be 0.35 kHz and 1.55 kHz, respectively. Each measurement is made four times and averaged to increase SNR. The amplitude and phase extraction is performed by capturing 25 cycles of the sensor response. Remembering that the sensor response exists at $2f_{in}$ and stimulus is applied to both x1 and x2, the total test duration for BIST mode is 87.5 ms. The linear regression technique has been practiced on 45 fabricated devices during experiments.

of 45 devices with a mean value of 67.4 mV/g, which is only 0.7% higher than the calculated mechanical sensitivity. The worst-case measured sensitivity is 3.1% greater than the calculated value. Notice that the red line displayed in Fig. 5.5 is a normal density function fit to the sensitivity distribution.

One of the independent parameters used in the model given in Eq. 2.7 is V_{off} . If it is measured in the stationary position, V_{int} will be equal to V_{off} , and it will represent the device offset. That is because V_{int} is proportional to ΔC_s , the difference between C_{s1} and C_{s2} . As mentioned in the offset extraction section, to reduce the number of measurements and to increase the accuracy, another parameter that is highly correlated with V_{off} , called A_{ratio} , is defined as in Table 5.2. Fig. 5.6 plots the relationship between V_{off} and A_{ratio} . As the

Fig. 5.6. The relationship between the servo integrator output voltage V_{int} , and A_{ratio} .

figure shows, there is a high correlation between the parameters, and therefore A_{ratio} will be used to represent the device offset in the statistical model. Note that when A_{ratio} crosses 1, V_{int} depicts voltage values close to 0 V since it is related to the difference between C_{s1} and C_{s2} .

Fig. 5.7 displays the scatter plot of the actual and the predicted mechanical sensitivities of the fabricated devices.

Fig. 5.7. Sensitivity prediction performance of the proposed BIST IC using measurement results. The proposed BIST method achieved 0.55% rms error in predicting the mechanical sensitivities of the fabricated devices using electrical-only measurements. More than half of the predicted sensitivities resides within $\pm 0.5\%$ range with a worst-case prediction error of 1.26%. The results support the high correlation between the electrical parameters (i.e., frequency response and offset) and the sensitivity of the capacitive MEMS accelerometers. Note that the red lines shown in Fig. 5.2, 5.6, and 5.7 are the least-squares lines superimposed on the scatter plots.

Fig. 5.8 illustrates the % error progression for the mechanical sensitivity prediction after each measurement added to statistical model during the learning phase. Here A_{low} , A_{high} and ϕ_{high} are defined as shown in Table 5.2. As shown in Fig. 5.8, until the last data point A_{ratio} , each measurement lowers the sensitivity prediction error. The reason why we do not

Fig. 5.8. Progression of prediction error after each measurement.

see any improvement for the last data set is the fact that the offset information is already embedded to previous measurements since A_{low} , A_{high} , and $\emptyset_{high}$ are the averages of the two readings taken from both fixed plates. Therefore, the offset measurement or A_{ratio} does not contribute as useful information and can be eliminated from the statistical model.

Fig. 5.9(a) shows 2.7 V_{pp}, 1 kHz original sinusoidal excitation signal generated by the BIST circuit, which is applied to a fixed excitation plate of a typical MEMS device. The first thing to note is that the instrument response, given in Fig. 5.9(b), is at twice the excitation frequency, at 2 kHz due to the square-law relationship between electrical force F_e and stimulus signal V as given in Eq. 2.4.

Fig. 5.9. (a) 2.7 V_{pp}, 1 kHz measured sinusoidal excitation signal generated by the BIST circuit (b) Measured time-domain response of a typical MEMS device at 2 kHz and 4 kHz and (c) The DAC clock and measured hard-limited device response at 2 kHz used for phase extraction.

Also, the reaction of the same device to a 2 kHz signal generates a smaller voltage swing due to frequency-dependent amplitude response of the accelerometer. Note also that, because of the high-pass nature of the front-end, both signals are ac-coupled. Finally, Fig. 5.9(c) displays the phase shift between the DAC clock and the hard-limited device response at 2 kHz. The product of these signals results in the phase information at 1 kHz.

Fig. 5.10 displays the measured spectrum of V_{out} taken from the 2nd order $\Sigma\Delta$ ADC output for an electrical stimulus signal at f_{in} of 1.55 kHz. As the figure shows, the output spectrum includes the MEMS response at $2f_{in}$. The amplitude of the response signal approximately corresponds to -3 dBFS because the modulator full-scale input range is 1 V_{p-p} (-15 dBV_{rms}). Note that the output also yields the excitation signal and its odd harmonics

Fig. 5.10. Measured spectrum for electrical excitation at 1.55 kHz.

due to capacitive coupling between the stimulus (x1) and readout (x2) plates. In addition, the measured noise floor is quite close to the calculated noise floor of $-96.5 \text{ dBV}_{\text{rms}}/\text{Hz}$.

CHAPTER 6

CONCLUSION

A physical-stimulus-free low-overhead BIST IC for capacitive MEMS accelerometer testing and sensitivity prediction purposes is presented. The circuitry includes three main blocks: a sine-weighted resistor string DAC, a C2V with a multi-rate servo feedback based dc-blocking, and a second-order discrete time $\Sigma\Delta$ ADC. The on-chip DAC stimulates the sensor to mimic the action of an inertial force caused by a physical acceleration. The C2V generates the output voltage corresponding to the capacitance variation caused by the stimulus. The amplified C2V output is applied to ADC to get digitized and further processed by the core signal processor. The proposed approach measures the amplitude and phase characteristics of capacitive MEMS accelerometers to predict mechanical sensitivity. The method offers sensitivity prediction by developing a low computational complexity multi-variate linear model between electrical and mechanical characteristics of the inertial sensor during the learning phase. According to experimental results of the test phase, 0.55% rms error in mechanical sensitivity prediction is achieved. The BIST IC circuitry consumes 8.9 mW and occupies 1.0 mm² on a 0.18- μ m CMOS process. Overall, the technique offers a good potential to guarantee acceptable fault coverage and a capability for calibration of capacitive accelerometers in production. Also, it can be used to perform in-field testing and calibration to adopt environmental changes.

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